

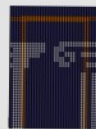
Task 2: Modeling and Simulation of Conducted and Radiated EMI from HPM and UWB Sources on PCBs and ICs

A. C. Cangellaris and E. Michielssen

ECE Department

Center for Computational Electromagnetics

University of Illinois at Urbana-Champaign



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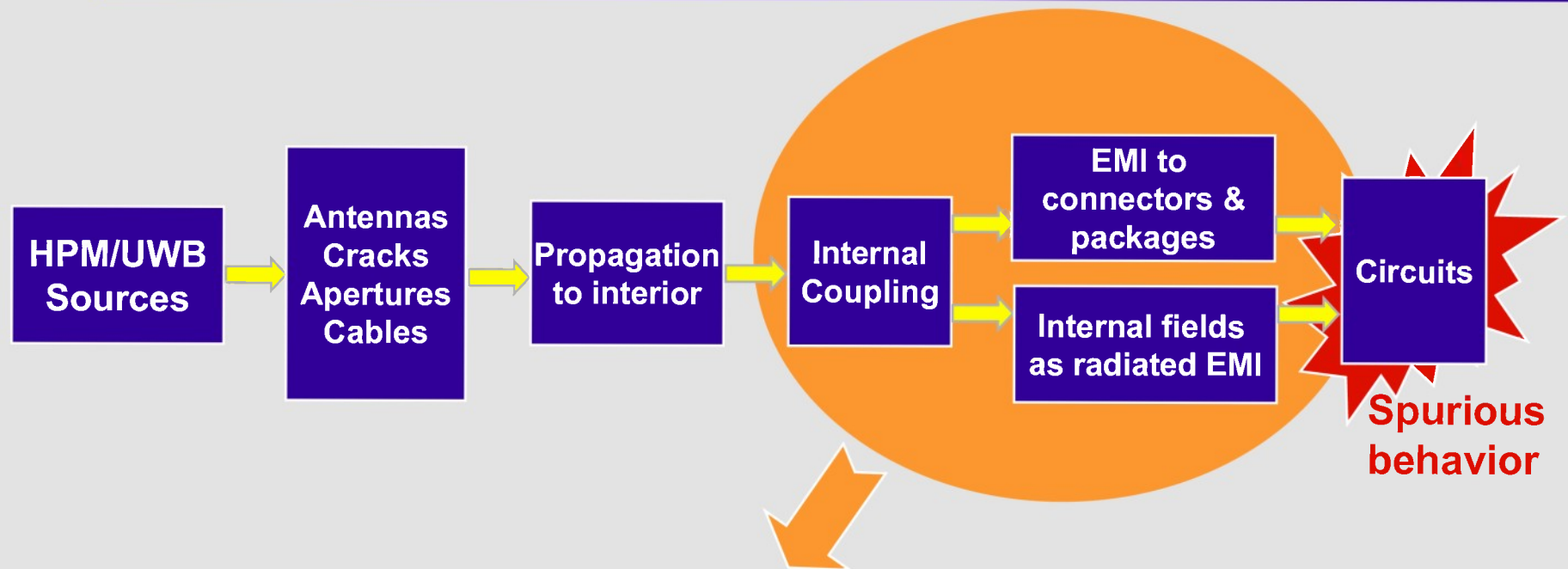
Report Documentation Page

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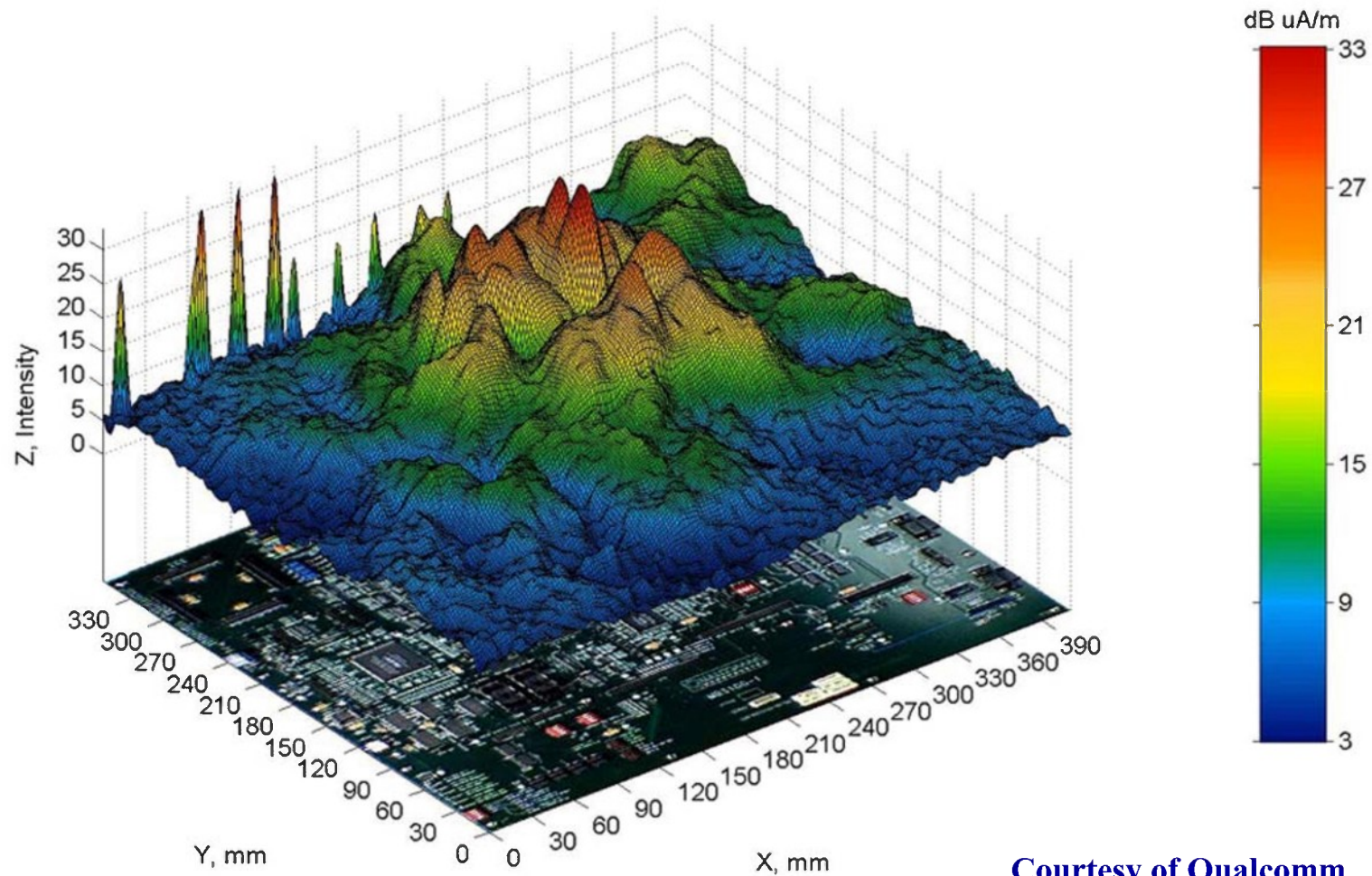
Objective



- Accurately “propagate” the spurious signals (noise) through the packaging hierarchy (printed circuit boards, cards, connectors, interposer, package...) to the die.



Major Obstacle: Tackling System Complexity



Courtesy of Qualcomm



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System Complexity translates to EM Complexity

■ EM Complexity

- Geometric complexity and distributed nature of the packaging hierarchy (“coupling path”)
- Broad frequency bandwidth of the interfering signal
- Non-linearity of the terminations

■ Tackling Complexity

- Hierarchical approach to the modeling of electromagnetic interactions
 - From lumped models, to transmission-line models, to quasi-3D full-wave models, to 3D full-wave models

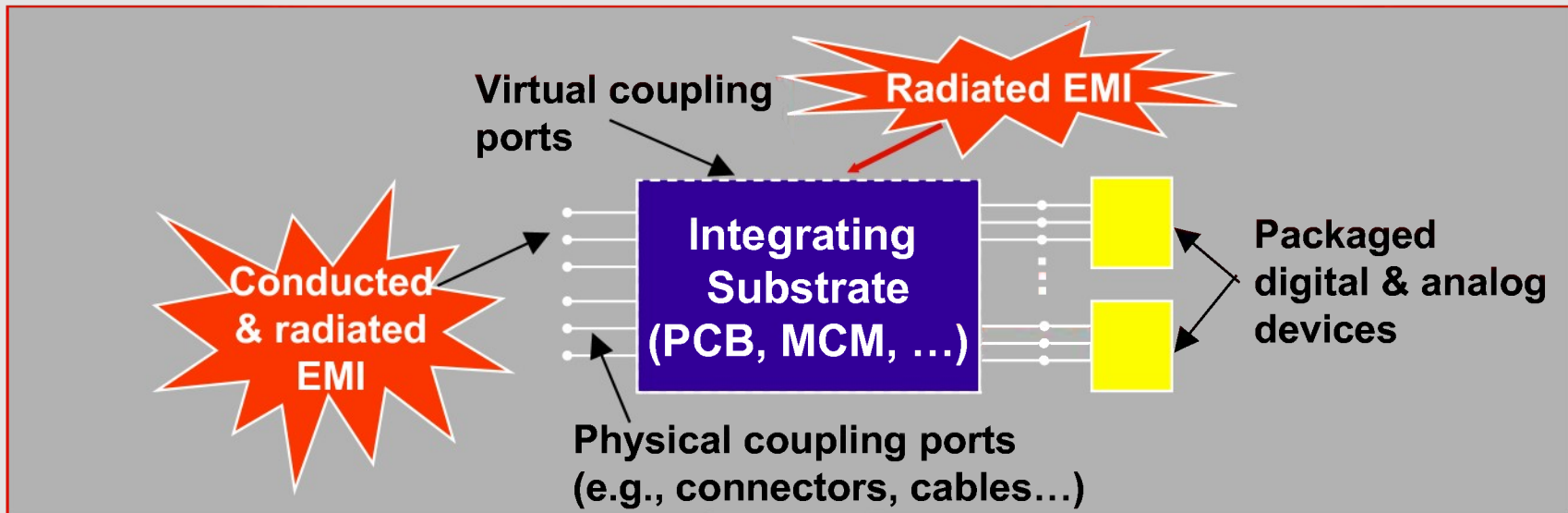
■ Abstracting Complexity

- Systematic order reduction of numerical models of the coupling path
- Equivalent circuit representation of the coupling path for its seamless incorporation in network-oriented non-linear circuit simulators

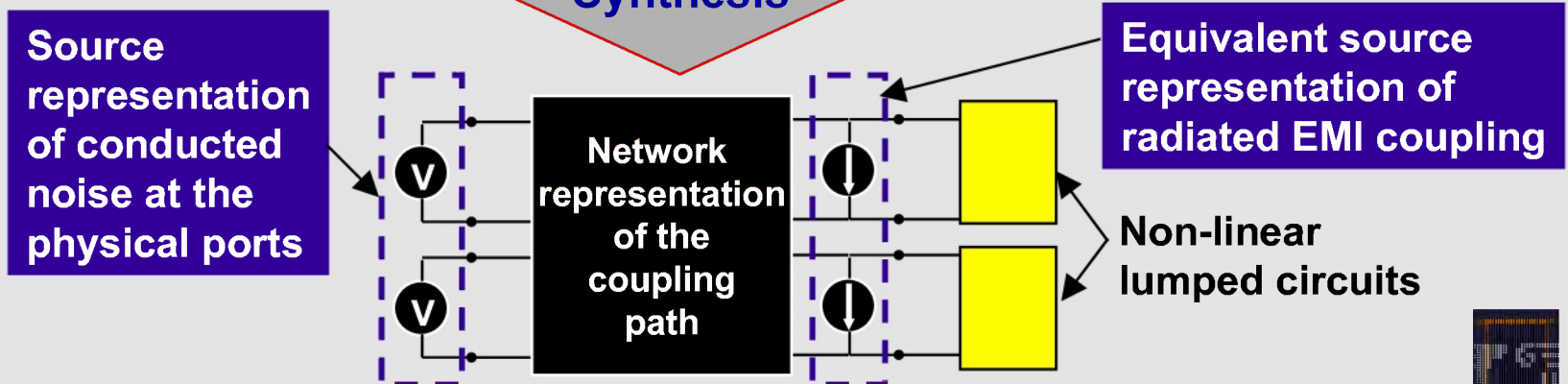


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SUMMARY OF MODELING OBJECTIVE



EM Modeling & Simulation Model Order Reduction Synthesis



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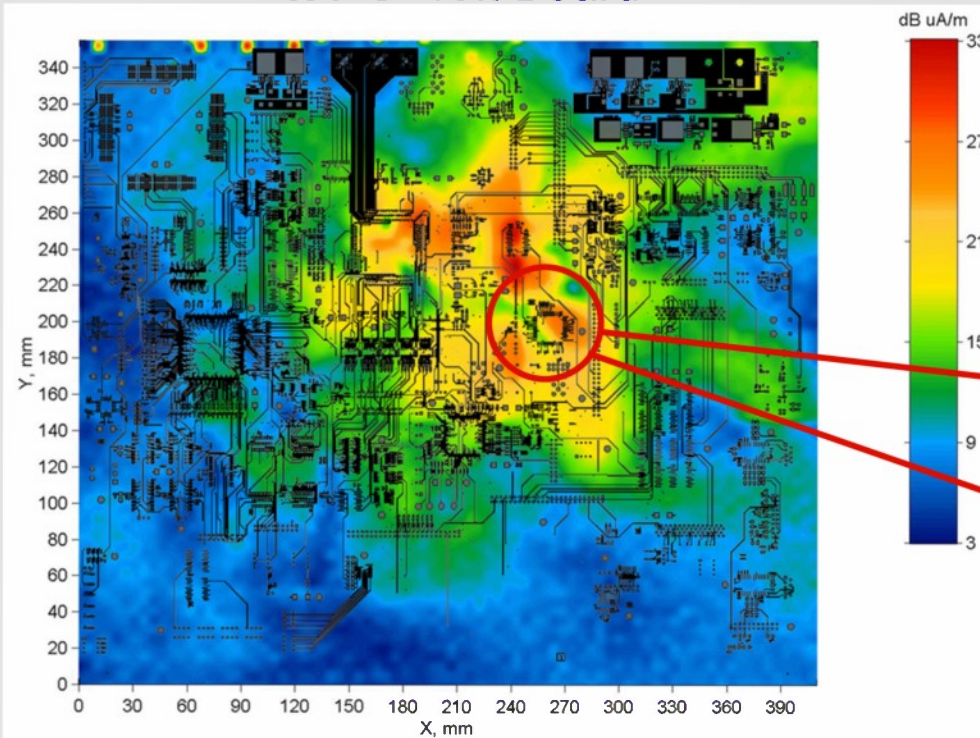
Specific Subtasks

- **Task 2.1** Development of a coupling path modeling methodology
- **Task 2.2** Development of a (EMI) source modeling methodology
- **Task 2.3** Non-linear Transient Simulation of the hybrid lumped-distributed non-linear network

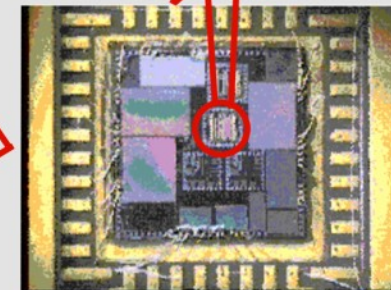
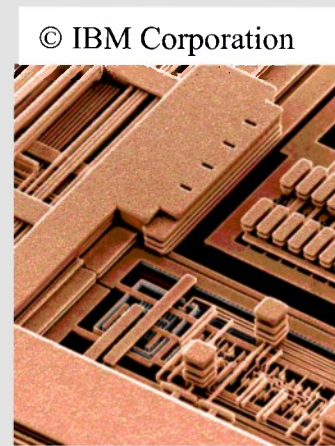


Subtask 1: Modeling of the Coupling Path

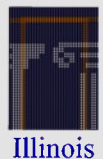
Printed Circuit Board



Chip

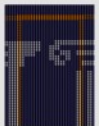


Package

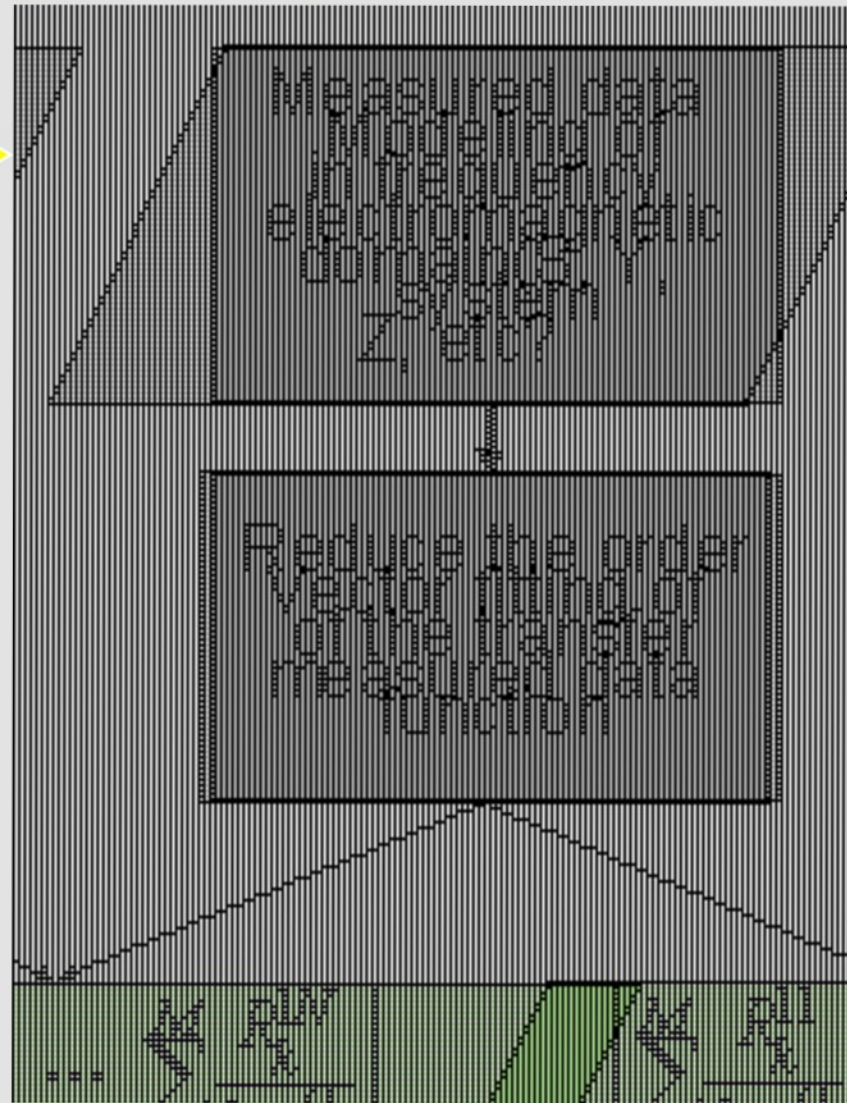
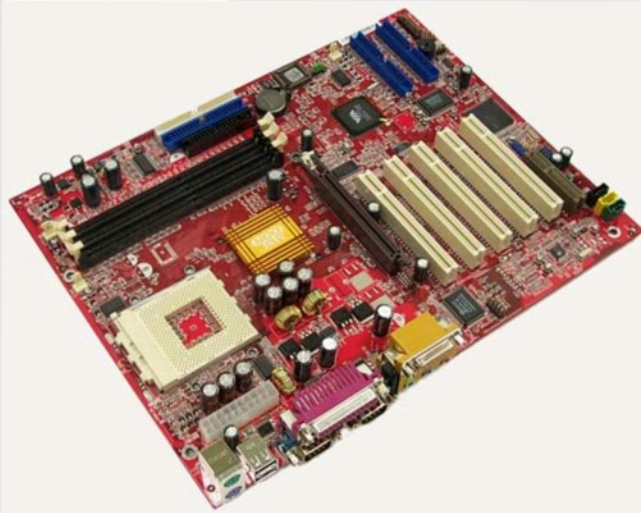
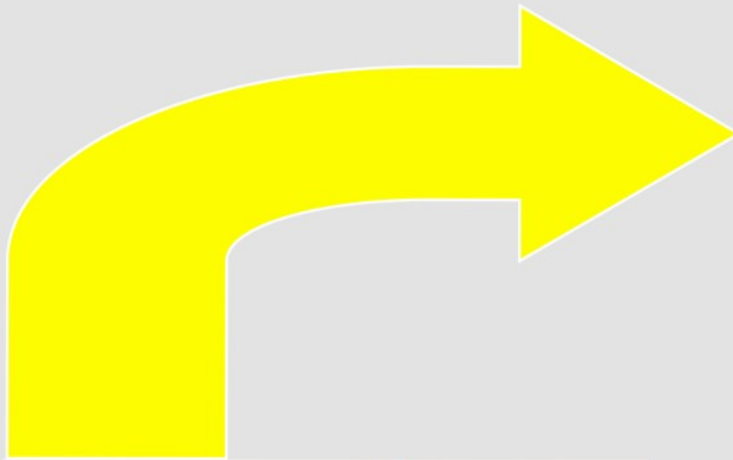


Subtask 1: Modeling of the Coupling Path (Cont)

- Our modeling approach is hierarchical
 - EM-Physics driven “divide and conquer” approach
- Use suitable EM modeling approach for individual blocks
 - RLC models for short interconnect at chip & package level
 - Multi-conductor Transmission Lines (MTL)
 - Balanced interconnects at the board level
 - Quasi-3D EM Modeling for PCB power delivery network
 - Full-wave modeling
 - Unbalanced interconnects at the board level
 - Coupling through cables
 - RF/microwave packages & boards
- Reduction of EM models to non-linear network simulator (e.g. SPICE)
 - Direct model order reduction
 - Equivalent circuit synthesis



Block Diagram of EM Modeling Flow



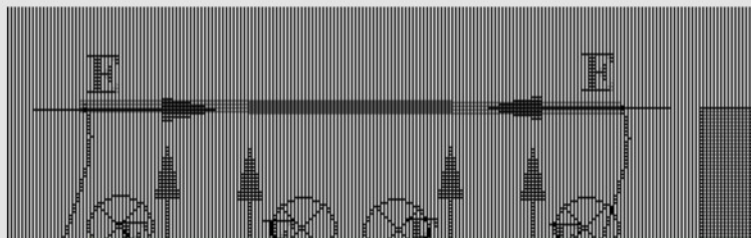
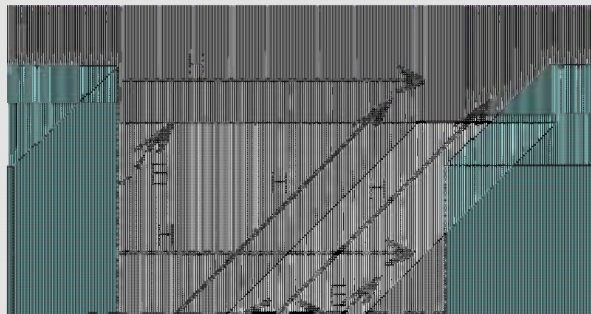
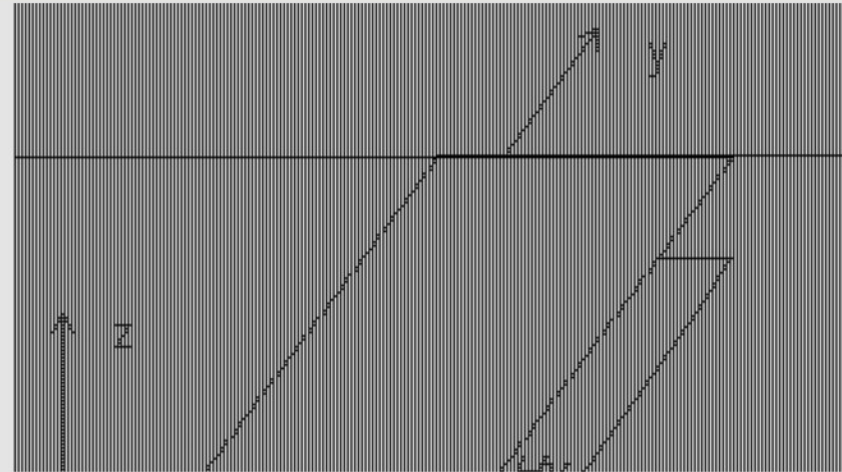
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Quasi-3D Modeling of Power Delivery Network

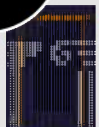
EM field between power/ground plane pairs exhibits, approximately, a two-dimensional variation

- Use simple 2D FDTD

Three-dimensional features (vias, pins, slots, voids, etc) require locally 3D models to capture the correct physics



$$\begin{aligned}
 j\omega\epsilon E_z(i, j) &= \Delta x^{-1} (H_y(i+1, j) - H_y(i, j)) \\
 &\quad - \Delta y^{-1} (H_x(i, j+1) - H_x(i, j)) \\
 -j\omega\mu\Delta y H_x(i, j) &= E_z(i, j) - E_z(i, j-1) \\
 j\omega\mu\Delta x H_y(i, j) &= E_z(i, j) - E_z(i-1, j)
 \end{aligned}$$



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The resulting discrete EM model

$$\begin{bmatrix} \mathbf{G} & -\mathbf{D}_I \\ -\mathbf{D}_V & \mathbf{R} \end{bmatrix} \begin{bmatrix} \mathbf{E}(s) \\ \mathbf{H}(s) \end{bmatrix} + s \begin{bmatrix} \mathbf{C} & \mathbf{0} \\ \mathbf{0} & \mathbf{L} \end{bmatrix} \begin{bmatrix} \mathbf{E}(s) \\ \mathbf{H}(s) \end{bmatrix} = \mathbf{F}\mathbf{U}(s), \quad \mathbf{V} = \mathbf{F}^T \mathbf{X}$$

$$\mathbf{V}(s) = \mathbf{F}^T (\mathbf{A} + s\mathbf{B})^{-1} \mathbf{F}\mathbf{U}(s) \quad \text{where } \mathbf{A} = \begin{bmatrix} \mathbf{G} & -\mathbf{D}^T \\ \mathbf{D} & \mathbf{R} \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} \mathbf{C} & \mathbf{0} \\ \mathbf{0} & \mathbf{L} \end{bmatrix}$$

The multiport transfer function is: $\mathbf{Y}(s) = \mathbf{F}^T (\mathbf{A} + s\mathbf{B})^{-1} \mathbf{F}$

- Direct time-domain simulation is possible if desired
 - Could be synchronized with time-domain IE solver
- Alternatively, model order reduction of the transfer function using an Arnoldi-based subspace iteration method (PRIMA) is used for the generation of a compact multiport

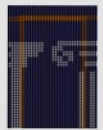


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Multi-port representation of the reduced-order model is in terms of rational functions

$$\mathbf{Y}(s) = \begin{bmatrix} \sum_{k=1}^M \frac{R_k^{11}}{s - P_k} & \cdots & \sum_{k=1}^M \frac{R_k^{1N}}{s - P_k} \\ \vdots & \cdot & \vdots \\ \sum_{k=1}^M \frac{R_k^{N1}}{s - P_k} & \cdots & \sum_{k=1}^M \frac{R_k^{NN}}{s - P_k} \end{bmatrix}$$

- Form compatible with circuit simulators that support rational function models (e.g. H-Spice, ADS)
- Equivalent circuit synthesis is possible also



Passive synthesis through Foster forms

For a passive, reciprocal multi-port, its admittance (or impedance) matrix may be cast in the following form:

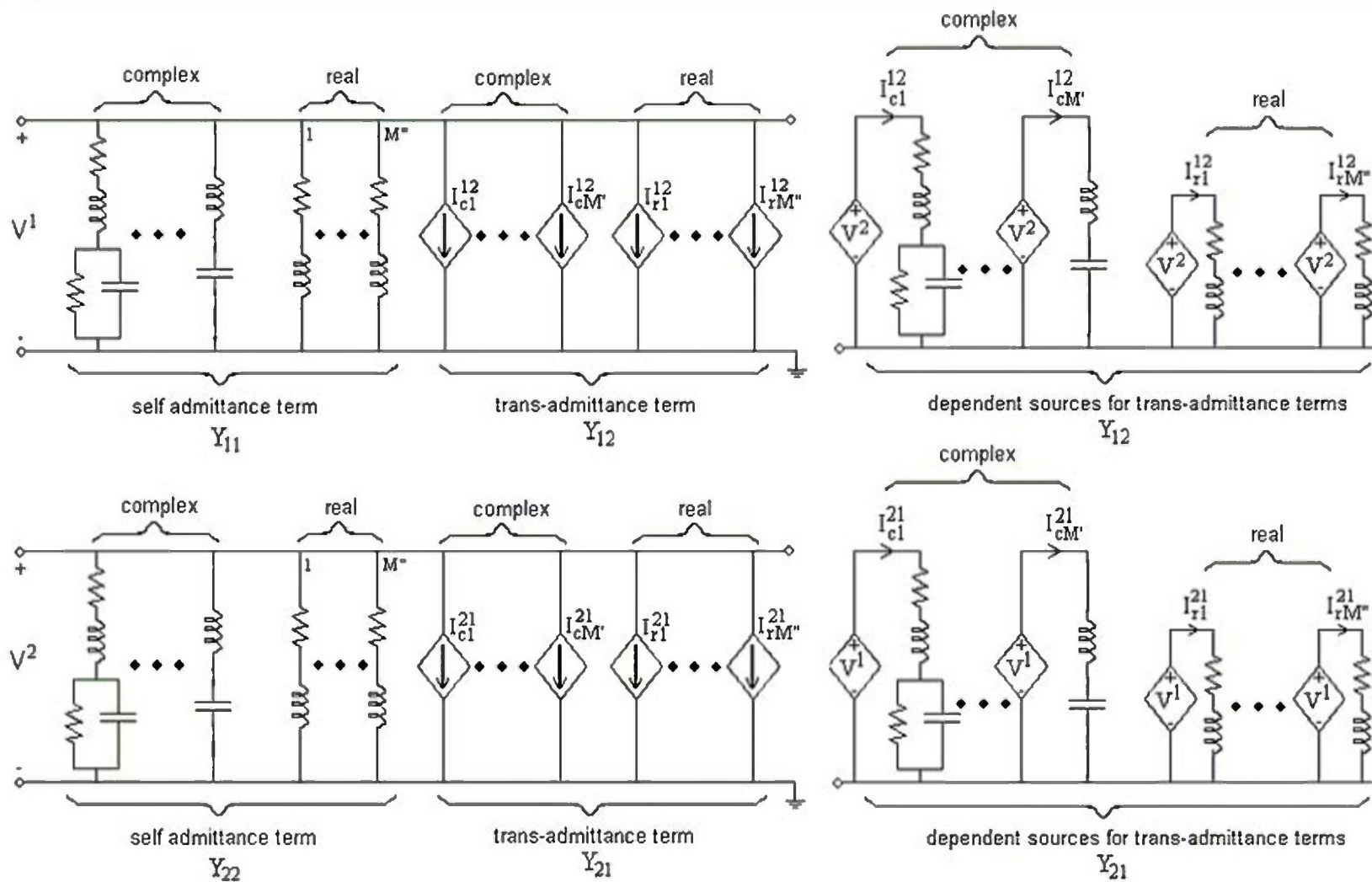
$$\mathbf{H}(s) = \mathbf{G}_0 + s\mathbf{C}_0 + \sum_{q=1}^Q \left(\frac{a_q}{s - p_q} + \frac{\bar{a}_q}{s - \bar{p}_q} \right) \mathbf{G}_q$$

where it is:

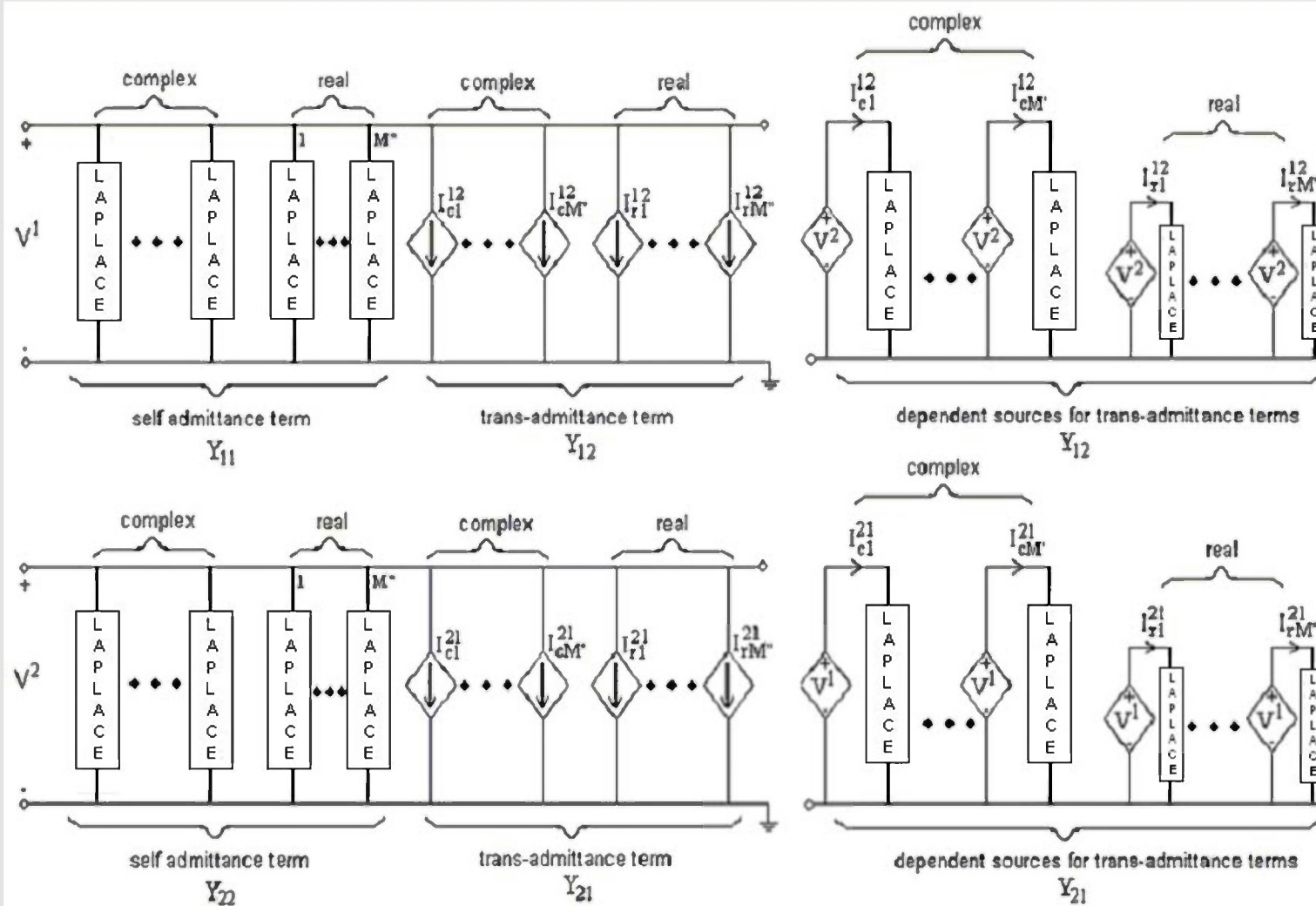
- $\operatorname{Re}\{p_q\} \leq 0, \quad q = 1, 2, \dots, Q$
- matrices \mathbf{C}_0 and $\mathbf{G}_q, \quad q = 0, 1, 2, \dots, Q$, are real and positive semi-definite
- $\operatorname{Re}\{a_q\} > 0, \quad q = 1, 2, \dots, Q$
- $0 < \operatorname{Im}\{a_q\} \operatorname{Im}\{p_q\} \leq \left| \operatorname{Re}\{a_q\} \operatorname{Re}\{p_q\} \right|, \quad q = 1, 2, \dots, Q$



Equivalent circuit for a two-port



Two-port sub-circuit for use in H-SPICE



The advantages of the direct use of the rational function macro-model in the simulator

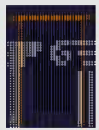
Elapsed Simulation Time

	3 ports	10 ports	36 ports
H-SPICE	0.7 sec	5.73 sec	21.2 min
Equivalent	2.3 sec	676.55 sec	>12 hours

Transient Data File Size

	3 ports	10 ports	36 ports
H-SPICE	25.9 KB	53.4 KB	172 KB
Equivalent	308.2 KB	269 MB	>2 GB

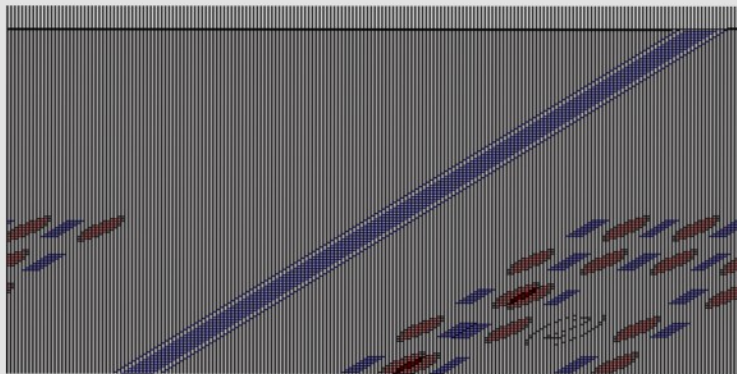
The secret is in the recursive convolution that is utilized for the interfacing of the macro-model with the rest of the circuit



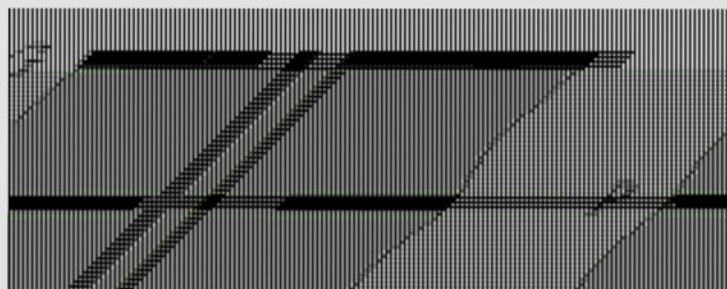
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Application to a 4-layer PCB

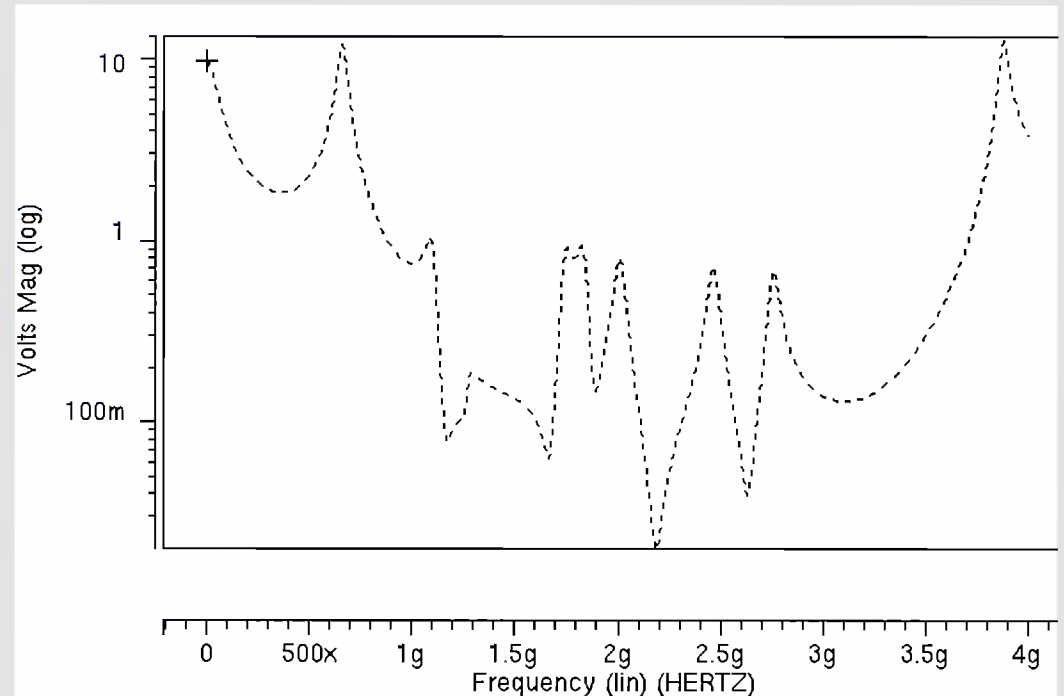
8 cm X 4 cm, 4 layer board. A 2mm gap is present all the way across the top ground plane. A total of 58 pins are used.



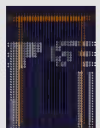
Top view



Cross-sectional view

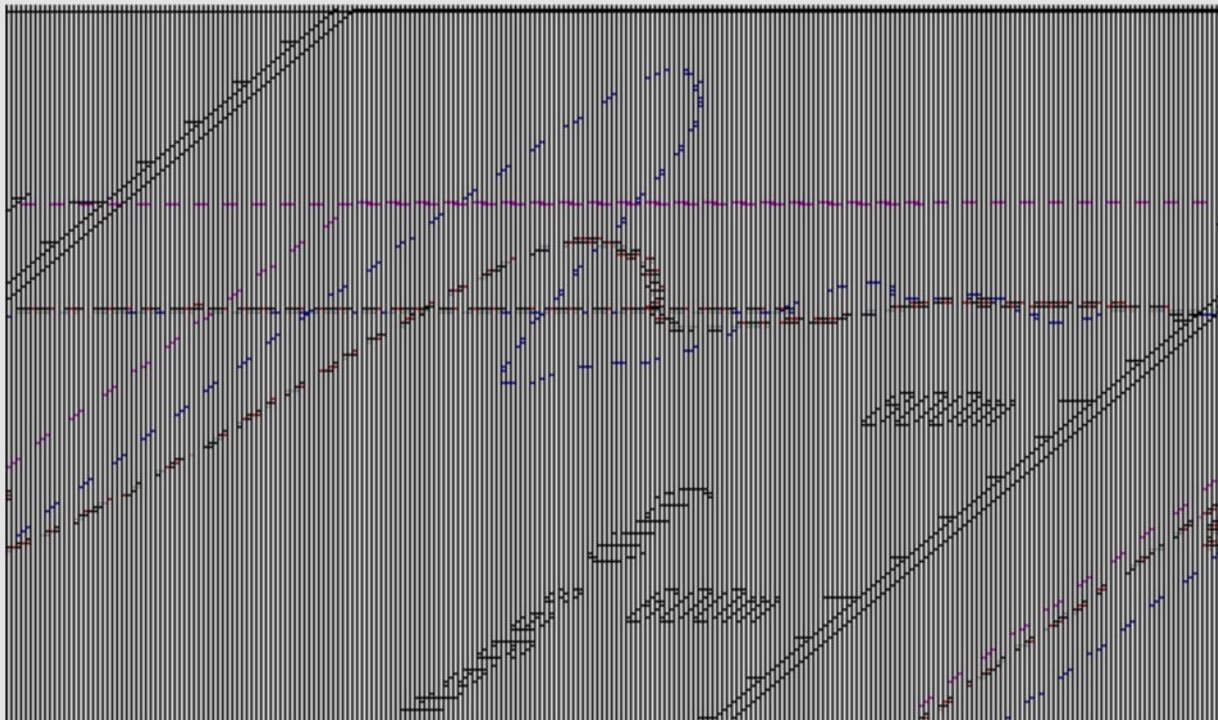


|Z₂₁| From H-SPICE



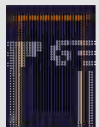
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Application to a 4-layer PCB (cont'd)



H-SPICE calculation of the transient response.

Switching occurs at port 1 while port 2 is terminated with 50ohm.
Voltage at port 1 is depicted by the solid line.
Voltage at port 2 is depicted by the dotted line.



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Validation study in progress

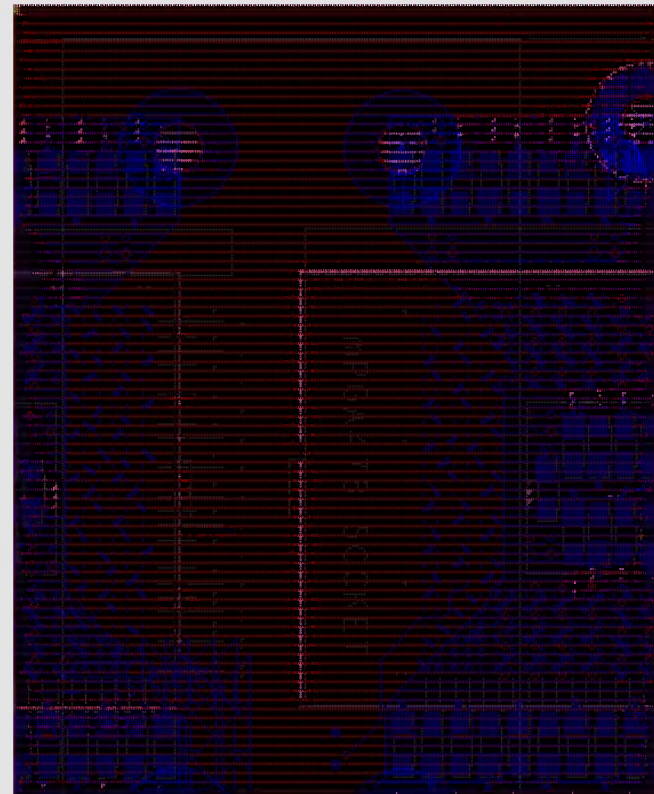
Intel 4-layer test board

1st layer: Power plane

2nd layer: Ground plane

3rd layer: Ground plane

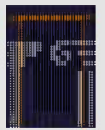
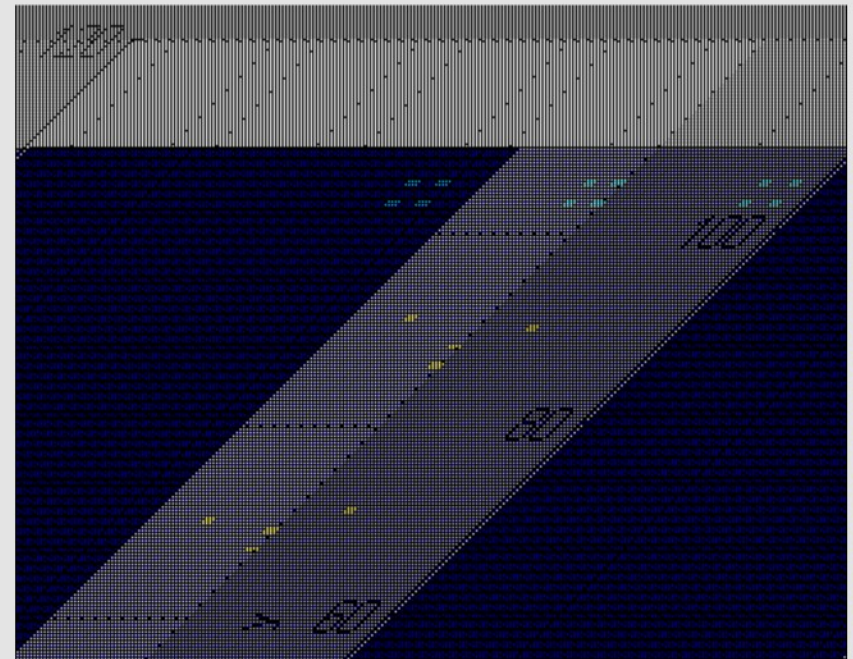
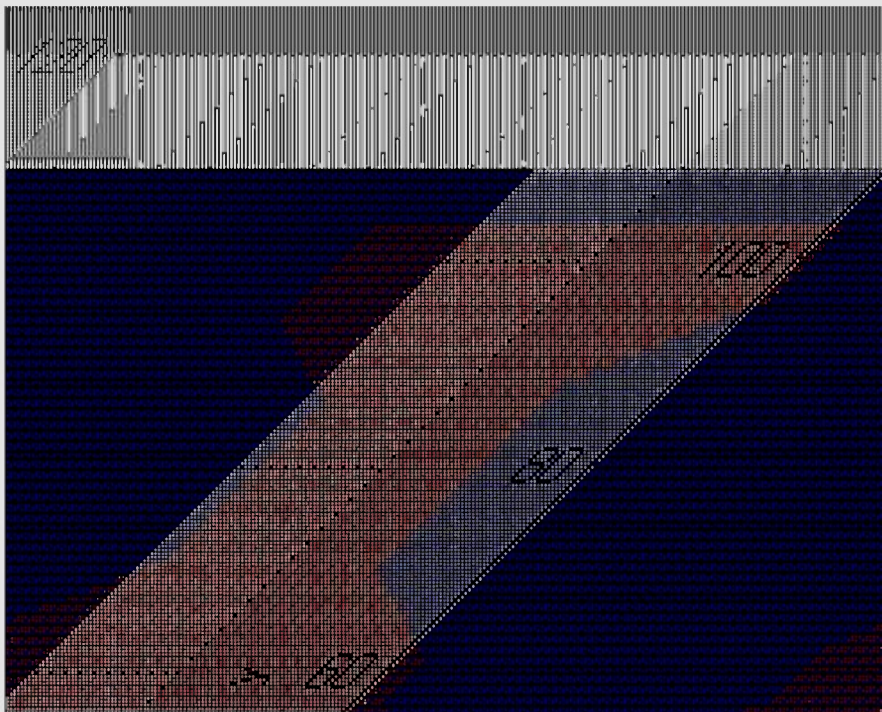
4th layer: Power plane



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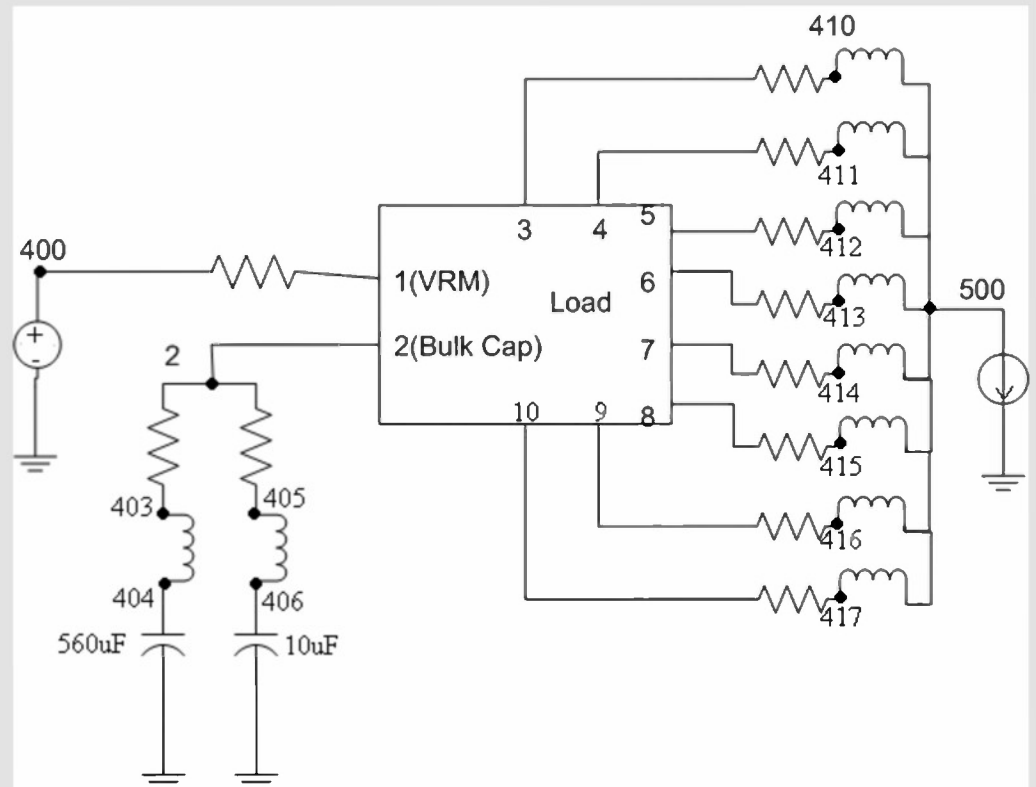
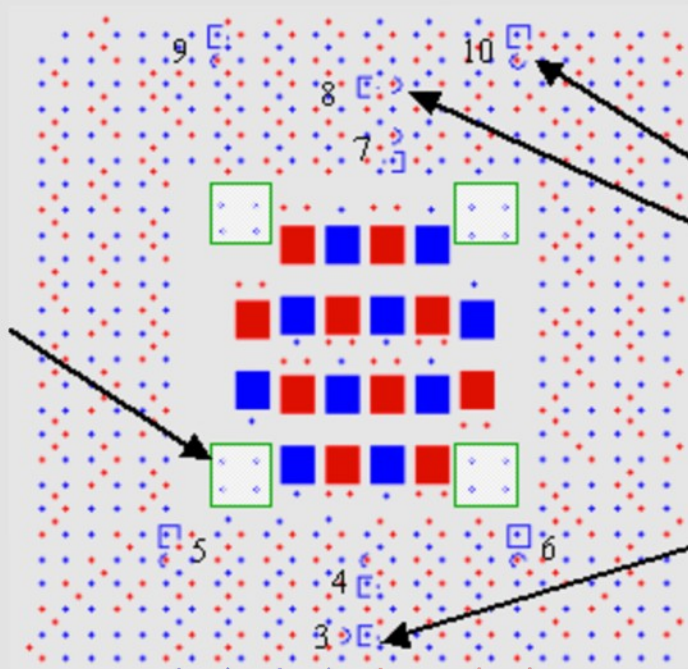
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Samples of the generated mesh



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Generated multi-port for switching noise simulation in SPICE



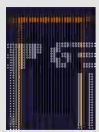
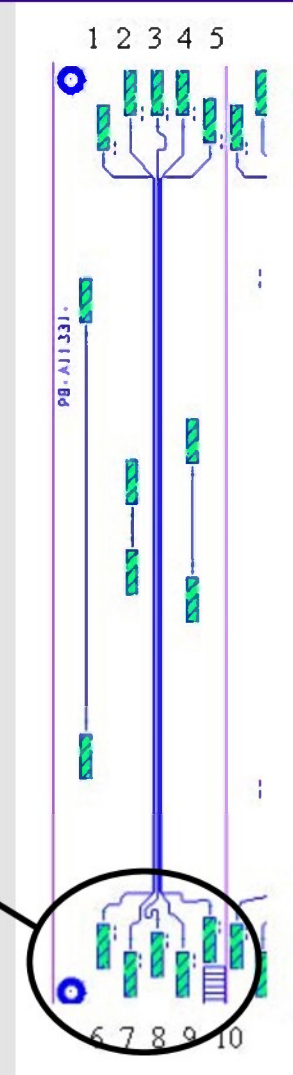
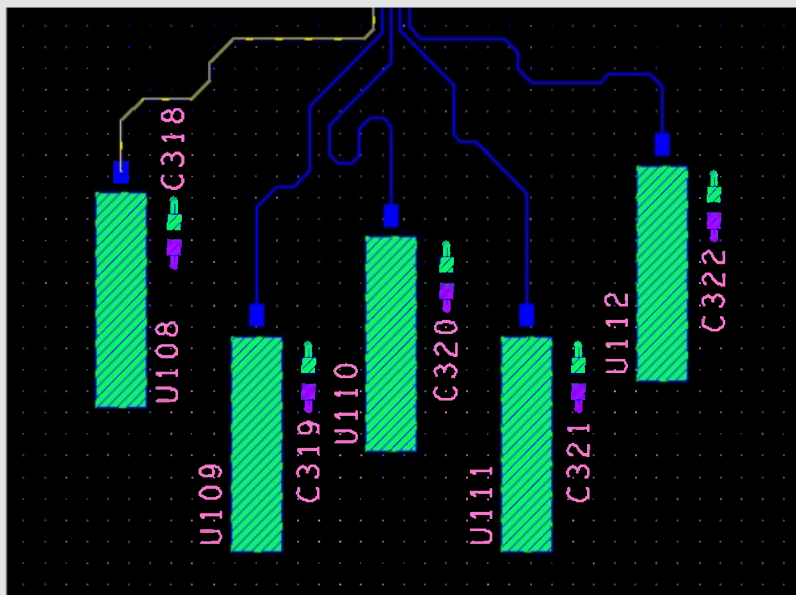
Rational function multi-port & equivalent circuit synthesis from raw data

- Data either from measurements or EM field solvers
- Step 1: Rational function fitting
 - Process guarantees stability but not passivity
 - Check fitted multi-port for passivity
 - If not passive, constrain fitting using Foster constraints
 - Repeat fitting



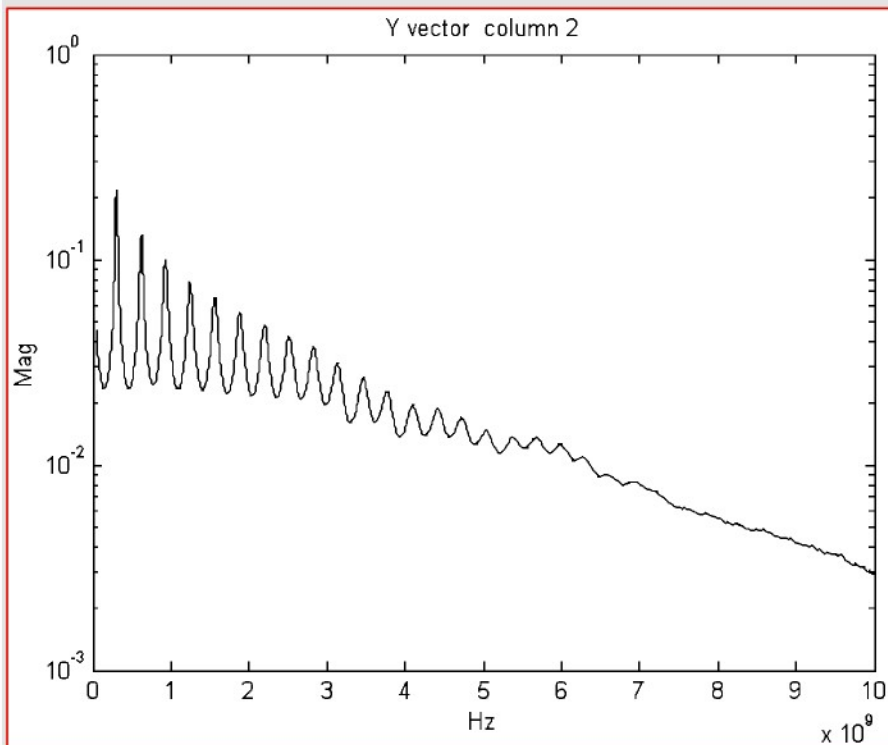
Validation of rational function fitting

PCB interconnect test structures courtesy of Intel

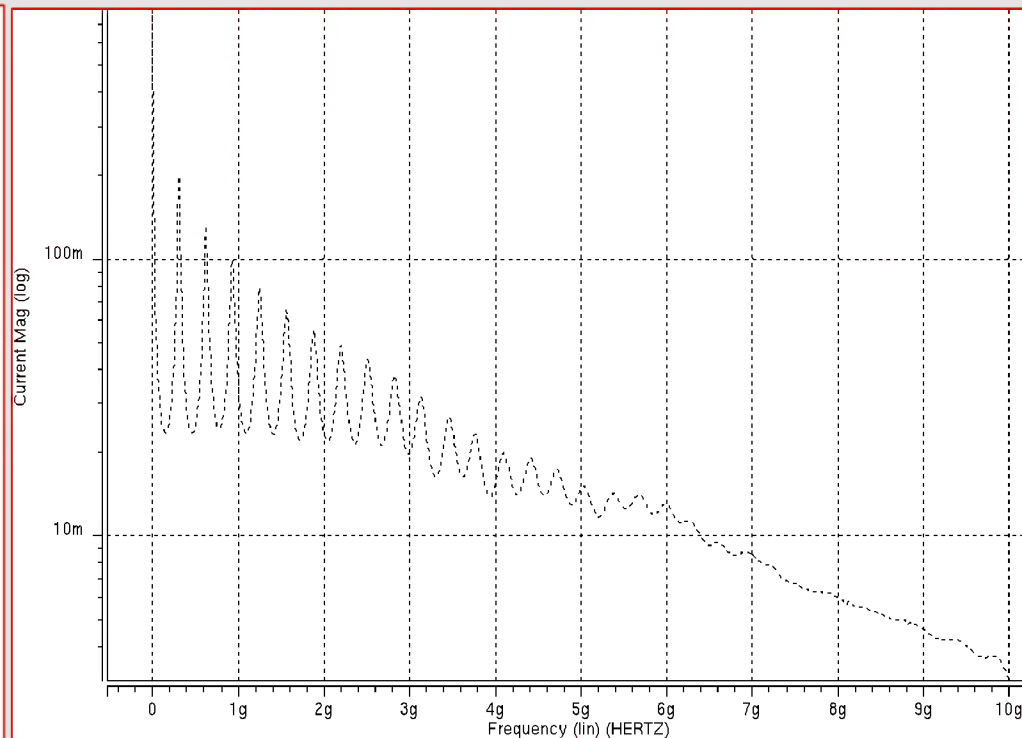


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Validation of fitting (cont'd)



Measured $|Y_{61}|^*$



Synthesized $|Y_{61}|$

(*) Measurements courtesy of Intel Corporation



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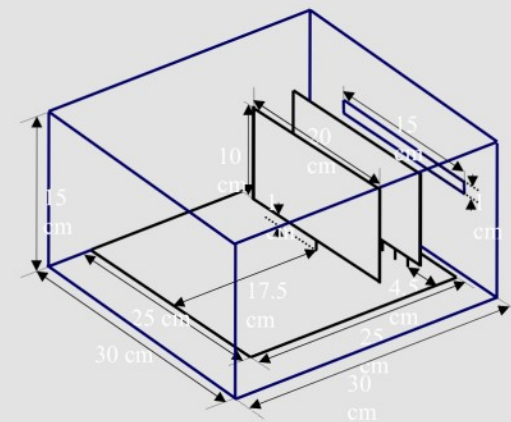
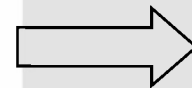
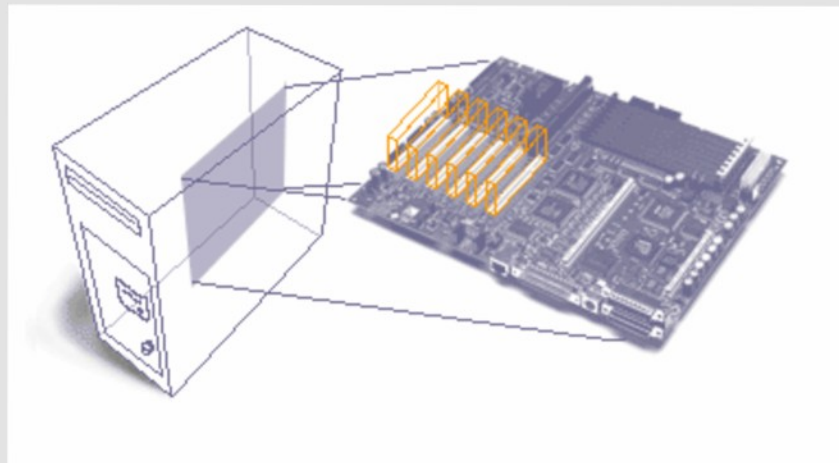
Task 2.1 Summary

- EM modeling flow for the coupling path established
- Quasi-3D EM Model for power delivery network completed
 - Validation in progress
 - Further enhancements include:
 - Incorporation of hooks for balanced MTLs
 - Incorporation of hooks for matrix transfer functions in Foster form
- Capability for SPICE-compatible broadband multi-port macro-model generation in place



Subtask 2.3: Non-linear Transient Simulation

- **Physics-oriented nonlinear transient simulator**
 - Full wave modeling of printed circuit boards (PCBs) with fine geometric features, finite (and possibly inhomogeneous) dielectrics, and nonlinear loads and circuits
 - Interfaces with SPICE solvers and models

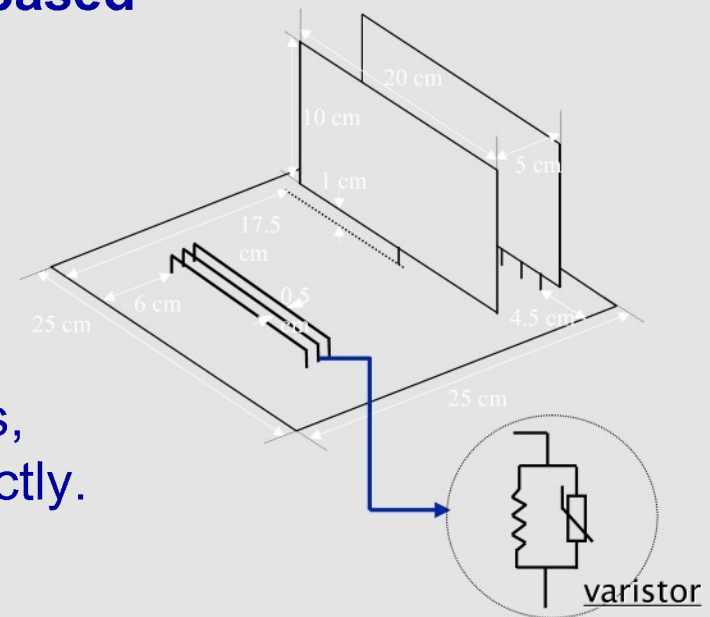


Introduction (cont.)

- **Time Domain Integral Equation (TDIE) based Marching-on-in-time (MOT) solvers**

- Have been known to the acoustics and electromagnetics communities since the sixties.
- Compared to frequency domain solvers, they can solve nonlinear problems directly.

Liu and Tesche (1976),
Landt and Miller (1983),
Djordjevic and Sarkar (1985),
Deiseroth and Singer (1995),
Orlandi (1996)



Introduction (cont.)

However TDIE - MOT solvers have long been conceived as

- **Unstable:** ... But recently many proposals have surfaced for stabilizing these schemes (Davies, Rao and Sarkar, Walker, Smith, Rynne,...);
- **Slow:** ... Computational complexity has prohibited application to analysis of large scale problems!
... **PWTD** technology removes this computational bottleneck

$$O(N_T N_S^2)$$

$$O(N_T N_S \log^2 N_S)$$

Now, we can / should be able to rapidly solve **large-scale, nonlinear** problems using the PWTD technology!!!



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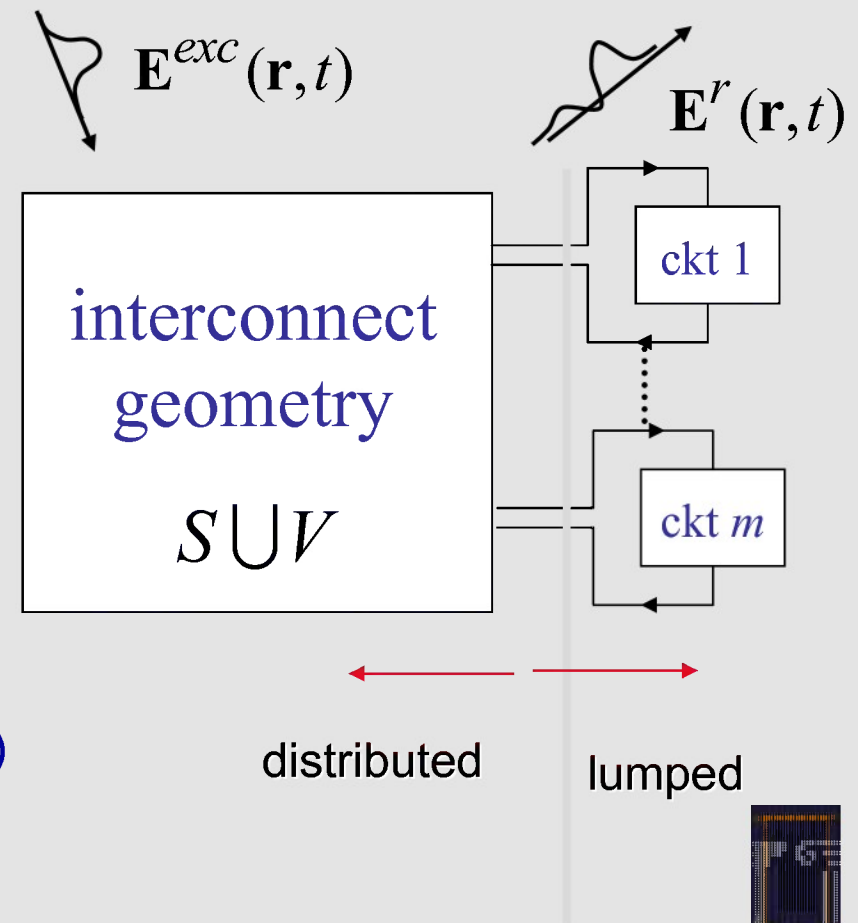
Formulation - Problem Definition

Given

- an of 3-D inhomogeneous dielectric bodies (V), and 3-D arbitrarily shaped PEC surfaces, wires, and surface-wire junctions (S),
- Multiple linear / nonlinear lumped circuits connected to $S \cup V$
- a temporally bandlimited excitation

Solve for

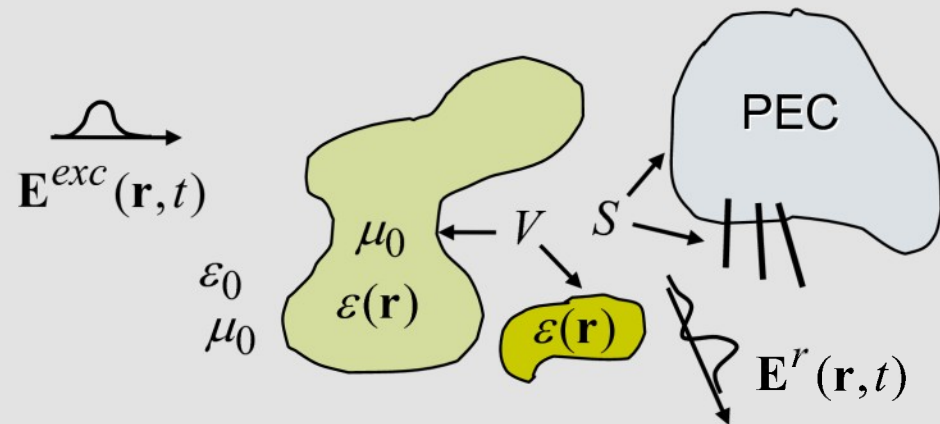
- all transient currents and voltages induced on the interconnect geometry $S \cup V$ and the the circuits (ckt 1, ..., ckt m)
- radiated electric and/or magnetic fields if required



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Formulation – Time Domain Electric Field

- Assume spatially-variable, frequency independent permittivity and free-space permeability in V , and thin wires in S .
- Radiated electric field:



$$\mathbf{E}^r(\mathbf{r}, t) = -\frac{\partial}{\partial t} \mathbf{A}(\mathbf{r}, t) + c^2 \int_0^t dt' \nabla \nabla \cdot \mathbf{A}(\mathbf{r}, t') \quad (1)$$

$$\mathbf{A}(\mathbf{r}, t) = \frac{\mu_0}{4\pi} \left[\int_S ds' \frac{\delta(t - R/c)}{R} * \mathbf{J}_{PEC}(\mathbf{r}', t) + \int_V dv' \frac{\delta(t - R/c)}{R} * \mathbf{J}_{DIEL}(\mathbf{r}', t) \right], \quad (2)$$

$$R = |\mathbf{r} - \mathbf{r}'|, \quad \mathbf{J}_{DIEL}(\mathbf{r}, t) = (\varepsilon(\mathbf{r}) - \varepsilon_0) \frac{\partial}{\partial t} \mathbf{E}^{total}(\mathbf{r}, t)$$

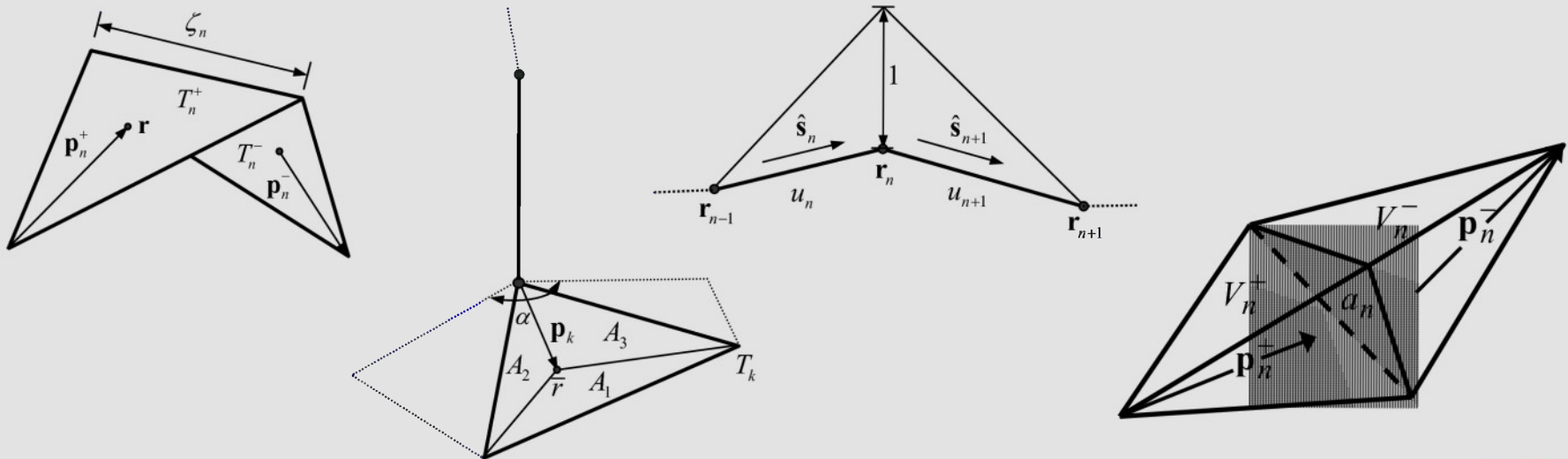


Formulation - MOT Algorithm

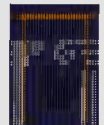
① Expand current as
$$\mathbf{J}(\mathbf{r}, t) \approx \sum_{n=1}^{N_S} \sum_{j=0}^{N_T} I_n^j \mathbf{f}_n^q(\mathbf{r}) T_j(t), \quad q = s, w, sw, d$$

$$N_S = N_{PEC} + N_{DIEL}$$

- Surface and Volume Spatial Basis Functions



- The temporal basis functions are local cubic polynomials



Formulation - MOT Algorithm (cont.)

- ② Construct a system of equations by applying spatial Galerkin testing at each time step.
- for the j 'th time step:

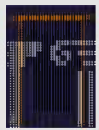
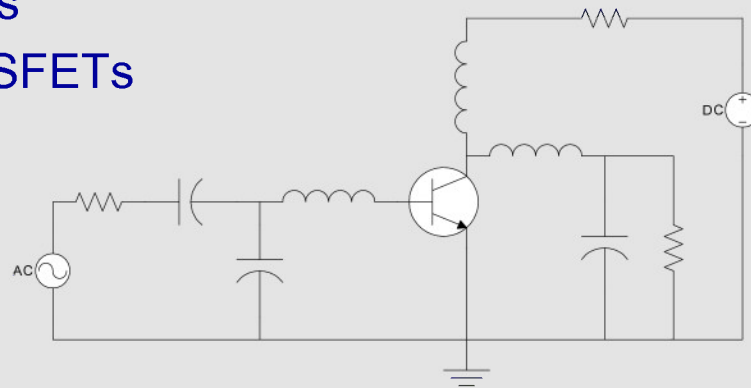
$$\bar{\mathbf{Z}}_0 \mathbf{I}_j = \mathbf{V}_j^{exc} - \sum_{l=1}^{j-1} \bar{\mathbf{Z}}_l \mathbf{I}_{j-l}$$

The diagram illustrates the equation $\bar{\mathbf{Z}}_0 \mathbf{I}_j = \mathbf{V}_j^{exc} - \sum_{l=1}^{j-1} \bar{\mathbf{Z}}_l \mathbf{I}_{j-l}$ with the following components:

- immediate interactions** (red box) points to $\bar{\mathbf{Z}}_0 \mathbf{I}_j$.
- unknowns** (green box) points to \mathbf{I}_j .
- tested incident field** (blue box) points to \mathbf{V}_j^{exc} .
- delayed interactions** (red box) points to $\bar{\mathbf{Z}}_l \mathbf{I}_{j-l}$.
- previously computed** (green box) points to $\bar{\mathbf{Z}}_l \mathbf{I}_{j-l}$.

Formulation - Transient Circuit Simulator

- SPICE-like transient circuit simulator
 - Performs linear and nonlinear large-signal analysis using Modified nodal analysis
 - Nonlinear equations solved using multi-dimensional Newton
 - Incorporates the following circuit elements:
 - Independent/dependent voltage and current sources
 - Resistors, inductors, capacitors
 - Diodes, BJTs, MOSFETs, MESFETs



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Formulation - Transient Circuit Simulator (cont.)

- Circuit behavior described by time-domain nodal equations (using trapezoidal rule for the j th time step)

$$\mathbf{G}_0(\mathbf{V}_j) = \mathbf{I}_j^{exc} + \mathbf{G}_1(\mathbf{V}_{j-1})$$

Diagram illustrating the nodal equation $\mathbf{G}_0(\mathbf{V}_j) = \mathbf{I}_j^{exc} + \mathbf{G}_1(\mathbf{V}_{j-1})$ with annotations:

- \mathbf{G}_0 : immediate interactions (red box)
- \mathbf{V}_j : unknowns (green box)
- \mathbf{I}_j^{exc} : sources (blue box)
- \mathbf{G}_1 : interactions from previous time step (red box)
- \mathbf{V}_{j-1} : previously computed (green box)

- For m circuits, the nonlinear system of equations is

$$\tilde{\mathbf{G}}_0(\tilde{\mathbf{V}}_j) = \begin{bmatrix} \mathbf{G}_0^1(\mathbf{V}_j^1) \\ \vdots \\ \mathbf{G}_0^m(\mathbf{V}_j^m) \end{bmatrix} = \begin{bmatrix} \mathbf{I}_j^{exc,1} \\ \vdots \\ \mathbf{I}_j^{exc,m} \end{bmatrix} + \begin{bmatrix} \mathbf{G}_1^1(\mathbf{V}_{j-1}^1) \\ \vdots \\ \mathbf{G}_1^m(\mathbf{V}_{j-1}^m) \end{bmatrix} = \tilde{\mathbf{I}}_j^{exc} + \tilde{\mathbf{G}}_1(\tilde{\mathbf{V}}_{j-1})$$

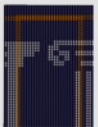


Formulation - Coupled EM / Circuit Equations

- Combine the EM and circuit nodal equations into a single consistent system to be solved for N_S EM and N_C circuit unknowns at each time step

$$\begin{bmatrix} \bar{\mathbf{Z}}_0 & \bar{\mathbf{C}}_v \\ \bar{\mathbf{C}}_i & 0 \end{bmatrix} \begin{bmatrix} \mathbf{I}_j \\ \tilde{\mathbf{V}}_j \end{bmatrix} + \begin{bmatrix} 0 \\ \tilde{\mathbf{G}}_0(\tilde{\mathbf{V}}_j) \end{bmatrix} = \begin{bmatrix} \mathbf{V}_j^{exc} - \sum_{l=1}^{j-1} \mathbf{Z}_l \mathbf{I}_{j-l} \\ \tilde{\mathbf{I}}_j^{exc} + \tilde{\mathbf{G}}_1(\tilde{\mathbf{V}}_{j-1}) \end{bmatrix}$$

- Coupling between the circuits and the interconnect structure is accounted for by matrices $\bar{\mathbf{C}}_v$ and $\bar{\mathbf{C}}_i$

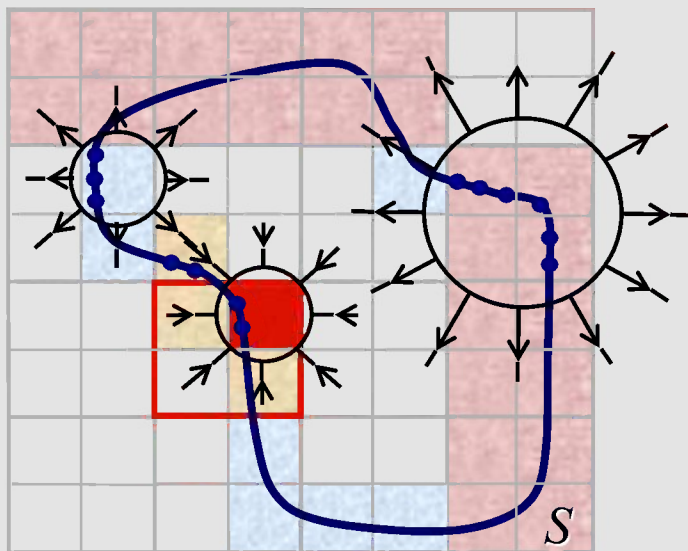


Formulation - the MLPWTD Algorithm

$$\bar{\mathbf{Z}}_0 \mathbf{I}_j = \mathbf{V}_j^{exc} - \sum_{l=1}^{j-1} \bar{\mathbf{Z}}_l \mathbf{I}_{j-l}$$

$O(N_T N_S \log^2 N_S)$

for typical PCB structures



Level	Direct(0)	1	2
Source block			
Observer block			



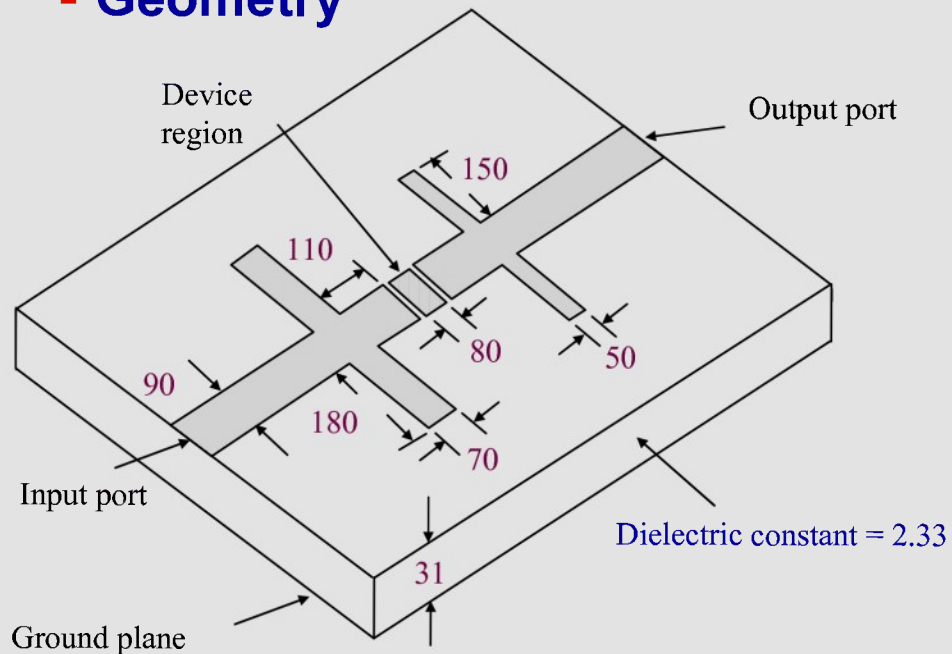
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Analysis of Active Nonlinear Microwave Amplifier

Objective

Characterize structure
from 2-10 GHz

Geometry



Simulation Parameters

$$N_s = 1468, N_v = 7096$$

$$N_s + N_v = 8564, N_t = 512$$

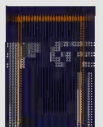
$$\Delta t = 5.0 \text{ ps}$$

Excitation pulse

$$\mathbf{V}^{inc}(\mathbf{r}, t) = V_0 \cos(\omega_0 t') e^{-t'^2/2\sigma^2}$$

$$\omega_0 = 2\pi \times 6 \times 10^9 \text{ rad/s}$$

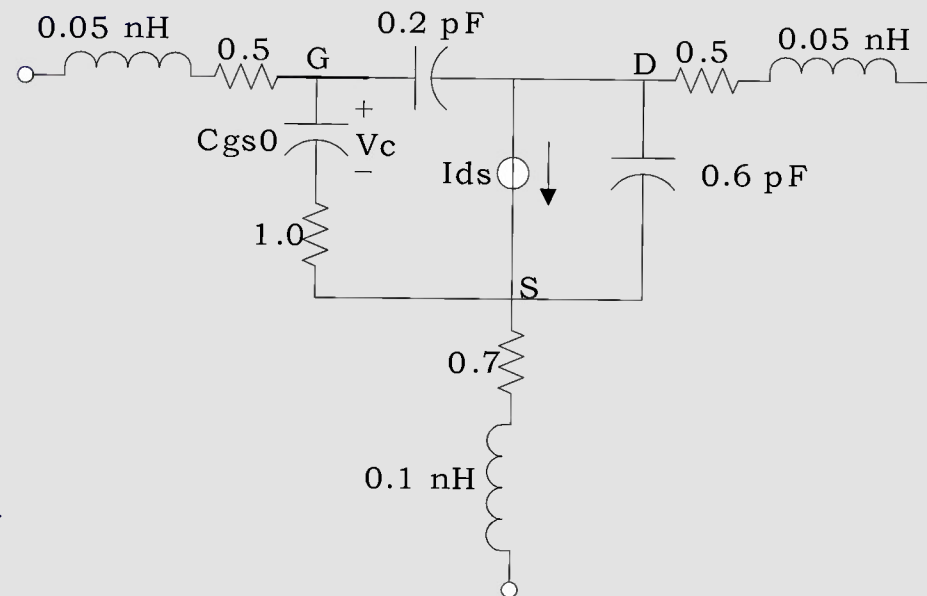
$$t' = t - 6\sigma, \quad \sigma = 6.82 \times 10^{-11} \text{ s}$$



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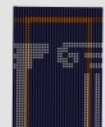
Amplifier : Nonlinear circuitry

■ MESFET Circuit Model



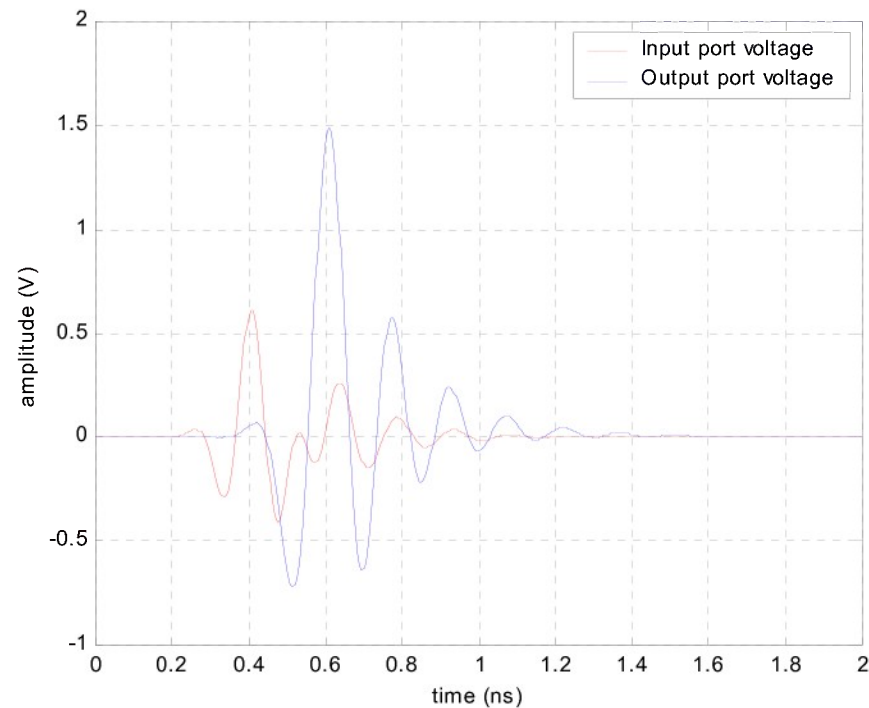
$$C_{gs}(v_c) = \frac{C_{gs0}}{\sqrt{1 - v_c / \phi_b}}$$

$$I_{ds}(v_{gs}, v_{ds}) = (A_0 + A_1 v_{gs} + A_2 v_{gs}^2 + A_3 v_{gs}^3) \tanh(\alpha v_{ds})$$

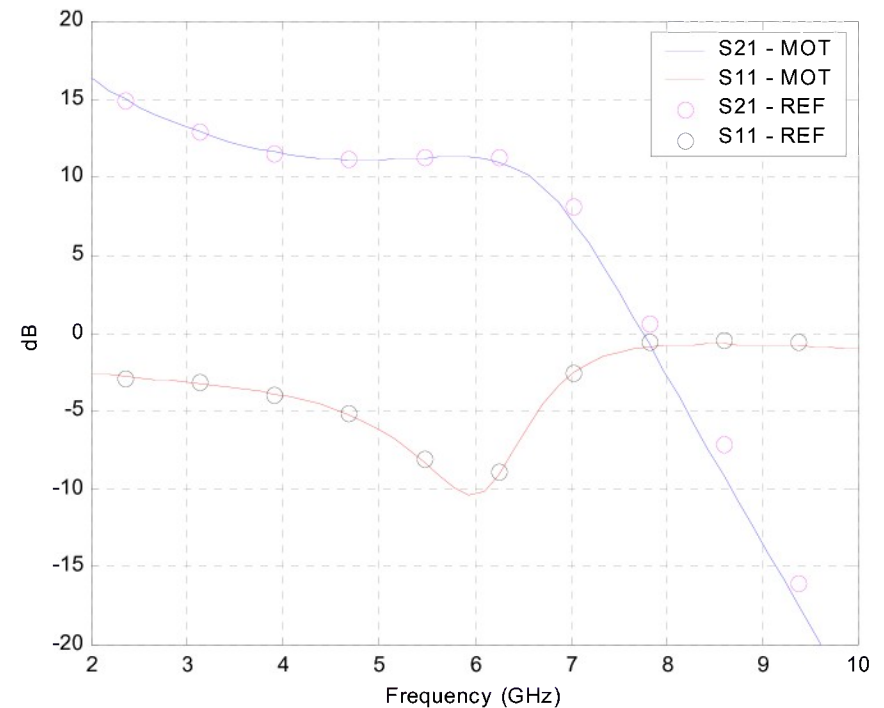


Amplifier: Plane Wave Interference

■ Transient input/output waveforms



■ MOT results*



* C. Kuo, B. Houshmand, and T. Itoh, "Full-wave analysis of packaged microwave circuits with active and nonlinear devices: an FDTD approach," IEEE Trans. Microwave Theory Tech., vol. 45, pp. 819-826, May 1997.



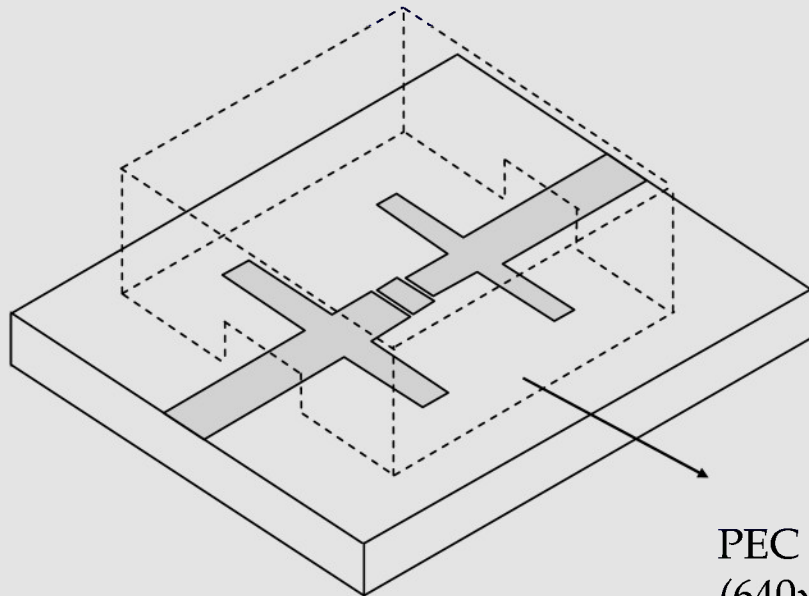
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Amplifier + Shield: geometry

- **Objective**

Determine effect of shielding box on S-parameters

- **Geometry**



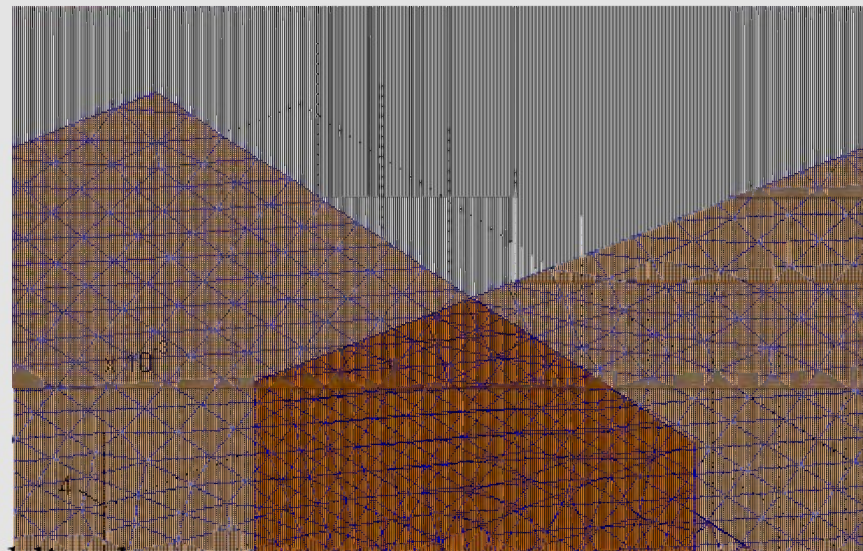
PEC shielding box
(640x186x690mils)

- **Simulation Parameters**

$$N_s = 3288, N_v = 7096$$

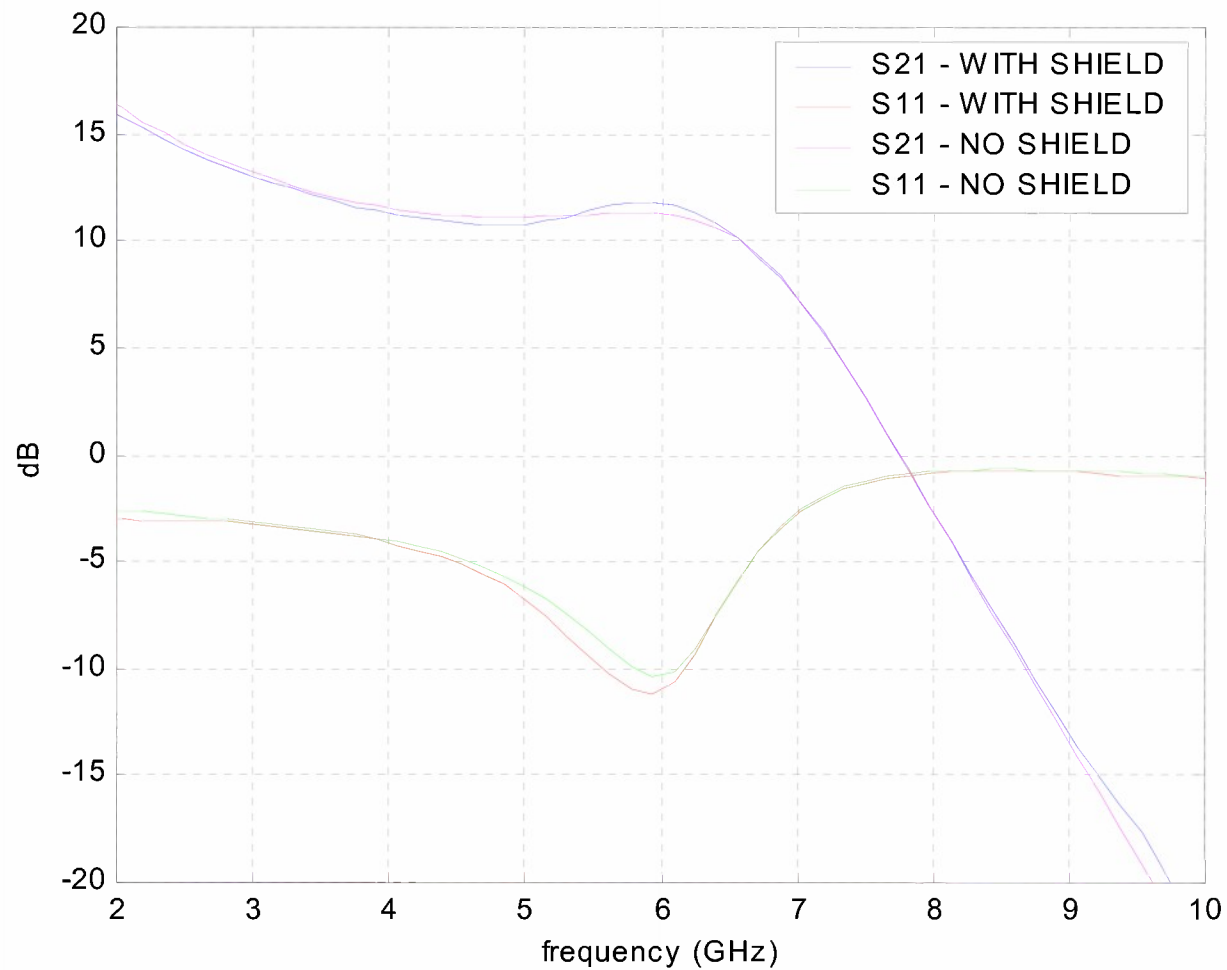
$$N_s + N_v = 10384, N_t = 700$$

$$\Delta t = 6.25 \text{ ps}$$



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Amplifier + Shield: S-parameters



Amplifier + Shield: Plane Wave Interference

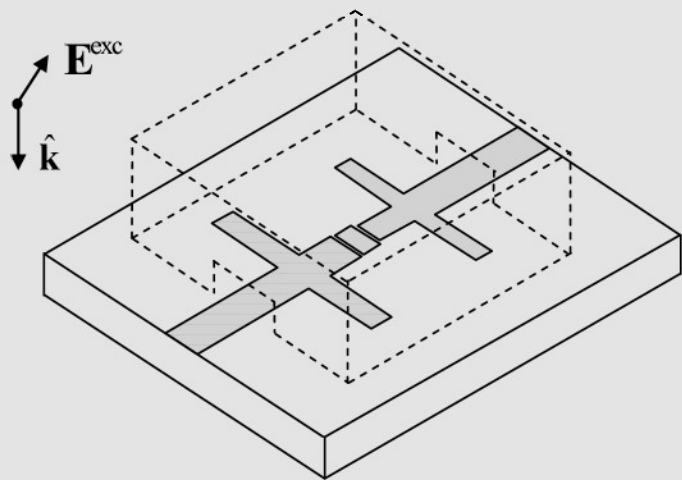
$$\mathbf{E}^{exc}(\mathbf{r}, t) = \mathbf{E}_0 \cos(\omega_0 t') e^{-t'^2/2\sigma^2}$$

$$\mathbf{E}_0 = 500\hat{\mathbf{x}} + 500\hat{\mathbf{y}} \text{ V/m}$$

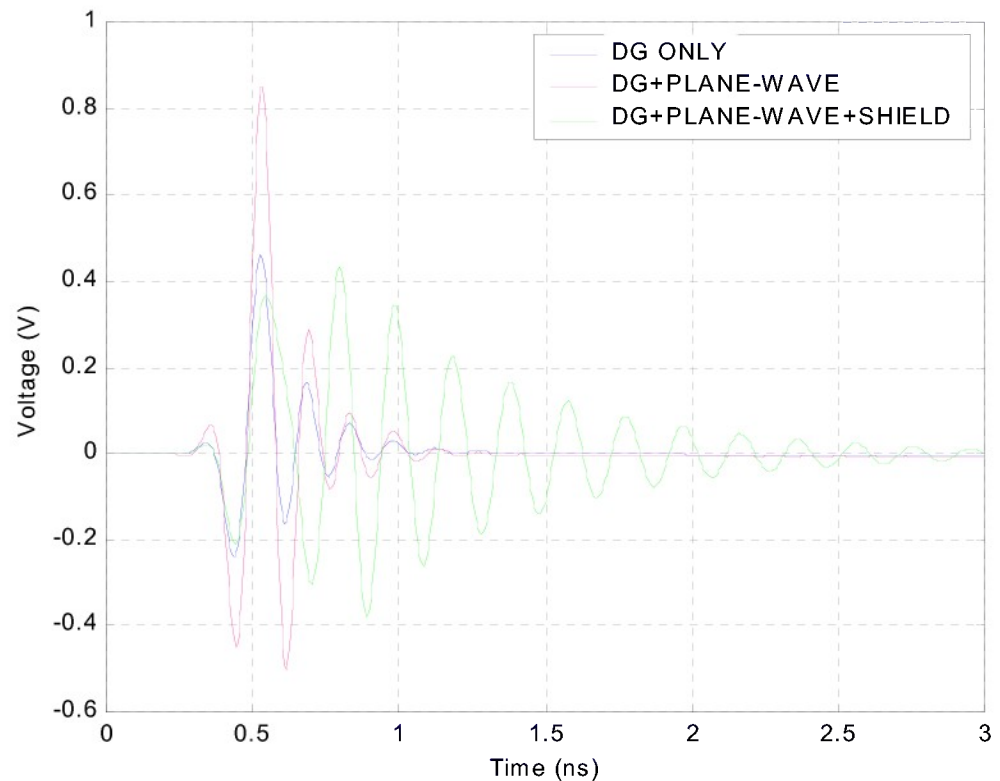
$$\omega_0 = 2\pi \times 6 \times 10^9 \text{ rad/s}$$

$$t' = t - 6\sigma + (\hat{\mathbf{z}} \cdot \mathbf{r})/c$$

$$\sigma = 8.68 \times 10^{-11} \text{ s}$$



Transient response at transistor output



Amplifier + Shield: Plane Wave Interference

$$\mathbf{E}^{exc}(\mathbf{r}, t) = \mathbf{E}_0 \cos(\omega_0 t') e^{-t'^2/2\sigma^2}$$

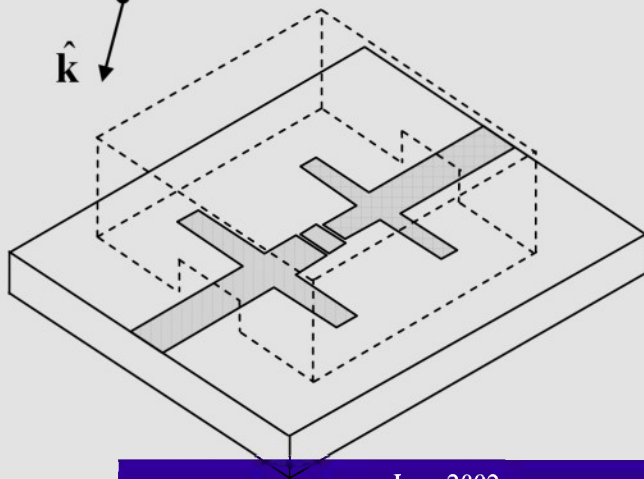
$$\omega_0 = 2\pi \times 4 \times 10^9 \text{ rad/s}$$

$$t' = t - 6\sigma - (\hat{\mathbf{k}} \cdot \mathbf{r})/c \quad \sigma = 1/4\pi \text{ ns}$$

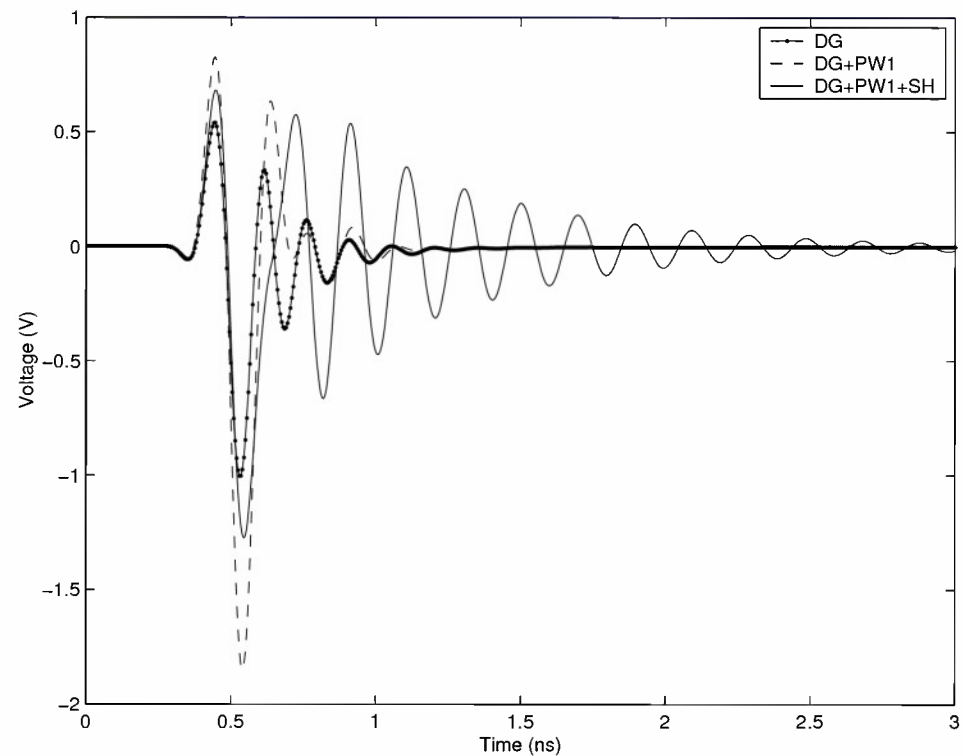
$$\theta_i = 145, \phi_i = 0$$

$$\hat{\mathbf{k}} = 0.5736\hat{\mathbf{x}} - 0.8192\hat{\mathbf{y}}$$

$$\mathbf{E}^{exc} \quad E_\theta = -500 \text{ V/m}, E_\phi = -500 \text{ V/m}$$



Transient response at transistor output



Amplifier + Shield: Plane Wave Interference

$$\mathbf{E}^{exc}(\mathbf{r}, t) = \mathbf{E}_0 \cos(\omega_0 t') e^{-t'^2/2\sigma^2}$$

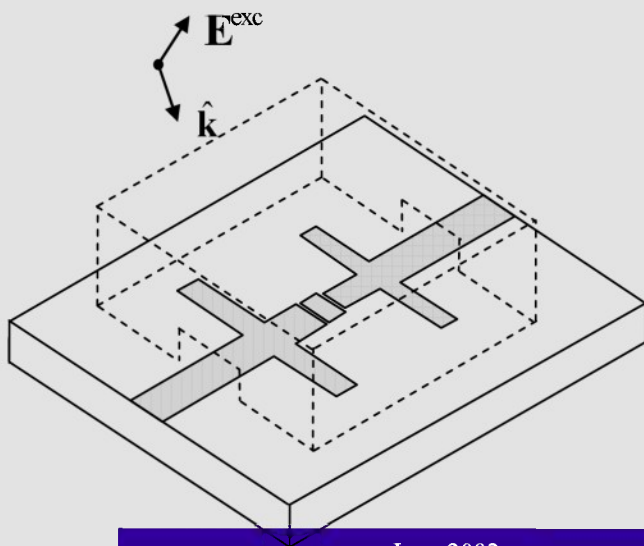
$$\omega_0 = 2\pi \times 3 \times 10^9 \text{ rad/s}$$

$$t' = t - 6\sigma - (\hat{\mathbf{k}} \cdot \mathbf{r})/c \quad \sigma = 3/14\pi \text{ ns}$$

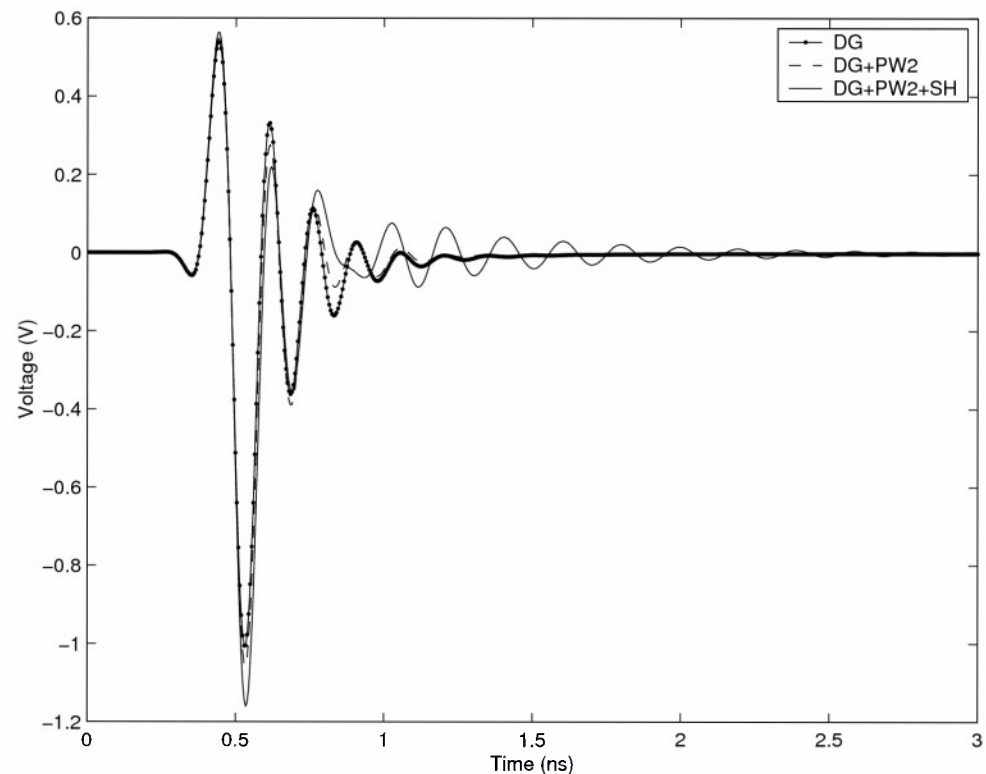
$$\theta_i = 115, \phi_i = 45$$

$$\hat{\mathbf{k}} = 0.6409(\hat{\mathbf{x}} + \hat{\mathbf{y}}) - 0.4226\hat{\mathbf{z}}$$

$$E_\theta = -500 \text{ V/m}, E_\phi = 500 \text{ V/m}$$



Transient response at transistor output



Amplifier + Shield: Plane Wave Interference

$$\mathbf{E}^{exc}(\mathbf{r}, t) = \mathbf{E}_0 \cos(\omega_0 t') e^{-t'^2/2\sigma^2}$$

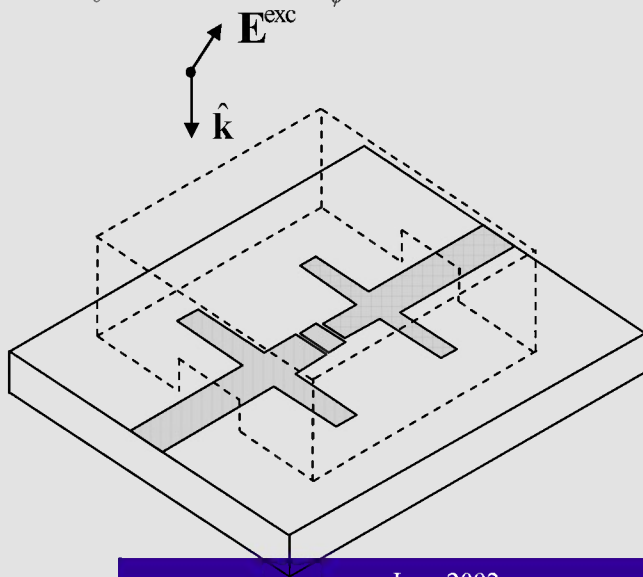
$$\omega_0 = 2\pi \times 6 \times 10^9 \text{ rad/s}$$

$$t' = t - 6\sigma - (\hat{\mathbf{k}} \cdot \mathbf{r})/c \quad \sigma = 3/11\pi \text{ ns}$$

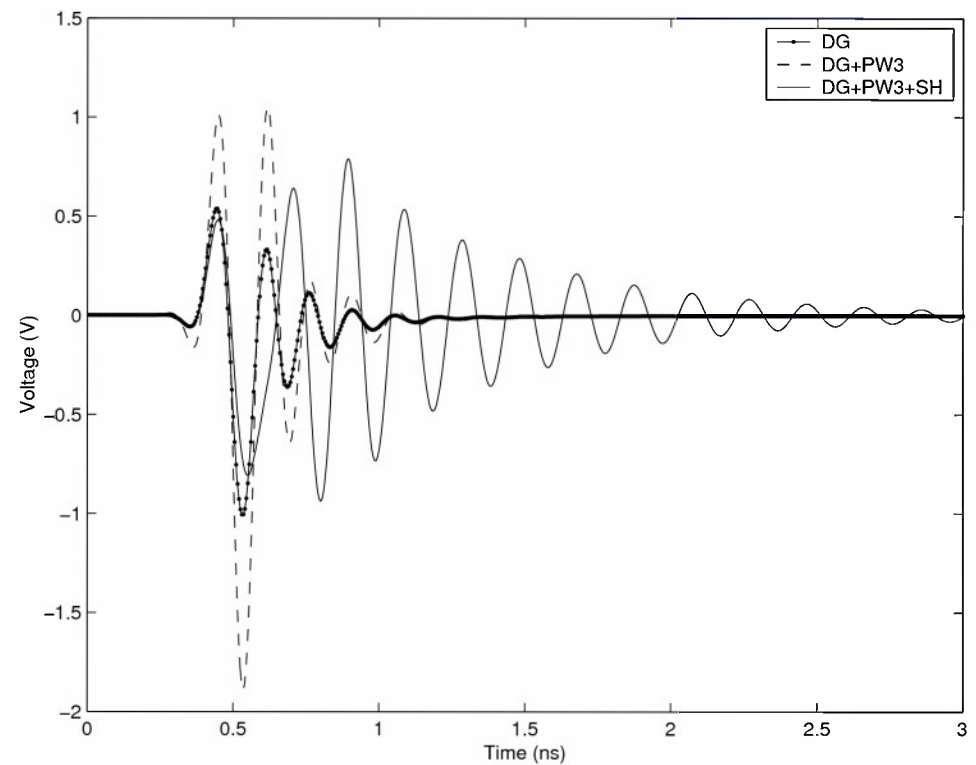
$$\theta_i = 180, \phi_i = 0$$

$$\hat{\mathbf{k}} = -\hat{\mathbf{z}}$$

$$E_\theta = -500 \text{ V/m}, E_\phi = 500 \text{ V/m}$$



Transient response at transistor output



Task 2.3: Summary

- 1) A **MOT** algorithm based on a **hybrid surface/volume** time domain integral equation has been developed for analysis of conducting/inhomogeneous dielectric bodies,
- 2) This algorithm has been accelerated with the **PWTD** technology that rigorously reduces the $O(N_T N_S^2)$ computational complexity of the MOT solver to $O(N_T N_S \log^2 N_S)$ for typical PCB structures,
- 3) Linear/Nonlinear circuits in the system are modeled by coupling **modified nodal analysis** equations of circuits to MOT equations,
- 4) A nonlinear Newton-based solver is used at each time step to **consistently** solve for circuit and electromagnetic unknowns.
- 5) The proposed method can find extensive use in EMC/EMI and signal integrity analysis of PCB, interconnect and packaging structures with realistic complexity.

