NAVAL POSTGRADUATE SCHOOL
Monterey, California

Analog-to-Digital Signal Processing

in a Prototype SATCOM Signal Analyzer

John E. Ohlson
William B. Zell, Jr.

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Project Report

NAVAL POSTGRADUATE SCHOOL
Monterey, California

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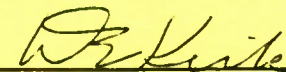
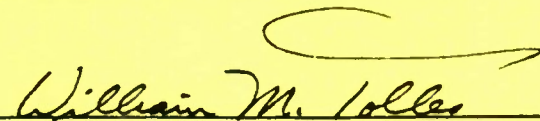This report was prepared by:

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A prototype SATCOM Signal Analyzer (SSA) has been designed which performs spectral analysis on transponder signals from the Navy's UHF communications satellites. As an integral part of the SSA, the Analog to Digital Control and Conversion subsystem converts four channels to baseband analog signals into equivalent digital representations while operating at variable sampling rates and offering either twelve or eight bits of resolution of the analog signal. The digital data thus derived is presented to an array processor

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ABSTRACT

A prototype SATCOM Signal Analyzer (SSA) has been designed which performs spectral analysis on transponder signals from the Navy's UHF communications satellites. As an integral part of the SSA, the Analog to Digital Control and Conversion subsystem converts four channels of baseband analog signals into equivalent digital representations while operating at variable sampling rates and offering either twelve or eight bits of resolution of the analog signal. The digital data thus derived is presented to an array processor for Fast Fourier Transform processing. This report documents the design and construction of the Analog to Digital Control and Conversion subsystem.

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I.   INTRODUCTION

A.   BACKGROUND

This project is one of a series of research projects concerning Navy UHF satellite communications (SATCOM) undertaken by the Satellite Communications Laboratory at the Naval Postgraduate School (NPS). Previous research efforts include, but are not limited to, the preparation and evaluation of a shipboard Radio Frequency Interference (RFI) measurement package (Refs. 1-3), the design and construction of the development model SATCOM Signal Analyzer (Refs. 4-6), and the measurement of transponder oscillator drift of the GAPFILLER satellite (Ref. 7). The project which constitutes the basis of this report had its beginning in late 1978 when this laboratory was funded by PME 106-1 of the Naval Electronic Systems Command (NAVELEX) to develop a prototype version SATCOM Signal Analyzer (SSA) system. Upon successful completion and field testing of the prototype, production models will replace the existing monitoring systems at various Naval Communications Stations (NAVCOMMSTA's) and will be used to perform various measurements on Navy UHF communications satellite transponders while operating in orbit.

B.   PROTOTYPE SYSTEM GOALS

The development of the prototype is based on the provision

of all equipment necessary to make real-time measurements at NAVCOMMSTA's. This equipment must have the capability to: 1) perform high speed spectral analyses and frequency measurements in the UHF (240-320 MHz) band using digital techniques; 2) monitor authorized users of the Navy SATCOM system, including the GAPFILLER and FLTSATCOM series satellites; 3) perform selective monitoring when the NAVCOMMSTA is in the footprint of multiple satellites; 4) characterize RFI signals through the use of an X-Y modulation display; and 5) operate in either manual or automatic (computer control) modes.

C. SCOPE OF THIS REPORT

Figure 1 is a block diagram of the prototype SSA system. This report documents the design and construction of the Analog-to-Digital Control and Conversion subsystem.

D. THE PROTOTYPE SSA SYSTEM

The prototype SSA system has been designed around a PDP-11/34 minicomputer. Standard peripherals have been provided which made the system self sufficient and readily adaptable to existing NAVCOMMSTA power transceiver and antenna systems. Four identical and independent receiver paths have been incorporated to enable the system to continue operation in the event of component failures in any of these channels. High speed digital processing of signal data is accomplished through the use of an Analogic AP-400 array processor which operates under control of the PDP-11/34.
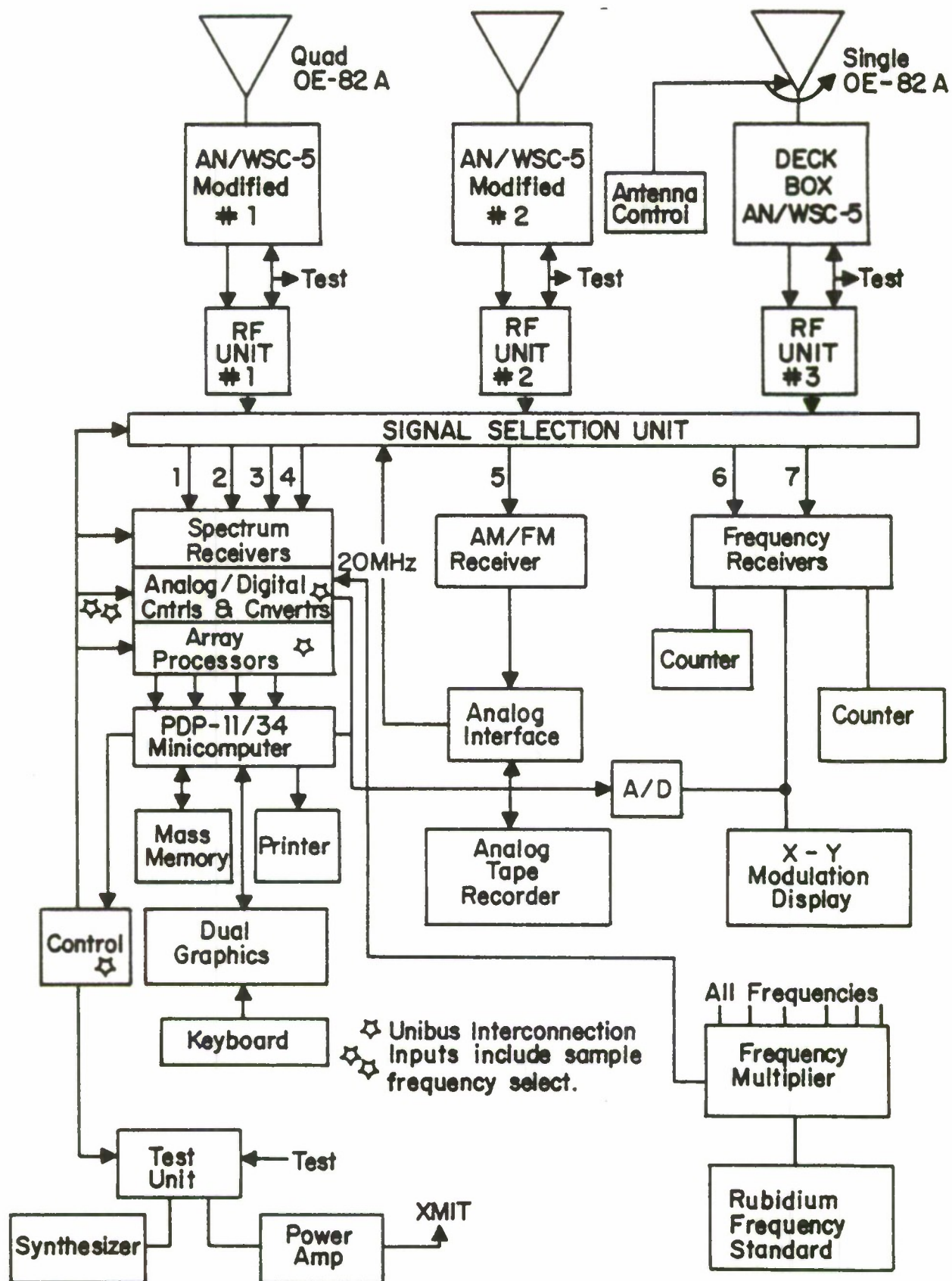
Figure 1
Block Diagram Of The Prototype SATCOM Signal Analyzer

The primary interface with the system operator is the dual graphics subsystem, consisting of two 17-inch, 60-Hz (non-interleaved), raster scan displays. Each of these units has the capability to display a single spectrum or nine separate spectra arranged in a three by three matrix format. Provisions have been made for hard copy reproduction of the information being displayed.

E. ANALOG-TO-DIGITAL CONTROL AND CONVERSION SUBSYSTEM

As may be observed in Figure 1, the Analog-to-Digital Control and Conversion subsystem is the interface between the Spectrum Receivers and the Array Processor. Within each of the four signal paths in the Spectrum Receiver, an incoming analog signal is downconverted to baseband frequency and bandwidth limited to a bandwidth appropriate to the desired spectral resolution. The Analog-to-Digital Control and Conversion subsystem converts this baseband signal into an equivalent digital "word" which in turn is presented to the AP-400 for array processor Fast Fourier Transform (FFT) processing.

In order to accomplish the above task, and to provide a high degree of flexibility in the spectral processing capabilities of the prototype SSA, design considerations required that the Analog-to-Digital Control and Conversion subsystem be capable of the following operations:

1. Sample-and-hold an analog signal at a maximum 2 MHz clock rate;

2. Analog-to-digital convert the sampled signal at a

maximum 2 MHz rate with eight bits of resolution, or a maximum 500 kHz rate with twelve bits of resolution;

3. Select sampling frequency rates for analog-to-digital conversion (ADC) under control of the PDP-11/34;

4. Select sampling frequency rates for the X-Y modulation display under control of the PDP-11/34;

5. Provide an interrupt of the ADC process in the event of failure of any of the power supplies;

6. Generate appropriate "handshake" signals to the AP-400 array processor; and

7. Be compatible in all respects with standard PDP-11/34 hardware and software.

Initial attempts to obtain an ADC system which would meet the above requirements revealed that no such units were commercially available. Accordingly, the Analog-to-Digital Control and Conversion subsystem was designed and constructed in this laboratory. The completed subsystem consists of five printed circuit (PC) boards: 1) four identical ADC boards (one per receiver signal path) which perform the actual analog-to-digital conversions; 2) one ADC Control Board which controls each of the ADC Boards and is in turn controlled by the Control Bus (also designed at NPS) which is driven by a DRIIC via the UNIBUS; and 3) an ADC Test Box to enable limited testing of any of the ADC Boards.

II. DESIGN CONSIDERATIONS

A. BASIC DESIGN CONSIDERATION

The prototype SSA system as depicted in Figure 1 was designed to be completely contained (with the exception of OE-82A antenna and AN/WSC-S transceivers) within five standard 19 inch racks. This represents a dramatic space reduction when compared with the SATCOM Signal Analyzer (developmental version) which performs the same functions (see references 4-6) as the prototype system but occupies 13 racks. Analogously, the Data Acquisition Unit of the SSA (developmental version) occupies one-half of a rack while the Analog-to-Digital Control and Conversion subsystem of the SSA prototype is wholly contained on five PC boards. Much of the reduction of space was obtained by performing the analog-to-digital conversions in the single vice dual channel mode.

B. SINGLE VERSUS DUAL CHANNEL ANALOG-TO-DIGITAL CONVERSION

As described in Appendix A, dual channel analog-to-digital conversion involves the simultaneous mixing (down-conversion) of an RF or IF signal with two equal magnitude, quadrature phase related local oscillator frequencies. The two down-converted signals are thus in phase quadrature with each other so that after analog-to-digital conversion, may be thought of as representing the "real" and "imaginary" components of a complex waveform. On the other hand, single

channel analog-to-digital conversion involves the mixing of an RF or IF signal with a single local oscillator frequency. Analog-to-digital conversion of this down converted signal results in a representation of the "real" component of a waveform. Each of these conversion schemes offers advantages to the system designer.

1. Sampling Requirements

Nyquist sampling theory states that an analog signal may be completely reconstructed from sampled values if the sampling rate is at least twice the highest frequency component contained within the signal. For spectral analysis this implies that each resolution unit (frequency line) requires two samples values. Dual channel conversion inherently provides these two values in the form of a "real" and "imaginary" component for each resolution unit, and sampling may thus be carried out at a rate equal to the highest frequency component within the analog signal. Therefore, for a given analog-to-digital converter, dual channel conversion offers the opportunity to either examine twice the bandwidth or operate at one-half the rate as in the single channel case. Inasmuch as the technology exists to adequately support the higher sampling rates required in single channel conversion, this limitation was considered acceptable in the design of the Analog-to-Digital Control and Conversion subsystem.

2. Hardware Requirements

Dual channel analog-to-digital conversion requires two identical processing channels (sample-and-hold modules,

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analog-to-digital converters, supporting circuitry) to simultaneously convert the quadrature related analog signals into the "real" and "imaginary" components of a complex data point. Single channel conversion requires only one processing channel, thereby reducing the number of components by one-half. This was considered highly advantageous in light of the space limitations imposed on the SSA prototype design.

3. Image and Zero Frequency Considerations

Performing spectral analysis by the dual channel technique results in a displayed spectrum which may contain misleading information. As explained in Appendix A, dual channel conversion results in a D.C. value in the baseband signal which represents the component of the RF signal at the local oscillator frequency. This appears in the spectral display as a signal at D.C. or zero frequency. Similarly, image frequencies may appear in the spectral display due to imbalances in the gains of the processing channels in the dual channel case. Either zero or image frequencies could lead the unsuspecting system operator to erroneously conclude that the R.F. signal contained components that are not in fact present. The fact that neither of these phenomena are present in single channel conversion, coupled with the fact the production versions of the SSA may eventually be operated by unsophisticated operators, make the latter technique both advantageous and desirable.

4. System Compatibility

Both conversion techniques are easily adaptable to

digital processing. However, dual channel conversion requires double the amount of computer interface for adequate control and monitoring and may restrict the flexibility of the host computer. Additionally, the single channel conversion technique lends itself readily to audio monitoring (and recording) of the baseband signal. This capability does not exist in the dual channel case as a result of the pre-baseband division of the analog signal.

C. EQUIPMENT SELECTION

1. Sample Rate Requirements

The minimum acceptable sampling rate for the Analog-to-Digital Control and Conversion subsystem is the Nyquist rate (see Section II. B. 1.). When this criterion is applied to a baseband signal, the sampling rate equals twice the bandwidth of that signal. However, if the bandwidth is taken, as is usually the case, as the half-power (or 3 dB) bandwidth, consideration must be given to aliasing. Aliasing results from the fact that a rectangular bandpass filter (BPF) is virtually impossible to implement and that a signal passed through such a BPF will have sloping, rather than abrupt, leading and trailing edges. If this signal is then sampled at the Nyquist rate, considerable distortion in the resultant spectrum may occur. The solution to aliasing is to sample at a rate based on a wider bandwidth, i.e., the 30 dB down bandwidth, where the effects of aliasing are not as significant. In the design of the Analog-to-Digital Control and Conversion subsystem, a rate of 2 MHz was considered

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adequate to successfully sample the satellite's wideband transponder channel while a rate below 500 kHz was deemed appropriate for sampling the narrowband channels.

2. <u>Bit Resolution Requirements</u>

The analog-to-digital conversion of any signal results in the generation of quantization noise which is added onto the noise of the input signal. The quantization noise effect is 6 dB of SNR per bit of resolution. Determination of the number of bits used in the digital representation of the analog signal is thus a tradeoff between the desired dynamic range of the analog-to-digital converter and tolerable levels of quantization noise. Experience gained in this laboratory while operating the developmental SATCOM Signal Analyzer (see references 4-6) indicated that eight bits of resolution were adequate for the wideband channel and were within the realm of existing technology. Similarly, 12 bits of resolution were considered adequate for the representation of signals in the narrowband channels.

3. <u>Equipment Selection</u>

The major functional components of the Analog-to-Digital Control and Conversion subsystem are the sample-and-hold module and two analog-to-digital converters. For purposes of clarification, the remainder of this thesis will refer to the high-speed analog-to-digital converter as that converter which operates at a 2 MHz rate and provides eight bits of resolution; the low-speed analog-to-digital converter as the converter which operates at or below a 500 kHz rate

providing 12 bits of resolution. Selection of the components to be used to fulfill the design requirements involved comparisons of existing hardware based on the following factors:

a. Specifications;

b. Cost;

c. Power supplied required;

d. Power dissipation; and,

e. Size

Based on the above criteria, the sample-and-hold module and low-speed analog-to-digital converter selected were the DATEL SHM-UH and DATEL ADC-EH12B3, respectively. In the case of the high-speed analog-to-digital converter, three units were selected for laboratory evaluation--the DATEL ABC-VH8B3, the TRW TDC-1001J, and the DDC (Digital Devices Corporation) ADC-1210. In each case the evaluation consisted of implementing the device, its supporting circuitry and power supplies on SK-10 breadboards and then applying signals similar to those which would be encountered in the operating system. Upon completion of the evaluations the TRW TDC-1001J was selected as the high-speed analog-to-digital converter.

III.   DETAILED OPERATION

A.   INTRODUCTION

The Analog-to-Digital Control and Conversion subsystem receives a baseband analog signal from each of the four channels of the Spectrum Receiver. Within the subsystem these four analog signals are independently analog-to-digital converted at various sampling rates determined by the system operator. The resultant digital representations of the analog inputs are then presented to a bank of four array processors for Fast Fourier Transform processing (see Figure 2). The subsystem consists of four identical printed circuit (PC) boards (ADC Boards) containing the analog-to-digital conversion circuitry and one PC board (ADC Control Board) containing the requisite circuitry to control the four ADC Boards and the X-Y display analog-to-digital converter. The system operator may perform limited testing on any of the ADC Boards through the use of the ADC Test Box in conjunction with the ADC Control Board. Table I provides the required external inputs and outputs of this subsystem.

B.   ADC BOARD

1.   Introduction

a.   Functions

Each of the four ADC Boards perform the following functions: 1) sample-and-hold an incoming signal at a maximum

Figure 2

Analog-to-Digital Control and Conversion Subsystem Block Diagram

* — Cable assembly carrying HI/LOW-SELECT, SAMPLE-ENABLE, 20 MHz clock and Sample Frequency clock

** — Cable assembly carrying Sample Frequency and 20 MHz clocks

*** — Ribbon cable carrying Sample-Frequency-Select signals

TABLE I

ANALOG TO DIGITAL CONTROL AND CONVERSION
SUBSYSTEM INPUT/OUTPUT SPECIFICATIONS

Power Supplies: +5 volts, ± 15 volts (provided
                                          by chassis connections)

Analog Inputs:

  Number   4 (1 per Spectrum Receiver
                                          channel)

  Voltage Range   ± 10 volts

  Maximum input Voltage   ± 15 volts

Reference Input: 20 MHz @ 13 dBm (sine wave)

Sampling Rates:

  High Speed   2 MHz

  Low Speed Range   781 Hz - 500 kHz (selectable)

  Selection Control   3 bits per analog input

Digital Outputs:

  Format   Two's complement or offset
                                          binary (selectable)

  Low Speed   One 12 bit word

  High Speed   Two 8 bit words (successive
                                          sample values) in parallel

  Handshake   150 nanosecond positive pulse
                                          (AP-400 compatible)

Clock Outputs for X-Y ADC:

  Reference   20 MHz square wave

  Sample Frequency Range   781 Hz - 96.2 kHz

  Selection Control   2 bits

2 MHz clock rate; 2) analog-to-digital convert the sampled signal at one of five sampling rates; 3) output digital data in a format compatible with the AP-400 (array processor); and, 4) generate "handshake" signals to the AP-400. As previously mentioned, each of the ADC Boards operates in conjunction with one channel of the Spectrum Receiver subsystem. Inasmuch as the ADC Boards are identical, future reference in this thesis to "the" board may be taken to mean any one of the ADC Boards. A generalized block diagram of the operation of the ADC Board is provided as Figure 3.

   b.   Inputs

        The ADC Board receives all operating and control signals from the ADC Control Board. These signals are as follows:

   (1)   Sample-Frequency Clock;

   (2)   HI/LOW-SELECT Signal;

   (3)   SAMPLE-ENABLE Signal; and,

   (4)   20 MHz reference Clock

These signals and their functions will be explained in detail later in this thesis. The ADC Board also receives the base-band analog signal from the corresponding channel of the Spectrum Receiver.

   c.   Outputs

        The ADC Board generates a 12 bit digital representation of the input analog signal while operating in the low-speed mode and an eight bit representation in the high-speed mode. The appropriate digital signals to the mode of
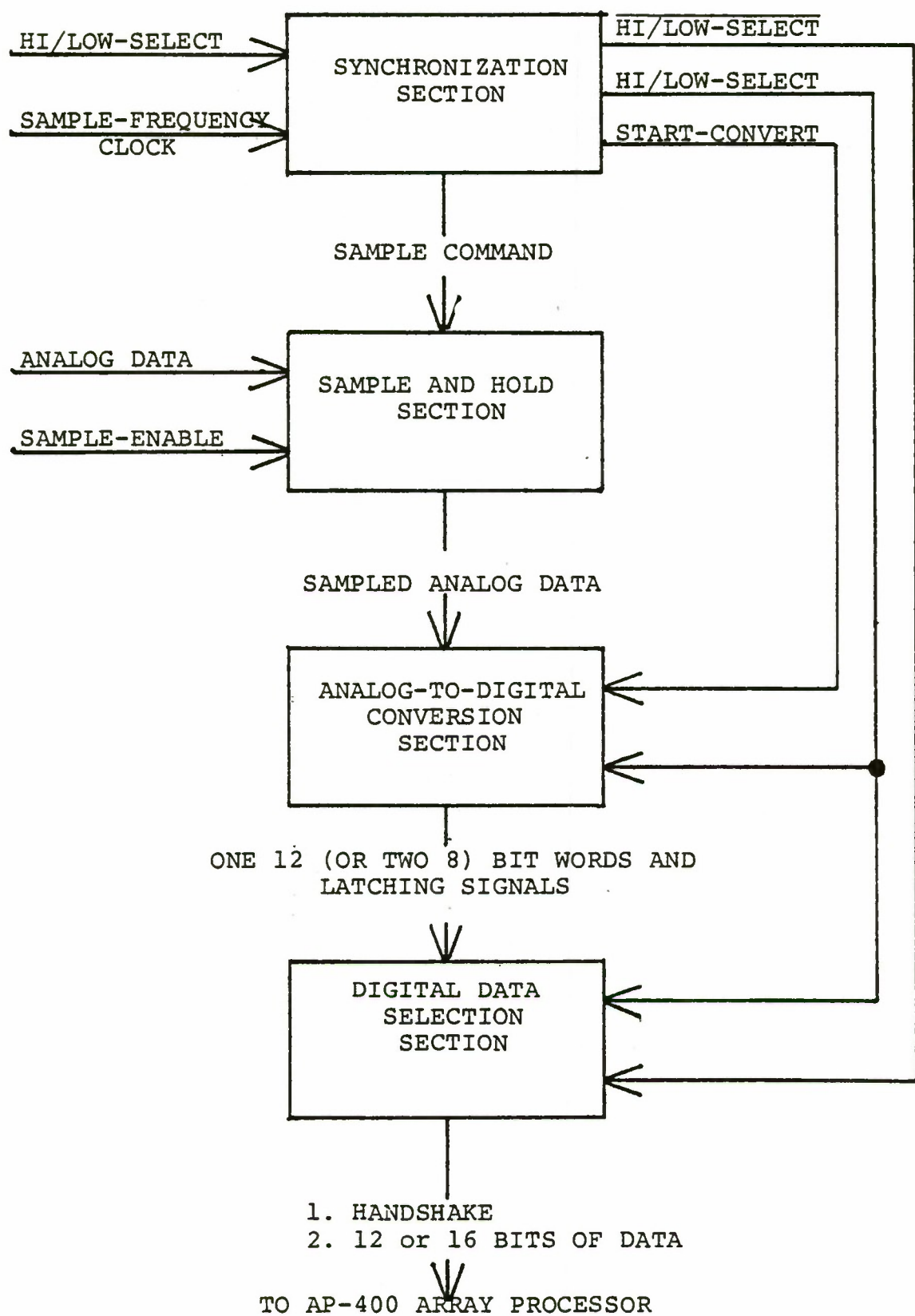
Figure 3
ADC BOARD OPERATION

operation and the "handshake" signal are routed to the AP-400 array processor. Additional outputs include a +5 volt signal which is provided to the ADC Test Box and a common GROUND signal provided to the ADC Control Board.

d. Implementation

The ADC Board is wholly contained on a standard PDP-11 QUAD size printed circuit (see Figure 4). Design layout and basic board construction were accomplished through the use of the facilities of the Etching Laboratory at NPS. The ADC Boards are designed to be mounted vertically on, and draw all power (+5 volts, $\pm$5 volts, GROUND) from, a standard PDP-11 backplane contained within a PLESSEY PM-1150/5 power chassis. Inputs from the ADC Control Board are brought onto the board via a CANNON DAM-7W25A Connector assembly which has provisions for two coaxial fittings and five standard pin connections. The signals carried by coaxial cable (20 MHz reference clock and Sample Frequency clock) are routed to their destinations via cable on the component side of the board. The analog signal interfaces with the ADC Board through a standard SMA Bulkhead fitting. Outputs from the ADC Board to the AP-400 exit the board via an ANSLEY 609-615M 34 pin ribbon cable mating connector. The GROUND and +5 volt outputs (to the ADC Control Board and ADC Test Box, respectively) are routed via the CANNON 7W25A connector. Pin connections for all connectors and backplane slots may be found in Appendix D.

Figure 4
ADC Board Component Layout
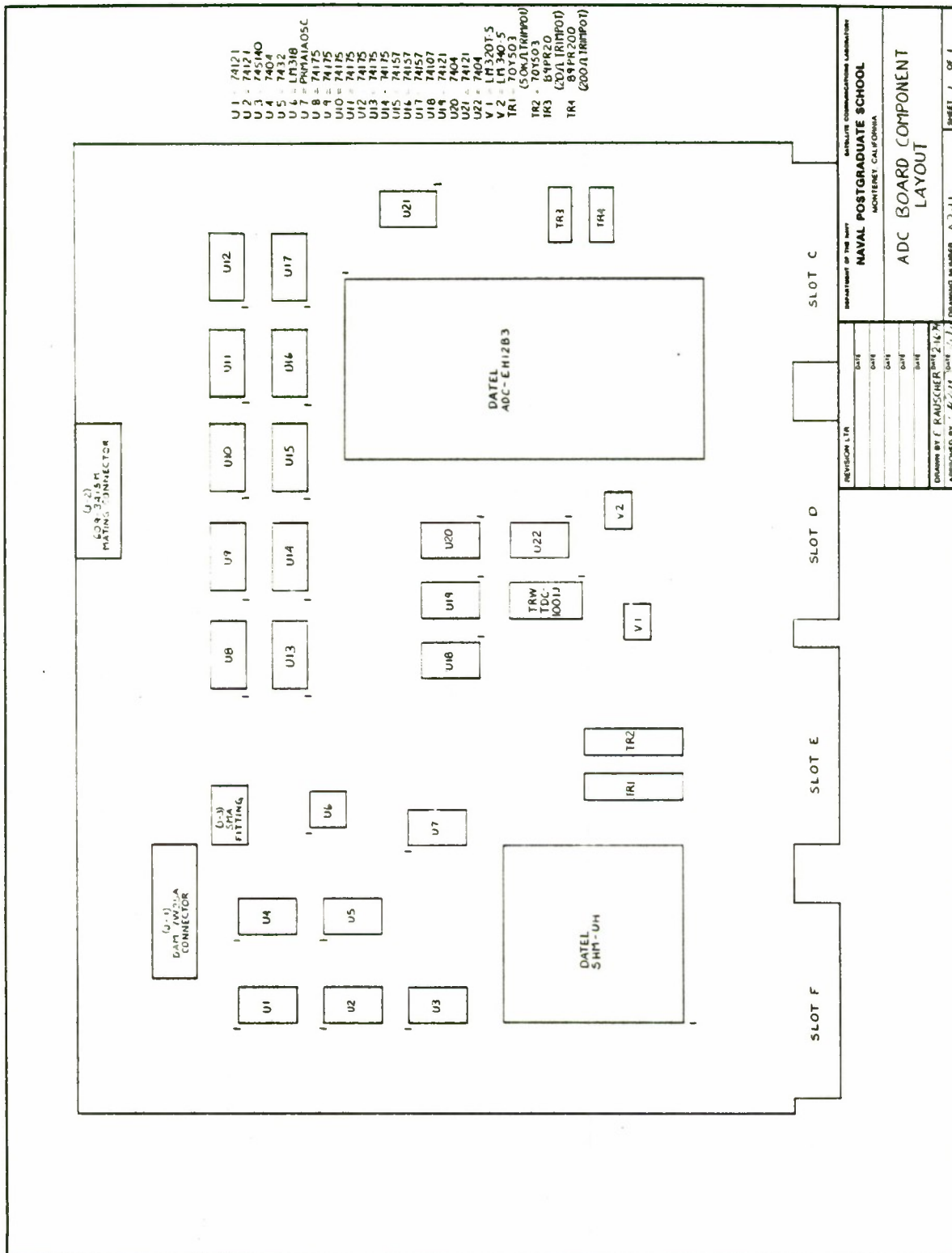
e. ADC Board Sections

The ADC Board has been subdivided into five functional sections. This division not only simplifies discussion of board operation but also represents an orderly progression in the signal processing which occurs on the board. The four sections are the Synchronization section, the Sample-and-Hold section, the Analog-to-Digital Conversion section and the Digital-Data-Selection section. An in-depth discussion of ADC Board operation will be accomplished by considering the operations performed within each section. The reader is advised to familiarize himself with Figure 3 prior to the reading of the following sections.

2. Synchronization Section

a. Introduction

The Syncrhonization section performs the following functions: 1) generation of the Sample-Command signal; 2) generation of the Start-Convert signals for both analog-to-digital converters; 3) buffering and inversion of the HI/LOW-SELECT signal; and, 4) selective enabling of the low-speed Start-Convert signal. The schematic diagram for this section is given in Figure 5, while Figure 6 depicts the time relationship among the various pulses generated in this section.

b. Master Pulse

The 40 nanosecond positive-going Master Pulse (MP) and its complement ($\overline{\text{MP}}$) are generated by U1, a 74121 monostable multivibrator. Triggering information is provided by the trailing edge of the Frequency clock which arrives

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Figure 5
Synchronization Section Circuit Diagram
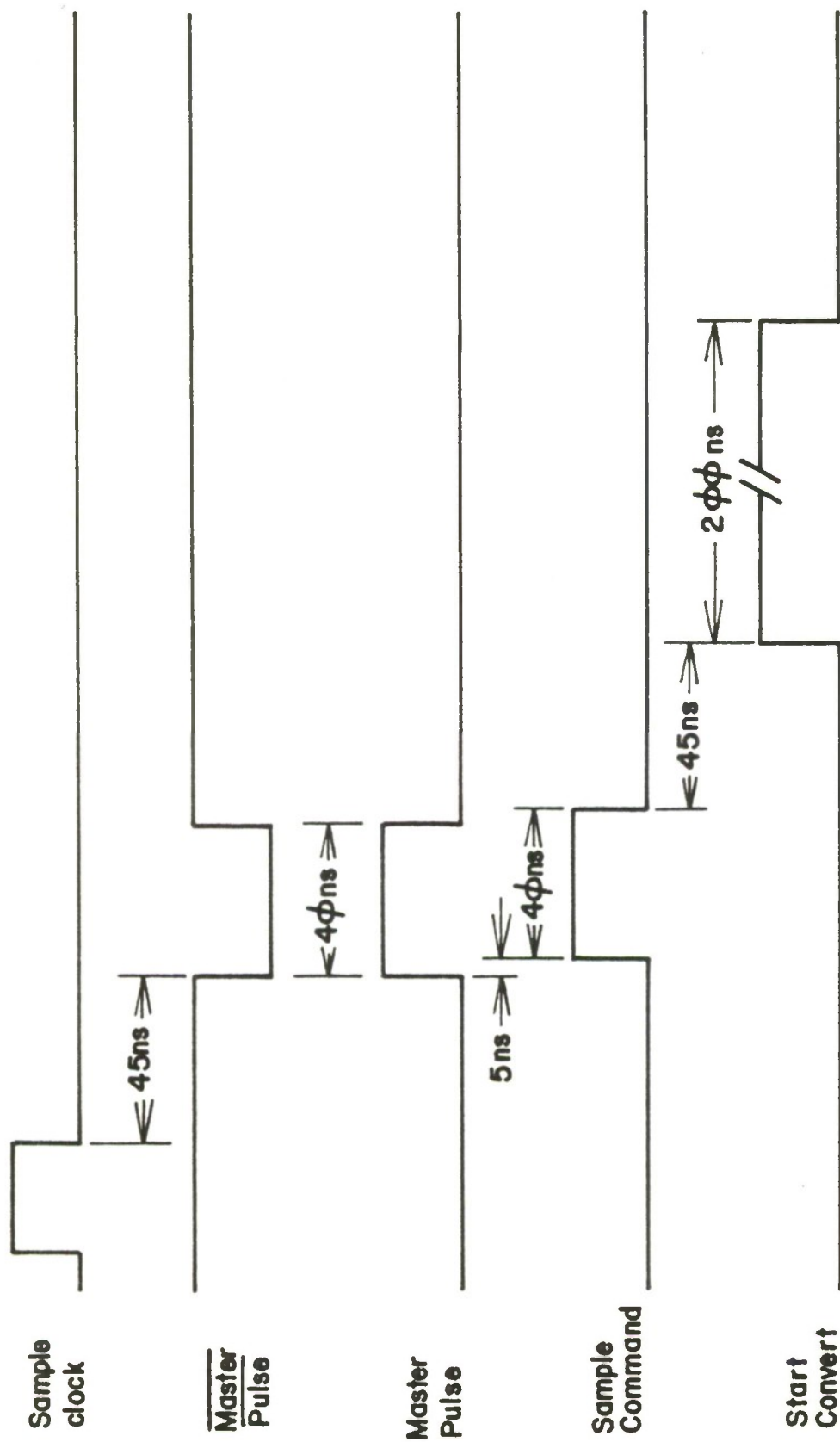
Figure 6
Synchronization Section Timing Diagram

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directly at pins 3 and 4 via the center conductor of a coaxial cable. The braid of the cable is grounded adjacent to the integrated circuit and a 50 ohm impedance matching resistor is placed across the braid and center conductor. The width of the Master Pulse is determined by the internal resistor/25 picofarad capacitor combination and was selected to meet the 35 nanosecond ($\pm$ 10 nanosecond) requirement of the sample-and-hold module with tolerance for variations in capacitor and resistor values.

      c. Sample-Command Pulse

      The sample-and-hold module (DATEL SHM-UH) requires a Sample-Command signal of the previously mentioned width which is capable of sourcing 100 milliamperes of current. Accordingly, the complement of the Master Pulse ($\overline{MP}$) is simultaneously provided to pins 1 and 13 of U3, a 74S140 dual 50 ohm line driver. All other inputs to U3 are held high so that the negative going pulse ($\overline{MP}$) results in a positive pulse at the outputs. These outputs are combined, and, in conjunction with a 100 ohm pull up resistor, provide the Sample-Command pulse which is of correct width and current sourcing capability to drive the sample-and-hold module.

      d. Start-Convert Pulse

      A 200 nanosecond positive going pulse is used as the Start-Convert pulse for both analog-to-digital converters. This width was selected to exceed the minimum requirements (high speed converter--50 nanoseconds, low speed--100 nanoseconds) and to provide adequate tolerance for resistor/

capacitor values. The pulse is generated by U2, a 74121 mono-
stable multivibrator with the width controlled by a 3.3 kilohm/
82 picofarad combination across pins 10, 11 and 14. Trigger-
ing is supplied by the trailing edge of the Master Pulse,
applied to pins 3 and 4. Use of this pulse for triggering
provides approximately 85 nanoseconds of delay from the be-
ginning of the sampling evolution until the analog-to-digital
conversions begin, thus assuring that the acquisition time of
the sample-and-hold (50 nanoseconds) has elapsed.

      e. HI/LOW-SELECT Signal Buffering and Inversion

      The HI/LOW-SELECT signal and its complement are
the most widely used control signals in the analog-to-digital
conversion process. Because of the number of loads it drives
on the ADC Board, it is buffered by double inversion at U4, a
HEX Inverter. The complement ($\overline{\text{HI/LOW-SELECT}}$) is generated
by a single stage of inversion. In the Synchronization sec-
tion, the HI/LOW-SELECT signal is used to enable the low-
speed Start-Convert signal. This enabling is required due
to the low-speed analog-to-digital converter having a maxi-
mum conversion rate to 500 kHz. The use of a common Start-
Convert signal to both converters implies that in the high-
speed mode (conversion rate = 2MHz), the low-speed converter
would be driven at four times its maximum rate. To avoid
this situation, the low-speed Start-Convert pulse-train is
logically OR-ed with the HI/LOW-SELECT signal (at U5), pro-
ducing a constant "high" output and thereby disabling the low-
speed converter.

3. Sample-and-Hold Section

a. Introduction

In the Sample-and-Hold section the analog signal from the associated channel of the Spectrum Receiver is sampled at the desired sample rate. The section is designed around the DATEL SHM-UH sample-and-hold module and associated protection circuitry. The schematic diagram for this section is given in Figure 7.

b. LM-318 Operational Amplifier

As shown in Figure 6, the baseband analog signal is applied to a unity gain LM-318 Operational Amplifier (OP-AMP) designed to operate in the differential mode. This configuration reduces ground loop noise. Laboratory experimentation revealed that operation in this mode with $\pm$ 15 volt power supplied results in a saturation voltage of $\pm$ 14 volts, which exceeds the input overvoltage protection range of the SHM-UH. The solution to this potential problem will be discussed in the following section.

c. Power and Overvoltage Protection

Experience in the operation of the SHM-UH in this laboratory has demonstrated that it is susceptible to failure if an analog signal is applied to the module without all power supplies operating. In order to avoid this occurrence, a CLARE PRMA1A05C reed relay was placed between the LM-318 OP-AMP and the analog input of the SHM-UH. The controlling voltage for this relay is the SAMPLE-ENABLE signal which is generated on the ADC Control Board. As previously mentioned,
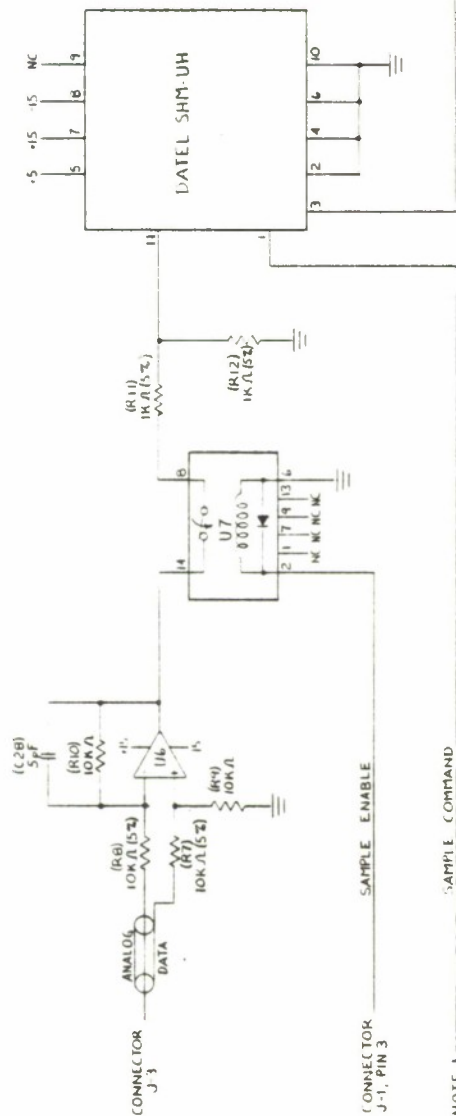
Figure 7

Sample And Hold Section Circuit Diagram

the input overvoltage protection range of the SHM-UH ($\pm$ 10 volts) is less than the saturation voltage of the LM-318 OP-AMP. In order to protect against over-voltage inputs, a two-to-one divider network has been implemented immediately prior to the reed relay which ensures that the maximum input voltage to the SHM-UH is approximately $\pm$ 7 volts.

d.   Sample-and-Hold Module, DATEL SHM-UH

The analog baseband signal from the Spectrum Receiver is sampled by the DATEL SHM-UH sample-and-hold module. It is controlled by the 40 nanosecond Sample-Command input generated in the Synchronization section and has a $\pm$ 5 volt full scale input range. The device is capable of operation at a sampling rate of 10 MHz which is well in excess of the maximum rate employed in this system. The output sampled values are noninverted $\pm$ 5 volt levels which are directly compatible with the input of the low-speed analog-to-digital converter and require reduction and offset to ensure compatibility with the high-speed converter input range. The SHM-UH has an internal offset trimpot which is adjusted according to the instructions contained in Appendix C. Detailed specifications of the SHM-UH may be found in Appendix B.

4.   Analog-to-Digital Conversion Section

a.   Introduction

The Analog-to-Digital Conversion section performs two functions: 1) analog-to-digital conversion of the sampled analog data with eight or twelve bits of resolution; 2) generation or conditioning of End-of-Convert (EOC) signals

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to ultimately be used as latch commands. The section was
designed around the DATEL ADC-EH12B3 and TRW TDC-1001J ana-
log-to-digital converters and all supporting circuitry.
Figure 8 is a schematic diagram for this section.

   b.   Low-Speed Analog-to-Digital Converter, DATEL
        ADC-EH12B3

        Sampled analog signal values from the SHM-UH
are routed directly to the DATEL ADC-EH12B3. This device
provides a 12 bit representation of the input signal value
and is capable of operation at a maximum rate of 500 kHz.
It is controlled by the 200 nanosecond Start-Convert pulse
generated in the Synchronization section. As demonstrated
in Figure 9, the parallel output data and EOC signal are
available approximately 2 microseconds after the leading
edge of the Start-Convert pulse. The twelve bits of paral-
lel output data is available in offset binary or two's com-
plement format. The preferred option is selected through
the use of a jumper wire on the reverse side of the ADC Board.
Connecting the cable between pads J and A provides the offset
binary format while connecting the wire between pads J and B
provides the two's complement format (see Table II). The EOC
signal is a negative-going pulse which occurs 100 nanoseconds
after the conversion is complete. This signal is then triple
inverted by the inverters in U20 and provided to the Digital-
Data-Selection section for use as a latching signal. Instruc-
tions for the adjustment of the external 20 ohm trimpot (GAIN
ADJUST) and 200 ohm trimpot (OFFSET ADJUST) are located in
Appendix C, while Appendix B provides detailed operating

Figure 8

Analog-to-Digital Conversion Section Circuit Diagram
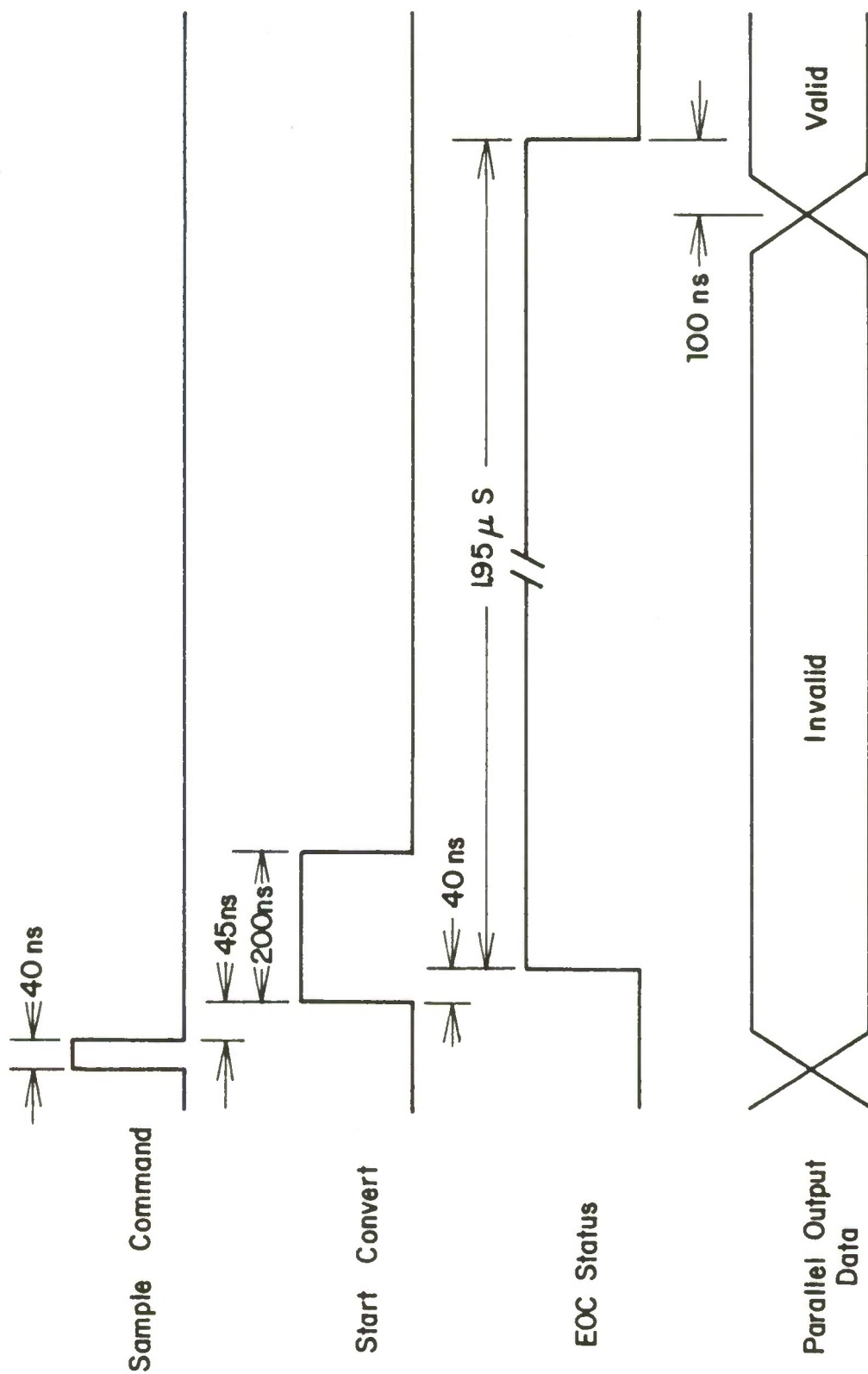
Figure 9
Low Speed Analog-To-Digital Conversion Timing Diagram

TABLE II

OFFSET BINARY AND TWO'S COMPLEMENT DATA FORMATS

LOW-SPEED CONVERSION FORMATS

Analog Input Voltage	Offset Binary (J-A Connection)*			Two's Complement (J-B Connection)*		
+5.00 volts	1111	1111	1111	0111	1111	1111
+2.50 volts	1100	0000	0000	0100	0000	0000
0.00 volts	1000	0000	0000	0000	0000	0000
-2.50 volts	0100	0000	0000	1100	0000	0000
-5.00 volts	0000	0000	0000	1000	0000	0000

*Pads A, B and J are located adjacent to pin 1 of the
ADC-EH12B3 module.

HIGH-SPEED CONVERSION FORMATS

Analog Input Voltage	Offset Binary (J-A Connection)*		Two's Complement (J-B Connection)*	
0.000 volts	1111	1111	0111	1111
-.125 volts	1100	0000	0100	0000
-.250 volts	1000	0000	0000	0000
-.375 volts	0100	0000	1100	0000
-.500 volts	0000	0000	1000	0000

*Pads A, B and J are located adjacent to pin 1 of U22.

specifications of the ADC-EH12B3.

      c.   High-Speed Analog-to-Digital Converter, TRW TDC-1001J

The TRW TDC-1001J analog-to-digital converter provides an eight bit representation of the analog input value and is capable of operation at a maximum rate of 2.5 MHz. The input analog voltage range is $\pm$ .25 volts around a center value of -.25 volts, which requires an offset and range adjustment of the sampled values originating at the SHM-UH sample-and-hold module. The range adjustment was accomplished by a twenty-to-one voltage division of the analog signal and offset adjustment was similarly accomplished by ten-to-one voltage division of the -5 volt power supply. Instructions for the requisite adjustment of the 50 kilohm trimpot to obtain the offset value are found in Appendix C. Laboratory experimentation revealed that this module is highly susceptibel to instabilities in the $\pm$ 5 volt power supplies. Inasmuch as -5 volts is not available on the PDP-11 backplane, and to provide essentially ripple free supply voltages, it was decided to provide these supplies by $\pm$ 5 volt regulators. The reference input (-5 volts) applied to pin 13 is obtained by a ten-to-one division of the -5 volt regulator output through the use of a fixed 1 kilohm resistor and a 50 kilohm trimpot. Appendix C contains instructions for this adjustment. The 20 MHz reference clock required by this module is applied directly to pin 18 via the center conductor of a coaxial cable which is terminated across a 50 ohm impedance matching resistor. The output of the TDC-1001J is eight bits of parallel

data presented in inverted offset binary format, i.e., the more negative full scale value (-.5 volts) appears as eight logical "ones". Converting this output to a true offset binary format is accomplished through the use of inverters in U20 and U22. The output of these inverters may be converted into two's complement or offset binary format by making the same pad/jumper cable connections as in the low-speed case (see Table II). The EOC signal is used to control the output latch register internal to the device and thus occurs approximately 110 nanoseconds prior to the output data being available at pins 3-9 and 11 (see Figure 10). The disparity in time, and the unique output format from the ADC Board to the AP-400 while operating in the high-speed mode, make this EOC signal unsuitable for use in the Digital-Data-Selection section which requires two separate latching signals during high-speed operation (see Section III, B.5.). Accordingly, the TDC-1001J EOC signal is applied as the triggering signal to U19, a 74121 monostable multivibrator, generating a 150 nanosecond positive-going pulse. This pulse is in turn applied as the clock signal to a negative edge triggered J-K flip-flop (contained in U19) which is configured in the toggle mode. The use of the trailing edge of the pulse generated in U19 as the clock signal to U18 ensures that the positive transitions occurring at either the Q or $\overline{Q}$ outputs are sufficiently delayed to act as latching commands. The flip-flop is enabled by the HI/LOW-SELECT signal and thus is disabled during operation in other than the high-speed mode.
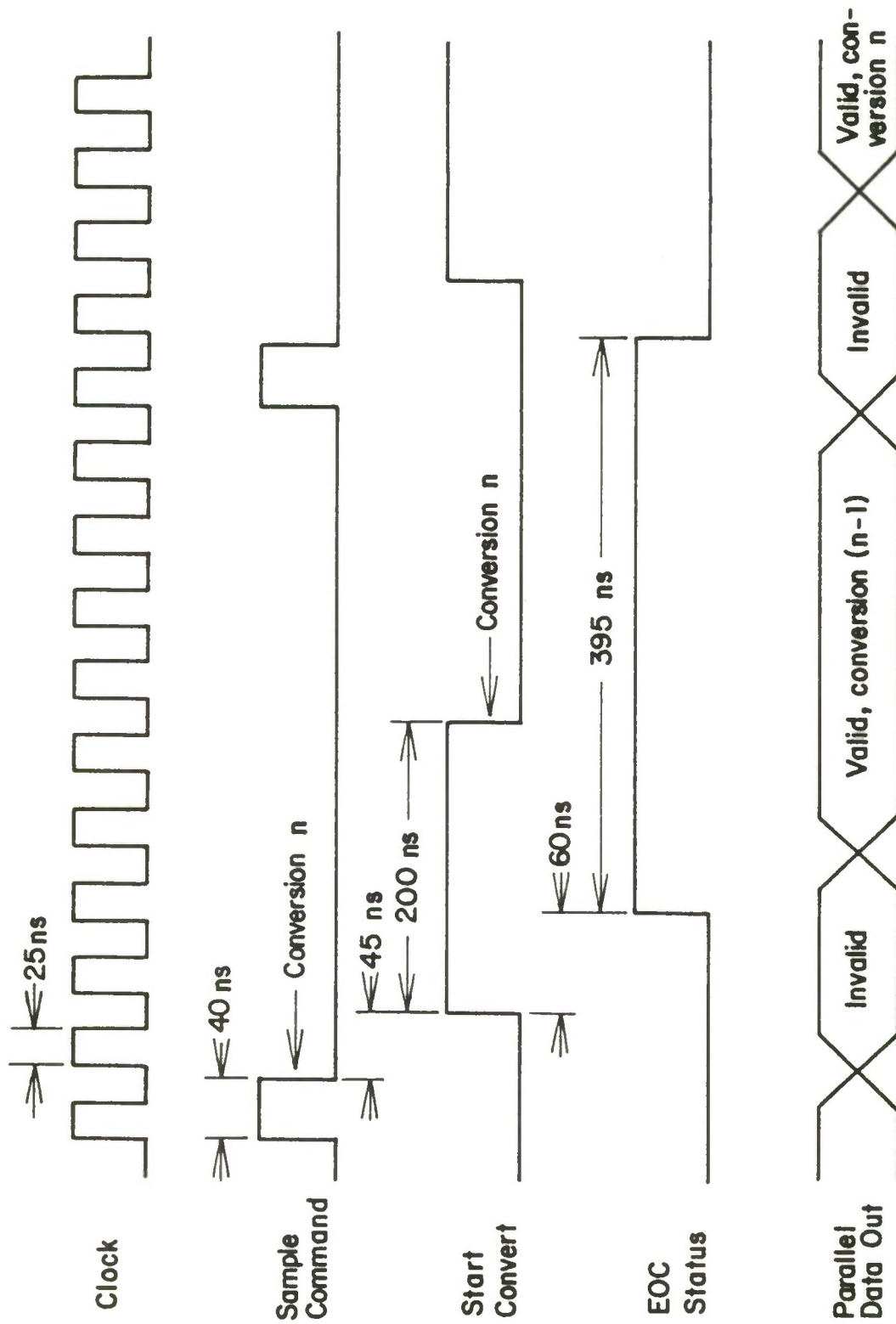
Figure 10
High Speed Analog-to-Digital Conversion Timing Diagram

The Q output of the J-K flip-flop makes a positive transition upon the completion of the first conversion after the high-speed mode is selected (and all subsequent odd numbered conversions) and hence is referred to as HIGH-SPEED-WORD-ONE-EOC. Similarly the $\overline{Q}$ output makes a positive transition upon completion of the second conversion (and all subsequent even numbered conversions) and is referred to as HIGH-SPEED-WORD-TWO-EOC.

5. Digital-Data-Selection Section

    a. Introduction

        The Digital-Data-Selection section performs three functions: 1) multiplexing of digital data and latching commands to the output latches; 2) latching the output data; and, 3) generation of the "handshake" signal to the AP-400. The schematic of this section is shown in Figure 11.

    b. Output Formats

        The outputs from the Digital-Data Selection section are provided directly to the AP-400 array processor. This device accepts up to 24 bits of data at a maximum 1 MHz rate, and is capable of processing these data bits (under PDP-11/34 control) as either one "word" or two "words" (of 16 and eight bit lengths). The AP-400 may be programmed to read any number of these bits in either format. In the low-speed mode of operation the 12 bits of output data are routed to the AP-400 inputs reserved for the 16 bit "word" and all nondata inputs are ignored. In the high speed mode two eight bit "words" are "packed" into the first eight inputs of the 16

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Figure 11

Digital Data Selection Section Circuit Diagram

bit "word" and all eight inputs of the eight bit "word", and the array processor is programmed to read these 24 bits as one "word" but to interpret them as two separate sample values. This technique allows the analog-to-digital conversions to be performed at a 2 MHz rate with the digital outputs being processed at a 1 MHz rate with no inherent loss of data. The required "handshake" signal to the array processor (IP/TRS INTERRUPT) is a 150 nanosecond positive-going pulse indicating that data is ready at the processor inputs. This signal is generated by U21, a 74121 monostable multivibrator, with a 2.7 kilohm resistor/68 picofarad capacitor combination across pins 10, 11 and 14. During low-speed operation, triggering is provided by the ADC-EH12B3 $\overline{EOC}$ signal while in the high-speed mode the trigger is provided by the HIGH-SPEED-WORD-TWO-EOC.

c. Data Latching

As demonstrated in Figure 11, output data from the Digital-Data-Selection section is made available to the AP-400 at various combinations of five 74175 quad memory latches (U8-U12). In the low-speed mode of operation, the 12 output bits appear at the outputs of U10-U12, with latching commands supplied by the positive transition of the ADC-EH12B3 $\overline{EOC}$ signal. The unused output latches (U8, U9) are disabled by the application of the HI/LOW-SELECT signal to pin one of both IC's. During high-speed operation, the eight digital data bits of the first conversion are applied to two intermediate latches (U13, U14) with latching commands to these

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latches by the HIGH-SPEED-WORD-ONE EOC signal. Upon completion of the second high-speed conversion, these eight bits and the eight bits from the second conversion are latched directly into U8, U9, U11 and U12, respectively, with latching commands supplied by the HIGH-SPEED-WORD-TWO-EOC signal. In the high-speed mode of operation the unused output latch (U10) is disabled by the $\overline{\text{HI/LOW-SELECT}}$ signal applied to pin one of that latch. Therefore, during high-speed operation the eight output bits of the first conversion are double latched and all 16 bits are applied to the output latches simultaneously. In both high-speed and low-speed modes the "handshake" signal appears at the output approximately 40 nanoseconds after the digital data appears at the outpus of the appropriate latches. This delay is attributable to the propagation time of the monostable multivibrator (U21) generating this signal.

d. Data Multiplexing

In order to minimize the number of components utilized, the first eight data bits of the low speed mode and the eight bits from the second conversion in the high-speed mode utilize the same output latches (U11, U12). These 16 bits of data are multiplexed prior to the output latches by two 74157, quad two-to-one multiplexers (U16, U17), with selection commands provided by the HI/LOW-SELECT signal. The latching commands to the five output latches (ADC-EH12B3 $\overline{\text{EOC}}$ and HIGH-SPEED-WORD-TWO-EOC) are similarly multiplexed through an additional 74157 (U15) which also has selection commands supplied by the HI/LOW-SELECT signal.

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C. ADC CONTROL BOARD

1. Introduction

    a. Functions

        The ADC Control Board is designed to provide all
control signals to each of the four ADC Boards. Accordingly,
it performs the following functions: 1) conversion of a 20
MHz sinusoid into a 20 MHz pulse-train; 2) generation of all
five Sample-Frequency-Clock signals; 3) generation of the
SAMPLE-ENABLE signal; and, 4) generation of the HI/LOW-SELECT
signal.

    b. Inputs

        The Master Control Bus of the PDP-11/34 provides
all operating signals to the ADC Control Board. These sig-
nals include three ADC Sample-Frequency-Selection signals for
each of the ADC Boards and two Sample-Frequency-Selection
signals for the X-Y modulation display. All operating fre-
quencies in the SSA Prototype system are based on a 5 MHz
rubidium standard. The 20 MHz sinusoidal input to the ADC
Control Board is generated by the up conversion of the 5 MHz
sinusoid in the frequency multiplication unit (see Figure 1).
Additionally, the ADC Control Board shares a common GROUND
with each of the ADC Boards, the analog-to-digital converter
of the X-Y Modulation Display, the Master Control Bus, and,
when appropriate, the ADC Test Box.

    c. Outputs

        The ADC Control Board outputs the following sig-
nals to each of the ADC Boards:

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(1)   20 MHz reference clock;

(2)   Sample frequency clock;

(3)   SAMPLE ENABLE signal;

(4)   HI/LOW SELECT signal.

Additionally, both of the clock signals are provided to the analog-to-digital converter of the X-Y Modulation Display.

d.   Implementation

The ADC Control Board was designed for implementation on a standard PDP-11 QUAD size printed circuit board with a two inch extension in the direction of slot B (see Figure 12). Use was made of the facilities of the NPS Etching Lab in the design layout and basic construction of the ADC Control Board. Inputs from the Master Control Bus arrive at this board via a ANSLEY 609-615M 16-pin ribbon cable mating connector which is equipped with a polarizing key to avoid incorrect mounting. The 20 MHz sinusoid is applied via coaxial cable to a standard SMA Bulkhead fitting. Outputs to each of the four ADC Boards are routed via four CANNON 7W25A connectors which, as mentioned previously, have provisions for two coaxial fittings and five standard pin connections. The two clock signals for the X-Y Modulation Display exit the board via the outer two (of three) coaxial fittings on a CANNON 3W3S connector. The ADC Control Board will be mounted adjacent to the four ADC Boards within the PLESSEY power chassis and will draw all power supplies (+5 volts, $\pm$15 volts, GROUND) from appropriate connections on the PDP-11 backplane. Appendix D provides a listing of pin connections for all
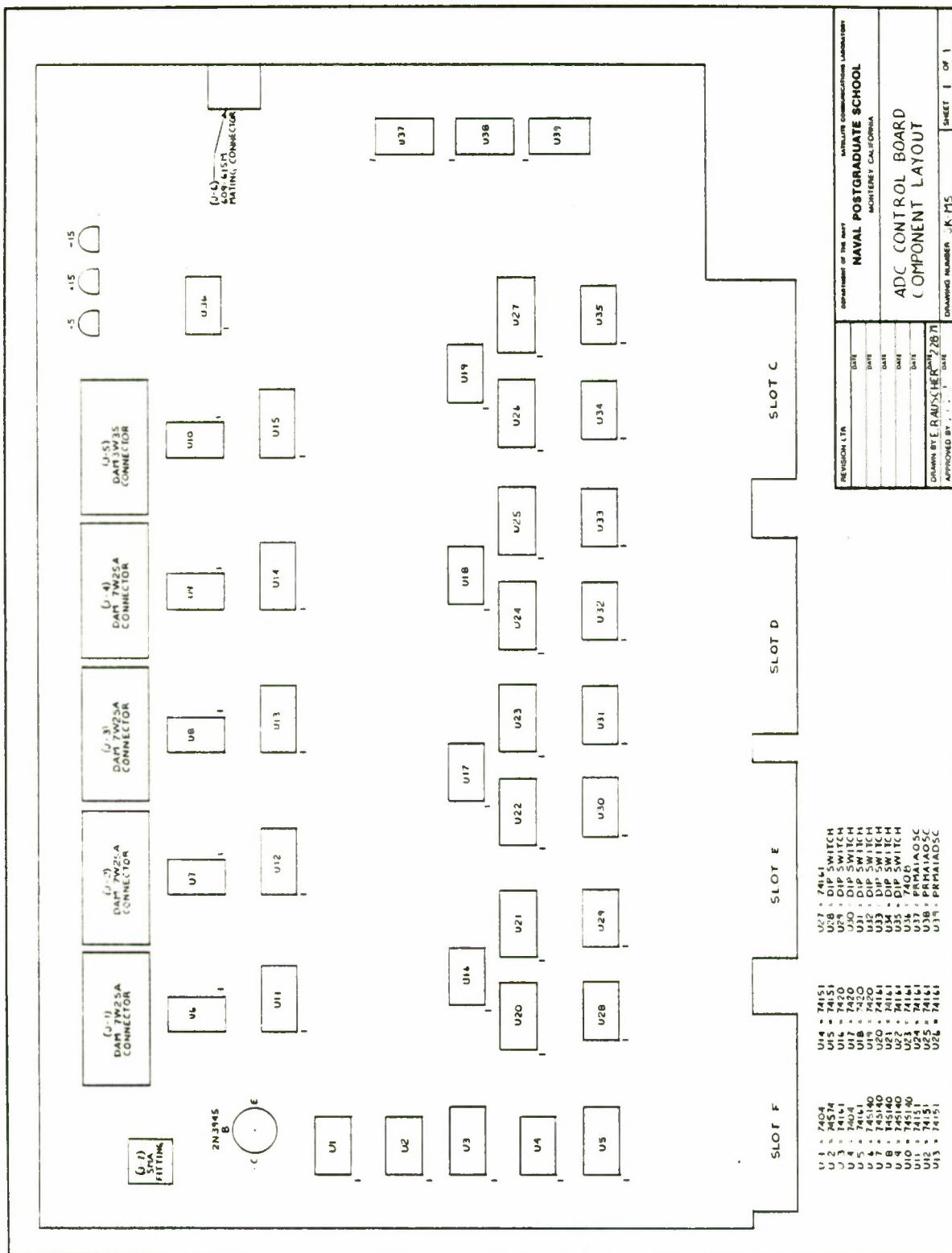
Figure 12

ADC CONTROL BOARD COMPONENT LAYOUT

connectors and backplane slots.

    e. ADC Control Board Section

        As in the case of the ADC Boards, the ADC Control
Board has been divided into functional sections to facilitate
discussion of board operations. The operations performed
within each of these areas will be presented in the following
sections of this thesis. The three sections are the Pulse
Forming/Power Protection section, the Divider Network, and
the Frequency-Selection section. Figure 13 is provided as
a generalized block diagram of the operation of the ADC Con-
trol Board.

    2. Pulse Forming/Power Protection Section

        a. Introduction

            The Pulse Forming/Power Protection section performs
three functions: 1) conversion of the 20 MHz sinusoid into a
20 MHz pulse-train; 2) generation of all reference frequen-
cies for use in the divider network; and, 3) generation of
the SAMPLE-ENABLE signal. The schematics of this section
are presented in Figure 14.

        b. SAMPLE-ENABLE Signal

            As mentioned in Section III.A.3., the application
of an analog signal to the SHM-UH sample-and-hold module with
one or more power supplies not operating is a failure condi-
tion for this device. Accordingly, each of the three power
supplies required for SHM-UH operation is provided to the
input of a CLARE PRMA 1A05C to pull in the relay of that de-
vice. An internal protection diode in each reed relay requires

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                    ┌─────────────────────────┐
  20 MHz SINUSOID ─▶│   PULSE FORMING/POWER    │  SAMPLE ENABLE
                    │      PROTECTION          │
                    │       SECTION            │
                    │                          │  20 MHz CLOCK
                    └─────────────────────────┘

                    REFERENCE FREQUENCIES
                            ▼▼
                    ┌─────────────────────────┐
                    │                          │
                    │        DIVIDER           │
                    │        NETWORK           │
                    │                          │
                    └─────────────────────────┘

                     SAMPLE FREQUENCIES
                            ▼▼
                    ┌─────────────────────────┐
                    │    SAMPLE FREQUENCY      │
  SAMPLE FREQUENCY ─▶│     SELECTION           │◀
  SELECTION SIGNALS  │      SECTION            │
                    │                          │
                    └─────────────────────────┘
```

1. 20 MHz REFERENCE CLOCK
2. SAMPLE FREQUENCY CLOCK
3. HI/LOW SELECT
4. SAMPLE ENABLE
5. GROUND

TO ADC BOARD
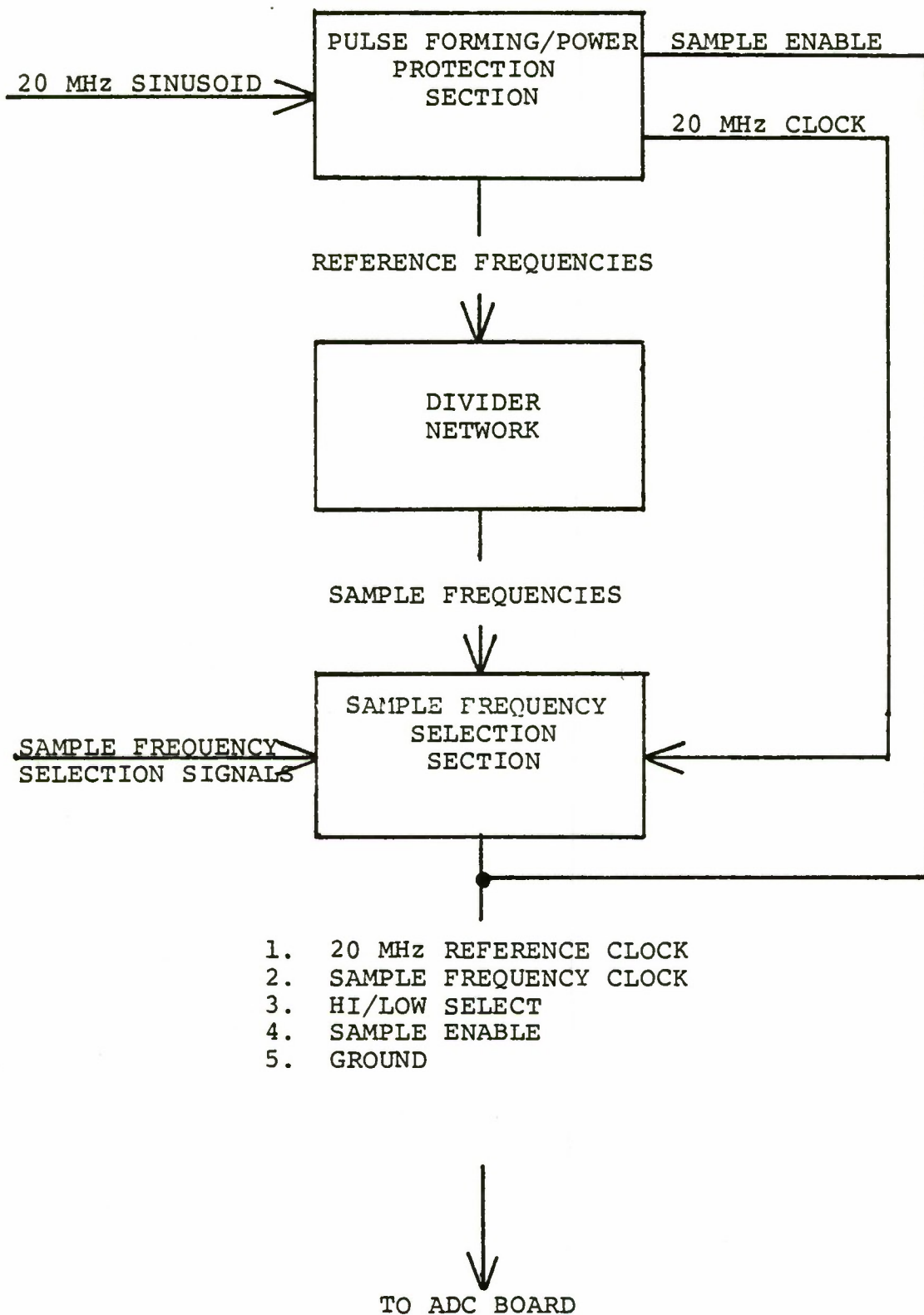
Figure 13
ADC CONTROL BOARD OPERATION
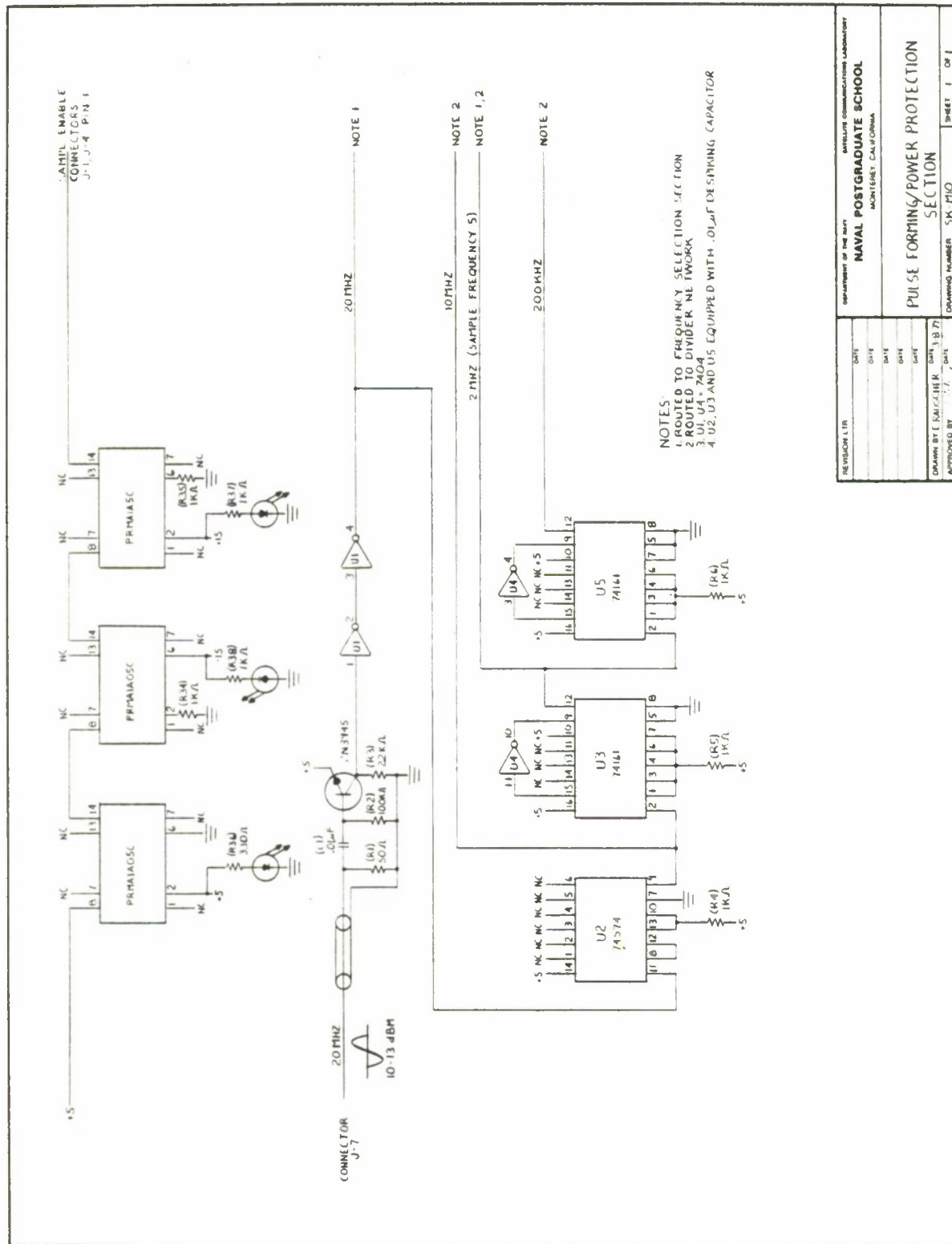
Figure 14

Pulse Forming/Power Protection Section Circuit Diagram

that the more positive signal be applied to pin 2 and that the ±15 volt inputs be routed through current limiting resistors (1 kilohm). A +5 volt signal is then passed in series through the three relays and is routed to the ADC Boards as the SAMPLE-ENABLE signal. Should one of the power supplied malfunction, the corresponding relay would open causing the SAMPLE-ENABLE signal to go "OFF" and open the relay which passes the analog signal to the SHM-UH. Three Light-Emitting-Diodes (LED's) are mounted at the upper edge of the ADC Control Board for quick visual reference to power supply status. The normal, power-on, condition is indicated by an illuminated LED.

c. Pulse Generation

The 20 MHz sinusoid from the frequency multiplication unit is converted to a 20 MHz pulse train by application to the base of a 2N3945 high power NPN transistor configured as shown in Figure 14. Double inversion of the collector output at U1 provides TTL compatible levels as well as a 50% duty cycle. The collector and base resistor values were determined to provide flexibility in the transistor types which could be employed in this circuit. Laboratory testing of three different transistors (2N3501, 2N3118, 2N3945) yielded satisfactory formation of the pulse train. The input sinusoid is designed to have a +13 dBm level; the circuit as designed works satisfactorily with sinusoidal input levels as low as +6 dBm, indicating that a 75% decrease in input level is tolerable. The 20 MHz pulse train is routed to the ADC Boards and X-Y Modulation Display where it serves as the reference clock for

the high-speed analog-to-digital converters.

    d.   Reference Signals

        The ADC Control Board is capable of producing one high-speed and four low-speed Sample-Frequency clock signals. The range of frequencies available provides a great deal of flexibility in resolution capability in the spectral analyses to be performed. Accordingly, this section of the board provides three reference signals (10 MHz, 2 MHz, 200 kHz) to the Divider Network where the low-speed sampling frequencies are generated (Note: 2 MHz is also the high-speed sampling frequency). As demonstrated in Figure 14, the 20 MHz pulse train is applied to U2, a D flip-flop designed to divide by two. This 10 MHz output signal is then routed to U3, a 74161 configured to divide by five. Finally, the resultant 2 MHz signal is divided by ten at U5, another 74161. These three reference frequencies are then routed to the Divider Network.

    3. Divider Network

    a. Introduction

        As previously mentioned, the Divider Network generates the low-speed sampling frequencies to be used in the spectral analyses by performing various divisions on the three reference frequencies. Figure 15 is a schematic of this section while Figure 16 provides a block diagram of the sample frequency generation process.

    b. Sample Frequency Generation

        Each of the reference frequencies generated in the Pulse Forming/Power Protection section is routed to a

Figure 15
Divider Network Circuit Diagram
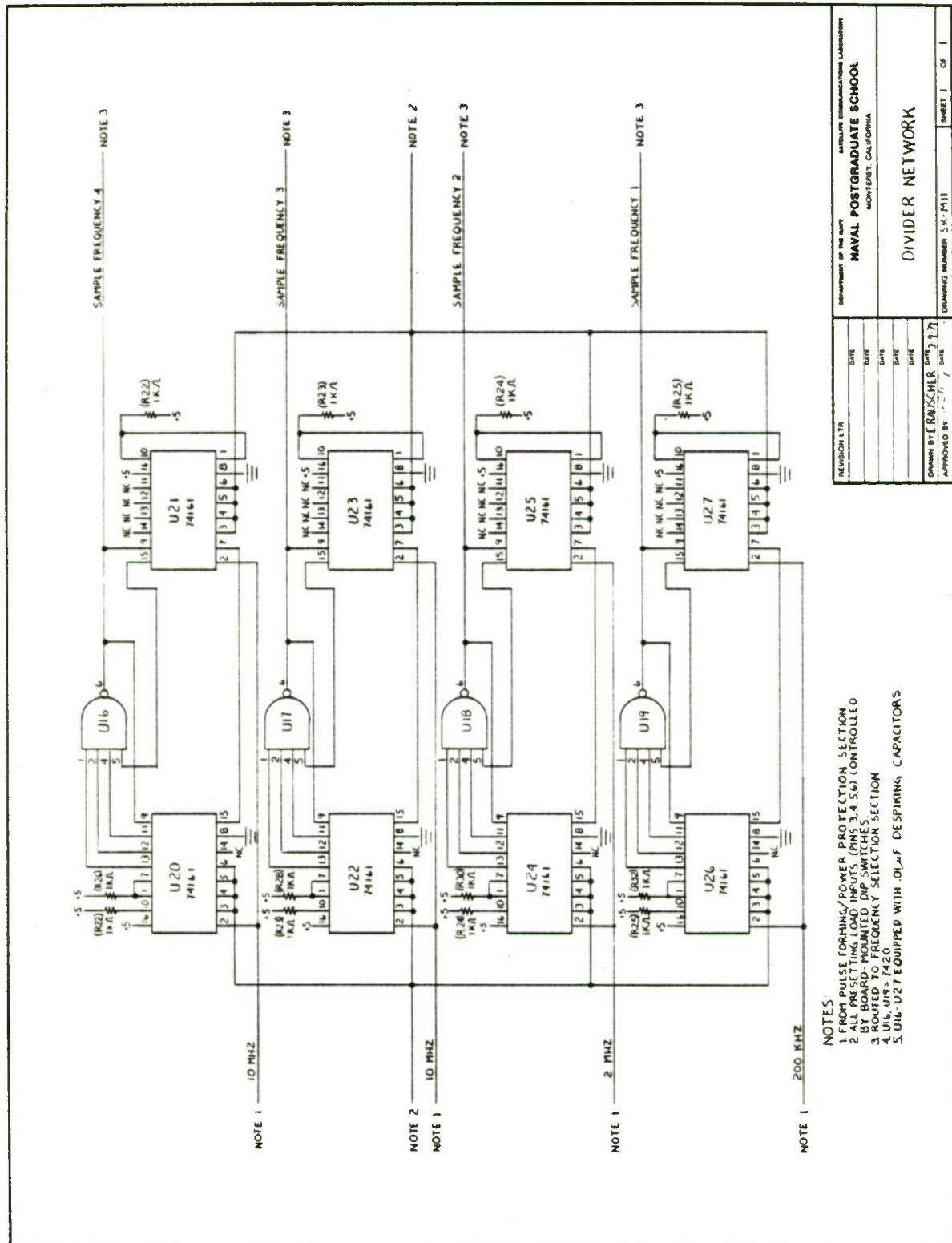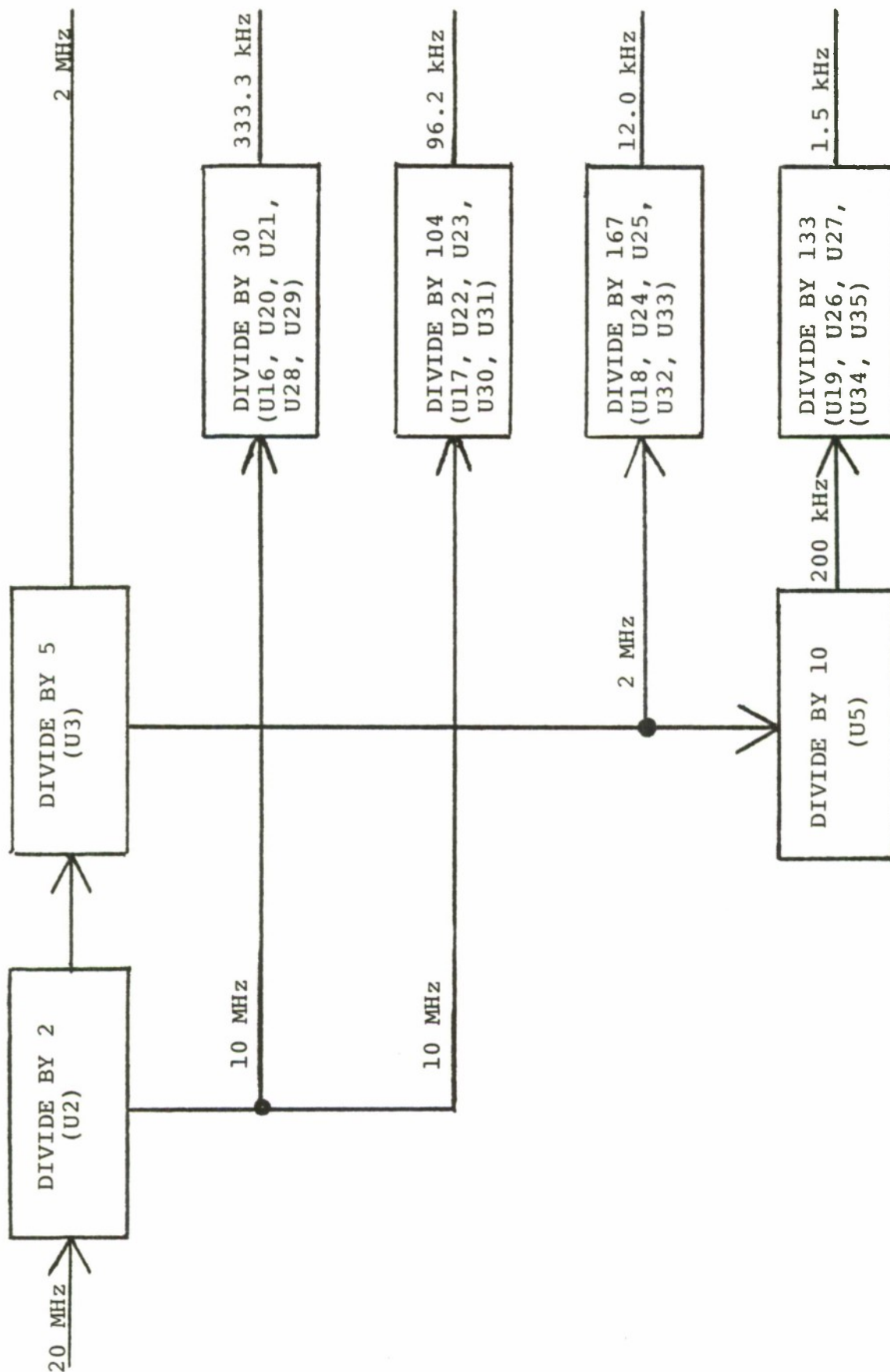
Figure 16
Sample Frequency Generation

variable modulo (up to 256) divider combination consisting of a 7420 dual input NAND gate, two 74161 divide-by-16 counters and two board-mounted, quad DPDT switches. This combination of components offers a great deal of flexibility in the selection of sampling frequencies (by making available all prime number in the 0-256 range) and simplifies the implementation of predetermined sampling frequencies. The 10 MHz reference frequencies may be converted into sampling frequencies in the 39.1 kHz to 10 MHz range through the application of such a combination. Similarly, the 2 MHz reference frequency could be converted into sampling frequencies in the 7.8 kHz to 2 MHz range; the 200 kHz reference input into sampling frequencies in the 781 to 200 kHz range. Control of the exact sampling frequency desired is accomplished by manipulation of the two quad switch packages which in turn control the preset load inputs to the divider I.C.'s. Implementation of a particular sampling frequency is accomplished by first determining which of the above ranges is appropriate to the desired frequency. The divider modulo number is then determined by division of the corresponding reference frequency by the desired sampling frequency (round-off may be required). The programming of the eight DPDT switches within each combination is determined by subtracting the modulo division number from 255 and converting the result to a base two representation. The eight switches in each combination represent ascending powers of the base two (2^0, 2^1 . . .), reading from left to right. The UP position on each switch places a logical "1" on that switch's

output while the DOWN position places a logical "0" on the output. Using this technique, the binary representation of the result of the (255-modulo division number) subtraction is placed on the eight switches and the desired frequency is generated at pin nine of the right most 74161 in the combination. As demonstrated in Figure 15, the tentative values of the five sampling frequencies are 1.5 kHz, 12.0 kHz, 96.2 kHz, 333.3 kHz and 2.0 MHz (all values rounded to nearest tenth) and are designated sample frequencies 1-5 respectively. Table III lists the switch settings utitlized to obtain the low speed sampling frequencies. The sample frequencies thus generated are routed to the Frequency Selection section.

    4.   Frequency-Selection Section

        a.   Introduction

        The Frequency-Selection section performs three functions: 1) selection of the desired sampling frequency for each ADC Board and the X-Y Modulation Display; 2) selective disabling of each ADC Board and X-Y Modulation Display; 3) generation of HIGH/LOW-SELECT signal. The schematic representation of this section is provided as Figure 17.

        b.   Sample-Frequency Selection

        The selection of the sample frequency for each ADC Board and the X-Y Modulation Display is accomplished through the use of five 74151 eight-to-one multiplexers (U-11 through U15). The five sampling frequencies generated in the Divider Network are applied to the multiplexer for each of the ADC Boards (U11 - U14) while the multiplexer for the X-Y

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TABLE III

SWITCH SETTINGS FOR TENTATIVE SAMPLING FREQUENCIES

FREQUENCY	LEFT SWITCH					RIGHT SWITCH				
	DESIGNATION	C1	C2	C3	C4	DESIGNATION	C1	C2	C3	C4
1.5 kHz	U34	0	1	0	1	U35	1	1	1	0
12.0 kHz	U32	0	0	0	1	U33	1	0	1	0
96.2 kHz	U30	1	1	1	0	U31	1	0	0	1
333.3 kHz	U28	1	0	0	0	U29	0	1	1	1

"0" = DOWN, "1" = UP
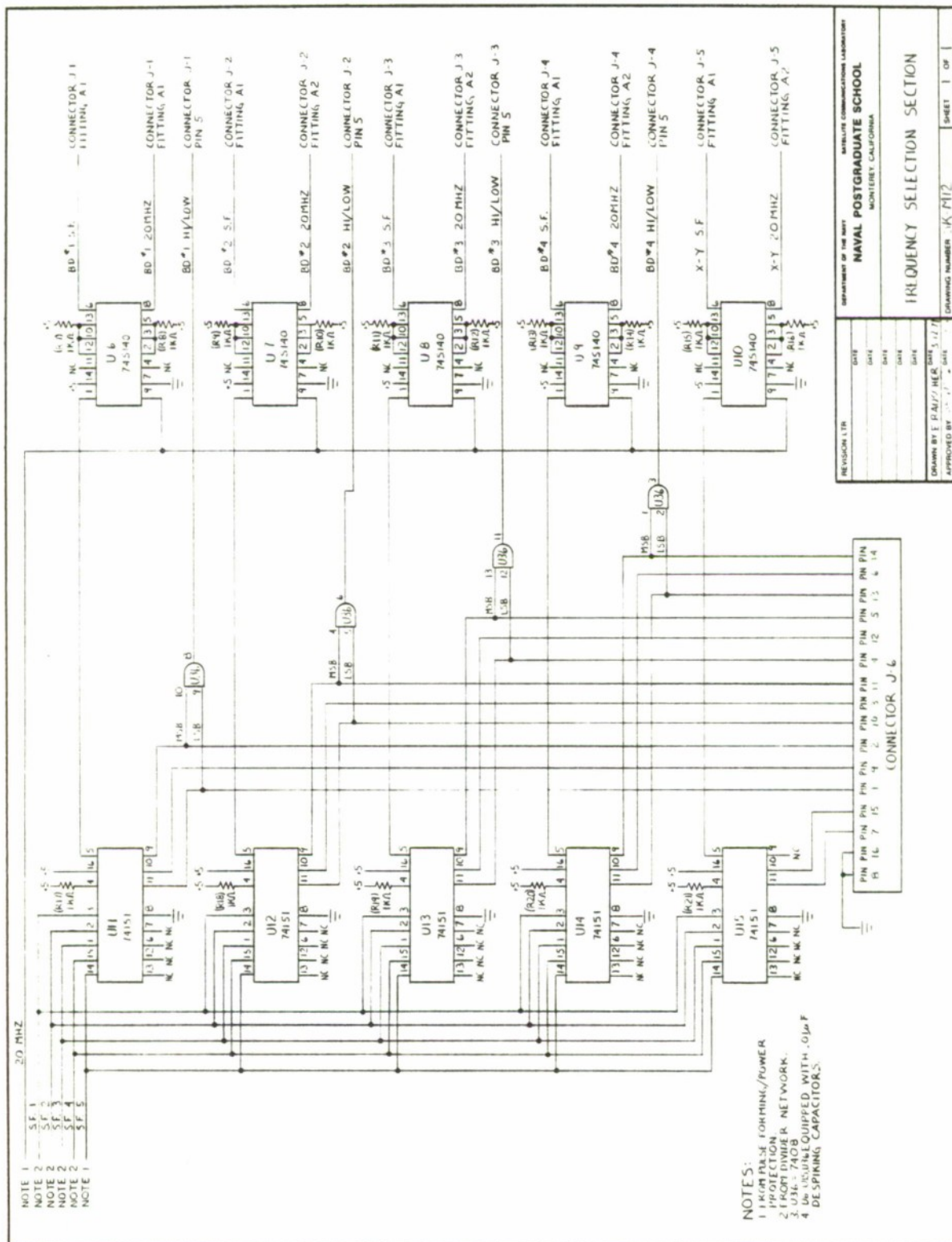
Figure 17
Frequency Selection Section Circuit Diagram

Modulation Display receives only Sample Frequencies 1-3. Design of this section includes the provision for the selective disabling of any of the ADC Boards and/or the X-Y Modulation Display. The disabling signal is a logical "0" placed on the Sample-Frequency coaxial cable to the board being disabled. This signal is obtained by the application of a logical "1" (+5 volts) to the D0 input of each multiplexer (pin 4), and is designated Sample Frequency 0. This value is inverted by the corresponding 74S140 dual 50 ohm line device thereby creating the disabling signal. Selection of the desired sampling frequency is controlled by the Sample-Frequency-Selection signals received from the Master Control Bus of the PDP-11/34. The multiplexer controlling the output frequency to each of the ADC Boards receives a three bit selection signal which allows for the selection of all six sample frequencies. Inasmuch as the multiplexer for the X-Y Modulation Display has only four possible sample frequency options, it receives a two bit selection signal. Table IV correlates the Sample-Frequency-Selection signals to the resultant output signals. As previously mentioned, each output sample frequency, as well as the 20 MHz reference clock, is applied to a 74S140 component to provide sufficient current sourcing for transmission via coaxial cable. All output signals to ADC Boards one through four exit the ADC Control Board via connectors J-1 through J-4, respectively. Connector J-5 is the interface for the two clock signals routed to the X-Y Modulation Display.

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TABLE IV

SAMPLE FREQUENCY SELECTION

Sample Frequency Select Signal (to each 74151)			Sample Frequency Number	Sample Frequency Value
Pin 9	Pin 10	Pin 11		
0	0	0	0	None, wired to +5 volts
0	0	1	1	1.5 kHz
0	1	0	2	12.0 kHz
0	1	1	3	96.0 kHz
1	0	0	4*	333.3 kHz
1	0	1	5*	2.0 MHz

* -- not available to multiplexer for X-Y Modulation
    Display (U15)

c. HI/LOW-SELECT Signal

The HI/LOW SELECT signal is used to control certain evolutions on the ADC Boards which are particular to the high-speed or low-speed modes of operation. In order to avoid confusion, the signal was designed to be at "high" level during high-speed operation (sample frequency 5 selected) and at a "low" level during low-speed operation (sample frequencies 0-4 selected). As demonstrated in Table IV, the Sample-Frequency-Select signal from the Master Control Bus is the binary representation of the decimal number of the sample frequency being selected. The HI/LOW-SELECT signal is generated by the logical AND-ing of the most significant and least significant bits of the Sample-Frequency-Select signal for each ADC Board. This signal is not provided to the X-Y Modulation Display analog-to-digital converter since that device will always operate in one of the low-speed modes.

D. ADC TEST BOX

1. Introduction

The ADC Test Box was designed to enable the SSA operators to monitor the operation of any one of the ADC Boards under limited test conditions, and may, therefore, serve as either a learning tool or a maintenance trouble shooting device. Operation of the ADC Test Box is premised on the proper functioning of the ADC Control Board which supplies the majority of the inputs to the device. The test box is inserted into a functioning system between the ADC Control Board and the ADC Board and, through proper switch

selection, may remain completely passive and thereby allow
(NORMAL) computer-controlled data exchange between the two
boards.   In the TEST modes, the ADC Test Box allows the
following options: 2) selection of the sampling frequency;
and, 2) selection of the mode of operation (low or high speed).
Figure 18 presents the schematics of the implementation of
these options.

2.   Inputs/Outputs

When the ADC Test Box is inserted between the ADC
Control Board and the ADC Board, it remains transparent to
the latter. This transparency is attributable to the signals
arriving at the ADC Board in the same form whether the ADC
Test Box is in the NORMAL mode or one of the TEST modes.
Accordingly, the inputs to, and outputs from, the ADC Test
Box are identical to the outputs of the ADC Control Board.
These signals include the following:

       a.   Sample-Frequency clock;

       b.   HI/LOW-SELECT signal;

       c.   SAMPLE-ENABLE signal; and,

       d.   20 MHz reference clock.

The inputs which are not included in the test options
(20 MHz reference clock and SAMPLE-ENABLE signal) are simply
routed through the ADC Test Box. The device receives +5 volts
from the ADC Board and shares a common GROUND with both boards.

3.   Implementation

The components comprising the ADC Test Box are socket
mounted on a 3 inch by 3 inch printed circuit board which was

Figure 18
ADC Test Box Circuit Diagram

designed and initially constructed at the NPS Etching Laboratory. This PC board is mounted within a BUD ALU-1083 aluminum utility cabinet. Inputs from the ADC Control Board arrive at the ADC Test Box via the same bunched cable assembly that would normally be routed to the appropriate ADC Board and are similarly terminated in a CANNON DAM-7W25A connector. Outputs exit the test device via a bunched cable assembly (no connector) which terminates in the CANNON DAM-7W25A connector on the ADC Board. The output cable assembly differs from the input assembly by the presence of an additional line on the former which carries the +5 volt supply to the ADC Test Box from the ADC Board. The switches controlling the NORMAL or TEST modes of operation are mounted on the top of the box with functional labeling located adjacent to each switch (see Figure 19).

    4. Operation

        a. HI/LOW Test Mode

The HI/LOW test mode allows the operator to interrupt the computer controlled signal on the HI/LOW-SELECT signal line and to manually control the high-speed or low-speed mode of operation on the ADC Board. The test mode is selected by positioning the HI/LOW toggle switch to the TEST-HIGH or TEST-LOW detents. In the TEST-HIGH position, a logical "1" is placed on the HI/LOW-SELECT signal line and the ADC Board is configured for high speed operation (testing). Selecting the TEST-LOW position configures the ADC Borad for low speed operation by placing a logical "0" on the HI/LOW-SELECT signal

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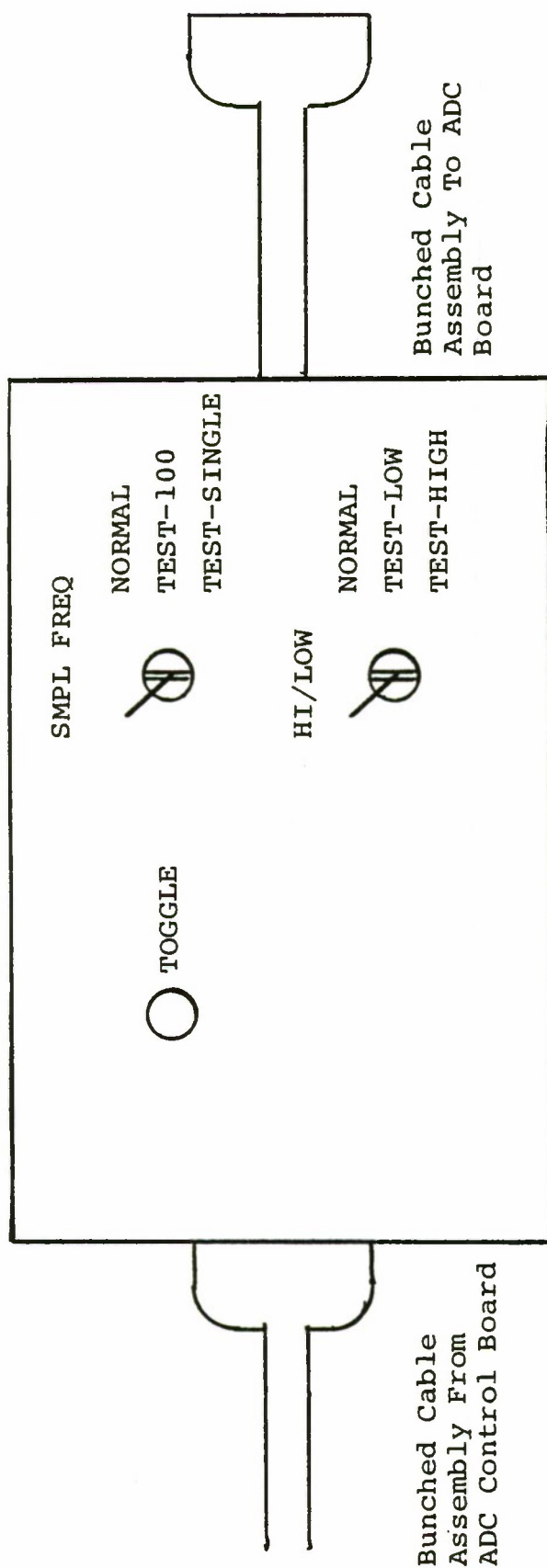
Figure 19
ADC Test Box (External View)

line to the ADC Control Board. The toggle switch employed is
an ALCO 205PA DPDT which has been configured to operate as a
SP3T switch as shown in Figure 20.

   b. SAMPLE FREQUENCY Test Mode

    The SAMPLE FREQUENCY test mode provides the op-
tions of obtaining a single sample or sampling at a 100 kHz
rate. The single sample mode of operation is selected by posi-
tioning the SMPL FREQ toggle switch to the TEST-SINGLE position
and depressing (and releasing) the TOGGLE momentary push but-
ton switch. Depression of the TOGGLE switch causes a logical
"0" to be applied to the input of a NAND gate contained in U1,
a 7400 quad NAND gate, resulting in a "1" to "0" transition.
This transition leads to the generation of appropriate pulses
on the ADC Board and results in a single conversion occurring.
Releasing the TOGGLE switch applies a logical "0" to another
NAND gate in U1 which causes a "0" to "1" transition and
thereby restores the SAMPLE FREQUENCY line to its original
condition. The interconnection of the two NAND gates into a
debouncing configuration ensures that each depression of the
TOGGLE switch results in a single transition (and conversion).
The TOGGLE pushbutton switch is an ALCO 205R DPDT momentary
switch which is configured as shown in Figure 19. The 100
kHz sampling rate is selected by positioning the SMPL FREQ
toggle switch to the TEST-100 position. The resultant 100
kHz sampling frequency is generated by U2, a 555 timer. The
timing resistors have values of 6.8 kilohms and 1.8 kilohms
while the charging capacitor has a rating of 1000 picofarads.

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```
              A            B            C
        ┌─────────────────────────────────┐
        │    1          2          3        │
        │    │          ─          │        │
        │                                   │
        │    │          ─          │        │
        │    4          5          6        │
        └─────────────────────────────────┘
```
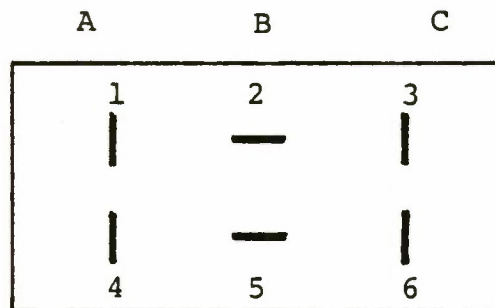
ALCO 205R and 205PA (Bottom View)

PIN NUMBER	SWITCH 1 (TOGGLE)	SWITCH 2 (SMPL FREQ)	SWITCH 3 (HI/LOW)
1	GROUND	pin 5	pin 5
2	U1, pin 1	OUTPUT	OUTPUT
3	NC	*Sample Fre-quency	*HI/LOW SELECT
4	NC	Single Pulse	+5 Volts
5	U1, pin 5	pin 1	pin 1
6	GROUND	100 kHz	GROUND

SWITCH POSITIONS	SWITCH 2 (SMPL FREQ)	SWITCH 3 (HI/LOW)
A	NORMAL	NORMAL
B	TEST-LOW	TEST-100
C	TEST-HIGH	TEST-SINGLE

* - From ADC Control Board

Figure 20
Switch Configurations

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The output of U2 is buffered by a HEX inverter contained in U3 to eliminate any ringing in the pulse train. Inasmuch as the Sample-Frequency clock signal is transmitted by coaxial cable, the output of the TOGGLE switch debouncer circuit and the 100 kHz pulse train are spplied to U4, a 74S140 dual 50 ohm line driver, prior to being applied to the SMPL FREQ toggle switch inputs. Positioning this toggle switch to the NORMAL position restores control of the Sample-Frequency clock signal to the ADC Control Board. The SMPL FREQ toggle switch is an ALCO 205PA DPDT switch which was converted to operate SP3T as demonstrated in Figure 20.

IV. FUTURE DESIGN MODIFICATIONS

The review of manufacturers' literature during the component selection stage revealed two components which could be successfully incorporated into the Analog-to-Digital Control and Conversion subsystem. Unfortunately, these items were under development by their respective manufacturers and would not be commercially available during the development period of the prototype SSA. One of these components is a DIP package sample-and-hold module which is being independently developed by TRW LSI Products and DATEL Systems, Inc. These units will be capable of speeds in excess of the 2 MHz required by this subsystem. The other component of interest is an analog-to-digital converter presently being designed by DATEL Systems, Inc., which incorporates the operating features of the ADC-EH12B3 but is mounted in a DIP package. The redesign of the ADC Board to incorporate these two components (when available) would result in significant savings in cost and printed circuit (PC) board space. At the time of this writing, the final sampling frequencies to be employed in the production versions of the SSA had not been determined. Accordingly, all sample frequencies mentioned in this thesis (with the exception of the 2 MHz high-speed rate) are estimates of the final fixed values. Once the determination of the sampling frequencies has been finalized, the ADC Control Board is subject to modification through the removal of the

board mounted switches which control the generation of the
sampling frequencies. The PC board modification to connect
the load inputs of the divider components directly to appro-
priate logical "1" or "0" values is a relatively minor change.
In addition to the obvious savings in board space, removal of
these switches provides protection against the use of incor-
rect sampling frequencies due to a switch being inadvertently
left in the wrong position. These proposed modifications are
easily implemented, represent no degradation in present sys-
tem capabilities, and would allow the associated components
to represent the technological state-of-the-art.

V. CONCLUSION

The Analog-to-Digital Control and Conversion subsystem
of the prototype SATCOM Signal Analyzer has been designed
and constructed. Inasmuch as the entire prototype system is
in various stages of construction, the ADC Control Board and
ADC Board(s) have not been exercised as components in an
operating system. However, both boards and the ADC Test Box
have been subjected to static and dynamic testing while
mounted in the PLESSEY PM-1150/5 power chassis. The ADC
Control Board and ADC Test Box have demonstrated the ability
to control the ADC Board(s) in the various modes of operation.
The ADC Board successfully carries out analog-to-digital
conversions in both the high-speed and low-speed modes.
Based on these results, the ADC Control and Conversion sub-
system is considered complete and operationally ready for
integration into the prototype SATCOM Signal Analyzer.

APPENDIX A

DUAL CHANNEL ANALOG TO DIGITAL CONVERSIONS THEORY

Dual channel analog-to-digital conversion is a technique
whereby an incoming IF signal is downconverted to two base-
band signals through mixing with two local oscillator sinu-
soids. The local oscillator signals have equal magnitude
and are phase related by 90 degrees. The mixing process
results in the two baseband signals having a quadrature
phase relationship. These signals are typically referred to
as the "In-phase" and "Quadrature-phase" components. When
these baseband signals are simultaneously sampled and analog-
to-digital converted, numerical estimates of the "In-phase"
and "Quadrature-phase" components are obtained. By allowing
the "In-phase" value to represent the real value and the
"Quadrature-phase" value to correspond to the imaginary val-
ue, a complex data point may be derived (see Figure 21).
Application of this complex data point to FFT processing re-
sults in an efficient use of the algorithm where all results
are meaningful. This is in contrast to the single channel
(real component) technique wherein the single (real) data
point, when processed by an FFT algorithm produces a symme-
tric output, half of which represents negative frequencies
and is therefore redundant. The dual channel conversion
method preserves all information within the bandpass of the
IF signal (and therefore the RF signal); the zero frequency
component in the resultant spectrum corresponds to the com-
ponent of the RF signal which is at the same frequency as the
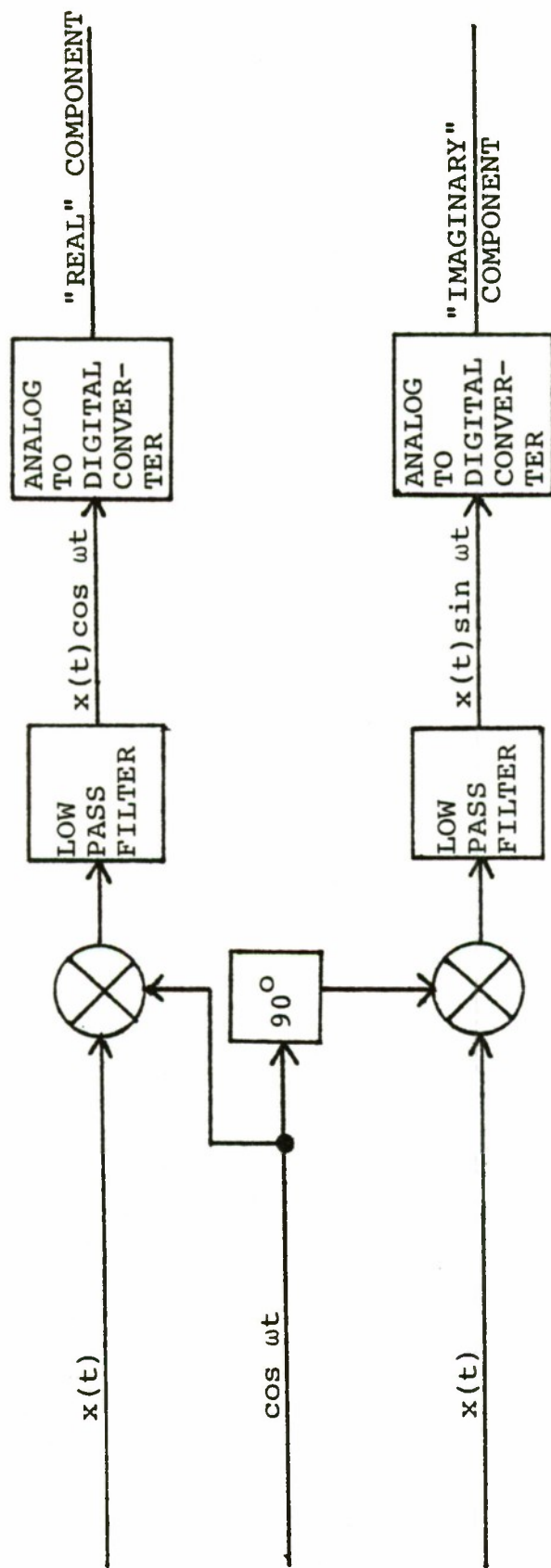
Figure 21
Dual Channel Analog-to-Digital Conversion

local oscillator, as demonstrated in the following develop-
ment:

IF Signal : $x(t)$

Local oscillator signal : $\cos \omega_L t$

"In-phase" component : $x(t) \cos \omega_L t$

"Quadrature-phase" component : $x(t) \sin \omega_L t$

Complex baseband signal: $y(t)$

$y(t)$ = "In-phase" component + j "Quadrature-phase" component

$$= \left[x(t) \cos \omega_L t + jx(t) \sin \omega_L t \right]$$

$$= x(t) \left[\cos \omega_L t + j \sin \omega_L t \right]$$

$$= s(t) \, e^{j \omega_L t}$$

Taking the Fourier Transform of $y(t)$ results in :

$$F\left[y(t) \right] = F \left[x(t) \, e^{j \omega_L t} \right]$$

$$= F_x (\omega - \omega_L)$$

APPENDIX B

This Appendix includes the major operating speicifcations of the DATEL SHM-UH sample-and-hold module, and the DATEL ADC-EH12B3 and TRW TDC-1001J analog-to-digital converters. It consists of Tables V through VII.

TABLE V

DATEL SHM-UH SPECIFICATIONS

Case size	2" W x 2" L x .375" H
Number of pins	11
Power supplies	15 volts, $\pm$ 15 volts
Analog input range	$\pm$ 5 volts
Input overvoltage	$\pm$ 10 volts
Input impedance	100 Megohms
Gain	+ 1
Sample command	35 nanoseconds ($\pm$ 10 nanoseconds) positive pulse
Settled output	50 nanoseconds
Output voltage range	$\pm$ 5 volts
Maximum sampling rate	10 MHz

TABLE VI

DATEL ADC-EH12B3 SPECIFICATIONS

Case size   4" L x 2" W x .4" H

Number of pins   26

Power supplies   + 5 volts, ± 15 volts

Input voltage range   ± 5 volts

Input overvoltage   ± 20 volts

Input impedance   1.15 kilohms

Start convert   100 nanosecond (minimum) posi-
                                 tive pulse

Outputs   12 parallel bits in two's com-
                                 plement or offset binary
                                 (both positive true)

Settled output   2 microseconds (maximum)

Maximum conversion rate   500 kHz

TABLE VII

TRW TDC-1001J SPECIFICATIONS

Case size	.3" W x .9" L x .4" H (DIP style)
Number of pins	18
Power supplies	$\pm$ 5 volts
Reference input	- 0.5 volts
Input voltage range	- 0.5 volts to 0.0 volts
Input overvoltage	- 5 volts to +1 volt
Input impedance	25 kilohms
Reference clock	Pulse train at nine times the sampling rate with width of 20 nanoseconds (both minima)
Start convert	50 nanosecond positive pulse (minimum)
Output	Eight parallel bits in inverted offset binary format
Settled output	Tenth reference pulse after conversion began
Maximum conversion rate	2.5 MHz

APPENDIX C

In order to optimize the accuracy of the digital outputs
from the ADC Board, each of the analog-to-digital converters
and the sample-and-hold module must be calibrated. In each
case the static calibration of these devices is accomplished
by adjusting either an internal or external resistance trim-
pot. The calibration process requires the ADC Board to be
mounted on standard PDP-11 extender boards with the bunched
cable assembly from the ADC Control Board connected as in
normal operations. Sample Frequency 2 (12.5 kHz) should be
selected during the calibration process.

DATEL SHM-UH Sample-and-Hold Module

The DATEL SHM-UH contains an internal trimpot which is
used to adjust the ZERO OFFSET of the device. Access to
this trimpot is via an opening on the lower side of the case
(as mounted on the ADC Board) between pins two and three.
The analog input to the ADC Board must be terminated in a
suitable load (50 ohm) to ensure a zero potential at the ana-
log inputs to the SHM-UH. Connect a precision DC digital
volt-meter to the analog outputs (pin 4 = High, pin 3 = Low)
and adjust the trimpot to obtain a reading of 0.0 volts on
the voltmeter.

DATEL ADC-EH12B3 Analog-to-Digital Converter

The DATEL ADC-EH12B3 has two adjustments (GAIN ADJUST and
OFFSET ADJUST) which are performed through the use of two

external trimpots (TR3, TR4). The OFFSET ADJUST calibration requires a precision DC voltage of -4.9988 volts to be applied to the analog input of the device. This is accomplished by the application of a precision DC voltage of -9.9976 volts to the analog input of the ADC Board. The serial version of the ADC-EH12B3 output may be observed on an oscilloscope by connecting a probe to pin 4 (located at the top right corner of the mounted board). The EOC signal (pin 1) may be used for oscilloscope display synchronization. Adjust the 200 ohm trimpot (TR4) to obtain a pulse train which flickers between 0000 0000 0000 and 0000 0000 0001. The GAIN ADJUST calibration requires that a precision voltage of +4.9854 volts be applied to the analog input of the device (+9.9708 volts to the analog input of the board). Observe the serial output of the device, as in the OFFSET ADJUST procedure, and adjust the 20 ohm trimpot (TR3) to obtain a pulse train which flickers between 1111 1111 1110 and 1111 1111 1111.

TRW TDC-1001J Analog-to-Digital Converter

The analog input voltage to the TRW TDC-1001J requires RANGE and OFFSET adjustment to be made to the output of the sample-and-hold module. This calibration requires the analog input to the ADC Board to be terminated in a zero potential (50 ohm) load. The RANGE adjustment is made by a twenty-to-one voltage (R13-R15) division of the analog output of the SHM-UH, which converts the ± 5 volt range into a ± .25 volt range. The OFFSET adjustment centers this reduced range at a center value of -.25 volts, obtained by a twenty-to-one

division of the -5 volt regulator output across a fixed 1
kilohm resistor (R13) and a 50 kilohm trimpot (TR1). Con-
nect a probe to Test Point 1 (located approximately in the
center of the board) and adjust the trimpot until a reading
of -.25 volts is obtained. The -.5 volt reference voltage
required by the TDC-1001J (pin 13) is similarly obtained by
a ten-to-one voltage division of the -5 volt signal across
a fixed 1 kilohm resistor (R16) and another 50 kilohm trim-
pot. A probe is connected to Test Point 2 (adjacent to Test
Point 1) and the trimpot is adjusted to obtain a reading of
-.5 volts at that point.

APPENDIX D

This appendix contains a listing of all pin and slot connections for the ADC Control Board and a typical ADC Board. The locations of the various connectors and slots may be determined from the component layout drawings (figures 4 and 12). Proper mounting of all ribbon connector mating connectors is facilitated by the etching of the number "1" on each board adjacent to the proper location of pin 1 of the corresponding connectors. The PDP-11 backplane slots contain 18 pin connections which are lettered, from right to left, ABCDEFHJKLMNPRSTUV. The components on each board are mounted on side number 1; the reverse side is number 2. This appendix consists of Tables VIII and IX.

TABLE VIII

ADC CONTROL BOARD PIN CONNECTIONS (Page 1 of 6)

Connector J-1 (Cannon DAM-7W25A)

Connection	Function	To ADC Board 1, Connector J-1, Connection
Pin 1	NC	
Pin 2	NC	
Pin 3	SAMPLE ENABLE	Pin 3
Pin 4	GROUND	Pin 4
Pin 5	HI/LOW SELECT	Pin 5
Fitting A1	Sample Frequency Clock	Fitting A1
Fitting A2	20 MHz Reference Clock	Fitting A2

Connector J-2 (Cannon DAM-7W25A)

Connection	Function	To ADC Board 2, Connector J-1, Connection
Pin 1	NC	
Pin 2	NC	
Pin 3	SAMPLE ENABLE	Pin 3
Pin 4	GROUND	Pin 4

TABLE VIII

ADC CONTROL BOARD PIN CONNECTIONS (Page 2 of 6)

Connection	Function	To ADC Board 2, Connector J-1, Connection
Pin 5	HI/LOW SELECT	Pin 5
Fitting A1	Sample Frequency Clock	Fitting A1
Fitting A2	20 MHz Reference Clock	Fitting A2

Connector J-3 (Cannon DAM-7W25A)

Connection	Function	To ADC Board 3, Connector J-1, Connection
Pin 1	NC	
Pin 2	NC	
Pin 3	SAMPLE ENABLE	Pin 3
Pin 4	GROUND	Pin 4
Pin 5	HI/LOW SELECT	Pin 5
Fitting A1	Sample Frequency Clock	Fitting A1
Fitting A2	20 MHz Reference Clock	Fitting A2

Connector J-4 (Cannon DAM-7W25A)

Connection	Function	To ADC Board 4, Connector J-1, Connection
Pin 1	NC	

TABLE VIII

ADC CONTROL BOARD PIN CONNECTIONS (Page 3 of 6)

Connection	Function	To ADC Board 4, Connector J-1, Connection
Pin 2	NC	
Pin 3	SAMPLE ENABLE	Pin 3
Pin 4	GROUND	Pin 4
Pin 5	HI/LOW SELECT	Pin 5
Fitting A1	Sample Frequency Clock	Fitting A1
Fitting A2	20 MHz Reference Clock	Fitting A2

Connector J-5 (Cannon DAM-3W3S)

Fitting	Function	To X-Y Modulation Display
A1	Sample Frequency Clock	Connection undetermined
A2	NC	
A3	20 MHz Clock	Connection undetermined

Connector J-6 (Ansley 609-615M)

Pin	Function	To Master Control Bus
1	GROUND	Connection undetermined
2	GROUND	Connection undetermined

TABLE VIII

ADC CONTROL BOARD PIN CONNECTIONS (Page 4 of 6)

Pin	Function	To Master Control Bus
3	X-Y Modulation Display Sample Frequency Select (LSB)	Connection undetermined
4	X-Y Modulation Display Sample Frequency Select (MSB)	Connection undetermined
5	ADC Board 4, Sample Frequency Select (center bit)	Connection undetermined
6	ADC Board 4, Sample Frequency Select (MSB)	Connection undetermined
7	ADC Board 3, Sample Frequency Select (MSB)	Connection undetermined
8	ADC Board 4, Sample Frequency Select (LSB)	Connection undetermined
9	ADC Board 3, Sample Frequency Select (LSB)	Connection undetermined
10	ADC Board 3, Sample Frequency Select (center bit)	Connection undetermined

TABLE VIII

ADC CONTROL BOARD PIN CONNECTIONS (Page 5 of 6)

Pin	Function	To Master Control Bus
11	ADC Board 2, Sample Frequency Select (center bit)	Connection undetermined
12	ADC Board 2, Sample Frequency Select (MSB)	Connection undetermined
13	ADC Board 1, Sample Frequency Select (MSB)	Connection undetermined
14	ADC Board 2, Sample Frequency Select (LSB)	Connection undetermined
15	ADC Board 1, Sample Frequency Select (LSB)	Connection undetermined
16	ADC Board 1, Sample Frequency Select (center bit)	Connection undetermined

Slot C

Pin(s)	Function	Pin(s)	Function
A1	NC		

TABLE VIII

ADC CONTROL BOARD PIN CONNECTIONS (Page 6 of 6)

Pin(s)	Function	Pin(s)	Function
A2	+5 volts	T1	GROUND
B1	NC	T2	NC
B2	-15 volts	U1	+15 volts
All C through S	NC	U2	NC

Slots D, E, F

Pin(s)	Function	Pin(s)	Function
A1	NC	All C through S	NC
A2	+5 volts	T1	GROUND
B1	NC	T2	NC
B2	-15 volts	U through V	NC

TABLE IX

ADC BOARD PIN CONNECTIONS (Page 1 of 4)

Connector J-1 (Cannon DAM-7W25A)

Connection	Function	To
Pin 1	NC	
Pin 2	+5 Volts	ADC Test Box (When connected)
Pin 3	SAMPLE ENABLE	ADC Control Board, Connector J-1, Pin 3
Pin 4	GROUND	ADC Control Board, Connector J-1, Pin 4
Pin 5	HI/LOW SELECT	ADC Control Board, Connector J-1, Pin 5
Fitting A1	Sample Frequency Clock	ADC Control Board, Connector J-1, Fitting A1
Fitting A2	20 MHz Reference Clock	ADC Control Board, Connector J-1, Fitting A2

Connector J-2 (Ansley 609-3425M)

Pin	Function	To AP-400 AUX PORT Pin
1	IF TRS/INPUT	1
2	NC	
3	NC	
4	NC	
5	NC	

TABLE IX

ADC BOARD PIN CONNECTIONS (Page 2 of 4)

Pin	Function	To AP-400 AUX PORT Pin
6	NC	
7	NC	
8	NC	
9	LOW SPD (OR HI SPD-WD2) BIT 2	5
10	LOW SPD (OR HI SPD-WD2) MSB	22
11	LOW SPD (OR HI SPD-WD2) BIT 4	6
12	LOW SPD (OR HI SPD-WD2) BIT 3	23
13	LOW SPD (OR HI SPD-WD2) BIT 6	7
14	LOW SPD (OR HI SPD-WD2) BIT 5	24
15	LOW SPD (OR HI SPD-WD2) BIT 8	8
16	LOW SPD (OR HI SPD-WD2) BIT 7	25
17	LOW SPD BIT 10	9

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TABLE IX

ADC BOARD PIN CONNECTIONS (Page 3 of 4)

Pin	Function	To AP-400 AUX PORT Pin
18	LOW SPD BIT 9	26
19	LOW SPD BIT 12	10
20	LOW SPD BIT 11	27
21	NC	
22	NC	
23	NC	
24	NC	
25	HIGH SPD WD1 BIT 2	13
26	HIGH SPD WD1 MSB	30
27	HIGH SPD WD1 BIT 4	14
28	HIGH SPD WD1 BIT 3	31
29	HIGH SPD WD1 BIT 6	15
30	HIGH SPD WD1 BIT 5	32
31	HIGH SPD WD1 BIT 8	16
32	HIGH SPD WD1 BIT 7	33
33	GROUND	17
34	GROUND	34

TABLE IX

ADC BOARD PIN CONNECTIONS (Page 4 of 4)

Slot C

Pin(s)	Function	Pin(s)	Function
A1	NC	T1	GROUND
A2	+5 Volts	T2	NC
B1	NC	U1	+15 Volts
B2	-15 Volts	U2, V1, V2	NC
All C through S	NC		

Slots D, E, F

Pin(s)	Function	Pin(s)	Function
A1	NC	All C through S	NC
A2	+5 Volts	T1	GROUND
B1	NC	T2	NC
B2	-15 Volts	U through V	NC

APPENDIX E

This appendix contains a complete listing of all components mounted on the ADC and ADC Control Boards. Exact locations of components (integrated circuits, connectors, conversion modules, etc.) may be determined by reference to component layout diagrams (Figures 4 and 12). Resistors and capacitors are generally located in close proximity to the components with which they appear in the board section schematics. This appendix consists of Tables X, XI, and XII.

TABLE X

ADC CONTROL BOARD COMPONENT LIST (Page 1 of 1)

Component(s)	Description
U1, U4, U36	7404 (Hex Inverter)
U2	74S74 (Dual D Flip Flops)
U3, U5, U20-U27	74161 (Presettable Divide-By-16 Counter)
U6 - U10	74S140 (Dual 50 Ohm Line Drivers)
U11 - U15	74151 (One-of-Eight Multiplexer)
U16 - U19	7420 (Dual Four Input NAND Gates)
U28 - U35	76COA (Quad DIP Mounted SPDT Switches)
U37 - U38	PRMA1A05C Reed Relays
R1	50 Ohm Resistor (1/4W, 10%0
R2	100 Ohm Resistor (1/4@, 10%)
R3	2.2 kilohm Resistor (1/4W, 10%)
R4 - R35, R37, R38	1.0 kilohm Resistors (1/4W, 10%)
R36	330 ohm Resistor (1/4W, 10%)
C1 - C29, C32, C33	.01 microfarad (50V) Ceramic Capacitors (DIP Style)
C30, C31	10 microfarad (50V) Electrolytic Capacitors
2N3945	High Power NPN Transistor
J-1 - J-4	Cannon DAM 7W25A Connectors
J-5	Cannon DAM 3W3S Connector
J-6	Ansley 609-615M Mating Connector
J-7	SMA Bulkhead Fitting
LED's (3)	Unidirectional
H.H. Smith 6298 (2)	Board Extractors

TABLE XI

ADC BOARD COMPONENT LIST (Page 1 of 2)

Component(s)	Description
DATEL SHM-UH	Sample-and-Hold Module
DATEL ADC-EH12B3	Low-Speed ADC Module
TRW TDC-1001J	High-Speed ADC Module
U1, U2, U19, U21	74121 (One Shot Multivibrator)
U3	74S140 (Dual 50 Ohm Line Driver)
U4, U20, U22	7404 (Hex Inverters)
U5	7432 (Quad Two Input OR Gates)
U6	LM318 Operational Amplifier
U7	PRMA1A05C Reed Relay
U8 - U14	74175 (Quad D Latches)
U15 - U17	74157 (Quad One-of-Two Multiplexer)
U18	74107 (Dual J-K Flip Flops)
V1	LM320T-5 (-5 V Regulator)
V2	LM340-5 (+5 V Regulator)
TR1, TR2	70Y503 (50 Kilohm Trimpots)
TR3	89PR20 (20 Ohm Trimpot)
TR4	89PR200 (200 Ohm Trimpot)
R1 - R6, R13, R14, R16	1 kilohm Resistors (1/4W, 10%)
R7 - R10	10 kilohm Resistors (1/4W, 10%)
R11, R12	1.0 kilohm Resistors (1/4W, 5%)
R15	18 kilohm Resistor (1/4W, 10%)
R17, R22	2.7 kilohm Resistor (1/4W, 10%)
R18	100 ohm Resistor (1/2W, 10%)
R19	3.3 kilohm Resistor (1/4W, 10%)
R20, R21	50 ohm Resistors (1/4W, 10%)
C1 - C18, C22, C24, C26, C30, C32, C33, C37-43	.01 microfarad Ceramic Capacitors (DIP Style)
C19	25 microfarad (1KV) Ceramic Capacitor
C20, C21	82 microfarad (1KV) Ceramic Capacitor

TABLE XI

ADC BOARD COMPONENT LIST (Page 1 of 2)

C23	.2 microfarad (16V) Ceramic Capacitor
C25	2.2 microfarad (35V) Tantalum Capacitor
C27	.22 microfarad (35V) Tantalum Capacitor
C28	5 microfarad (1KV) Ceramic Capacitor
C29	68 picofarad (1KV) Ceramic Capacitor
C31, C34-C36	10 microfarad (50V) Electrolytic Capacitors
J-1	CANNON DAM-TW25A Connector
J-2	ANSLEY 609-3415M Mating Connector
J-3	SMA Bulkhead Fitting
H.H. Smith 6298(2)	Board Extractors

TABLE XII

ADC TEST BOX COMPONENT LIST

Component(s)	Description
U1	7400 (Quad NAND Gates)
U2	555 (Timer)
U3	7404 (HEX Inverters)
U4	74S140 (Dual 50 Ohm Line Driver)
R1, R2	22 kilohm Resistors (1/4W, 10%)
R3	6.8 kilohm Resistor (1/4W, 10%)
R4	1.8 kilohm Resistor (1/4W, 10%)
R5, R6	1.0 kilohm Resistor (1/4W, 10%)
C1 - C4	.01 microfarad Ceramic Capacitor (DIP Style)
C5	.001 microfarad (1KV) Ceramic Capacitor
J-1	CANNON DAM-7W25A Connector
SW1	ALCO 205R DPDT (Momentary) Switch
SW2, SW3	ALCO 205PA DPDT Switch

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