Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
2008		**00-00-2008 to 00-00-2008**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Dynamics of Forward Voltage Drift in 4H-SiC PiN Diodes	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Naval Research Laboratory,4555 Overlook Avenue SW,Washington,DC,20375**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**Same as Report (SAR)**	**3**	

Dynamics of Forward Voltage Drift in 4H-SiC PiN Diodes

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Background: 4H-silicon carbide (SiC) is desired for electronic devices designed to be operated at high temperatures or at high electric powers. However, difficulties in the growth of high-purity, low defect density substrates and epitaxial layers have limited the use of SiC in commercial and military applications. One such impediment is the nucleation and expansion of Shockley stacking faults (SSFs) during forward-bias device operation (stressing), which induces an undesirable increase in the forward voltage drop (V_f). While efforts have been made to reduce the number of SSFs within a given device, these defects continue to provide a significant technological hurdle to the commercialization of 4H-SiC electronic devices, most especially for larger-area power devices that require close to defect-free active regions.

Electrical Degradation: The expansion of SSFs in SiC induces a drift in V_f. In other words, during forward-bias operation, the voltage required to turn the device on (reach a threshold current) increases continuously. Therefore, the turn-on voltage is a moving target and renders the device useless. This degradation in the forward-bias characteristics is illustrated in Fig. 6(a), where current-voltage (IV) curves collected from a PiN diode are presented. The initial IV curve is shown in blue. A current density of 14 A/cm^2 was then injected into the diode for twelve consecutive 5-min intervals, with each interval leading to a progressive flattening of slope of the IV curves (V_f drift increase). The final curve, collected after 60 total minutes of stressing is presented in red. This degradation is due to SSFs, which are localized, planar changes in the crystal stacking order from hexagonal (4H-SiC) to cubic (3C-SiC). Since cubic SiC has a significantly reduced bandgap, this causes the SSFs to act as tilted, planar electron traps. A schematic of a PiN diode is presented in Fig. 6(b) to illustrate the orientation of the SSFs.

SSF Expansion: Presented in Fig. 7(a) is an electroluminescence (EL) image collected from a 4H-SiC PiN diode prior to device stressing. In SiC, EL images are collected by driving a constant current (here, 1.4 A/cm^2) through the device for given time (here, 5 or 10 sec). In SiC, when current carriers (electrons and holes) recombine at defects such as SSFs, they give off excess energy in the form of light, which can be imaged using a CCD camera. In this image the partial dislocations that bound the SSFs can be seen as red lines. Since the SSFs are tilted 8° from the horizontal (see Fig. 6(b)), top-view EL images of the epilayer illustrate the position of these defects at a given time. As shown in Fig. 7(b), upon electrical stressing (1.75 min at 25 A/cm^2), the SSFs expand significantly, with the red partial dislocations now larger and clearly highlighting the periphery of the violet, triangular-shaped SSFs. The bright blue, vertical EL line indicates that one of the SSFs has terminated at the p-n junction. In Fig. 7(c), we see that following 8 min at 25 A/cm^2, almost all of the faults that were expanding to the left have also terminated there.

SSF Contraction: Until recently, it was believed that SSFs were the energetically favorable state; therefore, if enough energy were provided, the 4H-SiC would be readily converted into 3C-SiC SSFs. Here at NRL, it was discovered that thermal annealing of heavily faulted (degraded) PiN diodes for extended periods at temperatures between 210° and 700 °C led to the complete contraction of all SSFs. This is illustrated in Fig. 7(d), where the diode was annealed at 700 °C for 4 hrs. Annealing also induced a complete and repeatable recovery of the V_f drift, as presented in Fig. 6(c), where IV curves collected following several subsequent annealing cycles at 505 °C are displayed. These observations clearly illustrate that SSFs are not the thermodynamically favorable state.

Temperature Effects on V_f Drift: Further experimentation at NRL determined that continued device stressing led to a maximum V_f drift; however, temperature increases (or decreases in stressing current) reduced SSF expansion and therefore reduced this V_f drift maximum, as illustrated in Fig. 8(a). It was also determined that the annealing process is accelerated if an electrical current is injected during the process (current-induced recovery), which is illustrated in Fig. 8(b). In this case, the device was initially stressed at room temperature (blue circles) until the V_f drift maximum was attained. Following this, the device was heated to 242 °C (red squares) and the same current was applied, which led to the V_f drift partially recovering, eventually reaching a new, reduced maximum V_f drift. The temperature was then returned to room temperature and the process repeated; however, when the temperature was raised this second time, the current was reduced 100× (red, open squares), leading to an even larger V_f drift recovery.

Summary: These results illustrate that SSF expansion and its deleterious effects can be controlled to some degree, thereby providing hope that functional SiC bipolar devices may be possible, even if some small, yet manageable, SSF density is present, especially at

elevated operating temperatures. It also demonstrates that degraded devices may be repeatedly recovered. It should also be noted that very recently, NRL has developed a new epitaxial growth technique that has been observed to reduce the density of the SSF nucleation sites by up to 98%.

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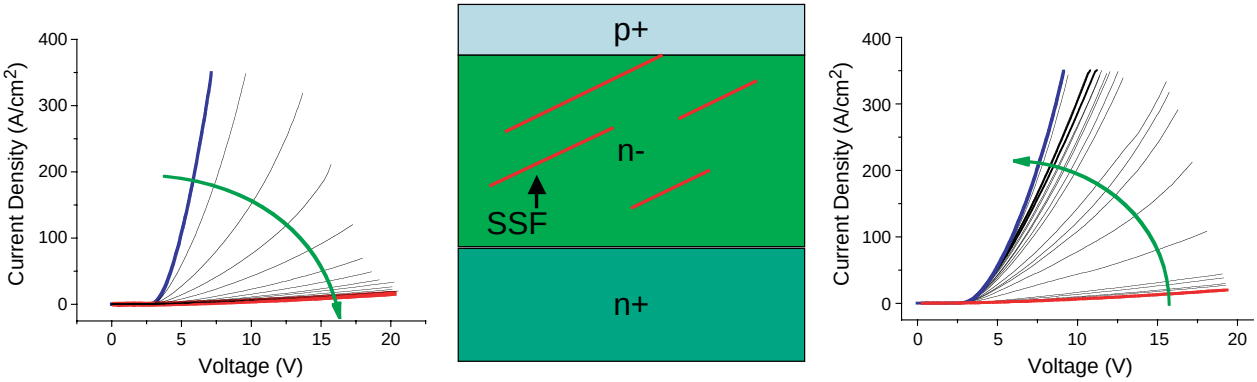

FIGURE 6
(a) Current-voltage (IV) traces collected prior to device stressing (blue curve), and following twelve consecutive 5-min periods of 14 A/cm^2 device stressing. (b) Pictorial representation of the cross-sectional view of a SiC PiN diode. The red lines represent the SSFs that are tilted 8° from the horizontal. (c) IV curves collected following subsequent periods of annealing at 505 °C. In both (a) and (c), the red and blue curves denote the IV data from the diode in the heavily faulted and the unfaulted states, respectively.

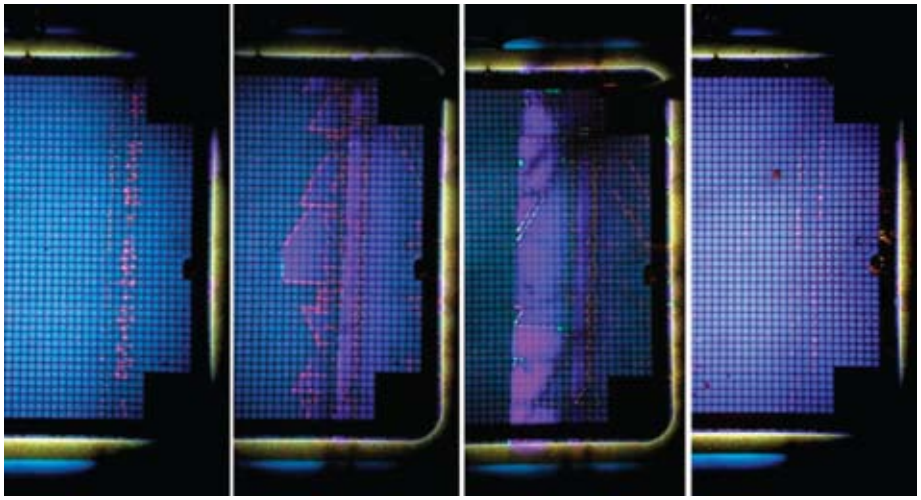

FIGURE 7
Electroluminescence (EL) images collected (a) prior to device stressing, (b) following 1.75 min of stressing and (c) 8 min of stressing at 25 A/cm^2, and (d) following a 4-hour, 700 °C anneal. The black regions are where the metal contact is present.

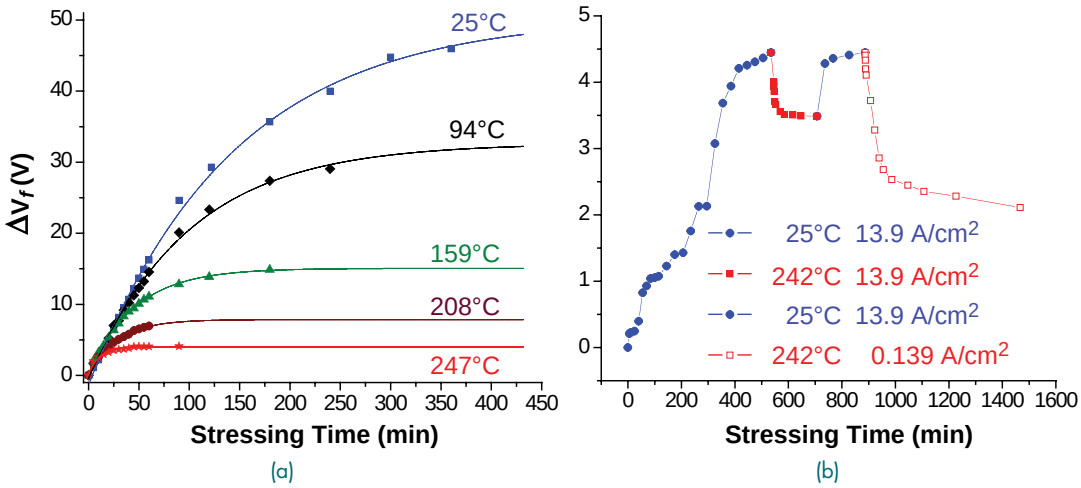

FIGURE 8
(a) Plot of the change in the V_f as a function of the stressing time within the same diode at various stressing temperatures. The device was fully annealed before each series of experiments at a given temperature. (b) Similar to (a), but the stressing temperature and current were changed at different points during the experiment (see legend) to illustrate current-induced recovery of the V_f drift. While the stressing was completed at various temperatures, the IV data points were collected at 25 °C.