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Threshold Voltage Tuning of Metal-Gate MOSFET Using an Excimer Laser

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EXECUTIVE SUMMARY

This report presents a localized method for tuning the threshold voltages (V_t) of multilayer metal-gate metal-oxide-semiconductor field-effect transistor (MOSFET) devices with a spatial area theoretically limited by the wavelength of the laser beam. This technique allows an independent means to tailor threshold voltage on a device-to-device basis that provides greater design flexibility. This maskless technique allows tailoring of thresholds by tuning the work function of the gate by intermixing titanium and titanium nitride using a laser pulse. The source and drains of the MOSFET are simultaneously annealed by the laser.

1. INTRODUCTION

With the increasing use of portable and wireless electronic systems, reduction in power/energy consumption has become one of the most important design concerns. Power dissipation not only affects performance and battery life, but also has a large impact on packaging, reliability, and heat removal costs.

Leakage power minimization has prompted various integrated circuit manufacturers to employ multiple-V_t processes [1]. Many process technologies provide dual-V_t transistors. This technique uses high-V_t for transistors in the non-critical paths to reduce the static power (minimizing overall leakage power) while low-V_t transistors are used in the performance-critical paths to meet performance requirements. Thus, an adjustable threshold voltage is highly advantageous not only for process control, but multiple-V_t applications as well.

There are several factors that control V_t. Gate oxide thickness, work function of the gate, and channel doping are the main independent factors. Ion implantation and subsequent furnace annealing is used to control the channel doping, which has a direct effect on the Fermi potential and the depletion charge. An increase in the channel doping increases V_t.

Gate oxide thickness controls V_t directly. As gate oxide thickness increases, the gate oxide capacitance is reduced and V_t will increase. However, the thickness of the oxide is determined by the technology node, and while multiple gate oxides are sometimes used, they are usually chosen to interface with outside power supplies. Three gate oxides on the same technology is usually all that is practical to manufacture due to the complexity of growing different thickness gate oxides on the same wafer.

The third factor is the gate work function. This method for V_t control may very well be the best approach because the choice of a lower resistance gate material directly results in a higher unity power gain, fmax, which is an important figure of merit for radio-frequency devices. Metals are attractive for replacing polysilicon (poly-Si) as the gate material due to their very low resistance properties. Therefore, it would be desirable to find a metal with a work function in the range of 4.4 to 5.0 eV, which is compatible with current silicon processing technology. However, current MOSFET technology uses a poly-Si gate that can withstand high-temperature furnace anneals.

A metal-gate MOSFET is desirable both for lowered resistance and the reduction of poly-Si depletion effects that leads to better short-channel effects. Metals with a suitable work function, such as aluminum (Al), were considered as a gate material, but could not be used due the high thermal processing temperatures exceeding the melting point of these metals. More recently, higher melting point metals such as tungsten (W) and tantalum (Ta) were proposed as alternative gate materials [2, 3].

As device threshold voltages are reduced, faster switching and higher current drive is achieved at the expense of decreased noise margin, increased leakage current, and increased power. Recent applications of multiple V_t technology have been demonstrated in IBM's G6 Microprocessor [4], where the low V_t threshold is approximately 90 mV lower than that of the nominal-V_t device. Their strategy was to add low-V_t devices, where acceptable, to all critical paths until the critical path was fully low-V_t. At this point, the processor has gained the maximum advantage (10% improvement) from low-V_t and adding more would unnecessarily increase power and noise. An example of dual-V_t or variable-V_t for leakage current reduction in memory circuits was reported by Margala for Static Random Access Memory (SRAM) applications [5]. Low-voltage complementary metal oxide semiconductor (CMOS) circuits have shown as much as 80% power leakage savings using dual-V_t technology [6].

The process for tuning the threshold voltage occurs after the metal-gate stack is formed via physical vapor deposition (PVD) and the source and drain of the MOSFET have undergone ion implantation. At this point, the device is irradiated with a series of laser pulses to anneal the source and drain regions while the majority of the laser energy impinging on the gate region is reflected off the metal gate. The substrate is preferably silicon-on-insulator (SOI) to facilitate higher temperatures near the gate interface in comparison to bulk Si.

2. EXPERIMENT

A self-aligned process is used to fabricate metal-gate MOSFET devices on a single SOI wafer formed by Separation-by-Ion-Implantation-of-OXide (SIMOX). The multilayer metal-gate of the self-aligned MOSFET was formed by PVD of 10-nm titanium (Ti), followed by 50 nm of titanium nitride (TiN) and 200-nm Al on top of a 7.5-nm gate oxide formed by dry oxidation.

After source and drain implantation, the devices were irradiated with a 308-nm XeCl excimer laser at a fluence (energy density) of 415 mJ/cm^2. Each laser pulse normally occurs on a time scale of 10 to 30 ns and activates the source and drain dopants, as well as initiating thermal mixing. The TiN layer intermixes with the bottom Ti layer as a result of N diffusion at 800°C temperatures. This intermixing causes the work function of Ti (4.33 eV) to shift towards the work function of TiN (4.55 eV), directly increasing the threshold voltage. The laser-induced thermal activation of channel dopants also contributes to the V_t increase as a smaller second-order effect for a larger number of laser pulses.

3. RESULTS AND DISCUSSION

Figure 1 shows the experimental results of the threshold voltage as a function of the number of laser pulses for a metal-gate device. The threshold voltage was obtained using the traditional linear extrapolation method at the point of maximum slope. A typical error of ±0.01 eV is assigned to each data point to account for discrepancies in the fabrication process. The threshold voltage exhibits a linear shift of 70 mV from 0.32 to 0.39 V over 20 laser pulses, which is controlled by the laser fluence and the number of pulses. A poly-Si gate transistor was fabricated for comparison. In this situation, the majority of the laser irradiation of the poly-Si gate is absorbed in the gate.

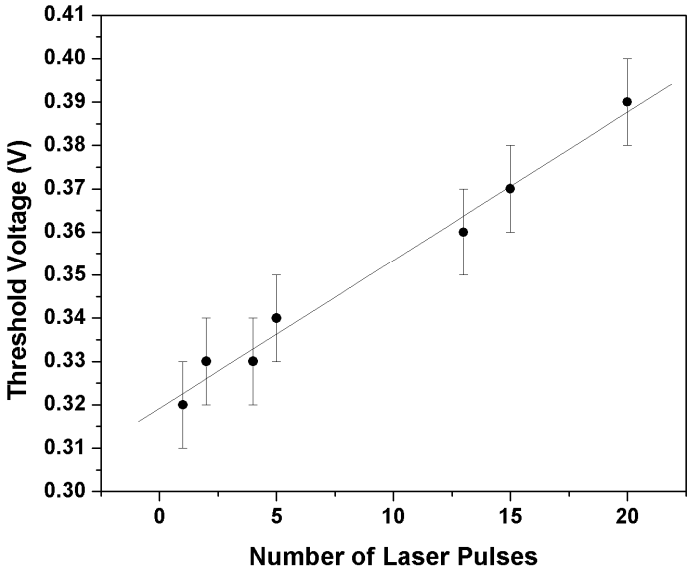

Figure 1. Experimental results of the threshold voltage as a function of the number of laser pulses for a metal-gate device.

Figure 2 shows the experimental results of the threshold voltage as a function of the number of laser pulses for the poly-Si gate device. A typical error of ±0.01 eV is assigned to each data point to account for discrepancies in the fabrication process. As compared to Figure 1, the threshold voltage remains relatively constant over a series of 20 laser pulses, thereby confirming the ability to control V_t using the inventive process of a metal-stack and laser annealing.

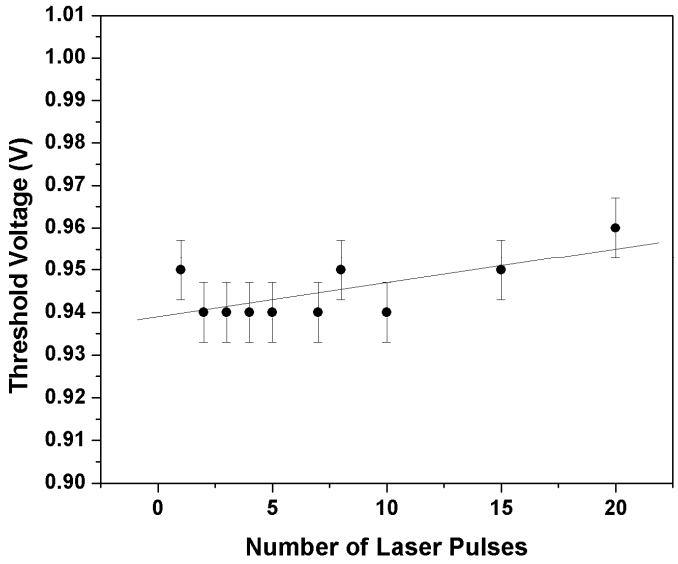

Figure 2. Experimental results of the threshold voltage as a function of the number of laser pulses for the poly-Si gate device.

4. CONCLUSION

A new method of tuning the threshold voltage of a MOSFET has been demonstrated with a Ti/TiN metal-gate MOSFET using a pulsed excimer laser [7]. The results show that the threshold voltage can change by up to 70 mV. These results could not be duplicated in an identical poly-Si gate MOSFET, which indicates that a model describing the intermixing of the metal multilayers causing a metal work function shift can be used to explain the shift in the threshold voltage as a function of the number of laser pulses.

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This report presents a localized method for tuning the threshold voltages (V_t) of multilayer metal-gate MOSFET devices with a spatial area theoretically limited by the wavelength of the laser beam. This technique allows an independent means to tailor threshold voltage on a device-to-device basis that provides greater design flexibility. This maskless technique allows tailoring of thresholds by tuning the work function of the gate by intermixing titanium and titanium nitride using a laser pulse. The source and drains of the MOSFET are simultaneously annealed by the laser.

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