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Time-Reversal Based Range Extension Technique for Ultra-wideband (UWB) Sensors and Applications in Tactical Communications and Networking

Technical Report (Quarterly)

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14. ABSTRACT

This final report summarizes major project activities and results achieved during last three years. This project has involved a great amount of theoretical and development work. The primary goal is to demonstrate an SNR gain without using multiple antennas, so that transmission range can be increased. This goal has been reached by using UWB time reversal on our real-time testbed. Propelled by the project, our overall research has harvested in a number of aspects. The first UWB time reversal system with real-time waveform precoding at the transmitter was demonstrated in our lab in year 2009. The original time reversal technique has been generalized by transmitting an optimization based waveform, considering implementation limitations. Tremendous experience in real-time system design and implementation has been gained throughout the development cycle.

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Executive Summary

This final report summarizes major project activities and results achieved during last three years. This project has involved a great amount of theoretical and development work. The primary goal is to demonstrate an SNR gain without using multiple antennas, so that transmission range can be increased. This goal has been reached by using UWB time reversal on our real-time testbed. Propelled by the project, our overall research has harvested in a number of aspects. The first UWB time reversal system with real-time waveform precoding at the transmitter was demonstrated in our lab in year 2009. The original time reversal technique has been generalized by transmitting an optimization based waveform, considering implementation limitations. Tremendous experience in real-time system design and implementation has been gained throughout the development cycle. This report is organized as follows. An overall project review and system description are provided in chapter 1 and 2. Major achievements and findings, including development and theoretical work, are given in chapter 3 and 4. In chapter 5 and 6, some current and future work influenced by this project are described, followed by an appendix to include a few most recent test results.

Contents

Part I

Brief Project Review and System Description

Chapter 1

Project Review

The major goal of this projeet is to develop a true UWB radio with time reversal precoding at the transmitter. Progress has been made gradually over last three years. Listed in Table 1.1 are milestones achieved. The first UWB time reversal system with real-time waveform precoding at the transmitter was demonstrated in our lab in year 2009. About 4-dB SNR gain was achieved in an indoor multiroom environment. An arbitrary waveform generator with 14-bit resolution and 500-MHz bandwidth has been built using commercial ADC and FPGA board. A unique 3-stage burst mode synchronization scheme has been implemented in FPGA. In addition to our development work, this project has also driven theoretical research efforts. Among many byproducts harvested from the project is the radio testbed. Now it is playing an important role in exploring multichannel front-ends and testing algorithms in real time. This project is benefiting and will continue to benefit our research work.

Table 1.1: Milestones Achieved

Stable Architecture	3rd quarter 2007
Arbitrary Waveform Generating	1st quarter 2008
Time Reversal System (baseline)	2nd quarter 2008
Full-Function Time Reversal	1st quarter 2009
Performance Test and Trials	3rd quarter 2009
System Improvement & Function Extension	4th quarter 2009

Chapter 2

Testbed System Description

A general purpose Time-Reversal UWB transceiver testbed for communication and ranging was developed. The main goal is to implement a pair of transmitter and receiver to verify our Time-Reversal conceptual-proof schemes. The design is based on energy (square law) detection reception technology. On April 14, 2008,we demonstrated the very first time reversal UWB radio in our lab. On April 2009, we improved the system, from demonstration it has been found that time reversal precoding can provide 3 to 4 dB gain over an ordinary single-carrier UWB system in indoor multipath environments with non-line-of-sight (NLOS). The major parameters of the testbed under test are as follows.

- 10-dB Bandwidth: 400 to 800 MHz
- Chip rate: 25 Mc/s
- Bit rate: 6.25, 3.125, 1.5625 Mb/s
- Synchronization method specially designed for burst mode transmission
- Digital modulation: on/off keying (OOK)
- Receiver sensitivity: -81 dBm
- Waveform Generator with 8-bit quantization and 1-GHz sampling
- I/Q quadrature frequency up-conversion
- Energy detector with different integration window sizes

- Adjustable and adaptive thresholds in synchronization and demodulation phases

This testbed design has a few advantages:

- Passband I/Q frequency up-conversion flexible for spectrum arrangement
- The received waveform envelope is optimized by adjusting a baseband complex FIR filter at the transmitter
- Virtually arbitrary waveform generating, taking full advantage of channel information.
- OOK modulation with simple energy detector receiver robust to timing error
- Analog-to-digital converter (ADC) and digital processing at the receiver able to test various algorithms
- The selected spectrum is very clean and the channels are very stable, so that system tests and trials are convenient.

Pulse based signaling and transmitter-side processing are adopted as system design guideline. Although direct pulse (carrierless) transmission can largely reduce complexity of transmitter RF front-end, it is not a good choice for multi-purpose radio testbed mainly because of its inflexibility. As a matter of fact, a modulated pulse is not only easy to generate but also more flexible: the center frequency is determined by a local oscillator and the spectral shape is governed by the baseband pulse. Conceptual testbed architecture is shown in Fig. 2.1. Following an FIR filter (embedded in the FPGA), the digital-to-analog converter (DAC) outputs desired analog waveforms. The simple-receiver philosophy is reflected in this testbed with OOK modulation and diode based non-coherent detector at the receiver. At the receiver, demodulation is done in digital domain, so that algorithms and parameters can be adjusted easily. Of course, the analog-to-digital converter (ADC) is power hungry and it may be replaced by some substitute circuits in commercialized products in the future.

Noticeable temporal focusing has been seen and successful data transmission has been experimentally demonstrated in this some how harsh environment. Double transmission distance involves a lot of challenging jobs including transplanting the receiver back-end from the Virtex-2 platform to the Virtex-5 platform, increase of the prefilter length, and solving the dynamic range problem, etc. At current stage, the receiver back-end is powered by Virtex-5 platform and we have modified the system to double transmission distance.

2.1 Transmitter

At the testbed's transmitter side, there are mainly five parts: Xilinx Virtex-5 LXT Prototype Platform, Fujitsu DK86064 DAC Evaluation Kit, TRF3703-15 Quadrature Modulator Evaluation Module, PSA4000A Local Oscillator Evaluation Board and Mini-Circuits ZVE-8G Amplifier. Transmitter Architecture is shown as Fig. 2.2. Baseband

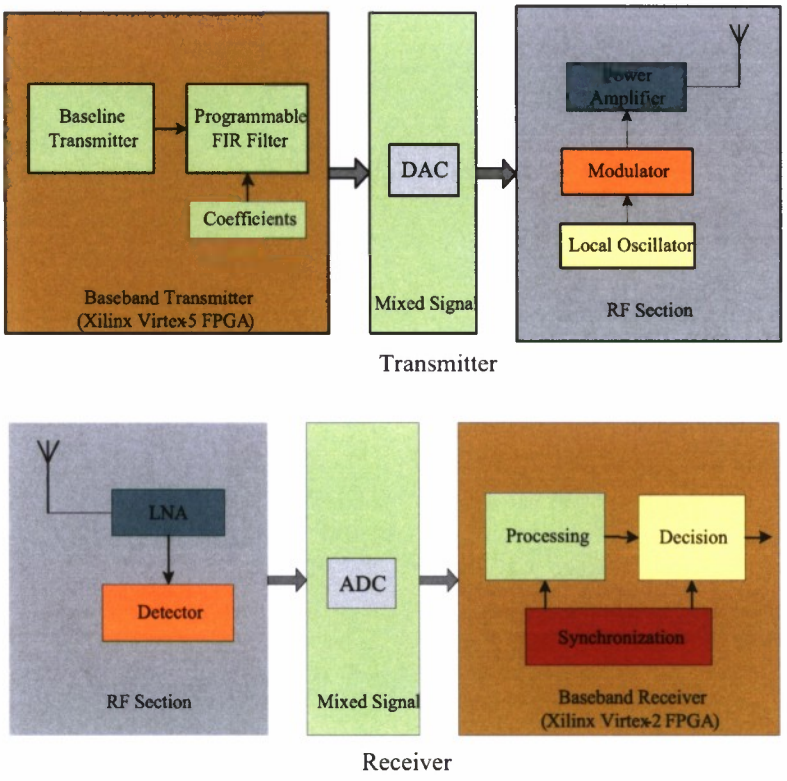


Figure 2.1: Overall testbed architecture.

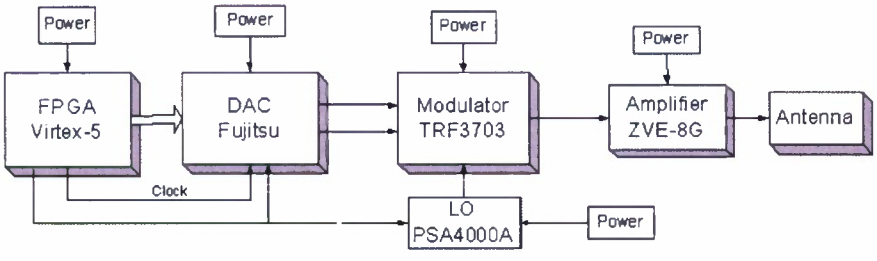


Figure 2.2: The architecture of testbed transmitter

Table 2.1: A List of Selected Components/Modules for Transmitter

FPGA back-end	Virtex-5 LXT	Xinlix	65 nm/1.0 V core/550 MHz/17,280 slices/680 User I/O
DAC	MB86064	Fujitsu	Dual 14-bit 1 GSa/s
Local oscillator	PSA4000A	Z-communications	Center frequency 4.0 GHz
Modulator (up-converter)	TRF3703-15	Texas Instruments	Direct quadrature modulator 400 MHz to 4 GHz
Amplifier	ZVE-8G	Mini-circuits	Wideband(2 to 8 GHz)/ low noise(4 dB typ)/35dB gain

signals from DAC are converted to passband signal by modulator and then be sent to the amplifier, the output signal of amplifier goes to the antenna and then be transmitted through the air. major components and modules for transmitter side are listed in Table 2.1.

Discrete-time waveform is generated by the waveform generator module in FPGA based on chip value, scrambling code and the pre-loaded waveform template,the discrete-time waveform is then fed to the DAC via the high-speed connection buses. The waveform generator will be described in detail in chapter 3.

Local Oscillator PSA4000A is used to generated 4.0GHz frequency for modulator, it is configured by FPGA board through an SPI port. whenever the FPGA board is powered on, the Local Oscillator is configured automatically to work at 4.0 GHz. As the RF picture shows, there is a DB9 cable which connect the Local Oscillator and FPGA. Quadrature modulator TRF3703-15 is used to convert complex modulated signals from baseband directly up to RF.

2.2 Receiver

The receiver design is based on energy (square law) detection reception technology, the architecture is shown as Fig. 2.3 and the actual picture is as shown as Fig. 2.4. The MAX108, an 8 bits,1.5 GHz flash ADC, is employed to convert the analog signal into digital signal in the baseband. the digital back-end is powered by newly transplanting Virtex-5 LXT development board.

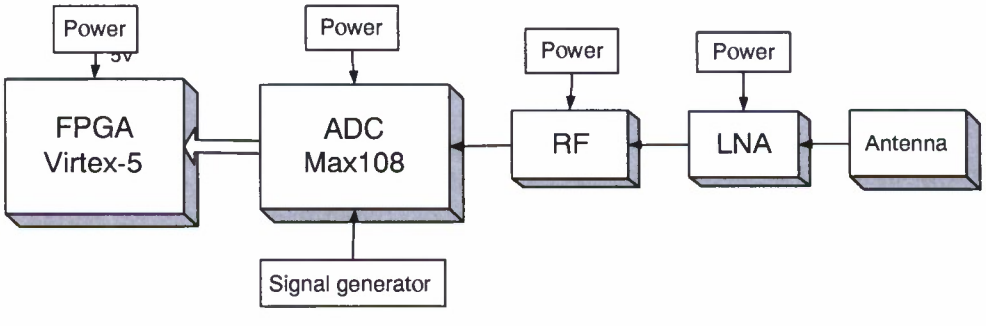


Figure 2.3: The architecture of the testbed receiver

All algorithms and signal processing tasks are described in Verilog codes and implemented in Xilinx Virtex family FPGA. Module-based coding style is adopted to expedite the overall development [1]. For our current testbed, an advanced Xilinx Virtex-5 FPGA board supporting high speed connection has replaced the old Virtex-5 board at transmitter side, and the receiver becomes much more powerful after replacing the Virtex-2 pro FPGA board by a Virtex-5 FPGA board. Among various features provided by Xilinx Virtex-5 FPGA family, its high speed capability for signals, clocks and I/O, as well as embedded IP cores, are extremely important to implementation of wide

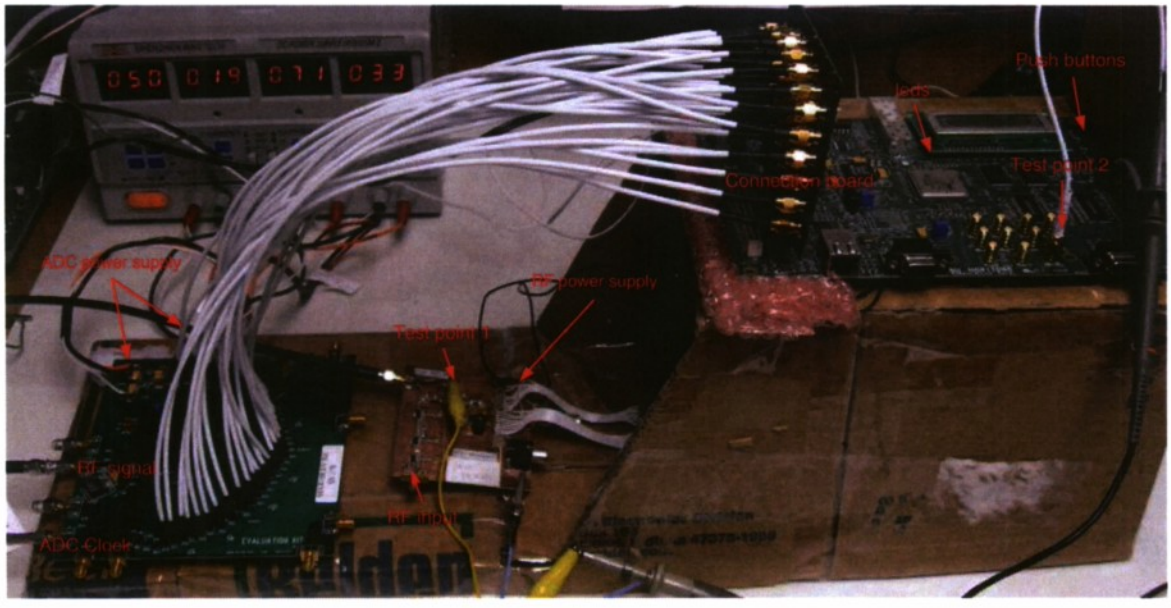


Figure 2.4: The picture of the testbed receiver

bandwidth systems.

Table 2.2 shows the FPGA resource usage on Xilinx Vitex-5 LXT FPGAs. Note that the FPGA chips used at the transmitter and the receiver are of the same model, but the transmitter FPGA chip has 1136 I/O ports while the receiver FPGA chip only has 665 I/O ports.

Table 2.2: FPGA Implementation Statistics at Transmitter and Receiver

Resources	Transmitter Amount used	Transmitter Percent used	Receiver Amount used	Receiver Percent used
Number of Slice Registers	5314	18%	4184	14%
Number of Slice LUTs	5019	13%	3088	10%
Number of occupied Slices	1719	24%	1713	23%
Number of bonded IOBs	40	8%	90	25%
Number of BlockRAM/FIFO	2	3%	1	1%
Number of BUFG/BUFGCTRLs	7	21%	10	31%
Number of DSP48Es	NA	NA	32	66%
Total equivalent gate count	275,214	NA	195438	NA

Part II

Achievements and Findings

Chapter 3

Development Aspects

3.1 UWB Time Reversal: From Theory to Practice

3.1.1 Background

Stimulated by the FCC's move that allows UWB waveforms to overlay over other systems', UWB radio has received significant attention recently [2–13]. Mainly due to potentially low implementation complexity, suboptimal reception strategies, such as transmitted reference (TR) [4] [8] , autocorrelation demodulation (ACD) [7] [9] [14] and energy detection [10, 15] , have gotten increasing attention for complexity and cost constraint UWB applications. However, these systems suffer performance loss in rich multipath environments. The UWB channel impulse response (CIR) contains a large number of resolvable components coming through different paths, especially in indoor environments. Our emphasis has been on making good use of these signal components.

A signal focusing technique called time reversal that can turn multipath into benefit and shift part of receiver complexity burden to the transmitter side [15,16]. Time Reversal (TiR) is a technology originated from underwater acoustic and ultrasound communications [16], and it has been extended to wireless applications recently [12, 13, 17, 18]. Given specific time and location, TiR precoding has been mathematically proved to be the optimum in the sense that it maximizes the amplitude of the field at that time and location [17]. It is then called spatio-temporal matched filter [19] because it is analogous to a matched filter both in time and space. It is also called transmit matched filter since the matched filter is placed at the transmitter side. The key element in a time reversal system is a transmitter-side filter that pre-filters the signal, leading to a condensed equivalent CIR. Two characteristics of time reversal are temporal focusing and spatial focusing. Temporal focusing can soften the impact of ISI. Time reversal combined with antenna array results in spatial focusing that can focus energy at a desired location, enabling a number of unique functions. A straight-forward thought is "spatial-division" multiple access. We can also take advantage of this spatial discrimination ability to reduce leakage of signal sent to an intended user, or prevent the signal from being detected or intercepted at other locations, which is equivalent to encryption using the CIR, resulting in additional location-based security enhancement from physical layer [18, 20].

While promising, applying UWB time reversal at present is extremely challenging. The main difficulties come from implementing the pre-filter in the case of such high bandwidth. It is desired for the pre-filter to accurately represent the time-reversed waveform. However, high-fidelity signal representation needs high sampling rate and

high resolution in magnitude, implying a prohibitively expensive solution. In this work a digital FIR filter followed by an interpolator is considered as the pre-filter. We found that the requirements for the FIR filter's tap spacing, coefficient resolution and filter length can be significantly reduced, while still providing good focusing property.

3.1.2 Waveform Preprocessing

Modern communication systems rely on analogue and digital signal processing to combat various impairments such as noise, channel fading (flat and frequency-selective fading), and interferences. For a given environment, a global optimum system under some sort of criterion delivers the best performance. By "global" we mean joint transmitter-receiver optimization. However, most existing work on the joint transmitter-receiver optimization is at symbol-rate level [21–26]. It can be expected that by breaking the symbol-rate constraint and allowing continuous-time or fractional-symbol-level processing, the performance can be improved further. In other words, given a communication channel, we prefer to design a set of transmit waveforms as well as a receiver with proper structure and algorithm, such that the system achieves some sort of optimum under some conditions and constraints. The signal processing goals could be capacity-reaching, maximum SNR, and minimum mean square error (MMSE), etc. In most wireless communication scenarios the channel characteristics are time-varying and up-to-date channel information is only available at the receivers. This is why traditionally signal processing efforts are focused on the receiver side.

It is reasonable to consider single-carrier pulse-based radio links for wireless sensor network (WSN) applications, since they have potential to be of low-complexity if major receiver-side linear processing functions are shifted to the transmitter side. It is well known that low probability of interception and low probability of detection (LPI/LPD) can be easily achieved using pulse-based signaling. Also, a narrow-pulse-based single-carrier system can be used for ranging or penetration radar purposes.

A unique issue associated with wireless communications is frequency-selective fading caused by multipath propagation. As for interferences in radio systems, ISI and inter-user interference (IUI) are typically concerned. Listed below are some receiver-based schemes to handle noise, multipath impact and interferences.

- Matched filter (MF): it is placed at the receiver and matches the given transmit symbol (or chip) waveform; for AWGN noise, it maximizes the SNR at the peak of the MF's output.

- RAKE receiver: a family of technique to collect the signal energy dispersed over multipath components; an ideal RAKE receiver actually matches the overall received waveform; when major paths are resolvable, a practical RAKE receiver structure can be a combination of a regular chip-level MF and a multipath combiner functioning as a finite impulse response (FIR) filter; a RAKE receiver operates at fractional-symbol (or fractional-chip) rate.

- Equalization: a symbol-rate discrete-time processing to remove or reduce ISI; an equalizer is placed at the receiver, usually taking symbol-rate samples from the MF's output as its input.

- (Receiver-based) multi-user detection: this is a broad range of techniques that remove or reduce IUI; the multi-user detection operates at symbol-rate.

When channel and/or multi-user information is available at the transmitter, it seems no strong reason not to use it. Recently, transmitter based signal processing, or preprocessing, has received increasing attention. Preprocessing can be time-reversal pre-filtering (or pre-RAKE), pre-equalization, multi-user precoding, or some processing for a set of compromised goals. Preprocessing can be used along in a transmitter-centric system where traditional receiver-based signal processing is shifted to the transmitters to simplify the receivers. It can also work with receiver-based signal processing to achieve joint transmitter-receiver optimization.

Our special interest is on preprocessing at fractional-symbol level (or simply, waveform preprocessing), in conjunction with a suboptimal receiver. Below are two examples of symbol waveforms.

- Pulse shaping: it uses a transmitter-side filter to create a transmit waveform that has desired roll-off spectrum; traditional pulse shapes include raised cosine and truncated sinc functions, etc.

- Maximum-SNR transmit waveform: a transmit symbol waveform to achieve the maximum SNR at the MF's output; it is an eigenfunction of the CIR autocorrelation (implying the CIR has to be known first); and a homogeneous Fredholm integral equation needs to be be solved for the eigenfunction with the strongest channel gain [27,28].

The transmit waveform optimization problem can be further stated in details as follows. It is well known that the optimum receiver matches the whole symbol waveform distorted by the channel, not the transmitted symbol waveform. However, from system optimization point of view, such a waveform matching alone is not enough. We can further maximize SNR at the receiver by carefully designing the transmitted waveform [27,28].

Given the channel impulse response $h(t)$ and fixed transmitted power P_t, we wish to achieve the maximum SNR at the receive by jointly designing the transmitted waveform and a good receiver. This problem has been discussed in [27] for communication over troposcatter channels and in [28] for radar detection.

Assuming the transmitted pulse $p(t)$ (to be optimized) is confined to the symmetric time interval $[-T/2, T/2]$. The energy of transmitted pulse is then

$$E_p = \int_{-T/2}^{T/2} |p(t)|^2 \, dt \; . \tag{3.1}$$

It follows from detection theory that the best receiver is still a MF matched to the received waveform $p(t) * h(t)$, where $h(t)$ is the CIR and "$*$" denotes convolution operation. The (maximum) SNR at the output of such an MF is given by

$$SNR = 2E_y/N_0, \tag{3.2}$$

where $E_y = \int_{-T/2}^{T/2} |p(t) * h(t)|^2 \, dt$ is the received signal energy. The problem is then reduced to find the optimum $p(t)$ such that E_y is maximized, under the constraint of fixed E_p.

It has been shown in [29] (p.125) and [28] that the optimum $p(t)$ can be obtained by solving the following homogeneous Fredholm integral equation

$$\mu_n \phi_n(t) = \int_{-T/2}^{T/2} \kappa(t-\tau)\phi_n(\tau) \, d\tau \; , \tag{3.3}$$

and let $p(t) = \phi_0(t)$, where $\phi_0(t)$ is the eigenfunctions corresponding to the maximum eigenvalue μ_0 and the kernel $\kappa(t)$ is the autocorrelation of the CIR: $\kappa(t) = h(t) * h(-t)$. When convolved with the kernel over the interval

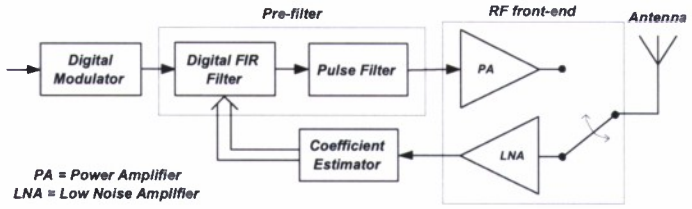


Figure 3.1: A conceptual transmitter structure capable of preprocessing (in the RF front-end frequency up- and down-conversion may be used to shift the signal frequency).

$[-T/2, T/2]$, pulse waveform $\phi_0(t)$ reproduces itself, scaled by a constant μ_0. With optimum $p(t) = \phi_0(t)$ we achieve the maximum SNR

$$SNR = 2\mu_0 E_p / N_0. \tag{3.4}$$

It is worth noting that this maximum-SNR waveform may lead to severe ISI if the duration of $p(t) = \phi_0(t)$ exceeds the symbol duration, which is one reason preventing the scheme from being widely applicable.

A transmitter capable of general waveform synthesizing or arbitrary waveform generating would be the ultimate goal of preprocessing. A digital FIR filter based waveform gencrator would be flexible and become more and more feasible as the semiconductor technology advances. A common structure of this type of waveform generators is a digital FIR filter followed by an analogue interpolating or shaping filter as illustrated in Fig.3.1. However, for any digital implementation, sampling rate as well as quantization resolution are limited. From a perspective of implementation, trade-off between performance and feasibility or cost must be made. Time reversal with mono-bit or ternary quantization and sub-Nyquist rate sampling has been proved working satisfactorily, according to computer simulation and test-bed based experiment [20,30]. The practical limitations should be considered in the performance optimization.

3.1.3 Energy Detector Based Receivers

Energy detection is a non-coherent detection technique that can be combined with many modulation schemes such as OOK, pulse position modulation (PPM) and frequency shift keying (FSK). Shown in Fig.3.2 is a conceptual architecture of energy detector based receiver. The advantages of energy detection include no need for channel estimation and higher energy efficiency than traditional TR. The energy detector can be implemented alternatively by a diode device working at square-law region, and an energy detector with OOK modulation can be of very low cost. Multiband energy detection receiver is a reasonable extension to support higher data rate and reject narrow-band interference (with filter bank).

Synchronization and thresholding are challenging issues with OOK energy detector receiver. The difficulty of initial timing acquisition is mainly due to not being able to use good PN codes with sharp autocorrelation, and multipath distortion makes the situation worse. The Optimal decision threshold for OOK and energy detector may be found theoretically [31]. In reality a real-time threshold must be available at the receiver, which motivates searching for adaptive- threshold strategies and effective algorithms.

Similar to TR receivers, gating or weighting the incoming signal has potential to improve the performance. To have the feature mentioned above, monitoring the signal strength in real time is a must, and the weighting method can add

too much computational complexity. In other words, implementing this feature can make the receiver less attractive because of increase of complexity.

Some research on performance evaluation of OOK energy detector scheme has been done recently [15]. The well-known Park's model that deals with Chi-square distribution approximately has been applied to OOK energy detector to obtain BER closed form considering ISI. The decision threshold is determined using the worst cases of ISI patterns.

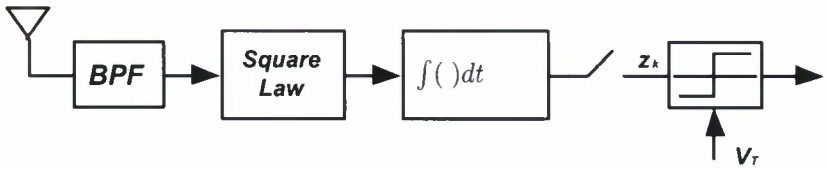


Figure 3.2: Energy detector receiver.

3.1.4 Prototyping

The main goal is to build a pair of concept-proof transmitter and receiver to test and verify various schemes. The testbed is expected to be flexible enough to accommodate several major transmission and reception techniques. The strategy is to develop the testbed based on our latest research work and use commercially available off-the-shelf components to expedite the project.

Module-based implementation methodology is adopted mainly in implementing the RF front-end to expedite the overall development. The pulse generator is based on gated oscillation principle that can be viewed as multiplying a digital pulse with an oscillation source. The major advantage of this pulse generator is high controllability of frequency band and spectral shape. The baseband part is implemented using FPGA and the signal processing is fully in digital domain, providing the test-bed with flexibility and programmability. A digital to analog converter (DAC) being able to offer a sampling rate at Giga samples per second (Gsps) is employed to generate desired waveform. The precoder challenge thus converts to the difficulty in mixed-signal circuitry, high-speed FIR filter and the interfaces between them. Connection bus between the D/A and FPGA baseband part is one of bottlenecks, and potential solutions include use of a bank of short coaxial cables. Even choosing the latest FPGA products, implementing the precoding and synchronization functions is extremely challenging.

The work of radio system design is to provide an efficient solution under some theoretical and practical criteria. A top-down design flow covers many aspects ranging from a very high level design to detailed implementations. A number of issues need to be considered: frequency band, architecture, data rate, modulation, synchronization, coexistence, interference, dynamic range, and many implementation issues. As for the system with preprocessing for wideband applications like UWB, one of the major challenges is in the waveform generator. Specifically, it is about how to choose a proper sampling rate as well as quantization resolution, and how to efficiently implement the algorithm. Based on our indoor experiments in UWB band, a reduced-complexity pre-filter can function very well and implementing time-reversal preprocessing for microwave-band communications is feasible [1]. A reference example of time reversal radio test-bed is presented in the following.

We adopt pulse based signaling and transmitter-side processing as system design guideline. Although direct pulse (carrierless) transmission can largely reduce complexity of transmitter RF front-end, it is not a good choice for

multi-purpose radio testbed mainly because of its inflexibility. As a matter of fact, a modulated pulse is not only easy to generate but also more flexible: the center frequency is controlled by a local oscillator and the spectral shape is governed by the baseband pulse. Conceptual testbed architecture is shown in Fig.2.1, where all baseband and control functions are implemented using FPGAs. Following an FIR filter (implemented in the FPGA), the DAC outputs desired analog waveforms. The simple receiver philosophy is reflected in this testbed with OOK or 2-PPM and diode based non-coherent detector at the receiver. At the receiver, demodulation is done in digital domain, so that algorithms and parameters can be adjusted easily.

3.2 Synchronization Based on Energy Detector

For a burst mode radio system, the synchronization has always been a challenge. In order to make the synchronization more robust for the testbed, we have made some improvements, which include modification of the frame structure, average samples for start pattern searching and various thresholds adjustment.

3.2.1 Synchronization Review

For UWB impulse radios signal initial acquisition is extremely difficult because of the very narrow pulses with ultra low power and low duty cycle. In the testbed, timing requirement is relaxed to the symbol level. Since energy detection employed in the testbed is not able to identify signal polarity, the initial acquisition has to rely on a unipolar sequence whose autocorrelation is typically less sharp than that of a bi-polar sequence. Optical orthogonal code (OOC) is used in the testbed for synchronization. The OOC codes can be more longer than the Barker code and exhibit better autocorrelation property, which is desirable for severe propagation cases. Two stage synchronization strategy is employed in the testbed. Tracking is not considered while the initial timing acquisition is implemented in the testbed.

The overall receiver functional diagram is shown as Fig. 3.3. The main modules include data interface between FPGA and ADC, integration, synchronization, decision, a finite state machine and thresholds control. Among them, the challenges at the receiver are mainly on the high speed interface, fast integration and the robust synchronization. We are currently using a 3 stage synchronization technique which is shown in Fig. 3.5.

Fig. 3.4 is the data flow for the receiver. First the interface module converts the high speed ADC output data to relatively low speed data streams through several steps. Then the data streams go to start pattern searching module to find the time of arrival and go to integration module for chip level energy integration. There are 32 fast integrators for integration, which are implemented by DSP cores embedded in Virtex-5 FPGA. The synchronization module combines the time of arrival signal and the integration results by finding the integrator with maximum energy, then it gets the chip threshold. After that the receiver applies frame level synchronization to find the fine timing and make decisions. The finite state machine and variable thresholds control module coordinate all the processes.

3.2.2 Frame Structure

The system is supposed to find the window with maximum energy in every 40 ns, which is the chip period. Fig. 3.5 shows the new frame structure of the system. The first stage is to search the time of arrival; the second stage is to average 128 chips energy to find the chip threshold; the third stage is to synchronize the whole frame. Data

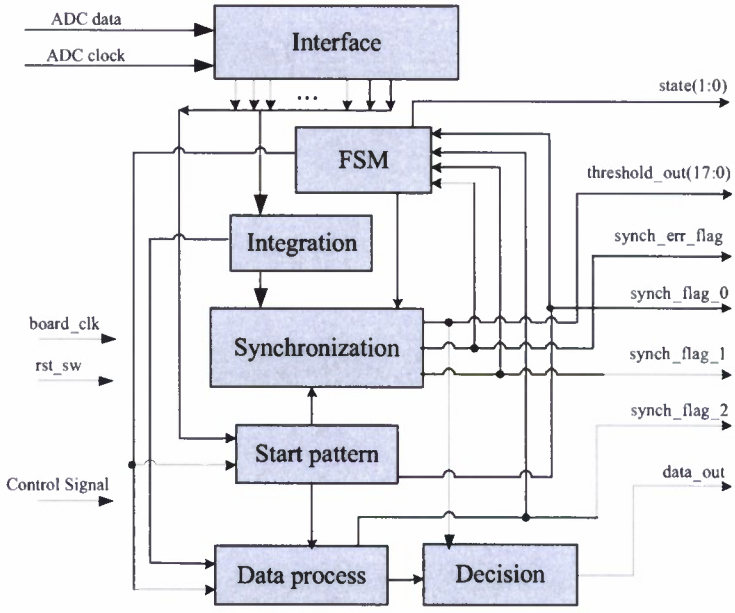


Figure 3.3: Receiver functional diagram

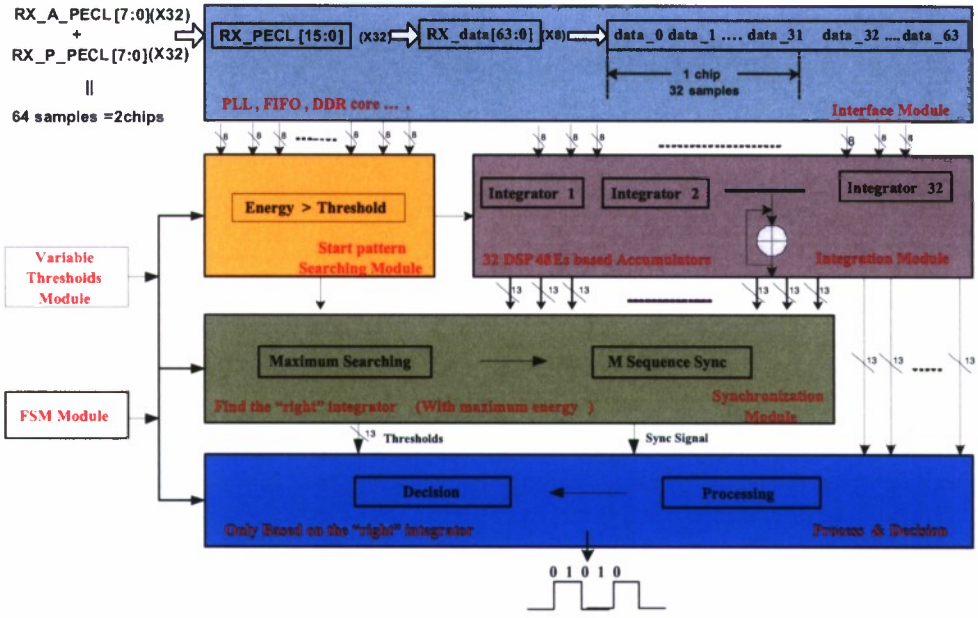


Figure 3.4: Receiver data flow

demodulation is performed after the three-stage synchronization. Fig. 3.5 also shows the sliding window integration diagram and the state transition diagram.

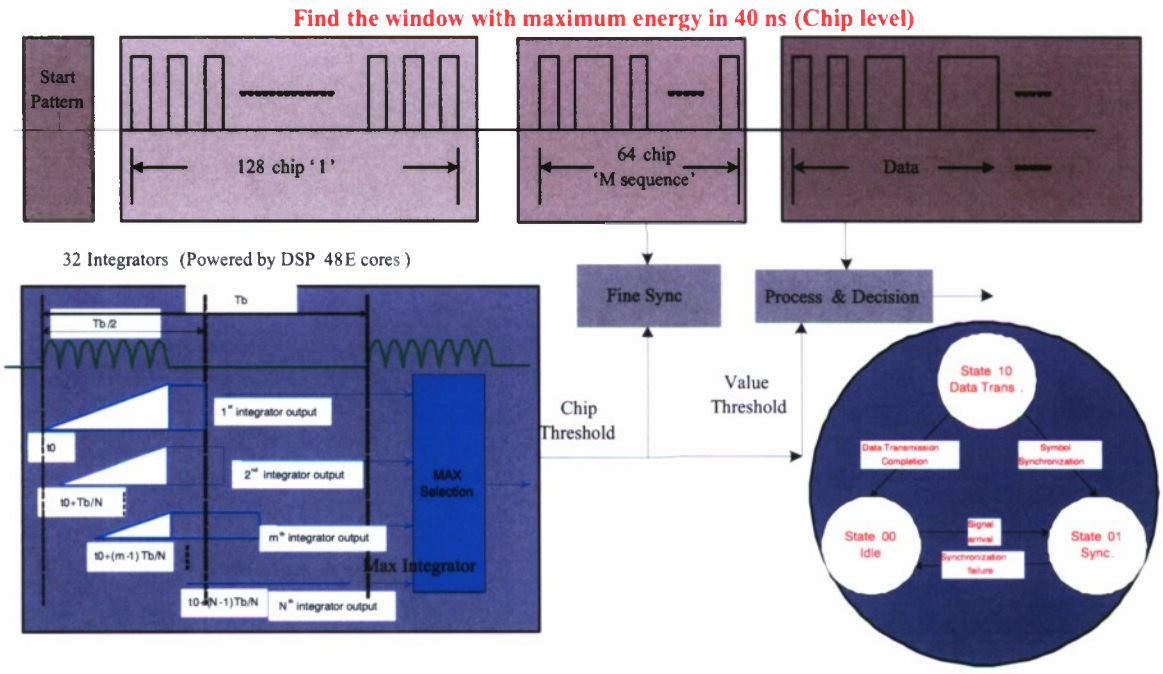


Figure 3.5: The new frame structure design

The modification in the synchronization head does not change the overall frame structure. The following parameters are kept: system's frame length: 4096 chips or 163.84 μs; payload efficiency: 94.49%; chip sync accuracy: one sample (1.25 ns); and frame sync accuracy: one chip (40 ns). If the overall clock accuracy is 20 PPM, then the maximum time drift is $163.84 \times 10^{-6} = 3.276$ μs.

3.2.3 Dense Pulses

However, even though we averaged the start pattern searching, we observed that the synchronization error still mainly comes from the first stage. In this stage, the threshold is very sensitive to noise level and DC offset of ADC sampling, especially for longer distance transmission. So we try to send 5 chips long dense pulses at the beginning of each frame to make sure the time of arrival is found each frame since the average value of these chips should be much higher than ordinary ones. Fig. 3.6 shows the real picture of dense pulses at the beginning of each frame.

3.2.4 Start Pattern Averaging

For the first synchronization stage, we accumulate the values of 32 consecutive samples and compare it with a threshold to claim whether it is one frame's time of arrival. However, due to the interference and environment's uncertainty, the first stage result should not be so reliable when it just counts on the value only one chip time, because the time frame is too short. So we try to average two chip time samples result to get the averaged value, and

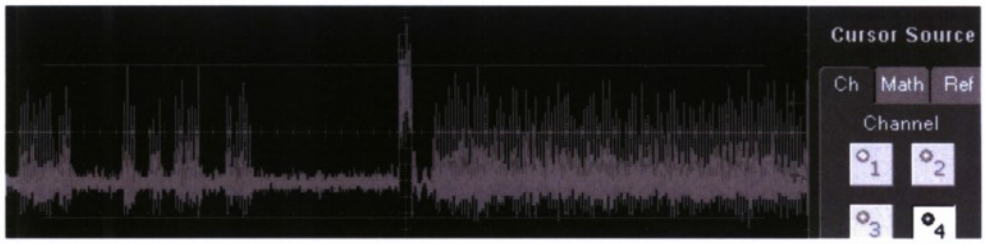


Figure 3.6: The picture of dense pulse at the beginning of each frame

compare it with a threshold, Fig. 3.7 shows the diagram of this improvement, where we set a more strict condition to claim the time of arrival result by comparing 5 times(or other number) instead of only one, and is in 5 chips time(or other number), 3 high results are needed to claim the first stage synchronization result. After that, because we send dense pulses at the beginning of each frame and there is a interval between the pulses and the real chips, we delay two chips time before the beginning of second stage.

3.2.5 Thresholds Adjustment

For energy detection based receiver, it is well known that the performance depends significantly on the choice of threshold level. A good threshold can bc determined by using some channel quality indicator and feedback information provided by the digital processor (back-end) at the receiver. There is an optimum threshold for lowest error rate. To deal with ISI situation, it is proposed to set a threshold based on two worst signal cases.

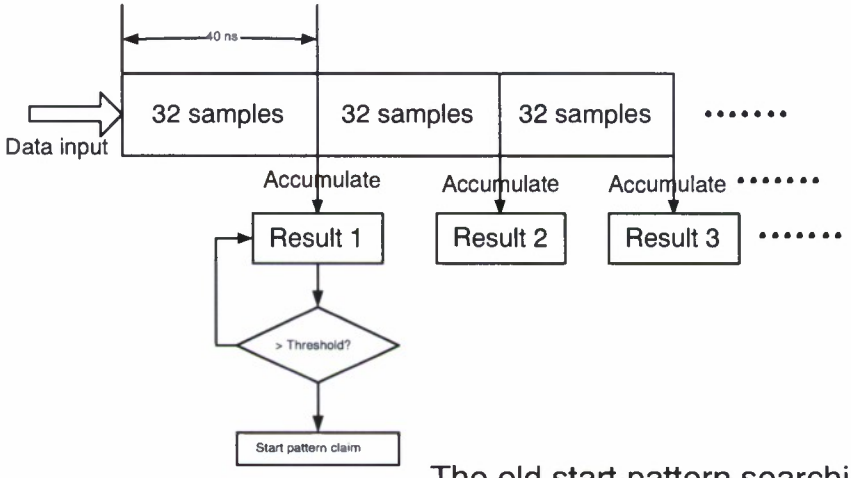
One phenomenon discovered is that a mono-bit ADC along with proper thresholding can be applied for quantizing the pre-filters coefficients, and the resulting signal still gets focused. It enables the development of a unique time reversal system with much lower complexity. Major points include: (1) optimization of the threshold for quantization; (2) development of an adaptive threshold method; (3) impact of tap spacing and length of the pre-filter. In our case, there are 4 variable thresholds at the receiver side with each corresponds to different stages of synchronization and detection. They are the threshold for start pattern searching, the threshold for ADC bias shift, the code distance for frame level synchronization and the threshold of chip threshold determine at the second synchronization stage. All these values are adjusted by thc pushbuttons on the receiver Virtex-5 board and the led lights can show any threshold's adjustment level.

DC offset causes performance degradation in signal processing systems especially for high-speed applications. For our ADC board in the receiver side, the DC shift makes the true quantization value hard to determine, thus makes the threshold vulnerable, especially for the energy detection based receiver with OOK modulation. DC offset can be reduced in real-time by subtracting the mean amplitude from each sample, or by calibrating the ADC board.

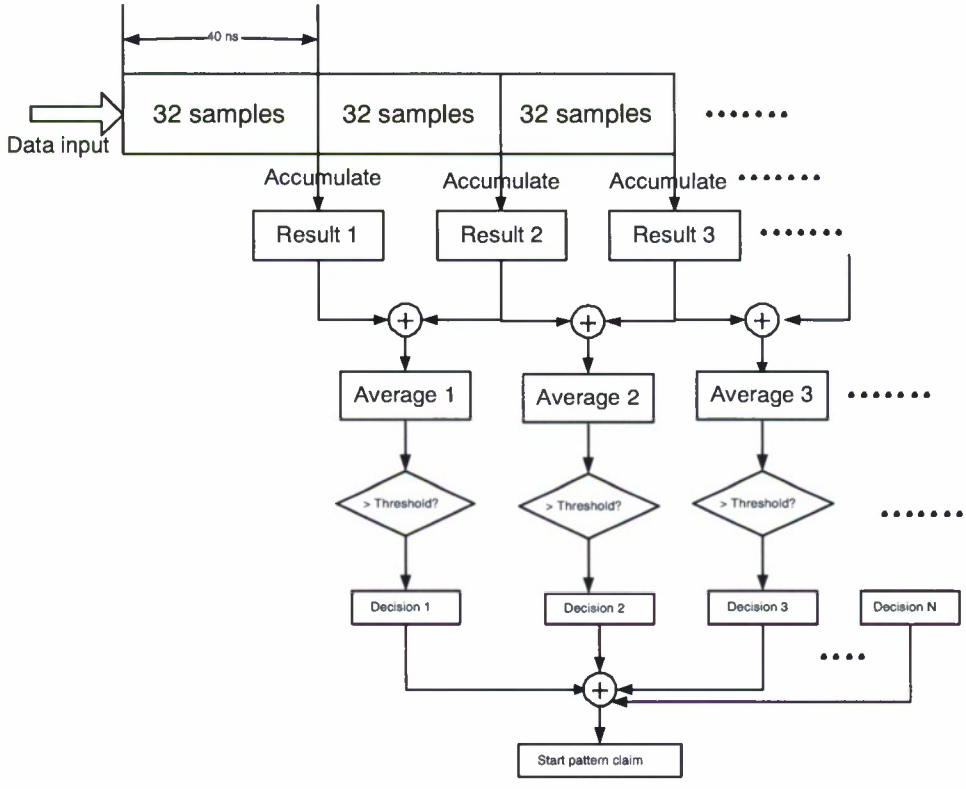
3.2.6 Other issues considered

For the third stage,we also utilized 60 bits M sequence instead of 60 bits OOC code for frame synchronization. This is mainly because the randomness of M sequence is much better than OOC code.

For time reversal system and non timc reversal system, the received pulses are very different at the width, typically 6 ns for time reversal and 15 ns for non time reversal. So in the energy integration module, the window size for



The old start pattern searching



The new start pattern searching

Figure 3.7: Start pattern searching improvement

integration should be different for different signal scenarios, this parameter is to be adjusted in integration module.

3.3 Arbitrary Waveform Generator

Arbitrary waveform generator (AWG) is one of the essential achievements in this project. AWG gives a way to implement a variety of waveforms for different kinds of systems, i.e. communication system, radar system or imaging system, which makes waveform diversity real and practical. Generally, AWG consists of RF part, high sampling rate digital to analog converter and digital AWG.

In this project, digital AWG is the core part in the backend at the transmitter. Digital AWG can generate virtually any type of transmitted waveforms according to the design objectives, which greatly increases the capability of UWB communication system. The performance parameters of current digital AWG is summarized as follows. The quantization resolution is 8 bits, which is enough for most of the real waveforms. The sampling rate of output digital data is 1 GHz which is much faster than any commercial systems. The number of channels is 2. Thus I/Q data can be generated simultaneously. The number of waveform coefficients is 160. Data memory is added into digital AWG. Data memory plus 8 groups of shift registers are used to store the waveform coefficients. In this way, the loading of waveform coefficients into FPGA is much easier. Boolean operation and mathematical computation are used, which can support the calculation of input data with higher quantization resolution.

How can we use FPGA with 550MHz maximum clock rate to generate the output digital data with 1GHz sampling rate? Parallel to Serial Converter gives us a hope. The overall structure of digital AWG for one channel is shown in Figure 3.8. Waveform coefficients are stored in Data Memory. When FPGA powers on, waveform coefficients can be automatically loaded from Data Memory to the corresponding group of shift registers. There are 8 groups of shift registers. And each group of shift registers corresponds to one Process Module. The clock rate of each group of shift registers plus the corresponding Process Module is 125 MHz. Finally Parallel to Serial Converter is used to generate the output digital data with 1GHz sampling rate.

For each channel, we have 8 groups of shift registers and each group can store 20 waveform coefficients shown in Figure 3.9. So totally we can have 160 waveform coefficients for each channel.

Now the multiplication and addition shown in Figure 3.10 are exploited to perform the calculation. In this way, the Verilog code is more compact and readable. The calculation of input data with higher quantization resolution can be supported.

Format Regulation uses Boolean operation to generate complementary code for the following processing in Process Module according to the scrambling code generated by Scrambling Code Generator and the value of input chip.

The key module in digital AWG is the high speed Parallel to Serial Converter, the structure of which is shown in Figure 3.11. Through this way, the high speed requirement of the output digital data is relaxed by parallel computation and Parallel to Serial Converter. The function of parallel to serial conversion is implemented by OSERDES logical resources in Virtex-5 FPGA. Each OSERDES logical component can support 6 to 1 parallel to serial conversion, but we need 8 to 1 parallel to serial conversion, so two components are used to build one converter. One component is called master and one other is slave. The function diagram is shown in Figure 3.12. In our design, the sampling rate of input data from 8 parallel branches is 125 MHz and sampling rate of the output digital data is 1 GHz.

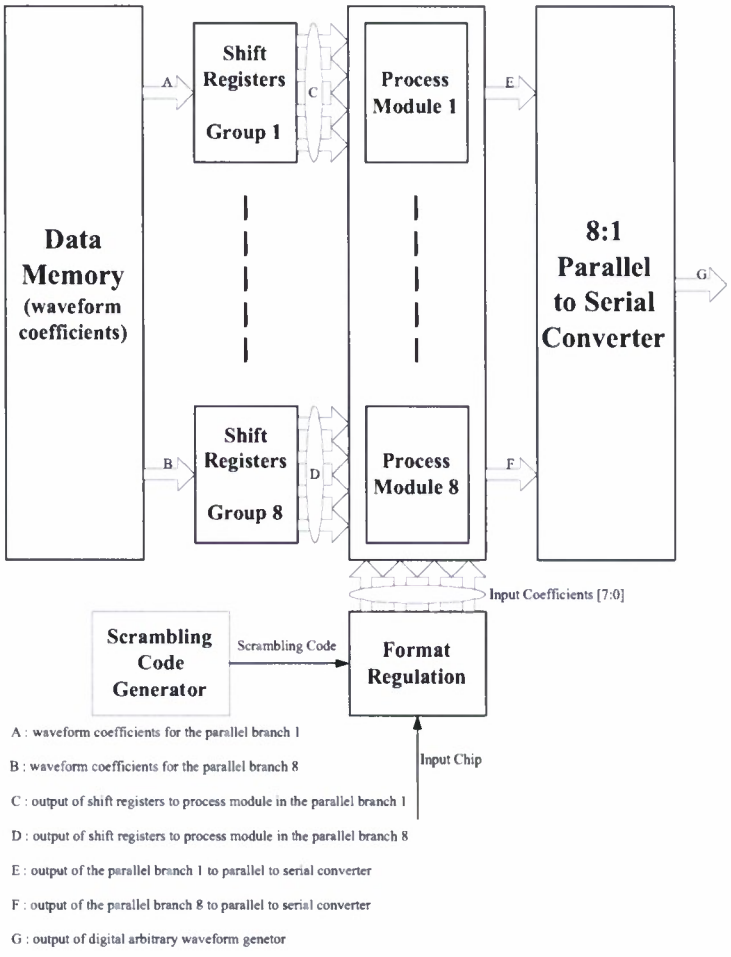


Figure 3.8: Overall structure of digital AWG for one channel.

3.4 High Speed FPGA-DAC Interface

High speed FPGA-DAC interface is challenging. Our Fujitsu MB86064 DAC supports dual channel 14-bit 1 GHz sampling rate. However, the earlier version of our testbed only reached 500 Msps with 2-bit resolution. This is far below the capability of the DAC. This limited performance is due to the interface between FPGA evaluation board (EB) and DAC development kit (DK). Since the FPGA EB of our earlier testbed version is not designed for high-speed connection, synchronized pins are rare when data rate is over 500 Mbps. In the final testbed platform, we used a new FPGA EB, ML550, which is designed for high-speed data transmission. Here we will introduce ML550 and the connection between it and DAC DK.

The ML550 Networking Interfaces Platform has an XC5VLX50T-FFG1136 FPGA on chip. The key features are:

- 64M x 8 DDR SDRAM memory
- Eight clock sources: - 200 MHz, 250 MHz, 133 MHz, and 33 MHz on-board oscillators - Two ICS8442 clock synthesizer devices

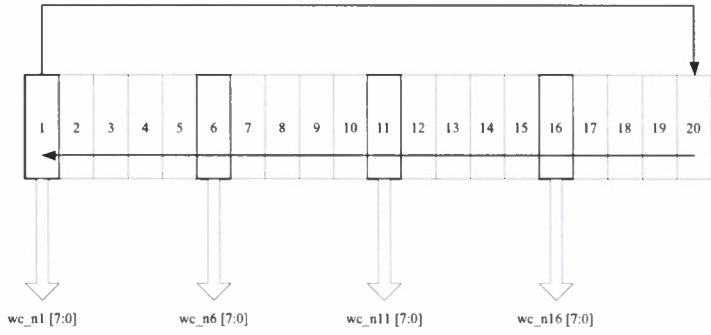


Figure 3.9: Digram of shift registers.

- One USB "B" port
- One 64 x 128 pixel LCD
- A System ACE CompactFlash (CF) Configuration Controller that allows storing Six Samtec LVDS connectors (a total of 53 differential input and 53 differential output
- Onboard power regulators with 5% output margin test capabilities, in 2.5% Power monitor connector for detailed current measurements on Vccint, Vccaux, and Vcco supplies

The clock and interfacing components on ML550 are very powerful. The differential SMA clock inputs are connected to the global clock inputs of the FPGA. An onboard 200-MHz oscillator calibrates the I/O delay, and an onboard 250-MHz oscillator is provided for general use. The two ICS8442 clock synthesizer devices output differential LVDS clocks in the 31.25 MHz to 700 MHz range, which can drive LVDS data rate up to 1.4 Gbps. The ML550 provides 53 pairs of transmit signals and 53 pairs of receive LVDS signals. These signals are distributed across three Samtec QSE-DP connectors for transmitting and another three connectors for receiving. The number of LVDS output and the speed of the LVDS data rate can maximize the DAC's capability to dual channel 14-bit 1 Gsps output.

Fujitsu and Xilinx developed an application to drive the DAC DK with ML550. An interface adapter is built by Fujitsu (Fig. 3.13). This adapter can be directly plugged onto the DAC DK 0.1" pitch header. Two SAMTEC EQCD high-speed ribbon cables are used to connect the adapter and ML550. The complete interface setup is illustrated in Fig. 3.14. The ribbon cable supports data rate up to 2.84 Gbps. The pin assignments, a.k.a. mappings between the Fujitsu DAC input ports and FPGA output ports are tested and built as a user constraint file. It can be loaded in the FPGA design and drive the DAC properly.

3.4.1 Interface Performance Test

Fujitsu and Xilinx provided an application note to verify this setup with MB86065. An experiment was tested to show that this setup can drive single-port 14-bit 1.3 Gsps data into DAC. In our application however, we need to verify its ability to drive dual-port 14-bit 1 Gsps data.

The purpose of the interface is to fully utilize the performance of the DAC, which is the dual channel, 1 Gsps and 14-bit quantization. A test environment is built to test the performance. All DAC outputs are driven from FPGA

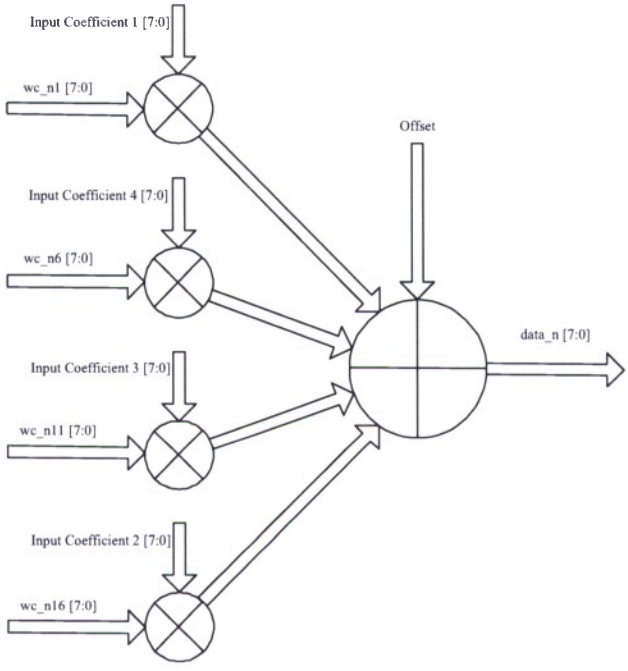


Figure 3.10: Strucuture of Process Module.

with the interface solution. FPGA driven waveforms are compared with the waveform memory module driven ones, since the latter ones are considered to be correct. We use ramp waveform as the test waveform. Two identical ramp waveforms are generated by FPGA to feed DAC ports A and B. They are both identical to the ones generated by waveform memory and they are perfectly synchronized. In another test with results shown in Fig. 3.15, a 14-bit mono-cycle 1 ns pulse is generated. The pulse width is a little bit over 1 ns and there is a tail behind the pulse. This is caused by the circuit of the DAC evaluation board because the property of the tail does not change according to cable lengths. The spectrum of the mono-cycle pulse is depicted in Fig. 3.16, with a 3 dB bandwidth around 1 GHz. Another result is that the lower 9-14 bits of the DAC are under the noise level and can not be observed. So, the configuration of the DAC becomes dual channel, 1 Gsps and 8-bit quantization, which is a great improvement to the earlier version of the testbed.

In the test, we have verified that all I/Os are synchronized. The maximum data rate is not limited by the DAC and interface, but FPGA. The maximum output rate of FPGA is 1.4 GHz. If we want to upgrade our DAC to over 1.4 GHz sampling rate, we need another solution. In such case, a DAC with in-chip parallel to serial conversion is necessary. For example, the MAXIM 4.3 Gsps DAC uses a 4:1 MUX to drive the DAC, and therefore the sampling rate of each of the 4 data channels is reduced to 1.075 GHz, which is below the limit of the ML550 I/O interface.

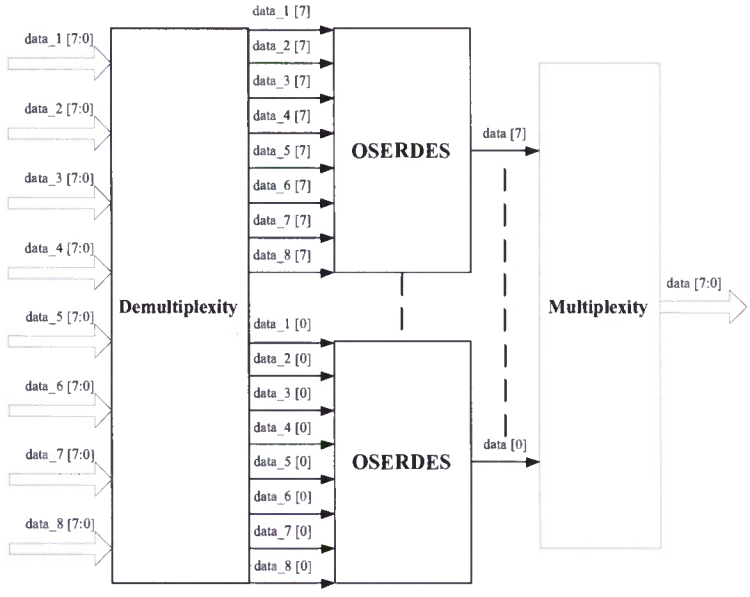


Figure 3.11: Strucuture of Parallel to Serial Converter.

3.5 Challenges in System Implementation

3.5.1 High Speed A/D and D/A Converters

We are utilizing the MAX108 evaluation board to perform the analog-to-digital conversion in the receiver side, the FPGA board and the ADC board are connected together through 50 Ω SMA cables, with a ADC/FPGA interface board which is plugged into the FPGA development board, The interface solution can support signals with frequency of up to several GHz.

For the design of the high-speed interface between ADC and FPGA, signal integrity has become a critical issue. Many signal integrity problems are electromagnetic phenomena in nature and hence related to the EMI/EMC. There are two concerns for signal integrity - the timing and the quality of the signal. Signal timing mainly depends on the delay caused by the physical length that the signal must propagate. Signal waveform distortions can be caused by reflection, cross talk and power/ground noise.An interface board must be carefully designed to solve the signal integrity issue.

A 4-layer PCB board is designed and fabricated to have 50 Ω characteristic impedance for each trace. The PCB layer stack is shown in Fig. 3.17. For each pair of LVPECL signals, the traces are designed to have same length such that the positive and negative signals experience same delay.

3.5.2 FPGA Implementation Timing Closure Issues

Tremendous effort has been made in developing the FPGA based digital back-ends. One lesson we have learned is that in the FPGA implementation phase time closure is very critical in dealing with nano-second-order signals,

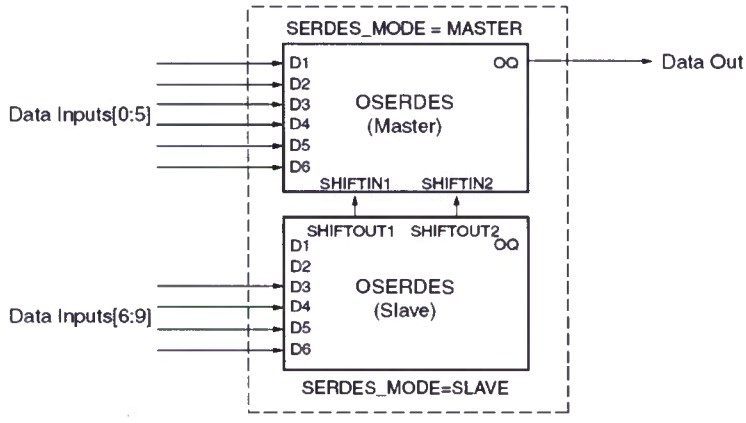


Figure 3.12: Strucuture of OSERDES expansion.

especially when the area usage is high (say, 80%). FPGA technology advances rapidly and many high-speed dense FPGA products are on the market. We have been using the latest Xilinx Virtex-5 FPGA chips in the test-bed, which truely lessens the in-chip timing problem. However, when we push the samping rate higher and higher, the connection between the FPGA chips and the DAC or ADC becomes new bottle neck.

For FPGA implementation, meeting timing requirements in speed-critical designs has been always a challenge, and this is often an iterative process ensuring that each and every path in the design meets the required timing. Meeting timing closure is easy and automatic for relatively slow or small designs. However, most designs do not fall into that happy category and as each critical path is adjusted in order to meet timing, new ones are uncovered or created anew. In the case of FPGAs implemented at the 65nm technology node, for example, wire delays can account for 80-to-90% of each path's delay.

An important technique for achieving successful timing closure on an aggressive design is to carefully review the most critical timing constraints. In our case, there are two critical paths at the transmitter: one is from the data loading module to the waveform generator module where huge parallel data steams exist, another critical path is in the parallel to serial conversion module requiring high clock rate. At the receiver side, the most critical path is from the integration module to the synchronization module which performs fast timing acquisition in parallel manner. Achieving clock-to-clock (global) timing for all internal signals in a synchronous design may be easy, but this simple approach will usually overconstrain the design and eventually lead to a failure. Therefore, we have applied different constraints to different paths depending on their timing requirements.

FPGA design sizes have reached unprecedented levels with million gate parts becoming increasingly common, However, the issue of timing closure on the larger and more complex FPGAs has become one of the more daunting for designers to tackle without the right set of tools. The timing closure problem for these high-end FPGAs has its root in the increased net delays in relation to the gate delays. The design size and interconnect issues together have led to an inefficient iterative methodology in completing designs.

Figure 3.13: Passive interface adapter

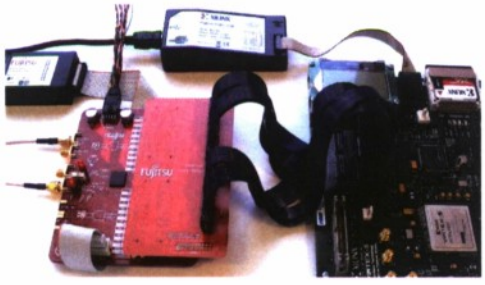


Figure 3.14: Interface setup connecting ML550 and Fujitsu DAC DK

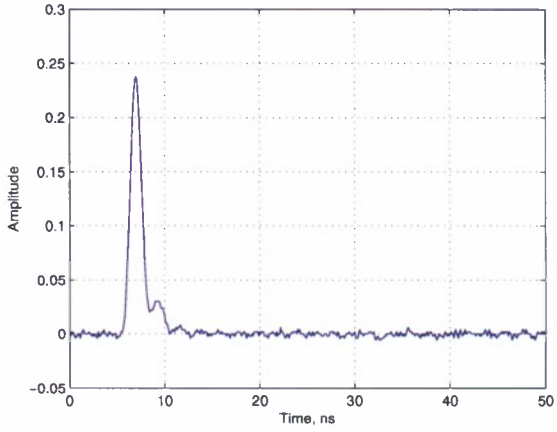


Figure 3.15: A 1 ns pulse generated by DAC.

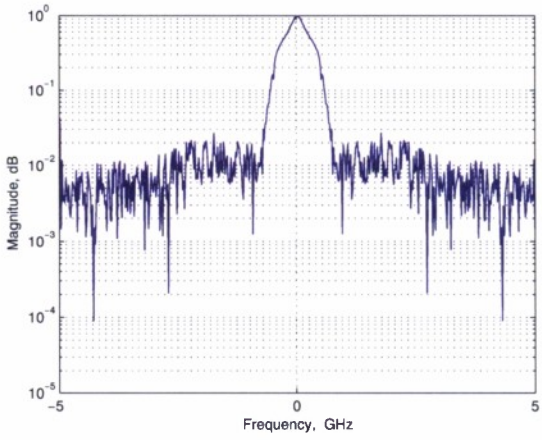


Figure 3.16: The spectrum of a 1 ns pulse generated by DAC.

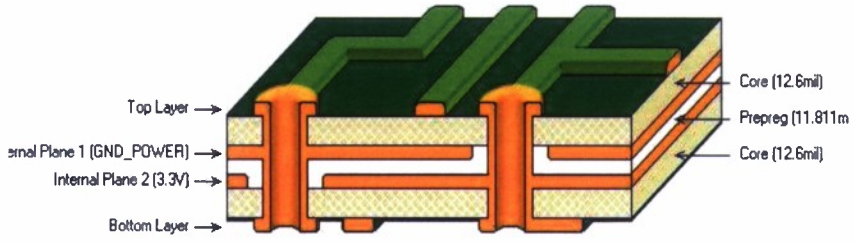


Figure 3.17: New interface board PCB layer stack

For the testbed, timing closure issues exist in both the transmitter side and receiver side. Since transmitter side utilizes less resources and the logic is not as complex as the receiver side, so the timing closure issue is relaxed. However, in the receiver side, timing closure is critical for its large design size and complex logics, even in the new Virtex-5 FPGA.

Typically, there are global timing constraints, Offset constraints, specific path constraints, groups constraints. In some advanced design, there are area constraints, which enable partitioning of the design into physical regions for mapping, packing, placement, and routing. The timing closure flow can be shown as Fig 3.18. Generally, designs over 50MHz should use timing constraints, while for the testbed, processing rate is up to 400Mhz in the interface module. After applying global timing constraints, if the system meets the timing requirements, then there is no need to add other constraints. Otherwise, there is a need to increase place and route effort, if it still fails to meets timing, then we need to find the specific paths and add critical path constraints. After that, we may need to run multi-pass place and route, further, we may also need to do some floorplan work. For special cases, area constraints may be employed. If all these strategies still can't meet timing closure requirements, then the only solution is to go back to start over and rewrite the codes.

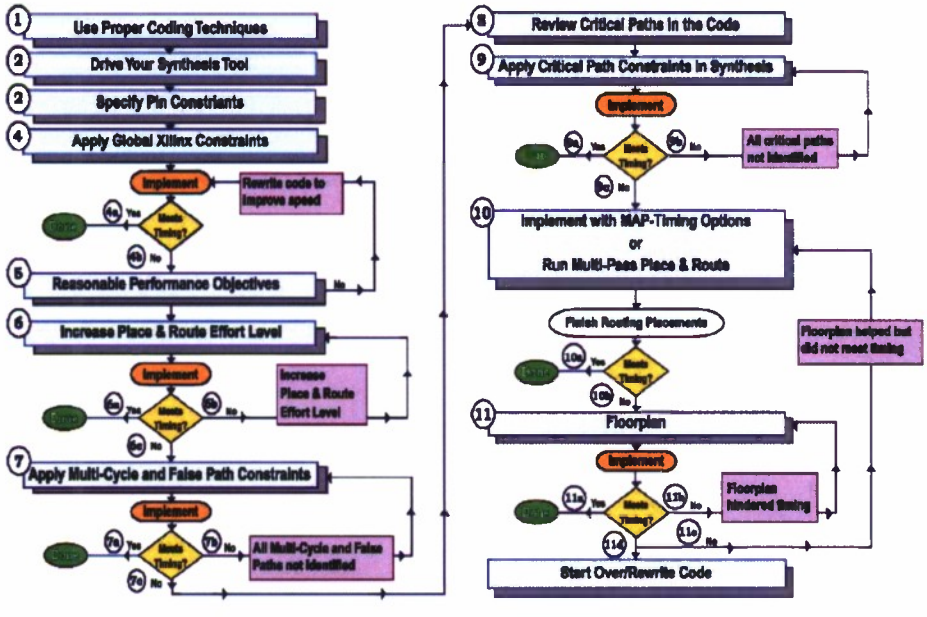


Figure 3.18: Xilinx FPGA timing closure flow

The impact of timing constraints can be seen in Fig. 3.19, where the left picture shows the output waveform from the DAC when appropriate timing constraints are applied, while the right one shows the waveform with unwanted spikes when timing constraints are not properly added.

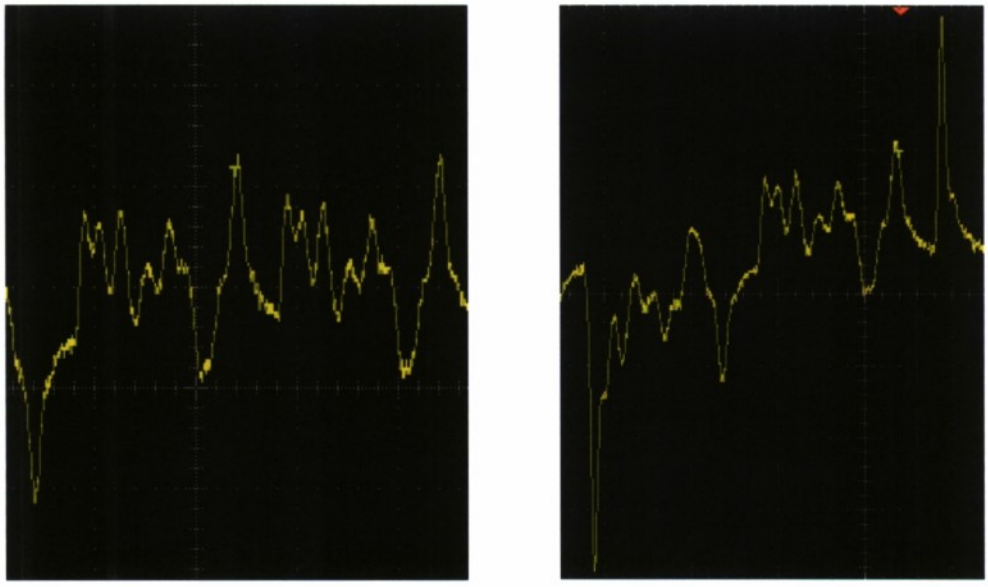


Figure 3.19: Output waveforms comparison with and without applying proper timing constraints

3.6 Some Lessons Learned

Tremendous effort has been made in developing the FPGA based digital back-ends. One lesson we have learned is that in the FPGA implementation phase time closure is very critical in dealing with nano-second-order signals, especially when the area usage is high (say, 80%). FPGA technology advances rapidly and many high-speed dense FPGA products are on the market. We have been using the latest Xilinx Virtex-5 FPGA chips in the test-bed, which truely lessens the in-chip timing problem. However, when we push the samping rate higher and higher, the connection between the FPGA chips and the DAC or ADC becomes new bottle neck. In the transmitter side, this sinal integrity problem prevents us from reaching higher clock rate beyond 500 MHz. In other words, to knock down this clock rate barrier we should seek a PCB-integrated FPGA/DAC solution.

Chapter 4

Theoretical Work and Forward Looking

4.1 Waveform Optimization

From theoretical point of view, one byproduct achievement form this project is systematic study of waveform optimization for wideband communication systems. Based on the transceiver scheme, radio environment and quality of service (QoS) requirement, the transmitted wideband waveform can be designed and optimized elaborately. This means the waveform can be diverse and adaptive, far beyond the traditional fixed Gaussian pulse or the time reversed channel impulse response.

4.1.1 Wideband Waveform Optimization for Energy Detector Receiver with Practical Considerations

System Description and Optimal Waveform

The system architecture is shown in Figure 4.1. We limit our discussion to a single-user scenario, and consider the transmitted signal with OOK modulation given by

$$s(t) = \sum_{j=-\infty}^{\infty} d_j p(t - jT_b) \tag{4.1}$$

where T_b is the symbol duration, $p(t)$ is the transmitted symbol waveform defined over $[0, T_p]$ and $d_j \in \{0, 1\}$ is j-th transmitted bit. Without loss of generality, assume the minimal propagation delay is equal to zero. The energy of $p(t)$ is E_p,

$$\int_0^{T_p} p^2(t)\, dt = E_p \tag{4.2}$$

The received noise-polluted signal at the output of the receiver front-end filter is

$$\begin{aligned} r(t) &= h(t) \otimes s(t) + n(t) \\ &= \sum_{j=-\infty}^{\infty} d_j x(t - jT_b) + n(t), \end{aligned} \tag{4.3}$$

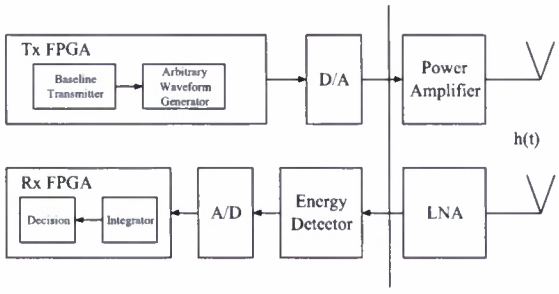


Figure 4.1: System architecture.

where $h(t), t \in [0, T_h]$ is the multipath impulse response that takes into account the effect of channel impulse response, the RF front-ends in the transceivers including antennas. $h(t)$ is available at the transmitter [32] [33]. "$\otimes$" denotes convolution operation. $n(t)$ is a low-pass additive zero-mean Gaussian noise with one-sided bandwidth W and one-sided power spectral density N_0. $x(t)$ is the received noiseless symbol-"1" waveform defined as

$$x(t) = h(t) \otimes p(t) \tag{4.4}$$

We further assume that $T_b \geq T_h + T_p \overset{\text{def}}{=} T_x$, i.e. no existence of ISI.

An energy detector performs square operation to $r(t)$ without any explicit analog filter at the receiver. Then the integrator does the integration over a given integration window T_I. Corresponding to the time index k, the k-th decision statistic at the output of the integrator is given by

$$z_k = \int_{kT_b+T_{I0}}^{kT_b+T_{I0}+T_I} r^2(t)dt \tag{4.5}$$

$$= \int_{kT_b+T_{I0}}^{kT_b+T_{I0}+T_I} (d_k x(t - kT_b) + n(t))^2 dt \tag{4.6}$$

where T_{I0} is the starting time of integration for each symbol and $0 \leq T_{I0} < T_{I0} + T_I \leq T_x \leq T_b$.

An approximately equivalent SNR for the energy detector receiver, which provides the same detection performance when applied to a coherent receiver, is given as [34]

$$\text{SNR}_{\text{eq}} = \frac{2\left(\int_{T_{I0}}^{T_{I0}+T_I} x^2(t)\,dt\right)^2}{2.3T_I W N_0^2 + N_0 \int_{T_{I0}}^{T_{I0}+T_I} x^2(t)\,dt} \tag{4.7}$$

For best performance, the equivalent SNR SNR_{eq} should be maximized. Define,

$$E_I = \int_{T_{I0}}^{T_{I0}+T_I} x^2(t)\,dt \tag{4.8}$$

For given T_I, N_0 and W, SNR_{eq} is the increasing function of E_I. So the maximization of SNR_{eq} in Eq. (4.7) is equvalent to the maximization of E_I in Eq. (4.8).

So the optimization problem to get the optimal $\mathbf{p}$ is shown below,

$$\begin{aligned} &\max \int_{T_{I0}}^{T_{I0}+T_I} x^2(t)\,dt \\ &s.t. \int_0^{T_p} p^2(t)\,dt = E_p \end{aligned} \tag{4.9}$$

In order to solve the optimization problem (4.9), numerical approach is employed. In other words, $p(t)$, $h(t)$ and $x(t)$ are uniformly sampled (assumed at Nyquist rate), and the optimization problem (4.9) will be converted to its corresponding discrete-time form. Assume the sampling period is T_s. $T_p/T_s = N_p$, $T_h/T_s = N_h$ and $T_x/T_s = N_x$. So $N_x = N_p + N_h$.

$p(t)$, $h(t)$ and $x(t)$ are represented by $p_i, i = 0, 1, \ldots, N_p$, $h_i, i = 0, 1, \ldots, N_h$ and $x_i, i = 0, 1, \ldots, N_x$ respectively [34].

Define,

$$\mathbf{p} = [p_0 \; p_1 \; \cdots \; p_{N_p}]^T \tag{4.10}$$

and

$$\mathbf{x} = [x_0 \; x_1 \; \cdots \; x_{N_x}]^T \tag{4.11}$$

Construct channel matrix $\mathbf{H}_{(N_x+1)\times(N_p+1)}$,

$$(\mathbf{H})_{i,j} = \begin{cases} h_{i-j}, 0 \leq i-j \leq N_h \\ 0, \quad else \end{cases} \tag{4.12}$$

where $(\bullet)_{i,j}$ denotes the entry in the i-th row and j-th column of the matrix or vector. Meanwhile, for vector, taking $\mathbf{p}$ as an example, $(\mathbf{p})_{i,1}$ is equivalent to p_{i-1}.

The matrix expression of Eq. (4.4) is,

$$\mathbf{x} = \mathbf{H}\mathbf{p} \tag{4.13}$$

and the constraint in the optimization problem (4.9) can be expressed as,

$$\|\mathbf{p}\|_2^2 T_s = E_p \tag{4.14}$$

where "$\|\bullet\|_2$" denotes the norm-2 of the vector. In order to make the whole document consistent, we further assume,

$$\|\mathbf{p}\|_2^2 = 1 \tag{4.15}$$

Let $T_I/T_s = N_I$ and $T_{I0}/T_s = N_{I0}$. The entries in $\mathbf{x}$ within integration window constitute $\mathbf{x}_I$ as,

$$\mathbf{x}_I = [x_{N_{I0}} \; x_{N_{I0}+1} \; \cdots \; x_{N_{I0}+N_I}]^T \tag{4.16}$$

and E_I in Eq. (4.8) can be equivalently shown as,

$$E_I = \|\mathbf{x}_I\|_2^2 T_s \tag{4.17}$$

Simply dropping T_s in E_I will not affect the optimization objective, so E_I is redefined as,

$$E_I = \|\mathbf{x}_I\|_2^2 \tag{4.18}$$

Similar to Eq. (4.13), $\mathbf{x}_I$ can be obtained by,

$$\mathbf{x}_I = \mathbf{H}_I\mathbf{p} \tag{4.19}$$

where $(\mathbf{H}_I)_{i,j} = (\mathbf{H})_{N_{I0}+i,j}$ and $i = 1, 2, \ldots, N_I + 1$ as well as $j = 1, 2, \ldots, N_p + 1$.

The optimization problem (4.9) can be represented by its discrete-time form as,

$$\begin{aligned} &\max E_I \\ &s.t. \ \|\mathbf{p}\|_2^2 = 1 \end{aligned} \tag{4.20}$$

The optimal solution $\mathbf{p}^*$ for the optimization problem (4.20) is the dominant eigen-vector in the following eigen-function [34],

$$\mathbf{H}_I^T \mathbf{H}_I \mathbf{p} = \lambda \mathbf{p} \tag{4.21}$$

Furthermore, E_I^* will be obtained by Eq. (4.18) and Eq. (4.19).

Trade-Off between Energies Within and Outside Integration Window

The energy outside of the integration window needs to be concerned somctimes, say, when ISI has to be considered. In order to reduce ISI, the energies within and outside of intcgration window should be balanced, which means the energy within integration window should be maximized and the energy outside of integration window should be minimized.

The entries in $\mathbf{x}$ outside of integration window constitute $\mathbf{x}_{\bar{I}}$ as,

$$\mathbf{x}_{\bar{I}} = [x_0 \ \cdots \ x_{N_{I0}-1} \ x_{N_{I0}+N_I+1} \ \cdots \ x_{N_x}]^T \tag{4.22}$$

and the energy outside of integration window $E_{\bar{I}}$ can be expressed as,

$$E_{\bar{I}} = \|\mathbf{x}_{\bar{I}}\|_2^2 \tag{4.23}$$

Similar to Eq. (4.19), $\mathbf{x}_{\bar{I}}$ can be obtained by,

$$\mathbf{x}_{\bar{I}} = \mathbf{H}_{\bar{I}} \mathbf{p} \tag{4.24}$$

where $(\mathbf{H}_{\bar{I}})_{i,j} = (\mathbf{H})_{i,j}$ when $i = 1, \ldots, N_{I0}$ and $(\mathbf{H}_{\bar{I}})_{i-(N_I+1),j} = (\mathbf{H})_{i,j}$ when $i = N_{I0} + N_I + 2, \ldots, N_x + 1$ as well as $j = 1, 2, \ldots, N_p + 1$.

In order to balance energies within and outside of integration window, the trade-off factor α is introduced. The range of α is from 0 to 1. Given α, the optimization problems is formulated as follows,

$$\begin{aligned} &\max \alpha E_I - (1-\alpha) E_{\bar{I}} \\ &s.t. \ \|\mathbf{p}\|_2^2 = 1 \end{aligned} \tag{4.25}$$

The optimal solution $\mathbf{p}^*$ for the optimization problem (4.25) is the dominant eigen-vector in the following eigen-function,

$$\left[\alpha \mathbf{H}_I^T \mathbf{H}_I - (1-\alpha) \mathbf{H}_{\bar{I}}^T \mathbf{H}_{\bar{I}}\right] \mathbf{p} = \lambda \mathbf{p} \tag{4.26}$$

Binary Waveform

If the transmitted waveform is constrained to the binary waveform because of the hardware limitation or implementation simplicity, which means $p_i, i = 0, 1, \ldots, N_p$ is equal to $-\frac{1}{\sqrt{1+N_p}}$ or $\frac{1}{\sqrt{1+N_p}}$, then the optimization problem

is expressed as,

$$\begin{array}{l} \max E_I \\ s.t.[(\mathbf{p})_{i,1}]^2 = \frac{1}{1+N_p}, i = 0, 1, \ldots, N_p \end{array} \tag{4.27}$$

One suboptimal solution $\mathbf{p}_{b1}^*$ to the optimization problem (4.110) is derived from the optimal solution $\mathbf{p}^*$ of the optimization problem (4.20). When $\mathbf{p}^*$ is obtained, then

$$(\mathbf{p}_{b1}^*)_{i,1} = \begin{cases} \frac{1}{\sqrt{1+N_p}}, (\mathbf{p}^*)_{i,1} \geq 0 \\ -\frac{1}{\sqrt{1+N_p}}, (\mathbf{p}^*)_{i,1} < 0 \end{cases} \tag{4.28}$$

This simple method can lead to the optimal solution to the optimization problem (4.110) when $T_I \rightarrow 0$, which can be proofed by CauchySchwarz inequality, but if T_I is greater than zero, there is still a improvement potential to this suboptimal solution obtained from Eq. (4.28).

It is well known that the optimization problem (4.27) is Quadratically Constrained Quadratic Program (QCQP) and general QCQP is NP-hard, so a semidefinite relaxation method is proposed to give the suboptimal solution to this optimization problem.

Define,

$$\mathbf{P} = \mathbf{p}\mathbf{p}^T \tag{4.29}$$

$\mathbf{P}$ should be a symmetric positive semidefinite matrix, i.e. $\mathbf{P} \succ= 0$ and rank of $\mathbf{P}$ should be equal to 1. Reformulate E_I as,

$$\begin{aligned} E_I &= \mathbf{p}^T \mathbf{H}_I^T \mathbf{H}_I \mathbf{p} && (4.30) \\ &= \text{trace}\left(\mathbf{H}_I^T \mathbf{H}_I \mathbf{p}\mathbf{p}^T\right) && (4.31) \\ &= \text{trace}\left(\mathbf{H}_I^T \mathbf{H}_I \mathbf{P}\right) && (4.32) \end{aligned}$$

Rank constraint is nonconvex constraint, so after dropping it, QCQP is relaxed to the Semidefinite Program (SDP),

$$\begin{array}{l} \max \text{trace}\left(\mathbf{H}_I^T \mathbf{H}_I \mathbf{P}\right) \\ s.t. (\mathbf{P})_{i,i} = \frac{1}{1+N_p}, i = 0, 1, \ldots, N_p \\ \quad \mathbf{P} \succ= 0 \end{array} \tag{4.33}$$

The optimal solution $\mathbf{P}^*$ of the optimization problem (4.33) can be obtained by using CVX tool [35] and the value of the objective function in the optimizatiion problem (4.33) gives the upper bound of the optimal value in the optimization problem (4.27). Project the dominant eigen-vector of $\mathbf{P}^*$ on $-\frac{1}{\sqrt{1+N_p}}$ and $\frac{1}{\sqrt{1+N_p}}$ based on Eq. (4.28), the suboptimal solution $\mathbf{p}_{b2}^*$ is achieved [36].

Finally, the designed binary waveform is,

$$\mathbf{p}_b^* = \arg \max_{\mathbf{p} \in \{\mathbf{p}_{b1}^*, \mathbf{p}_{b2}^*\}} \mathbf{p}^T \mathbf{H}_I^T \mathbf{H}_I \mathbf{p} \tag{4.34}$$

Ternary Waveform

If the transmitted waveform is constrained to the ternary waveform, which means $p_i, i = 0, 1, \ldots, N_p$ is equal to three levels, i.e. $-c$, 0 or c, then the optimization problem is expressed as,

$$\begin{aligned} &\max E_I \\ &s.t.[(\mathbf{p})_{i,1}]^2 = c^2 \text{ or } 0, i = 0, 1, \ldots, N_p \\ &\quad \|\mathbf{p}\|_2^2 = 1 \end{aligned} \tag{4.35}$$

where the value of c will be determined later.

The optimization problem (4.35) is still NP-hard and can be approximately reformulated as,

$$\begin{aligned} &\max E_I \\ &s.t. \text{Cardinality}\,(\mathbf{p}) \leq k \\ &\quad 1 \leq k \leq N_p + 1 \quad \|\mathbf{p}\|_2^2 = 1 \end{aligned} \tag{4.36}$$

where $\text{Cardinality}\,(\mathbf{p})$ denotes the number of non-zero entries of $\mathbf{p}$ and cardinality constraint is also a nonconvex constraint.

Because k is the integer number between 1 and $N_p + 1$, the optimization problem (4.36) can be decomposed into $N_p + 1$ independent and parallel sub-problems and each sub-problem is shown as,

$$\begin{aligned} &\max E_I \\ &s.t. \text{Cardinality}\,(\mathbf{p}) \leq k \\ &\quad \|\mathbf{p}\|_2^2 = 1 \end{aligned} \tag{4.37}$$

where k is equal to 1, 2, $\cdots$, or $N_p + 1$;

The sub-problems (4.37) can be solved in parallel and then the solutions are combined to get the solution of the original optimization problem (4.35). Reuse the definition in Eq. (4.29) and the sub-problem (4.37) can converted to the following SDP by semidefinite relaxation combined with l1 heuristic [36],

$$\begin{aligned} &\max \text{trace}\left(\mathbf{H}_I^T \mathbf{H}_I \mathbf{P}\right) \\ &s.t. \text{trace}\,(\mathbf{P}) = 1 \\ &\quad \mathbf{a}^T |\mathbf{P}|\, \mathbf{a} \leq k \\ &\quad \mathbf{P} \succ= 0 \end{aligned} \tag{4.38}$$

where $\mathbf{a}$ is all-1 column vector and,

$$\|\mathbf{p}\|_2^2 = \mathbf{p}^T \mathbf{p} \tag{4.39}$$

$$= \text{trace}\left(\mathbf{p}\mathbf{p}^T\right) \tag{4.40}$$

$$= \text{trace}\,(\mathbf{P}) \tag{4.41}$$

The CVX tool [35] is also operated to get the optimal solution $\mathbf{P}_k^*$ of SDP (4.38). From the dominant eigen-vector $\mathbf{p}_k^*$ of $\mathbf{P}_k^*$ and the threshold p_{thk}, the solution for the sub-problem (4.37) can be achieved as,

$$(\mathbf{p}_{\text{tk}}^*)_{i,1} = \begin{cases} c_k, (\mathbf{p}_k^*)_{i,1} > p_{\text{thk}} \\ 0, \left|(\mathbf{p}_k^*)_{i,1}\right| \leq p_{\text{thk}} \\ -c_k, (\mathbf{p}_k^*)_{i,1} < p_{\text{thk}} \end{cases} \tag{4.42}$$

where

$$p_{\text{thk}} = \arg\max_{\{p_{\text{th}}\}} \left(\mathbf{p}_{\text{tk}}^*\right)^T \mathbf{H}_I^T \mathbf{H}_I \mathbf{p}_{\text{tk}}^* \quad s.t. \text{Cardinality}\left(\mathbf{p}_{\text{tk}}^*\right) \leq k \tag{4.43}$$

and

$$c_k = \frac{1}{\sqrt{\text{Cardinality}\left(\mathbf{p}_{\text{tk}}^*\right)}} \tag{4.44}$$

Finally, the designed ternary waveform is,

$$\mathbf{p}_t^* = \arg \max_{\mathbf{p} \in \left\{\mathbf{p}_{\text{tk}}^*, k=1,2,\ldots,N_p+1\right\}} \mathbf{p}^T \mathbf{H}_I^T \mathbf{H}_I \mathbf{p} \tag{4.45}$$

Sparse Waveform

Due to the sparse characteristics of channel impulse response or the implementation limitation, sometimes, the transmitted waveform should be sparse, which means within the waveform duration some of the waveform coefficients are zeros. In this way, the consumption of hardware resources will be greatly reduced. The optimization goal is to design sparse waveform with least number of non-zero waveform coefficients and with higher percentage of the received energy compared with the optimal waveform.

Generally, it is hard to get the optimal sparse waveform directly. However, exploiting iterative algorithm coming from the optimization problem (4.37) and its corresponding relaxation issue (4.38) can gives us the reasonable solutions.

The iterative algorithm is based on the loop of k from 1 to $N_p + 1$. For each k, the optimal waveform to the optimization problem (4.38) can be obtained. And then, the abstract values of the waveform coefficients are sorted from smallest one to the biggest one. We can set some of the smaller values to be zeros such that the energy of the remaining values is above some threshold, for example, 95 percent of total waveform energy. Accordingly, the sparse waveform for the certain k is achieved and the true sparsity of the waveform $\tilde{k}$ can also be gotten. Sometimes k is not equal to $\tilde{k}$. Finally, after the iterative algorithm is done, the relationship between the optimal energy and the sparsity is determined. Based on this relationship, we can choose the reasonable sparse waveform such that the energy loss in the receiver is tolerable.

Another phenomenon found by the simulation is that some of the waveform coefficients in the optimal waveform obtained from the optimization problem (4.38) is very small compared with other waveform coefficients. In this way, these small waveform coefficients can directly be set to zeros, which does not impact the system performance obviously.

Peak-to-Average Power Ratio

PAPR is one of major concerns in waveform design. Because of nonlincarity caused by nonlinear devices such as Digital-to-Analog Converter (DAC) and Power Amplifier (PA), maximal transmitted power has to be backed up, resulting in inefficient utilization. PAPR in OFDM has been well studied. PAPR is handled under a unified

optimization framework. It is defined as,

$$\mathrm{PAPR} = \frac{\|\mathbf{p}\|_\infty^2}{\|\mathbf{p}\|_2^2 \Big/ (N_p + 1)} \tag{4.46}$$

where

$$\|\mathbf{p}\|_\infty = \max\left(|p_0|, |p_1|, \cdots, |p_{N_p}|\right) \tag{4.47}$$

If $\|\mathbf{p}\|_2^2$ is given, reducing PAPR is equivalent to setting the upper bound for $\|\mathbf{p}\|_\infty$. So the optimization problem can be expressed as,

$$\begin{aligned} &\max E_I \\ &s.t. \|\mathbf{p}\|_2^2 = 1 \\ &\quad \|\mathbf{p}\|_\infty \leq \mathrm{ub} \end{aligned} \tag{4.48}$$

The bound constraint $\|\mathbf{p}\|_\infty \leq \mathrm{ub}$ can also be written as,

$$-\mathrm{ub} \leq p_i \leq \mathrm{ub}, i = 0, 1, \ldots, N_p \tag{4.49}$$

which can be further simplified as,

$$p_i^2 \leq (\mathrm{ub})^2, i = 0, 1, \ldots, N_p \tag{4.50}$$

Reuse the definition in Eq. (4.29), the optimization problem (4.46) can be relaxed to SDP,

$$\begin{aligned} &\max \mathrm{trace}\left(\mathbf{H}_I^T \mathbf{H}_I \mathbf{P}\right) \\ &s.t. \left(\mathbf{P}\right)_{i,i} \leq (\mathrm{ub})^2, i = 0, 1, \ldots, N_p \\ &\quad \mathrm{trace}\left(\mathbf{P}\right) = 1 \\ &\quad \mathbf{P} \succ= 0 \end{aligned} \tag{4.51}$$

By CVX tool [35], the optimal solution $\mathbf{P}^*$ of the optimization problem (4.51) is obtained. If the rank of $\mathbf{P}^*$ is equal to 1, then the dominant eigen-vector of $\mathbf{P}^*$ will be the optimal solution $\mathbf{p}^*$ for the optimization problem (4.48). But if the rank of $\mathbf{P}^*$ is not equal to 1, the dominant eigen-vector of $\mathbf{P}^*$ can not be treated as the optimal solution for the optimization problem (4.48), because of the violation of bound constraint.

So a computationally-efficient iterative algorithm is proposed to get the suboptimal solution $\mathbf{p}^*$ to the optimization problem (4.48) as follows.

1. Initialization: $P = 1$, $\mathbf{H}_0 = \mathbf{H}_I^T \mathbf{H}_I$ and $\mathbf{p}^*$ is set to be all-0 column vector.

2. Solve the following optimization problem to get the optimal $\mathbf{q}$.

$$\begin{aligned} &\max \mathbf{q}^T \mathbf{H}_0 \mathbf{q} \\ &s.t. \|\mathbf{q}\|_2^2 = P \end{aligned} \tag{4.52}$$

3. Find i, such that $|q_i|$ is the maximal value in the set $\{|q_j| \,||q_j| > \mathrm{ub}\}$. If $\{i\} = \emptyset$, then the algorithm is terminated and $\mathbf{p}^* := \mathbf{p}^* + \mathbf{q}$. Otherwise go to step 4.

4. If q_i is greater than zero, then $(\mathbf{p}^*)_{i,1}$ is set to be ub. Otherwise $(\mathbf{p}^*)_{i,1}$ is set to be $-\mathrm{ub}$.

5. $P := P - (\mathrm{ub})^2$ and set $(\mathbf{H}_0)_{i,j}, j = 1, 2, \ldots, N_p + 1$ and $(\mathbf{H}_0)_{j,i}, j = 1, 2, \ldots, N_p + 1$ all to zeros. Go to step 2.

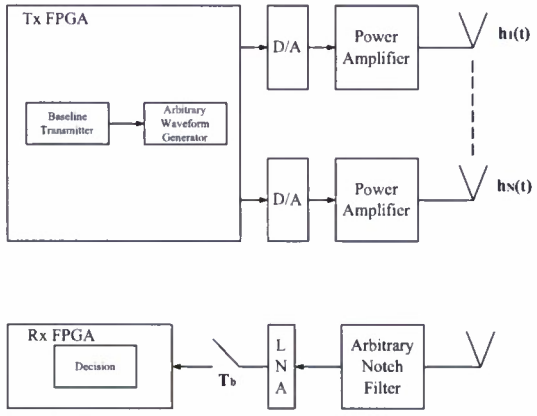


Figure 4.2: System architecture.

4.1.2 Wideband Waveform Optimization for Multiple Input Single Output Cognitive Radio with Practical Considerations

Wideband Waveform Optimization Using Cauchy–Schwarz Inequality-based Iterative Method

The system architecture considered in this document is shown in Figure 4.2. We limit our discussion to a single pair of cognitive radios scenario. There are N antennas at the transmitter and one antenna at the receiver. OOK modulation is used for transmission. Thus the transmitted signal at the transmitter antenna n is,

$$s_n(t) = \sum_{j=-\infty}^{\infty} d_j p_n(t - jT_b) \tag{4.53}$$

where T_b is the bit duration, $p_n(t)$ is the transmitted bit waveform defined over $[0, T_p]$ at the transmitter antenna n and $d_j \in \{0, 1\}$ is j-th transmitted bit. Without loss of gencrality, the minimal propagation delay is assumed to be zero. The energy of transmitted waveforms is E_p,

$$\sum_{n=1}^{N} \int_0^{T_p} p_n^2(t)\, df = E_p \tag{4.54}$$

The received noise-polluted signal at the output of low noise amplifier (LNA) is,

$$\begin{aligned} r(t) &= \sum_{n=1}^{N} h_n(t) \otimes s_n(t) + n(t) \\ &= \sum_{j=-\infty}^{\infty} d_j \sum_{n=1}^{N} x_n(t - jT_b) + n(t) \end{aligned} \tag{4.55}$$

where $h_n(t), t \in [0, T_h]$ is the multipath impulse response that takes into account the effect of channel impulse response, the RF front-ends in the transceivers such as power amplifier, LNA and arbitrary notch filter as well as

antennas between the transmitter antenna n and the receiver antenna. $h_n(t)$ is available at the transmitter [32] [33]. $\int_0^{T_h} h_n^2(t)\,dt = E_{nh}$. "$\otimes$" denotes convolution operation. $n(t)$ is AWGN. $x_n(t)$ is the received noiseless bit-"1" waveform defined as

$$x_n(t) = h_n(t) \otimes p_n(t) \tag{4.56}$$

We further assume that $T_b \geq T_h + T_p \overset{\text{def}}{=} T_x$, i.e. no existence of ISI.

If the waveforms at different transmitter antennas are assumed to be synchronized, the k-th decision statistic is,

$$\begin{aligned} r(kT_b + t_0) &= \sum_{j=-\infty}^{\infty} d_j \sum_{n=1}^{N} x_n\left(kT_b + t_0 - jT_b\right) + n\left(t\right) \\ &= d_k \sum_{n=1}^{N} x_n\left(t_0\right) + n\left(t\right) \end{aligned} \tag{4.57}$$

In order to maximize the system performance, $\sum_{n=1}^{N} x_n\left(t_0\right)$ should be maximized. Thus the optimization problem can be formulated as follows to get the optimal waveforms $p_n(t)$,

$$\begin{aligned} &\text{maximize } \sum_{n=1}^{N} x_n\left(t_0\right) \\ &\text{subject to} \\ &\sum_{n=1}^{N} \int_0^{T_p} p_n^2\left(t\right) dt \leq E_p \\ &0 \leq t_0 \leq T_b \end{aligned} \tag{4.58}$$

An iterative method is proposed here to give the optimal solution to the optimization problem (4.58). This method is a computationally efficient algorithm. For simplicity in the following presentation, t_0 is assumed to be zero, which will not degrade the optimum of the solution if such solution exists.

$$x\left(t\right) = \sum_{n=1}^{N} x_n\left(t\right) \tag{4.59}$$

From inverse Fourier transform,

$$x_{nf}\left(f\right) = h_{nf}\left(f\right) p_{nf}\left(f\right) \tag{4.60}$$

and

$$x_f\left(f\right) = \sum_{n=1}^{N} h_{nf}\left(f\right) p_{nf}\left(f\right) \tag{4.61}$$

where $x_{nf}\left(f\right)$, $h_{nf}\left(f\right)$ and $p_{nf}\left(f\right)$ are the frequency domain representations of $x_n(t)$, $h_n(t)$ and $p_n(t)$ respectively. $x_f(f)$ is frequency domain representation of $x(t)$. Thus,

$$x\left(0\right) = \sum_{n=1}^{N} x_n\left(0\right) \tag{4.62}$$

and,

$$x_n(0) = \int_{-\infty}^{\infty} x_{nf}(f)\, df \tag{4.63}$$

If there is no spectral mask constraint, then according to the Cauchy–Schwarz inequality,

$$\begin{aligned} x(0) &= \sum_{n=1}^{N} \int_{-\infty}^{\infty} h_{nf}(f)\, p_{nf}(f)\, df \\ &\leq \sum_{n=1}^{N} \sqrt{\int_{-\infty}^{\infty} |h_{nf}(f)|^2\, df \int_{-\infty}^{\infty} |p_{nf}(f)|^2\, df} \\ &\leq \sqrt{\sum_{n=1}^{N} \int_{-\infty}^{\infty} |h_{nf}(f)|^2\, df} \sqrt{\sum_{n=1}^{N} \int_{-\infty}^{\infty} |p_{nf}(f)|^2\, df} \\ &= \sqrt{E_p \sum_{n=1}^{N} E_{nh}} \end{aligned} \tag{4.64}$$

when $p_{nf}(f) = \alpha h_{nf}(f)$ for all f and n, two equalities are obtained.

$$\alpha = \sqrt{\frac{E_p}{\sum_{n=1}^{N} \int_{-\infty}^{\infty} |h_{nf}(f)|^2\, df}} \tag{4.65}$$

In this case, $p_n(t) = \alpha h_n(-t)$, which means the optimal waveform $p_n(t)$ is the corresponding time reversed multipath impulse response $h_n(t)$.

If there is spectral mask constraint, then the following optimization problem will become more complicated,

$$\begin{aligned} &\text{maximize } x(0) \\ &\text{subject to} \\ &\sum_{n=1}^{N} \int_0^{T_p} p_n^2(t)\, dt \leq E_p \\ &|p_{nf}(f)|^2 \leq c_{nf}(f) \end{aligned} \tag{4.66}$$

where $c_{nf}(f)$ represents the arbitrary spectral mask constraint at the transmitter antenna n.

Because $p_{nf}(f)$ is the complex value, the phase and the modulus of $p_{nf}(f)$ should be determined.

Meanwhile,

$$x(0) = \int_{-\infty}^{\infty} x_f(f)\, df \tag{4.67}$$

and,

$$x_f(f) = \sum_{n=1}^{N} |h_{nf}(f)|\, |p_{nf}(f)|\, e^{j2\pi\left(\arg\left(h_{nf}(f)\right)+\arg\left(p_{nf}(f)\right)\right)} \tag{4.68}$$

where the angular component of the complex value is $\arg(\bullet)$.

For the real value signal $x(t)$,

$$x_f(f) = x_f^*(-f) \tag{4.69}$$

where "$*$" denotes conjugate operation. Thus,

$$x_f(-f) = \sum_{n=1}^{N} |h_{nf}(f)|\,|p_{nf}(f)|\, e^{-j2\pi\left(\arg\left(h_{nf}(f)\right)+\arg\left(p_{nf}(f)\right)\right)} \tag{4.70}$$

and $x_f(f) + x_f(-f)$ is equal to

$$\sum_{n=1}^{N} |h_{nf}(f)|\,|p_{nf}(f)| \cos(2\pi\left(\arg\left(h_{nf}(f)\right) + \arg\left(p_{nf}(f)\right)\right)) \tag{4.71}$$

If $h_{nf}(f)$ and $|p_{nf}(f)|$ are given for all f and n, maximization of $x(0)$ is equivalent to,

$$\arg\left(h_{nf}(f)\right) + \arg\left(p_{nf}(f)\right) = 0 \tag{4.72}$$

which means the angular component of $p_{nf}(f)$ is the negative angular component of $h_{nf}(f)$.

The optimization problem (4.66) can be simplified as,

$$\begin{array}{l} \text{maximize } \sum\limits_{n=1}^{N} \int_{-\infty}^{\infty} |h_{nf}(f)|\,|p_{nf}(f)|\,df \\ \text{subject to} \\ \sum\limits_{n=1}^{N} \int_{-\infty}^{\infty} |p_{nf}(f)|^2\,df \le E_p \\ |p_{nf}(f)|^2 \le c_{nf}(f) \end{array} \tag{4.73}$$

Because,

$$|h_{nf}(f)| = |h_{nf}(-f)| \tag{4.74}$$

$$|p_{nf}(f)| = |p_{nf}(-f)| \tag{4.75}$$

$$|c_{nf}(f)| = |c_{nf}(-f)| \tag{4.76}$$

for all f and n. Thus uniformly discrete frequency points $f_0, \ldots, f_M$ are considered in the optimization problem (4.73). Meanwhile, f_0 corresponds to the DC component and $f_1, \ldots, f_M$ correspond to the positive frequency components.

Define column vectors $\mathbf{h}_f, \mathbf{h}_{1f}, \ldots, \mathbf{h}_{Nf}$,

$$\mathbf{h}_f = [\mathbf{h}_{1f}^T\ \mathbf{h}_{2f}^T\ \cdots\ \mathbf{h}_{Nf}^T]^T \tag{4.77}$$

$$(\mathbf{h}_{nf})_i = \begin{cases} |h_{nf}(f_{i-1})|, i = 1 \\ \sqrt{2}\,|h_{nf}(f_{i-1})|, i = 2, \ldots, M+1 \end{cases} \tag{4.78}$$

where "T" denotes transpose operation.

Define column vectors $\mathbf{p}_f, \mathbf{p}_{1f}, \ldots, \mathbf{p}_{Nf}$,

$$\mathbf{p}_f = [\mathbf{p}_{1f}^T\ \mathbf{p}_{2f}^T\ \cdots\ \mathbf{p}_{Nf}^T]^T \tag{4.79}$$

$$(\mathbf{p}_{nf})_i = \begin{cases} |p_{nf}(f_{i-1})|, i = 1 \\ \sqrt{2}\,|p_{nf}(f_{i-1})|, i = 2, \ldots, M+1 \end{cases} \tag{4.80}$$

Define column vectors $\mathbf{c}_f$, $\mathbf{c}_{1f}$, ..., $\mathbf{c}_{Nf}$,

$$\mathbf{c}_f = [\mathbf{c}_{1f}^T\ \mathbf{c}_{2f}^T\ \cdots\ \mathbf{c}_{Nf}^T]^T \tag{4.81}$$

$$(\mathbf{c}_{nf})_i = \begin{cases} \sqrt{|c_{nf}(f_{i-1})|}, i = 1 \\ \sqrt{2\,|c_{nf}(f_{i-1})|}, i = 2, \ldots, M+1 \end{cases} \tag{4.82}$$

Thus, the discrete version of the optimization problem (4.73) is shown below,

$$\begin{array}{l} \text{maximize } \mathbf{h}_f^T \mathbf{p}_f \\ \text{subject to} \\ \|\mathbf{p}_f\|_2^2 \le E_p \\ 0 \le \mathbf{p}_f \le \mathbf{c}_f \end{array} \tag{4.83}$$

An iterative algorithm (Algorithm I) is shown as follows to give the optimal solution $\mathbf{p}_f^*$ to the optimization problem (4.83), which was proposed in [37] and is extended to waveform design in the context of MISO cognitive radio:

1. Initialization: $P = E_p$ and $\mathbf{p}_f^*$ is set to be all-0 column vector.

2. Solve the following optimization problem to get the optimal $\mathbf{q}_f^*$ using Cauchy−Schwarz inequality.

$$\begin{array}{l} \text{maximize } \mathbf{h}_f^T \mathbf{q}_f \\ \text{subject to} \\ \|\mathbf{q}_f\|_2^2 \le P \end{array} \tag{4.84}$$

3. Find i, such that $\left(\mathbf{q}_f^*\right)_i$ is the maximal value in the set $\left\{ \left(\mathbf{q}_f^*\right)_j \middle| \left(\mathbf{q}_f^*\right)_j > (\mathbf{c}_f)_j \right\}$. If $\{i\} = \emptyset$, then the method is terminated and $\mathbf{p}_f^* := \mathbf{p}_f^* + \mathbf{q}_f^*$. Otherwise go to step 4.

4. Set $\left(\mathbf{p}_f^*\right)_i = (\mathbf{c}_f)_i$.

5. $P := P - (\mathbf{c}_f)_i^2$ and set $(\mathbf{h}_f)_i$ to zero. If $\|\mathbf{h}_f\|_2^2$ is equal to zero, then the algorithm is terminated; otherwise go to step 2.

When $\mathbf{p}_f^*$ is obtained for the optimization problem (4.83), from Eq. (4.72), Eq. (4.79) and Eq. (4.80), the optimal $p_{nf}(f)$ and the corresponding $p_n(t)$ can be smoothly achieved.

Wideband Waveform Optimization Using SDP-Based Iterative method

The $p_n(t)$ and the $h_n(t)$ are uniformly sampled at Nyquist rate. Assume the sampling period is T_s. $T_p/T_s = N_p$ and N_p is assumed to be even, $T_h/T_s = N_h$. $p_n(t)$ and $h_n(t)$ are represented by $p_{ni}, i = 0, 1, \ldots, N_p$ and $h_{ni}, i = 0, 1, \ldots, N_h$ respectively.

Define,

$$\mathbf{p}_n = [p_{n0}\ p_{n1}\ \cdots\ p_{nN_p}]^T \tag{4.85}$$

and

$$\mathbf{h}_n = [h_{nN_h}\ h_{n(N_h-1)}\ \cdots\ h_{n0}]^T \tag{4.86}$$

If $N_p = N_h$, then $\sum_{n=1}^{N} x_n(t_0)$ can be equivalent to $\sum_{n=1}^{N} \mathbf{h}_n^T \mathbf{p}_n$. Define,

$$\mathbf{p} = [\mathbf{p}_1^T\ \mathbf{p}_2^T\ \cdots\ \mathbf{p}_N^T]^T \tag{4.87}$$

and

$$\mathbf{h} = [\mathbf{h}_1^T\ \mathbf{h}_2^T\ \cdots\ \mathbf{h}_N^T]^T \tag{4.88}$$

Thus,

$$\sum_{n=1}^{N} \mathbf{h}_n^T \mathbf{p}_n = \mathbf{h}^T \mathbf{p} \tag{4.89}$$

Maximization of $\mathbf{h}^T\mathbf{p}$ is the same as maximization of $(\mathbf{h}^T\mathbf{p})^2$ as long as $\mathbf{h}^T\mathbf{p}$ is equal to or greater than zero.

$$\begin{aligned} (\mathbf{h}^T\mathbf{p})^2 &= (\mathbf{h}^T\mathbf{p})^T (\mathbf{h}^T\mathbf{p}) \\ &= \mathbf{p}^T\mathbf{h}\mathbf{h}^T\mathbf{p} \\ &= \text{trace}\,(\mathbf{h}\mathbf{h}^T\mathbf{p}\mathbf{p}^T) \\ &= \text{trace}\,(\mathbf{H}\mathbf{P}) \end{aligned} \tag{4.90}$$

where $\mathbf{H} = \mathbf{h}\mathbf{h}^T$ and $\mathbf{P} = \mathbf{p}\mathbf{p}^T$. $\mathbf{P}$ should be rank-1 positive semidefinite matrix. However, rank constraint is non-convex constraint, which will be omitted in the following optimization problems. Thus the optimization objective in the optimization problem (4.66) can be reformulated as,

$$\text{maximize trace}\,(\mathbf{H}\mathbf{P}) \tag{4.91}$$

Meanwhile,

$$\begin{aligned} \|\mathbf{p}\|_2^2 &= \mathbf{p}^T\mathbf{p} \\ &= \text{trace}\,(\mathbf{p}\mathbf{p}^T) \\ &= \text{trace}\,(\mathbf{P}) \end{aligned} \tag{4.92}$$

Thus the energy constraint in the optimization problem (4.66) can be reformulated as,

$$\text{trace}\,(\mathbf{P}) \leq E_p \tag{4.93}$$

For cognitive radio, there is a spectral mask constraint for the transmitted waveform. Based on the previous discussion, $\mathbf{p}_n$ is assumed to be the transmitted waveform, and $\mathbf{F}$ is the discrete-time Fourier transform operator, thus the frequency domain representation of $\mathbf{p}_n$ is,

$$\mathbf{p}_{fn} = \mathbf{F}\mathbf{p}_n \tag{4.94}$$

where $\mathbf{p}_{fn}$ is a complex value vector. If the i-th row of $\mathbf{F}$ is $\mathbf{f}_i$, then each complex value in $\mathbf{p}_{fn}$ can be represented by,

$$(\mathbf{p}_{fn})_{i,1} = \mathbf{f}_i\mathbf{p}_n, i = 1, 2, \ldots, \frac{N_p}{2} + 1 \tag{4.95}$$

Define,

$$\mathbf{F}_i = \mathbf{f}_i^H \mathbf{f}_i, i = 1, 2, \ldots, \frac{N_p}{2} + 1 \tag{4.96}$$

Given the spectral mask constraint in terms of power spectral density $\mathbf{c}_n = \left[c_{n1}\, c_{n2} \cdots c_{n\frac{N_p}{2}+1}\right]^T$, so

$$\begin{aligned} \left|(\mathbf{p}_{fn})_{i,1}\right|^2 &= |\mathbf{f}_i \mathbf{p}_n|^2 \\ &= \mathbf{p}_n^T \mathbf{f}_i^H \mathbf{f}_i \mathbf{p}_n \\ &= \mathbf{p}_n^T \mathbf{F}_i \mathbf{p}_n \\ &\leq c_{ni}, i = 1, 2, \ldots, \frac{N_p}{2} + 1 \end{aligned} \tag{4.97}$$

where $|\bullet|$ is the modulus of the complex value.

Define selection matrix $\mathbf{S}_n \in R^{(N_p+1)\times(N_p+1)N}$,

$$(\mathbf{S}_n)_{i,j} = \begin{cases} 1, & j = i + (N_p + 1)(n-1) \\ 0, & \text{else} \end{cases} \tag{4.98}$$

So,

$$\mathbf{p}_n = \mathbf{S}_n \mathbf{p} \tag{4.99}$$

and

$$\begin{aligned} \left|(\mathbf{p}_{fn})_{i,1}\right|^2 &= \mathbf{p}_n^T \mathbf{F}_i \mathbf{p}_n \\ &= \mathbf{p}^T \mathbf{S}_n^T \mathbf{F}_i \mathbf{S}_n \mathbf{p} \\ &= \text{trace}\left(\mathbf{S}_n^T \mathbf{F}_i \mathbf{S}_n \mathbf{p}\mathbf{p}^T\right) \\ &= \text{trace}\left(\mathbf{S}_n^T \mathbf{F}_i \mathbf{S}_n \mathbf{P}\right) \end{aligned} \tag{4.100}$$

The optimization problem (4.66) can be reformulated as SDP based on (4.91), (4.93), (4.97) and (4.100),

$$\begin{aligned} &\text{maximize trace}\,(\mathbf{HP}) \\ &\text{subject to} \\ &\text{trace}\,(\mathbf{P}) \leq E_p \\ &\text{trace}\left(\mathbf{S}_n^T \mathbf{F}_i \mathbf{S}_n \mathbf{P}\right) \leq c_{ni} \\ &i = 1, 2, \ldots, \tfrac{N_p+1}{2} \\ &n = 1, 2, \ldots N \end{aligned} \tag{4.101}$$

If the optimal solution $\mathbf{P}^*$ to the optimization problem (4.101) is the rank-1 matrix, then the optimal waveforms can be obtained from the dominant eigen-vector of $\mathbf{P}^*$. Otherwise, E_p in the optimization problem (4.101) should be decreased to get the rank-1 optimal solution $\mathbf{P}^*$ to satisfy all the other constraints.

An SDP-based iterative algorithm (Algorithm II) is proposed to get the rank-1 optimal solution $\mathbf{P}^*$:

1. Initialization of E_p.

2. Solve the optimization problem (4.101) and get the optimal solution $\mathbf{P}^*$.

3. If the ratio of dominant eigen-value of $\mathbf{P}^*$ to $\mathrm{trace}(\mathbf{P}^*)$ is less than 0.99, then set E_p to be $\mathrm{trace}(\mathbf{P}^*)$ and go to step 2; otherwise, the algorithm is terminated.

The optimal waveforms can be obtained from the dominant eigen-vector of $\mathbf{P}^*$ and Eq. (4.87).

Peak-to-Average Power Ratio

PAPR is one of major concerns in waveform design. Because of nonlinearity caused by nonlinear devices such as Digital-to-Analog Converter (DAC) and Power Amplifier (PA), maximal transmitted power has to be backed up, resulting in inefficient utilization. PAPR in OFDM has been well studied. PAPR is handled under a unified optimization framework. It is defined as,

$$\mathrm{PAPR} = \frac{\|\mathbf{p}_n\|_\infty^2}{\|\mathbf{p}_n\|_2^2 \big/ (N_p+1)} \tag{4.102}$$

where

$$\|\mathbf{p}_n\|_\infty = \max\left(|p_{n0}|, |p_{n1}|, \cdots, |p_{nN_p}|\right) \tag{4.103}$$

If the denominator of Eq. (4.102) is omitted, reducing PAPR is equivalent to setting the upper bound for $\|\mathbf{p}_n\|_\infty$. The bound constraint $\|\mathbf{p}_n\|_\infty \leq \mathrm{b}_n$ can also be written as,

$$-\mathrm{b}_n \leq p_{ni} \leq \mathrm{b}_n, i = 0, 1, \ldots, N_p \tag{4.104}$$

which can be further simplified as,

$$p_{ni}^2 \leq (\mathrm{b}_n)^2, i = 0, 1, \ldots, N_p \tag{4.105}$$

Define selection vector $\mathbf{s}_{ni} \in R^{1\times(N_p+1)N}$,

$$(\mathbf{s}_{ni})_{1,j} = \begin{cases} 1, & j = i + (N_p+1)(n-1) \\ 0, & \text{else} \end{cases} \tag{4.106}$$

So,

$$\mathbf{p}_{ni} = \mathbf{s}_{ni}\mathbf{p} \tag{4.107}$$

and

$$\begin{aligned} p_{ni}^2 &= \mathbf{p}_{ni}^2 \\ &= (\mathbf{s}_{ni}\mathbf{p})^2 \\ &= (\mathbf{s}_{ni}\mathbf{p})^T (\mathbf{s}_{ni}\mathbf{p}) \\ &= \mathbf{p}^T \mathbf{s}_{ni}^T \mathbf{s}_{ni}\mathbf{p} \\ &= \mathrm{trace}\left(\mathbf{s}_{ni}^T \mathbf{s}_{ni}\mathbf{p}\mathbf{p}^T\right) \\ &= \mathrm{trace}\left(\mathbf{s}_{ni}^T \mathbf{s}_{ni}\mathbf{P}\right) \end{aligned} \tag{4.108}$$

The optimization problem (4.66) or the optimization problem (4.101) together with PAPR consideration can be presented as SDP,

$$\begin{array}{l} \text{maximize trace}\,(\mathbf{HP}) \\ \text{subject to} \\ \text{trace}\,(\mathbf{P}) \leq E_p \\ \text{trace}\left(\mathbf{S}_n^T \mathbf{F}_i \mathbf{S}_n \mathbf{P}\right) \leq \mathrm{c}_{ni} \\ \text{trace}\left(\mathbf{s}_{ni}^T \mathbf{s}_{ni} \mathbf{P}\right) \leq \mathrm{b}_{\mathrm{n}} \\ i = 1, 2, \ldots, \frac{N_p+1}{2} \\ n = 1, 2, \ldots N \end{array} \tag{4.109}$$

Similarly, if the optimal solution $\mathbf{P}^*$ to the optimization problem (4.109) is the rank-1 matrix, then the optimal waveforms can be obtained from the dominant eigen-vector of $\mathbf{P}^*$. Otherwise, E_p in the optimization problem (4.109) should be decreased to get the rank-1 optimal solution $\mathbf{P}^*$ to satisfy all the other constraints.

An SDP-based iterative algorithm (Algorithm III) is proposed to get the rank-1 optimal solution $\mathbf{P}^*$:

1. Initialization of E_p.

2. Solve the optimization problem (4.109) and get the optimal solution $\mathbf{P}^*$.

3. If the ratio of dominant eigen-value of $\mathbf{P}^*$ to $\text{trace}\,(\mathbf{P}^*)$ is less than 0.99, then set E_p to be $\text{trace}\,(\mathbf{P}^*)$ and go to step 2; otherwise, the algorithm is terminated.

The optimal waveforms can be obtained from the dominant eigen-vector of $\mathbf{P}^*$ and Eq. (4.87).

Binary Waveform

If the transmitted waveform is constrained to the binary waveform because of the hardware limitation or implementation simplicity, or equivalently if $p_{ni}^2 = \frac{E_p}{(N_p+1)N}$, then The optimization problem (4.66) or the optimization problem (4.101) together with binary waveform design can be formulated as SDP,

$$\begin{array}{l} \text{maximize trace}\,(\mathbf{HP}) \\ \text{subject to} \\ \text{trace}\,(\mathbf{P}) == E_p \\ \text{trace}\left(\mathbf{S}_n^T \mathbf{F}_i \mathbf{S}_n \mathbf{P}\right) \leq \mathrm{c}_{ni} \\ \text{trace}\left(\mathbf{s}_{ni}^T \mathbf{s}_{ni} \mathbf{P}\right) == \frac{E_p}{(N_p+1)N} \\ i = 1, 2, \ldots, \frac{N_p+1}{2} \\ n = 1, 2, \ldots N \end{array} \tag{4.110}$$

However, the constraints $\text{trace}\,(\mathbf{P}) == E_p$ and $\text{trace}\left(\mathbf{s}_{ni}^T \mathbf{s}_{ni} \mathbf{P}\right) == \frac{E_p}{(N_p+1)N}$ usually bring non-rank-1 optimal solution $\mathbf{P}^*$ or invalid solution, i.e. no feasible region for the optimization problem because of the constraints, to the optimization problem (4.110). Thus the equality constraints are relaxed to the inequality constraints and the

optimization problem (4.110) is relaxed to,

$$\begin{aligned} &\text{maximize trace}\,(\mathbf{HP}) \\ &\text{subject to} \\ &\text{trace}\,(\mathbf{P}) \leq E_p \\ &\text{trace}\left(\mathbf{S}_n^T\mathbf{F}_i\mathbf{S}_n\mathbf{P}\right) \leq c_{ni} \\ &\text{trace}\left(\mathbf{s}_{ni}^T\mathbf{s}_{ni}\mathbf{P}\right) \leq \frac{E_p}{(N_p+1)N} \\ &i = 1, 2, \ldots, \frac{N_p+1}{2} \\ &n = 1, 2, \ldots N \end{aligned} \tag{4.111}$$

However, such relaxation forces us to verify the feasibility of the optimal solution $\mathbf{P}^*$ to the optimization problem (4.111). If the dominant eigen-value of $\mathbf{P}^*$ is the same as E_p, which means trace $\left(\mathbf{s}_{ni}^T\mathbf{s}_{ni}\mathbf{P}\right)$ is equal to $\frac{E_p}{(N_p+1)N}$ for all i and n, then the optimal solution $\mathbf{P}^*$ is feasible and the optimal binary waveforms can be obtained from the dominant eigen-vector of $\mathbf{P}^*$ and the dominant eigen-value of $\mathbf{P}^*$. Otherwise, E_p in the optimization problem (4.111) should be decreased.

An SDP-based iterative algorithm (Algorithm IV) is proposed to get the rank-1 optimal solution $\mathbf{P}^*$:

1. Initialization of E_p.

2. Solve the optimization problem (4.111) and get the optimal solution $\mathbf{P}^*$.

3. If the ratio of dominant eigen-value of $\mathbf{P}^*$ to E_p is less than 0.9999, then set E_p to be trace $(\mathbf{P}^*)$ and go to step 2; otherwise, the algorithm is terminated.

The optimal waveforms can be obtained from the dominant eigen-vector of $\mathbf{P}^*$ and Eq. (4.87).

Robust Waveform

For the practical consideration of uncertainty, multipath impulse responses can not be obtained exactly due to the limitation of sounding system and feedback system or the perturbation of the radio environment and the fading of radio channel. The norm of uncertainty for each multipath impulse response is assumed to be bounded by the known value.

$$\mathbf{h}_n = \mathbf{h}_n^0 + \Delta\mathbf{h}_n \tag{4.112}$$

and

$$\|\Delta\mathbf{h}_n\|_2 \leq \varepsilon_n \tag{4.113}$$

where $\mathbf{h}_n^0$ is the nominal value of multipath impulse response, $\Delta\mathbf{h}_n$ is the uncertainty of multipath impulse response and ε_n is the norm bounded value for uncertainty.

Based on Eq. (4.88), Eq. (4.112) and Eq. (4.113), $\mathbf{h}$ can be reformulated as,

$$\mathbf{h} = \mathbf{h}^0 + \Delta\mathbf{h} \tag{4.114}$$

where,

$$\mathbf{h}^0 = \left[\left(\mathbf{h}_1^0\right)^T \cdots \left(\mathbf{h}_N^0\right)^T\right]^T \tag{4.115}$$

and

$$\Delta\mathbf{h} = \left[(\Delta\mathbf{h}_1)^T \cdots (\Delta\mathbf{h}_N)^T\right]^T \tag{4.116}$$

The norm of $\Delta\mathbf{h}$ is

$$\|\Delta\mathbf{h}\|_2^2 = \sum_{n=1}^{N} \|\Delta\mathbf{h}_n\|_2^2 \leq \sum_{n=1}^{N} \varepsilon_n^2 = \varepsilon^2 \tag{4.117}$$

From Eq. (4.89), maximization of $\mathbf{h}^T\mathbf{p}$ is the same as maximization of $\left|\mathbf{h}^T\mathbf{p}\right|$ as long as $\mathbf{h}^T\mathbf{p}$ is equal to or greater than zero. Based on the triangle inequality [38] [39],

$$\begin{aligned} \left|\mathbf{h}^T\mathbf{p}\right| &= \left|\left(\mathbf{h}^0 + \Delta\mathbf{h}\right)^T\mathbf{p}\right| && (4.118)\\ &= \left|\left(\mathbf{h}^0\right)^T\mathbf{p} + \Delta\mathbf{h}^T\mathbf{p}\right| && (4.119)\\ &\geq \left|\left(\mathbf{h}^0\right)^T\mathbf{p}\right| - \left|\Delta\mathbf{h}^T\mathbf{p}\right| && (4.120) \end{aligned}$$

Meanwhile, according to Cauchy–Schwarz inequality,

$$\left|\Delta\mathbf{h}^T\mathbf{p}\right| \leq \|\Delta\mathbf{h}\|_2 \|\mathbf{p}\|_2 = \varepsilon \|\mathbf{p}\|_2 \tag{4.121}$$

Hence,

$$\left|\mathbf{h}^T\mathbf{p}\right| \geq \left|\left(\mathbf{h}^0\right)^T\mathbf{p}\right| - \varepsilon \|\mathbf{p}\|_2 \tag{4.122}$$

and if the uncertainty is small compared with the nominal value of multipath impulse response, i.e,

$$\left|\left(\mathbf{h}^0\right)^T\mathbf{p}\right| - \varepsilon \|\mathbf{p}\|_2 \geq 0 \tag{4.123}$$

then

$$\begin{aligned} \left|\mathbf{h}^T\mathbf{p}\right|^2 &\geq \left(\left|\left(\mathbf{h}^0\right)^T\mathbf{p}\right| - \varepsilon \|\mathbf{p}\|_2\right)^2 && (4.124)\\ &= \left|\left(\mathbf{h}^0\right)^T\mathbf{p}\right|^2 - 2\varepsilon\left|\left(\mathbf{h}^0\right)^T\mathbf{p}\right| \|\mathbf{p}\|_2 + \varepsilon^2 \|\mathbf{p}\|_2^2 && (4.125)\\ &\geq \left|\left(\mathbf{h}^0\right)^T\mathbf{p}\right|^2 - 2\varepsilon \left\|\mathbf{h}^0\right\|_2 \|\mathbf{p}\|_2^2 + \varepsilon^2 \|\mathbf{p}\|_2^2 && (4.126) \end{aligned}$$

Define $\mathbf{H}^0 = \mathbf{h}^0\left(\mathbf{h}^0\right)^T$ and reuse $\mathbf{P} = \mathbf{p}\mathbf{p}^T$, $\left|\mathbf{h}^T\mathbf{p}\right|^2$ can be further relaxed as,

$$\begin{aligned} \left|\mathbf{h}^T\mathbf{p}\right|^2 &\geq \operatorname{trace}\left(\mathbf{H}^0\mathbf{P}\right) - 2\varepsilon \left\|\mathbf{h}^0\right\|_2 \operatorname{trace}\left(\mathbf{P}\right) + \varepsilon^2 \operatorname{trace}\left(\mathbf{P}\right) && (4.127)\\ &= \operatorname{trace}\left(\tilde{\mathbf{H}}\mathbf{P}\right) && (4.128) \end{aligned}$$

where,

$$\tilde{\mathbf{H}} = \mathbf{H}^0 + \left(\varepsilon^2 - 2\varepsilon \left\|\mathbf{h}^0\right\|_2\right)\mathbf{I} \tag{4.129}$$

Thus,

$$\min_{\|\Delta\mathbf{h}\|_2 \leq \varepsilon} \left|\mathbf{h}^T\mathbf{p}\right|^2 = \operatorname{trace}\left(\tilde{\mathbf{H}}\mathbf{P}\right) \tag{4.130}$$

For robust optimization, the worst-case performance should be guaranteed and the worse-case constraint should be beat. The optimizaton problem for robust waveform design can be formulated as SDP,

$$\begin{aligned} &\text{minimize trace}\,(\mathbf{P}) \\ &\text{subject to} \\ &\text{trace}\left(\tilde{\mathbf{H}}\mathbf{P}\right) \geq \delta \\ &\text{trace}\left(\mathbf{S}_n^T\mathbf{F}_i\mathbf{S}_n\mathbf{P}\right) \leq c_{ni} \\ &i = 1, 2, \ldots \frac{N_p+1}{2} \\ &n = 1, 2 \ldots, N \end{aligned} \tag{4.131}$$

where δ minimum peak energy needed for the receiver to meet QoS. If there is a rank-1 optimal solution $\mathbf{P}^*$ to the optimization problem (4.131), then the optimal waveforms can be obtained from the dominant eigen-vector of $\mathbf{P}^*$ and Eq. (4.87); otherwise, there is no solution to the robust waveform design problem.

Multi-User Waveform

Multi-user scenario will be more complex than previous single user scenario. In multi-user scenario, there is one transmitter with multiple antennas and there is more than one receiver. Each receiver with single antenna represents one user. These users are distributed and have no cooperation at the receiver side. Meanwhile, all the receivers are assumed to be synchronized to the transmitter. The transmitter will serve all the receivers based on the type of services. The transmitter is assumed to know all the multipath impulse responses between transmitter and receivers. Thus the joint waveform design and optimization will be performed at the transmitter side.

Assume there are M users in the multi-user scenario. The type of service is multi-cast, which means the same information will be sent to all the users simultaneously and equally. If bit 1 is sent, then all the users will receive 1. If bit 0 is sent, then all the users will receive 0. Extended from Eq. (4.90), $\mathbf{H}_m$ will contain the information on multipath impulse response for user m. The optimization problem for the multi-cast service can be formulated as SDP,

$$\begin{aligned} &\text{minimize trace}\,(\mathbf{P}) \\ &\text{subject to} \\ &\text{trace}\,(\mathbf{H}_m\mathbf{P}) \geq \delta_m \\ &m = 1, 2, \ldots, M \\ &\text{trace}\left(\mathbf{S}_n^T\mathbf{F}_i\mathbf{S}_n\mathbf{P}\right) \leq c_{ni} \\ &i = 1, 2, \ldots \frac{N_p+1}{2} \\ &n = 1, 2 \ldots, N \end{aligned} \tag{4.132}$$

where δ_m is the minimum peak energy needed for user m to meet its QoS.

If the optimization problem (4.132) can be solved with rank-1 optimal solution $\mathbf{P}^*$, then the optimal waveforms with minimum transmitted power can be obtained. Otherwise, there is no solution to the multi-cast service and all the users can not be served simultaneously and satisfactorily. Thus user selection should be performed to select part of users to be served. The goal of user selection is to maximize the number of users whose QoS is met. If the number of users in the scenario is small and limited, exhaustive search can be exploited to choose the users. However if the number of users is large, the computation of exhaustive search is prohibitive. Generally, the greedy kind of algorithms can be used to do user selection practically.

The algorithms on user selection or admission control were discussed in [40] [41]. A greedy deflation approach, i.e.

adding user, and a greed inflation approach, i.e. deleting user, were mentioned. Similarly an inflation based greedy algorithm is proposed here to perform user selection:

1. Set $G_{\text{serve}} = \emptyset$ and $G_{\text{init}} = \{1, 2, \ldots, M\}$.

2. Choose $i \in G_{\text{init}}$, formulate $G_i = G_{\text{serve}} \cup \{i\}$ and solve the optimization problem (4.132). If there is a rank-1 optimal solution $\mathbf{P}^*$, then $p_i = \text{trace}(\mathbf{P}^*)$; otherwise $p_i = +\infty$.

3. $i^* = \arg\min\{p_i\}$ and $p_i^* = \min\{p_i\}$. If p_i^* is equal to $+\infty$, then the algorithm is terminated; otherwise, $G_{\text{serve}} = G_i$ and remove i from G_{init}. If $G_{\text{init}} = \emptyset$, then the algorithm is terminated; otherwise go to step 2.

If the type of service is uni-cast, different information will be sent to different users simultaneously. For example, on the current bit duration, bit 1 is sent to user 1 and bit 0 is sent to user 2. All the users can be divided into two groups. Users in the first group G_1 will receive bit 1 and the corresponding peak energys should be equal to or greater than the pre-defined thresholds for bit 1. While users in the second group G_2 will receive bit 0 and the corresponding peak energys should be equal to or less than the lower thresholds for bit 0. G_1 and G_2 are the sets, which contains the indices of users in the first group and second group respectively. $G_1 + G_2 = \{1, 2, \ldots, M\}$ The optimization problem for the uni-cast service can be formulated as SDP,

$$\begin{array}{l} \text{minimize trace}(\mathbf{P}) \\ \text{subject to} \\ \text{trace}(\mathbf{H}_{m_1}\mathbf{P}) \geq \delta_{m_1} \\ m_1 \in G_1 \\ \text{trace}(\mathbf{H}_{m_2}\mathbf{P}) \leq \delta_{m_2} \\ m_2 \in G_2 \\ \text{trace}\left(\mathbf{S}_n^T\mathbf{F}_i\mathbf{S}_n\mathbf{P}\right) \leq c_{ni} \\ i = 1, 2, \ldots \frac{N_p+1}{2} \\ n = 1, 2 \ldots, N \end{array} \tag{4.133}$$

where δ_{m_1} is the minimum peak energy needed for user m_1 to receive bit 1 and δ_{m_2} is the maximum peak energy needed for user m_2 to receive bit 0.

If the optimization problem (4.133) can be solved with rank-1 optimal solution $\mathbf{P}^*$, then the optimal waveforms with minimum transmitted power can be obtained. Otherwise, there is no solution to the uni-cast service and all the users can not be served simultaneously and satisfactorily. User selection for uni-cast service is more complex than that for multi-cast service. The latter can be done once for all. While the former need be done for each bit duration separately due to the dynamic change of G_1 and G_2. If so, the connectivity of selected user can not be guaranteed. For example, one user is served on the current bit duration and may be kicked out for the next bit duration. Taking connectivity into account, user selection for uni-cast service should also be performed once for all. Once a user is selected, this user will be served to end. Meanwhile, the combination of G_1 and g_2 is huge in terms of the number of users. Thus the complexity of user selection algorithm should be well controlled. A deflation based greedy algorithm is proposed here to perform user selection:

1. Set $G_{\text{serve}} = \{1, 2, \ldots, M\}$.

2. Randomly choose G_1 and G_2 such that $G_1 + G_2 = G_{\text{serve}}$ and $G_1 \cap G_2 = \emptyset$.

3. Solve the optimization problem (4.133). If there is a rank-1 optimal solution $\mathbf{P}^*$, then go to step 2; otherwise, remove one user from G_1 or G_2 in order to get the optimal rank-1 solution $\mathbf{P}^*$ with the minimum transmitted power.

If such a user exist, remove this user from G_{serve} and go to step 2; otherwise randomly remove one user from G_{serve} and go to step 2.

The algorithm will be terminated: (1) for all randomly selected patterns of G_1 and G_2, the optimization problem (4.133) will has a corresponding rank-1 optimal solution $\mathbf{P}^*$; (2) $G_{\text{serve}} = \emptyset$.

4.2 A Compressed Sensing Based Ultra-Wideband Communication System

4.2.1 Introduction

Ultra-wideband (UWB) [3,42–44] represents a new paradigm in wireless communication. The unprecedented radio bandwidth provides advantages such as immunity from flat fading. Two primary challenges exist: (1) how to collect energy over the rich multipath components; (2) extremely high sampling rate analog to digital conversion (A/D). Time reversal [45] provides a promising solution to the first problem [46]. In particular, the concept of time reversal has recently demonstrated in a real-time hardware test-bed [47, 48]. At the heart of time reversal, the channel itself is exploited as a part of the transceiver. This idea makes sense since when few movements exist, the channel is time-invariant and reciprocal [49]. In principle, most of the processing at the receiver can be moved to the transmitter—where energy consumption and computation are sufficient for many advanced algorithms.

A natural question arises: Can we move the hardware complexity of the receiver to the transmitter side to reduce the sampling rate of A/D to the level of 125 Msps—for which excellent high dynamic range commercial solutions are available? Fortunately compressed sensing (CS) [50, 51] is a natural framework for our purpose.

CS has been used to UWB communications [52, 53]. Our major contribution is to exploit the channel itself as part of compressed sensing, through waveform-based pre-coding at the transmitter. Only one low-rate A/D is used at the receiver. We also have demonstrated (Fig. 4.3) a UWB system covering the 3 GHz – 8 GHz frequency band that would, if with the conventional sampling technology, take decades for the industry to reach.

This section is organized as follows. Section 4.2.2 introduces the CS theory background and extends CS concept to a continuous time filter based architecture. Section 4.2.3 describes the proposed CS based UWB system together with a CS based channel estimation method. Section 4.2.4 shows the simulation results and section 4.2.5 gives the conclusions.

4.2.2 Compressed Sensing for Communications

Compressed sensing background

Reference [54] gives a most succinct highlight of the CS principles and will be followed here for a flavor of this elegant theory. Consider the problem of reconstructing an $N \times 1$ signal vector x. Suppose the basis $\Psi = [\psi_1, ..., \psi_N]$ provides a K-sparse representation of x, where $K << N$; that is

$$x = \sum_{n=0}^{N-1} \psi_n \theta_n = \sum_{l=1}^{K} \psi_{n_l} \theta_{n_l} \tag{4.134}$$

Here x is a linear combination of K vector chosen from Ψ; $\{n_l\}$ are the indices of those vectors; $\{\theta_{n_l}\}$ are the coefficients. Alternatively, we can write in matrix notation

$$x = \Psi\theta, \tag{4.135}$$

where $\theta = [\theta_0, \theta_1, ..., \theta_{N-1}]^T$. In CS, x can be reconstructed successfully from M measurements and $M << N$. The measurement vector y is done by projecting x over another basis Φ which is incoherent with Ψ, i.e. $y = \Phi\Psi\theta$. The reconstruction problem becomes an $l_1 - norm$ optimization problem:

$$\hat{\theta} = \arg\min ||\theta||_1 \quad s.t. \quad y = \Phi\Psi\theta. \tag{4.136}$$

This problem can be solved by linear programming techniques like basis pursuit (BP) or greedy algorithms such as matching pursuit (MP) and orthogonal matching pursuit (OMP).

When applying CS theory to communications, the sampling rate can be reduced to sub-Nyquist rate. In [55] and [56] a serial and a parallel system structure were proposed, respectively. Sampling rate can be reduced to less than 20% of Nyquist rate. However, they were designed for signals that are sparse in frequency domain. In this section we propose a serial system structure which is suitable for pulse-based UWB communications, which is sparse in time domain. The analog-to-information converter (AIC) structure in [55] is not suitable for UWB communications. 3 – 8 GHz UWB signal is considered as an example in describing the reasons:

- The pseudo noise (PN) chip rate requirement for PN sequcnce makes it difficult for UWB signals, which must be at least twice the maximum signal frequency. For example, a 3 – 8 GHz UWB signal needs at least 16 GHz chip rate.
- The multiplier, which can be a mixer, supporting such high bandwidth for 3 – 8 GHz UWB signal is difficult to implement.
- The system is time-variant. Each measurement is the product of a streaming signal and a changing PN sequence. This requires a huge amount of storage space and complex computation.

In this section, a simple architecture that is suitable for UWB signals is proposed using a finite impulse response (FIR) filter-based architecture.

Filter-based compressed sensing

Random filter based CS system for discrete time signals was proposed in [57]. This idea can be extended to continuous time signals. We use $*$ to denote the convolution process in a linear time-invariant (LTI) system. Assume that there is an analog signal $x(t), t \in [0, T_x]$ which is K-sparse over some basis Ψ:

$$x(t) = \sum_{n=0}^{N-1} \Psi_n(t)\,\theta_n = \Psi(t)\,\theta, \tag{4.137}$$

where

$$\Psi(t) = [\Psi_0(t), \Psi_1(t), ..., \Psi_{N-1}(t)], \tag{4.138}$$

$$\theta = [\theta_0, \theta_1, ..., \theta_{N-1}]^T. \tag{4.139}$$

Note that there are only K non-zeros in θ. $x(t)$ is then fed into a length-L FIR filter $h(t)$:

$$h(t) = \sum_{i=0}^{L-1} h_i \delta(t - iT_h), \tag{4.140}$$

where T_h is the time delay between each filter tap.

The output $y(t) = h(t) * x(t)$ is then uniformly sampled with sampling period T_s. T_s follows the relation $T_s/T_h = q$, where q is a positive integer. M samples are eolleeted so that $M \cdot T_s = \lfloor L \cdot T_h + T_x \rfloor$, where $(L \cdot T_h + T_x)$ is the duration of $y(t)$.

Now we have the down-sampled output signal $y(mT_s), m = 1, 2, ..., M-1$:

$$\begin{aligned} y(mT_s) &= h(mT_s) * x(mT_s) \\ &= \int_0^{T_y} h(mT_s - \tau) x(\tau) d\tau \\ &= \int_0^{T_y} \left[\sum_{i=0}^{L-1} h_i \delta(mT_s - iT_h - \tau) \right] x(\tau) d\tau \\ &= \sum_{i=0}^{L-1} h_i x(mT_s - iT_h) \\ &= \Phi x, \end{aligned} \tag{4.141}$$

where Φ is a $quasi - Toeplitz$ matrix and

$$x = [x(0), x(T_h), ..., x((M-1) qT_h)]^T = \Psi\theta, \tag{4.142}$$

$$\Psi = [\Psi(0), \Psi(T_h), ..., \Psi((M-1) qT_h)]^T. \tag{4.143}$$

A $quasi - Toeplitz$ matrix has such property: each row of Φ has L non-zero entries and each row is a copy of the row above, shifted right by q places.

Let $y_m = y(mT_s)$, we have

$$y = [y_0, y_1, ..., y_{M-1}]^T. \tag{4.144}$$

Combining Equations 4.137, 4.138, 4.139, 4.141, 4.142, 4.143 and 4.144, we have:

$$y = \Phi\Psi\theta = \Theta\theta \tag{4.145}$$

Now the problem becomes recovering $N \times 1$ vector θ from the $M \times 1$ measurement vector y, which is exactly the same as the problem posed in Equation 4.136. The number of measurements for successful recovery depends on the sparsity K, duration of the analog signal T_x, filter length L and the incoherence between Φ and Ψ. Numerical results in Section 4.2.3 show that when $x(t)$ is sparse and $h(t)$ is a PN sequence, θ can be reconstructed successfully with a reduced sampling rate, requiring only $M << N$ measurements. Note that measurement y is a projection from x via an FIR filter. We use this feature to design our proposed system.

4.2.3 Compressed Sensing Based UWB Communication System

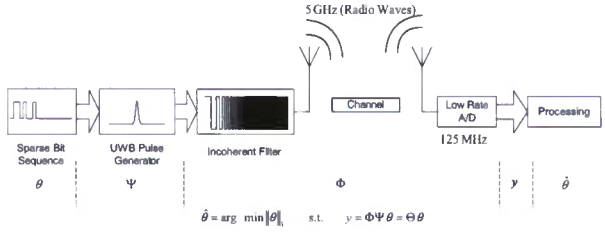


Figure 4.3: The system architecture of the proposed CS based UWB system. The communication problem of recovering the transmitted information can be modeled as a CS problem.

Communication system architecture

With the knowledge of Section 4.2.2 and Section 4.2.2, we propose a CS-based UWB communication system which is able to reduce the sampling rate to 1.25% of Nyquist rate. The system architecture is illustrated in Fig. 4.3. A UWB signal is transmitted by feeding a sparse bit sequence through a UWB pulse generator and an pre-coding filter. Then, the received signal is directly sampled after the channel, using a low-rate A/D and then processed by a recovery algorithm. Φ is the projection matrix consisting of the pre-coding filter and the channel. It can be noticed that channel itslef is part of the projection matrix in CS, so the receiver is very simple, with only one low-rate A/D to collect measurement samples. Our simulation in Section 4.2.4 shows that $3 - 8$ GHz UWB signals can be successfully recovered by a 125 Msps A/D.

K-pulse position modulation (PPM) is used to modulate sparse bit sequence. Each PPM symbol is K-sparse: there are N positions and only $K << N$ pulses in each symbol, as illustrated in Fig. 4.4. The output of the UWB pulse generator can be written using the notations in Equation 4.137 and 4.138, with $\Psi_n(t) = p(t - nT_p)$, where $p(t)$ is the function of the UWB pulse and T_p is the period of the pulse. Pre-coding filter and channel are modeled as FIR filters, with combined impulse response $h(t) = f(t) * c(t)$, where $f(t)$ and $c(t)$ are the impulse response for the pre-coding filter and the channel, respectively. Here $h(t)$ is equivalent to the $h(t)$ in Equation 4.140. The received signal $y(t) = h(t) * x(t)$ is then uniformly sampled by an A/D with sampling period T_s. Similar to Equation 4.141 and 4.144, the down-sampled measurements form the $M \times 1$ vector $y = \Phi\Psi\theta = \Theta\theta$, where Φ is a $quasi - Toeplitz$ matrix. Now, the communication problem becomes a problem of estimating $\hat{\theta}$ from $M << N$ measurements, which is again identical to the problem described as Equation 4.136.

The success of recovery relies on the sparsity K and the incoherence between Ψ and Φ. Sparsity is easily met by controlling the transmitted sequence. In our simulation, $K = 1$, which means that there is only one pulse in PPM symbol. The incoherence property can be met by proper selection of the pre-coding filter $f(t)$. Simulation results

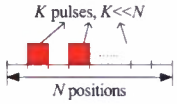


Figure 4.4: The structure of the transmitted symbol. This symbol is K-sparse. There are K pulses in N positions and $K << N$.

Figure 4.5: Block diagram of channel estimation

show that if $f(t)$ is a PN sequence whose chip rate is equal to the bandwidth of the UWB pulse $p(t)$, θ can be successfully recovered using recovery algorithms. So far the discussion is in baseband. If the transmitted UWB is passband, then up-conversion is applied after the pre-coding filter. PN chip rate and the receiver structure remain the same. No down-conversion is required at the receiver. For example, as will be shown in the simulation, a 3 – 8 GHz UWB pulse requires a 5 GHz PN chip rate, which is the same as the signal bandwidth, not the Nyquist rate of the maximum signal frequency, as required by the AIC system. A/D at the receiver directly samples the received signal, without doing down-conversion.

The number of measurements M and sampling rate are related and determined by the length of the combined filter $h(t)$. If $h(t)$ is long, the received signal is "spread out" in the time domain, therefore sufficient measurements can be made under a lower sampling rate.

Channel estimation

After down-sampling, y is processed at the receiver with Θ using BP. In constructing Θ, $f(t)$, $c(t)$ and $\Psi(t)$ are required. $f(t)$ and $\Psi(t)$ are fixed and can be considered as prior knowledge at the receiver. The channel, $c(t)$, however, needs to be estimated. A CS based channel estimation method is proposed. A 3 – 8 GHz channel can be estimated by a 500 Msps A/D.

Similar to Equation 4.140, the UWB channel can be modeled as:

$$c(t) = \sum_{i=0}^{L-1} c_i \delta(t - iT_h) \tag{4.146}$$

The channel estimation block diagram is illustrated in Fig. 4.5. A UWB probing pulse $p(t) * f(t)$ is transmitted to "probe" the channel, where $p(t)$ is a UWB pulse and $f(t)$ is a PN sequence. At the receiver, sub-Nyquist rate A/D collects M uniform measurements. This process can be represented as $y = D \downarrow (c(t) * f(t) * p(t))$, where $D \downarrow$ denotes a down-sampling factor of $\lfloor N/M \rfloor$ and y denotes the measurement vector. Since the system is LTI, an alternative block diagram can be drawn as Fig. 4.6. Then, $y = D \downarrow ((f(t) * p(t)) * c(t))$. In matrix notation, $y = \Theta c$, where Θ is a $quasi-Toeplitz$ matrix derived from $f(t) * p(t)$ and $c = [c_0, c_1, ..., c_{L-1}]^T$. The channel estimation problem is to get $\hat{c}$ from measurements y, which is identical to the CS problem described in Equation 4.136.

Successful recovery requires c to be sparse and the incoherent property of measurement matrix Θ [51]. Indoor UWB

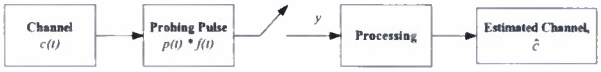


Figure 4.6: An equivalent block diagram of channel estimation

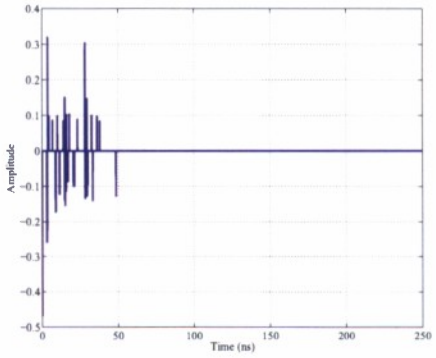


Figure 4.7: Time domain channel derived from VNA measurement. The sparsity of this channel is 50.

channel is sparse and PN sequence structured Θ has the incoherent property. PN chip rate should be the same as the bandwidth of the channel under estimation. We use simulation to show the estimation result.

First, we need to set up the real channel $c(t)$ as the estimation target. Vector network analyzer (VNA) is used to get the real indoor channel coefficient c. 3 – 8 GHz channel is measured by VNA with 1 MHz frequency step and 128 averages. $c(t)$ (Fig. 4.7) is derived from the VNA data using CLEAN algorithm with a rectangular window. There are about 50 non-zero entries in c. PN chip rate is 5 GHz and length of $f(t)$ is 1 μs. Baseband Gaussian UWB pulse $p(t)$ has 5 GHz bandwidth. Since the measured channel is in passband, up-conversion is applied after the PN filter. At the receiver, 500 Msps A/D is used to get measurements. BP is then used to get the estimated vector $\hat{c}$ with the knowledge of $f(t)$, $p(t)$ and y only. Additive white Gaussian noise (AWGN) is added at the received samples as $y = \Theta c + w$, where w is the noise vector. Basis pursuit denoising (BPDN) is used to solve the recovery problem with noise. Fig. 4.8 (a) shows the estimation result and Fig. 4.8 (b) shows the zoomed in result. It can be seen that though $\hat{c}$ is a little noisy, all major paths in $\hat{c}$ perfectly match to c. Only the amplitudes are slightly different.

We will use c as "perfect estimation" to form the measurement matrix Φ and the noisy $\hat{c}$ as "imperfect estimation" to form the measurement matrix $\hat{\Phi}$ in the CS-based UWB communication system symbol error rate simulation. Interestingly, though imperfect estimation is noisy, the symbol error rate is similar to perfect estimation.

4.2.4 Simulation Results

Since UWB channel is stable when few movements exist in the indoor environment, we assume that channel is time-invariant during the channel estimation and communication process.

In the simulation, each symbol has only one pulse in 256 candidate positions, containing 8 bits information. This is a special case of the PPM symbol illustrated in Fig. 4.4, with $K = 1$. More pulses can be used to increase the information per symbol. Since the purpose of this work is to recover θ, not maximizing the data rate, the case

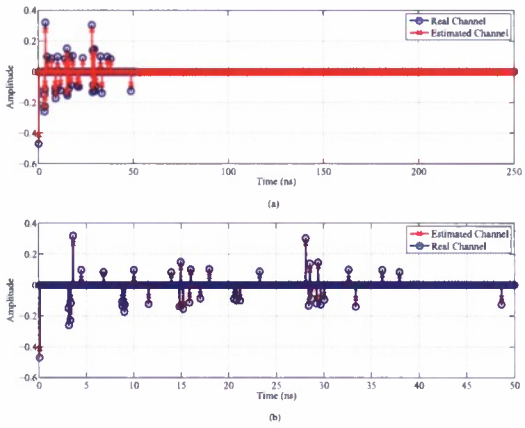


Figure 4.8: (a) Channel estimation result. (b) Zoomed in version of the result.

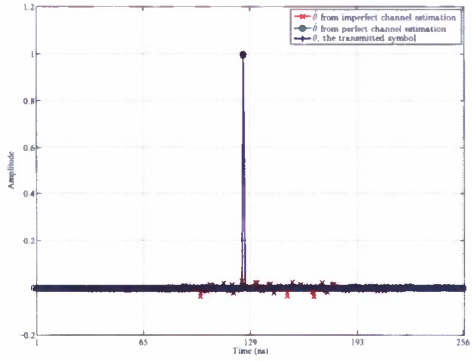


Figure 4.9: Recovery of $\hat{\theta}$ using 125 Msps A/D, perfect/imperfect channel estimation. No noise is added.

when $K > 1$ is not simulated. The UWB pulse generator produces a 5 GHz bandwidth Gaussian pulse. The precoding filter is a PN sequence with 128 ns duration and 5 GHz chip rate. Then the signal is modulated with a 5.5 GHz sinusoidal, up-converting to the $3 - 8$ GHz frequency band. Measured channel $c(t)$ in 4.7 is used. Due to the delay spread of the channel and the length of PN sequence, the received signal y(t) is spread out over 256 ns. A 256 ns guard period is added between symbols to avoid intersymbol interference (ISI). At the receiver, perfect synchronization is assumed. 125 Msps, 250 Msps and 500 Msps sampling rates are simulated to evaluate the symbol error rate VS SNR per symbol performance. Since measurements are made in a 512 ns period, the relating numbers of measurements M for 125 Msps, 250 Msps and 500 Msps are 64, 128 and 256, respectively. BPDN provided by [58] is used as the reconstruction algorithm. The position with maximum amplitude in $\hat{\theta}$ is compared with the position in θ. If two positions are exactly the same, the symbol is considered as reconstructed successfully. 20000 simulations were performed for each SNR plot.

Fig. 4.9 shows the reconstruction result under 125 Msps sampling rate without any additive noise. $\hat{\theta}$ reconstrueted from perfect/imperfect channel profile is compared with original θ. From Fig. 4.9, we can see that $\hat{\theta}$ from imperfect channel profile is a bit more noisy. However, the position of maximum amplitude is exactly the same as the one in θ. Therefore, the transmitted symbol is recovered successfully. After 20000 simulations, no errors can be found.

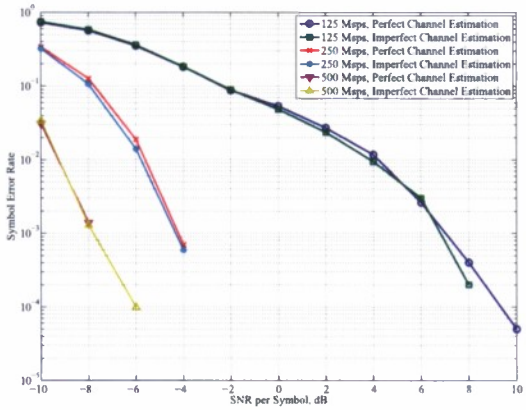


Figure 4.10: Simulation results of symbol error rate vs SNR per symbol at the receiver.

Fig. 4.10 shows the results under AWGN. Perfect/imperfect channel estimation and 125 Msps/250 Msps/500 Msps sampling rate are simulated. We can see that higher sampling rate provides better symbol error rate performance. This is because more measurements are collected under higher sampling rate. It is also noticed that under same sampling rate, the symbol error rate of perfect channel estimation and imperfect channel estimation have almost no difference. From the 500 Msps sampling rate curve, we can see that the symbol error rate is 0 when SNR is over -6 dB, in 20000 simulations.

Many interesting topics are raised after the simulation. Does the measurement matrix Φ and Ψ satisfy the incoherence property in theory? What is the relationship for sampling rate, SNR and symbol error rate? Why the imperfect channel estimation shows similar performance with perfect channel estimation? How to achieve synchronization with the system? Further effort needs to be done to explain these questions.

4.2.5 Conclusions

Our proposed approach is to exploit the projection matrix with channel itself and a waveform-based pre-coding at the transmitter. Taking the channel as part of CS results in a very simple receiver design, with only one low-rate A/D. The pre-coding is implemented in a natural way using an FIR filter. The concept has been demonstrated, through simulations, using real-world measurements. Realistic channel estimation is also considered. The philosophy is to trade computation complexity for hardware complexity, and move receiver complexity to the transmitter.

This work is just the beginning of the pre-coded CS. Future work includes reduction of algorithm complexity. Much quicker algorithms are required for real-time applications such as UWB communications. Deterministic CS [59] will be considered in the context of UWB channel.

Traditional pre-coding optimizes the system in the digital domain. The waveform-based pre-coding optimizes the transceiver in both mixed signal and digital domain. CS provides a natural framework. It may be more natural to combine waveform-based pre-coding with sampling innovation [60], since pre-coding can be used to reduce the degrees of freedom—thus the sampling rate.

4.3 Publication List

Here is a list of publications credited to this project.
Journal Papers:

- R. Qiu, N. Guo, H. Li, Z. Wu, V. Chakravarthy, Y. Song, Z. Hu, P. Zhang, and Z. Chen, "A Unified Multi-Functional Dynamic Spectrum Access Framework: Tutorial, Theory and Multi-GHzWideband Testbed," Sensors, no. 8, pp 6530-6603, August 2009.
- C. Zhou and R. C. Qiu, "Pulse Distortion and Optimum Transmit Waveform for Pulse-based UWB Communications," International Journal of Ultra Wideband Communications and Systems (IJUWBCS), Vol. 1, No. 1, pp. 32-48, 2009.
- C. Zhou, N. Guo and R. C. Qiu, "Time Reversed Ultra-Wideband (UWB) Multiple-Input Multiple-Output (MIMO) Based on Measured Spatial Channels," IEEE Trans. Vehicle Technology, Vol. 58, No. 6, pp. 2884-2898, July 2009. (1 citation)
- Z. Hu, R. C. Qiu and D. Singh, Spectral Efficiency for MIMO UWB Channel in Rectangular Metal Cavity, JOURNAL OF NETWORKS (JNW), Vol. 4, No. 1, pp. 42-52, Feb. 2009. C. Zhou and R.C. Qiu, Pulse Distortion Caused by Cylinder Diffraction and Its Impact on UWB Communications, IEEE Trans. Vehicular Technology, Vol . 56, No. 4, pp. 2385-2391, Jul. 2007.

Proceedings Papers:

- Z. Hu, N. Guo and R. C. Qiu, "Wideband Waveform Optimization with Energy Detector Receiver in Cognitive Radio," IEEE SoutheastCon 2010, SC, March, 2010.
- Z. Chen and R. C. Qiu, "Prediction of Channel State for Cognitive Radio Using Higher-Order Hidden Markov Model," IEEE SoutheastCon 2010, SC, March, 2010.
- Y. Song, N. Guo and R. C. Qiu, "Real-time MISO UWB Radio Testbed and Waveform Design," IEEE SoutheastCon 2010, SC, March, 2010.
- Z. Chen, Z. Hu and R. C. Qiu, "Quickest Spectrum Detection Using Hidden Markov Model for Cognitive Radio," IEEE MILCOM'09, Boston, MA, October 18-21, 2009. (2 citation)
- Z. Hu, N. Guo and R. C. Qiu, "Wideband Waveform Optimization for Energy Detector Receiver with Practical Considerations," IEEE ICUWB09, Vancouver, Canada, September 9-11, 2009.
- A. S. Saini, Z. Hu and R. C. Qiu, "Spectrum Sensing and Reconstruction for Cognitive Radio," IEEE SSST'09, Tullahoma, TN, USA, March 15-17, 2009. (1 citation)
- N. Guo, Z. Hu, A. S. Saini and R. C. Qiu, "Waveform-level Precoding with Simple Energy Detector Receiver for Wideband Communication," IEEE SSST'09, Tullahoma, TN, USA, March 15-17, 2009. (3 citations)
- P. Zhang, Z. Hu, R. C. Qiu and B. M. Sadler, "Compressive Sensing Based Ultra-wideband Communication System," IEEE ICC'09, Dresden, Germany, Jun. 14-18, 2009. (1 citation)

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Part III

Technical Impacts

4.4 UWB MIMO Testbed

For more than decades, multiple-antenna technology has been an important field of communications research [61]. It has became a key technology for wireless local area networks (WLANs), wireless metropolitan area networks (WMANs), and cellular mobile communication systems (3G, 4G), because they promise greater coverage, higher data rates, and improved link robustness by adding a spatial dimension in addition to the time, the frequency, and the code dimensions [62]. Intensive theoretical researches have been performed on multiple-antenna system often based on simplified models of reality. There are few practical implementations to verify the theoretical gain of a multiple-antenna system, especially for the wideband multiple-antenna system that introduces much more challenges over the narrowband system. The accurate performance investigation over realistic imperfect channels have motivated the design of a real time radio testbed. In the authors' group, MISO UWB characteristics and performances have been well studied and various results have been demonstrated in [63] [64]. Further more, a simple 2 by 1 MISO UWB testbed based on time reversal system has already been presented in last quarterly report, it employs an FPGA for fast parallel processing of transmitted data, and the operation and performance of this MISO UWB radio testbed are investigated in the case of wideband waveform level precoding.

4.4.1 2-By-1 UWB MISO Testbed Description

The whole testbed is a module-based system as described in [65]. Figure 4.11 shows the system architecture, where there are two transmit channels at transmitter side and only one receive channel at receiver side. As the most powerful device for parallel signal processing, FPGA plays a critical role in the system, all waveform algorithms will be implemented in FPGA. The two digital outputs with both I and Q phase from the FPGA board will be sent to two identical dual channel digital-to-analog converter (DAC) boards, which are capable of 1Gsamples/sec and 14 bits of precision,In the FPGA design of the transmitter, there are two waveform generators modules which support both I-phase and Q-phase modulation. The receiver is energy detection based as a low-complexity reception technique which eliminates the need for channel estimation and precise synchronization.

4.4.2 Potential UWB MIMO Testbed

Another RF receiver chain will be needed to evolve the current 2-by-1 MISO testbed to a 2-by-2 MIMO testbed, the baseband processing unit also need to be able to receive two RF signals. The RF solution is the wideband demodulator ADL5380 and dual-channel digital gain trim amplifier AD8366, which are described in appendix and both are from Analog,Inc.

For the baseband processing solution, we have already purchased the EV8AQ160 QUAD ADC evaluation board manufactured by E2V, Fig 4.12 shows the picture. The Quad ADC is constituted by four 8-bit ADC cores which can be considered independently (four channel mode) or grouped by two cores (two-channel mode with the ADCs interleaved two by two or one-channel mode where all four ADCs are all interleaved).

The EV8AQ160-EB Evaluation Board is very straightforward as it implements e2v EV8AQ160 Quad 8-bit 1.25 Gsps ADC device, Atmel ATMEGA128 AVR, SMA connectors for the sampling clock, analog inputs and reset inputs accesses and 2.54 mm pitch connectors compatible with high-speed acquisition system probes. Thanks to its user-friendly interface, the EV8AQ160-EB Kit enables to test all the functions of the EV8AQ160 Quad 8-bit 1.25 Gsps ADC using the SPI connected to a PC.

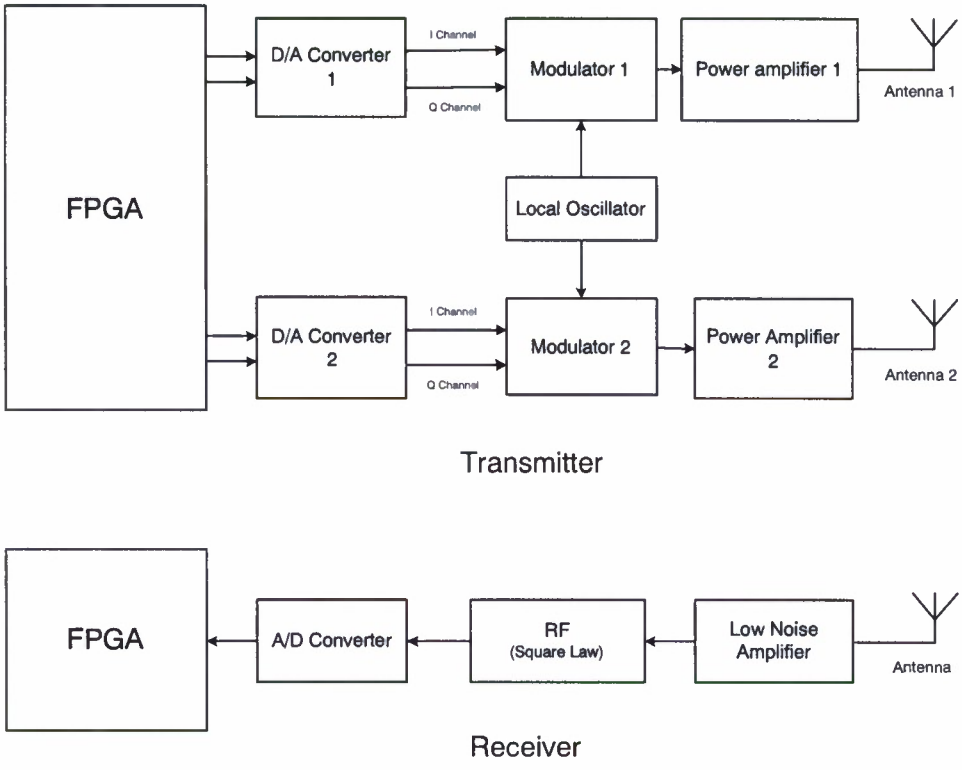


Figure 4.11: MISO UWB testbed architecture

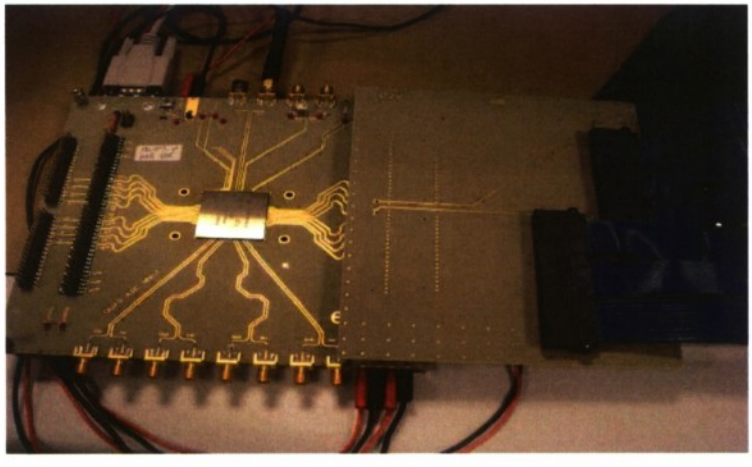


Figure 4.12: Picture of EV8AQ160-EB Evaluation Board

Chapter 5

Waveform Diveristy

This project drives our investigation in waveform diversity and helps reveal the importance of as well as insight into waveform diversity. Waveform diversity is a key research topic currently in wireless communications, radar, sensing, and imaging. Waveform should be designed or optimized according to different requirements or objectives, and it should be adapted or diversified dynamically to the operating environment in order to achieve a performance gain [66]. For example, the waveform should be designed to carry more information to the receiver in terms of capacity. If the energy detector is employed at the receiver, the waveform should be optimized such that the signal energy within the integration window at the receiver reaches the maximum [1] [34] [67] [37]. For navigation and geolocation, an ultra short waveform should be used to increase the resolution. For multi-target identification, the waveform should be designed so that the radar returns can bring more information back. In clutter dominant environments, maximizing the target energy and minimizing the clutter energy should be considered. In electronic warfare, anti-jamming is a critical task for the outcome of the warfare. Though currently anti-jamming is performed at the receiver, if the transmitter knows some kind of information about the jamming at the receiver, for example, the second order statistics about jamming, the transmitter can elaborately design the waveform and help the receiver cancel the jamming signal and reduce system power consumption.

Multiple Input Single Output (MISO) system is one type of multi-antenna system in which there are multiple antennas at the transmitter and one antenna at the receiver. MISO system can explore the spatial diversity and execute the transmitter beamforming to focus energy on the desired direction or point and avoid interference to other radio systems. It is well known that waveform and spatially diverse capabilities are made possible today due to the advent of lightweight digital programming waveform generator [68] or arbitrary waveform generator. Waveform diversity can also be applied to wideband system. A variety of waveforms with different time-frequency characteristics can be explored in wideband systems to support high data rate and physical layer security for radio communications as well as high resolution and accuracy for radars. Waveform design/optimization for wideband multiple-antenna systems is documented in [69]. From theoretical point of view, the contribution of [69] can be summarized as follows: (1) the equivalent baseband waveforms are designed for the passband system. (2) Different waveforms for different transmitter antennas are jointly optimized to reach global optimum performance. At the receiver, the received signals from different transmitter antennas are combined over the air such that the receiver antenna sees only a single copy of signal from the transmitter no matter how many transmitter antennas exist. In order to achieve this over-the-air phase coherency for the passband signals, precise synchronization between these signals has to be achieved at the transmitter [68].

In the context of cognitive radio, a cognitive radio user, or secondary user can coexist with other secondary and

primary users. However, waveform design/optimization gives us more flexibilities to design the radio and may make the coexistence even better. Consider a scenario where wideband secondary users with low spectrum density are allowed to overlay with narrowband primary users. In addition to the traditional communication objectives and constraints, spectral mask constraint at the transmitter and the interference cancellation at the receiver can be jointly considered in optimizing the waveform. Spectral mask constraint is imposed on the secondary-user transmitted waveform such that the transmitter has no or limited interference to the primary users, while some interference cancellation scheme implemented at the secondary-user receiver cancels the narrowband interference caused by the primary users.

Though the thought of waveform diversity for the radar systems can be traced back to the World War II, due to the computational capability and hardware limitations, many waveform design algorithms can not be implemented into the radar systems [66] for many years. Nowadays, these bottlenecks are knocked down and waveform diversity becomes a hot spot afresh in the radar society. Time reversal or phase conjugating waveform, colored waveform, sparse and regular non-uniform Doppler waveform, non-circular waveform, and so on, are handled based on advanced mathematics tools in [70]. New trends in coded waveform design for radar applications are presented in [71]. The modern semidefinite programming (SDP) and the novel algorithm on Hermitian matrix rank-one decomposition are exploited to perform code selection, which can maximize the detection performance and control the Doppler estimation accuracy as well as the similarity with a pre-fixed radar code [71]. Meanwhile, another force to propel the research on waveform diversity is the introduction of cognition to the radar systems. A cognitive radar can actively learn about the environment, and the whole radar system forms a dynamic feedback loop involving the transmitter, environment and receiver [72]. Waveform diversity will play an important role in cognitive radar. The radar transmitter can adjust its illumination (waveform) in an intelligent, effective, adaptive and robust manner, taking into account the results of learning and perception on the environment [72]. Thus, the philosophy of sequential testing [73] can be embraced under the umbrella of cognitive radar smoothly. Several rounds of testing illuminations will be used until the belief of correct decision is made. The waveform and the transceiver scheme for each round of test can be adjusted according to the results of the previous tests. For example, adaptive compressing sensing (CS) [74] gives us the hint on this research field.

The previous theoretical researches on waveform diversity do not take into account the robustness seriously. There are several reasons for that: (1) the theory of robust optimization was not that mature in the old days; (2) Robustness makes waveform diversity more complex; (3) the research on waveform diversity was only limited to computer simulation. As the theory of robust optimization becomes mature and the bottlenecks of computation and implementation (e.g., arbitrary waveform generator) are knocked down, robust optimization for waveform diversity (or robust waveform diversity) will bring more attentions. Robustness truly bridges the gap between theoretical work and practical situation.

Obviously waveform diversity is implemented at the transmitter side. But waveform diversity should have broader meaning and significance. First of all, any type of signal processing in the waveform level at the receiver should also be included into the waveform diversity framework. One common signal processing is the receiver beamforming including the narrowband beamforming and wideband beamforming. Robust receiver beamforming is dealt with in [39] [75]. The uncertainty comes from the mismatch of steering vector and from the estimation error of the sampled covariance matrix of interference plus noise. If implementation uncertainty is taken into account [76], robust optimization will play an important role in waveform diversity.

Chapter 6

Wideband Digital Beamforming

6.1 Wideband Multichannel RF Front-End For Beamforming

The multichannel receiver is a building core for any MIMO system in either communication or radar. Especially from military perspective, there has been a critical and constant need for enhanced multichannel receivers for array and radar applications. More channels and bandwidth are required, while less power consumption, lower cost, and smaller sizes are expected. There is also a trend that the receivers are more and more digital, thanks to the advance in semiconductor technologies. Having seen so much progress in hardware, especially, dramatic increase of sampling rate in digital processing, newer type of receivers that take advantages of all possible new concepts and most advanced components/devices are expected. A variety of available technologies have to be considered and compromising has to be made among a large number of factors.

6.2 Overall Architecture

Illustrated in Fig.6.1 is a high level multichannel receiver architecture containing three functional blocks: analog front-end (tuner), digitizer and digital backend. In choosing the sampling rate and determining digital computational load, we will attempt to be a little aggressive, expecting that digital processing power will increase while the cost will drop continuously. There are a number of options in selecting a digital processing platform. We prefer to use an array of high performance FPGAs such as Xilinx Virtex-5 or Virtex-6 series, in conjunction of a DSP engine. This hybrid signal processing platform is not only flexible, but compromises both real-time filtering and highly computational beamforming, thus it is particularly attracting for wideband digital beamforming prototyping.

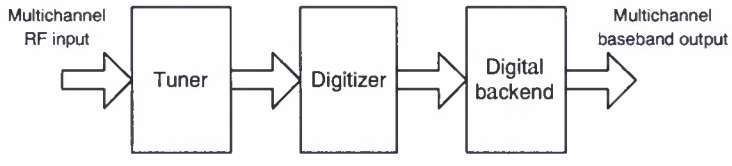


Figure 6.1: High level multichannel receiver architecture.

6.3 Analog Front-end (Tuner)

In general there are two popular options for radio front-end architecture: heterodyne (or superheterodyne) and zero-IF (or direct-conversion, homodyne) architectures. The heterodyne architecture has better performance if compared with the other, and therefore it has been the most popular receiver architecture sine it was invented by Edwin H. Armstrong in 1918. On the other hand, although the concept of zero-IF reception was first proposed by F.M. Colebrook as early as in 1924 (6 years before the heterodyne receiver was invented), it was not until 1947 that it was put into practice, the first application being measurements in telephony. Since 90's, zero-IF architecture has been especially promoted in software defined radio (SDR) community. Compared with the traditional receiver architecture, its main advantages are the following:
(1) The problem of image rejection is overcome, so that the receiver preselection portion is simplified and frequency planning is unnecessary.
(3) The fact that most signal processing is done at low frequencies implies using LPFs as channel-select filters.
(4) Amplification is mainly at the baseband stage, hence power is saved. In general, a zero-IF receiver contains less hardware and has very high level of integration.

While being attractive, the zero-IF receiver architecture has many drawbacks: DC offset, I/Q imbalance (or mismatching) with analog quadrature downconverter, even-order distortion, self-mixing, 1/f (or clicker) noise, and local oscillator (LO) leakage. In order to combine the advantages of both the heterodyne and zero-IF architectures, a low-IF receiver architecture was proposed in later 90's. This architecture indeed keeps a high level of integration and eliminates most of the drawbacks associated with the zero-IF receivers, but it introduces image rejection requirement. When the RF frequencies are lower than 2 GHz (HF, VHF, UHF and L bands), the rather low IF frequency image rejection is difficult to implement and image rejection mixer techniques are required instead of an image rejection filter. In practical image rejection mixers, the amplitude and phase mismatches between I and Q channels are ultimate limitation of the image rejection ratio [77]. In addition, designing and implementing ultra wideband image rejection mixers is extremely difficult.

Although the low-IF structure has many advantages, it may not be feasible For UWB applications, due to the limitation of the digitizer's sampling rate. The zero-IF structure will be the first choice at present. In the future, low-IF can be considered if the digitizer's sampling rate significantly increases or the signal bandwidth is much less than 500 MHz.

6.4 Multichannel Digitizer with FPGA Based Filters

We have chosen Sundance SMT702 Digitizer boards to build a wideband beamformer. Fig. 6.2 shows the 4-channels system architecture consists of 5 SMT702 boards, each channel with both I phase and Q phase channel, capable of handling 3Gsps sampling. In this architecture, the Sundance SHB cables will be used to connect all the boards. High speed data filtering and combining are relied on the on-board FPGA chips. A DSP engine which is not shown in Fig. 6.2 will take care of sophisticated beamforming computation.

The SMT702 is a PXI Express Peripheral Module (3U), which integrates two 3 Gsps 8-bit ADCs, a clock circuitry, 2 banks of 1GByte DDR2 Memory each and a Xilinx Virtex5 LX110T-3 FPGA, under the 3U format. The good news for this product is it can be standalone and with a number of general I/Os.

Both ADC chips are identical and can produce 3 Giga-samples per second each, with an 8-bit resolution. The

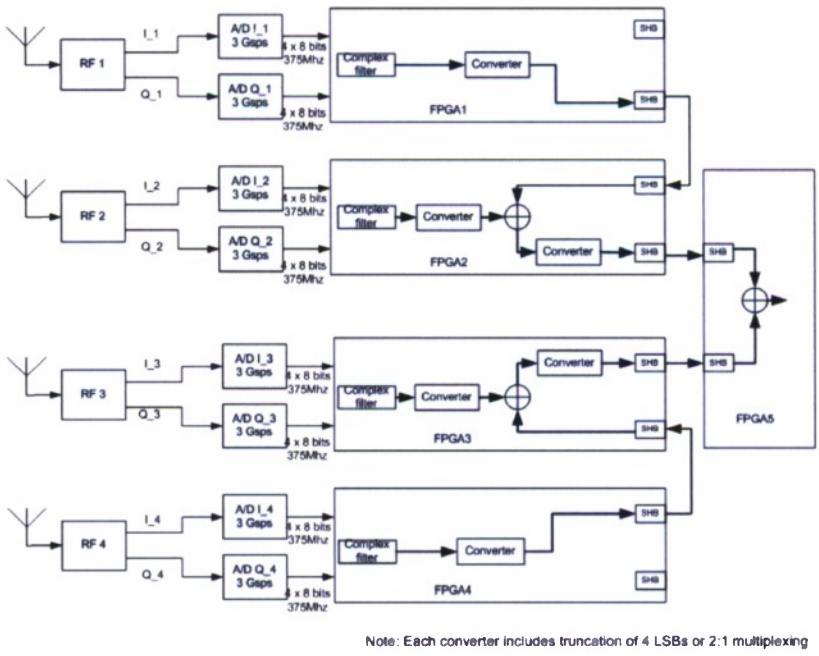


Figure 6.2: Wideband beamforming architecture wiht 5 SMT702 high speed digitizers.

manufacturer is National Semiconductor and the part number is ADC083000. Analog-to-Digital converters are clocked by circuitry based on a PLL coupled with a VCO in order to generate a low-jitter signal. The full bandwidth is 3GHz. Each ADC integrates settings such as offset and scale factor, which makes the pair of ADC suitable to be combined together in order to make a 6GSPS single Analog to Digital converter. This will be subject to a specific application note.

The Virtex5 FPGA is responsible for controlling all interfaces, including PXI (32-bit) and PXIe (up to 8 lanes not all PXI Express controller support 8 lane), as well as routing samples. The FPGA fitted on the SMT702 is part of the Virtex-5 familly from Xilinx, XC5VLX110T-3 (fastest speed grade available).

Two DDR2 memory banks are accessible by the FPGA in order to store data on the fly. An SHB connector is available in order to transfer data/samples to an other Sundance module (SMt712 for instance). All analog connectors on the front panel are SMA.

For software development, the SMT7026 is an efficient, ready to use, host side interface for the SMT702. It allows us to control the SMT702 from the host as well as to exchange data between the host. It can configure the FPGA from the Host, transfer data from the SMT702 to the Host and even provide a C++ type interface to the FPGA module.

6.5 Wideband Beamforming: An Example

The architecture of wideband beamforming is shown in Fig. 6.3. Assume there are M antennas in phased array radar. The distance between antennas is d. The mutual coupling in phased array radar is not considered here. $\delta(t)$ is the signal in the far field of phased array radar and impinges on it from the angle θ_0. The characteristics of RF chains related to different branches are given by $h_m(t), t \in [0, T]$.

Because of the limitation of ADC, the sampled data for each branch is $h_m[n, \theta]$ the time duration of which is $T + \frac{(M-1)d}{c}$. Fractional dclay mcthod is used to get $h_m[n, \theta]$ from $h_m(t), t \in [0, T]$.

The goal of the task is to design filter $w_m[n]$ for each branch in the digital domain to form the wideband beam under different requirements. After summation of each branch's responsc,

$$x[n, \theta] = \sum_{m=1}^{M} h_m[n, \theta] * w_m[n] \tag{6.1}$$

and

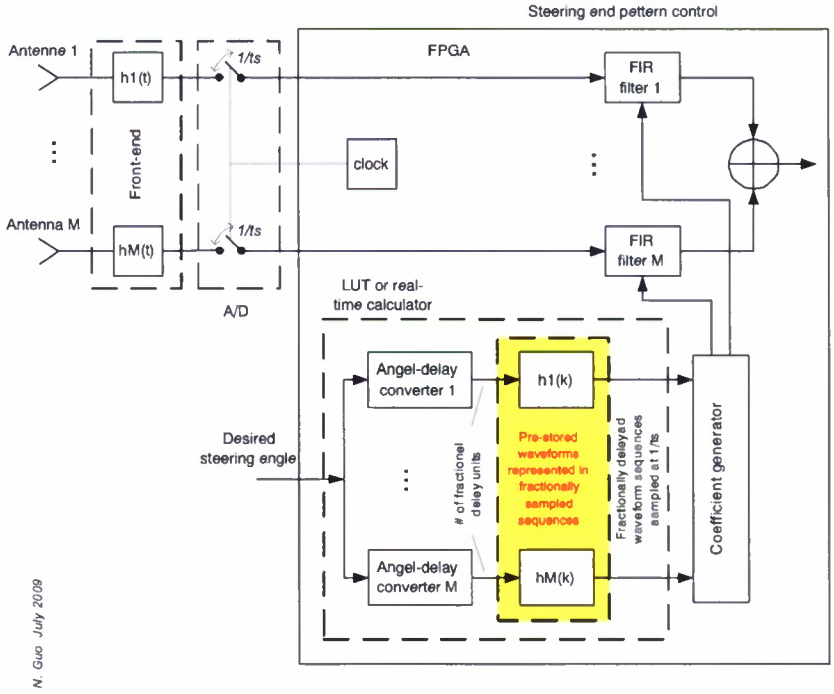
$$x[n_f, \theta] = \text{FFT}\{x[n, \theta]\} \tag{6.2}$$

The beam of phased array radar can be defined as,

$$b[n_f, \theta] = x[n_f, \theta] \tag{6.3}$$

Assume the vector representations of $w_m[n]$, $x[n, \theta]$, $x[n_f, \theta]$ and $b[n_f, \theta]$ are $\mathbf{w}_m$, $\mathbf{x}[\theta]$, $\mathbf{x}_f[\theta]$ and $\mathbf{b}[\theta]$. The toeplitz matrix representation of $h_m[n, \theta]$ is $\mathbf{H}_m[\theta]$. $\mathbf{F}$ is the discrete-time Fourier transform operator. Assume,

$$\mathbf{H}[\theta] = [\mathbf{H}_1[\theta]\ \mathbf{H}_2[\theta]\ \cdots\ \mathbf{H}_M[\theta]] \tag{6.4}$$



Widebend digital beamforming implementetion option 2 (fractionel deleys ers hendled by e LUT).
Adventege: no need for fractional delay saction; disadvantage: large number of combinations to store.

Figure 6.3: Wideband digital beamforming implementation option.

and

$$\mathbf{w} = [\mathbf{w}_1^H \ \mathbf{w}_2^H \ \cdots \ \mathbf{w}_M^H]^H \tag{6.5}$$

where $(\bullet)^H$ denotes the conjugate transpose of matrix.

Eqn. 6.1 and Eqn. 6.2 can be reformualted and combined as,

$$\mathbf{x}_f[\theta] = \mathbf{FH}[\theta]\mathbf{w} \tag{6.6}$$

Assume $\mathbf{A}[\theta] = \mathbf{FH}[\theta]$, thus,

$$\mathbf{b}[\theta] = \mathbf{A}[\theta]\mathbf{w} \tag{6.7}$$

If $\mathbf{p}[\theta_0]$ is the desired array response, i.e. beampattern at θ_0, then the $\|\mathbf{b}[\theta_0] - \mathbf{p}[\theta_0]\|_{l_2}^2$ should be minimized. If there is the broad null from θ_1 to θ_2, then $\sum_{\theta=\theta_1}^{\theta_2} \|\mathbf{b}[\theta]\|_{l_2}^2$ should be minimized.

Assume $\Omega_\theta = [-\frac{\pi}{2}, \frac{\pi}{2}] - \{\theta_0\} - [\theta_1, \theta_2]$, then, the optimization problem can be formulated as,

$$\min_{\mathbf{w}} \|\mathbf{b}[\theta_0] - \mathbf{p}[\theta_0]\|_{l_2}^2 + \lambda_1 \sum_{\theta=\theta_1}^{\theta_2} \|\mathbf{b}[\theta]\|_{l_2}^2 + \lambda_2 \sum_{\theta\in\Omega_\theta} \|\mathbf{b}[\theta]\|_{l_2}^2 \tag{6.8}$$

Let

$$f(\mathbf{w}) = \|\mathbf{b}[\theta_0] - \mathbf{p}[\theta_0]\|_{l_2}^2 + \lambda_1 \sum_{\theta=\theta_1}^{\theta_2} \|\mathbf{b}[\theta]\|_{l_2}^2 + \lambda_2 \sum_{\theta\in\Omega_\theta} \|\mathbf{b}[\theta]\|_{l_2}^2 \tag{6.9}$$

The optimization problem (6.8) is the unconstrained convex optimization problem, the optimal solution can be obtained by solving the following conjugate gradient equation,

$$\frac{\partial f(\mathbf{w})}{\partial \mathbf{w}^*} = 0 \tag{6.10}$$

Thus,

$$\mathbf{w} = \left(\mathbf{A}[\theta_0]^H \mathbf{A}[\theta_0] + \lambda_1 \sum_{\theta=\theta_1}^{\theta_2} \mathbf{A}[\theta]^H \mathbf{A}[\theta] + \lambda_2 \sum_{\theta\in\Omega_\theta} \mathbf{A}[\theta]^H \mathbf{A}[\theta] \right)^{-1} \mathbf{A}[\theta_0]^H \mathbf{p}[\theta_0] \tag{6.11}$$

The simulation setting is $M = 16$, $\theta_0 = 0^o$, $\theta_1 = -61^o$, $\theta_2 = -51^o$, $\lambda_1 = 1$, $\lambda_2 = 0.0001$, $d = 20cm$ and the number of taps in each filter is 160. The modulus of each entry in $\mathbf{p}[\theta_0]$ is 1 and the phase is linear phase. The simulated wideband beam is shown in Fig. 6.4.

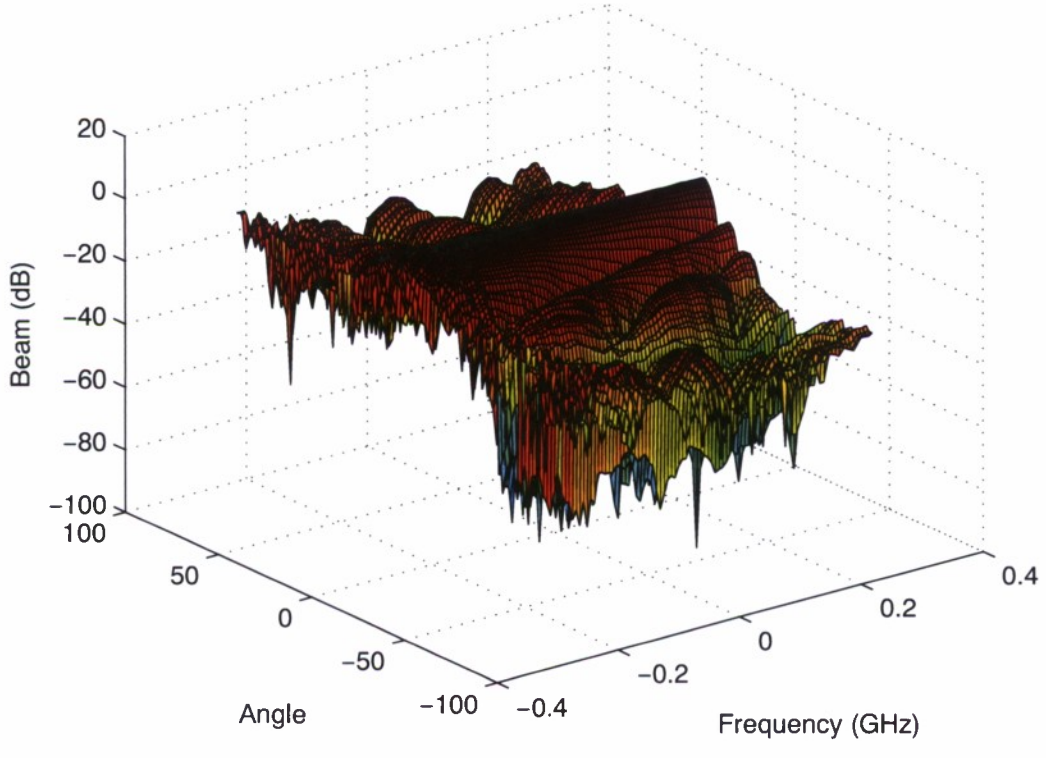


Figure 6.4: Wideband Beamforming

Part IV

Appendix

Wideband Coherent RF Front-End–Device Test

To build a coherent receiver front-end, a wideband quadrature demodulator ADL5380 from Analog Devices has been chosen. The performanee has been tested using its evaluation board ADL5380-29A-EVALZ for operation from 3GHz to 4GHz. As a building block, a baseband amplifier AD8366 from Analog Devices has also been introduced.

The ADL5380 is a high performance quadrature I-Q demodulator that covers an RF input frequency range from 400 MHz to 6 GHz, With typical values NF = 13dB, IP1dB = 12dBm and IIP3 = 31dBm at 2.5GHz, the demodulator offers good dynamic range suitable for the demanding infrastructure direct-conversion requirements. The ADL5380 provides a typical voltage conversion gain of 4dB, helping minimize the gain requirements of the receiver front cnd.

Fig. 6.5 shows the diagram of the evaluation board schematics, where the differential RF inputs provide a well-behaved broad-band input impedanee of 50Ω and be driven from a 1:1 balun for the best performanee. For the LO input interface, a 1:1 RF balun that converts the single-ended RF input to differential signal is used.

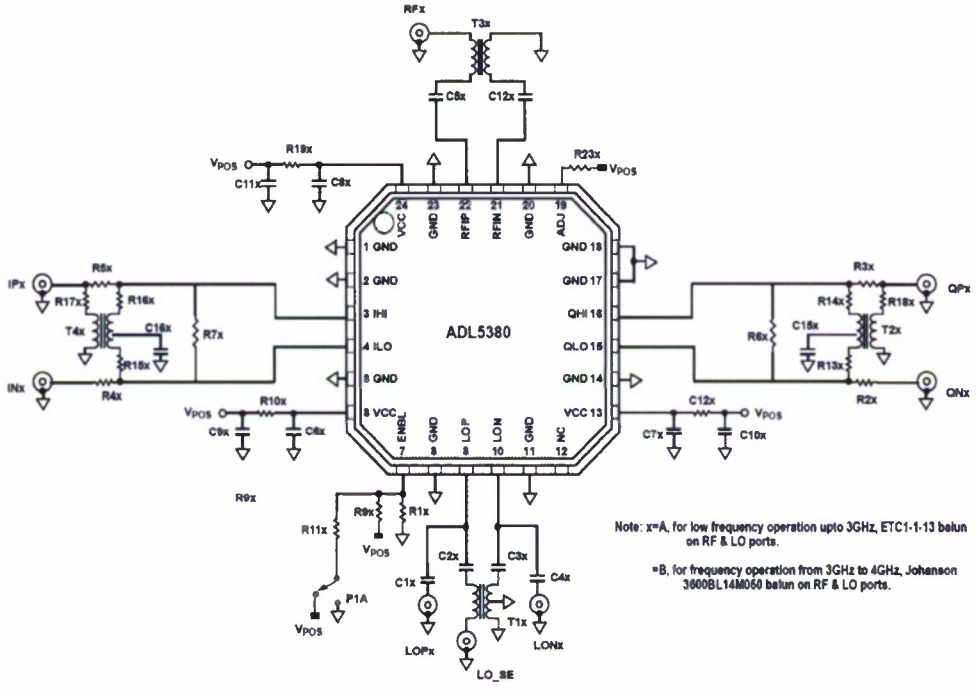


Figure 6.5: Diagram of ADL5380 Evaluation Board.

The baseband output of the evaluation board can be configured to Single-Ended output or full differential outputs. The original baseband outputs are from pins IHI, ILO, QHI and QLO in differential format. For single-ended output, the balun TCM9-1 converts a differential high impedance IF output to a single-ended output, and resistors R13x to R18x are populated for an appropriate balun interface. When loaded with 50Ω, this balun presents a 450Ω load to the device. By populating resistors R2x to R5x with 0Ω and not populating R13x to R18x, the the TCM9-1 transformer is bypassed to allow for differential baseband outputs. The default baseband outputs are differential not single-ended as the datasheet says.

Setup for the quadrature demodulation is shown in Fig. 6.6. At the transmitter side, the in-phase and quadrature baseband signals are generated by the DAC's waveform memory, then the signals are up-converted by the quadrature modulator ADL5375. The Local oscillator provide a 3.3 GHz carrier frequency for both the modulator and demodulator, where a power splitter is used. The modulator and demodulator are connected by a SMA cable to ensure appropriate RF signal level. A few test parameters are listed below.

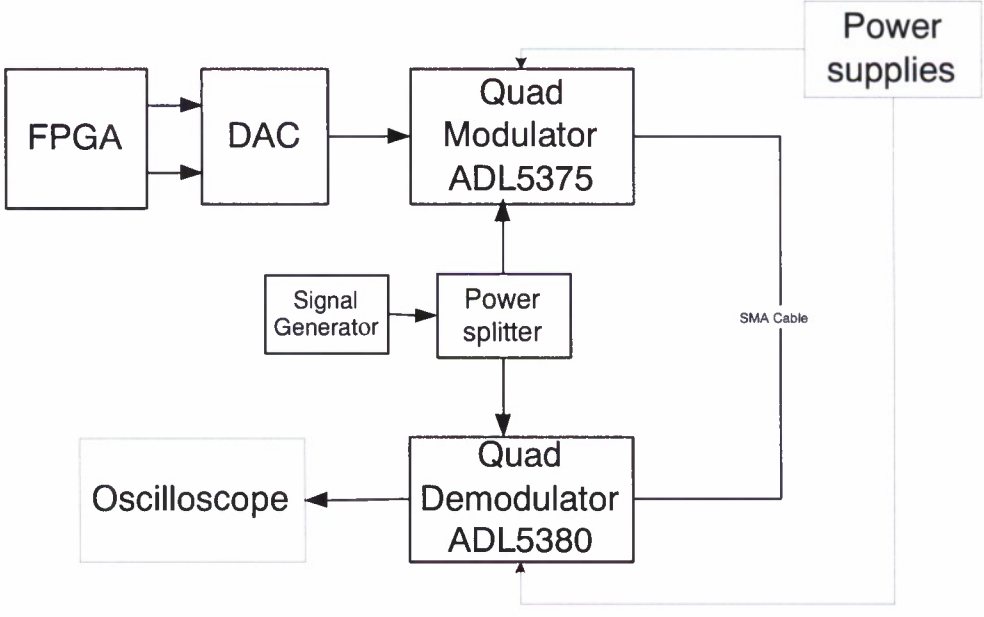


Figure 6.6: Testing setup for ADL5380 Evaluation Board.

1) LO signal generator output: 3.3GHz, 9dBm.
2) LO power splitter input: 3.3Ghz, 4.83dBm, Vpp at 1.104v, (Because of cable loss)
3) LO ADL5375 input: 3.3Ghz, -0.5dBm, Vpp at 592mv, (Power splitter attenuation and cable loss)
4) DAC CLK input: 550MHz.
5) DAC waveforms: sine_1024_14b.vec and ramps_1024_14b.vec.
6) RF ADL5375 modulator output: Vpp at 552mv.
7) Baseband ADL5380 demodulator output: VPP at 272mv.

Fig. 6.7 shows the modulator's output when transmitting sine waveform both on I-phase channel and Q-phase channel, Fig. 6.8 is the corresponding demodulation results when transmitting both sine waveforms on I-phase channel and Q-phase channel. Fig. 6.9 is the corresponding demodulation results when transmitting sine waveform on I-phase channel and ramp waveform on Q-phase channel. All these results show that the demodulator is working

properly.

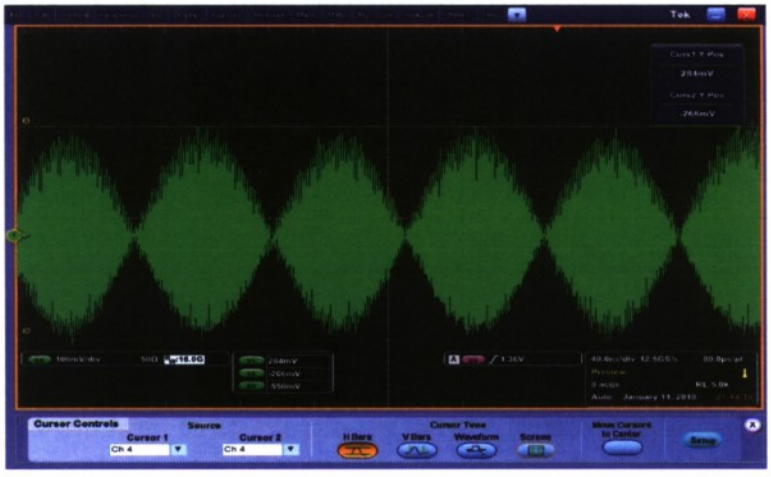


Figure 6.7: Modulator's output when transmitting both sine waveforms on I-phase channel and Q-phase channel.

The companion AD8366 is the industry's first dual-channel digital gain trim amplifier (DGTA) and is designed to enable, integrate and cost reduce direct conversion radio receivers. The combined two-chip solution, as Fig. 6.10 shows, can reduce the active component count by 60 percent within a radio design, providing considerable board area and bill of material (BOM) savings.

The AD8366 has a 0.25 dB step over 4.5 to 20.5dB gain range, it is ideally suited for analog I/Q quadrature ADC driving, maintaining excellent quadrature accuracy for direct conversion radio receivers. The fine gain control allows flexible and precise tuning of gain-critical to multi-standard and wideband radio receivers. Additionally the AD8366 features include adjustable output common mode for matching to ADC input ranges, and DC output offset correction loops to minimize demodulator DC offsets. The AD8366 is fully specified for direct conversion receiver designs capable of handling the widest of signal bandwidths with the lowest distortion. For example, the AD8366 supports the second and third harmonic distortion >88 dBc for 10 MHz signals at max gain.

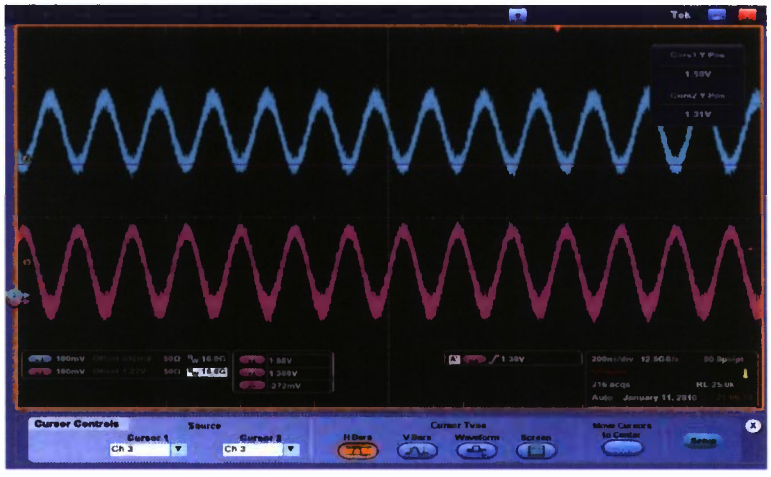


Figure 6.8: Demodulation results when transmitting both sine waveforms on I-phase channel and Q-phase channel.

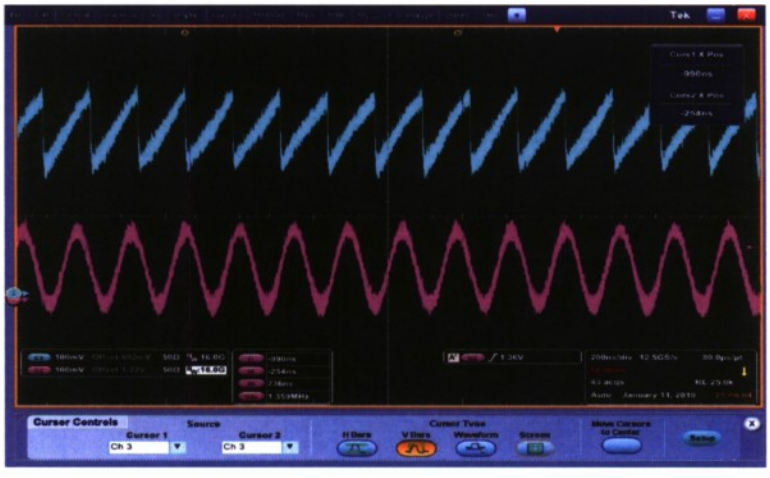


Figure 6.9: Demodulation results when transmitting sine waveform on I-phase channel and ramp waveform on Q-phase channel.

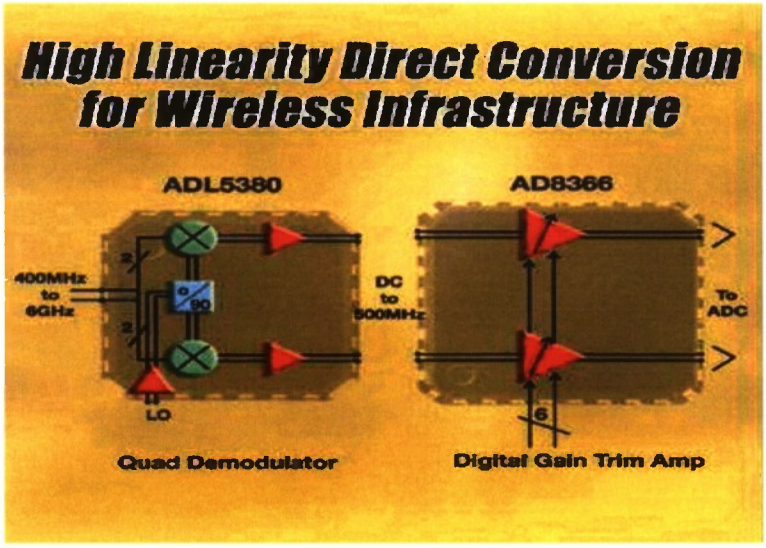


Figure 6.10: Architecture of ADL5380 and AD8366 combined solution.

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