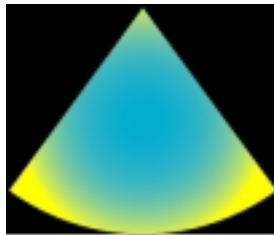




SONOELECTRONICS PROGRAM  
**LOW-POWER,  
HIGH-RESOLUTION  
3D SONAR IMAGING SYSTEM**



**TERATECH**

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# Report Documentation Page

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## SONOELECTRONICS PROGRAM

# LOW-POWER, HIGH-RESOLUTION 3D SONAR IMAGING SYSTEM

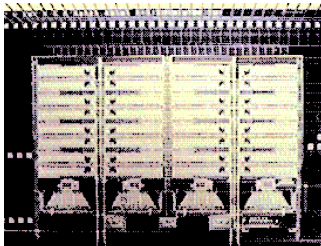


## OBJECTIVE

- DEVELOP HIGH-RESOLUTION, LOW-POWER LOW-COST, HAND-HELD SONAR IMAGER BASED ON SPARSE ARRAY CONCEPT
- 128 X 128 PIXEL IMAGE @ 400 (2D) FRAMES/s or 4 (3D rendered) FRAMES/s WITH 1 cm CROSS-RANGE & DOWN-RANGE RESOLUTION
- FULLY-INTEGRATED ELECTRONIC BEAMFORMING

## ACHIEVEMENTS

- WIDEBAND SPARSE ARRAY SIMULATION with 40 dB SIGNAL-TO-SIDELobe RATIO
- PROCESSING/COMPONENT DEVELOPMENT 32-CHANNEL 1D TIME-DOMAIN BEAMFORMING 5 BILLION OPs/s @ 1 WATT
- 1D-SPARSE-ARRAY DELIVERED TO NUWC; DATA OBTAINED IN NEWPORT, RI TEST FACILITY



## APPROACH

- STATE-OF-THE-ART 2D SPARSE ARRAY (TETRAD)
- BANDWIDTH SELECTION IMPROVING SIGNAL TO SIDELobe RATIO (NUWC)
- LOW-POWER, HIGH-THROUGHPUT CHARGE-DOMAIN ELECTRONIC BEAMSTEERING/BEAMFORMING (TERATECH)
- ICs MANUFACTURABLE IN CMOS FOUNDRY (TERATECH)

## MILESTONES

- SPARSE ARRAY WITH 32 ACTIVE ELEMENTS (7/99)
- SPARSE ARRAY WITH 128 ACTIVE ELEMENTS
- 128-ELEMENT SUBARRAY MODULE DEMO
- 20X20 cm 2D SPARSE ARRAY WITH ELECTRONIC BEAMFORMING
- 20X20 cm 2D SPARSE ARRAY WITH ELECTRONICS SYSTEM DEMONSTRATION

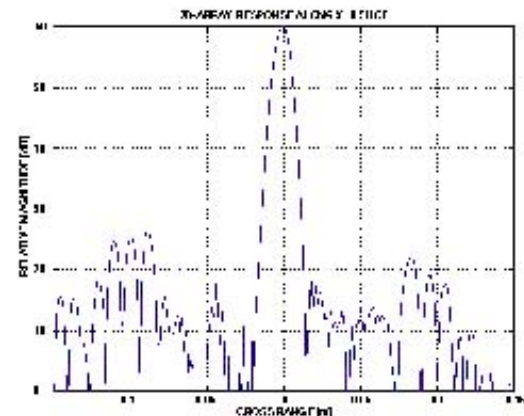
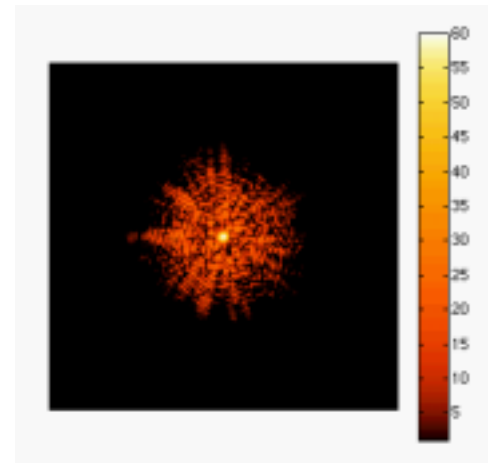
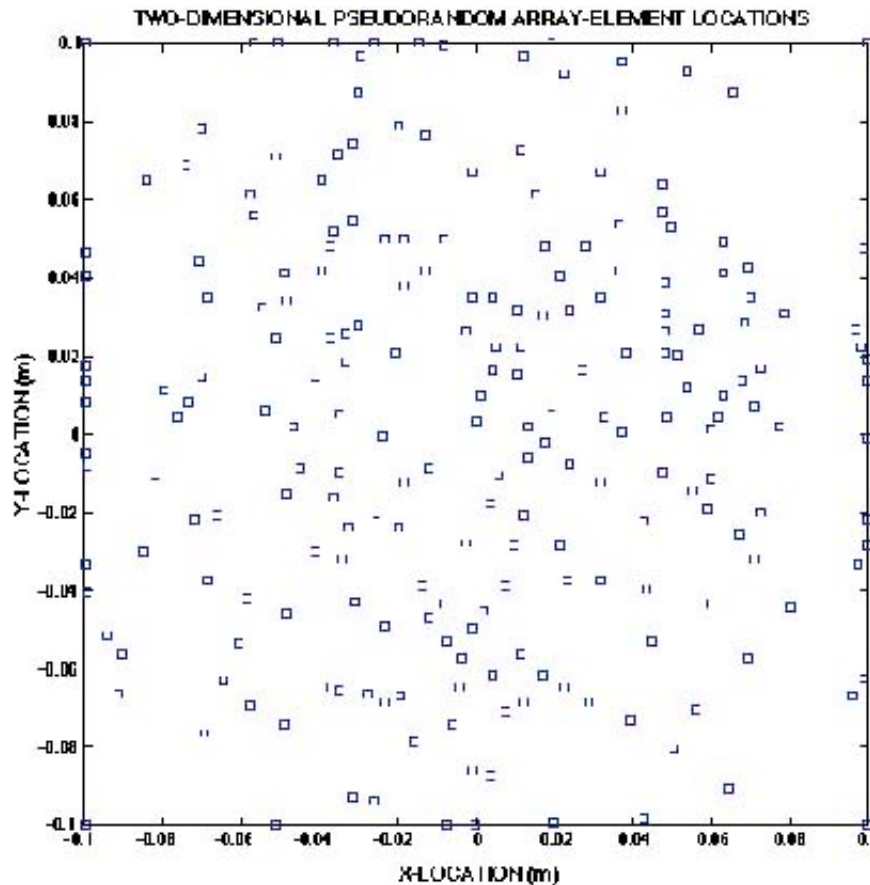


# SONOELECTRONICS PROGRAM 2D SPARSE-ARRAY OPTIMIZATION



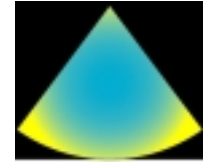
## •WIDEBAND SPARSE-ARRAY OPTIMIZATION

- WIDE BANDWIDTH, RANDOM PLACEMENT FOR IMPROVED BEAM PROFILE
- 40 dB SIGNAL-TO-AVERAGE SIDELOBE RATIO AND 30 dB SIGNAL-TO-PEAK SIDELOBES





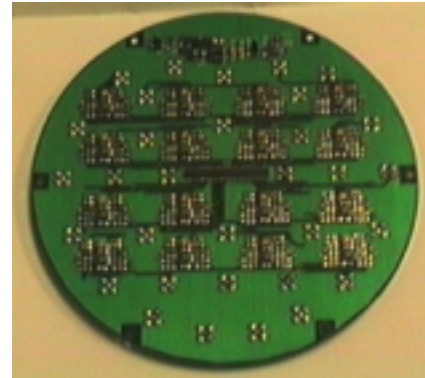
# SONOELECTRONICS PROGRAM 1D SPARSE-ARRAY SONAR SYSTEM



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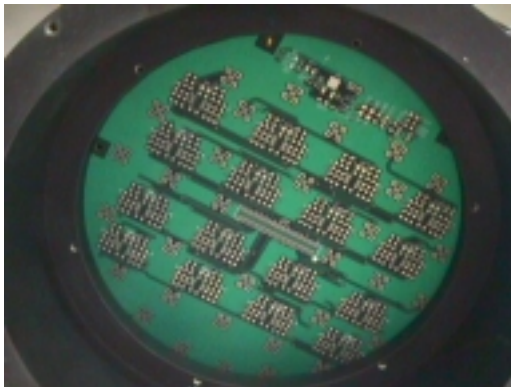
## •WIDEBAND 1D SPARSE-ARRAY

- ELEMENT-PLACEMENT OPTIMIZATION ALGORITHM YIELDS >20 dB SIGNAL-TO-PEAK SIDELOBES
- PROVIDES VERIFICATION OF WIDE BANDWIDTH, 2D-ARRAY



## •1D SPARSE-ARRAY AND ELECTRONICS EVAL SYSTEM

- 32-ELEMENT, 20 cm ONE-DIMENSIONAL ARRAY MATED TO CUSTOM PC BOARD
- 32-PREAMPLIFIER OUTPUTS CONNECTED TO DRY-END DATA ACQUISITION PLATFORM - NUWC

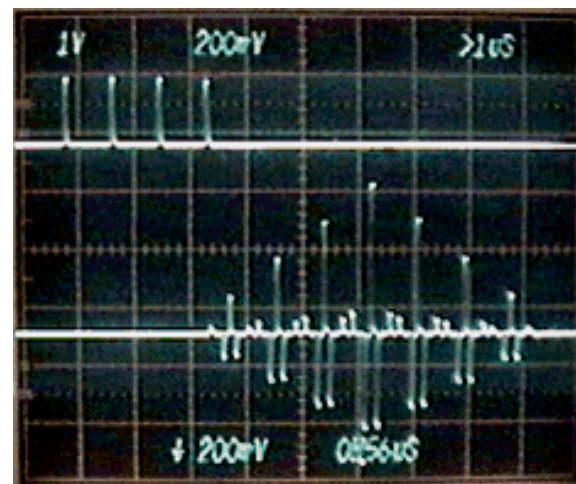
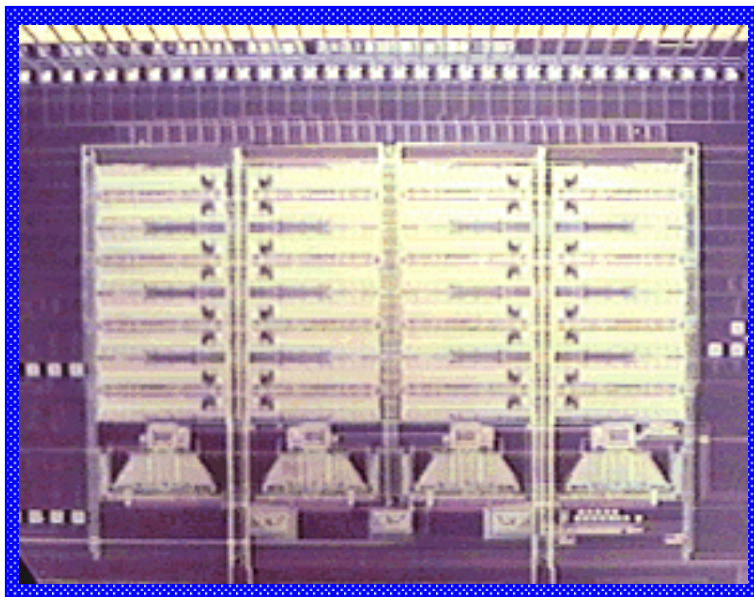




SONOELECTRONICS PROGRAM  
**32-CHANNEL, CCD/CMOS  
ELECTRONIC BEAMFORMER**



**FULLY-PROGRAMMABLE, APODIZED, DELAY LINES  
WITH ON-CHIP BANDPASS FILTER**



**5.5 BILLION OPs/s @ 1 WATT POWER DISSIPATION  
CHARGE-TRANSFER INEFFICIENCY  $< 1.39E-4$   
AT 20 MHz CLOCK RATE**