VARIABLE SWING OPTIMAL PARALLEL LINKS –

MINIMAL POWER, MAXIMAL DENSITY FOR PARALLEL LINKS

by

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A dissertation submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering

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To my superhero, to my role model, to my best friend, to the one who always makes me laugh, to the cutest person I know, to the most beautiful person I have met, and to the loving memory of Ata.

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ABSTRACT

The rapid growth of chip-to-chip interconnect density, speed, and the demand for smaller and more portable devices has taken signal integrity engineers to the limits of PCB (Printed Circuit Board) design. Special care has to be taken in the design stage to guarantee that noise specifications are met and power specifications and geometry of the links ensure minimal crosstalk noise in the system.

In parallel links, specific parameters of layout geometry are dictated during the design stage to meet noise requirements, generally increasing the space between channels to minimize crosstalk noise. This step determines and fixes the characteristic impedance of the lines and the induced crosstalk among them. Given that design planning is done to ensure that all specifications are met in the worst case scenario, the lack of layout freedom leads to a waste of space in high-speed systems. With the increasing interconnect density, a waste of power and space can no longer be afforded.

The work presented in this dissertation provides a novel technique to minimize the crosstalk in parallel links by the use of anti-coupling capacitances between adjacent links using an onboard accelerated Bit Error Rate (BER) testing technique. With this methodology, the channels can be routed as close as possible minimizing the space needed. The methodology automatically optimizes the values of the capacitances so that noise specifications will be met.

The designed receiver also allows the algorithm to adjust the termination resistance to minimize the reflections based on accelerated BER measurements. After

both optimizations have been done, each differential pair on the parallel link can be treated as a serial link, allowing a per-link power optimization using accelerated BER measurements.

Testing and simulation platforms were built to test the algorithm in a multilink environment and the developed technique is fully explained. This dissertation describes the algorithm, testing and simulation platforms used, and the methodology and results of the algorithm applied to a parallel link configuration.

Simulation results showed an improvement of up to 87% in crosstalk noise power between two differential pairs routed as close as possible. And previous work on power optimization showed a 10X power savings. Combining these two components, a higher bandwidth-per-unit-area can be achieved, while minimizing power consumption of the interconnect. This optimization provides a simple and efficient solution to mitigate two of the main problems of interconnects nowadays: Power and Space.

Chapter 1

1 INTRODUCTION

As the size of electronic devices shrink and mobile devices continue to take all the attention from users and manufacturers, the requirement for higher data rates using less power has become a must. The development of battery operated devices requiring integrated multimedia, bigger and higher definition displays, among other high data consuming peripherals, increases every year. This trend is seen in the cell phone industry, which traditionally have been the top developers of mobile devices. However important CPU manufactures, like Intel Corporation, have also started to design smaller and more power aware CPUs [1]. Mobility is nowadays a key in the design of electronic devices.

This increasing trend in the use of more power aware devices pursuing higher computational capabilities implies an increase in the number of system components that need to communicate with each other, an increase in the transfer rates used and an increase in the number of signals that need to be wired around the system [2]. Thus, interconnect designers are facing two challenges. First, obtain a design that reduces power consumption to the lowest possible level. Second, produce schemes that can transmit at high data rates in a limited physical space.

This dissertation describes the design of a parallel link interconnect that addresses both of this issues. The design provides an algorithm which dynamically adjusts transmission power of the interconnect, while maximizing the density of the parallel link. The interconnect can use the minimum spacing between channels while

keeping the crosstalk to an acceptable level. This is achieved by inserting anti-coupling capacitance between adjacent channels. The algorithm achieves a 78% decoupling between two differential transmission lines which is as good as having the lines spread apart without paying the overhead in spacing. Once the lines are isolated, the power optimization algorithm developed by J. Kramer [3] can be applied to every single line in the parallel link. The algorithm will be described in Chapter 2 since it gives the basics for the optimization algorithm developed in this dissertation.

Using the methodology for power reduction in a serial interconnect [3], the focus of this work is to extend it by targeting higher data transfers or applications that require a parallel (multilink) communication. Even though SERDES (serializer-deserializers) are being highly used nowadays to minimize the size of the devices, the physical limit of the PCBs restrains the serial speed that a link can take, thus requiring the use of multilink interconnects.

However, placing links close to each other, originate Signal Integrity problems. Specifically, close by links interfere with each other, reducing the quality of data transmission. Signal Integrity analysis is the field studying the problems that arise in high speed designs due to interconnects. It describes how electrical properties of interconnects, interact with the high speed signals and how it can affect the overall performance of the system. It can be grouped into 4 different categories: Signal quality of the net, crosstalk between adjacent lines, rail collapse in the power and ground distribution, and electromagnetic interference and radiation from the entire system [4]. In the scope of this work, which attempts to solve the need for smaller factor while maintaining a high speed and minimum power consumption, we will focus on crosstalk and the electromagnetic interference assuming that signal quality on

the net is good, meaning that there are no impedance mismatches through the net, and that there is no rail collapse in the power and ground distribution.

Until now, the most important solution from signal integrity point of view for the crosstalk has been to spread apart adjacent channels so that, for a given transmission power, there is negligible crosstalk. This thesis presents a proposed solution to the crosstalk and reflections using an accelerated BER testing algorithm and a set of anti-coupling capacitors that reduce the crosstalk by up to 78%.

With this methodology and the use of a power optimization algorithm, merged in one design, interconnects can improve in the use of the two scarcest resources nowadays in circuit design: Power and Space.

1.1 State of the Art of Signal Integrity

Many Signal Integrity problems are directly related to dV/dt or dI/dt; faster rise time significantly worsens some of the signal integrity problems such as ringing, crosstalk, and power/ground switching noise; decreasing the signal to noise ratio of the system.

Many studies have been done to model not only the transmission line itself but also the signal integrity issues in transmission lines [5] [4] [6] [7] and in differential transmission lines [8]; based on this models, alternative transmission lines have been also developed, different solutions like flexible interconnects for mobile devices [9] have also been studied.

One of the main problems in signal integrity occurs when two lines are routed closely: crosstalk, which is caused by electromagnetic coupling between multiple transmission lines, generates noise on the adjacent quiet lines that may lead to false logic switching. The amount of crosstalk is related to the signal rise time, to

the spacing between the lines, to the spacing between the lines and the return plane and to actual length of the lines. Simulations models for crosstalk in time domain [10] [11] and in frequency domain [5] [12] have been studied in the past. Some simulation models using the widely used simulation tool: Pspice have also been developed [13] and main CAD tools like Cadence, Synopsys, Ansoft include signal integrity analysis tools based on W-Elements or S-Parameters in their products.

The modeling and simulation tools developed have leaded to investigate ways to control or minimize this signal integrity effects on the system, the models give guidelines to analyze the signal integrity problem and nowadays its analysis is getting a higher role in any high speed design flow.

To control the crosstalk, one can make the lines space apart, add ground guarding band in between the signal lines, keep the parallelism to minimum, and keep the traces close to the reference metal planes. Many optimizations based on those parameters have been done in the past to minimize crosstalk issues; most significant findings are described below:

Some early works present a guideline for PCB designers to avoid crosstalk as the one presented in [14] where the author gives a series of design rule of thumbs to minimize the effect of crosstalk. [15] also presents a similar approach and advises to follow layout rules for transmission lines to enhance board operation: avoid 90° turns and use arcs or 45° bevels. Keeping the distance between two traces constant in order to avoid discontinuities in differential impedance also enhances the signal quality on the net. Avoid the use of vias in the transmission lines is also suggested.

In other approaches, like in [16], the authors use a stochastic model for global signal wiring, a new model for global power/ground wiring area, a global clock

bandwidth requirement, and a crosstalk noise requirement to implement an optimization of the architecture of the global signal, clock, and power/ground distribution networks of a system-on-a-chip. A similar work found in [17] determines the optimal combination of free parameters that maximizes the Signal Integrity of the channel; the measurement of improvement is the eye diagram of the communication. This work takes into account all free parameters, like packaging and termination resistance to optimize the eye opening.

The authors in [18] presented a formulation for the average power dissipated by interconnects. The power model accounts for signal and temporal correlations when computing effective capacitance. The authors also modeled the maximum crosstalk effects between neighboring wires to reflect the aspects logical of Domino Logic as well as electrical factors. Based on the coupling power model and the maximum crosstalk model, the authors optimize the coupling power by using track perturbation; gridded channel routing is specifically considered in their work. The objective of track assignment is to minimize the effective coupling capacitance in order to reduce coupling power, while satisfying all the constraints.

Different topologies than the classical planar structure had also been studied like the proposed in [19] where the authors proposed a novel technique for achieving high density on-chip bus lines using differential transmission lines and had shown a high-density, crosstalk-robust and high-speed bus line on-chip. This technique although delivered great outcomes, results difficult to implement in a PCB because it uses 3D approach to eliminate crosstalk.

The optimization of signal integrity effects showed in [20], based on numerical inversion of Laplace transform (NILT) finds a gradient based minimax

optimization, that integrated with a proposed sensitivity analysis technique, demonstrates the feasibility and practicality of the physical/geometrical oriented interconnect.

Another optimization method studied in [21], also intends to minimize the crosstalk and optimize the CMOS power by an algorithm based the switching activity of the cell. The algorithm automatically optimizes the position and length of every single wire segment in a routed design depending on the swithching activity found for the specific net.

The work showed in [22] shows a multi-channel ACCI that provides 36Gbps over a six-bit wide bus, it uses a fully differential receiver and a 4X spacing between channels that combined with a RZ signaling minimizes the effect of crosstalk and noise induced by adjacent channels.

The authors of [23] study as an alternative the use of optical surface-plasmons (SPs) propagating on metallic structures. In that study, the authors show that electrical interconnects force a trade-off between signal delay and the interconnect density to avoid crosstalk. But their study on SP waveguide interconnects force a trade-off between energy per bit and interconnects density.

The work described in [24] implemented a method to quantify the amount of crosstalk-induced jitter from the mutual capacitance and inductance between two adjacent lines. Based on the mathematical derivation of crosstalk induced jitter, it proposes a jitter equalization technique that induces a data dependent delay to compensate for crosstalk jitter.

As described above, until now all the work done to minimize crosstalk includes the modification of the physical parameters of the transmission lines,

generally increasing their size or finding a tradeoff between space and speed and allowed crosstalk. The methodology described in this dissertation approaches the crosstalk issue by keeping the minimum spacing between channels and adding an anti-coupling set of capacitors that effectively minimizes the crosstalk without decreasing the interconnect density.

1.2 Contributions and Overview of this work

This dissertation presents a solution for two of the main problems that interconnect designers and signal integrity engineers overcome when working with high speed buses: Power savings and Signal integrity issues (Reflections and Crosstalk). The use of the algorithm developed leads to the maximum power savings for all links in the bus and also achieves up to 87% of crosstalk reduction for short links using the minimum spacing on the signal routing. Thus, this algorithm minimizes the power and maximizes the density on a parallel link.

The rest of this dissertation is organized as follows. Chapter 2 presents the serial version of the VSMPL – Variable Swing Minimal Power Link – algorithm which is the base for the VSOPL – Variable Swing Optimal Parallel Links – algorithm. It describes in detail the inherit challenges on a parallel link configuration and the problems that arise when applying the serial VSMPL algorithm to them. It also presents a mathematical background on crosstalk modeling and provides the solution to minimize the crosstalk while still using the minimum spacing between adjacent differential channels. Finally it provides a complete description of the implementation of the optimization algorithm for parallel links.

Chapter 3 describes the testing platform and the simulation setup used to test and prove the algorithm. It describes in detail the platform in a system level and also describes each of the components: ASIC, PCB and simulation setup.

Chapter 4 presents the results obtained from both, simulation and testing platform. And finally, Chapter 5 concludes the dissertation with a summary of the work presented and the accomplishments and elaborates on future work that could be done to improve the performance of interconnects.

Chapter 2

2 DERIVATION OF THE PARALLEL LINK VSMPL ALGORITHM

This Chapter explains the optimization algorithm that achieves minimum power and maximum density in a parallel link communication. The algorithm uses an accelerated BER measurement, that allows interconnects to transmit data at the minimum required power to achieve a desired BER. The method takes advantage of the accelerated BER measurement to obtain an estimate of the interference induced by other lines in a parallel link. The anti-coupling capacitances are then tuned according to this estimate.

The organization of this chapter is as follows: Section 2.1 describes the serial version of the algorithm proposed by Joshua Kramer [3]. By using an accelerated BER measurement technique the algorithm can estimate the minimum power required for data transmission over a serial link. Section 2.2 discuses Signal Integrity problems arising when the algorithm is used in a multilink interconnect. A novel technique of using anti-coupling capacitances to minimize coupling between adjacent lines is described. Finally, in Section 2.3 the optimization of signal integrity and power is explained.

2.1 Power optimization over a serial link

The standards available today for interconnects have fixed specifications and power dissipation is usually dictated by the standard, which implies a suboptimal design in terms of power consumption. They are also usually designed for long

distance links; which evidently are not optimal for small factor devices. Thus, the power used by the driver exceeds link requirements, resulting in an enormous amount of wasted power.

Current optimization techniques, such as circuit optimization, can only go so far to optimize link power consumption. Furthermore, it is very difficult to predict the environment in which the circuit will work. Therefore, interconnect designers always account for a power guard band, making transmitted power suboptimal.

J. Kramer presented in [3] an accelerated bit error rate testing technique, which successfully optimizes power consumption based on simple on chip measurements. Using this method, a device can optimize the transmitted power for the link environment it is used in with minimal assumptions about the link. This methodology is especially applicable to power aware devices that use variety of links, each working in a different environment.

It was also shown that current-sense receivers are optimal for power consumption since the transmission power is not limited by the transmission line termination resistor. In that case the transmission power can become minimal according to the link's requirement. The approach combines the current-sense receiver and differential signaling to increase noise immunity, thus allowing lower swings and lower power consumption while also increasing operating speed

To determine how low the transmitted power can go, it is necessary to determine a target BER (Bit Error Rate) for the link. This method has been applied to wireless links [25], but it's implementation in electrical links requires an optimization since the environment for a wired link is typically better compared to a wireless link.

Although several accelerated measurement techniques have been developed [26] [27] [28]. The advantage of the work in [3] is that instead of modifying the noise power to increase the error rate, it modifies the signal power to increase the error rate. This removes the need for specialized circuitry to inject noise and relies instead on adjusting the transmitter power which in a power aware device is an already given feature.

The next subsections describe the VSMPL – Variable Swing Minimal Power Link – algorithm, derived for short length, serial link communications. It consists of a Bit Error Rate Measurement methodology described in Subsection 2.1.1 and a Dynamic Power Optimization methodology presented in Subsection 2.1.2. Subsection 2.1.3 presents the hardware implementation of the power efficient interconnect.

2.1.1 Bit Error Rate Measurement

The BER (Bit Error Ratio), as defined by Maxim [29], is a measure of the number of erroneous bits which can be expected in a specified number of bits in a serial stream. It is one of the most important measurements of a communication system performance; and can be expressed as:

$$BER \approx \frac{N_e}{B * t_0}, \qquad (2.1)$$

where, Ne is the number of erroneous bits measured, B is the data rate, and t0 is the total time interval for the measurement. This value is used as an approximation for the probability of error, P(e), for the link. The more bits received, thus, longer t_0 intervals, will give better estimates. It has been observed that around 10/P(e) bits gives a 95% confidence interval [27].

The most accurate measurements of the BER are performed by transmitting a known pseudorandom data sequence on the link and recording errors by comparing the received values with the sent values [27]. BER measurements for electrical links are extensively time consuming since the quality of electrical links is expected to be very good (BER in the order of 10^{-13}). A good measurement (high confidence level) for this order of magnitude at high speeds will require hours or days [27] therefore techniques for accelerated BER testing are required for fast and effective BER measurements.

As shown in [3], given that noise in electrical links can be modeled as Gaussian, the probability of having a 1 is equal to the probability of having a 0, and the noise is i.i.d. Therefore the error probability or BER is expressed as:

$$P_e = \frac{1}{2} erfc\left(\frac{D}{\sqrt{2}}\right), \tag{2.2}$$

Where $D = \frac{S}{2\sigma}$, S is the amplitude of the signal for a 1 symbol, and $\sigma_0 = \sigma_1 = \sigma$ is the noise standard deviation. From the equation is clear that the error probability is directly and only related to the signal to noise ratio (SNR) of the link. So to vary the error probability (or the BER), one can either decrease the signal strength or increase the noise power.

2.1.2 Single line VSMPL Technique

Various methods of quickly approximating the BER have been developed. Basic features of these methods are:

- Degradation of the link SNR to increase the error rate over the normal operating rate.

- A means of measuring this modified error rate for different degrees of link degradation.
- A method of extrapolating these measurements to approximate the non-degraded rate

VSMPL technique is based on a sinusoidal interference erfc approximation technique, which basically, by applying noise to the system and by approximating the erfc function, gets the following linear relation between the pseudo-error rate and the amplitude of the sine wave:

$$\psi\left(P_e\right) = D - \rho = \frac{-c_2 + \sqrt{{c_2}^2 - 4c_1\left(c_3 + \ln\left(2P_e\right)\right)}}{2c_1} \tag{2.3}$$

A straight line fit of the $\psi(P_e)$ measurement can be extrapolated to zero sinusoidal interference for the approximate value of D. From this fit, the approximate BER for the link can be calculated [3].

VSMPL method adjusts the transmitter power instead of adding noise to the signal. The first advantage of this change in methodology is that to add noise requires additionally circuitry whose only purpose is to degrade the signal while the circuitry to change the transmitter current is typically built in for the additional purpose of power saving. Secondly, since the extrapolation in the method is done based on the transmitter power, the approximate BER for a range of power settings can be calculated as opposed to the other method which gives it for a range of noise power [3].

It can be shown that when the variation parameter is the signal strength, then the new $\psi(P_e)$ function is given by:

$$\psi(P_e) = \frac{S-\xi}{\sigma} = \frac{-c_2 + \sqrt{{c_2}^2 - 4c_1\left(c_3 + \ln\left(2P_e\right)\right)}}{2c_1} \tag{2.4}$$

Figure 2.1 shows the graphical relation between $\psi(P_e)$ and BER [3].

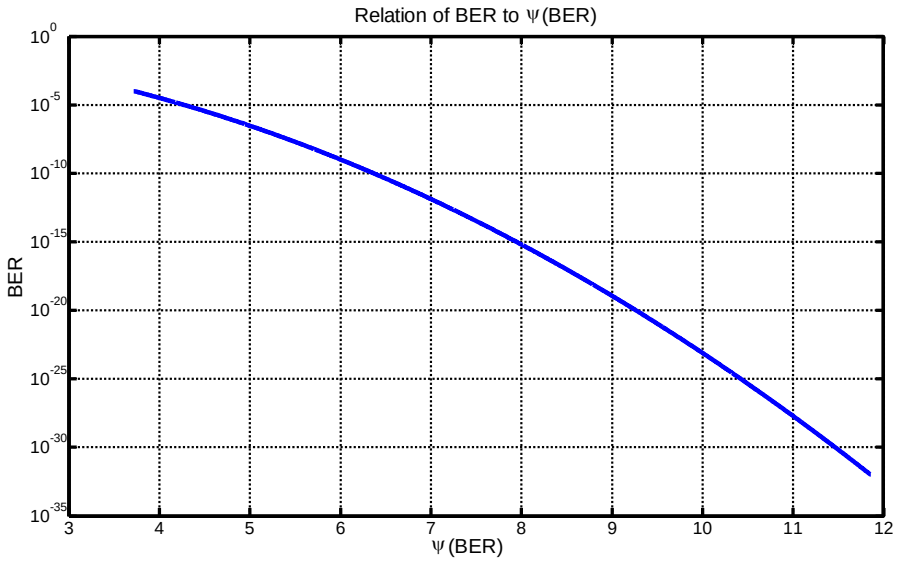


Figure 2.1 - Relation between BER and Pe function; for the range of BER of interest this relation can be approximated as linear [3].

Using the result in (Eq. 2.4), a testing methodology for optimizing the transmitter power based on the approximated value of the link BER was presented. The optimization strategy can be summarized as follows:

- Set the transmitter power to the point that the channel BER is about 10-4, as this is the upper limit for the erfc(•) approximation.
- Step up the transmitter power and save the BER value at each step.
- Calculate the $\psi(P_e)$ for each data point.
- Fit a line through the data points.

- Solve for the transmitter power setting to provide the desired BER value.

2.1.3 Hardware implementation

Data transmission presents always a tradeoff between the power used to transmit a signal and the maximum distance that a signal can travel and the maximal achievable transmission rate. There are various standards for data transmission over a differential pair. As shown in Figure 2.2, each standard was designed with a particular application in mind. CML is used in cases where the length of the transmission line is a determinant design parameter. On the contrary, Whisper Bus was design to optimize energy consumption. Different standards differ from one another not only in the transmission power they use to transmit the signals, but also in the way in which they code data for transmission. Next a brief overview of the standards considered in this thesis is presented.

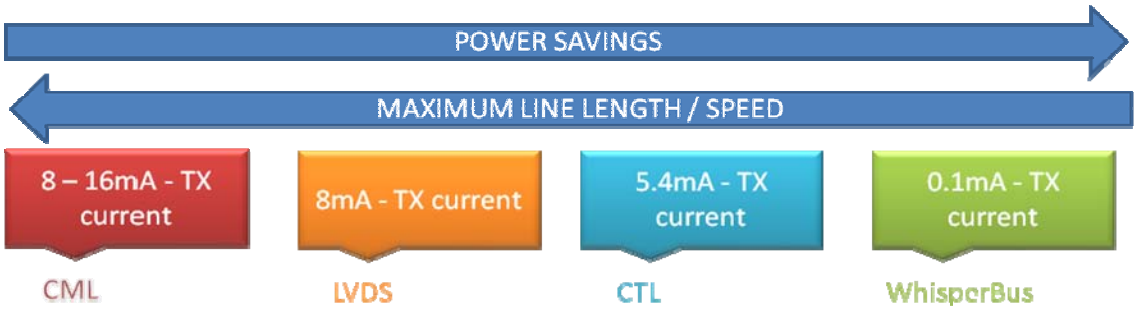


Figure 2.2 - Existing standards in the power/length/speed spectrum. Today's standards are fixed for a given power/length/speed specification; little flexibility is given to the interconnect designer to optimize power consumption for a custom design.

Low Voltage Differential Signalling

First introduced in 1994 by National Semiconductors, Low-Voltage Differential Signaling (LVDS) has become one of the most popular standards for high speed transmissions since there are no specific functional requirements. It was standardized by the Telecommunications Industry Association/Electronic Industries Association as the ANSI/TIA/EIA-644-A (LVDS) standard in 2001. The ANSI/TIA/EIA-644-A standard provides a theoretical maximum data rate of 1.923 Gbps, which assumes an ideal transmission medium. The standard also provides a maximum recommended data rate if it is run over twisted pair copper cables, 655 Mbps. If higher speeds are required, a parallel bus of LVDS links could be used [30].

An LVDS link, shown in Figure 2.3, consists of a differential transmitter, transmission line, termination resistor and receiver. The driver is a current-mode transmitter while the receiver is voltage mode. The current-mode transmitter consumes the same power across operating frequency. Figure 2.3 also shows a simplified schematic implementation of an LVDS CMOS transmitter.

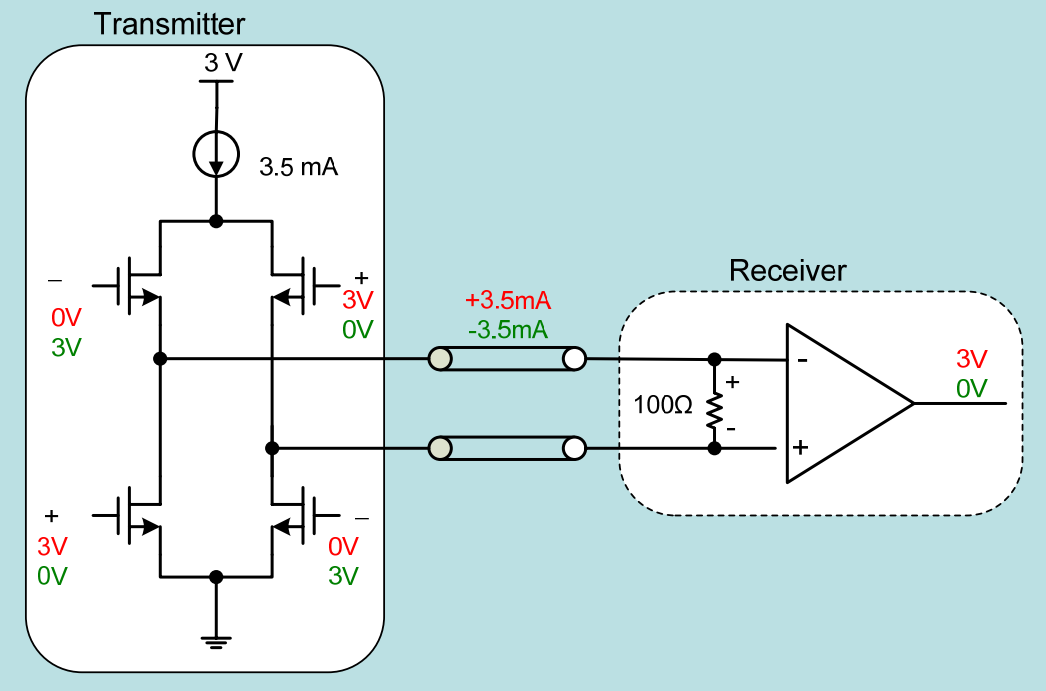


Figure 2.3 - LVDS link

CML – Current Mode Logic

As opposed to LVDS, current mode logic (CML) is a de facto standard in which the implementation is entirely up to the manufacturer [7]. Depending on the manufacturing process used, the serial signaling rate can range from 1 Gbps to higher than even 10 Gbps, the power consumption, increases as the data rate increases. While the typical transmitter current for LVDS is 3.5 mA, a CML link can range from 8 mA to 16 mA, depending on how the manufacturer chooses to implement it [3].

CML transmitter operates in current-mode. Figure 2.4 shows an example of a CML link as well as the simplified CMOS implementation of the transmitter. The

receiver on the other hand is a voltage-mode receiver, which amplifies the voltage generated across the termination resistor.

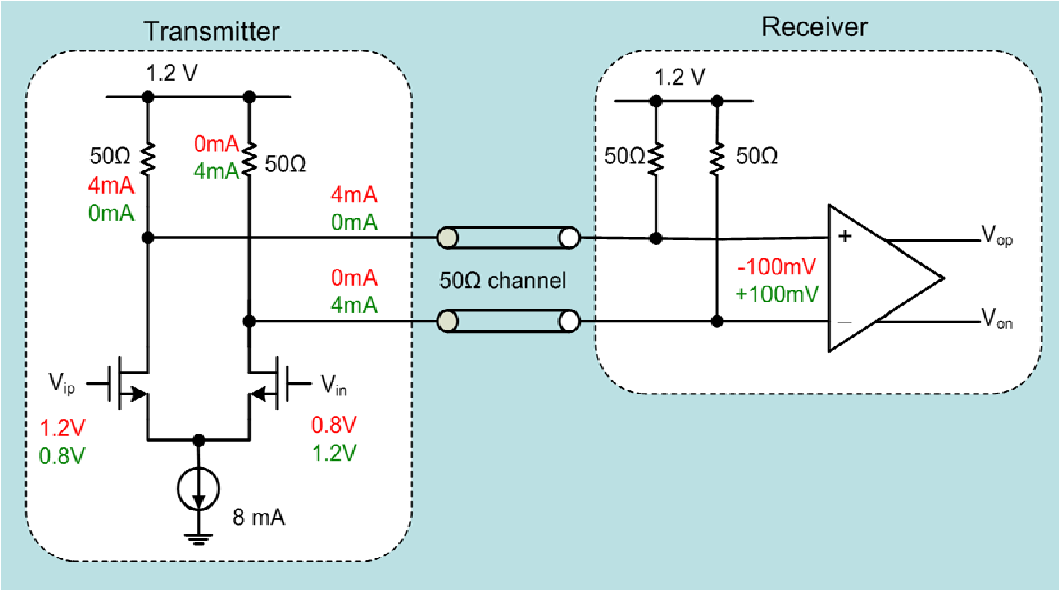


Figure 2.4 - CML link

Implementation of VSMPL Driver and Receiver

Figure 2.5 shows the basic concept for one side of the differential low swing link. The two important components in this design are the bipolar transistor in the common base amplifier (CBA) configuration and the amplifier connected to the base of the transistor. The CBA has low input impedance and high output impedance, thus functioning as an impedance transformer. This configuration effectively decouples the transmission line termination resistor and the current to voltage conversion resistor. Although the input impedance of the CBA is low, it is still on the order of 50 Ω. Since we can more accurately terminate the line with a separate

resistor, an amplifier is connected to the base of the transistor to reduce the input impedance of the CBA such that the termination resistor dominates the input impedance of the receiver. Our proposed architecture is designed in 0.12 µm SiGe technology that implements on chip transmission line termination and differential input to get an operation bandwidth of up to 10 Gb/s.

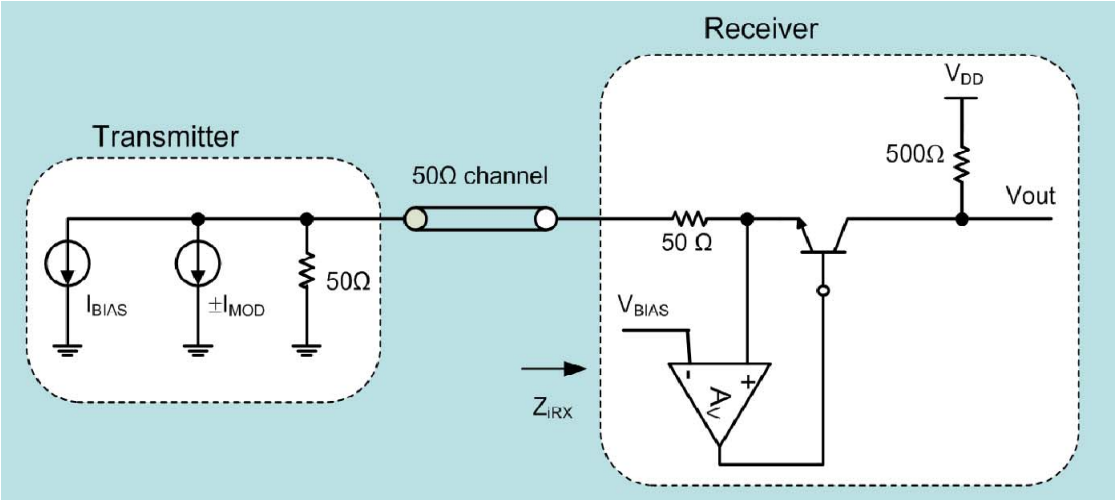


Figure 2.5 - Simplified schematic of one side of the differential VSMPL link. VSMPL is a current mode transmitter and current mode receiver which represents a power saving of up to 10X compared with voltage mode counterparts

A detailed schematic implementation of the differential receiver and transmitter circuits used in the test IC are shown in Figure 2.6 and Figure 2.7 respectively. A more detailed explanation will be given in Chapter 3.

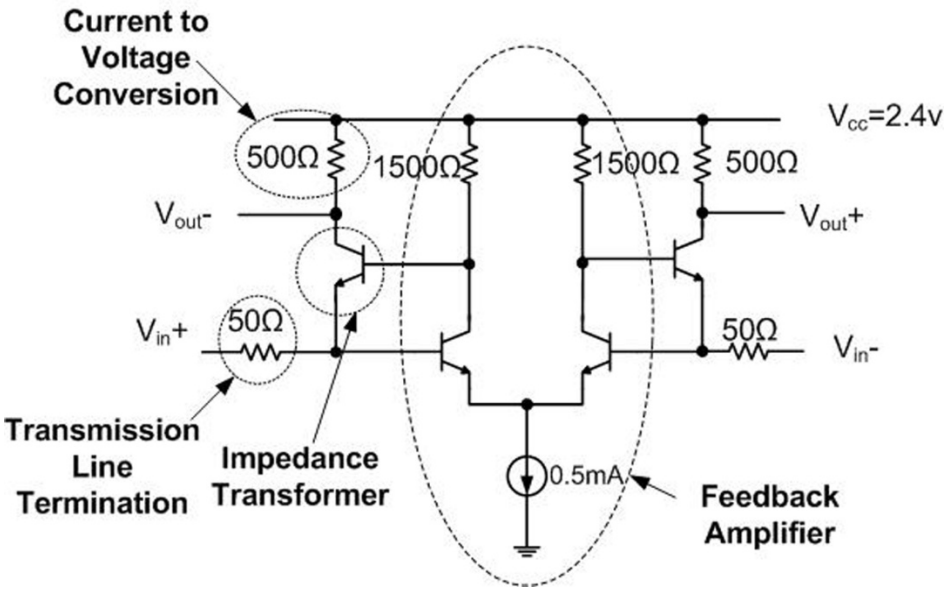


Figure 2.6 - Differential Low Swing Receiver. The current to voltage conversion occurs after the impedance transformer using the 500ohm resistor, therefore avoiding the need of extra amplification.

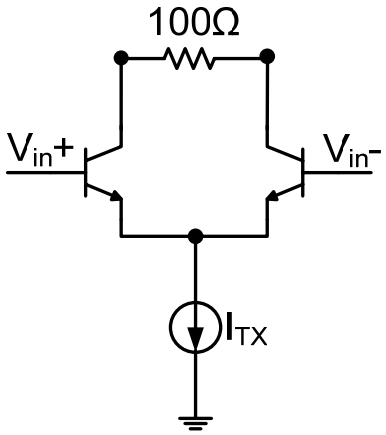


Figure 2.7 - Differential Low Swing Transmitter. Current mode transmitter is a simple differential pair with the termination 100ohm resistor.

2.2 Space optimization with multiple links

To implement an algorithm that dynamically adjusts its power based on a performance measurement in a multilink interconnect. e.g., the VSMPL algorithm described in the previous section, signal integrity issues have to be addressed first.

To see this, consider the case when the algorithm measures the BER in a single link L. The electromagnetic interference from other links or crosstalk will cause this link L to measure a high BER, indicating it has to increase its power to achieve the target BER. However, increasing the power in link L will induce more interference in adjacent lines that are also implementing the algorithm. Thus all other lines will then increase power to attempt to obtain the target BER, which in turn causes more interference in link L, make it increase its transmission power even more.

A solution to this problem would be to separate lines from each other to reduce interference. However to design the spacing between lines a reference power is needed. As VSMPL uses variable power, channels need to be separated according to the maximum power of the circuit to avoid interference, implying a bigger form factor of the device.

To understand the effects of crosstalk and to properly derive the optimization configuration, this section gives a background on transmission line modeling and differential transmission line modeling. After this discussion a solution using anti-coupling capacitances is described.

2.2.1 Transmission line modeling

An electrical model of an interconnect is often referred as its characteristic impedance. The characteristic impedance is directly related to the geometry of the interconnect. Models for different transmission lines geometries have been developed.

Among them, the microstrip in which the transmission line is above the ground plane, the stripline where the transmission line is between two power planes, and a wire pair which does not require a ground plane. A twisted pair is an example of this last configuration. Figure 2.8 shows the geometry difference among the configurations.

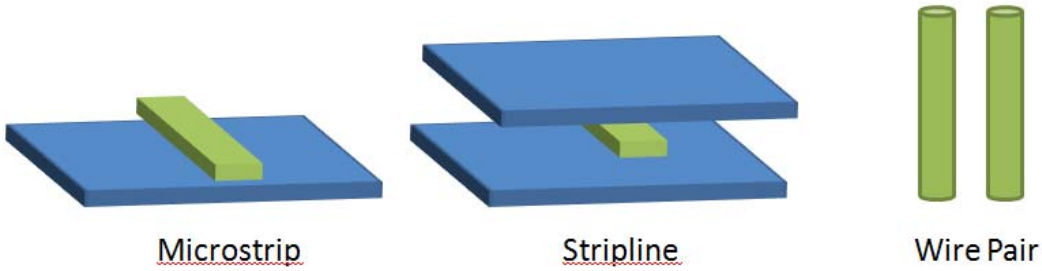


Figure 2.8 - Different transmission lines configurations. The work on this dissertation focuses on the microstrip configuration.

All the transmission lines have basic parameters such as per-unit-length R (resistance), L (inductance), G (conductance) and C (capacitance), unit-length time delay (inverse of the propagation speed), and characteristic impedance. For simple transmission line structures such as parallel-plate, these parameters can be analytically obtained. For other types of transmission line structures, usually a 2D static EM field solver (or some empirical formulas) is needed to obtain these parameters.

In general, an ideal transmission line can be modeled using infinite lumped devices, inductance and capacitances, as shown in Figure 2.9. There is a uniform capacitance per-unit-length C_L and a uniform loop inductance per-unit-length L_L. The total impedance of the transmission line is given by

$$Z_0 = \sqrt{\frac{L_L}{C_L}}. \qquad (2.5)$$

Time delay (TD) can also be obtained as a function of C_L and L_L: [4]

$$TD = Len * \sqrt{C_L L_L} = \frac{Len}{v}, \qquad (2.6)$$

where Len is the total length of the line and v is the transmission rate.

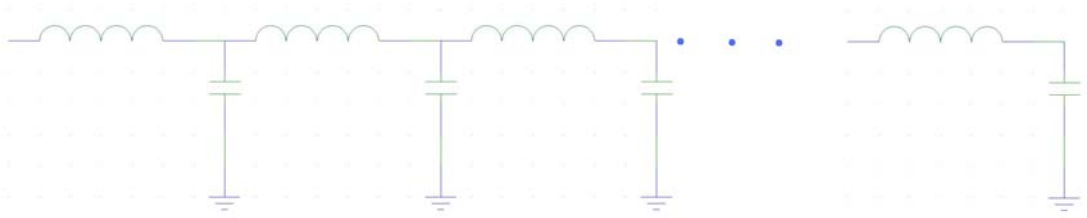


Figure 2.9 - Model of an ideal transmission line using infinite lumped devices

Since modeling an infinitesimal segment of the transmission line results impractical, a good approximation of the ideal transmission line can be obtained if the number of lumped devices (n) is calculated based on the bandwidth of the model (BW) and the time delay of the transmission line (TD). The number of lumped dices (n) for this approximation is [4]:

$$n = 10 * BW * TD. \qquad (2.7)$$

The calculations shown above assume that capacitance per–unit-length and inductance per–unit-length are known values. However as they are in terms of the geometry of the transmission line, to calculate the parameters for a specific configuration, signal integrity engineers need to use approximations or 2D/3D solvers.

This work focuses in the use of Microstrip configurations. This configuration has the advantage of simple implementation which lends to small structures. It also allows surface mounting the components on it, which minimizes the impedance discontinuities on the transmission line by avoiding the use of vias. Its main disadvantage is that given the geometry, it radiates high electromagnetic emissions, thus exhibiting a higher coupling and crosstalk in parallel link configurations.

Modeling the microstrip based on its geometry has been widely studied [6] [4] and all electrical characteristics are defined by: the width of the transmission line (w), the thickness of the conductor (t), the distance from the transmission line to the ground plane (h) and the effective relative permittivity of the dielectric between the transmission line and the ground plane (ε_r). All these parameters are shown in Figure 2.10.

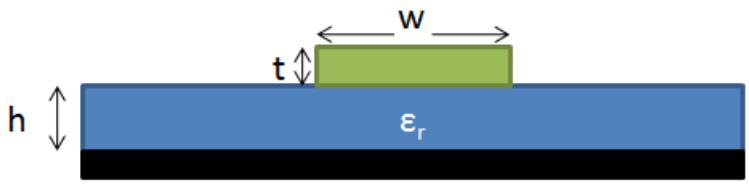


Figure 2.10 - Geometry parameters of the microstrip define electrical characteristics of this transmission line configuration.

An approximation to the characteristic impedance of the microstrip, based on its geometry, is given by

$$Zo = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right), \qquad (2.8)$$

and an approximation of its time delay is given by: [6].

$$TD = 85\sqrt{0.475\varepsilon_r + 0.67}\,. \qquad (2.9)$$

2.2.2 Coupled modeling of transmission lines

When the signal is propagating in the transmission line, it generates electric-field lines between the line and the return path and loops of magnetic field lines around the signal and return paths. The electric and magnetic fields generated by the line will affect the signal quality of the lines around it by adding undesired noise as shown in Figure 2.11.

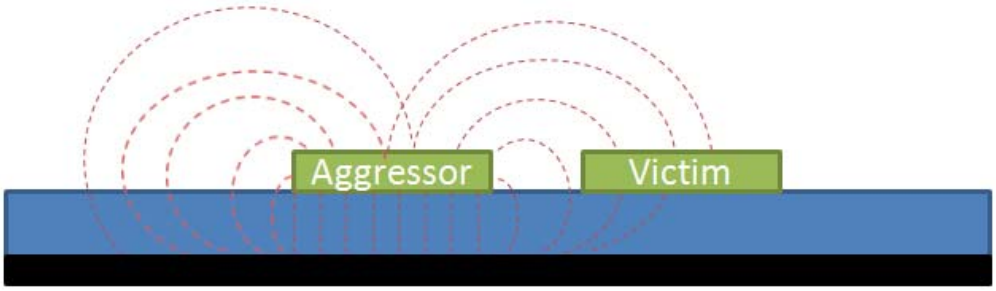


Figure 2.11 - Crosstalk in a victim line is due to electromagnetic fields generated by a close by aggressor

At this point, it is important to note that interconnects are linear and passive systems, therefore basic principles like superposition can be applied to them. It means that the noise generated from all nearby transmission lines will add to the

total noise measured at the line of interest. The line affected by the noise is typically called victim or quiet net and the source(s) of noise are called aggressor(s) or active net(s).

The coefficient of electrical fields interaction between two lines is modeled with a parasitic capacitance between them called mutual capacitance. And the coefficient of magnetic loops interaction is modeled with an inductor called mutual inductance and acts the same as a small transformer between the lines. The values of the mutual capacitance and the mutual inductance decreases as the lines are moved farther apart. Figure 2.12 presents the circuit model of one of the sections of an n-section lumped circuit model showing the coupling elements.

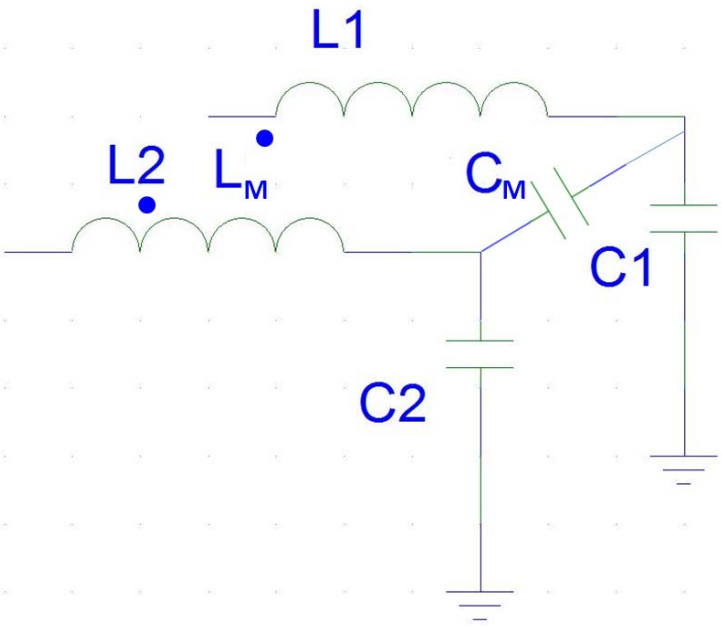


Figure 2.12 - One section of an n-section lumped circuit model. Electric and magnetic fields produce coupling among transmission lines, this coupling can be modeled using mutual capacitances and mutual inductances

The value of the mutual capacitance (C_M) can be approximated by taking measurements of the induced current (I_{quiet}) in the quiet line and by the rate of change of the voltage in the aggressor line ($V_{aggressor}$). The approximated C_M is given by [6]:

$$C_M = \frac{1}{I_{quiet}} \frac{dV_{aggressor}}{dt}. \qquad (2.10)$$

Same kind of approximation can be made for the mutual inductance (L_M), but in this case, it depends on the voltage that the aggressor induces in the quiet line (V_{quiet}) and the rate of change of the current in the aggressor line ($I_{aggressor}$). The approximation is given by [6]:

$$V_{quiet} = L_M \frac{dI_{aggressor}}{dt} \qquad (2.11)$$

Both, the mutual inductance and the mutual capacitance, contribute to the crosstalk noise seen in the quiet line. The crosstalk induced by the mutual capacitance is given by:

$$Crosstalk_C = \frac{R_B C_M}{T_r} \qquad (2.12)$$

and the crosstalk induced by the mutual inductance is given by:

$$Crosstalk_L = \frac{L_M}{R_A T_r}, \qquad (2.13)$$

Equation 2.1 - Crosstalk noise due to mutual inductance

where R_B is the impedance of the receiver, R_A is the impedance in the transmitter and T_r is the rise time of the signal. Total crosstalk in the quiet line is obtained by adding both factors:

$$Crosstalk_{TOTAL} = Crosstalk_C + Crosstalk_L \qquad (2.14)$$

Now, since crosstalk grows linearly with both, the mutual capacitance and mutual inductance, the amount of electric and magnetic field interaction between the lines, will decrease if the lines are spread out. This principle has been the foundation for all the crosstalk optimization that has been done until now. This dissertation describes a different way to address this problem, therefore the theory behind spacing and crosstalk will not be covered.

If the noise voltage is measured in both ends in a quiet transmission line, the patterns for each side will be different. To distinguish each end, it is common to refer to the closest to the driver as the "near-end" and the farthest as the "far-end" (Figure 2.13). When the lines are properly terminated, the noise on each end has a special shape: the near end noise rises up quickly and then stays constant for a time equal to twice the time delay of the coupling length and then drops down. The constant saturated amount of noise is called Near End Crosstalk or NEXT coefficient (Figure 2.14). This value is expressed as a percentage of the incident voltage in the aggressor and it can be calculated using:

$$NEXT = \frac{1}{4}\left(\frac{C_{mL}}{C_L} + \frac{L_{mL}}{L_L}\right), \qquad (2.15)$$

where C_{mL} is the mutual capacitance per length, C_L is the capacitance per length of the signal trace, L_{mL} is the mutual inductance per length, L_L is the inductance per length of the signal trace.

The far-end noise has a very different signature, it increases after one time delay (TD) of the coupling length. The width of the pulse is equal to the rise time of the signal; the peak of the voltage is labeled as the far-end crosstalk or FEXT

coefficient (Figure 2.15). The value of FEXT on the lumped-circuit model can be calculated using:

$$FEXT = \frac{Len}{RT} * \frac{1}{2v} * \left(\frac{C_{mL}}{C_L} - \frac{L_{mL}}{L_L} \right), \qquad (2.16)$$

where *Len* is the length of the coupled region between the lines, *v* is the speed of the signal on the line and *RT* is the rise time of the signal. A detail description on this topic can be found on [6].

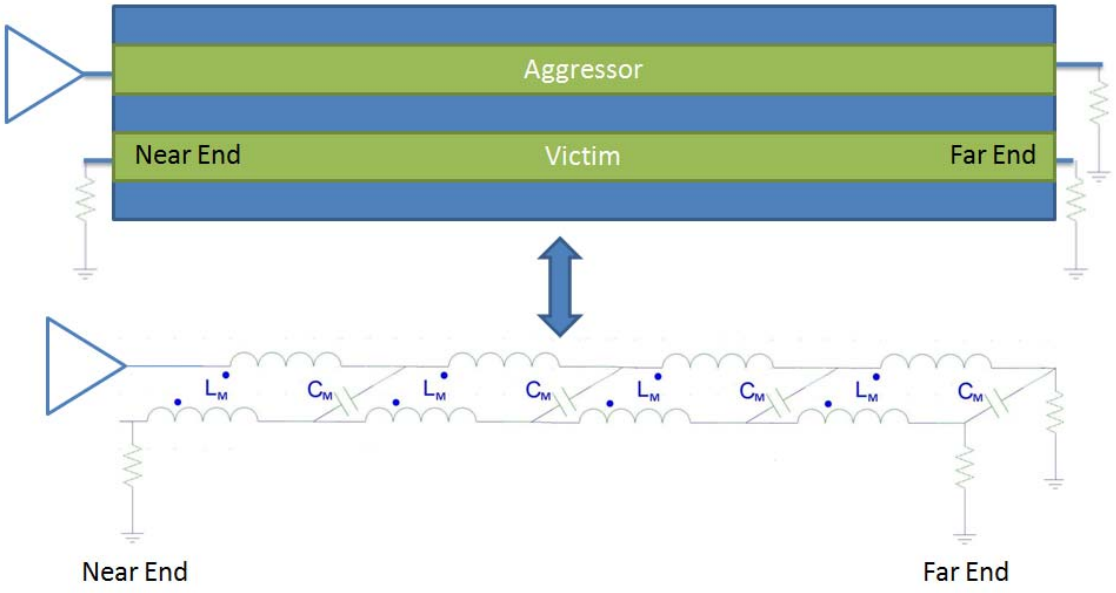


Figure 2.13 - Aggressor and victim lines in physical representation and lumped-circuit representation showing only the mutual components. Crosstalk noise has a different pattern on each end.

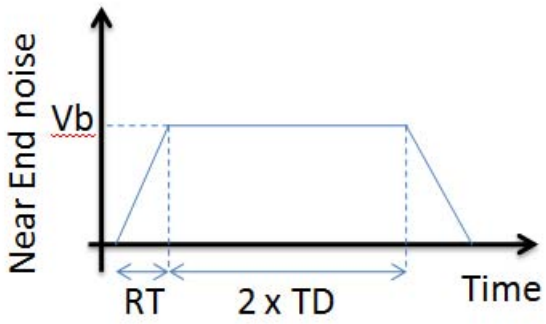


Figure 2.14 – Shape of the near end crosstalk noise

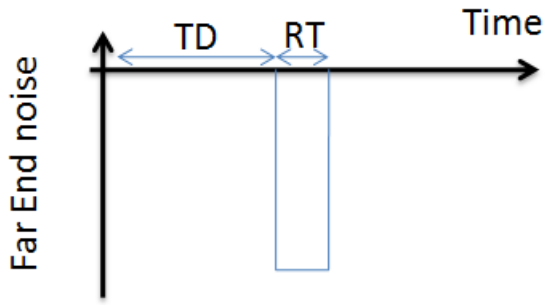
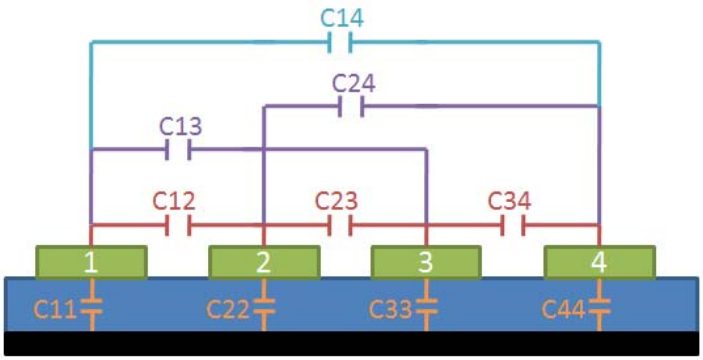


Figure 2.15 - Shape of the far-end crosstalk

The models described above can be extended to more than two transmission lines since the principle of superposition can be applied. All transmission lines in the system will have a mutual inductance and capacitance among all other lines in the system. The analysis and their lumped-circuit model gets more complicated, thus matrices are used to describe the interaction among lines as shown

in Figure 2.16. A set of similar matrices can be generated for all the elements (C, L, R, and G) in the lumped-circuit model. This set is then used to construct the W-Element matrix that can be simulated using a 2D solver like H-Spice.



	1	2	3	4
1	C11	C12	C13	C14
2	C12	C22	C23	C24
3	C13	C23	C33	C34
4	C14	C24	C34	C44

Figure 2.16 - Capacitance matrix for 4 coupled transmission lines. The diagonal of the matrix represents the self capacitance with respect to ground. Other values represent mutual inductance among lines

Differential Pairs

Differential pairs are a subset of coupled transmission lines that take the advantage of differential signaling. In differential signaling, one transmission line drives the signal and the adjacent line drives its complement. Therefore, the

differential voltage, defined as the voltage in one line minus the voltage in the adjacent line, will have a higher noise rejection and it is unaffected by ground voltage shifts because the return current from one of the lines is cancelled by its complement. The only signal current returning from a differential signal pair is that due to any imbalance between the two transmitted signals.

If two lines are not coupled, the differential impedance between them can be calculated as

$$Z_{diff} = Z_0 + Z_0 , \qquad (2.17)$$

where Zo is the characteristic impedance of each line with respect to its return path. However, when the two lines are coupled, the mutual impedance affects the characteristic impedance on each line and the effect is data dependant, this is known as proximity effect [4]. Thus, when the lines are coupled, the characteristic impedance of the differential line must be calculated by using information of the the transmitted signals.

In differential signaling, there are two possible scenarios, the odd mode and the even mode. In the even mode, both lines transmit the same signal. This is referred as common mode transmission. There is no dV/dt between the signal lines so the current produced by the mutual capacitance is 0. The current produced by the mutual inductance in both lines is equal, therefore the pattern will be propagated without distortion.

In the odd mode, opposite-transitioning signals are applied to each line. Some far-end noise is generated due to coupling but since the coupled line is transmitting exactly the same pattern but inverted, the far-end noises will cancel and the result is a voltage pattern that will propagate unchanged down the differential pair.

To quantize the effect of crosstalk between lines, the differential impedance (even mode) and the common impedance (odd mode) need to be calculated. Let Z_{odd} be the odd impedance of a line, defined as the impedance of one line with respect to the ground plane measured when the differential channel is transmitting in differential mode. Also define the even impedance Z_{even} as the impedance of one line with respect to the ground plane measured when the channel is transmitting in common mode.

Then, when the lines are driven in odd-mode, the differential impedance is two times the odd impedance of the line:

$$Z_{diff} = 2 * Z_{odd} . \qquad (2.18)$$

When the lines are driven in even-mode, the common impedance is one half of the even impedance:

$$Z_{comm} = Z_{equiv} = \frac{1}{2} Z_{even} \qquad (2.19)$$

Odd-mode impedance per-unit-length and the even-mode impedance per-unit-length can be approximated using the lumped-circuit model shown in Figure 2.12, therefore the differential impedance of a differential pair can also be approximated using this model. The results of the analysis are shown in Eq. 2.20 to Eq. 2.25.

$$C_{odd} = C_1 + 2C_M \tag{2.20}$$

$$L_{odd} = L_1 - L_M \tag{2.21}$$

$$C_{even} = C_1 \tag{2.22}$$

$$L_{even} = L_1 + L_M \tag{2.23}$$

$$Z_{odd} = \sqrt{\frac{L_{odd}}{C_{odd}}}, Z_{even} = \sqrt{\frac{L_{even}}{C_{even}}} \tag{2.24}$$

$$TD_{odd} = \sqrt{L_{odd} C_{odd}}, TD_{even} = \sqrt{L_{even} C_{even}} \tag{2.25}$$

The above equations can be extended to any number of transmission lines, allowing the calculation of differential and common mode impedance, as well as time delay characteristics for any degree of coupling.

2.2.3 Anti-coupling capacitance to minimize crosstalk in differential pairs

Crosstalk in differential pairs occurs when an aggressor is routed close to the differential pair, as shown in Figure 2.17. In this case, the amount of crosstalk noise induced to the closest line is higher than the amount of noise induced in its complement line. Given the nature of differential signaling, the total amount of crosstalk affecting the signal's integrity will be the difference between the induced crosstalk in each line. It is shown in Figure 2.17 that, the total voltage in each line will be its own voltage (V1 or V2) plus the amount of crosstalk coupled from the coupling impedance between the line and the aggressor (in this case labeled as Vn).

The coupling impedance decreases as space between the line increases, therefore, the coupling between Vn and V1 (labeled as b* in Figure 2.17) will be smaller than the coupling between Vn and V2 (labeled as d* in Figure 2.17)

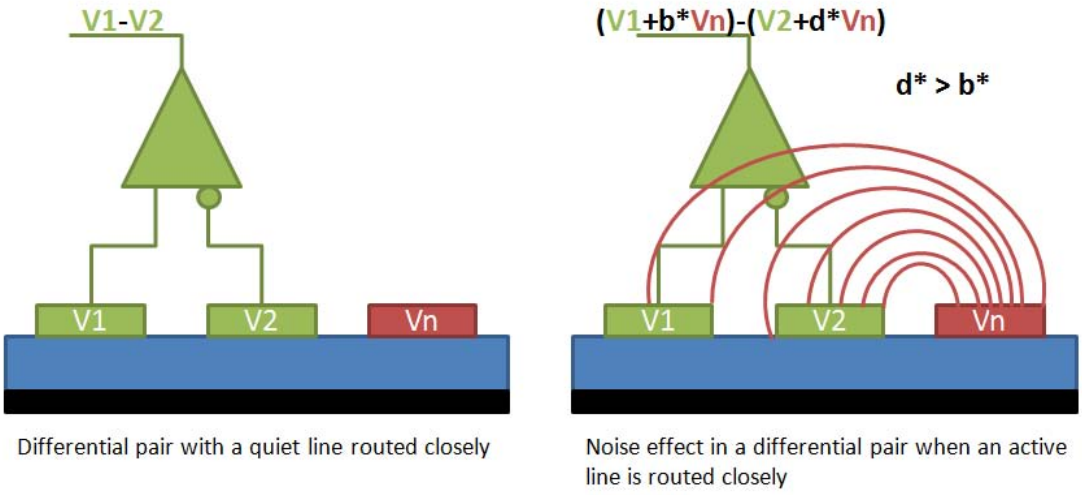


Figure 2.17 - Crosstalk is an issue in differential pairs when the coupled noise is unbalanced between the differential lines. When an active trace is routed close to a differential pair it will induce more crosstalk noise in the closest line.

To minimize crosstalk, this dissertation presents a solution in which the noise on both lines of the pair is matched. As the output of the differential line is given by the difference between the lines, the resulting effective differential crosstalk noise will be minimized.

In a differential bus, all routed signals have differential drivers and receivers, as shown in Figure 2.18. The effective noise in the victim receiver is minimized if the coupled noise from the aggressor's positive line is neutralized by increasing the effect of the aggressor's negative line. This could be achieved by placing an external matched-coupling element between the aggressor and the victim lines.

Figure 2.18 - In a differential bus, all routed transmission lines have a complement line routed next to it that is transmitting its opposite signal

Using the lumped-circuit model approximation, and assuming that the lines are short (less than 100mm), the distributed effect of the mutual impedance can be mitigated by placing anti-coupling capacitors between the differential pairs; the purpose of placing the anti-coupling capacitances is to match the amount of crosstalk in both lines so that the coupled differential noise, both FEXT and NEXT, will be minimized.

The crosstalk noise in a quiet differential line induced by an aggressor is shown in Figure 2.19. It also shows the analysis of the total crosstalk induced in each line in terms of the voltage in each aggressor line. To minimize the effect of the mutual capacitances anti-coupling capacitances are placed, as shown in Figure 2.20. Also in Figure 2.20 the analysis done to mitigate the effect of induced crosstalk. The noise in each line is minimized, by inducing a voltage proportional to the noise but in

opposite phase. Given that the nature of differential signaling, this voltage is easily obtained by taking it from the complement line, as can be noted in Figure 2.20.

The value of the capacitances can be controlled based on BER measurements on the link. Using the accelerated Bit Error Measurement technique introduced by Joshua Kramer and described in Section 2.1 the crosstalk between channels can be taken to the minimum.

The algorithm that minimizes the crosstalk starts with a minimum transmitted power (to achieve a BER in the order of 10^{-4}) in the victim line; this step allows that changes in the BER to be easily detected. Then, the aggressor line is turned on at its maximum power generating crosstalk noise in the adjacent channel, thus increasing the BER. Then, the values of the capacitances are changed to minimize the BER.

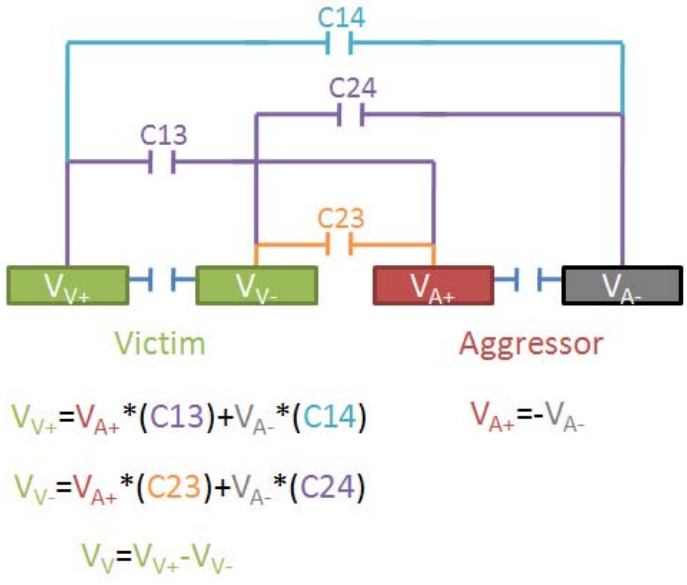


Figure 2.19 - Crosstalk in a victim differential pair induced by an aggressor differential pair in terms of mutual capacitance

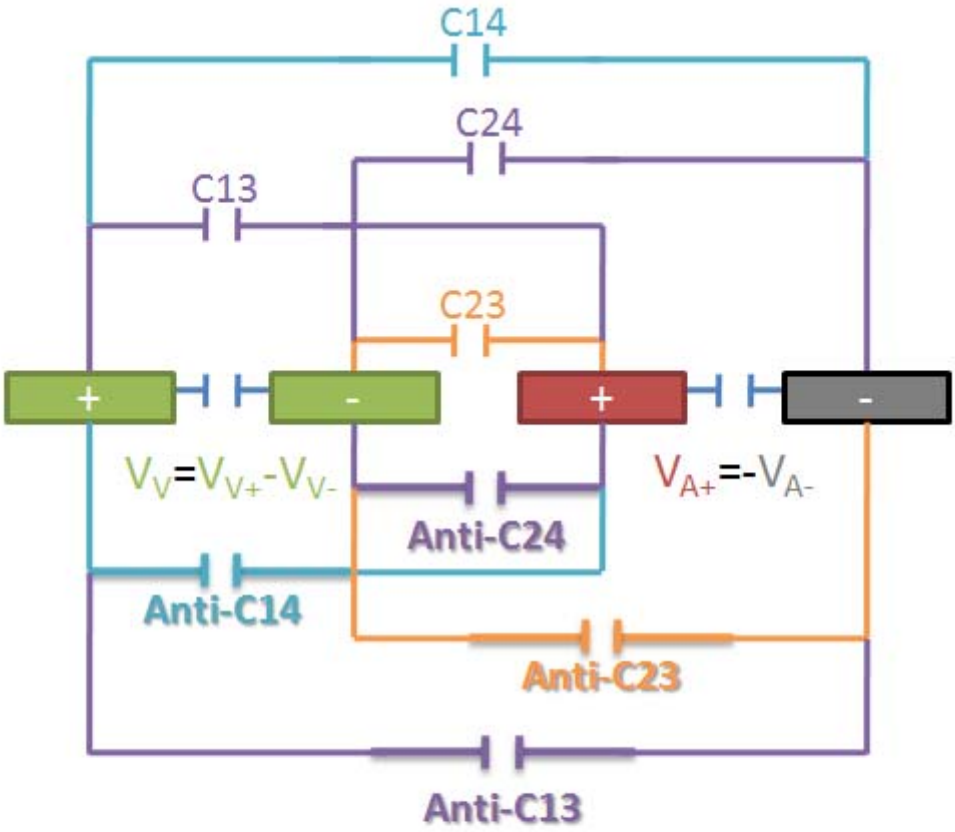


Figure 2.20 - Differential signaling allows the placing of anti-coupling capacitances that will mitigate the effect of crosstalk among differential pairs

To reduce the complexity of the optimization algorithm, and to obtain a balanced system, the anti-coupling capacitances “Anti-C24” and “Anti-C13” have the

same fixed value, that can be obtained during design and it is equal to the mutual capacitance C13=C24. The anti-coupling capacitances “Anti-C23” and “Anti-C14” are found by an optimization algorithm.

2.2.4 Termination impedance control

In high-speed systems, reflection noise produces many signal integrity issues like ringing, overshoot, undershoot and time delay increase. The main factor that causes reflection is the impedance discontinuity along the signal transmission path. When a signal finally reaches the receiving end of a transmission line, if the load is not matched with the transmission line characteristic impedance, reflection will also happen. Common practices to minimize reflection noise, include: controlling trace characteristic impedance (through trace geometry and dielectric constant), eliminating stubs, choosing appropriate termination scheme (series, parallel, RC, Thevenin), and always using a solid metal plane as the reference plane for return current [4].

The optimization algorithm proposed in this dissertation takes care of the mismatch between the transmission line’s impedance and the termination impedance at the receiver, minimizing the noise generated by reflections therefore incrementing the signal to noise ratio in the system. This optimization also uses the BER measurement of the signal at low power. For each differential pair at a time the transmitter power is set to a low value (where the BER is in the order of 10^{-4}), then the input resistance of the receiver is changed until the minimum BER is achieved. Again, since the BER is high, any change in BER will be noticed fast. As an increase in the transmission power will not affect the differential impedance of the line, the line will still be properly terminated, when the estimated power that achieves the target bit rate is used.

2.3 Multilink VSMPL algorithm: the complete solution

Using the elements described above, an optimization algorithm was developed to achieve a high performance parallel-link for differential signaling. The algorithm is described below.

1. Tune the termination resistor on the receiver: this is done by changing the gain of the differential amplifier based on the BER measurement on the link at low power.
2. Tune the anti-coupling capacitances: Using the superposition principle, this step can be done using the first two lines, tuning the crosstalk between them and then continue to the next two lines and so on until the end of the parallel link is reached. The parameter to measure the effect of the capacitance is the BER on the victim line.
    a. Turn on the victim line at low power (so that BER is in the order of 10^{-4})
    b. Turn on one neighbor at the highest power. The BER in the victim line will increase due to crosstalk noise.
    c. Tune anti-coupling capacitance until minimum BER is reached.
3. Review impedance matching for the lines: once the capacitors are tuned, the differential impedance changes and the receiver's termination resistance has to be done again. Repeat 1 and 2 until stable.
4. Once the lines have been uncoupled, they can be treated as serial links and the power optimization described in section 2.1.3 can be applied to each line.

Figure 2.21 shows the block diagram of a two channels link, showing the optimization parameters that are tune to achieve a target BER.

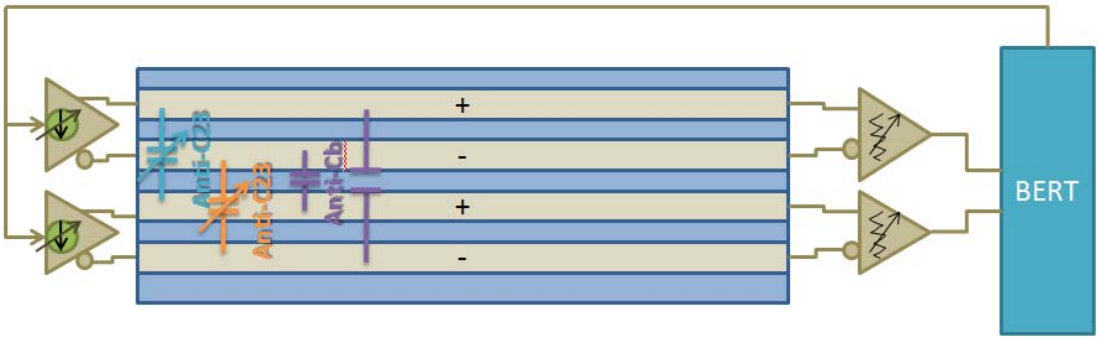


Figure 2.21- Block diagram of the optimization algorithm for a 2 channels high speed parallel link. Parameters that can be adjusted during the optimization algorithm are transmitter power, termination resistance and anti-coupling capacitances.

Chapter 3

3 TESTING AND SIMULATION PLATFORMS

This chapter describes the testing setup used to characterize the first version of the VSMPL algorithm, developed by J. Kramer and explained in Chapter 1, in bus configuration, and it also describes the simulation platform used as a proof of concept for the Multilink VSMPL algorithm. The chapter is divided in three sections. Section 3.1 provides a description of the ASIC and a detailed description of the PCB Section 3.2 describes the software used to do an accurate simulation of the signal integrity behavior of the system. Finally, Section 3.3 provides a high speed design flow – from die to system integration – given as a guide for future high speed designers that want to apply the multilink VSMPL algorithm to their systems.

3.1 Testing Platform

A platform to test the VSMPL algorithm in a bus configuration was built. It consisted of two ASICs each with 25 VSMPL channels and a PCB to communicate them. ASICs can communicate using 3 different bus topologies, providing flexibility to test the algorithm in various configurations. The test plataform also includes a Labview interface to program the ASICs, a Bit Error Rate Tester and an oscilloscope to measure the performance of the system.

3.1.1 ASIC Overview

The test ASIC has 25 VSMPL I/O channels, each designed to operate at 20Gb/s using 3.2mW; it also has a pseudo-random bit stream (PRBS) generator that operates up to 30Gb/s and can be programmable to provide either 27-1 or 215-1 codes. The chip also has an on chip voltage controlled oscillator (VCO) that generates a clock frequency of up to 30Gb/s. All the features on the ASIC can be programmable during operation using a shadow register and a Labview interface which will be described in detail in the next section. It was fabricated in the IBM 8HP 120nm SiGe process. Figure 3.1 shows a picture of the chip and Figure 3.2 shows its architecture. This subsection provides a brief overview of each block of the ASIC highlighting the main features on each.

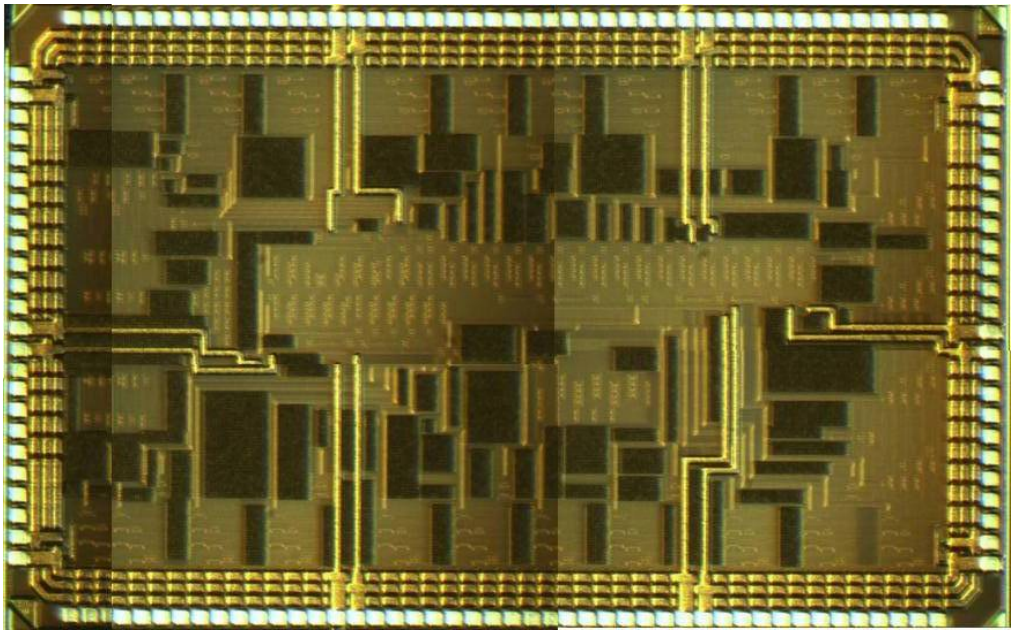


Figure 3.1 - . The Multilink VSMPL testing ASIC features 25 VSMPL channels, an on chip VCO that works up to 30Gb/s and an on chip LFSR

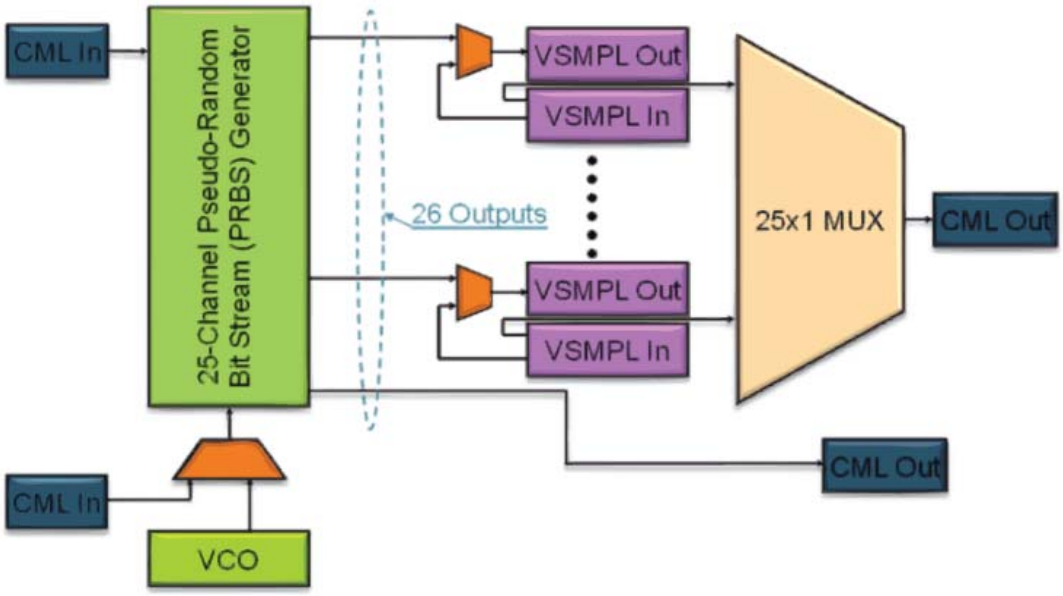


Figure 3.2 - The multilink VSMPL ASIC architecture Includes CML inputs used to trigger the chip externally and to input external data. CML outputs are used to communicate with standard equipment.

Voltage controlled oscillator

The 30Gb/s VCO was designed using a ring oscillator configuration of three stages. Each stage provides a delay that determines the VCO's frequency of operation. The block diagram of the VCO is shown in Figure 3.3. The actual frequency used to trigger chip is a divided version of this clock, so at the output of the VCO there is a divider by 2, 4, 8, 16 and 32. The value of the divider as well as the frequency of operation of the VCO can be programmed through Labview.

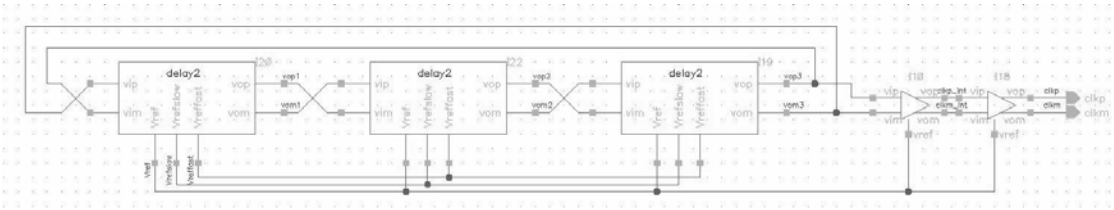


Figure 3.3 - Three stages ring oscillator. Each delay stage is an inverter which delay determines the VCO's frequency of operation. Maximum speed of the VCO is 30Gb/s

Pseudo Random Bit Stream (PRBS) Generator

A Linear Feedback Shift Register (LFSR) was used to generate the pseudo random sequence. Using the flexibility of programming the chip while it is running, a 7 or 15 tap can be selected which means that a pseudo random code of 2^7-1 or 2^{15}-1 is generated. The LFSR was designed to work with a clock of up to 30Gb/s, and it also has the capability of bypassing itself an allow an external pseudo random sequence to be used in the system.

Low Swing Transmitter

A current mode, fully differential transmitter was implemented; it allows controlling the transmitter current by a simple design of a differential pair with a 100 ohms termination resistor.

Figure 3.4 shows the schematic of the transmitter. The transmitter consists of a differential pair and a 100ohm termination resistor. The current of the differential pair, which is the same transmitter current, is controlled with a 5-bit DAC. To be able to test the real transmitted current for every setting of the DAC, a exact copy of this DAC is connected directly to one of the pins of the chip; an extensive profiling of the

DAC was performed to measure the amount of power sent by the transmitter at every digital setting. From this profiling we have a complete characterization of the transmitted current. The results provided a very linear response of the DAC with a low temperature coefficient. The characterization of the DAC is described further in Chapter 4. The complete driver has four basic components: the transmitter, an amplifier, a level shifter, and a multiplexer that takes data from the LFSR circuit or re-outputs the data coming into the VSMPL channel receiver. In the second case it will be working in a loopback configuration.

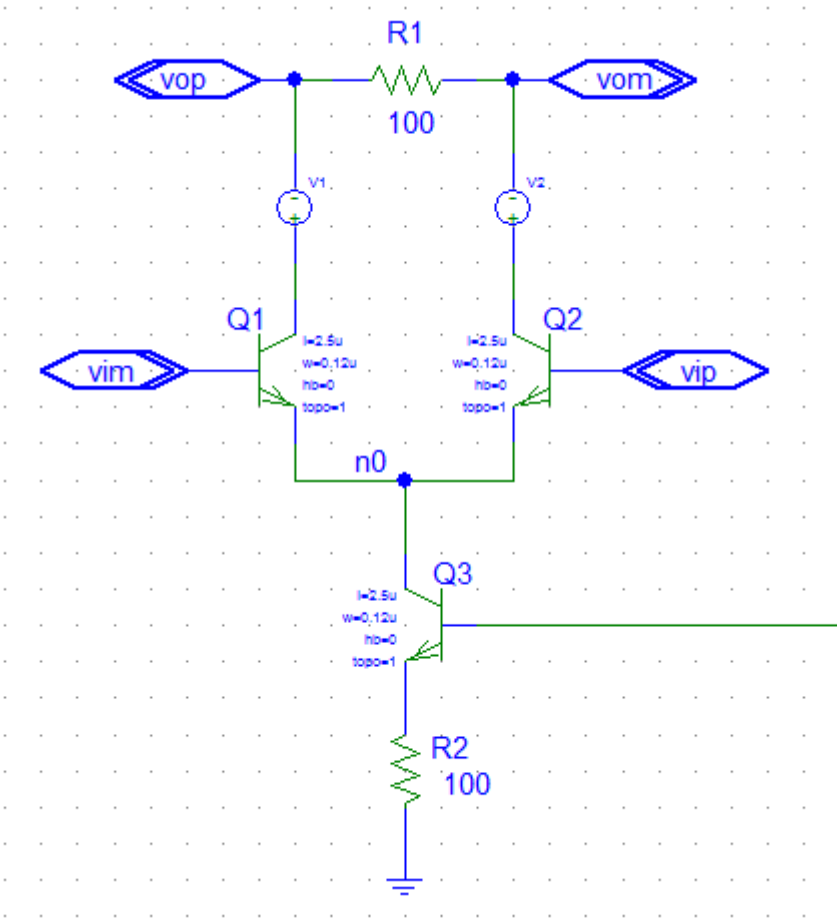


Figure 3.4 - The Low Swing transmitter consists on a differential pair with the proper 100ohm termination resistor. The transmission current is controlled digitally with the Labview interface.

Low Swing Receiver

The receiver is a current mode receiver that minimizes its power consumption. Its design also allows the tuning of the termination resistance by a DAC that controls the impedance of the impedance transformer; this feature is crucial for the optimization algorithm because the signal integrity of the transmission line is greatly improved.

In the low swing receiver design in the schematic on Figure 3.5; RT1 is used to terminate the transmission line. The current to voltage conversion is done by the 500ohm resistor RF1 which is located after the impedance transformer (Q3). RF1's placement avoids a post-amplification since the voltage swing at the output of the transceiver is 10 times higher than the swing achieved in a regular voltage mode receiver where the current to voltage conversion is done by a 50ohm resistor. Thus the power needed by the receiver is reduced. The differential amplifier is used to tune the termination impedance of the transmission line allowing a higher transmission data rate by minimizing the reflections.

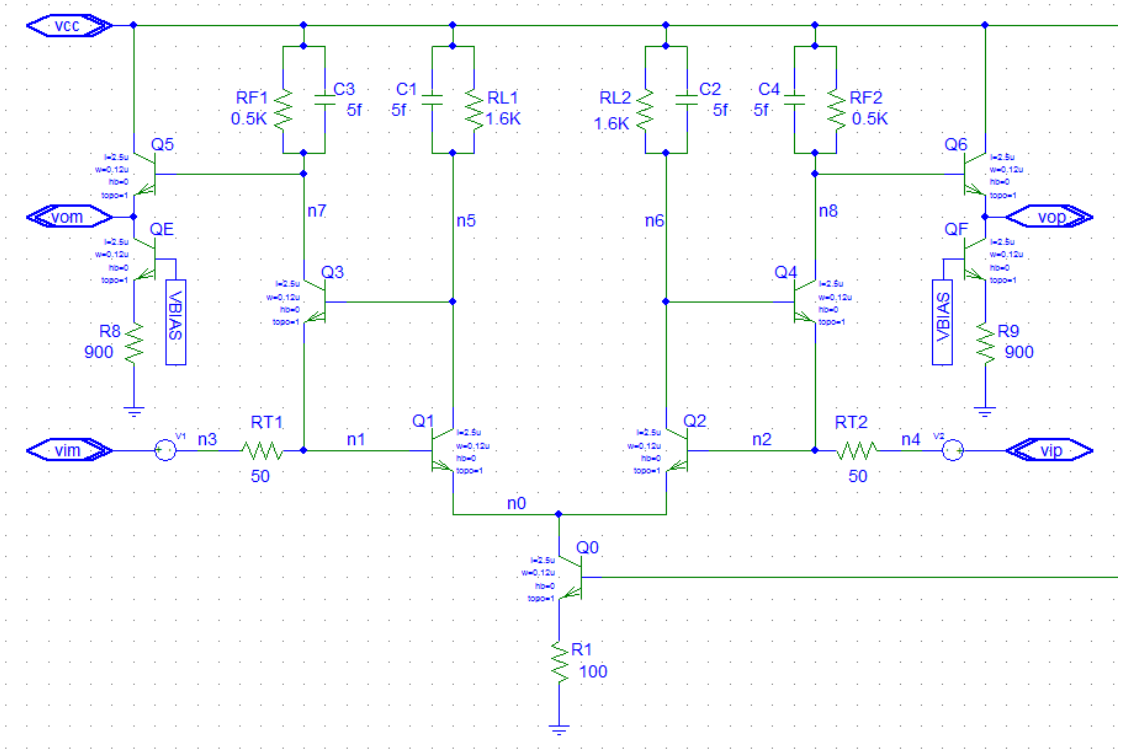


Figure 3.5 – The current mode differential VSMPL receiver uses RT1 and RT2 (50ohm resistor) only to terminate properly the line; the 500ohm resistor after the impedance transformer does the current to voltage conversion allowing the use of the minimum power on the receiver

Multiplexer

The multiplexer allows switching between two high speed signals. The multiplexer selects one of the 26 possible VSMPL outputs to use a CML driver; the block diagram of the multiplexer is shown in Figure 3.6. A basic two input multiplexer as the base for all the multiplexers in the ASIC.

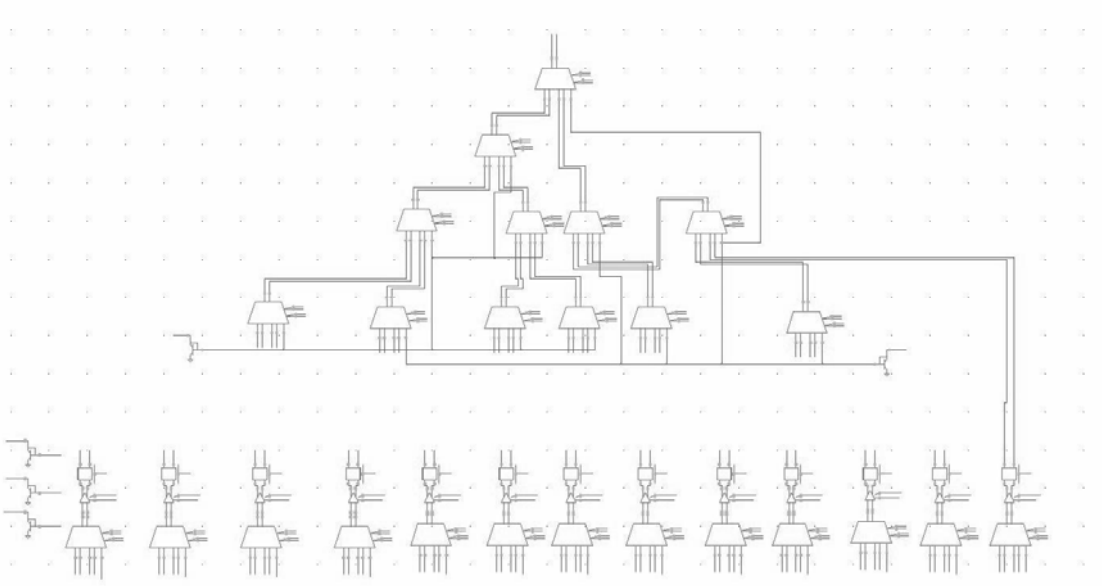


Figure 3.6 - Block Diagram of the 26-1 Multiplexer. Basic building block is a 2-1 high speed differential multiplexer.

Registers

The shift register scan chain programs all the settings on the chip. Transmitted power and termination impedance, among others, are programmed using a Labview interface that saves configuration information in the shift registers. A shadow register scheme was added that allows the user to reprogram the chip while it is running. The scan-chain is 3400 bits long, but because of the shadow register structure, a total of 6800 shift registers were used for programmability. The schematic of the shift registers is shown in Figure 3.7.

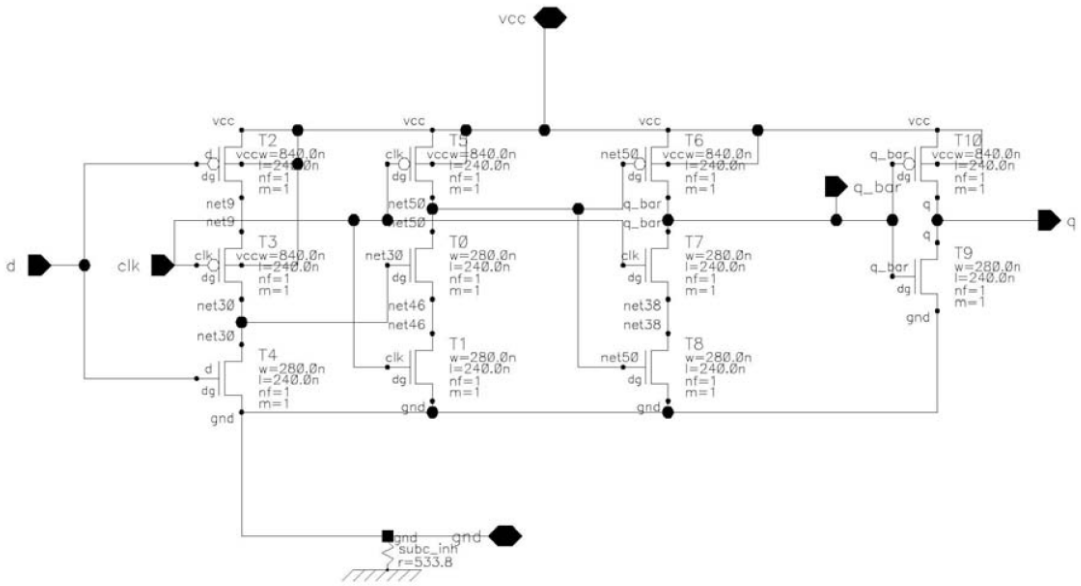


Figure 3.7 - Flip-Flop structure of the shift-registers.

3.1.2 PCB Design

A custom board was designed to test the chip; three different scenarios were considered in the design to be able to measure the effect of crosstalk and electromagnetic interference in the performance of the VSMPL links.

- The first scenario, shown in Figure 3.8, is a basic “rule of thumbs”, which states that if two differential lines are separated from each other a distance equal to five times the distances between the positive and the negative path, the crosstalk received is unnoticeable.

Figure 3.8 - Rule of Thumbs, each differential pair is separated from its neighbors five times the minimum spacing

- The second scenario, shown in Figure 3.9, includes a grounded and properly terminated guard band between the differential channels; this technique is widely used because it gives a good tradeoff between space used and crosstalk received.

Figure 3.9 - Guard Trace, each differential pair is separated from its neighbors by a properly terminated guard trace

- Finally, in the third scenario, shown in Figure 3.10, the differential lines are routed separated with the minimum space possible between positive and negative of the differential channels.

Figure 3.10 - Minimum spacing between channels. The distance between channels is the minimum allowed by the manufacturer.

The board provides two different lengths for all scenarios; this allows a greater testing flexibility. Figure 3.11 shows the top layer of the board labeling the different scenarios.

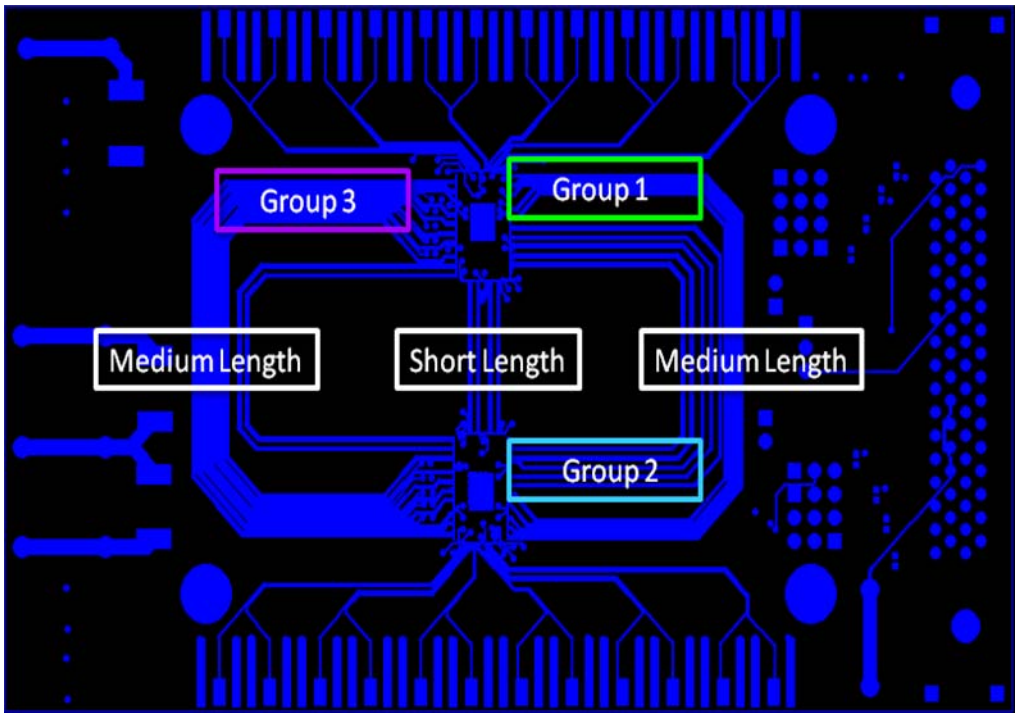


Figure 3.11 - The design of the PCB includes 2 different link lengths and 3 different configuration of spacing between channels (Minimum Spacing, Rule of thumbs, Guard Trace) to evaluate crosstalk for the different scenarios.

The board has 6 layers. The top and bottom layers are reserved for high speed signal routing. Following the design guidelines, ground layers are adjacent to these two layers. Vcc plane is placed in one of the center layers. The remaining center layer is used for routing the low speed signals to program the chip using the Labview interface. Figure 3.4 shows the cross section of the board.

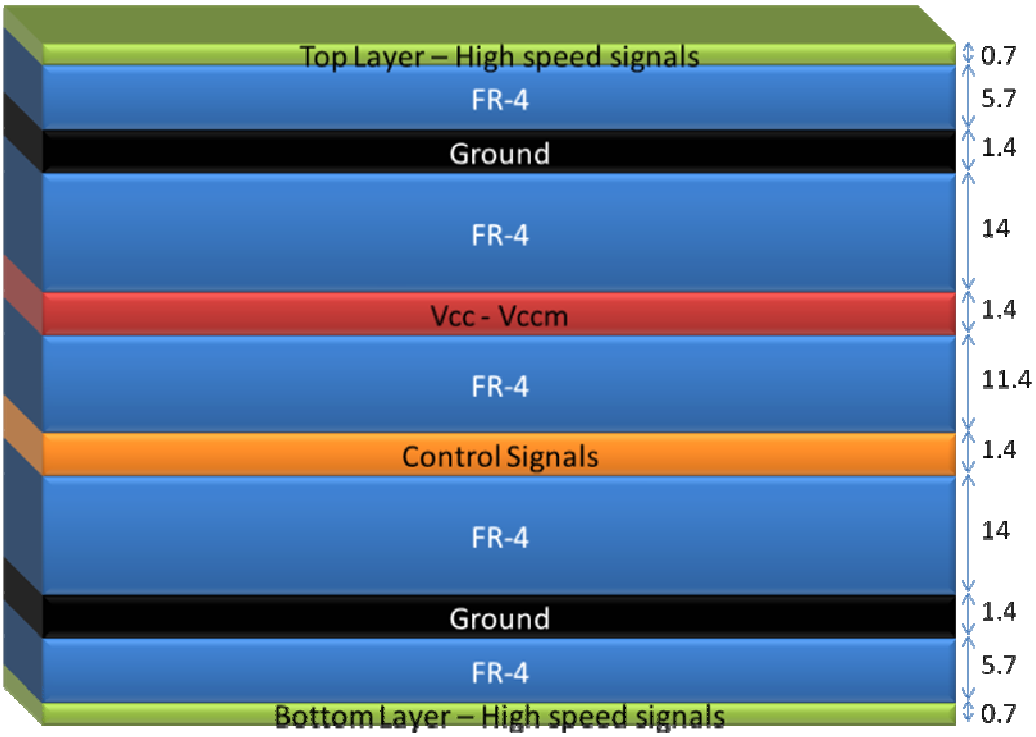


Figure 3.12 – The cross section of the PCB is designed to minimize signal integrity issues by proper design of its geometry.

The top layer was designed to have 100ohms differential impedance. All the values for the trace width, spacing between channels, and the cross-section values of the board were given by the manufacturer. Figure 3.13 shows the top layer routing of the fabricated board. All connectors used for high speed signals are SMA connectors; although, through-hole connectors have a smaller size. The use of vias in high speed signals affect the impedance on the line. Thus the use of a surface mounting connector is preferred for a better signal quality.

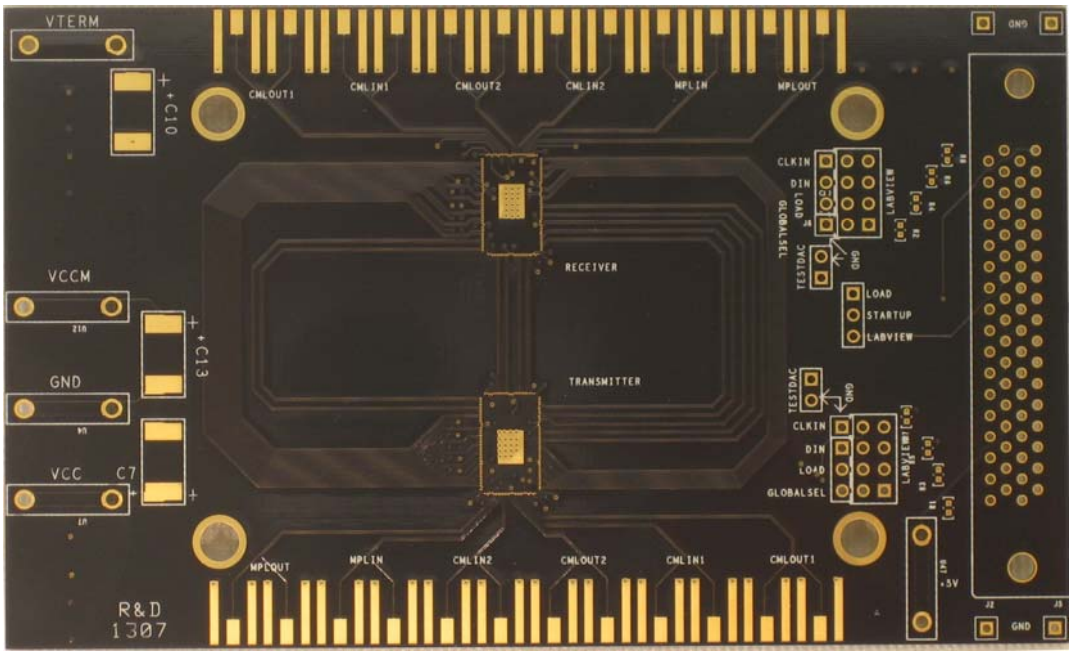


Figure 3.13 - Top view of the PCB showing the high speed routed buses and the two VSMPL ASICs placing.

Figures Figure 3.14 and Figure 3.15 show the ground plane and the Vcc/Vccm plane respectively. The ground plane was designed to have the lowest defects possible to increase the signal quality of the nets routed in the high speed layers. The Vcc/Vccm plane is split in two parts as the circuit uses 2 different voltage sources. One plane for the low swing signals and another plane for everything else.

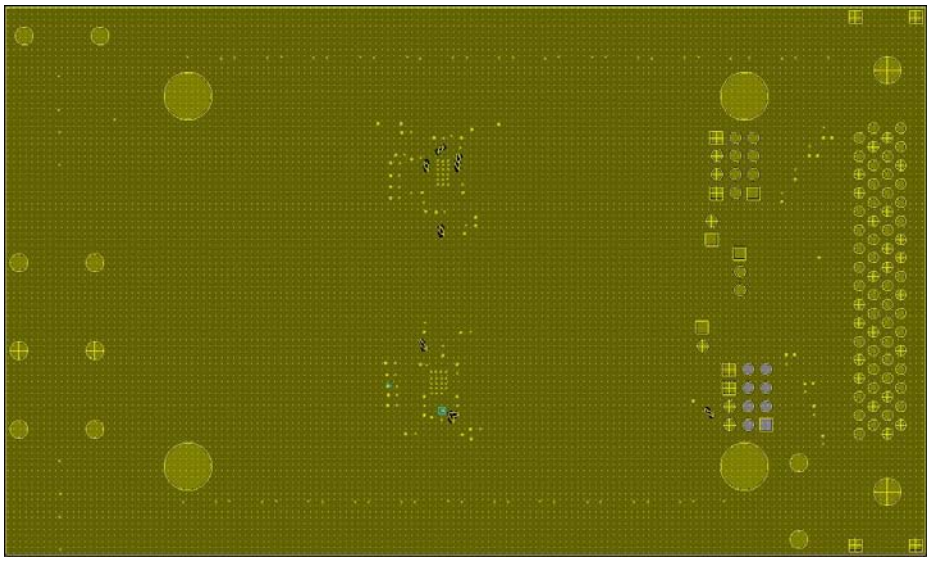


Figure 3.14 - Ground Layer was designed to provide the cleanest return path to the high speed signals routed above.

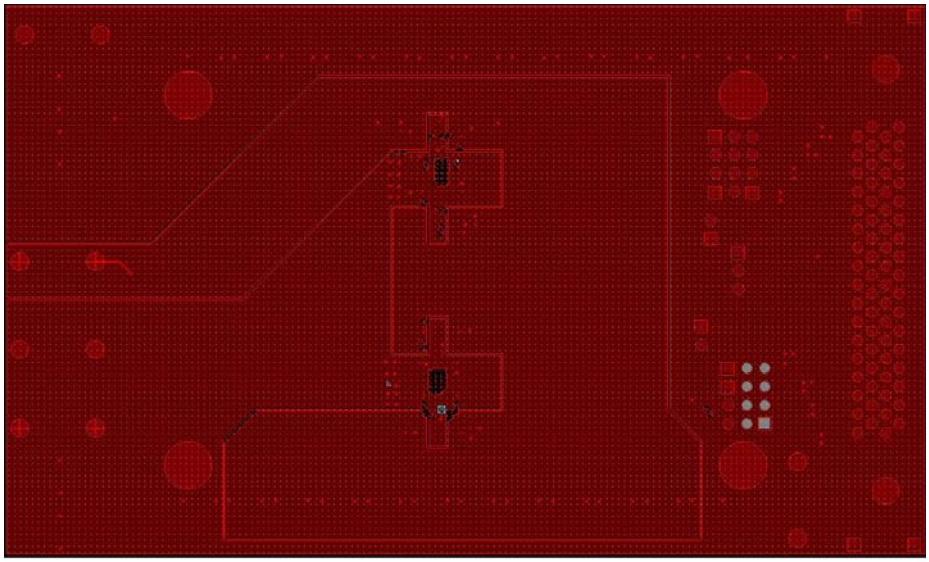


Figure 3.15 - The Vcc layer was split in two parts because of the use of two different voltage sources. One of them only drives the VSMPL low swing transceiver and the other one drives everything else.

The control layer is shown in Figure 3.16 - All signals in the control layer are low speed signals needed to program the chips through LabView.. All the signals in this layer are low speed signals used to program the ASICs.

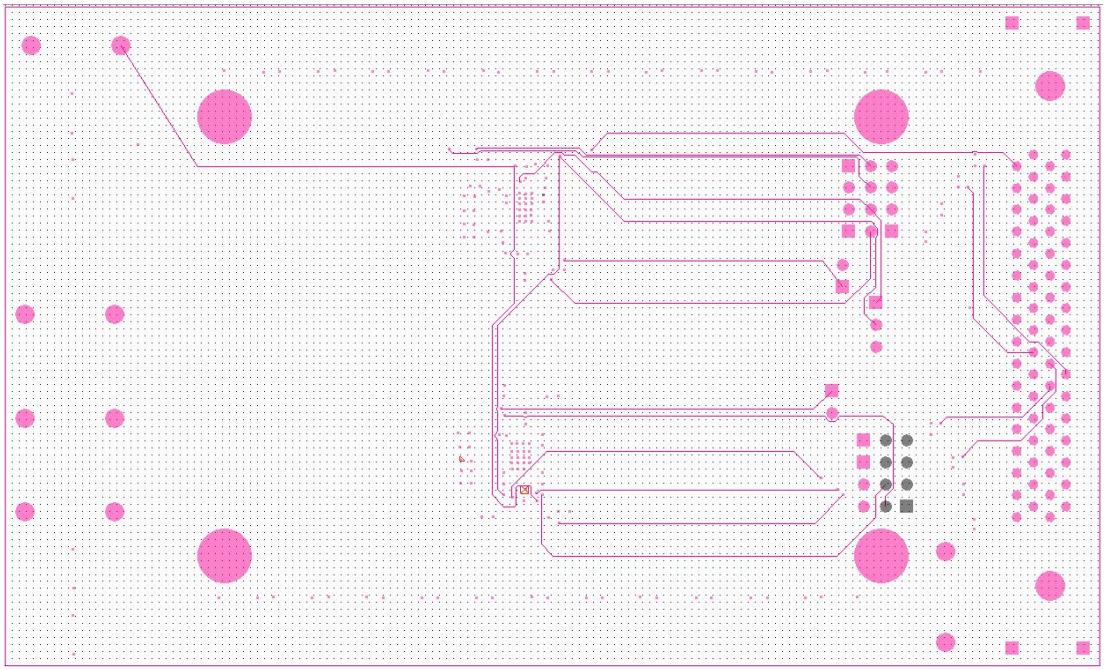


Figure 3.16 - All signals in the control layer are low speed signals needed to program the chips through LabView.

Finally, the Bottom layer is shown in Figure 3.17 - PCB Bottom Layer. There are only three high speed signals routed in this layer, which are VSMPL driver outputs. The purpose of each of them is to be able to measure the VSMPL output for each of the configurations described above without the effect of the multiplexer and the transition to the CML Driver.

Figure 3.17 - PCB Bottom Layer

3.1.3 Labview Interface

The board also contains a Labview interface for easier programmability while running. Figure 3.18 shows the designed Labview interface that was developed with the help of a fellow graduate student, Jirar Helou. The Labview card used for this testing is the PCI-6251 and the Labview version used to do the program was Labview 8.1

The Labview interface consists on different tabs that control each part of the chip. The “Chip Config” tab was designed to control the ASIC to be programmed. Since there are two VSMPL ASICs on the board, one serving as the transmitter and the other serving as the receiver, the interface should provide easy programmability for both. The TestDAQ tab controls a test DAC that is directly connected to one of the output pins of the ASIC. This allowed us to be able to test the correct operation of all

the internal DACs in the system. It also allowed a better characterization of the silicon DAC since it determines the transmitter and receiver power for every VSMPL channel. Next tab controls the clock; it can use an external clock to trigger the data or it could use the internal VCO to generate it. If the user selects chip operation with the internal VCO, the program allows the clock speed and power to be configured. The LFSR tab controls the Pseudorandom Generator. The user can select as data input the internal Pseudorandom Generator using the internal LFSR or an external input to the system.

MPL_CHL tab controls the settings of each of the VSMPL channels individually or it gives an option to program all the channels in the same way; the controls include power setting for the channel and it also gives the option to test the channel in loopback configuration (a or b selection, being ‘b’ the option to enable loopback testing). Each channel also has two different bias reference generators, one of them has a high temperature compensation, but since it was first used in this design as a backup a regular bias reference generator was also placed on the ASIC. Finally, the last tab is the CML configuration which has essentially the same settings as VSMPL channels.

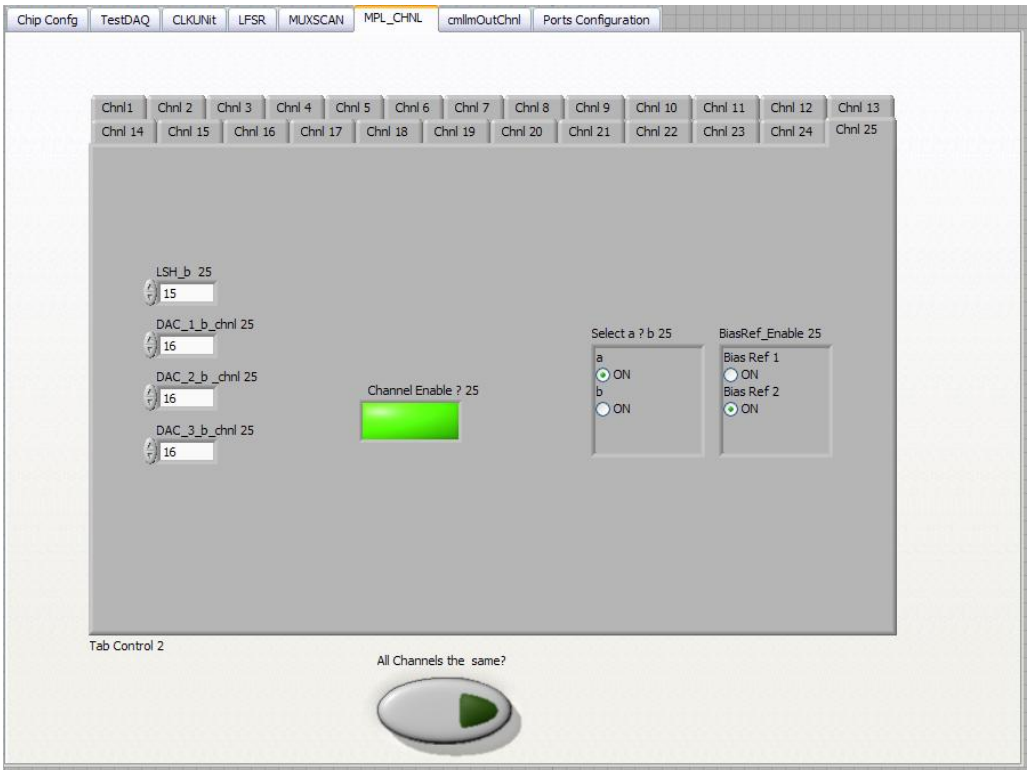


Figure 3.18 - The Labview interface to progam the ASIC consists of different tabs that control each part of the ASIC. Figure shows the controls for one VSMPL channel.

3.1.4 System Integration

The ASICs were wire-bonded to the PCB as shown in Figure 3.19. A first configuration uses one of the ASICs as transmitter and the second ASIC working as receiver. On a second configuration shown in Figure 3.20, the receiver takes the data from the transmission line connected to the transmitter of the same ASIC. Using the internal loopback capability the transmitter sends the again on the same channel. In this case the second ASIC is working as a repeater that forwards the data to the testing equipment.

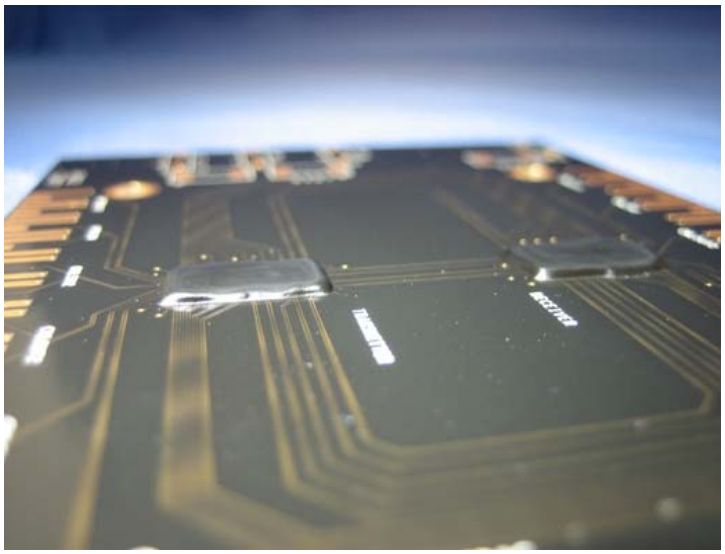


Figure 3.19 - Final PCB design showing wire-bonded ASICs

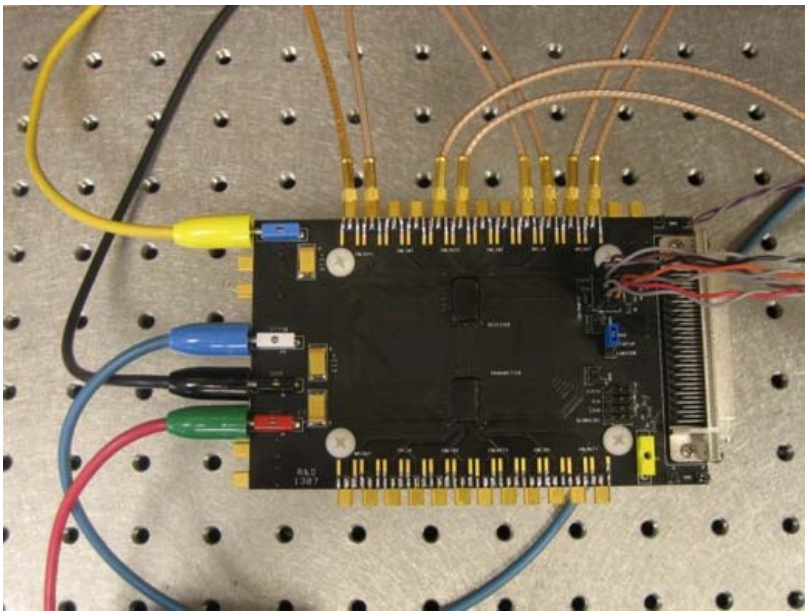


Figure 3.20 - In the loopback configuration shown the receiver ASIC takes the data from the transmitter ASIC and re-transmits it using its own driver.

A block diagram of the testing setup is shown in Figure 3.21, the Labview Card provides the correct programming to the ASICs and the Anritsu Digital Data Analyzer is used to generate the pseudo random bit stream and perform Bit Error Rate testing. Testing results are shown in Chapter 4.

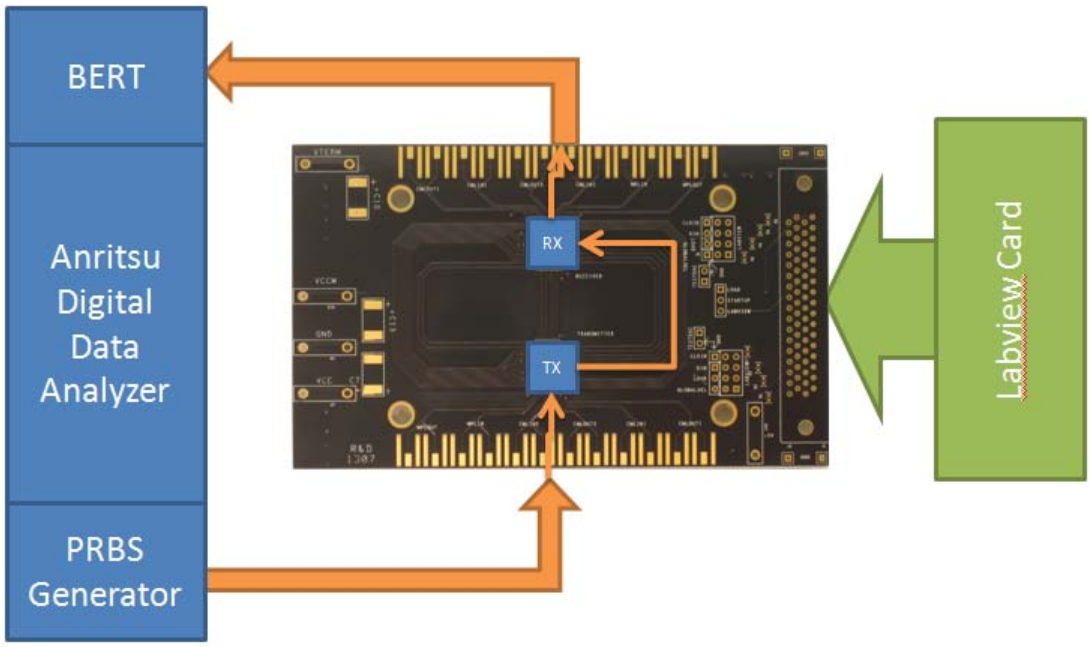


Figure 3.21 - Block Diagram of the testing setup

3.2 Simulation Platform

A simulation platform was designed to test the anti-coupling algorithm. It provides the flexibility necessary to test the theory, which is described in Chapter 2, without going into the expense of fabricating a new PCB. The simulation platform consists of three main programs: PSpice, HSpice and Cadence Allegro PCB SI GXL.

The first set of simulations (Figure 3.22) extracted the transmission lines of the PCB using Cadence's Constraint Manager tool. Then, using CML drivers, the complete link was simulated using Cadence's SigXplorer tool. An example of the extracted circuit is shown in Figure 3.23.

Cadence's simulator uses DML language, which is specific for Cadence products to model all the drivers and receivers. The DML language is based on IBIS models. IBIS refers to I/O Buffer Interface Specification (IBIS), also known as ANSI/EIA-656 [31]. It is a widely used specification that allows the use of the buffers without sharing the internal architecture, technology, or intellectual property of the device. The use of IBIS models is not desirable when the PCB designer has schematic models for all the devices on the design; in this case, the translation to IBIS removes important information from the simulation.

The first simulation, designed to prove that the transmission lines models of the PCB were correct without going into the translation of VSMPL buffers to DML, it was decided to use CML drivers which models were given by the tools. With these models a first set of simulations were run and all the signal integrity issues of the PCB were characterized. After this simulation, it was determined that a new board needed to be designed in order to get a better estimation of the effects of the use of the optimization methodology.

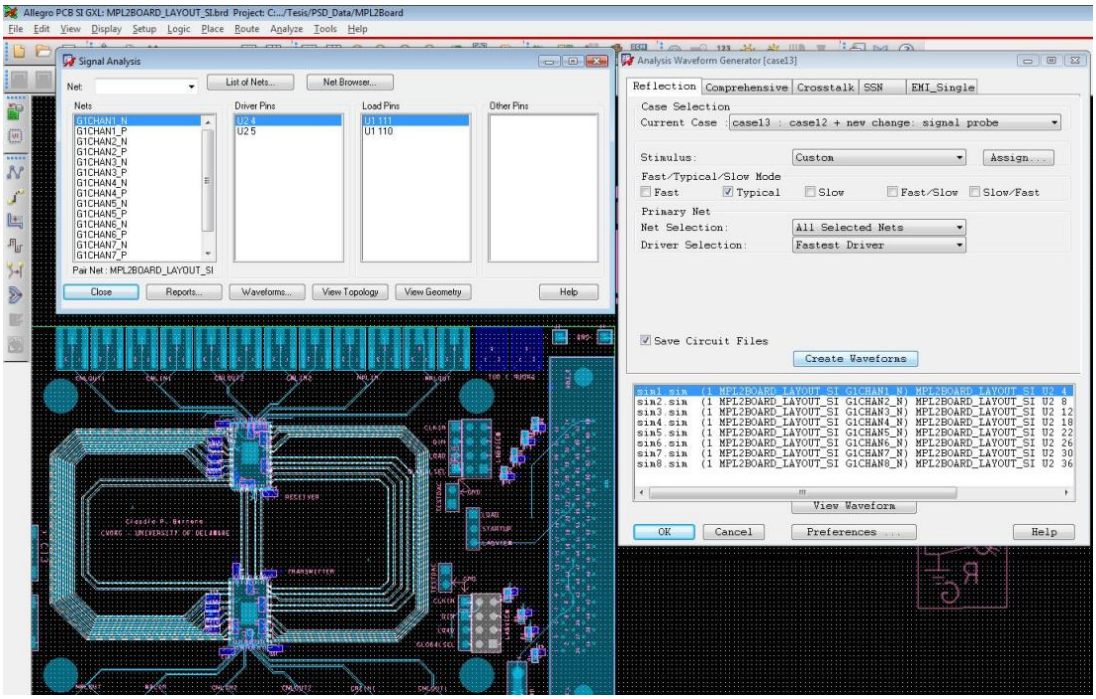


Figure 3.22 - Allegro PCB SI is a great tool for pre and post-routing simulations. Providing easy access to reflections, crosstalk, SSN, and EMI simulations.

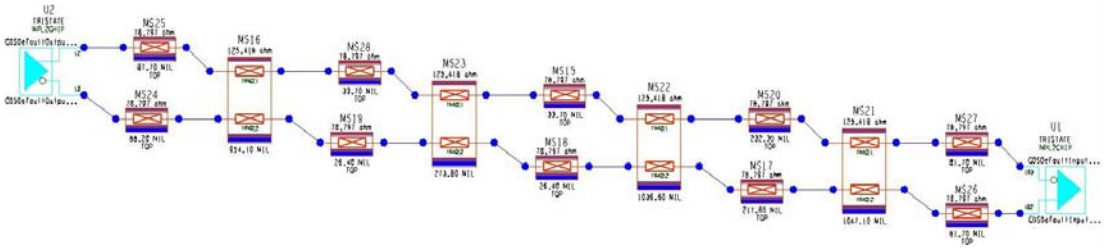


Figure 3.23 - Extracted differential pair from Contraint Manager to SigXplorer. Due to all the curvatures and discontinuities of the transmission lines, the extracted model is composed of coupled segments as well as uncoupled segments; for both cases the characteristic impedance of the line is not close to the designed 100ohms.

The second set of simulations was designed to simulate the VSMPL channel using the real extracted data from the PCB. Cadence SigXplorer provides two simulator options, Tlsim (Cadence's simulator) and HSpice. To simulate with Hspice the user needs to have a valid license from Synopsys and all the Pspice devices need to be in DML format. We decided not to use this option because of the difficulties with integrating the two tools. Also the translation from Spice to DML limits the testing of the VSMPL concept, as it requires a new DML to be generated each time the power setting is changed in Pspice. Instead, the H-parameters generated from SigXplorer were used in the HSpice simulation. Using this flow, the W-elements are generated only once per topology; thus, this file is used as TLINE2 block in the PSpice Block diagram shown in Figure 3.24

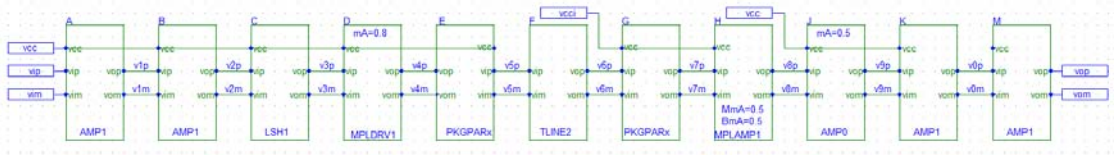


Figure 3.24 - PSpice block diagram of one differential pair. TLINE2 block diagram is generated using Cadence's SigXplorer tool.

After the simulation was done, a third set of simulations was generated to prove the anti-coupling capacitance theory. Since the original design of the PCB had many signal integrity problems with reflections, and EMI, a new design was generated using a simple 100mm transmission line. This design is shown in Figure 3.25. The parameters of the transmission line are shown in Table 3.1. Simulations usually vary

the spacing between the two differential pairs. This parameter can be easily setup and corresponds to the field “spacing 2” in Table 3.1.

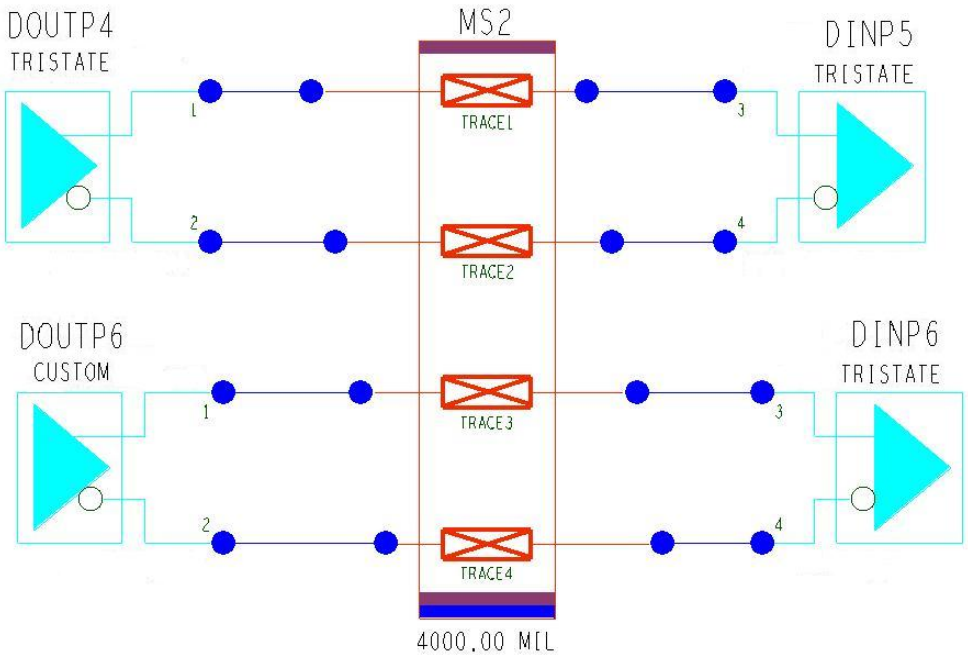


Figure 3.25 - 100mm coupled transmission line with 2 drivers and 2 receivers.

MS2	
d1Constant	4.5
d1LossTangent	0.035
d1Thickness	5.70 MIL
d2Constant	1
d2LossTangent	0
d2Thickness	0.00 MIL
length	4000.00 MIL
spacing	4.00 MIL
spacing2	4.00 MIL
spacing3	4.00 MIL
traceConductivity	595900 mho/cm
traceThickness	0.70 MIL
traceWidth	6.50 MIL
traceWidth2	MS2.traceWidth
traceWidth3	MS2.traceWidth
traceWidth4	MS2.traceWidth

Table 3.1 – Designed parameters of the simulated transmission line. 2 differential pairs equally spaced.

An example of the W-Element matrix generated using the SigXplorer extraction tool is shown in Figure 3.26; this matrix was generated for four conductors equally spaced and 6.5mils wide.

```
* Number of conductors
4
* L0 matrix
3.6682e-007
9.4242e-008 3.6071e-007
3.4506e-008 9.2701e-008 3.6071e-007
1.627e-008 3.4506e-008 9.4242e-008 3.6682e-007
* C0 matrix
9.5292e-011
-1.4069e-011 9.8252e-011
-8.2789e-013 -1.3928e-011 9.8252e-011
-3.737e-013 -8.2789e-013 -1.4069e-011 9.5292e-011
* R0 matrix
5.7167
0 5.7167
0 0 5.7167
0 0 0 5.7167
* G0 matrix
0
0 0
0 0 0
0 0 0 0
```

Figure 3.26 - Example of the W-Element matrix generated using SigXplorer extraction tool.

The last set of simulations including the crosstalk component were done using Hspice simulator. The schematic shown in Figure 3.27 shows the Pspice schematic used without the anti-coupling capacitors and the schematic shown in Figure 3.28 shows the placement of the anti-coupling capacitance.

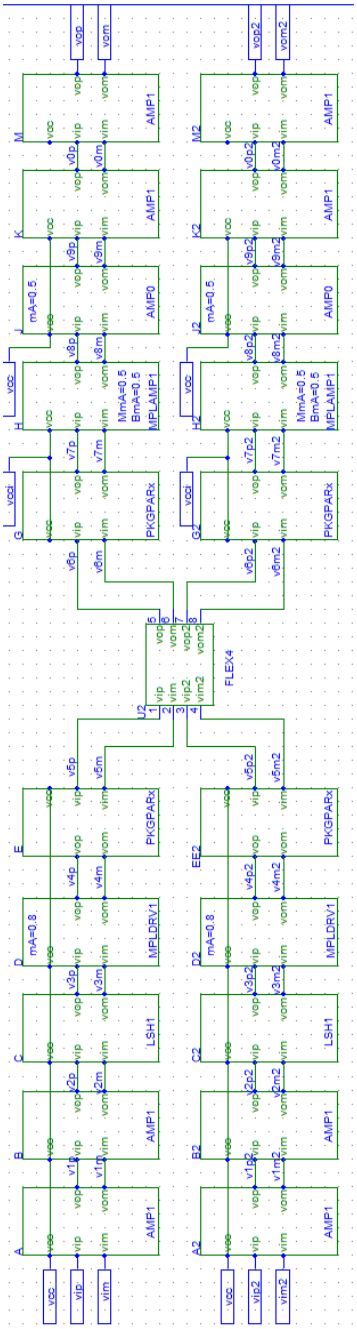


Figure 3.27 - Schematic for crosstalk simulator without anti-coupling capacitors.

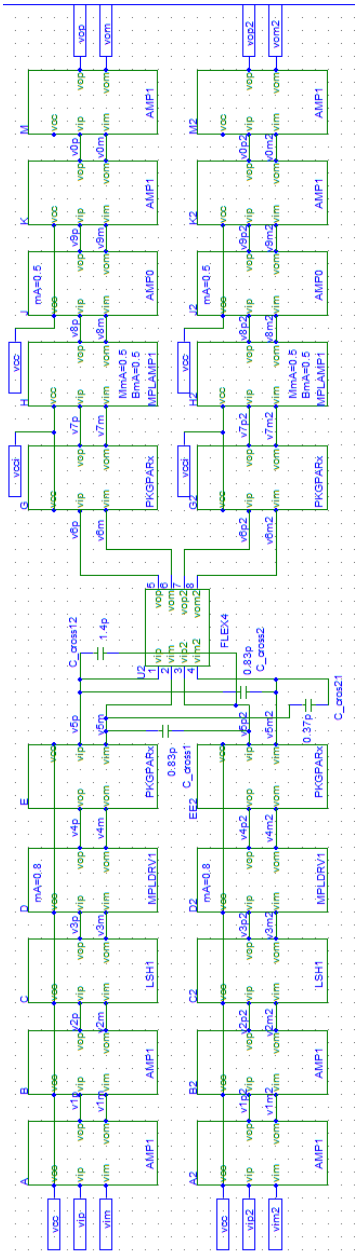


Figure 3.28 - Schematic for crosstalk using anti-coupling capacitance. Note that the capacitors are placed directly after the packaging model and before the transmission line.

The simulation platform provides a complete solution and takes into account most of the parasitics found in the testing platform. The only parasitics that were not included are the ones related to the anti-coupling capacitances which can be neglected by using high precision capacitors. Packaging effects were also included. The use of the HSpice 2D field solver to simulate the extracted transmission line gives an accurate result that will be easily reproduced in a future testing platform of the methodology.

Chapter 4

4 RESULTS

This chapter is divided in two sections: first section shows the results obtained from the testing platform and second section shows the results from the simulation platform where the optimization methodology was implemented.

4.1 Testing results

The ASIC was extensively tested and the functionality of all its blocks was verified. The design of VSMPL2 included a temperature independent current source that is digitally programmable using Labview. A test, including temperature variations on the chip, was done showing a linear relation of the DAC current with respect to the digital value, as shown in Figure 4.1. This linear behavior is very important for the optimization algorithm since the current given by the DAC determines the transmitting current of the transmitter and it also adjusts the termination impedance in the receiver. The transmitted current also needs to be immune to temperature variations to be able to accurately predict the power setting needed to achieve a target BER at any operating temperature. The temperature dependency test was also done and the results shown in Figure 4.2 show a high rejection to temperature variations of the DAC.

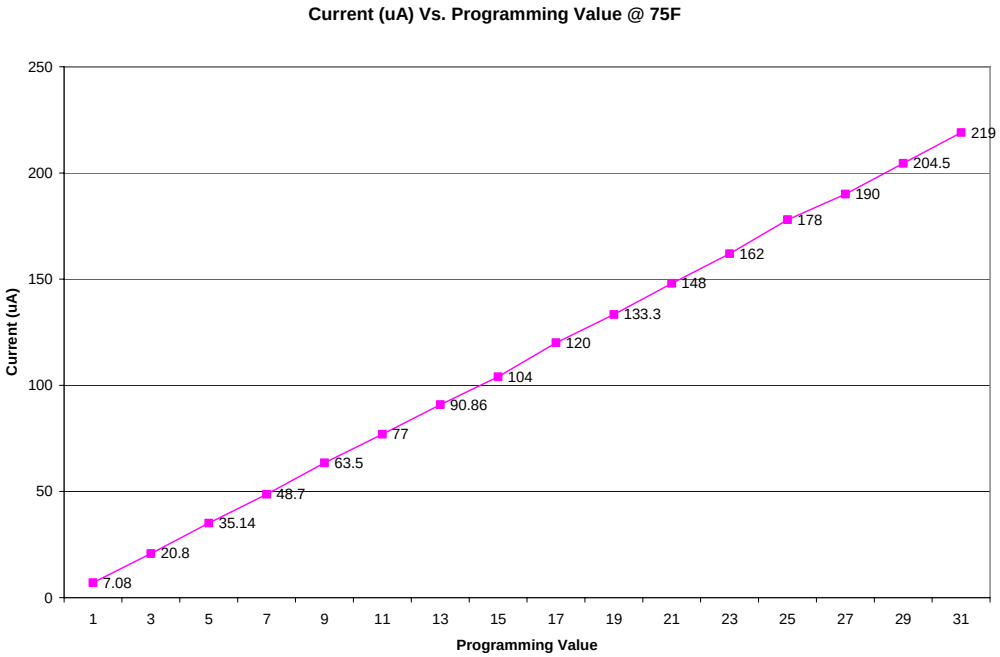


Figure 4.1 - Characterization of the DAC, the linear behavior of it is very important to the optimization algorithm since it determines the transmitting power and it also adjusts the value of the termination impedance.

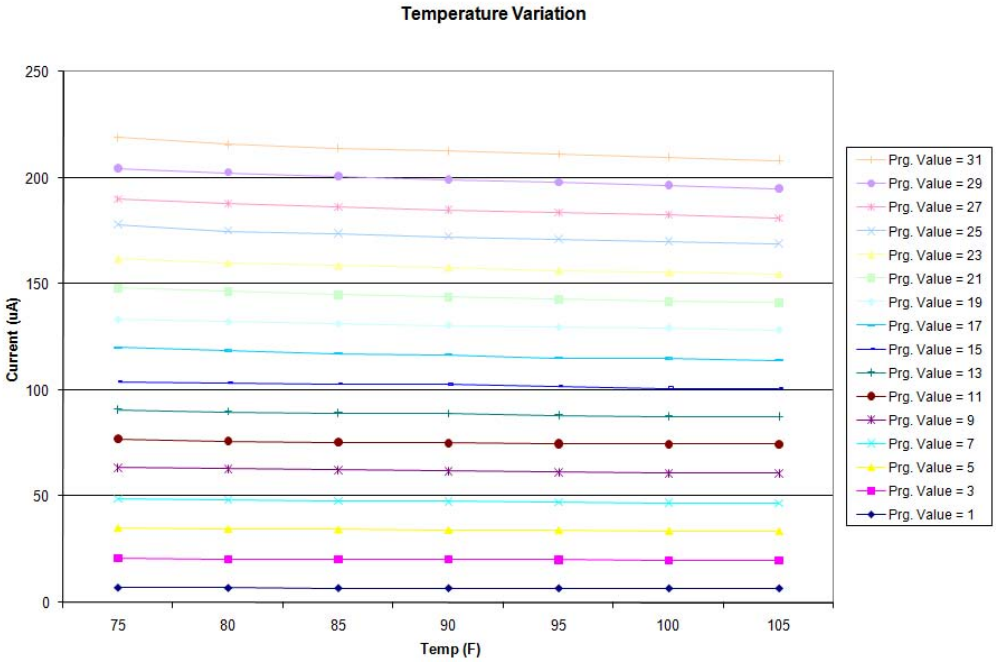


Figure 4.2 - The DAC showed a high immunity to temperature variations in the range of interest (75F-105F). The current value was hold of all the settings through the temperature range.

VCO and PRBS were also tested showing a total power consumption of 3W when the VCO was working at 10Gbps. Figure 4.1 shows the eye diagram of the VSMPL driver working at 2Gbps after one hour of operation.

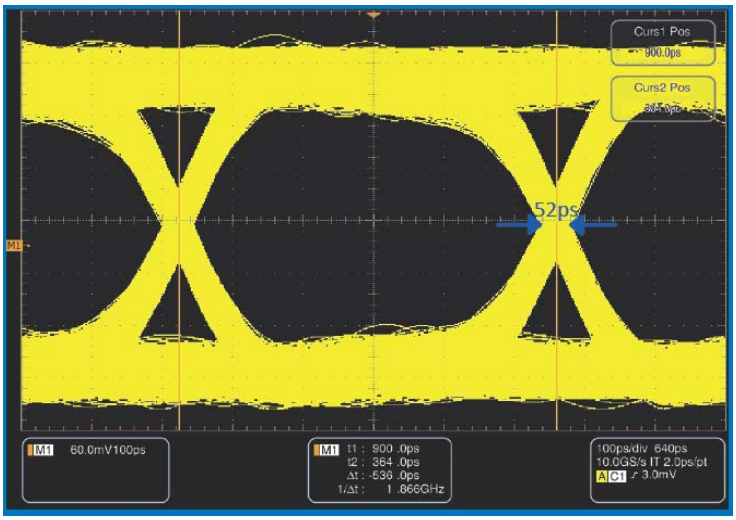


Figure 4.3 - 2.0Gb/s Link Eye measured after 1 hour of continuous operation VSMPL I/O Link

After testing the functionality of all the blocks, a test was performed using an external PRBS input and measuring the eye diagram and Bit Error Ratio for different power settings. Testing was also done for an individual channel with and without aggressors, meaning that its neighbor channels were on or off for each of the configurations. Figure 4.4 shows the eye diagrams for each case.

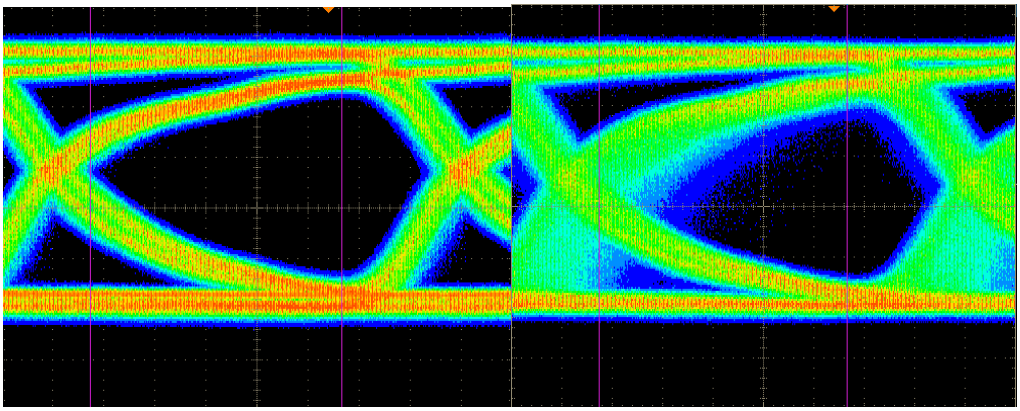


Figure 4.4 - The effect of crosstalk affects the quality of the signal which is reflected in its eye diagram. A 1Gbps communication with BER of 10E-12 (left) after affected by crosstalk interference had a measured BER of 10E-4 (right)

The effect in power increment for the same channel with or without aggressor is shown in Figure 4.5 where the BER measurement for each power level is shown. The graph shows that effectively the BER of a channel increases when the neighbor channels are active but more interestingly is the fact that as power increases, the difference between the two line increases too. This means that although increasing the power in a channel results in a decreased BER, if all the channels increase their transmission power, at some point, the BER will not improve any more. If power is further increased beyond this point the communication will only worsen.

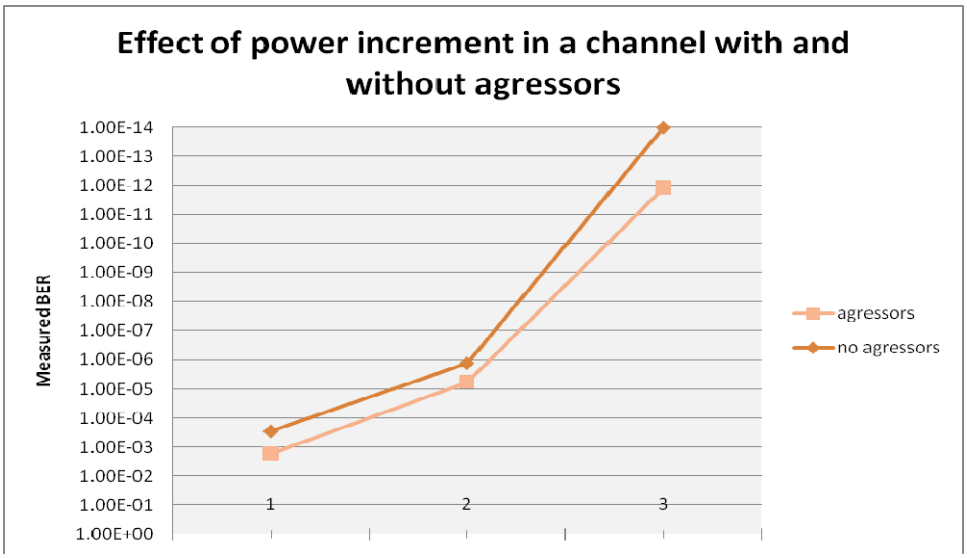


Figure 4.5 - Comparison of the effect of power increment in a channel without aggressors and with aggressors.

Testing results were also collected for a group of channels. Results for the minimum spacing configuration are shown in Figure 4.6. The graph shows the measured BER for each channel where the physical location of the channel matches the x-axis in the graph (channel 3 is the middle line in the bus). It can be noted that channel 3 that is in the middle of the bus, has a very low BER by default, therefore when the other channels are turned on, its BER although still higher than its neighbor's has decreased more significantly in percentage than the other channels, which means that the crosstalk effect is affecting it the most.

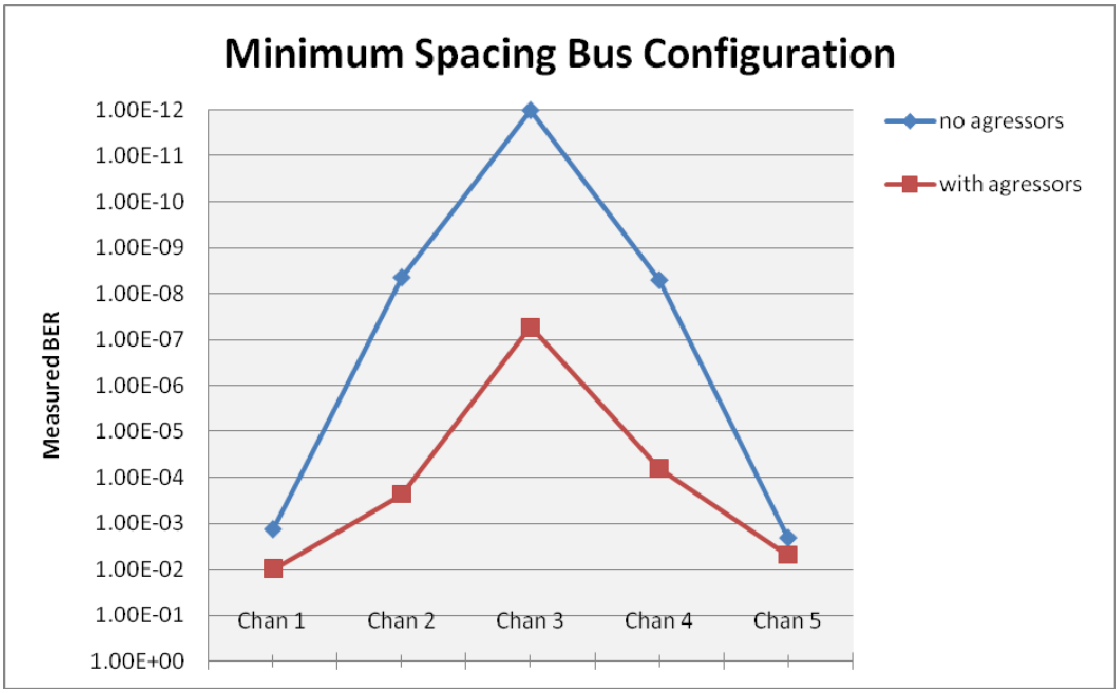


Figure 4.6 - Measurements of the BER for minimum spacing group were done on each individual channel using the same power for each line. All the traces were turned on at the same time and the BER was measured again. The effect of crosstalk was proportionally higher on the middle route.

Figure 4.7 shows the same situation but applied to the rule of thumbs configuration. In this case, even though there is still an effect on the channels produced by the aggressors activity, this effect is affecting equally all the channels.

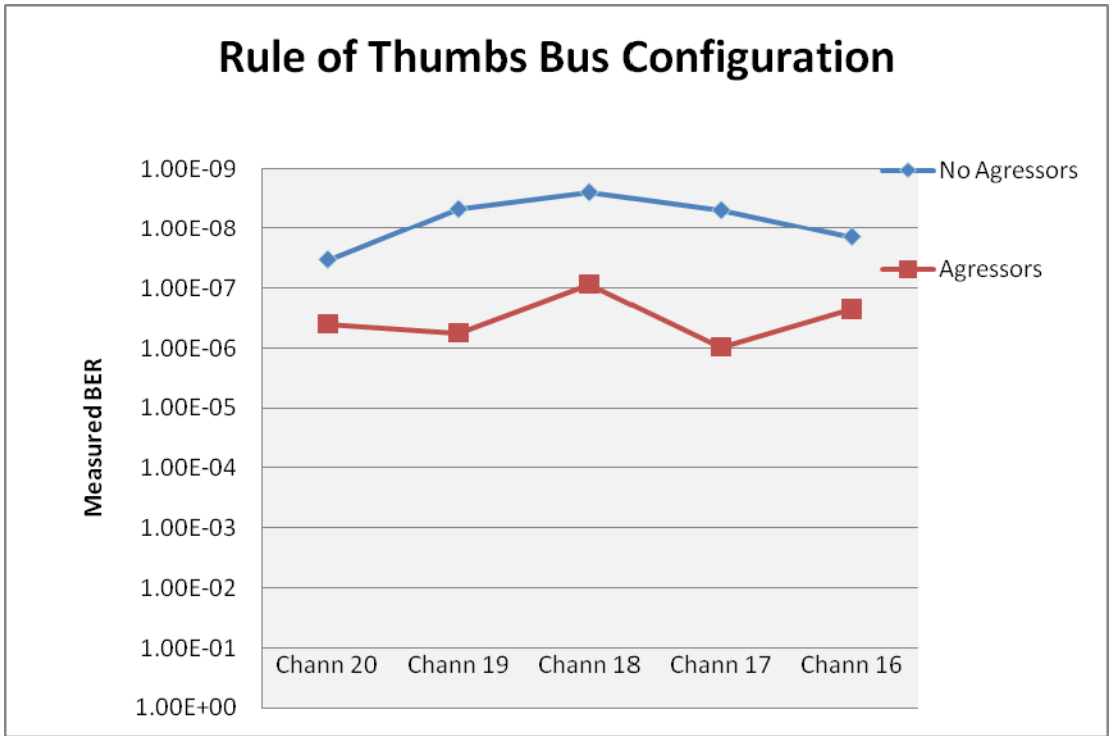


Figure 4.7- Measured BER for a rule of thumbs spacing configuration

4.2 Simulation results

The obtained testing results, especially with the minimum spacing, lead us go back to simulation the board to further analyze if the results were due to signal integrity issues embedded by the board or it is due to the communication channel and a positive feedback given by the algorithm itself. The first set of simulations used a CML and the eye diagram of each trace was obtained. Figure 4.8 shows the eye diagram at 1Gbps of an extracted trace that is driven by a CML transmitter.

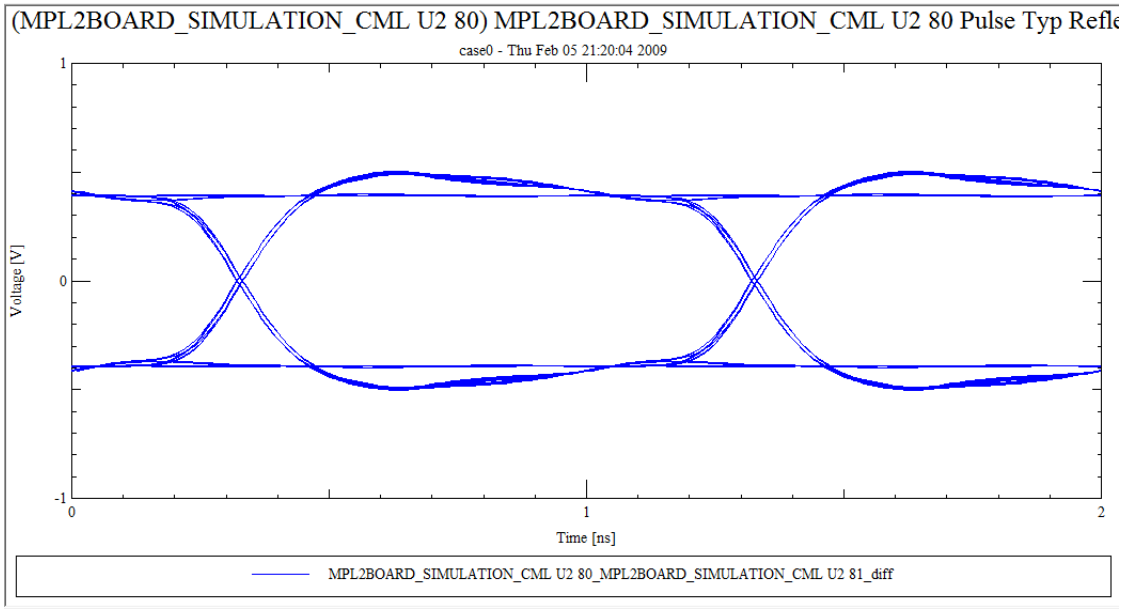


Figure 4.8 - Eye diagram at 1Gbps of one of the extracted traces of the fabricated PCB showing a good eye opening measured at the receiver

To be able to fully test the VSMPL algorithm by modifying the transmitter power and using the designed transceiver, the simulation platform described in Chapter 3 was used and given the intrinsic signal integrity problems of the designed PBC, a new PCB was generated. To minimize the crosstalk there are 4 different capacitors that can be tuned, shown in Figure 4.9. By fixing the value of three of them, Anti-C24=AntiC13=0.83pF and Anti-C14=0.34pF, and tuning only Anti-C23, which is cancelling the effect of the highest coupled lines, testing results that up to a 78% decrease in crosstalk voltage can be achieved at the receiver. The relationship between the value of Anti-C23 and the crosstalk voltage is shown in Figure 4.10.

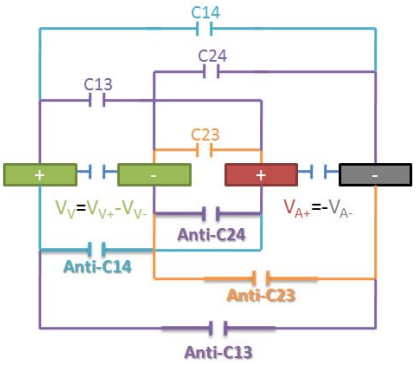


Figure 4.9 - Physical placement of anti-coupling capacitors. Since the major contribution from crosstalk is induced by the coupling between 2 and 3, the first simulation optimized the value of Anti-C23. All other capacitances had a fixed value, Anti-C24=AntiC13=0.83pF, Anti-C14=0.34pF

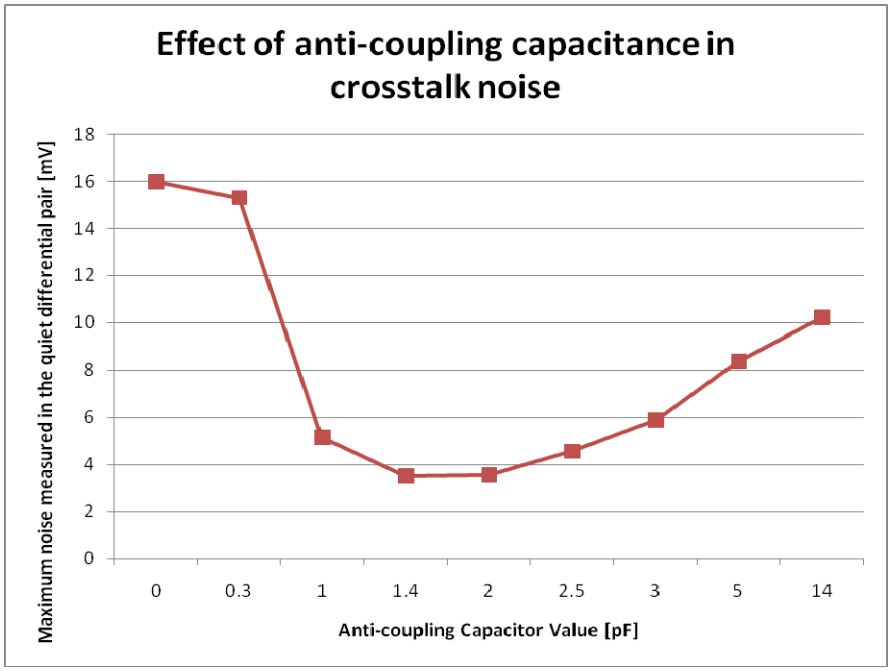


Figure 4.10 - 78% crosstalk voltage reduction by properly setting one of the anti-coupling capacitances and keeping all other capacitances fixed.

To measure the performance impact of crosstalk reduction using the anti-coupling capacitors, the same measurement of induced noise voltage due to crosstalk was taken but this time the spacing between the two channels was changed from 1X to 6X. X being the minimum spacing allowed by the technology between two lines. The simulation showed that to obtain the same noise reduction it is necessary to space the channels six times the minimum spacing, the results are shown in Figure 4.11. This means that using the anti-coupling capacitances, the bandwidth per unit area can be increased six times.

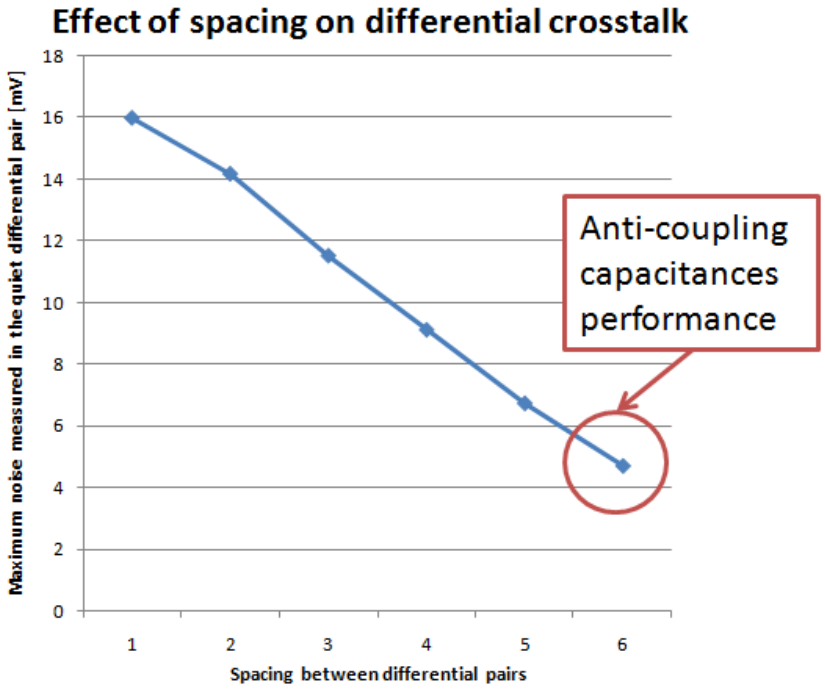


Figure 4.11 - To achieve the same cancelling effect of the anti-coupling capacitances it is necessary to space the channels 6X. X being the minimum spacing allowed.

The same comparison can be done by taking the Fast Fourier Transform (FFT) of the noise signals and measuring the spectral power for each configuration. Figure 4.12 shows the noise spectrum for three configurations: minimum spacing between channels without anti-coupling capacitances, 5X spacing between channels without anti-coupling capacitances and minimum spacing between channels adding the anti-coupling capacitances. When the lines are spread farther apart the noise spectrum is a scaled version of the noise in the minimum spacing case. But when the anti-coupling capacitances are added, the noise spectrum on the victim line is not only scaled but has a different shape. This effect is allowing the anti-coupling capacitances configuration to have a higher impact on noise reduction.

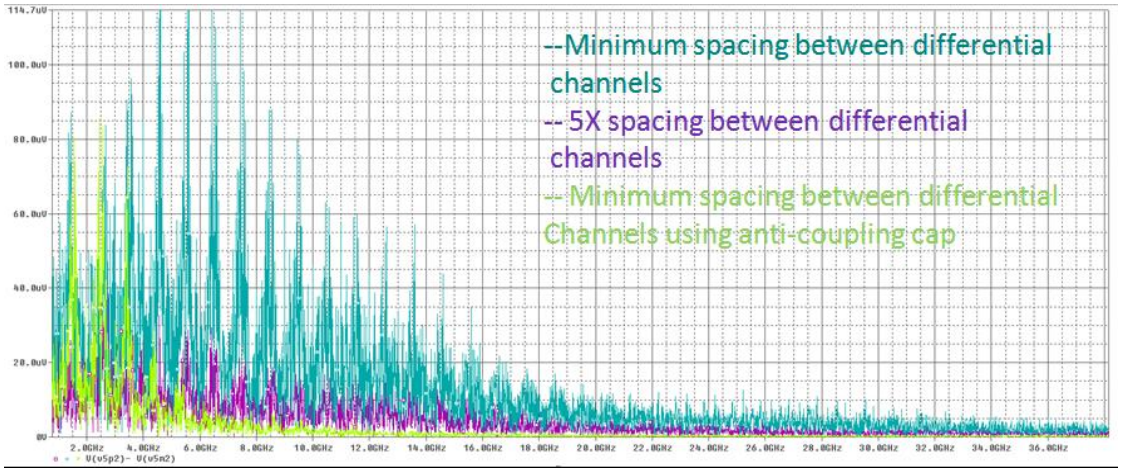


Figure 4.12 - The effect of adding the anti-coupling capacitance can be measured in the frequency domain by taking the Fast Fourier Transform of the signal induced by crosstalk on the quiet line. The effect of adding the capacitance is reducing the crosstalk noise in all frequencies.

The effect of the anti-coupling capacitances was also measured in time domain for Far End Crosstalk and Near End Crosstalk. The results are shown in Figure 4.13 and Figure 4.14 respectively. The time domain effect can be seen by a reduction of induced noise when the anti-coupling capacitors are placed.

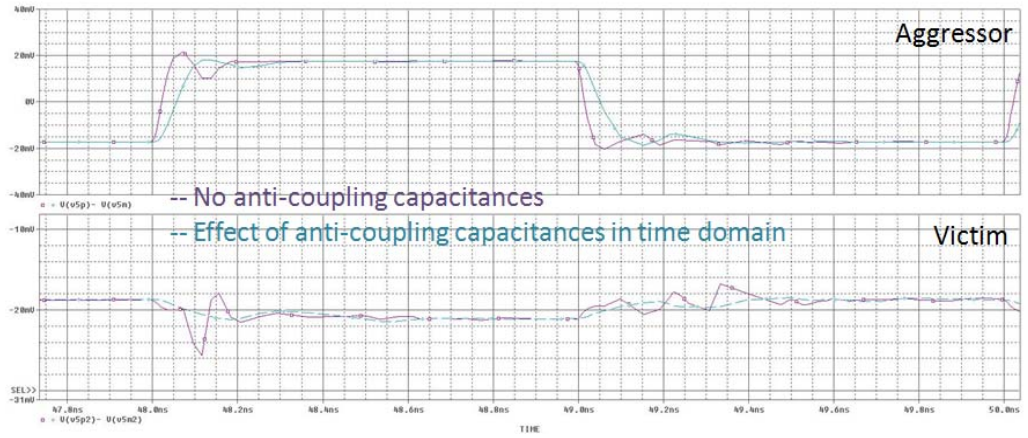


Figure 4.13 – Time domain Near End crosstalk,

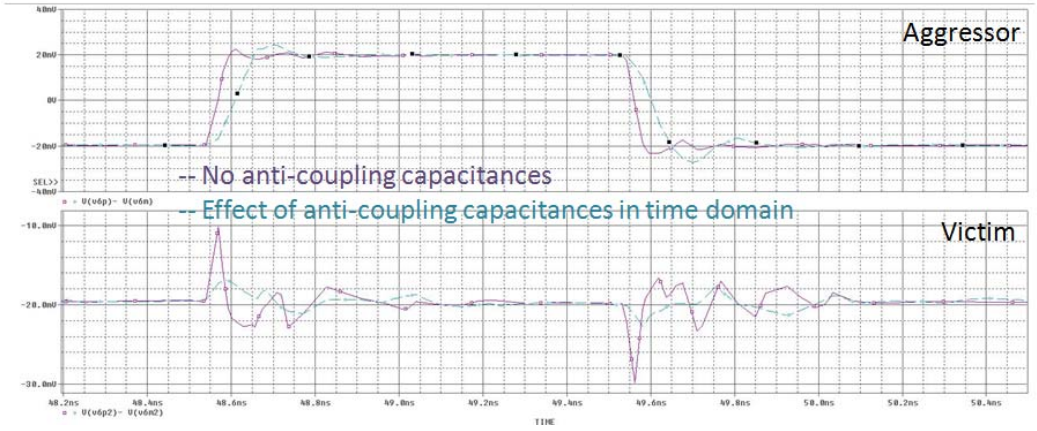


Figure 4.14 - Time domain, Far End crosstalk

The improvement of the eye diagram was also measured by a simulation in which the aggressor channel had a higher transmitter power than the victim, The results are shown in Figure 4.15. The eye diagram of the victim signal was measured showing an improvement in both, height and width of the eye. The jitter measured for the configuration without the anti-coupling capacitors was 140ps and the jitter measured for the anti-coupling configuration was 17ps, an improvement of 87% in jitter was obtained using the anti-coupling capacitors.

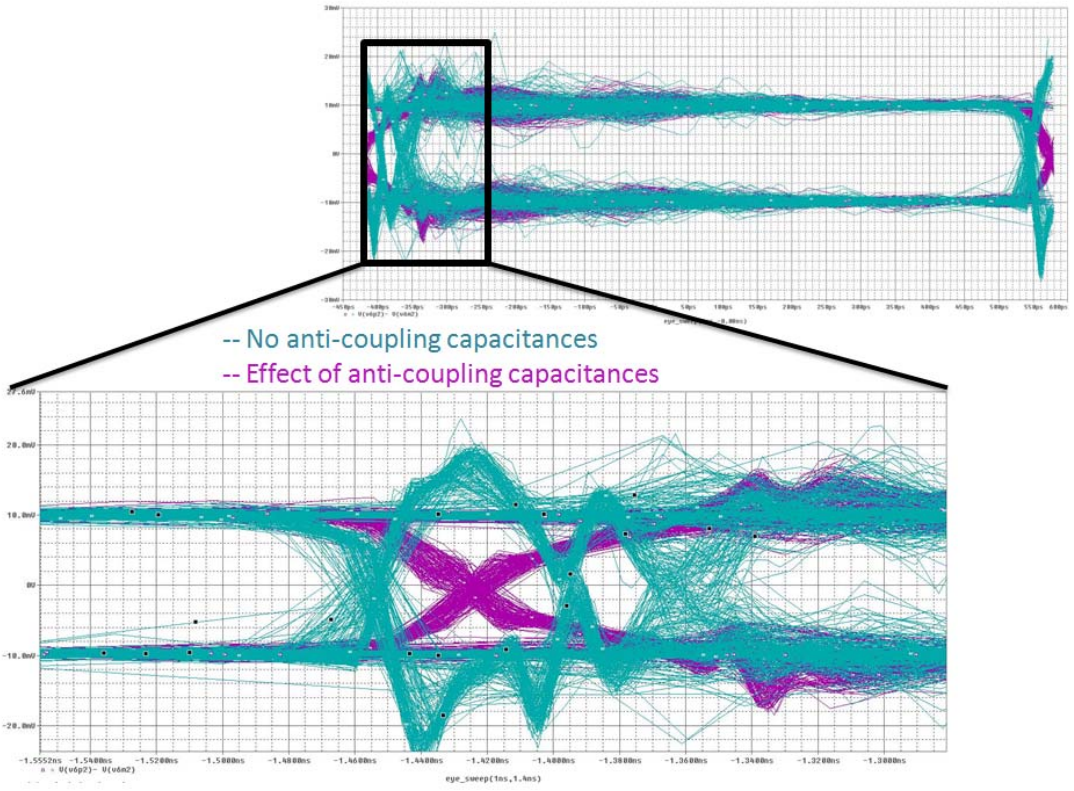


Figure 4.15 - Adding the anti-coupling capacitors increased the eye height and width. Meassured jitter without capacitors is 140ps and with the capacitors it was reduced to 17ps

Since the optimization algorithm based on accelerated BER measurements will tune the value of the capacitors to find the minimum BER that can be achieved, it is required to demonstrate that the function of noise power converges to a minimum, when the value of the capacitors is changed. Several simulations were run to illustrate it and they were plot with using Matlab. Figure 4.16 shows the crosstalk noise power measured at the near end when two of the capacitors (Anti-C24 and Anti-C13) were fixed at 0.83pF and the other two were swept in a rage from 0 to 2pF. The graph shows that the noise power is minimized for a range of capacitor values, this is better explained in Figure 4.17 where the top view of the function is shown. Darker areas indicate that the power is lower and bright color areas indicate that the measured power is higher. The lowest crosstalk noise power that can be achieved is 0.7mW compared with 3.3mW obtained without the anti-coupling capacitances, which translate in a reduction of 79% of the noise power.

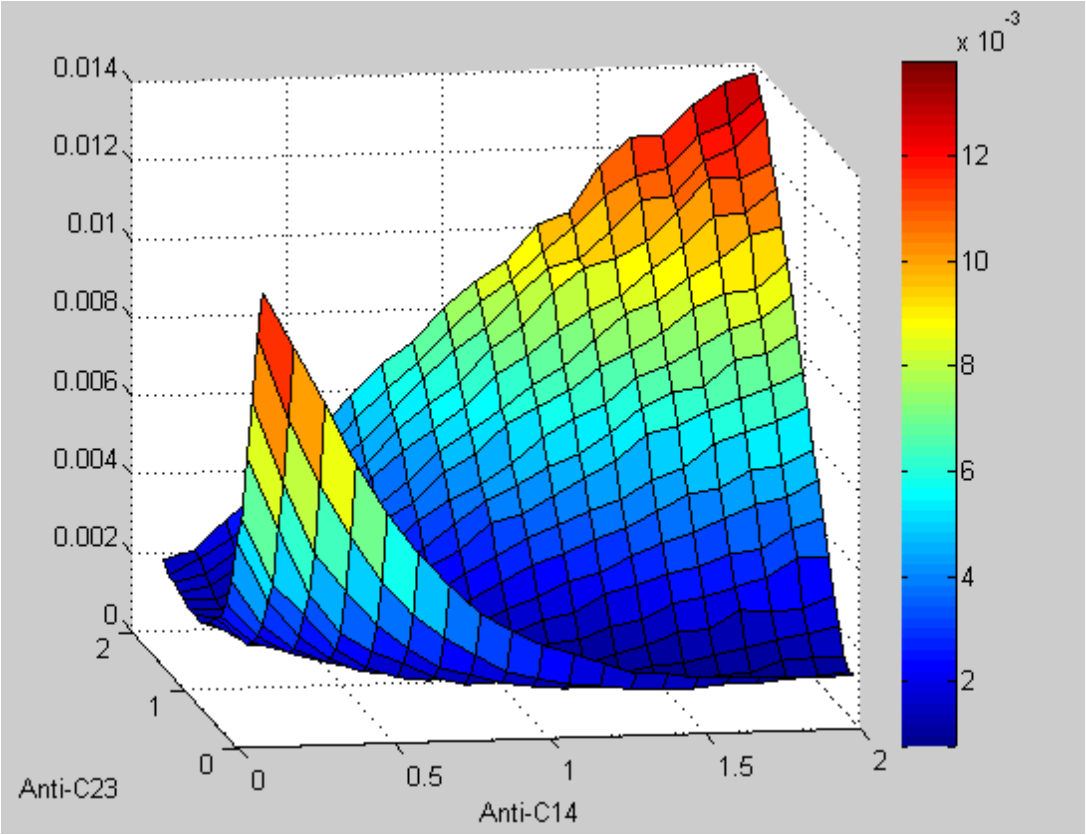


Figure 4.16 - Power measured at the victim line as a function of the value of two anti-coupling capacitors

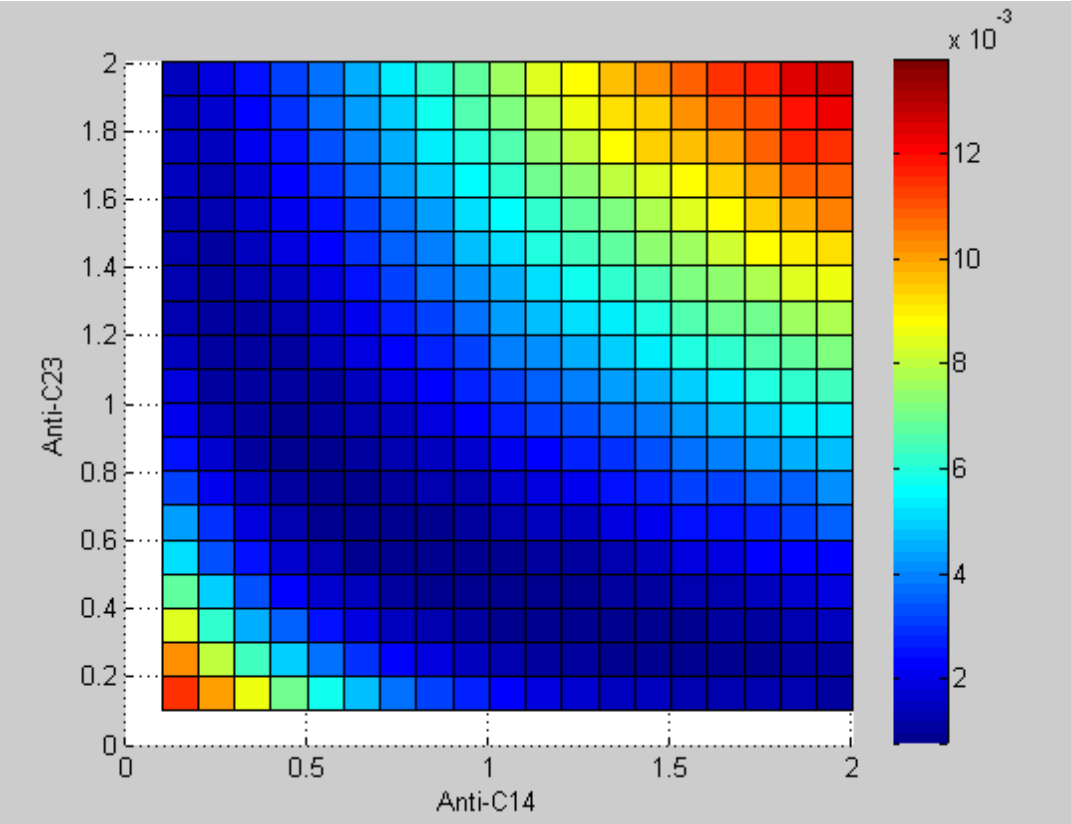


Figure 4.17 - Top view of the noise power measured at the victim when the value of Anti-C14 and Anti-C23 are changed.

To obtain a symmetrical response, and minimum crosstalk noise in both channels, Anti-C14 and Anti-C23 should have the same value; therefore the optimization procedure can be easily implemented in hardware. If both capacitors have the same value and the value of Anti-C24 and Anti-C13 must be equal too, the function now becomes a two variables function. Several simulations were run to characterize the noise power response when the capacitors had the same value and the result is shown in Figure 4.18. The minimum crosstalk noise power obtained in this

case was 0.4mW that compared with the no-capacitors configuration results in a 87% reduction in power of crosstalk noise.

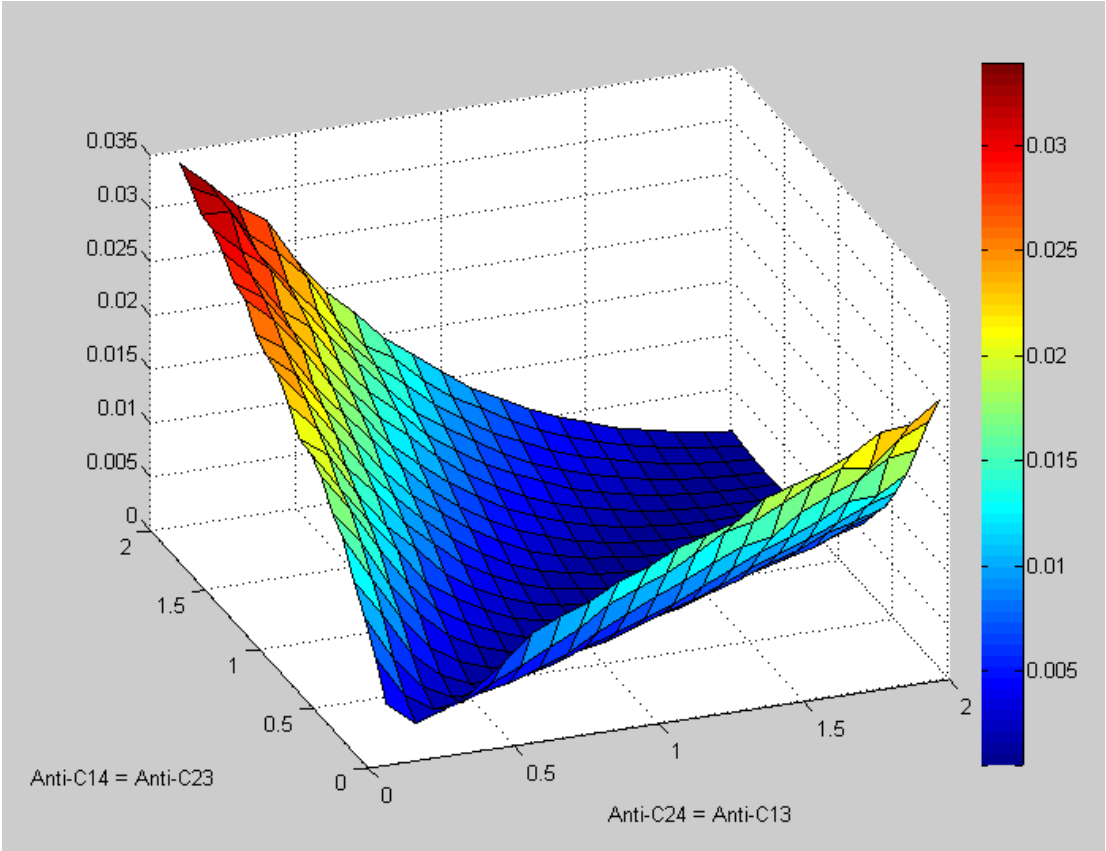


Figure 4.18 - Noise power at the victim channel when Anti-C24=Anti-C13 and Anti-C14=Anti-C23. Minimum noise power obtained is 0.4mW compared with noise power of 3.7mW without the anti-coupling capacitances. An improvement of 87% can be achieved using the proper value of the capacitors.

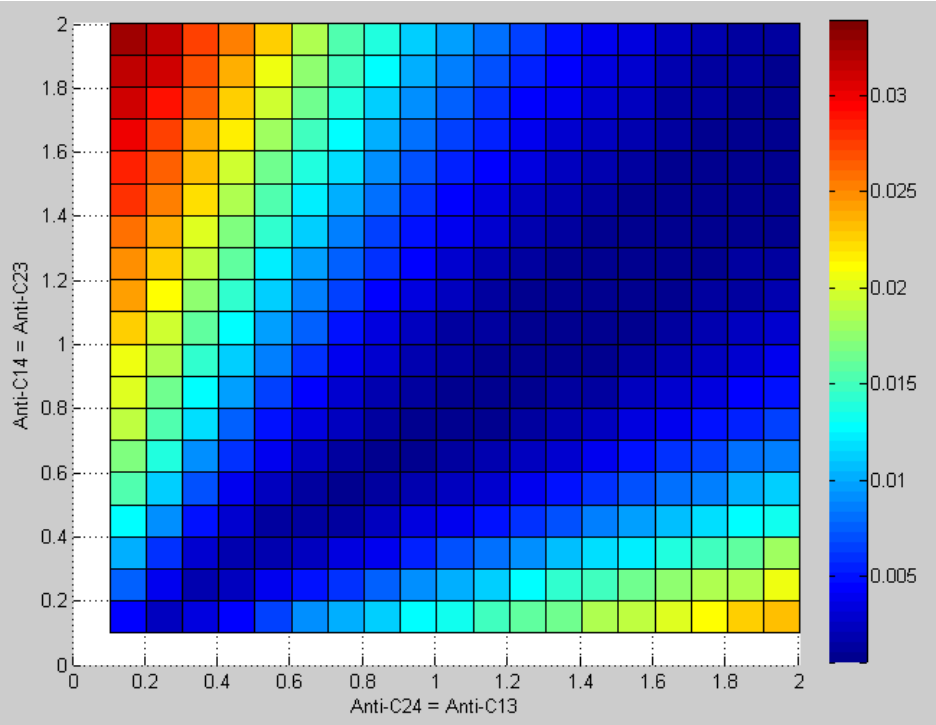


Figure 4.19 - A noise reduction of 87% can be obtained by tuning the values of the anti-coupling capacitors.

Finally, a simulation of two channels routed as close as possible, each of them running at 10Gbps at the lowest power was run using the anti-coupling capacitance. Distance between the two lines was the minimum allowed by the manufacturer. The eye diagram of the signal after the receiver amplification is shown in Figure 4.20 which proves that the implementation of a high speed dense parallel link is possible using the optimization methodology described in this dissertation.

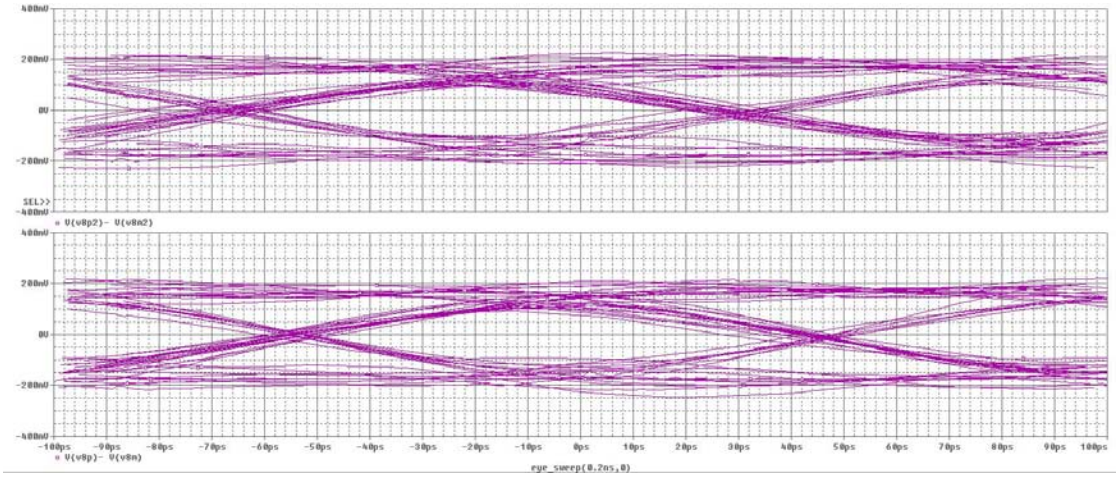


Figure 4.20 - Successful implementation of two channels routed as close as possible, each channel was transmitting at 10Gbps and the crosstalk noise was minimized by the use of the anti-coupling capacitances.

Chapter 5

5 CONCLUSIONS

The optimization methodology presented in this work uses an accelerated BER measurement to automatically optimize the signal integrity and power of a differential parallel link. A novel technique to reduce the crosstalk between adjacent channels was presented using anti-coupling capacitances. Until now, the method that has been used to reduce crosstalk is spacing the lines farther apart, creating a space limitation for bandwidth-per-unit-area.

The purpose of the anti-coupling capacitors is to cancel out the crosstalk voltage induced by the mutual impedances in the transmission lines. In a differential pair, one of the lines is closer to the aggressor therefore receiving more crosstalk noise. The anti-coupling capacitors are set such that the other line will receive the same amount of crosstalk noise, and at the differential receiver the total common noise is negligible thus the effect of crosstalk is successfully minimized.

The technique to minimize the crosstalk noise was implemented in a simulation platform that provided: extraction tools to simulate the routed paths in a 6 layers FR4 PCB, a 2D solver to simulate the transmission lines interaction, and transistor level simulation for the transceivers circuits and for all packaging parasitics. This simulation platform provides reliable results that accurately predict performance in hardware implementation.

The implementation of the anti-coupling capacitances provided encouraging and satisfactory results showing an improvement of 78% in noise power

using a simple optimization algorithm for the values of the capacitors. But simulation results showed that a maximum of 87% reduction of noise power can be achieved by properly selecting the values of the anti-coupling capacitors.

To measure the impact of the results comparing them with the traditional solution to minimize crosstalk, the same measurement was performed spacing the lines. The results showed that to achieve the same performance, the lines need to be spaced six times the minimum spacing allowed by the manufacturer. This means that the implementation increases six times the bandwidth-per-unit-area in a parallel link communication.

Simulation results of two differential channels, each of them transmitting at 10Gbps and routed as close as possible, provided satisfactory results in terms of the eye diagram. Thus, the implementation of the anti-coupling capacitances is decreasing the size of devices, while allowing higher data rates for chip to chip communications. This provides a solution for high performance computing by addressing the bottleneck of off-chip memory transactions. It also benefits mobile devices as smaller form factor components can be built.

After the channels are electrically un-coupled, they can be treated as serial links. In that case, the implementation of a power optimization algorithm for each line is possible and the final result is a dense high-speed parallel link optimized for minimum power consumption.

Through the development of this work, we noticed that the accelerated BER measurement gives a new perspective to electrical interconnect designers since it opens new possibilities of dynamically improving performance of the link according to its specific needs. Specifically, the power can be minimized to achieve the lowest

power consumption, the crosstalk noise can be mitigated and the reflections on the line can be reduced.

Further work should consider the implementation of the algorithm using an FPGA, since some FPGA developers already have the capability of adjusting the power of the transceivers, or selecting a proper termination resistor, like Rocket IO. This capability is meant to be set during the design stage, but given the flexibility of an FPGA system it could be modified to use it during the operation.

The implementation of the optimization algorithm in an FPGA is also simple since the BERT is usually a given component by the manufacturers or it could be easily implemented in VHDL. The only addition needed in the system is the anti-coupling capacitances that can be placed off-chip.

Improvement of the optimization methodology is possible in several stages. A better optimization algorithm can be implemented using optimization techniques to allow a faster convergence. More capacitances can also be added to allow the implementation of the crosstalk reduction for longer paths.

The effect of the anti-coupling capacitances in the bandwidht of the transmission lines needs to be considered. Since the value of the capacitances reduces the rising and falling times of the signal, the anti-coupling capacitances must be modified for applications requiring a rising time higher than 10ps.

On-chip communications can also benefit from the methodology proposed in this dissertation. While the medium is different and different considerations need to be assumed, small modifications can lead to higher performance of the on-chip interconnects.

Several communications that are being done today use single ended configurations, like LVTTL, LVCMOS, PCI, and DDR. Since this work only provides a solution for differential links, a similar implementation using the accelerated BER measurement for single ended configurations should be studied.

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