SRI International

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Covering the Period 1 November through 30 November 2009

POWER MEMS DEVELOPMENT

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SRI Project P19063

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Prescribed by ANSI Std Z39-18

ACTIVITIES AND PROGRESS

MEMS RESETTABLE CIRCUIT BREAKER (TASK 1.1) AND MEMS SWITCH FOR DC-DC VOLTAGE CONVERTERS (TASK 1.2)

Task 1.1 Contributors: Susana Stillwell, Sunny Kedia, Weidong Wang

Task 1.1 Deliverable: 10 prototype packed MEMS-based resettable circuit breakers for testing and analysis in ONR laboratories.

Task 1.2 Contributors: Sunny Kedia, Shinzo Onishi, Scott Samson

Task 1.2 Deliverable: Functional MEMS-based DC-DC converter in a vacuum package.

Task 1.1 and Task 1.2 Progress:

Short Loop Experiments

During this period we completed one short loop experiment to verify the use of chromium (Cr) as a hard mask for silicon dioxide (SiO_2) wet etching. This Cr hard mask was used during the fabrication of the Indent layer in the process flow. For this experiment, we deposited 3 µm of SiO_2 on the wafer and then sputtered a layer of Cr. We patterned and etched the Cr, creating the hard mask, and then etched the SiO_2 using a 6:1 buffered oxide etchant. The Cr made an excellent hard mask in our process. Figure 1 is a scanning electron microscope (SEM) image of the ~3 µm undercut of the SiO_2 using the Cr hard mask, this undercut is expected with an isotropic wet etch.

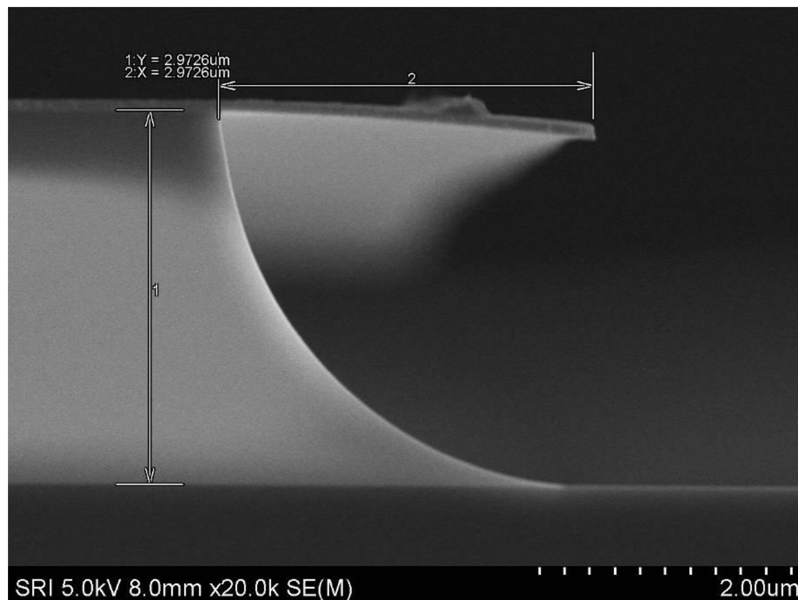


Figure 1: SEM image showing ~ 3 µm undercut and Cr hard mask.

Fabrication

With the short loop experiments, described above and in last period, completed, we began full loop wafer processing using the previously developed process flow which incorporates two wafers, one silicon double-sided polished (DSP) and one silicon-on-insulator (SOI), which will be bonded together using our EVG wafer-to-wafer bonding tool to complete the devices.

The DSP wafer was completely processed using the Indent, Metal 1, Metal 2 and Singulation (dicing lines) mask layers. SEM images of the DSP wafer with the four completed layers prior to wafer-to-wafer bonding are shown in Figure 2 and Figure 3. As noted last period, the masks and process flows incorporate structures for both Task 1.1 and Task 1.2 (MEMS Switch for DC-DC Voltage Converters) on one pair of wafers.

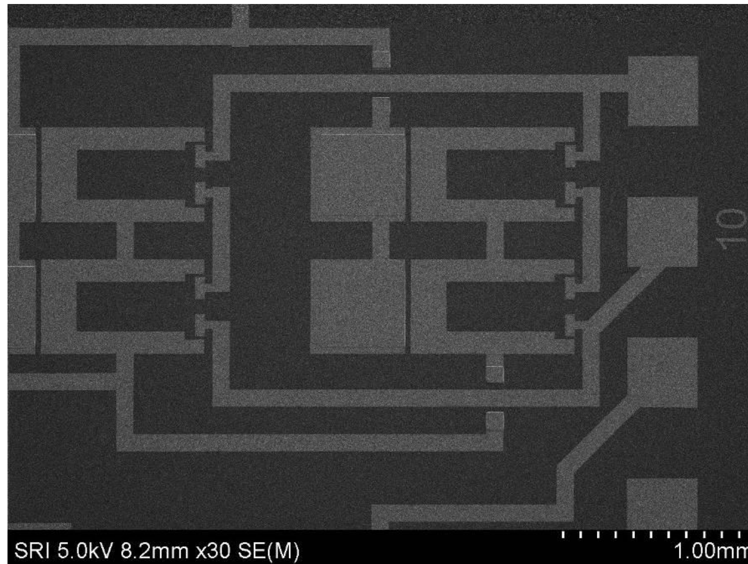


Figure 2: SEM Image of Task 1.1 structures fabricated on DSP wafer prior to bonding

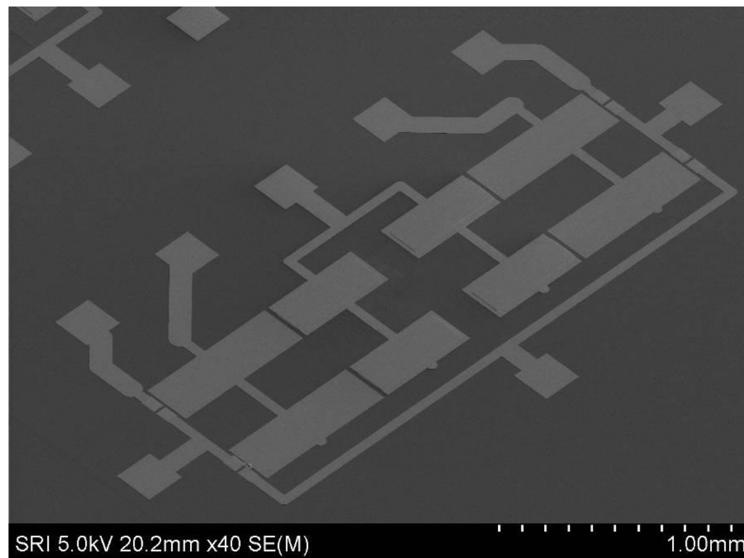


Figure 3: SEM Image of Task 1.2 structures fabricated on DSP wafer prior to bonding

Processing of the first SOI wafer was also finished and included the Oxide, Metal 3, 4, 5, Cantilever, and Release mask layers. Representative structures from this wafer are shown in the SEM images in Figure 4 and Figure 5.

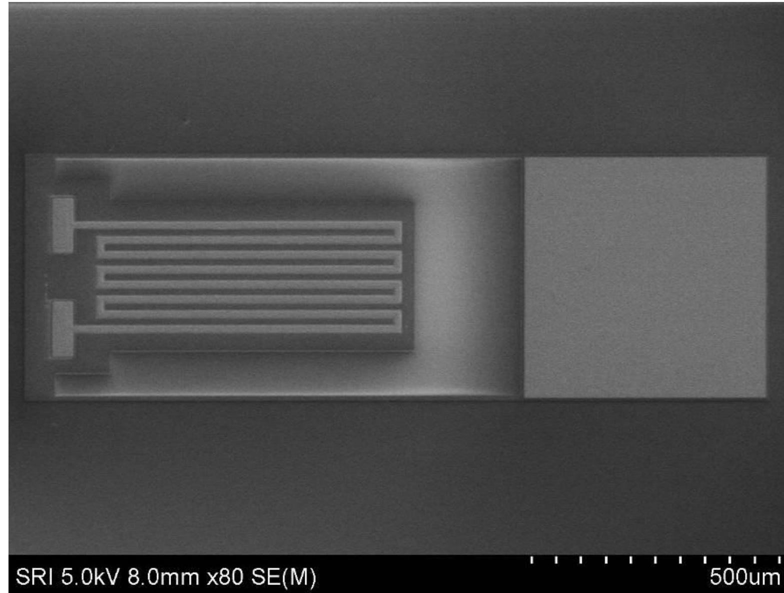


Figure 4: SEM Image of Task 1.1 structures fabricated on SOI wafer prior to bonding

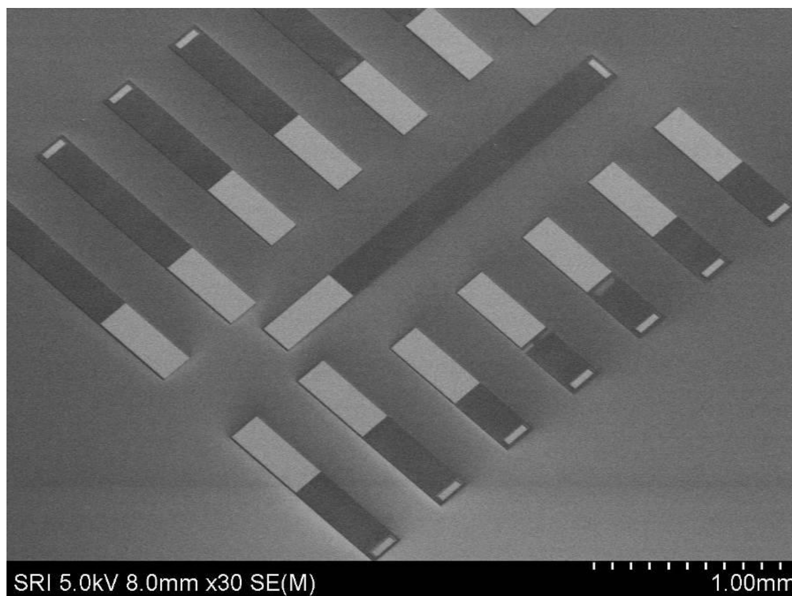


Figure 5: SEM Image of Task 1.2 structures fabricated on SOI wafer prior to bonding.

The DSP and SOI wafers were successfully bonded together using a gold-gold (Au-Au) thermocompression bonding process. The handle Si of the SOI wafer was removed using deep

reactive ion etching (DRIE). We measured the profile of the released cantilevers with a Wyko optical interferometer and found significant bow in the structures shown in Figure 6. We then used reactive ion etching (RIE) to remove the exposed buried oxide layer layer, alleviate the stress, and expose the Si cantilevers.

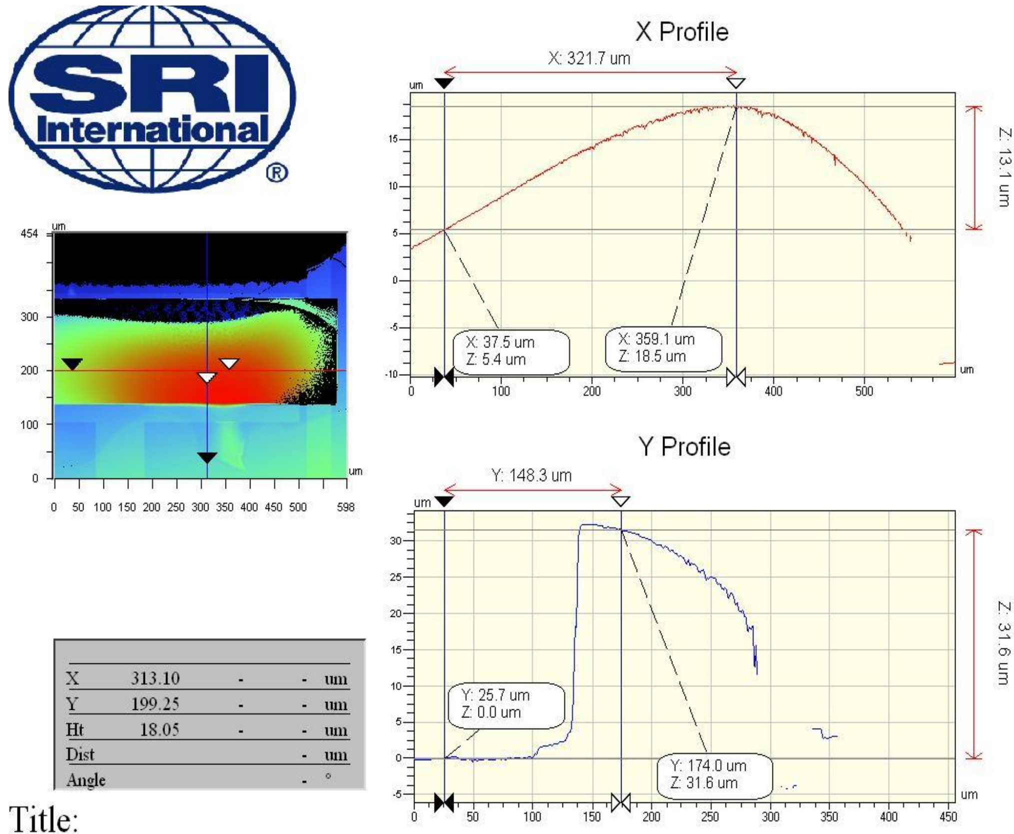


Figure 6: Wyko Interferometer data for cantilever after DRIE of handle Si.

Testing (Wafer Level)

After completing the RIE, the circuit breaker cantilevers were bent upwards as shown in Figure 7, where the raised tip/end and the rest of the cantilever are out of focus. The change in focus shows that the end and anchor of the cantilever are not in-plane with each other. This may be due to either the bimorph effect of the heater element on the underside of the cantilever or residual stress in the films. The heater is composed of silicon dioxide and platinum, which both have coefficients of thermal expansion (CTE) that are different from that of silicon. This CTE mismatch would cause the cantilevers to bend upwards. Electrical probing showed that the heater/electrostatic pads were not shorted. However, up to 100 V was applied to the electrostatic actuation pads and no movement was observed.

Figure 7: Optical microscope image of circuit breaker after RIE showing the tip of the cantilever in focus and the contact pads below out of focus due to the upward bend in the released cantilevers

After RIE, the voltage converter cantilevers were not as bowed as the circuit breaker cantilevers. Figure 8 is a 3D Wyko image illustrating the different shapes and sizes of cantilevers that were incorporated in the design. The smaller cantilevers (400 µm and 600 µm) were flatter than the longer cantilevers. The cantilevers show a bow or bend in the middle and are very close to the contact pad at the end.

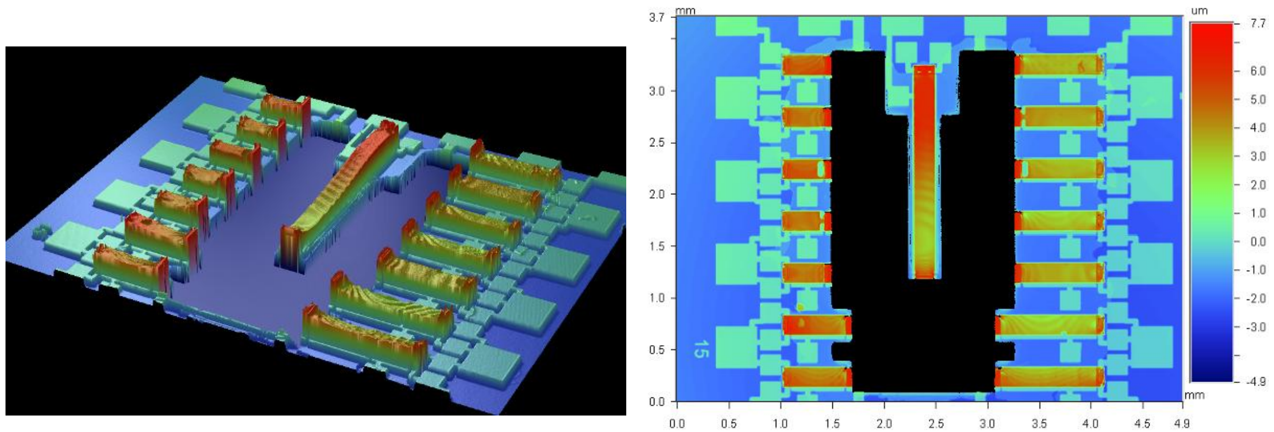
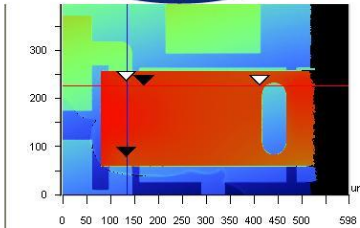
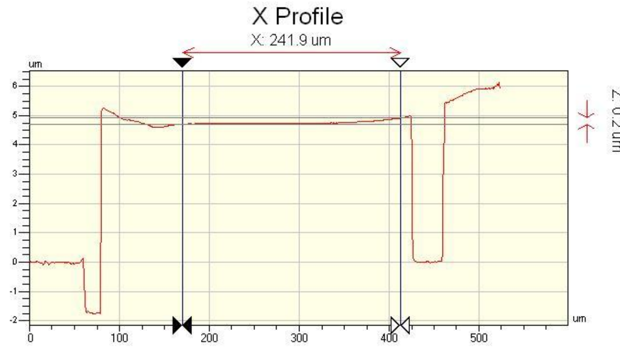


Figure 8: Wyko image of voltage converter cantilevers after RIE.

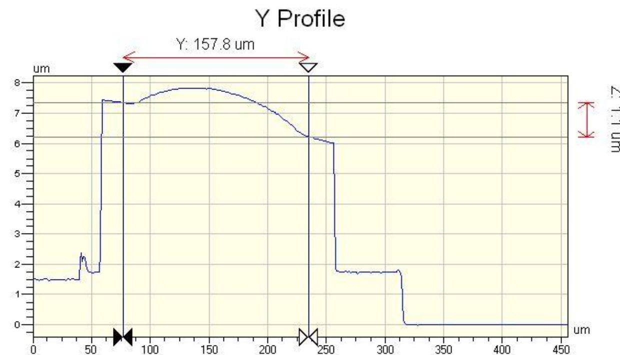
Figure 9 is a profile of a 400-µm-long cantilever, which after RIE is flat to the bottom electrode, while the contact area at the end of the cantilever is curled upwards. However, upon application of voltage to the contact area of the cantilever, the end did not have much motion; the center section moves (at 30-35 V) and sticks down to the bottom electrode. This phenomenon was observed in most of the short cantilevers.





Rq	0.05	um
Ra	0.03	um
Rt	0.22	um
Rp	4.91	um
Rv	4.69	um

Angle	888.89	urad
Curve	93.96	mm
Terms	User Fit	
Avg Ht	4.75	um
Area	1147.17	um2



Rq	0.45	um
Ra	0.36	um
Rt	1.63	um
Rp	7.85	um
Rv	6.22	um

Angle	-7.19	mrad
Curve	-2.77	mm
Terms	User Fit	
Avg Ht	7.41	um
Area	1166.98	um2

X	134.19	-	-	um
Y	224.86	-	-	um
Ht	3.65	-	-	um
Dist			-	um
Angle			-	°

Title:

Figure 9: Wyko image of voltage converter cantilever after RIE.

Finite Element Modeling

We simulated the circuit breaker cantilever using ANSYS finite element analysis (FEA). Figure 10 shows the bottom view of the model with different materials: light green is the Si cantilever, red is Au anchor (bonding material), purple is thermal SiO_2 for temperature compensation and electrical isolation, and blue is platinum (Pt) heater. Only half of the structure was modeled since it is symmetric about the center line of the cantilever (i.e., XZ plane). We have performed thermal-stress analyses to investigate the bending of the cantilever. During the simulation, we applied a uniform temperature across the entire structure and used different reference temperatures to simulate the high-temperature processing steps. The anchor was set at zero displacement, and a symmetric boundary condition was applied to the center line of the cantilever.

Figure 11 shows the cantilever has a 59.9 µm upward bending at room temperature (20°C) after application of an 800°C reference temperature. Figure 12 shows the parametric simulations for maximum cantilever Z-displacement vs. different reference temperatures, using thermal SiO_2 thickness as the parameter. As shown, higher reference temperature corresponds with larger bending. Also, thicker SiO_2 causes greater bending. We will perform more simulations to evaluate what variations of thickness and structure shape will provide the cantilevers with minimum bending and will apply the results to the next iteration of fabrication and mask design.

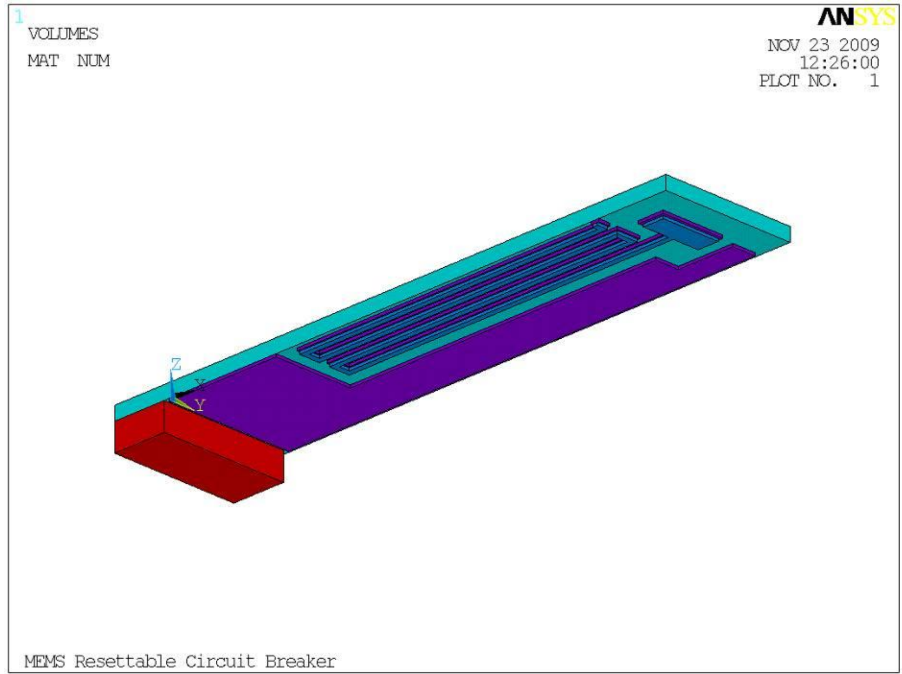


Figure 10: FEA model of the cantilever structure

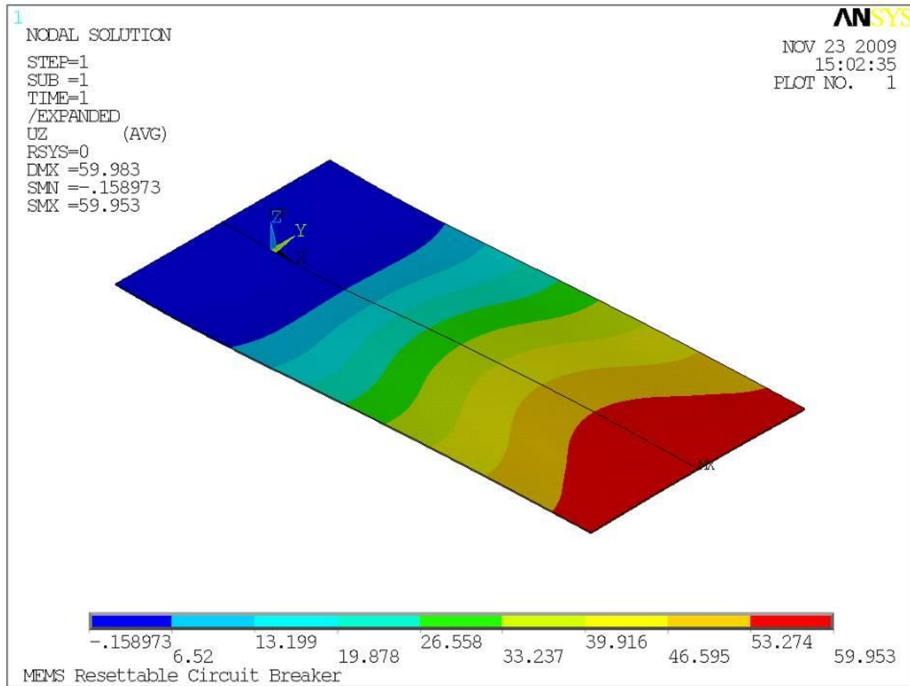


Figure 11: FEA simulation shows an upward bending of the cantilever

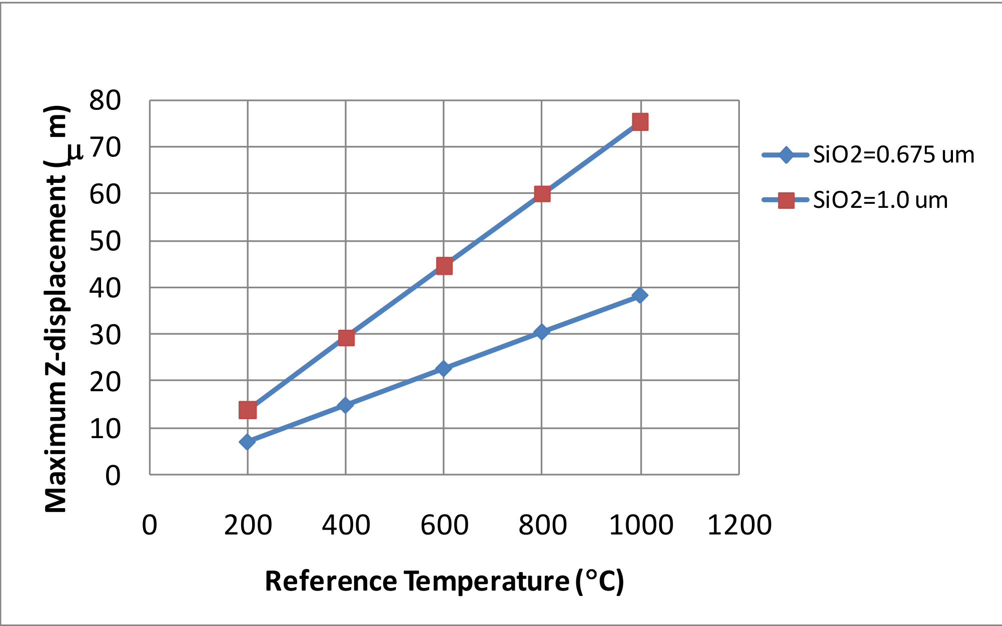


Figure 12: Parametric simulation

DIAMOND HEAT SPREADER OR HEAT SINK FOR HIGH POWER MEMS SWITCHES APPLICATIONS (TASK 1.3)

Contributors: Priscila Spagnol, Shinzo Onishi, Drew Hanser, John Bumgarner

Deliverable: Prototype device fabricated on a thin-film diamond heat spreader layer and individual samples of diamond on Si or other suitable substrates for material evaluation.

Progress:

During this reporting period we made several design changes to the 3-omega circuit configuration in order to isolate the 3-omega voltage on the measurement resistor and improve the signal-to-noise ratio. We made these changes after performing measurements that resulted in data that differed from the expected values reported in the current literature. Several circuit configuration iterations (presented in Figure 13) were used and considered to improve the collected data.

We measured thermal conductivities of a Pyrex substrate and silicon substrates with thermally grown SiO_2 layers with thicknesses of 240 nm and 50 nm using the 2-terminal bridge circuits; however, the thermal measurement data were not as expected when compared to published results for measurements on similar wafers. Upon analysis, it was determined the measurement system we were using could not eliminate the end effects of the heated wire in the measurement resistor. In addition, the measurement system could not provide good null compensation and a poor signal-to-noise ratio contributed to the discrepancy in the data. A new circuit design was needed to address these problems.

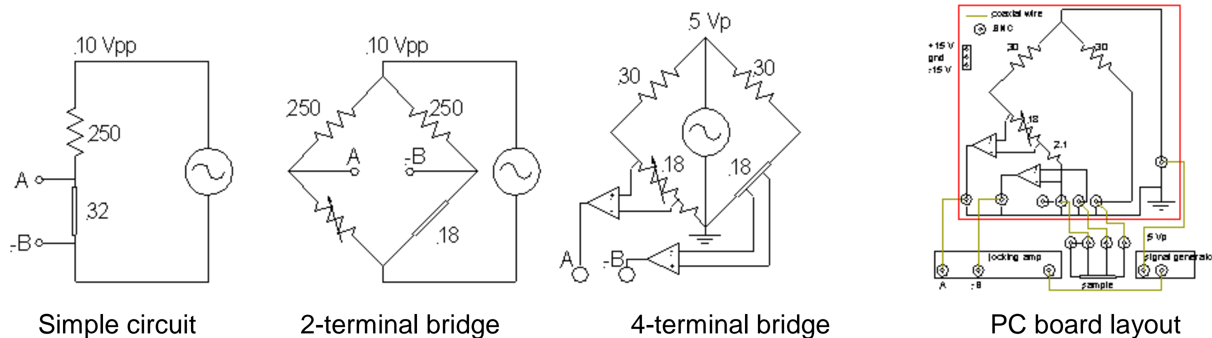


Figure 13. Circuits developed to improve the 3 omega measurements.

Figure 13 shows three schematic diagrams of the circuits used for measurement of the 3-omega voltage signal ($V_{3\omega}$) and the PC board layout of the 4-terminal bridge circuit. A simple circuit was used initially for measuring $V_{3\omega}$ across the metal line heater using a lock-in amplifier and a signal generator. An Agilent 33250A signal generator was used to supply the sinusoidal current, and a Signal Recovery 7280 DSP lock-in amplifier was used to measure the non-equilibrium 3ω voltage of the balanced bridge circuit, which generated the $V_{3\omega}$ voltage signal. The initial circuit configuration did not sufficiently isolate the $V_{3\omega}$ voltage signal from the primary voltage signal (V_{ω}). We improved the configuration by using a 2-terminal bridge, which allowed us to subtract V_{ω} from the voltage across the metal line resistor, improving the signal. Upgrading to a 4-terminal bridge circuit, we eliminated the end effect of the metal line heater by allowing the end part of the metal line to be excluded from the measurement. Since the lock-in

amplifier has only one pair of differential input terminals, a double differential amplifier front end was required in a 4-terminal bridge circuit operation. A potentiometer is also used to balance the bridge circuit, and signals are fed to two instrumentation differential amplifiers with unity gain. Based on this circuit design, a 4” x 4” PCB board (Figure 14) was designed to improve the signal from the 3ω circuits to the bridge circuits using BNC connectors. The circuit design has been completed and the components and PC board have been ordered.

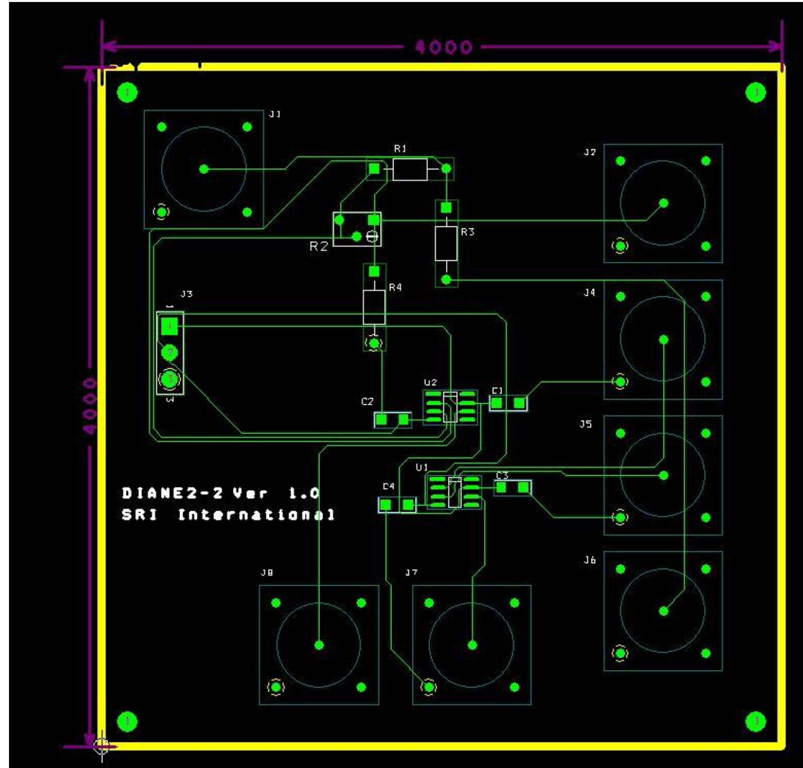


Figure 14. PC board design.

Preliminary Results

We used a Pyrex wafer, a SiO_2(50 nm)/Si wafer and a SiO_2(240 nm)/Si wafer to evaluate the system. The thermal conductivity of the samples remained at 0.2 to 0.35 W/m·K, but these values were expected to vary from 0.7 to 1.7 W/m·K as reported in the literature. As described above, a new circuit configuration was designed to improve the measurements.

POSITRON TRAPPING AND STORAGE (TASK 2)

Contributors: Ashish Chaudhary, Friso van Amerom, Tim Short

Deliverable: A minimum of four MEMS-based trap structures for RF trapping of electrons

Progress:

Simulations

We performed simulations on SIMION software using hyperbolic DC end caps to determine if they have any electron focusing effect that would help to improve the trapping time. We observed no significant changes in the electron trajectory during reflections at hyperbolic end caps. Trapping time was comparable to the design with straight DC end caps.

We performed a finite element analysis in SolidWorks COSMOxpress to determine the design of the chip separation mask that would be sufficient to withstand the helium backside pressure in the DRIE chamber used to keep the wafer cool during etching. For large windows of Si etched at the boundary, this results in a significant force on the Si. A set of 250- to 350-µm-wide Si bridges were incorporated to enhance the structural stability of Si during DRIE operation. A 3x safety factor was used to determine if the DRIE separation mask design was adequate.

Figure 15 shows the Si chip design and the DRIE separation mask. The Si bridges, shown in the figure, will be removed after the DRIE step by diamond scriber or a roller on a flat plate. Figure 16 shows the displacement plot of the Si structure with 8 Torr backpressure. The deformation scale (vertical axis) has been scaled by a factor of 204 to show in the image.

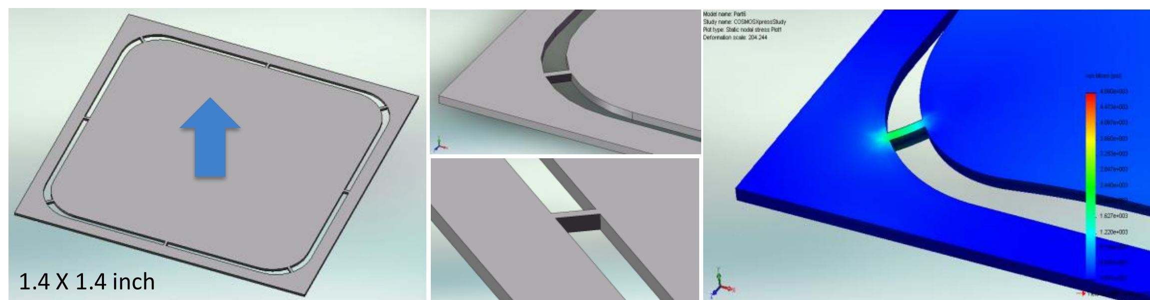


Figure 15 Left: Chip separation design with a street of Si etched all the way around the Si chip to achieve separation; **Center**: Close-up of the Si bridge for mechanical stability; **Right**: Stress plot of the Si chip showing the region of maximum stress, which is in green and is half of the yield value.

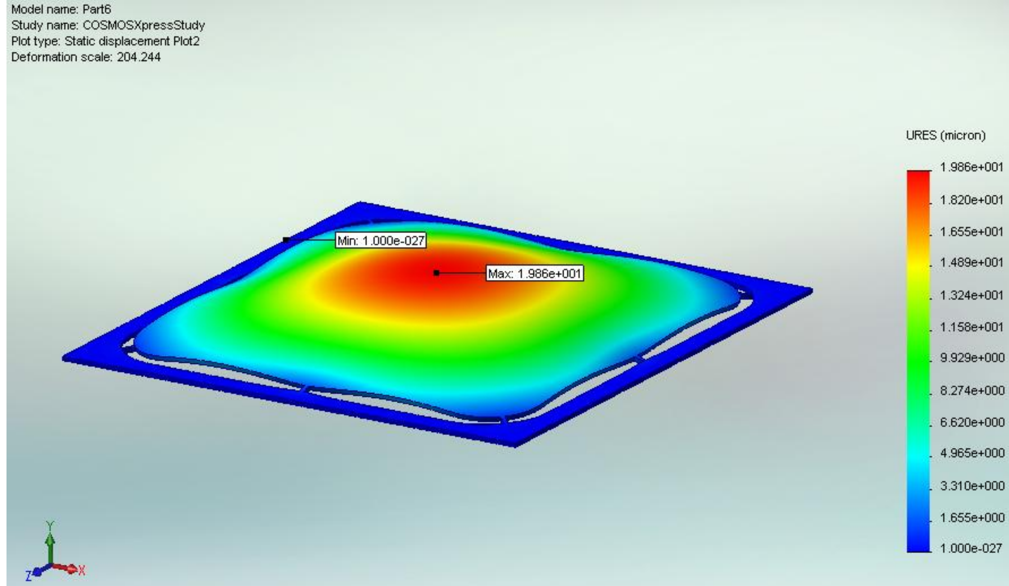


Figure 16: Displacement plot of the Si structure showing a maximum displacement of 20 µm at the center of the die and less than 1 µm near the edges.

Table 1 shows a summary of the bridge designs and factor of safety (FOS). The information in this table will be used for the full wafer fabrication.

Table 1: The bridge design and the respective FOS. 300-µm-wide Si bridges (4 at corners and 4 at sides) would be required to achieve a satisfactory FOS (>3)

Part Name	Wafer (um)	Bridge Location	Bridge width (um)	Pressure (Torr)	Pressure (PSI)	Load style	FOS
Part 3	350	4 Corners	300	8	0.154	Normal to Face 1	1.392
Part 4	350	4 Corners	350	8	0.154	Normal to Face 1	1.49
Part 5	350	4 Corners + 2 sides	350	8	0.154	Normal to Face 1	2.22
Part 6	350	4 Corners + 4 sides	350	8	0.154	Normal to Face 1	3.56
Part 7	350	4 Corners + 4 sides	300	8	0.154	Normal to Face 1	3.33
Part 8	350	4 Corners + 4 sides	250	8	0.154	Normal to Face 1	2.95

Short Loop Fabrication Experiments

a) Wet etch rates of 75 nm zinc oxide (ZnO) layers grown by atomic layer deposition using 1% aqueous hydrochloric acid (HCl) were measured at 11-15 nm/s using photoresist as a mask.

b) Wet etch rates of the same ZnO in the PR developer RD6 were measured to be 2.25 nm/min. This range of etch rates is low enough and thus does not require protecting the ZnO layer with PR during a 45 s development of PR in RD6 in a subsequent lithography step.

c) We determined the etch selectivity of low-pressure chemical-vapor-deposited silicon nitride (Si_3N_4) to Si in our DRIE tool to be 106:1 with an etch recipe that etched the bulk Si at 0.85 µm/Bosch cycle.

Results of the short loop experiments are shown in Table 2.

Table 2*:* Summary of the results of the short loop experiments described above

Measured	Value
Etch rate of Si_3N_4 in RIE	30 nm/min
Etch rate of Si in DRIE	0.85 um/cycle
Etch rate of PR1 2000 in RIE	18.75 nm/min
Etch selectivity of Si_3N_4:Si	1:106
Etch rate of ZnO in 1% HCL in H_20	11-15 nm/sec
Etch rate of ZnO in developer RD6	2.2.5 nm/min

First Fabrication Run

We finalized the mask layout and ordered and received the mask set. We started the first device fabrication run based on the process flow developed and the results of the short loop experiments. The first two photolithography steps have been performed. We expect to finish the process run by the first week of December.

Test Setup

We assembled the main frame of the test setup using Kimball Physics eV parts based on the assembly as illustrated in Figure 17. We ordered the phosphor screen, the silicon photomultiplier, and the driving electronics.

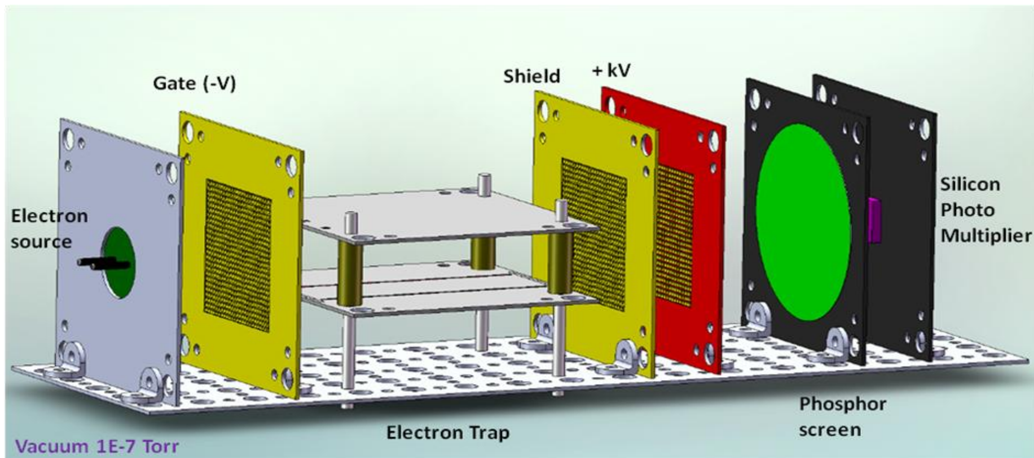


Figure 17: 3-D model of the test setup conceptualized for RF electron traps.

FINANCIAL STATUS

R&D Status Report

Program Financial Status

15 July 2009 through 21 November 2009

Contract Item No.	Current Funding	Current Period Expenses	Cumulative Expenses	% Budget Complete
0001	$1,829,849	$71,231	$384,635	21%
Project Commitments		(1,526)	258,509	
Total	$1,829,849	$69,705	$643,144	

Based on currently authorized work:

Is current funding sufficient for the current fiscal year (FY)? (Explain if NO) **Yes**

What is the next FY funding requirement at current anticipated levels **N/A (base fully funded)**