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14. ABSTRACT
Metal contacts to semiconductor nanowires share similarities with their thin-film counterparts, but they also exhibit important differences due to geometry. For example, in the formation of platinum silicide contacts to silicon nanowires, it is possible to achieve uniform platinum silicide/silicon segmented nanowires, but some ratios of platinum to silicon and annealing conditions lead to a peculiar kinking of the nanowires not analogous to the thin-film case. Also interesting is the effect of geometry on Schottky barrier contacts to semiconductor nanowires,

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Problem Statement

Nanoscale contacts are required for a wide variety of electronic and optoelectronic devices. This report describes contacts to semiconductor nanowires from both the point of view of how the nanoscale geometry affects the reactions of metals with the semiconductor nanowires and how the nanowire geometry affects the electrical characteristics of the contacts.

Interfacial Reactions in Metal/Silicon Nanowires

Part of this research program was devoted to the study of the interfacial reactions between metal contacts and silicon nanowires, focusing on metals used in the study of the electrical properties of the contacts.

Pt Contacts to Si Nanowires

The SiNWs used by Bangzhi Liu in the study of Pt contacts to Si nanowires were grown using the vapor-liquid-solid (VLS) technique by Prof. Joan Redwing's research group.[1] The nanowire diameters were widely distributed between 20 and 100 nm following VLS growth catalyzed by a thin Au film deposited on an oxidized Si wafer. To prepare the nanowire for Pt deposition, as-grown samples were treated in buffered oxide etch for 1–2 min to remove the native oxide, then rinsed in DI water, blown dry with N_2, and loaded promptly into an electron-beam evaporation chamber. Platinum films of 20 and 50 nm thicknesses were evaporated at a base pressure of 10^{-7} Torr. After deposition, samples were annealed under gettered N_2 in a tube furnace at temperatures between 250 and 700 °C for 5–60 min. The NWs were then released from the wafer on which they were grown using sonication and put on lacey carbon films for observation by TEM using a JEOL 2010F TEM. Strikingly different morphologies of the reacted nanowires were observed by TEM, depending on the annealing temperature, platinum film thickness, silicon nanowire diameter, and level of unintentional oxygen contamination in the annealing furnace.

After annealing at 250 °C for 1 h, only a slight interfacial reaction was observed, with most of the Pt and Si remaining unreacted. However, some silicide formation was con-

firmed through selective etching experiments. One such nanowire is shown in Fig. 1. The extent of reaction increased after annealing for 1 h at 350 °C, with larger silicide grains forming. When the annealing temperature was raised further, however, a new phenomena was observed not associated with the thin film case.

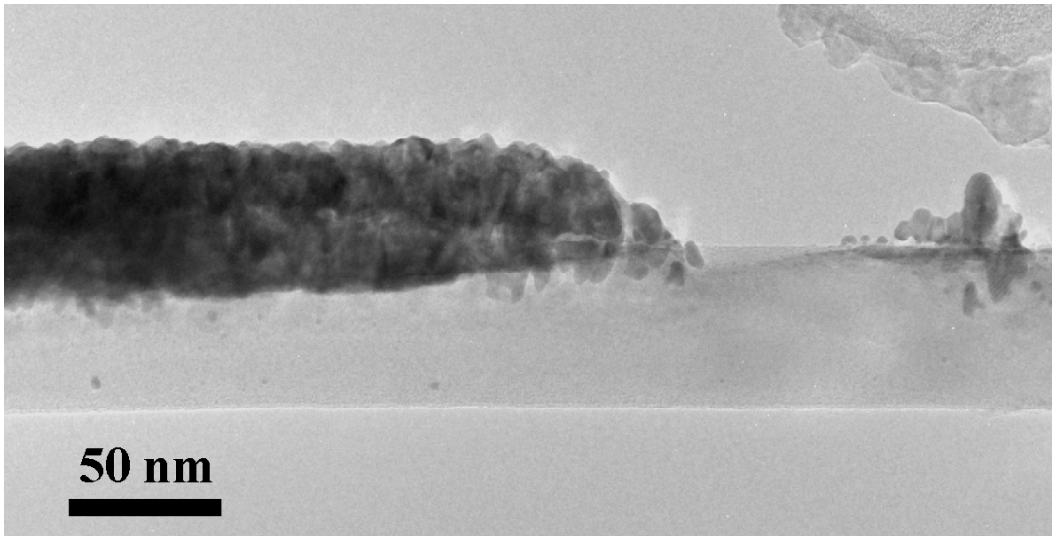

Figure 1. TEM image showing a SiNW with Pt on it after annealing at 250ºC for 1h.

Figure 2 shows a SiNW on which 50 nm of Pt was deposited before annealing at 550 °C for 45 min. The morphology of the reacted nanowire was irregular, and the nanowire exhibited kinks. Electron diffraction patterns showed that Pt_2Si was the predominant phase formed along with PtSi, and all Si was consumed. This high Pt/Si ratio is linked to the unusual morphology shown in the figure, as explained later in this report. We reduced the Pt film thickness to 20 nm in our next experiments.

The samples with 20 nm Pt were annealed at 350 °C or higher, since only slight interfacial reaction was observed in the samples with 50 nm Pt annealed below 350 °C. Full consumption of Pt was observed when the samples were annealed from 400–700 °C for 30 min. The uniformity was improved above 450 °C, and a large number of SiNWs were converted into smooth PtSi NWs with diameters between 35 and 45 nm. The typical morphology shown in Figure 3 is desirable for nanowire devices and fundamental contact

studies. This morphology is also more suitable for field effect transistors with metal nanowire contacts. Large nanowires with lower Pt/Si ratios retained some unreacted Si along with the PtSi.

The morphology we observed depended on the starting SiNW diameters and the amount of metal deposited, or alternatively, the atomic ratio between Pt and Si. The uniformity of the silicided NWs was strongly correlated to the Pt/Si ratio in the sample. The phase PtSi was predominant in the uniformly-silicided NWs with Pt:Si atomic ratios near 1:1, but Pt-rich conditions led to the formation of Pt_2Si and irregularly-shaped NWs.

Considering the crystal structures of Si and the platinum silicide phases, we note that when we have complete silicidation and formation of PtSi, the resultant PtSi volume is 1.49 times that of the original SiNW (corresponding to a diameter increase of 1.22 times). This case is common for our samples with 20 nm Pt deposited. When Pt is in excess, however, the Pt_2Si phase forms. Its volume is about 2.29 times that of the initial silicon volume. This large increase in volume may cause a stress during silicidation, forcing the silicided NWs to bend and kink, as observed in Fig. 2.

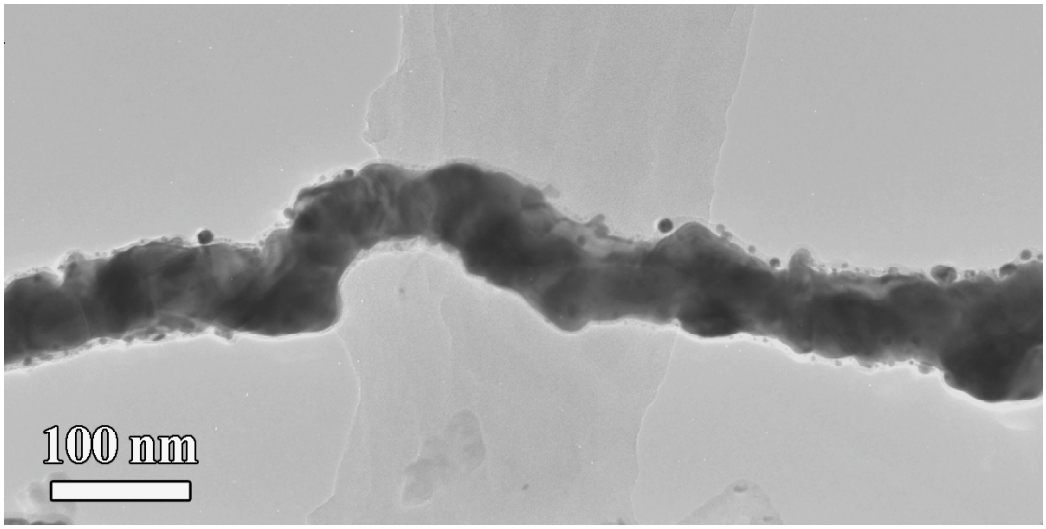

Figure 2. TEM image showing the result of the reaction of a 50 nm Pt film on a SiNW annealed at 550ºC for 45 min. The reaction product is Pt_2Si.

One other important characteristic of the reaction of thin Pt films on Si wafers is an extreme sensitivity to low levels of oxygen in the annealing environment, due to the ability of Pt to catalyze the oxidation of Si. This SiO_2 formation occurs between the silicide and Pt, and it reduces the rate of reaction or can even stop it completely. This effect was more pronounced in the nanowire case compared to thin film control samples. This work on the formation of platinum silicides was presented at the AVS meeting in November 2006 and reported in 2007 in *Nano Letters*.[2]

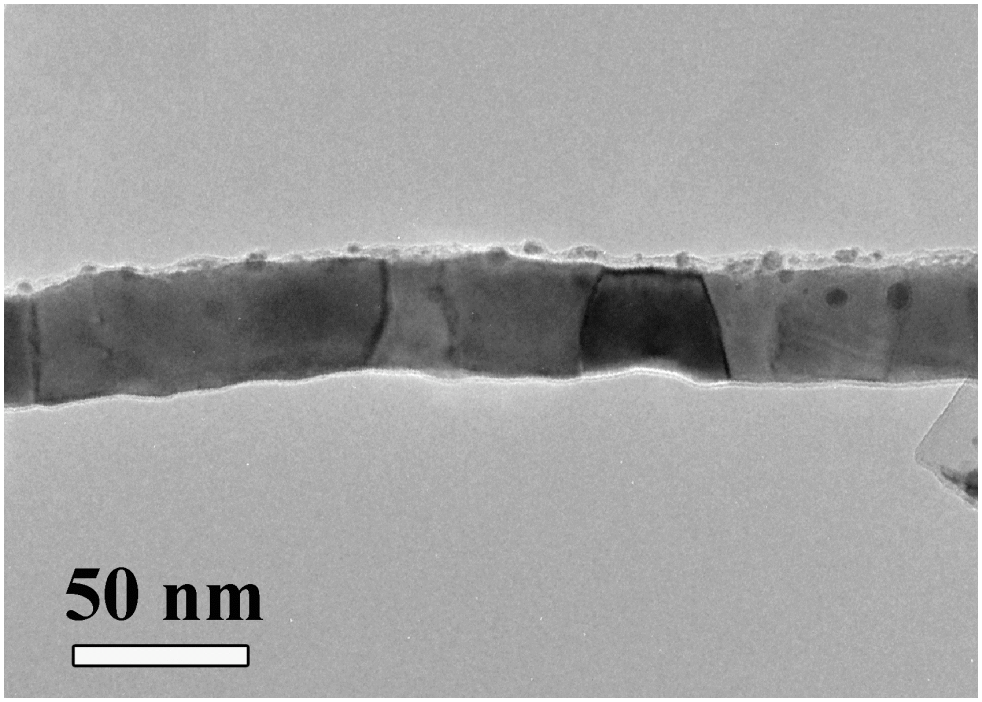

Figure 3. 20 nm Pt on a SiNW annealed at 550ºC for 30 min. The grains are identified as PtSi by electron diffraction.

Interfacial Reactions in Ni Contacts to SiNWs

Bangzhi Liu also performed initial work on the silicide formation in a new geometry, borrowing a TEM workbench approach developed for another project, to allow us to fabricate nanoscale devices on electron-transparent silicon nitride membranes and view them in the microscope. The advantage of this approach is that we are able to observe interfacial reactions in contacts in exactly the same geometry as is used for nanowire transistors or other devices. We have made detailed observations of phase transformations in annealed Ni contacts to SiNWs. Surprisingly, we have observed not one but two different sequences of phase transformations, both of which differ from that usually observed in Ni thin films on Si wafers. In one case, $NiSi_2$ is the first phase to form. In the other, the metastable θ-Ni_2Si phase forms. Phase formation is dependent on the orientation of the nanowire and is described in a *Journal of Applied Physics* article.[3]

Schottky Barrier Contacts

Sharon Woodruff (who was co-advised by Profs. Mayer and Mohney and supported by an NSF Fellowship during part of this program) fabricated and extracted effective barrier heights and ideality factors for annealed Schottky barrier contacts to n-type SiNWs in two different geometries, including that shown in Fig. 4. This figure shows an ohmic contact (Ti/Al) prepared to a heavily-doped n-type end of the nanowire, an oxide shell around the nanowire to help passivate the bare semiconductor surface, and a nickel sil-

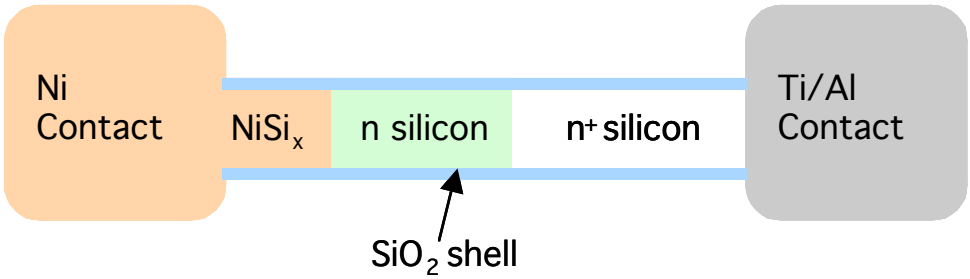

Figure 4. Schematic of the device used to test the characteristics of nickel silicide Schottky barrier contacts to n-type SiNWs. The Ti/Al metallization is used as an ohmic contact on the opposite end of the nanowire.

icide nanowire segment serving as the Schottky barrier contact to the lightly doped segment of the SiNW. The silicide was formed during annealing of the Ni contact.

Note that we used the term “effective barrier height” in describing the results of our electrical characterization. The nanowires have very small diameters (55–70 nm), and their I-V characteristics can change depending on whether testing is performed in air, N_2, or vacuum. To mitigate this effect, we applied a bias to the back of the wafer on which the test structures were fabricated. Negligible current was transported from the back of the wafer through the dielectric layer on which the nanowires rested, and the applied bias created a field effect in the nanowire and served as a “back gate”. We therefore measured I-V curves at different back gate voltages. For the annealed nickel silicide Schottky barriers to n-type SiNWs, the extracted barrier heights ranged from 0.52 eV (n = 1.18) to 0.69 eV (n = 1.09) for gate biases of 20 V and 0 V, respectively. When heavier doping was used, high ideality factors were measured (near 3.8), indicating a much greater contribution of tunneling to the current transport. This work was published in the *Journal of Vacuum Science and Technology*.[4]

Simulations

This work made it obvious that understanding the I-V curves of a Schottky barrier contact to a semiconductor nanowire requires more careful analysis than the case of a Schottky barrier contact to a wafer or epilayer. Ordinarily, we are concerned about band bending in the semiconductor in only one dimension in a Schottky barrier contact. In a nanowire, however, we must be concerned with band bending due to both the metal/semiconductor interface and the interface between the nanowire’s circumference and its surroundings. Hence, the depletion region in the semiconductor at the metal/semiconductor interface may be shaped in various ways, including those shown in Fig. 5.

Therefore, simulations of Schottky barrier contacts to semiconductor nanowires were pursued by Karthik Sarpatwari using a three-dimensional device simulator called Sentaurus (by Synopsys), and we considered semiconductor nanowires with diameters from 20–100 nm. The device modeled is a three-terminal structure (Schottky barrier, ohmic con-

tact, and gate metallization). In Fig. 4, these terminals would correspond to the nickel silicide Schottky barrier contact, Ti/Al ohmic contact, and a gate metallization all the way around the SiO_2 shell. This simulated structure (which was eventually fabricated) provides an improvement over that used in our previous experiments in that the new device is completely symmetric when it is rotated about the long axis of the nanowire.

Figure 5. Schematic diagram of the shape of the edge of the depletion region beyond the metal/semiconductor interface, with a (a) thicker or (b) thinner barrier around the nanowire circumference.

Since the surround gate system is essentially a gated diode, the carrier concentration profile in the diode depends on the applied gate bias. Under the influence of the gate, the semiconductor adjacent to the surrounding oxide can be biased into inversion, depletion or accumulation. As a result, the band bending across the nanowire cross-section is not uniform, which greatly influences the I-V curves of the Schottky barriers.

Also important are the effects of interface traps and tunneling. The main contribution of the interface traps is to smear out the gate voltage effect. A part of the gate voltage is balanced by the charge in the nanowire, and the rest is balanced by the interface trapped charge. Consequently, the voltage range for the various modes (depletion, accumulation or inversion) is expanded.

The non-uniform barrier profile at the metal/semiconductor interface can result in a very important localized tunneling contribution. The tunneling current contribution requires both the presence of carriers and an altered barrier. With the nanowire circumference in accumulation and inversion conditions, both these criteria are met, leading to significant

tunneling current contributions. With the nanowire depleted around its circumference, the electron current flow is restricted to a reduced effective area determined by the depletion region at a particular gate bias.

Current-voltage characteristics of the simulated nanowire Schottky diode are heavily influenced by the gate bias, interface traps and tunneling contributions around the periphery of the nanowire. As the gate voltage is swept from accumulation to inversion, the electron and hole contributions to the total current vary. The evolution of the simulated I-V characteristics with gate bias is shown in Figure 6. The extracted barrier height using the conventional thermionic emission theory is then plotted in Figure 7. Because of the effects of electron and hole tunneling, we obtain a gate bias-dependent barrier height profile. The primary effect of tunneling is a reduction of the extracted barrier height in the near-depletion and accumulation modes. The change in barrier height with gate voltage ($d\Phi_B/dV_g$) can also be tracked as a function of the applied gate bias. Figure 7 also shows the dependence of $d\Phi_B/dV_g$ vs. V_g. The extracted barrier height at the gate voltage corresponding to the peak of $d\Phi_B/dV_g$ matches the input barrier height value. This simulation therefore points to how to collect and interpret data in Schottky barrier test structures with surround gates, which we have fabricated.

To compare with the simulations, Nick Dellas fabricated surround gate (SG)-NW Schottky diodes (Figure 4a) during the final semester of the program. The Schottky contact is a metal silicide formed by rapid thermal annealing of the deposited contact metal. The θ-Ni_2Si/n-Si NW Schottky diodes were tested at room temperature in a N_2 environment using an Agilent 4156B Precision Semiconductor Parameter Analyzer. With increasing gate bias, the ideality factor increases and apparent barrier height decreases. In the case of the simulations, extrapolation of the effective barrier height plotted against the ideality factor to n = 1 yields the actual barrier height, neglecting image force lowering (Figure 8). Using the same approach, in the case of the experimental θ-Ni_2Si/n-Si NW Schottky diode, a barrier height of 557 meV is obtained by extrapolation to n = 1, where image force lowering is expected to be small for the lightly doped nanowires. This work has recently been submitted to *Solid-State Electronics*.

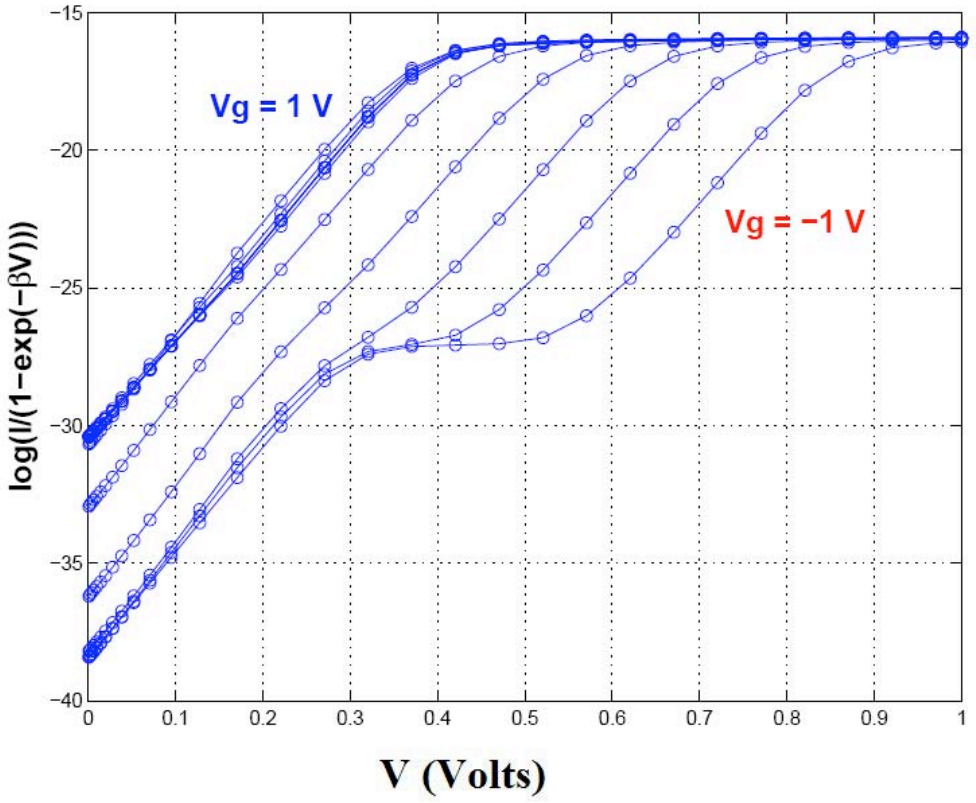

Figure 6. I-V characteristics plotted for different values of gate bias (V_g). As is often done for Schottky barrier contacts, we have plotted the logarithm of the current divided by $(1 - e^{-qV/kT})$.

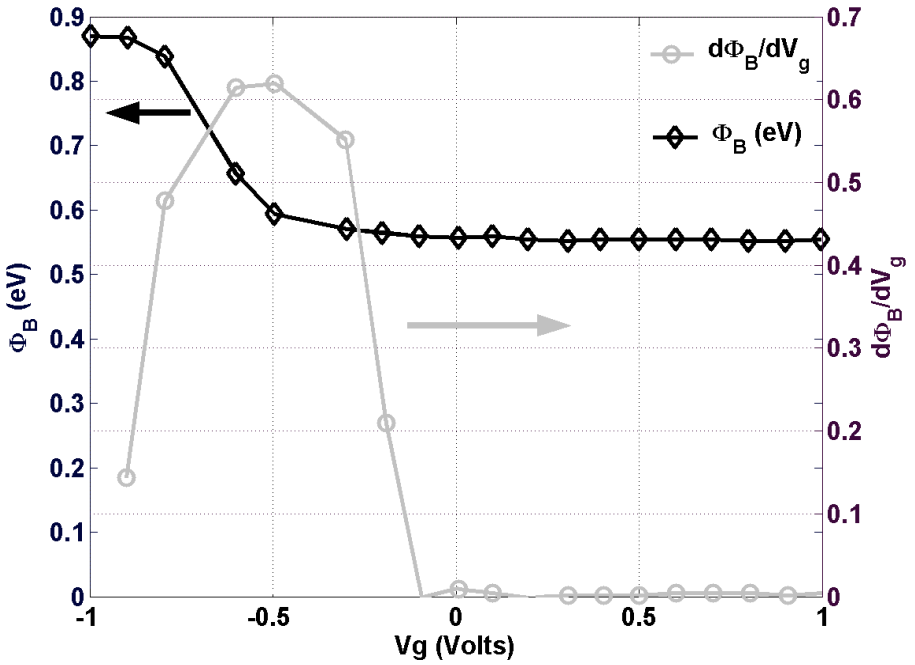

Figure 7. Extracted barrier height evolution with gate voltage. In these simulations for 25 nm diameter SiNWs, a Schottky barrier height of 0.6 eV was input. The simulated I-V curves, analyzed by the conventional approach used for Schottky barriers, indicated a barrier height of 0.6 eV only when $d\Phi_B/dV_g$ was a maximum.

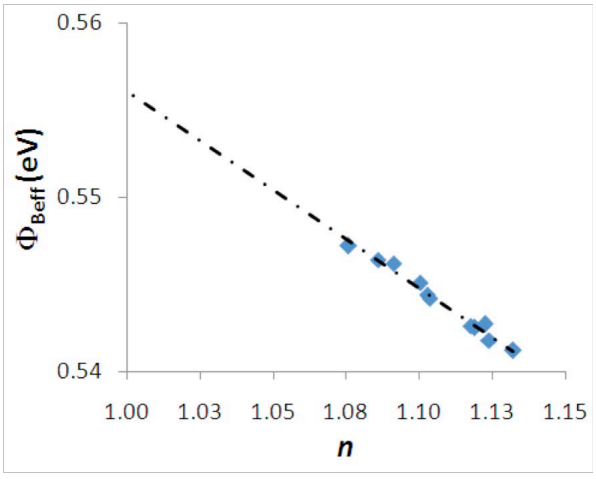

Figure 8. Extracted effective Schottky barrier heights and ideality factors obtained for different SG biases and extrapolated to an ideality factor of 1.

Ohmic Contacts

Sharon Woodruff tested two basic geometries for ohmic contacts. Both required an electrofluidic alignment of nanowires onto sacrificial silver pads patterned by photolithography on a silicon nitride film on a silicon wafer. The sacrificial pads were etched away once the nanowires were positioned. Top contacts were next patterned using photolithography and/or electron-beam lithography, metals were deposited by electron-beam evaporation, and lift-off was performed. A single-nanowire multi-terminal test structure with Ti/Al contacts to a GaN nanowire is shown in Fig. 9. For the second type of test structure, many nanowires were aligned in parallel between a pair of contacts, as shown in Fig. 10. Parallel-nanowire test structures have some useful advantages. They transport higher currents, which are easier to measure. Arrays of nanowires may even present a practical configuration for chemical and biological sensors. Because many nanowires are measured simultaneously, nanowire-to-nanowire variations also tend to be averaged out, making it easier to spot trends more quickly than when many single-nanowire devices are fabricated and measured. However, this averaging could mask some of the interesting characteristics of individual nanowires and the contacts to them.

The parallel-nanowire test structures were used primarily to help us identify conditions for forming ohmic contacts to the GaN and Si nanowires. For the GaN nanowires, 45 nm of Ti was deposited directly on the GaN, followed by 205 nm of Al. They became ohmic when annealed at either 550 or 600 °C for 2 min. Back-gating of the test structures revealed n-type conductivity in the unintentionally doped GaN nanowires. Taking our cue from past work at Penn State on contacts to n-GaN, we were next able to lower the optimal annealing temperature to 500 °C by reducing the Ti layer thickness and forming Ti/Al 35 nm/215 nm contacts. Though this lower Ti:Al ratio could result in reduced thermal stability of the contacts, our studies do not require great thermal stability. This work was presented in a poster at The Electrochemical Society meeting in October 2006.

Ohmic contacts are most readily formed to heavily doped nanowires, and this was also explored for Si nanowires. Using the parallel-nanowire test structures, we formed ohmic

contacts to n+ Si nanowires using Ti/Al (100/100 nm), as shown in Fig. 11. For p+ Si, we formed ohmic contacts using Pt, which has a high work function. We were especially interested in forming platinum silicide for these contacts, since platinum silicide has a very low barrier height to p-type Si. Annealing at 450°C reduces the resistance of Pt/Si contacts to p+ Si nanowires, as shown in Fig. 12, and corresponds to conditions for significant platinum silicide formation as long as the annealing environment is sufficiently free of oxygen.

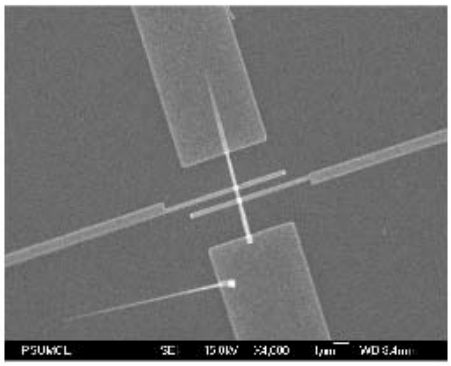

Figure 9. Single-nanowire test structure.

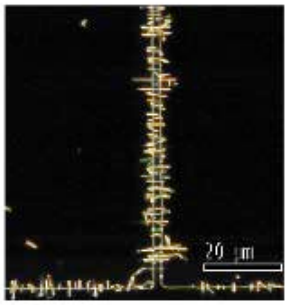

Figure 10. Parallel-nanowire test structure.

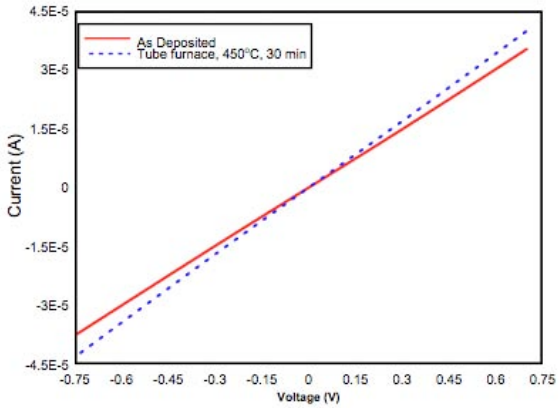

Figure 11. Ti/Al contacts on n+ Si nanowires as-deposited and annealed.

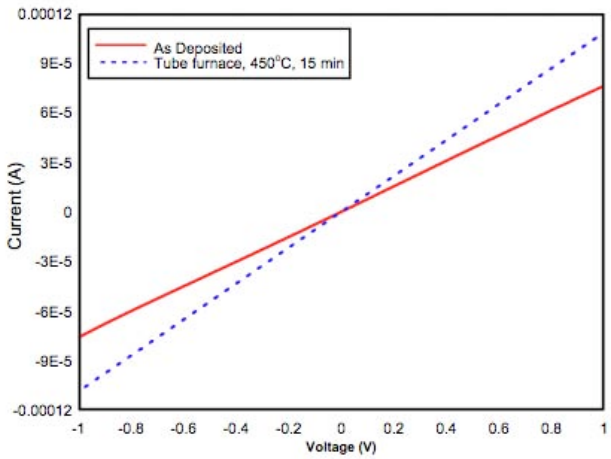

Figure 12. Pt/Si contacts to p+ Si nanowires as-deposited and annealed.

Additional Activity

Prof. Mohney also collaborated with Prof. Redwing and her student on the measurement of the resistivity of arrays of Si nanowires grown in aluminum oxide membranes. The bottom ohmic contacts were made to short, heavily-doped Si segments through the reaction of Co with the silicon nanowires during growth. Top ohmic contacts to n-type and p-type nanowires were deposited and annealed in our laboratory using Al for p-type Si nanowires and Ti/Pt/Au for n-type nanowires. Using an approach reminiscent of common ohmic contact test structures, arrays of nanowires of different lengths were sandwiched between top and bottom contacts to allow the contributions to the total resistance from the semiconductor nanowires and contacts to be separated. For all but the most lightly doped nanowires, linear I-V curves were measured after annealing at 250-300 °C, and the resistance of the contacts was small compared to that of the very long Si nanowires, which had resistivities from 0.034–0.22 Ohm-cm. This work was presented at Optics East (SPIE) and MRS and reported in a SPIE proceedings volume.

Dr. Bangzhi Liu performed transmission electron microscopy of gold that was selectively plated on n-type segments of Si nanowires with p-n junctions for junction delineation and nanofabrication. This work appeared in *Nano Letters*.[5] He also assisted with the characterization of top-gated nanowire field effect transistors, and this work was published in 2008 in the *Journal of Vacuum Science and Technology*.[6]

Karthik Sarpatwari, who received partial support and conducted the modeling of the surround-gate Schottky barriers, also performed measurements on other Schottky barrier test structures, resulting in one publication on Schottky barrier contacts to ZnO.[7]

Yaw Owusu-Boamah, an undergraduate minority student, was a summer intern at Penn State in 2008 and received a stipend through the NSF National Nanotechnology Infrastructure Network. This opportunity for undergraduates provides research experiences in the field of nanofabrication, and students generally affiliate with an ongoing research project at Penn State. Mr. Owusu-Boamah worked closely with the graduate student on our ARO project, Mr. Karthik Sarpatwari, to prepare inhomogeneous Schottky barriers and collect experimental data to feed into our ongoing simulation efforts.

An undergraduate student from the University of Puerto Rico Cayey, Gloriell M. Cardona, conducted research on electrical contacts to nanocomposites of inorganic semiconductor nanocrystals and organic semiconductors in the summer of 2007. Her stipend was provided by a program at her university, but her laboratory expenses were provided by this research project. In collaboration with Prof. Jian Xu, this opportunity allowed us to begin investigating the closely-related problem of current transport in electrical contacts to nanoscale composites that have the potential for photovoltaics and light emitting devices.

Summary of the Most Important Results

Contacts to semiconductor nanowires share similarities with their thin-film counterparts, but they also exhibit some important differences due to geometry. For example, in the formation of platinum silicide contacts to Si nanowires, it is possible to achieve uniform platinum silicide/silicon nanowire contacts, but some annealing conditions and Pt:Si ratios can also lead to a peculiar kinking of the nanowires not analogous to the thin-film case. Also interesting is the effect of geometry on Schottky barriers to semiconductor nanowires, as studied using both experiments and simulations. Control of the semiconductor nanowire surface adjacent to an axial metal/semiconductor nanowire contact is

necessary for accurate extraction of the Schottky barrier height and can be achieved with a wrap-around gate. In this work, conditions were also identified to form ohmic contacts to n-GaN, n-Si, and p-Si nanowires. Ti/Al contacts were used for the n-type nanowires and Pt contacts for the p-Si nanowires.

Bibliography

[1] K.-K. Lew and J. M. Redwing, J. Cryst. Growth 254 (2003) 14.

[2] Bangzhi Liu, Yanfeng Wang, Sarah Dilts, Theresa S. Mayer and Suzanne E. Mohney, Nano Lett. 7 (2007) 818.

[3] N. S. Dellas, B. Z. Liu, S. M. Eichfeld, C. M. Eichfeld, T. S. Mayer, and S. E. Mohney, J. Appl. Phys. 105 (2009) 094309.

[4] S. M. Woodruff, N. S. Dellas, B. Z. Liu, S. M. Eichfeld, T. S. Mayer, J. M. Redwing, and S. E. Mohney, J. Vac. Sci. Technol. B 26 (2008) 1592.

[5] Chad M. Eichfeld, Carolyn Wood, Bangzhi Liu, Sarah M. Eichfeld, Joan M. Redwing, and Suzanne E. Mohney, Nano Lett. 7 (2007) 2642.

[6] Bangzhi Liu, Yanfeng Wang, Tsung-ta Ho, Kok-Keong Lew, Sarah M. Eichfeld, Joan M. Redwing, Theresa S. Mayer, and Suzanne E. Mohney, J. Vac. Sci. Technol. A 26 (2008) 370.

[7] K. Sarpatwari, O. O. Awadelkarim, M. W. Allen, S. M. Durbin, and S. E. Mohney, Appl. Phys. Lett. 94 (2009) 242110.