Silicon Photonics: Challenges and Future

An OIDA Forum Report

Prepared by

Dr. W. S. Ring
WSR Optical Device Solutions LLC

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Optoelectronics Industry Development Association
1133 Connecticut Avenue, NW - Suite 600
Washington, DC 20036
Tel: 202-785-4426; Fax: 202-785-4428
URL: http://www.oida.org

Report Documentation Page

Form Approved
OMB No. 0704-0188

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1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
2007		**00-00-2007 to 00-00-2007**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Silicon Photonics: Challenges and Future	**W911NF-06-1-0004**
	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Optoelectronics Industry Development Association (OIDA),1220 Connecticut Avenue, NW, Washington,DC,20036**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) **US Army RDECOM ACQ Ctr -W911NF, 4300 Miami Blvd, Durham, NC, 27703**	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES
See also ADM002197.

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**Same as Report (SAR)**	**91**	

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1 Introduction

Today's electronic society is seeing increased demand for data transfer, internet downloads, online applications, video sharing, and storage. Banks, companies, universities, and governments require large secure data centers connected to secure networks. This continuously drives the development of more powerful servers and computer systems. Today's data centers are not single computer systems but networked systems with distributed processing, computational power, and memory. The systems are connected by 'nodes,' which connect the components of the 'computer.' The configuration depends on the applications, functionality, and user requirements. This demanding environment is evolving and pushing for the development of higher speed interconnects.

Copper interconnects are currently used extensively within the data center environment. Fiber optic technology is used as a connectivity solution when higher performance is required and the cost differential compared to a copper solution is affordable. Fiber optic technology offers several key advantages over copper solutions for data transmission. Within today's data center, there is ubiquitous use of multi-mode fiber and optical transceivers for rack to rack connections. The fiber ports provide dedicated links, with reach up to 300 meters on multi-mode fiber and 2 km on single mode fiber. The fiber connections allow networks to connect to the wide area or local area networks (WAN or LAN). As improvements have occurred in fiber optic transceiver performance and cost has been reduced, there has been further proliferation of fiber optics within the data center.

Traditionally, there has been a debate on the distance-cost crossover from a copper to an optic solution. III-V photonics offers a solution, but in recent years there has been a drive to integrate silicon technology with III-V technology. Within the communications field, the integration of silicon and III-V devices has been a goal for the last 20 years. Initial development centered on silicon optical bench technology as a route to lower cost, passive optical alignment, and integration. Several major computer and connector companies invested heavily in this area during the late 1980s and early 1990s. AMP Incorporated purchased the GTE patent portfolio, specifically to develop optical components based on silicon microbench technology. Lucent Technologies, under the Laser 2000 program, developed optical sub-assembly technology for low-cost active alignment and high-speed RF transmission. Lucent was also the developer of optical micro electro-mechanical systems (MEMS) devices for all optical switching. The MEMS' mirror technology has been implemented in high definition projection televisions (DLP) by Texas Instruments. The integration of silicon and III-V has generated tremendous numbers of patents and publications.

The III-V community has tried to develop optical electronic integrated circuits (OEIC) with increased functionality, but no significant application driver has prevailed. The integration of different functions on a single chip has been demonstrated. Several products are manufactured today, including tunable lasers, which take advantage of the functional integration technology. Integrated circuit (IC) packaging offers the chance to

develop optical input/output (I/O) for electronic chip sets and provide a new volume market for optical communications devices. The integration of silicon and III-V technology offers a potential solution to the I/O bottleneck that has been predicted for IC technology.

Several companies and non-profit organizations within the silicon semiconductor industry have highlighted the technology issues facing copper interconnects for inter-chip, intra-chip, and board-to-board communications. OIDA held a workshop in November 2004 to discuss several of these aspects. Because of the emphasis on silicon photonics today as a potential optical interconnect solution, OIDA held a silicon photonics forum, in conjunction with an interconnect forum, to understand the issues and technology paths being pursued. This report reviews aspects of this subject, provides a synopsis of the information from the meeting, and offers some conclusions.

2 Industry status

The computer industry and communications industry are linked today because of the Internet. The ubiquitous use of data and the transport of that data between servers, data centers, and access points requires fast uninterrupted connections. Today's computers are complex systems based upon several technologies. The connection between the memory and the central processing unit (CPU) is not necessarily on the same board or in the same packaged IC chip. The data center is a distributed computer system with multiple nodes that have to be connected. These nodes sit at different levels, whether they are on the chip, in the server, in the rack, or at an alternative location. How these connections are made is highly dependent on the architecture.

The optical communications industry developed from the need for people to communicate. The telecommunications industry has been the driver for implementation of optical technology, which offers several advantages over copper wireline communications. As the computer industry moved to higher clock frequencies, smaller process nodes, and multiple core architectures, fundamental signaling issues drove the need to look at optics as an alternative.

Copper media, multi-mode fiber, and single mode fiber are used in today's data center to transport information between racks. The current architecture of the servers and data centers is based on copper interconnect technology. As the speed requirement between the different nodes increases, new approaches to the problem need to be discussed. Copper interconnect technology continues to evolve and improve as the industry moves forward. The crossover point between optics and copper solutions has been debated and price and performance are regarded as key metrics. Signal integrity and thermal performance are additional metrics that cannot be ignored.

The computer industry has several organizations that look at the future bottlenecks that can impact the industry. For the semiconductor chip makers, the International Technology Roadmap for Semiconductors (ITRS) has developed several roadmaps and highlighted areas of concern. Interconnects is a key area. ITRS has highlighted a "red brick wall" that is looming for the integrated circuit chip makers. Optical technology offers a solution, but the implementation and architecture to overcome the red brick wall are not understood. Relative to the traditional semiconductor industry, the optical component industry is immature. How to address this is unclear.

Today, optical component companies serving the communications segment are providing solutions for server I/O connections. For short reach links, vertical cavity surface-emitting laser (VCSEL) technology is primarily used. The parallel VCSEL array transmitter and receiver (transceiver) is in production for server rack connections. Several government and industry initiatives have been investigating VCSELs for interboard connections. The alternative approach currently receiving attention is "silicon photonics," i.e., the integration of silicon IC technology and III-V light emitters. Silicon photonics is not a new concept. It has been investigated for more than 15 years and is utilized today in communications network equipment. The production of a group IV light emitting struc-

ture has not yet been realized. Currently, hybrid technology is believed to be the best route forward.

As we move to the inter-chip and intra-chip connection, the issues become more complex. Circuit board manufacturing and the reliance on FR-4 are hindrances to new technology implementation and providing economies of scale for higher performance materials. The optical technology for circuit boards is developing along the path that provides waveguides imbedded in the circuit board. The removal of high speed electrical signaling traces needs to be complemented by changes in the I/O architecture of the IC signaling pins and circuit card connectors. It is believed by several companies that silicon photonics provides a distinct advantage in this area. By developing optical solutions that are complementary metal-oxide semiconductor (CMOS)-compatible, wafer scale integration can potentially enable optical I/O pins on the IC package. The alternative is to pursue the co-packaging of OE modules within the IC package using more standard III-V devices. The industrial roadmap, cost/performance, economy, and scale of the silicon industry vs. the communications industry needs to be considered when reviewing this issue.

The argument for a wafer scale solution is not new. Silicon optical bench technology is used today in several optical communications applications. The development and implementation has required intensive research and large amounts of investment to enable the current technology. The term “wafer scale’” needs to be handled with caution. Several economic factors need to be considered when discussing the integration platforms and direction of the industry segments. There are economic issues that have impacted the traditional optical transport business and the current optical components industry. This has lead to a downturn in research and investment in optical component technology in the United States. Globally, investment in optics is continuing. In Europe, the 7th Framework program has established optical technology as a key focus area. Both in Europe and in Japan, investment in optics is now addressing broader market segments and applications. As Japan continues to implement its fiber-to-the-home (FTTH) program and broadband requirements, data center transport and signaling are being addressed.

There are a limited number of U.S. companies researching silicon photonics for product implementation. Traditional optical communications component companies are focusing on next generation component development for their traditional markets, i.e., Ethernet, Fibre Channel, and InfiniBand. The copper interconnect companies continue to drive for higher backplane interconnects and copper cables. Today, the Defense Advanced Research Projects Agency (DARPA) is sponsoring programs on silicon photonics. The motivation is driven by the need to address computer interconnects for inter-chip and intra-chip applications.

3 Background

The computer industry and the optical communications industry have different requirements. The market is segmented into low cost, high volume PC/laptop sales, low-end servers, mid-range servers, and high-end servers. Each segment has different pricing and economic requirements. In looking at the interconnect market we need to review several of the drivers.

3.1 Server market

The server/computer market is a multibillion dollar entity. The data centers utilize servers, data storage, and communication networks. The total server market is dominated by a few well known players. These companies utilize proprietary and/or standard protocols, develop their own chipsets, or partner with major chip manufacturers. The inside of the chassis is not interchangeable. The total estimated market for servers is around $56 billion. This estimate includes cabling, processors, etc. The major players involved are IBM, Sun, Hewlett-Packard, Dell, and Fujitsu. Figure 1 shows the estimated share reported by International Data Corporation's (IDC) independent server market tracker.

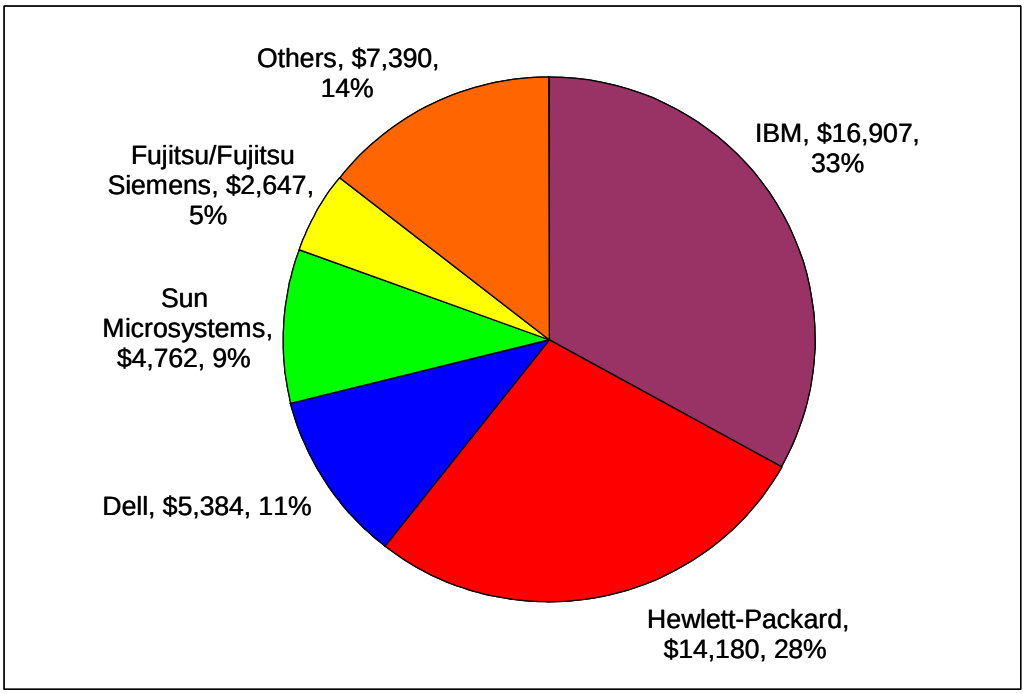

Figure 1: Worldwide server revenue and market share for 2005 (US$M)

(Source: IDC Quarterly server tracker)

The software which runs on the servers is broken down into three principal operating systems: Microsoft Server, Linux, and UNIX. The market is currently deploying 64-bit processor systems with multi-core designs. The industry has moved to multi-core designs rather than continuing clock frequency increases due to thermal and power management

issues. According to this tracker, blade shipments accounted for around 4.6% of the total market revenue in 2005. The blade architecture was reported as growing in popularity. Fiber optic cabling is utilized in the 'high end' servers. The main ongoing concerns for this market include power consumption and thermal management. The current I/O ports for the servers run at varying signaling rates. These range from 33 MHz (PCI^2) to more than 2 Gb/s (PCI Express), with multi-drop busing used at the lower speeds and point to point links at the higher speeds.

3.2 Silicon industry technology drivers

The silicon industry is around a $200 billion market. The major microprocessor and memory manufacturers employ state-of-the-art fabrication facilities. These large fabrication facilities are fully automated and can manufacture devices on 300 mm diameter wafers. The fabrication facility requirements depend on the market segment being served. The dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), and microprocessor segments are driven by constant reduction of device feature size to enable better performance and reduce costs. Figure 2 highlights this driver in linewidth reduction and processing node.

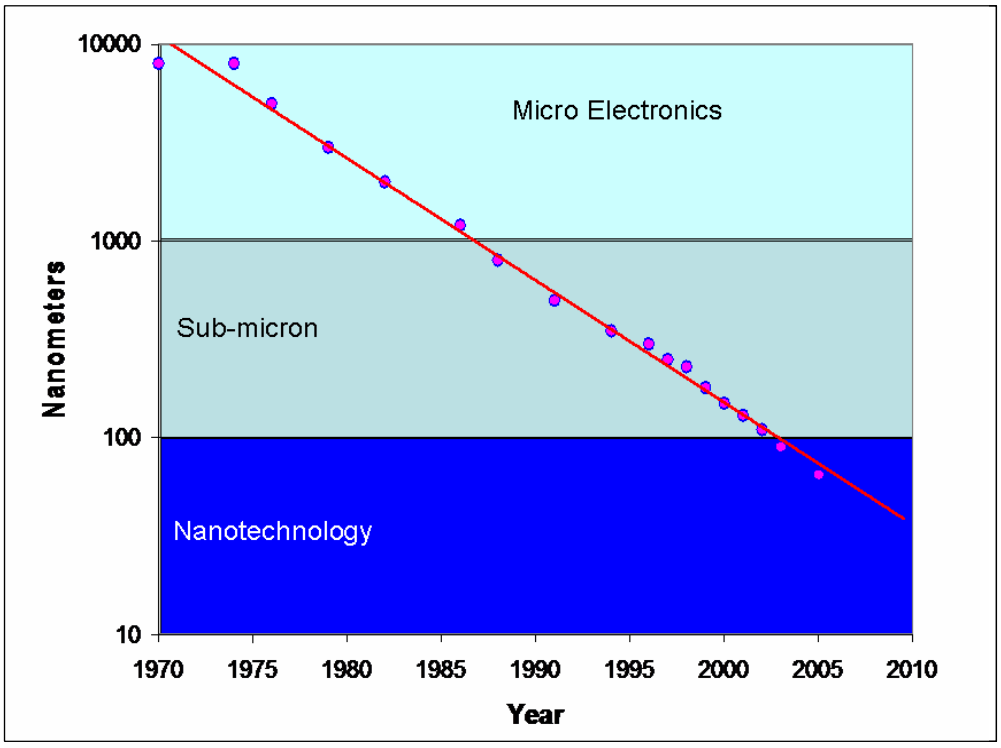

Figure 2: Production line widths in silicon (extended to 2010)

The push in the microprocessor industry for smaller and smaller features has driven it to develop more precisely-controlled fabrication processes and implement different materi-

als, i.e., low-k dielectrics and copper conductors. The push for smaller feature size and larger wafers has made a dramatic impact on the fabrication facility investment cost. To remain competitive, many companies transition to larger wafer size. Figure 3 highlights the transition trend for wafer size production.

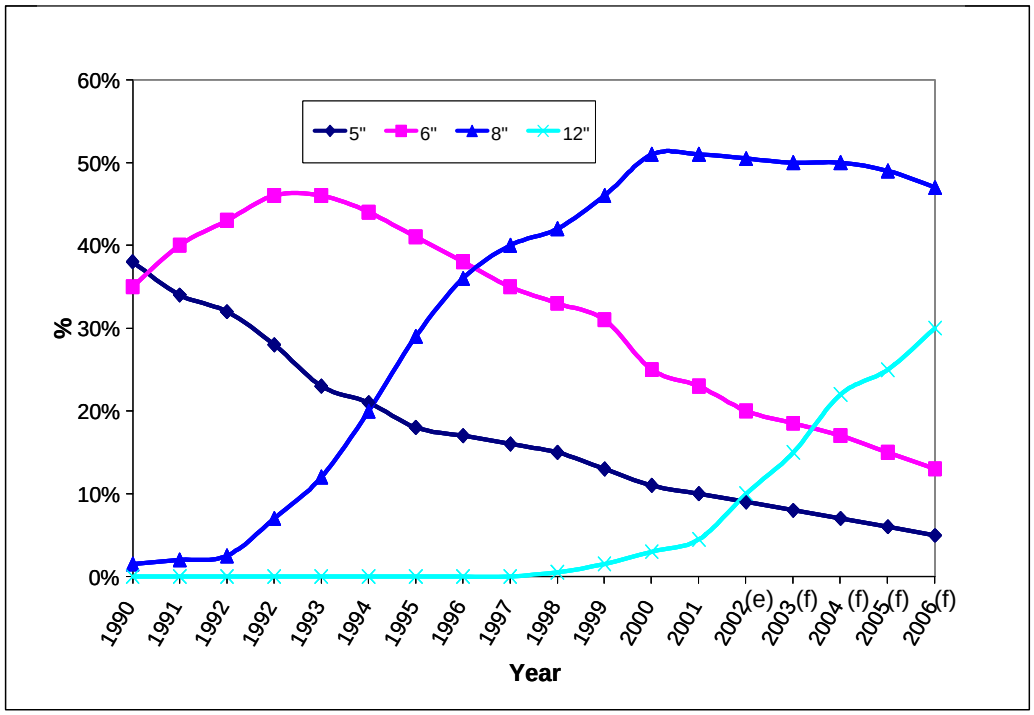

Figure 3: Wafer size fabrication facility trend

(Source: IC Insights)

The constant process node trend and wafer size change increases the investment cost for a semiconductor fabrication facility. Figure 4 highlights the increased cost in facility investment as the feature size has decreased.

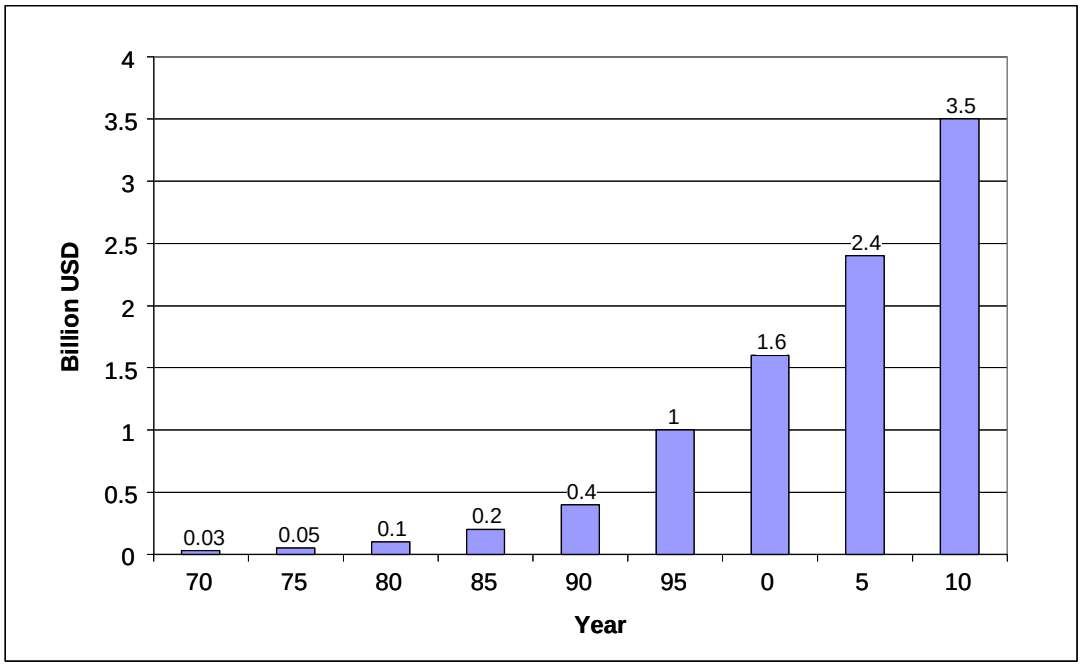

Figure 4: Wafer facility cost trend

(Source: IC Insights)

The estimated cost of building a state-of-the-art 300 mm wafer facility is now close to $3 billion. The primary manufacturer of microprocessors is Intel. It is the largest pure play silicon fabrication company and leads in investment in semiconductor technology.

The silicon industry has developed standard processes and design tool sets. The wafer foundry model used by several companies today was developed from a U.S. government-sponsored program, Metal Oxide Semiconductor Implementation Service (MOSIS). The standard design sets and process tools enabled the silicon foundry model. There are several electronic silicon foundries, such as TSMC, Charted Semiconductor, and United Microelectronics. These companies offer standard processes and tool sets at different process nodes. Typically, they are one generation behind the latest node being implemented by the vertically integrated player Intel.

For companies with revenue streams of around $200 million or less annually, a fabless model makes tremendous sense and is preferred. It reduces the investment cost for these companies and allows them to develop new design and chip sets on essentially a shared cost line.

3.3 Silicon photonics drivers

One of the key drivers for silicon photonics is the issue of bandwidth. Electrical signal integrity and impairments become more important as the data rate between nodes increases. Optics offers higher bandwidth solutions with fewer signal integrity problems compared to equivalent electrical cabling. The current bandwidth in multi-core proces-

sors is expected to increase exponentially as we move to more parallelism within the processor design. This drives increasing bandwidth requirements and hence data rate transmission between nodes. The scale of the bandwidth in the processor architecture is highlighted in Figure 5.

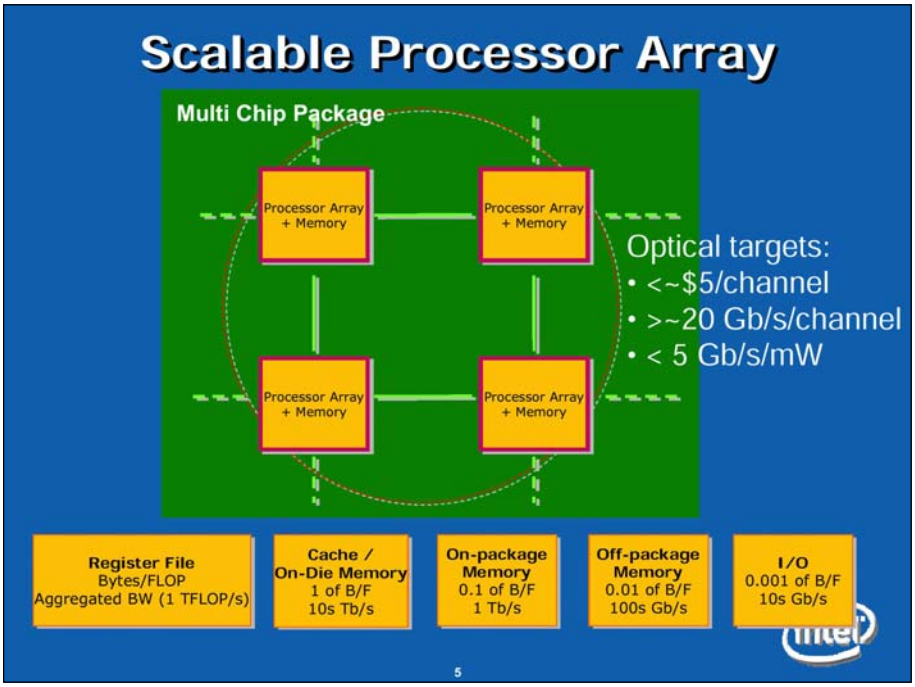

Figure 5: Scaleable processor array and the bandwidth requirements at each node
(Courtesy of M. Morse, Intel)

The principle of silicon photonics is not new. The communications industry has been developing solutions based on silicon as a platform for the last 20 years. As the microprocessor and computer industries have developed and with the ever-increasing bandwidth requirements, fundamental signaling limits of the copper traces are being questioned. The principle is very simple: can we use optical instead of electrical signaling for routing within the computer architecture? This basic question has many different answers depending on one's point of view. The implementation of optical signaling instead of copper signaling fundamentally depends on the technological advantages and the cost. The computer industry continues to develop new and novel approaches to extend the useful life of copper interconnects.

The basic problem with silicon photonics is light emission: silicon is an indirect band gap material and therefore does not emit light. III-V semiconductors are the current mainstay of optical technology and can be found in many aspects of our daily life. The cost of optics is volume-dependent. Compact disc (CD) and digital versatile disc (DVD) lasers are considerably cheaper than telecom lasers, but the volume is orders of magnitude larger. For the computer industry, optical interconnect technology will need to use a

hybrid solution for the generation of light unless emission using silicon can be realized by electronic and material engineering.

With the computer market being very cost and high-volume sensitive, a different philosophy is required from the traditional communication optical component manufacturers entering the silicon photonics arena. The differences in operating temperature of the optics chips and the reliability performance metric all need to be redefined or adapted. The computer industry cannot force price demands on optical companies. The technology evolution and implementation will require partnerships to be forged to provide a path that is sustainable.

Silicon photonics based on integrating computer-aided designs (CAD) with die bonded lasers is the starting point for silicon photonic devices. This is a hybrid approach that uses traditional component manufacturing. The disadvantage for silicon vendors is the optical devices are not integrated into the wafer fabrication process. Instead they are part of the assembly process. A semiconductor approach is required to change this methodology, hence the current idea of using wafer bonded devices, rare earths, epitaxial growth, or nanocrystals.

Application development can help drive some of the silicon photonics interconnect technology. Several companies are looking at smart cable assemblies or inter-board interconnects. These applications are faced with either developing new technology dominated by low cost cabling or III-V optical solutions. Figure 6 highlights some of the initial concepts for silicon photonics.

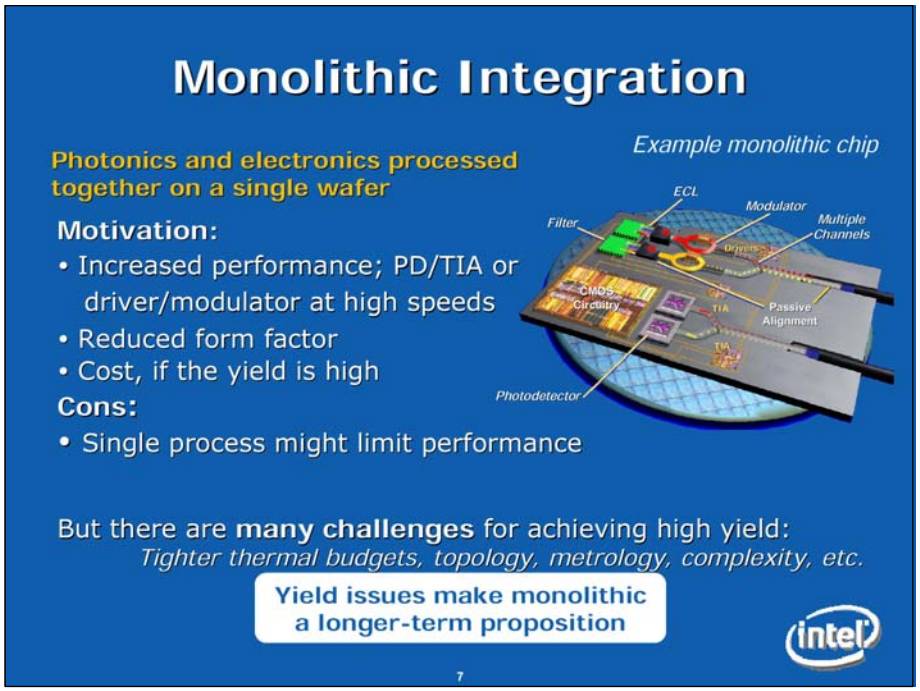

Figure 6: Example of monolithic integration of optical devices on a silicon motherboard
(Courtesy of M. Morse, Intel)

Using silicon as a platform for integration and increased functionality is the best way to move into the optical application space. This approach competes directly with III-V optical photonics integration currently being developed in research laboratories. The potential advantage of silicon photonics is a function of the industry drivers. The application space of the computer and communications industries combined offer real potential for growth. The inertia of the traditional computer architecture will need to be addressed to enable optical implementation. If the drive comes from within the computer industry, there is a significant chance of success.

3.4 Silicon industry companies

The major semiconductor manufacturers utilize in-house fabrication, foundries, or a combination of both. The major companies in this field are outlined in Table 1. The table also highlights the major foundry suppliers. This list is based on 2005 revenue streams. The major semiconductor manufacturer is Intel, the principal CPU manufacturer.

Semiconductor Companies					
Company	**Location**	**Revenue 2005**	**OI**	**Outsource**	**Notes**
Intel Corporation	United States	$ 38,826.00	$ 8,664.00	No	
Texas Instruments Incorporated	United States	$ 13,392.00	$ 2,324.00	No	
AMD	United States	$ 5,847.60	$ 165.50		
Freescale Semiconductor	United States	$ 5,843.00	$ 563.00	Yes	
Infineon Technologies AG	Europe	$ 10,060.30	$ (340.00)	No	2006 income
STMicroElectronics	Europe	$ 8,882.00	$ 266.00	Yes	
Philips Semiconductors	Europe	$ 7,452.90		Yes	
NEC Electronics Corporation	Japan	$ 6,583.10	$ 149.10	No	
Matsushita	Japan	-			
		-			
Silicon Semiconductor Foundries					
Company	**Location**	**Revenue 2005**		**Outsource**	
TSMC	Taiwan	$ 8,103.60	$ 2,292.70		
United Microelectronics Corporation	Taiwan	$ 3,058.40	$ (477.70)		
Chartered Semiconductor	Singapore	$ 1,032.70	$ (159.60)		

Table 1: Top silicon semiconductor companies by revenue

The semiconductor industry is cyclic in nature. The industry is driven by consumer demand, new product development, and technology introductions. The optical interconnect requirements today are being driven primarily by companies that are producing microprocessors and memory chip sets.

3.5 Communications industry overview

The communications industry has evolved over the last 30 years as a result of significant changes in government regulations and global requirements. The initial development of communications networks was monopolized by the telecom operators. In the United States, this was AT&T, in the UK it was British Telecom, and in Japan, NTT.

During the early 1980s politics had a major impact on the telecommunications industry in the U.S. and abroad. In 1984, the U.S. government decided to stimulate competition in the telephone sector. AT&T was broken up and 22 local Bell companies were formed into seven independent regional Bell operating companies (RBOC) often called the "Baby Bells."

In the 1990s, several significant events led to over-investment in the industry which resulted in the telecommunications "bubble." The investment drivers in the communication networks came from the Internet and wireless telephone adoption. The lighting up of the dark fiber and resultant introduction of dense wavelength division multiplexing (D-WDM) were major changes that occurred with the wireline fiber optic network. During the 1990s, most of the major equipment vendors spun out their optical component groups. This changed the business and research investment model for the industry in the United States and Europe. In Japan, the vertical nature remained through close links between the major component suppliers and the system houses.

With the advent of the Internet, communication networks changed. The traditional telecom networks were based on voice traffic, with billing on a per minute basis. As the Internet expanded and proliferated, they became dominated by data traffic. This has filled the major network pipes today. Looking forward, the telecom carriers are now entering the video market and offer voice, video, and internet services (triple play services). This has led recently to resurgence in demand for new network components. It is expected that video services will dominate fiber optic network traffic in the future. As high definition television (HD-TV) proliferates and on-demand video services are offered to consumers, more bandwidth will be consumed. New video download and sharing services, such as You Tube, are also filling the pipes. These new services are expected to impact the data center. For video-on-demand service, one potential solution to alleviate metro traffic buildup is local video caching; it has been shown that it is cheaper to store data than to transmit data.

Today, most family members have a cell phone. Figure 7 shows the adoption rate of wireless phones in the U.S. Cell phone operators such as Verizon, Cingular, Sprint, and T-Mobile have each built large cell networks and are now beginning to offer wireless fidelity (Wi-Fi) broadband access to the consumer and business user. This new service provides a roaming internet protocol (IP) network with constant connectivity.

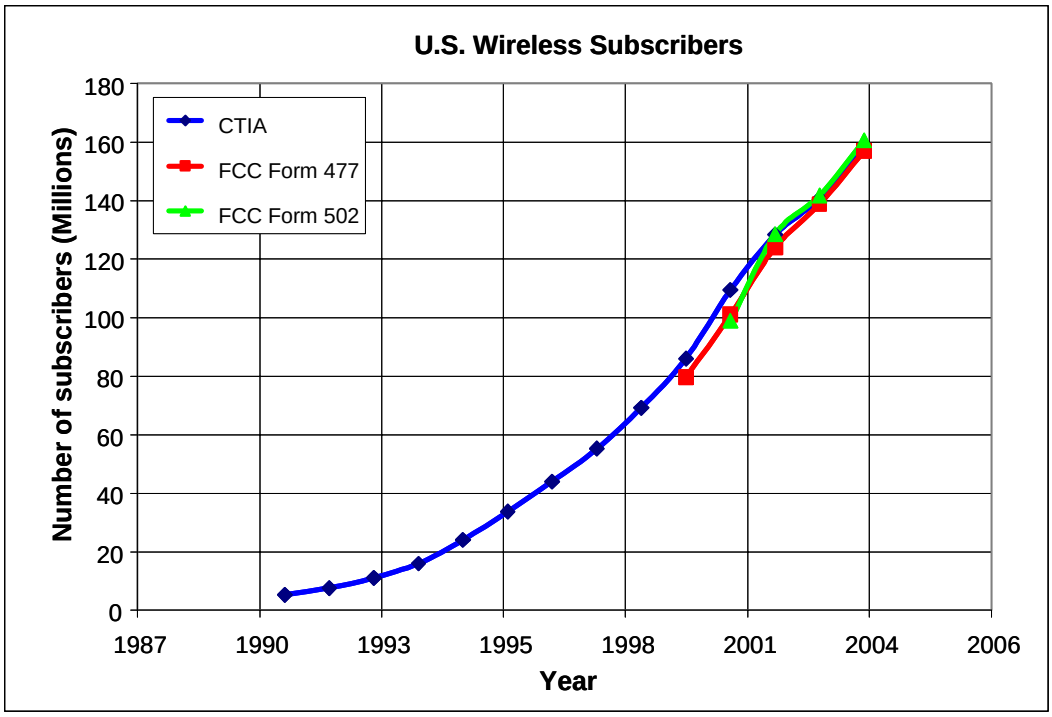

Figure 7: U.S. adoption of wireless handsets from 1990 to 2004

(Source: FCC)

With the breakup of the large vertical telecom companies, a horizontal optical component business model now exists in the United States. The current data center requirements and data transport services have changed the network structure. Due to its lower inherent cost structure, Ethernet has a started to become the network protocol of choice even for the telecom carriers.

Since the "telecommunications bubble," there has been a switch in revenue leadership among storage, LAN, and telecom. Storage laser sales outstrip telecom laser sales today. This is understandable due to the proliferation of optical storage media and optical video players. The optical storage market for CD, DVD, high definition DVD (HD-DVD), and Blu-ray™ has different drivers than the optical communications market. The optical storage market is served by several chip manufacturers that provide both communications and storage devices. The storage market has a different set of requirements to enable read, write, and erase functions on the optical disc. The next generation optical storage medium is the Blu-ray or HD-DVD disc. The optical heads now utilize three laser components based on the requirement for backward compatibility. The shortest wavelength used is 405 nm, which utilizes InGaN material to produce the source.

Conversely, the focus for optical communications companies remains developing faster and/or high power devices. The wavelengths of interest are centered on the transmission windows of the optical fiber, i.e., 850 nm, 1300 nm, and 1550 nm. These companies are also engaged in developing faster I/O optical devices for servers and data centers, but remain cautious of the cost requirements for server links.

3.5.1 Optical components companies

Several companies serve both the communications and storage markets. The companies that are principally manufacturing devices for communications networks and I/O ports sell into the following application segments:

- Ethernet
- Fibre Channel
- SONET/OTN
- InfiniBand
- proprietary

The current optical components vendors have seen tremendous price erosion in their respective markets. With lower selling prices and high manufacturing costs, most companies have suffered significant losses since the "telecom bubble" burst. Table 2 highlights the operating income of several of the major component vendors.

Company	2006 Revenues	Operating Income (OI)	2004 Revenues	Operating Income (OI)	Notes
	(Millions)	(Millions)	(Millions)	(Millions)	
AVANEX	$ 162.90	$ (54.70)	$ 106.90	$ (124.10)	
Finisar	$ 364.30	$ (24.90)	$ 185.60	$ (113.80)	
Agilent			$ 7,181.00	$ 349.00	Note 1
Avago Tech	Private Company				
EMCORE	$ 143.50	$ 58.70	$ 93.10	$ (13.50)	Note 2
JDSU	$ 1,204.30	$ (151.20)	$ 635.90	$ (115.50)	
Cyoptics	Private Company		Private Company		
Bookham	$ 231.60	$ (87.50)	$ 79.80	$ (67.40)	
LuminentOIC			$ 271.70	$ (10.70)	
OCP	$ 70.10	$ 1.40	$ 57.10	$ (1.30)	
Eudyna	-	-	-	-	
Excelight					
Sigma-Links					
Opnext	$ 151.70	$ (30.50)	$ 79.40	$ (80.50)	
Mitsubishi	$ 41,048.30		$ 31,917.80	$ 424.40	
Note 1: Agilent sold the Optics piece and it was formed as Avago Technologies Note 2: Include Sale of GelCore and Electronic materials					

Table 2: Review of current active component vendors and their financial results

The movement to transceiver modules compared to the traditional "golden box" discrete component has commoditized the market. There are several factors that have improved the operating income of several of the fiber optic transceiver companies, including the resurgence in the volume of sales to near-2000 levels. The optical components companies have also been actively engaged in downsizing by either pushing manufacturing off-shore or outsourcing production. Significant changes in the company structures have provided an ability to improve gross margins and get closer to breakeven. Each company should be reviewed based on its core competency and product portfolio. Both Finisar and Opnext have shown evidence of profitability in several recent quarters. Generally, the sector is

improving but is still not healthy enough to allow increased spending on R&D, a critical issue for the next generation of networks and component development.

3.6 Government initiatives

Governments around the world enable development of new technology and research through nationally funded programs. These programs impact the competitiveness and economic prosperity of a country. The U.S. government has traditionally funded research in areas that impact peoples' lives through several of its agencies.

This section highlights some of the facts related to research and development funding and information for the super computer segment and its impact on interconnect development in the United States and Japan. The principal reason to highlight these two countries' programs is the continued race to achieve the highest performance super computer. This race spins off of development activities that impact the mid-range and low-end computer markets which benefit the overall computer industry.

3.6.1 In the United States

The U.S. government has been the primary driver for high performance computer development over the last 40 years. The impetus for this has been:

1. National security needs
    a. Intelligence
    b. Conventional and nuclear arms
    c. Weather forecasting
2. U.S. competitiveness vs. the rest of the world
    a. Science and industry
3. Use of high performance computing (HPC) technology
    a. Medicine
    b. Climate research
    c. Biology
    d. Chemistry
    e. Materials
    f. Basic computer simulation (CS) tools research

The focus on HPC has enabled new advanced optical interconnect devices. There are several government agencies that fund research, including Department of Energy (DOE), National Science Foundation (NSF), National Security Agency (NSA), National Aeronautics and Space Administration (NASA), and the Defense Advanced Research Projects Agency (DARPA).

DARPA has provided a major focus for the computer companies by funding programs between industry, government, and universities. The level of interest and investment by

the U.S. government in optical interconnect technology can be understood from several programs that DARPA has invested in. Several of these are highlighted in Table 3.

DARPA Project Name	Period	Budget ($MM)
Analog Optical Signal Processing	2002-2005	37
Chip to Chip Optical Interconnects	2003-2007	45
Chip Scale WDM	2002-2005	40
Data in Optical Domain- Network	2002-2006	60
Optical CDMA	2003-2007	45
Photonic A/D Technology	1998-2001	40
Note: Reference Science and Technology Trends No.20 July 2006		

Table 3: Summary of several DARPA-funded programs related to optical interconnects

(Source: Science and Technology Review, Quarterly Review No. 20 - July 2006)

The continued focus on next generation and enabling technology by DARPA and other government agencies has helped the U.S. economy and has enabled technology leadership for many U.S.-based companies.

3.6.2 In Japan

The Japanese government has continued to invest heavily in optical communication components. The size of the FTTH market is a clear indication of the demand within Japan and the government's goal for a connected society. When we look at computer systems and servers, there has always been a race between the U.S. and Japan for the "biggest and best" super computer. The race remains heated, with the U.S. and Japanese governments investing heavily in this area.

The Japanese optical components companies are researching several key areas in long wavelength communications for high data rate applications. For example, companies are currently investing in directly modulated 40 Gbit distributed feedback (DFB) lasers. Several key results were presented at the 2007 Optical Fiber Conference (OFC). There are a number of agencies in Japan that invest in new technology. A summary of the programs funded by the Japanese government (Figure 8) underscores the importance of optical technology to the country.

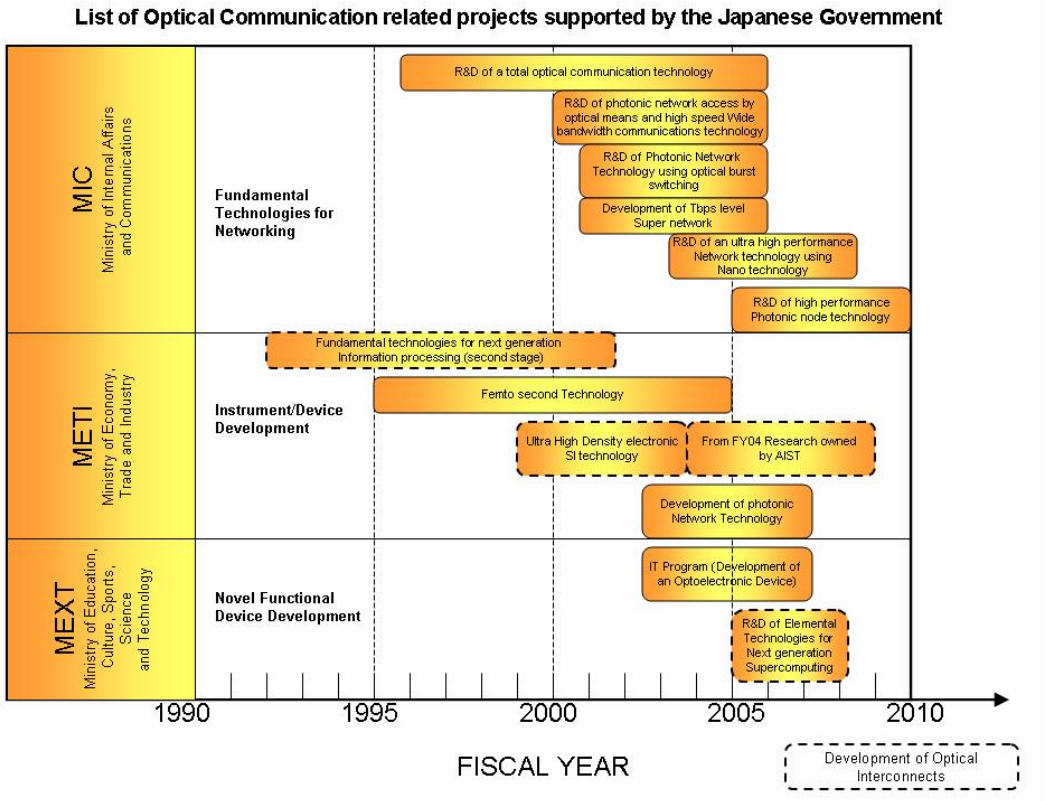

Figure 8: Overview of the government programs related to optical interconnects

(Source: Science and Technology Quarterly Review No. 20 - July 2006)

3.7 ITRS road map

The International Technology Roadmap for Semiconductors (ITRS) has defined a path for the next generation of technology nodes (Table 4). As part of the roadmapping process, the issues facing the semiconductor industry are discussed in this report.

Year of Production	2006	2007	2008	2009	2010	2011	2012	2013	....	2020
DRAM Stagger contacted metal 1 (M1) 1/2 Pitch (nm)	70	65	57	50	45	40	36	32		14
MPU/ASIC stagger contacted metal 1 (M1) 1/2 Pitch (nm)	78	68	59	52	45	40	36	32		14
Flash Uncontacted Poly Si 1/2 Pitch (nm)	64	57	51	45	40	36	32	28		13
MPU Printed gate length (nm)	48	42	38	34	30	27	24	21		9
MPU Physical Gate Length (nm)	28	25	23	20	18	16	14	13		6
Source: ITRS 2006 up-date										

Table 4: Predicted year of production and process node linewidth

(Source: ITRS roadmap)

Several bottlenecks have been predicted. A number of these issues were reported in a November 2004 OIDA forum on interconnects. Two areas were highlighted that optical device technology might be able to address:

1. The I/O pin count versus signaling rate per pin
2. intra-chip interconnects on the intermediate and global level (“red brick wall”)

These two areas are being addressed by research laboratories to find a potential solution. It is believed that continued advances in copper interconnect technology will dominate for the next 5 to 10 years until these bottlenecks can no longer be addressed by electrical solutions.

3.8 Standards development

Standards play a very important role in the development of communication networks and components. There are several different standards bodies for the different levels of network architecture, including:

OIF – Optical Internetworking Forum
IEEE – Institute of Electrical and Electronic Engineers
IETF – Internet Engineering Task Force
ITU – International Telecommunications Union
TIA – Telecommunications Industry Association

The use of standards, different protocol requirements, and technical specifications allows open network configuration and compatibility. Each organization has a vested interest in its own requirements and development. The ITU is trying to understand the next generation telecommunications network. IEEE develops standards for local area networks and is currently addressing 100 Gbit Ethernet as the next generation data rate for switched networks.

Today’s data center and servers utilize several of the standards developed by these bodies. How the implementation of protocols changes within the data center over the next decade is not clear. As we look forward to board-to-board and intra-chip optical interconnects, different standards bodies may be involved.

4 Electrical interconnects overview

Within the data center, there are several different types of interconnects. To enable some distinction between the different requirements for optical technology, this report segregates the connections into intra-chip, inter-chip, and backplane interconnects.

Today, the majority of connections are copper based. Optical solutions can enable higher performance and fast data rates. The penalty that will be paid as signals move around optically is associated with the electrical to optical conversion either at the transmitter or the receiver. The extent of this penalty is connection–dependent and needs to be analyzed as part of any cost or improvement driver.

4.1 Overview of the interconnect segmentation

The next few sections provide a basic overview of the types of interconnects and challenges associated with each.

4.1.1 Intra-chip interconnects

Within the IC, the individual transistor and circuit blocks must communicate via metal wires. As the photolithography linewidth decreases, the transistors become smaller and faster. This leads to more transistors per unit area and denser intra-chip interconnects.

The IC the wiring hierarchy typically uses shorter wires nearer to the silicon surface and increasing longer wires at higher layers. The lower levels of interconnect are thin and are used in local routing. Intermediate layers are of medium thickness and used for semi-global routing. Finally, the top layers are the thickest and are used for global routing across the IC. The different levels of interconnect are customarily laid out in orthogonal directions to minimize cross-talk between adjacent levels. Furthermore, this convention helps to simplify routing patterns. Figure 9 highlights an example of this wiring hierarchy.

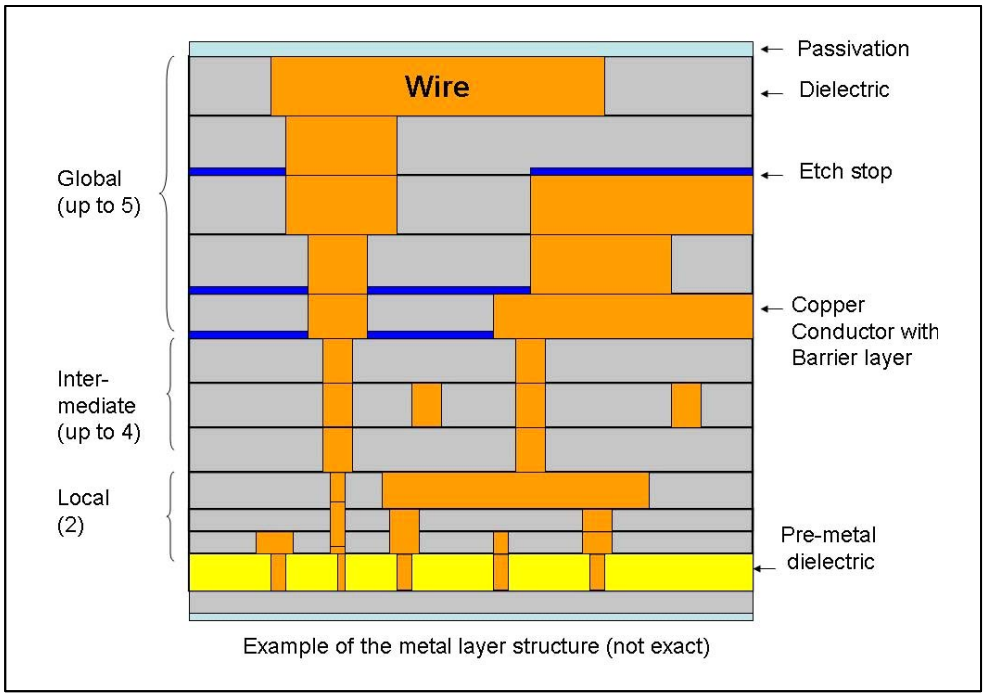

Figure 9: Example of the metal interconnects layers in an IC

As the clock frequency increases and the processing node decreases, global interconnects which span the chip exhibit higher resistance-capacitance (RC) time constants. This leads to increasing interconnect delay, transition time, and cross talk. In the majority of CMOS processes used today, the global interconnects are typically broken up into shorter links and signal is regenerated with repeaters. This breaks the long wires into smaller short segments which decreases the overall delay. The delay now becomes linear in nature rather than quadratic. The issue with the repeater is the delay introduced by the repeater itself and the associated power penalty because of this additional circuitry. For processors operating at Gigahertz clock frequencies, the global wires must be designed assuming resistance, inductance, and capacitance (RLC), not just resistance and capacitance.

The two main parameters characterizing the electrical interconnects are propagation delay and the interconnect bandwidth density. The delay can be reduced by increasing the interconnect width, but this is at the expense of a smaller bandwidth density. As the global interconnects are delay limited, it is expected that optical interconnects should be able to provide advantages here over the current approach. The current figure of merit for delay optimized global electrical interconnects is 1mW/mm, but this is expected to increase in the future. As the process node is lowered, the electrical bandwidth density can increase. This provides a moving target for optical interconnects to hit. For optical intra-chip interconnects, the main challenges are:

- technology implementation (silicon photonics, organic waveguides?)
- thermal and power consumption

- architecture and design rule changes
- package design

4.1.2 Inter-chip interconnects

There is a requirement on the circuit card to transfer data more efficiently between the CPU and off-chip memory. Chip packages today connect to off-chip memory using ball grid array packages that connect to the circuit card traces. The interconnection point and trace can provide loss of signal integrity. To implement an optical solution, we would need to change the I/O from optical to electrical, as shown in Figure 10.

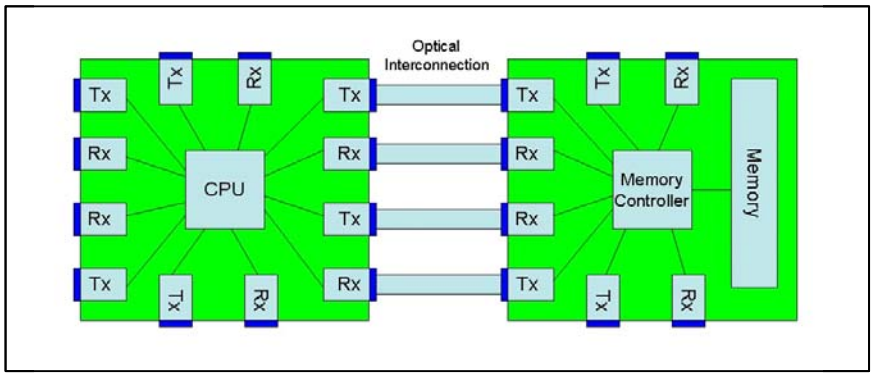

Figure 10: CPU and memory module example configuration

This represents a significant departure from current IC packaging and circuit design. There are fundamentally two elements that would need to change:

1. circuit card design and materials
2. I/O from the IC package

The design of this “OE extension” module that connects to the silicon circuit is not currently defined by any industry standard. There are several technical publications that show the potential of the VCSEL array to connect to a receiver array on board. The desire to provide the OE connection is a continuing challenge with the current industry dynamics.

The main implementation in practice today is rack-to-rack connections with parallel optical modules based on SNAP-12 or POP 4 multi-source agreements.

4.1.3 Backplane interconnects

Today’s servers are mainframes, racks, or blade server configurations. Copper backplanes connect between server blades or cards. The copper connectors in the backplane are produced by several key manufacturers, such as Tyco, Teradyne, Molex, and FCI.

These manufacturers have released a roadmap for copper connectors up to 40 Gbit/s (Table 5).

		1Gb/s	2.5Gb/s	3.125Gb/s	4.0Gb/s	6.125Gb/s	10Gb/s	40Gb/s
Connector Technology	Teradyne connectors	HDM		VHDM & VHDM L-Series		VHDM-HSD	GBX	GBX
	ERNI Connectors	ERNet		ER met		Ermet ZD	ERmetZD	Ermet Zero XT
	Tyco Connectors	HM-ZD		Z-Pack HM-ZD MultiGig RT-1		Z-Pack HM-ZD	MultiGig RT-2	MultiGig RT-3
	FCI	Metral 2000		AIRMAX VS Metral 4000		AIRMAX VS		AIRMAX
	Fujitsu			FCN-261Z00x			FCN260D	
	Winchester			xcell				SIP-1000 I platform
	Molex	Molex is teradyne licensee						
Published by iNEMI								

Table 5: Copper technology roadmap published by International Electronics Manufacturing Initiative (iNEMI)

(Source: www.inemi.org)

The backplane provides for board-to-board interconnects. The architecture is a switched fabric architecture. There are principally two switch fabric architectures, as highlighted in Figure 11.

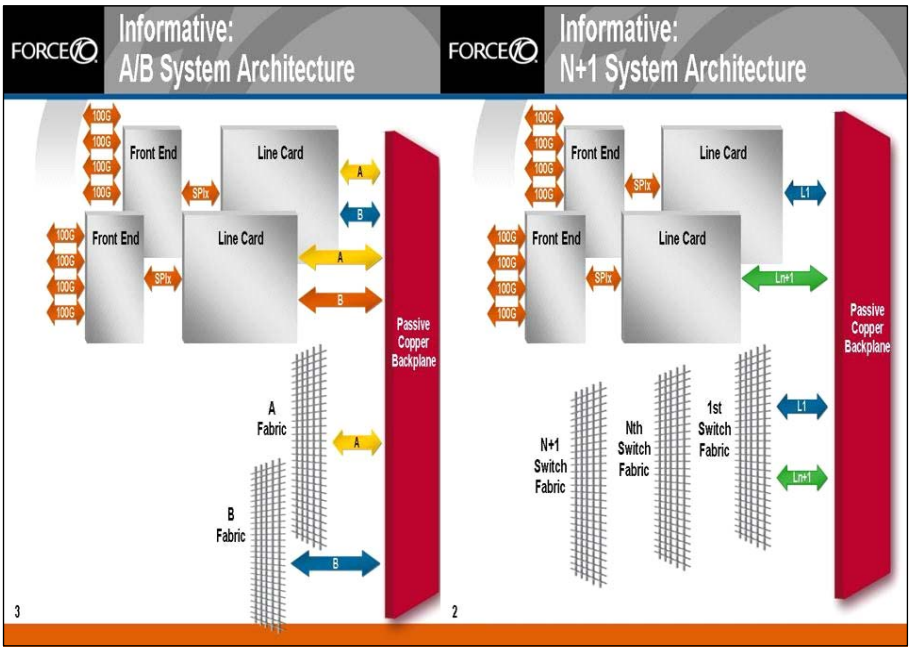

Figure 11: Backplane switching architecture

(Courtesy of J. Goergan, Force10 Networks – OIDA 100 Gb Ethernet Forum)

To move to an optical backplane, optical waveguides and connectors in the printed circuit board (PCB) need to be developed. Implementation would need to be standardized by the IPC-Association Connecting Electronics Industries or other standards organization. Sev-

eral companies are developing optical waveguide technology for the PCB with great success, but several key challenges remain, including:

- architecture
- fiber/polymer or embedded waveguides
- implementation approach
- connector type

Optical will eventually be required. The market and application may not necessarily be in servers first, but could be in other markets such as cell phones.

5 Photonics in the communications industry

There are several requirements for the optical interconnect to move further toward the chip domain in computer and server systems. The technology in use today is based on the switch and router requirements for long distance optical networks. The dichotomy in the area is between short reach links (links < 300 meters in length) and long reach links (links > 300 meters). The breakdown in optical networks is based on the link budget requirements and so has been segregated into transmitter and receiver type vs. distance and bit rate. Examples of these specifications are provided in Tables 6 and 7. These show the classification imposed on links for SDH transport networks.

Application		Intra-Office			Inter- Office		
			Short Haul		Long Haul		
Source Nominal Wavelength nm		1310	1310	1550	1310	1550	
Type of Fiber		Rec. G652	Rec. G652	Rec. G652	Rec. G652	Rec. G652 Rec.	Rec. G653
Distance (Km)		<2	15		40	80	
	STM-1	I-1	S-1.1	S-1.2	L-1.1	L-1.2	L-1.3
STM Level	STM-4	I-4	S-4.1	S-4.2	L-4.1	L-4.2	L-4.3
	STM-16	I-16	S-16.1	S-16.2	L-16.1	L-16.2	L-16.3

Table 6: Application table from the ITU, specifying link length classification

(Source: ITU-T G957 Specification)

	Unit	Values					
Digital Signal		STM-16 according to Recommendations G707 and G958					
Nominal Bit rate	kbit/s	2488320					
Application code		I-16	S-16.1	S-16.2	L-16.1	L-16.2	L-16.3
Operating Wavelength range	nm	1266-1360	1260-1360	1430-1580	1280-1335	1500-1580	1500-1580
Transmitter at reference point S							
Source type		MLM	SLM	SLM	SLM	SLM	SLM
Spectral Characteristics							
- Maximum RMS	nm	4					
-Maximum -20dB width	nm		1	<1	1	<1	<1
-minimum side mode	dB		30	30	30	30	30
-suppression ratio							
Mean Launched Power							
- maximum	dBm	-3	0	0	3	3	3
-minimum	dBm	-10	-5	-5	-2	-2	-2
Minimum Extinction ratio	dB	8.2	8.2	8.2	8.2	8.2	8.2

Table 7: Application table specifying transmitter and receiver requirements

(Source: ITU-T G957 Specification)

By providing distinct operating requirements, these types of standards enable interoperability between systems. Because of the standards specified for networks, optical components have moved to a module-based component structure. The modules are referred to as transceivers and contain memory, driver, and receiver chip sets, and can contain CDR, MUX, and DE-MUX functions. The actual complexity of the module depends on the form factor and requirements from the customer (switch, router, or host bus adaptor). For server and board interconnects, the question on applicability may require alternative standard requirements and reliability requirements. For intra-chip and inter-chip connections, the actual “module” might develop into different form factors

than those readily available today. The main issue for the current entrenched supply base is the lack of incentives and investment money to exploit a potential high volume server chip interconnect market.

5.1 Fiber optic connectors and cable assemblies

The standard fiber optic components in servers and switches today are transceivers and fiber optic cable assemblies. These are based on well known and mass manufactured products. For circuit board routing, optical waveguide is an alternative device technology that can be employed. For Fibre Channel SANs and Ethernet LANs, fiber optic components utilize both single-mode and multi-mode fiber cable assemblies. These are typically duplex (two) fiber connections. For servers using proprietary and/or InfiniBand connections, parallel optic modules are utilized. Parallel modules use ribbon fiber cable assemblies. The different connectors for the fiber cable used today are MT-RJ, LC, SC, and MPO connectors. All of these connectors provide a different ferrule size and fiber spacing. Table 8 provides dimensions of each connector type.

Connector Type	Ferrule Diameter	Fiber spacing	SM/MM
ST	2.5mm		Both
SC	2.5mm		Both
LC	1.25mm	6.25mm	Both
MT-RJ	2.5mm x 4.5mm	0.75mm	Both
MPO	3mm x 7mm	0.25mm	MM

Table 8: Ferrule dimension and connector types

For high density applications, the multi-fiber push on (MPO) fiber cable assembly is preferred. The cable assembly can be fanned out to other connector types or simply be MPO-to-MPO. Alternative fiber management techniques have been developed where effectively the fiber is encased in a plastic jacket and routed with terminated connectors at either end of the assembly. This approach is simple but custom to the chassis being used. With the fiber connector technology, if the transceiver solution goes parallel, there are two choices:

1. Combine multiple wavelengths down a single fiber – e.g., D-WDM/CWDM
2. Utilize parallel arrays e.g., 2-D and/or 1-D array ribbon fiber

Fiber optic cable is used extensively to transmit data across communication networks. It was first developed for the telecom network in the early 1970s. Improvements in drawing of the fiber and reduced impurities decreased the attenuation of single-mode fiber significantly. As fiber optic networks have evolved and new devices developed, the advantage of fiber has been employed on an ever-increasing scale. Local area networks employed multi-mode fiber with LED-based transmitters for 100 Mbit links and today 40 Gbit links are being employed in the core networks of the telecom carriers. Fiber optic cables for I/O connections for servers have been growing in popularity as the benefits and reliability

of the optic components improve. Multi-mode fiber is used extensively for short reach links because of the benefit of signal launch tolerance, cleaning, and low cost of the fiber optic transceivers.

There are different types of multi-mode fiber. The differences are characterized by the over-filled launch bandwidth. Due to its construction, the bandwidth of the fiber depends on the core diameter and material effective index profile. Table 9 summarizes the multi-mode fiber currently available.

Fiber	Wavelength	Core Diameter	Over Filled Launch Bandwidth
OM-1	850nm	62.5um	200
	1310nm		500
OM-2	850nm	50um	500
	1310nm		500
OM-3	850nm	50um	2000
	1310nm		
OM-3+	850nm	50um	4700
	1310nm		

Table 9: Fiber types in production and their over filled launch bandwidth

The multi-mode fiber modal properties have been studied extensively in the IEEE standard groups to allow higher data rate transmission over 62.5 um and 50 um core fiber. At 10 Gbit/s, electrical compensation techniques for the optical signal are used when the bandwidth of the fiber is too low. The single emitter standard developed for this application is the IEEE 10 GBASE LRM standard. For server and SAN applications, these restrictions are not typical as new cable can be deployed. Multi-mode fiber is currently the fiber of choice for the data center.

The high bandwidth fiber allows longer distances or higher data rate for equivalent distance. From the trend in cable type, higher bandwidth fiber is preferred for new installations over smaller bandwidth OM-2 or OM-1 fiber. Fiber length is also important to understand in terms of fiber cable interconnects. Current information suggests that 100 Gbit parallel optic transceiver links can meet a 100 meter distance requirement by utilizing OM-3 fiber.

5.2 Optical transceivers

Fiber optic transceivers are utilized in most network switches and SAN environments. For switches, the preferred transceiver is currently the pluggable module. For host bus adaptor cards, the through-hole version is preferred. The transceivers typically utilize InP devices for long wavelength 1310 nm applications and GaAs VCSEL devices for short wavelength 850 nm multi-mode applications. The parallel optical modules utilize VCSEL arrays for the SNAP-12 and POP-4 designs. The transmitter and receiver devices are the

core of the transceiver. The InP and GaAs material systems today have been shown to allow modulation from the p-n junction device up to data rates of 40 Gbit/s.

The long wavelength devices are dominated by ridge and buried heterostructure devices. These are typically distributed-feedback (DFB) or Fabry-Perot (FP) laser devices that are either directly modulated or externally modulated. The cost of these devices is volume and overhead dependent. These devices are principally used in single-mode fiber applications. Single-mode fiber imposes a tight alignment tolerance on the packaging unless mode expanders or waveguide manipulation are utilized. They are predominately used for long reach links greater than 300 meters.

The two principal transceiver module interfaces are duplex (LC/SC) or MPO connector. Alternative interfaces for transceivers are used in the automobile market (plastic optical fiber), but these are not discussed in this report.

5.2.1 Single channel – duplex

There are multiple types of fiber connectors. The transceivers that are shipped in volume today are mainly LC duplex interfaces. When the market moved from the 1x9 footprint to the small form factor footprint, there were several interfaces/connectors initially developed (Table 10).

Connector	Ferrule size	Fiber spacing	Latch
LC	1.25mm	6.25mm	RJ-top 2 latch
MT-RJ	2.5 x 4.4mm	0.75mm	RJ-top latch
SC-DC	2.5mm	0.75mm	SC push-pull
VF-45	None	4.5mm	RJ-top latch

Table 10: Connectors initially developed for the SFF transceiver

The issues of repeatability, insertion loss, back reflection, and mechanical stability were all investigated. The two connectors that prevailed were the LC and MT-RJ connectors. The LC is most widely used today because of the compatibility with TO-can technology and package diameter. The LC connector mated well with TO-46 and TO-56 assembly techniques for single-mode and multi-mode optical subassemblies. The fiber spacing provided enough mechanical tolerance to package two TO cans side by side. Other ceramic package types that utilized LC interface exist and these were developed later to enable cooling, optical isolation, or high speed RF feed through.

The market is segmented by protocol. The Ethernet and SANs markets are predominately served today by short wavelength transceivers. D-WDM, C-WDM, and SONET/OTN are mainly served by long wavelength transceivers. The FTTH market is different. This market typically uses fiber pigtailed product on a single fiber output/input.

The short wavelength market is dominated by the 850 nm VCSEL device. It utilizes a Bragg reflector in the device structure to launch the light through the top surface of the device. The VCSEL is a multi-mode device and replaced the 850 nm edge emitter technology in Fibre Channel (FC) applications. Short wavelength transceivers utilize multi-mode fiber interfaces/connectors. These VCSEL devices are widespread, dominating the 1 Gbit Ethernet optical transceiver market and SAN market. The ratio of short reach to long reach transceiver ports in the Ethernet market is 70:30 (850 nm:1310 nm) at 1 Gbit/s. This is expected to reverse at 10 GbE. For Ethernet, the SFP and X-type transceivers dominate. Examples of these transceivers are shown in Figure 12.

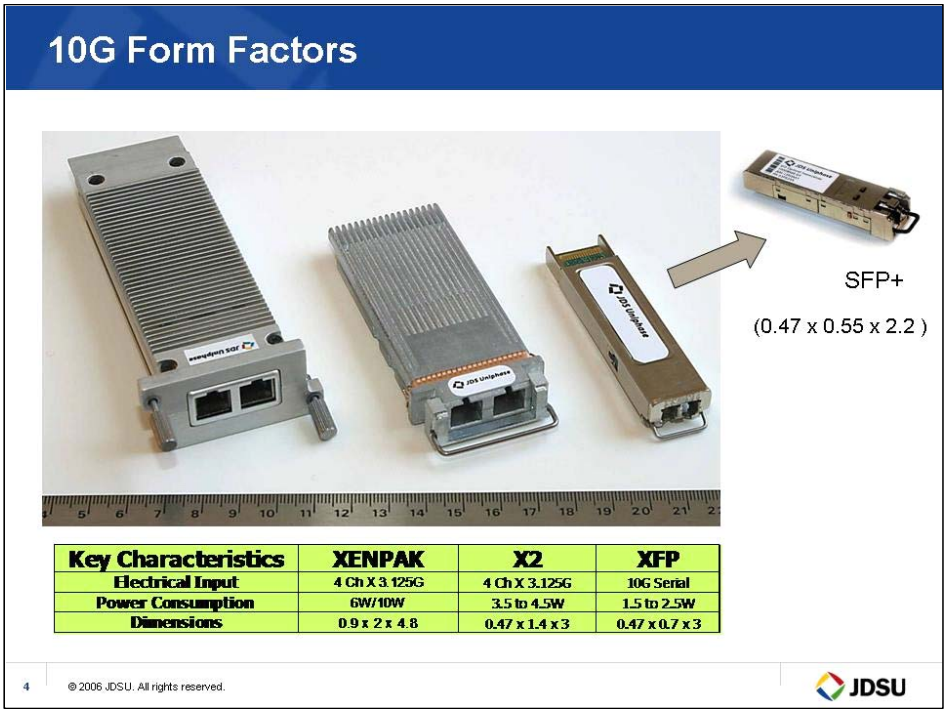

Figure 12: Examples of the duplex transceivers

(Courtesy of W. Jiang, JDSU – OIDA 100 Gbit Ethernet Forum)

At the higher data rates of 10 Gbit/s, additional ICs were initially incorporated into the transceivers to provide signal re-timer or multiplexer/de-multiplexer functions. The current trend in the industry is to push these functions back into the SER-DES on the host board. This is expected to reduce the electrical component cost within the transceiver. The reduction in footprint allows more ports per blade to be incorporated, increasing the density of 10 Gbit duplex transceivers on a board.

Work is progressing in the current Ethernet environment on developing 100 Gbit transceivers. The exact footprint, power consumption, and interface are still not clear. Due to cost constraints and development budgets, the industry trend is to utilize current component technology. This is an issue the industry will need to address as demand for high speed components becomes more pressing over the next few years.

5.2.2 Parallel channel

The parallel fiber architecture for interconnects was developed initially to solve the computer interconnect problem. A majority of funding of the basic research to enable these transceivers was provided by DARPA. The basic approach is similar to the ribbon cable used in the printers and computers in the 1980s. Instead of a parallel electrical connection, a parallel optical connection is used. The transceivers are E-O converters with parallel signal inputs (Figure 13). The transmission (optical) lines must be compensated for skew, but this method allows increasingly higher aggregate bandwidth to be provided, which is proportional to the fiber count.

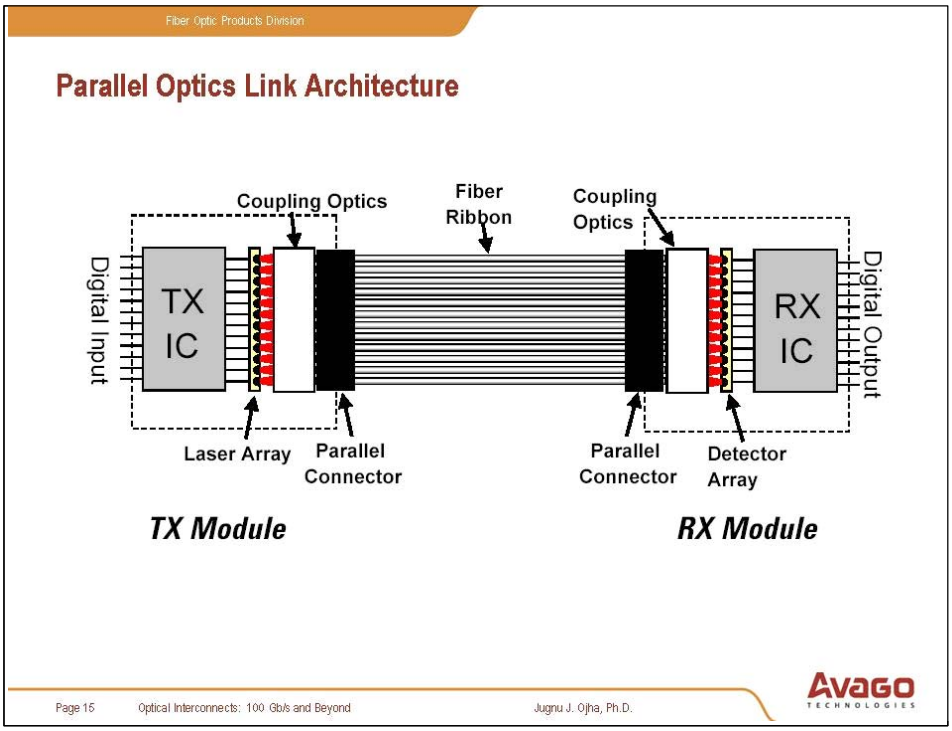

Figure 13: Parallel optical link architecture using VCSEL arrays

(Courtesy of J. Ojha, Avago Technologies)

The parallel links take advantage of VCSEL array technology. The array (photodiode or VCSEL) sits on top of an alignment substrate or electrical IC. The actual design is dependent on the manufacturer. Only a few companies have been successful with VCSEL array transceiver products. When these modules were initially released during the optical bubble, modules would fail catastrophically. The reliability concerns for parallel transceivers stem from the infant mortality issues related to dark line defects (DLD).

In the parallel module, certain designs require the VCSEL to sit on top of the electrical circuit. This design allows thermal transfer from the IC to the VCSEL array, which increases the junction temperature. As reliability and infant mortality are accelerated with increasing temperature and drive current, the removal of the heat from the package re-

quires careful design. The importance of junction temperature and heat load in parallel modules has been published by several companies.

As the GaAs material system suffers from DLD, all VCSEL devices require a burn-in to weed out the weak devices. Typically, the burn-in forces the DLD to move into the active region if it is present. To overcome this problem, Agilent Technologies (now Avago Technologies) released several publications on their 1x12 transceiver suggesting that moving to a longer wavelength alleviated this problem. By adding indium into the quantum well and shifting the wavelength to 980 nm, they showed that infant mortality could be reduced.

The advantage the parallel transceiver offers is that the aggregate transmission data rate can be 4 to 12 times higher than the current duplex transceivers. Additionally, a parallel transceiver can provide equivalent aggregate data rate to a duplex transceiver but utilize lower electrical data rates. This approach can alleviate some of the signal integrity challenges that are seen at 10 Gbit/s and above. Figure 14 provides an overview of a parallel module.

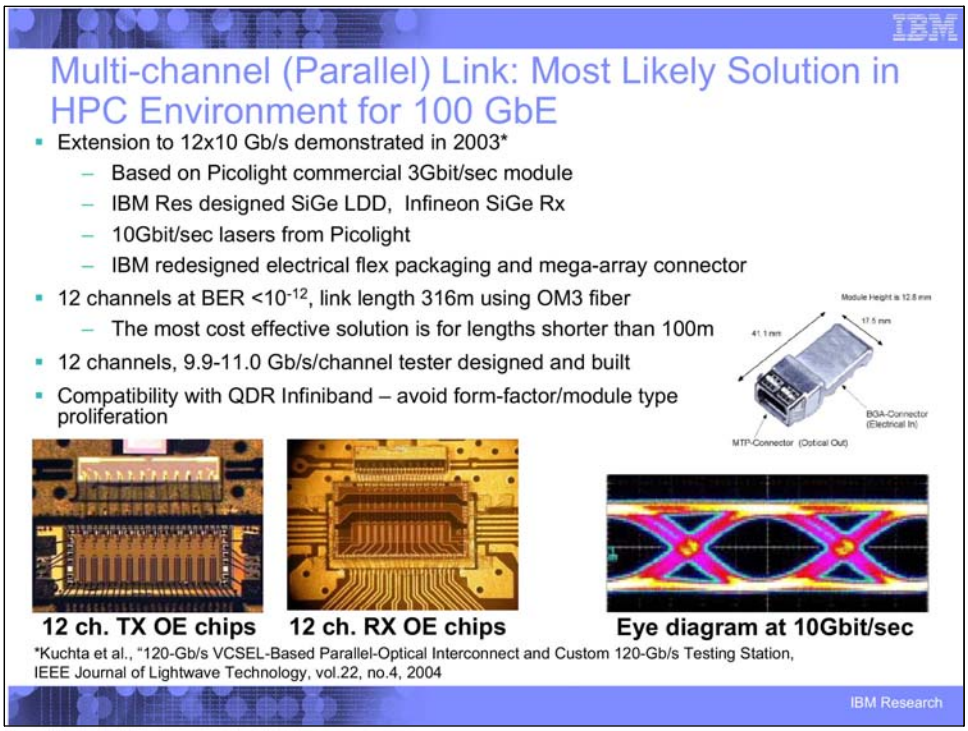

Figure 14: High performance computing parallel transceiver solution

(Courtesy of P. Pepeljugoski, IBM – OIDA 100 Gbit Ethernet Forum)

The VCSEL bandwidth, ESD and reliability are related to the active region diameter. Conference publications have demonstrated 20 Gbit/s modulation in the laboratory. If the VCSEL is unable to achieve higher bandwidth, do we need to look at alternative device technology for parallel modules? In the serial transmission space, the electro-absorption (EA) modulator or Mach-Zender (MZ) modulator approaches up to 40 Gbit/s are in production today. For rates above this, perhaps a different device will be required.

Alternatives to the POP-4 and SNAP 12 transceiver modules have been developed. The quad small form-factor pluggable (QSFP) module, which is based on the XFP mechanical package, has been released to the market. It utilizes an MPO fiber optic connector to allow parallel transmission from a pluggable port, similar to the current XFP duplex transceiver. The design takes advantage of the XFP surface mount connector, allowing migration to 4x10 Gbit or 12x10 Gbit/s modules. With the current development of high speed surface mount connectors these rates could potentially move to 4x25Gbit/s or 12 x 25 Gbit/s per electrical lane. A 12 x 25 Gbit/s parallel module would provide a 300 Gbit/s interconnect solution.

For board-to-board optical interconnects, the transceiver packaging will need to change. Potential solutions include co-packaging within the IC package or implementation of a silicon photonics solution. One of today's solutions is to integrate 850 nm VCSEL technology into the ball grid array (BGA) package or as an 'add-on' to the current silicon IC package. Co-packaging an O-E converter within the IC package will enable on-board optical interconnectivity. Several groups are using VCSEL technology because of the low drive voltages and alignment tolerance to multi-mode fiber or optical waveguides. Array technology is relatively mature and demonstrations of 2-D arrays connecting to circuit boards have been produced. The question of burn-in of the array and packaging/alignment is similar to the parallel module mechanics. This approach is a packaging exercise and very high precision assembly orientated. To move to a lower cost implementation, wafer scale integration will need to occur.

The current alternative solution is silicon photonics. This approach is being investigated by several companies, including Intel. The main question with a wafer scale approach is generating the light transmitter or light source. Several silicon photonic building blocks have been demonstrated including modulators, receivers, and transceivers. These demonstrations have used extrinsic sources. The simplest integration of the light source is currently achieved using standard flip chip die bonding techniques. To achieve a wafer scale source, the integration into the silicon fabrication line would be preferred. One method is to use wafer bonding of III-V material to the silicon. Wafer bonding is a common process in the LED industry. The idea is simply to add some III-V semiconductor that can generate the photons for the silicon laser resonator. This topic will be covered in more detail later in this report.

Integrated O-E converters would enable the optical PCB industry. The problem will be whether it should be based on 850 nm VCSELs or 1310 nm silicon photonics. The actual wavelength will need to be determined to enable the right properties of the waveguides to be implemented. 1310 nm VCSEL technology has been developed but is not in mass deployment.

Fundamentally, the conversion to an optical signal should be part of the silicon IC to achieve the lowest cost. The next section addresses the state of play of photonics integration.

6 Photonics integration

The long term goal for optical companies is the development of photonics integrated circuits. This objective has been discussed over the last 20 years. Optical technology is pervasive in our society. The optical industry, which invested heavily in InP and GaAs material systems initially, has enabled basic research that has spun out into different markets which have had widespread social and economic impacts. The optical storage industry and development of the GaAs-based CD and DVD laser have revolutionized the music and video industries.

Communications companies have tried to develop the all-optical network and have looked for the equivalent device building block of the ”optical” transistor to enable integration similar to the electronics industry. There has been a distinct lack of progress in this area. This lack of standardized semiconductor building blocks and the economic situation that many optics companies have faced over the last decade have provided an unfavorable environment. The industry remains segmented and distinct with many companies believing that the fabrication process provides their differentiation.

With regard to optical interconnects for the server and computer industries, there are key issues that need to be resolved. Several issues are driven by economics while others challenge the semiconductor material and integration requirements. As optical component transmission technology is currently at a different evolutionary stage than electronic manufacture, the goals and targets to enable the optical I/O need to be carefully evaluated. Research and development paths need to be evaluated and implemented. Fundamentally, integration of the optical semiconductor community with the electronic sector needs to occur in a coordinated fashion. Several of the ‘old’ ideas for optical semiconductors should be re-evaluated and the technology utilized and built upon.

6.1 III-V OEIC direction and challenges

Within the III-V optical community, photonics integration is a technology area that requires redefinition and evaluation. The current devices used in communication transport products are finally being developed with some functionality, but not yet on the scale required to make a drastic impact. Progress is hindered in standard building blocks and design tool sets by the ‘economic survival’ requirement. The lack of a ‘killer’ application is typically blamed for the inertia. Optoelectronic integrated circuit (OEIC) development and deployment are hindered by the requirement for a volume application and by questionable cost arguments.

The approach within optical communications, up to now, has been to utilize silicon as a platform for integration or low cost packaging. Several interesting developments have occurred as a result of this philosophy. For example, silicon micro electro-mechanical systems (MEMS) technology was developed for optical routing during the optical bubble. Today, this is the basic element of the consumer digital light processing (DLP) television, which produces high definition projection systems with 32 million color capability. In the packaging of components, low-cost technology is being utilized for optical storage. The

CD/DVD industry is currently required to provide backward compatibility. The optical read heads need to provide different powers and wavelengths. This is currently achieved by co-packaging of different laser die.

At present, there are several examples of III-V photonic integration. The simplest developments have employed integrating different functions within the same optical chip. An example of this is the tunable laser (Figure 15). The tunable laser provides a low-cost alternative to individual discrete wavelength lasers. It allows tuning over a wide wavelength window simply by altering the current on the electrodes of the device.

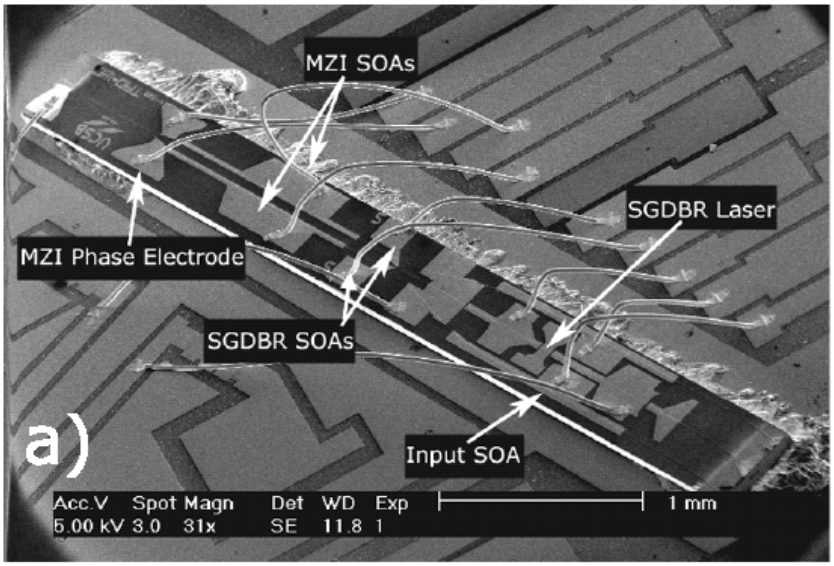

Figure 15: Tunable laser structure

(Courtesy of N. Puetz, JDSU – OIDA InP Foundry Workshop)

Integration of semiconductor optical amplifier technology provides variable power output and an additional control function.

Several researchers have demonstrated that band structure engineering can enable different functionality within the devices. Examples of this include polarization switching for optical flip flops and self pulsations for locking or providing an optical clock.

Waveguides on the III-V semiconductor can enable additional functionality. One difference between III-V technology and silicon electronics processing is epitaxial growth. In III-V devices, regrowth to provide device functionality is a standard practice. Epitaxial regrowth of silicon is not standard within electronic circuits. III-V regrowth allows buried waveguides or alternative routing schemes to be developed and deployed. The application of different layers with mode converters or adaptors is a critical area of design to prevent optical noise or beating. Routing then becomes a waveguide design problem coupled to the interaction of positive optical gain within a fixed cavity or confined structure. Complex waveguide modeling is required to understand the profiles coupled to the active

transparent optical light emitter. Beating and adiabatic transformation need to be analyzed and enabled/disabled depending on the required device functionality.

Several photonic circuits are currently being deployed within commercial systems for long distance communications. These chips or devices provide increased functionality with lower cost and added complexity. For optical transport, dense wavelength division multiplexing has increased the effective bandwidth density of optical fiber. Systems currently provide around 2 Terabits of fiber bandwidth. The transport of multiple wavelengths off of a single transmitter chip has been realized by Infinera. Their transport product utilizes an InP photonic integrated chip to provide a multi-wavelength transmitter (Figure 16).

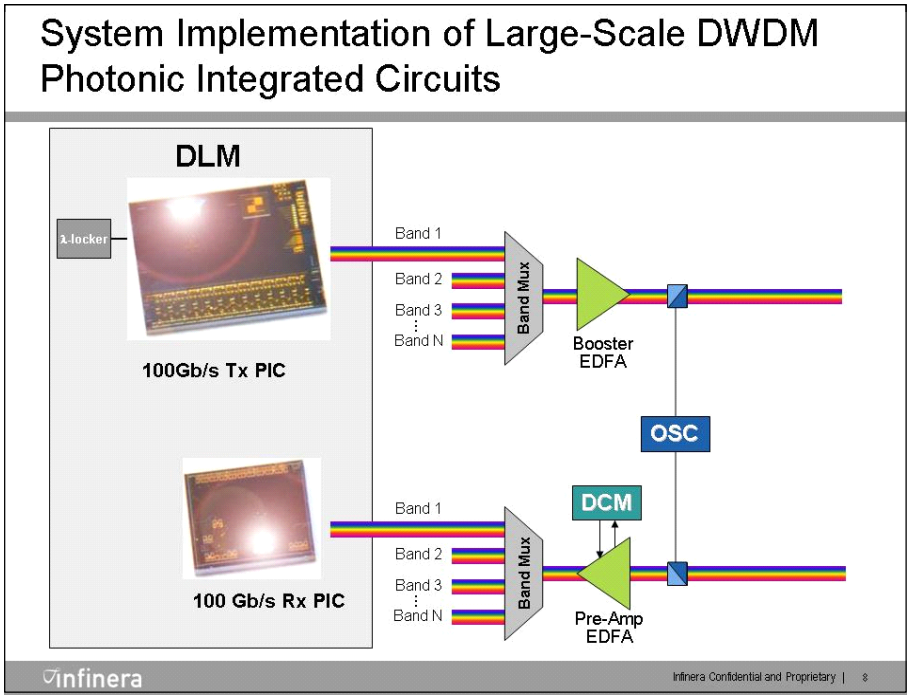

Figure 16: Example of a photonic integrated chip system

(Courtesy of F. Kish, Infinera – OIDA Micropackaging Workshop)

This approach is based on III-V waveguides married to III-V optical transmit and receive die on a single InP semiconductor wafer. This example leverages the economies of wafer scale production but is based on III-V substrates.

There are several waveguide approaches that can be employed and which have been published. These include the use of buried waveguides, ridge waveguides, or silicon waveguides. How to implement silicon waveguides depends on whether your definition of wafer scale is active devices on the same substrate or integration through deposition, epitaxial growth, etching, or fusion.

The deposited waveguide approach allows interconnection between elements using surface waveguides. An example of this is to use silicon dioxide deposition as a planar

waveguide process. This approach has been studied by Sarnoff Corporation for integrated optical functionality (Figure 17).

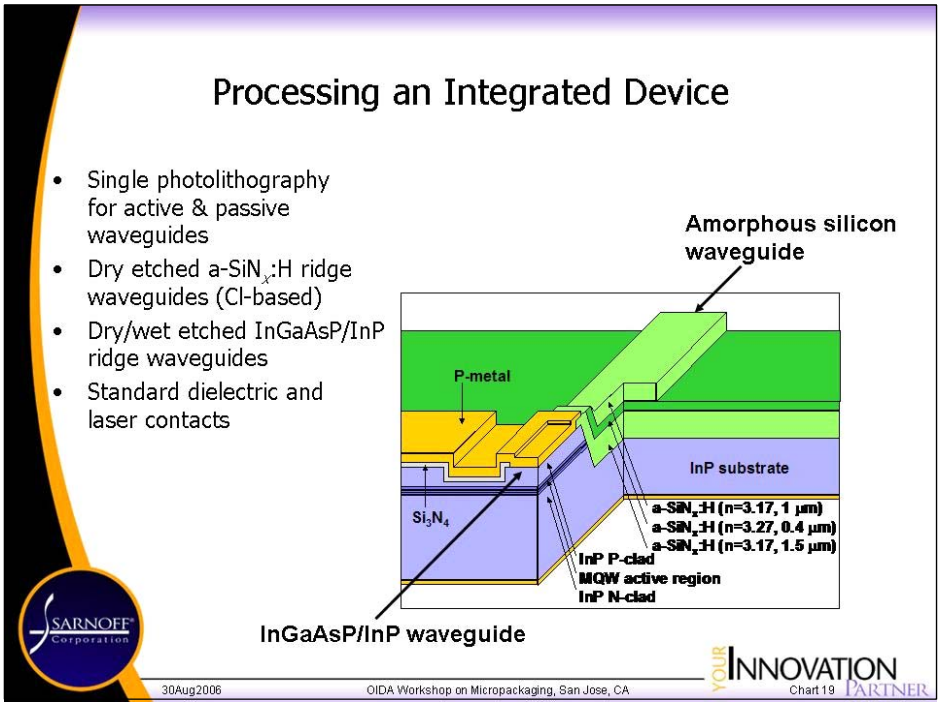

Figure 17: Processing example of an integrated waveguide to an active optic device
(Courtesy of J. Abeles, Sarnoff Corporation – OIDA Micropackaging Workshop)

By depositing the waveguide on the etched surface and using photolithography mask steps on the planar surface, functionality can be added. This approach allows the integration of current industry standard devices such as arrayed waveguide grating devices (AWG) to emitters and receivers (Figure 18). The wavelength discriminator (i.e., AWG) can be implemented without additional bonding or optical packaging. The alignment step is now wafer level and simply another deposition and photolithographic step. The major concern with this approach is the InP substrate. Commercial substrates today are relatively small compared to silicon wafers. Most processing of InP optical devices remains on two- to four-inch diameter wafers, which are relatively brittle compared to silicon.

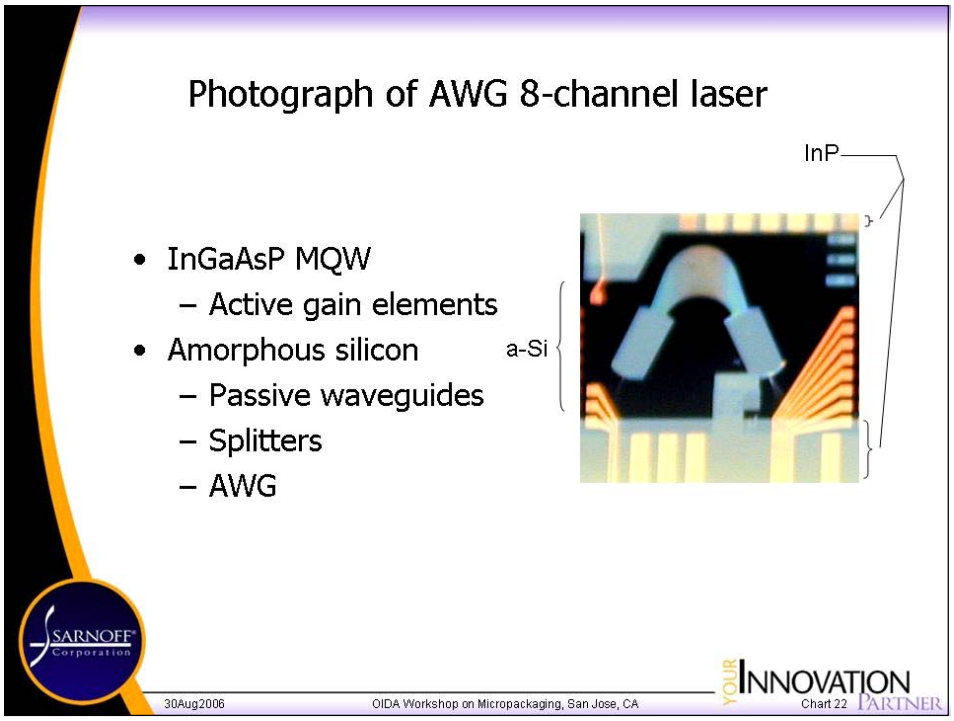

Figure 18: Processing example of an AWG active optic device

(Courtesy of J. Abeles, Sarnoff Corporation:– OIDA Micropackaging Workshop)

The issue with increased optical functions is the wafer area required. For example, a wavelength of 621 nm is equivalent to a photon with energy of 2eV. For an electron, the 2eV energy is equivalent to a wavelength of only 0.87 nm. Using this simple argument, photonic circuits require two orders of magnitude more wafer area than the equivalent electronic device. This is a huge implication for optical photonic circuit functionality. Density is a problem that would need to be assessed prior to replacing equivalent electrical functionality.

A neglected area that most silicon companies must consider, as we move above 100GHz frequencies, is the relatively high breakdown voltage of InP electronics. Electronic drivers and receiver circuits developed on III-V materials have produced extremely high f_{max} values with larger breakdown voltages than silicon germanium transistors. Recent work under a DARPA program enabled modulation to be achieved at 160 Gbit/s (Figure 19). This technology could be married to optical components in an integrated IC with waveguide technology to achieve ultrahigh bit rate processing.

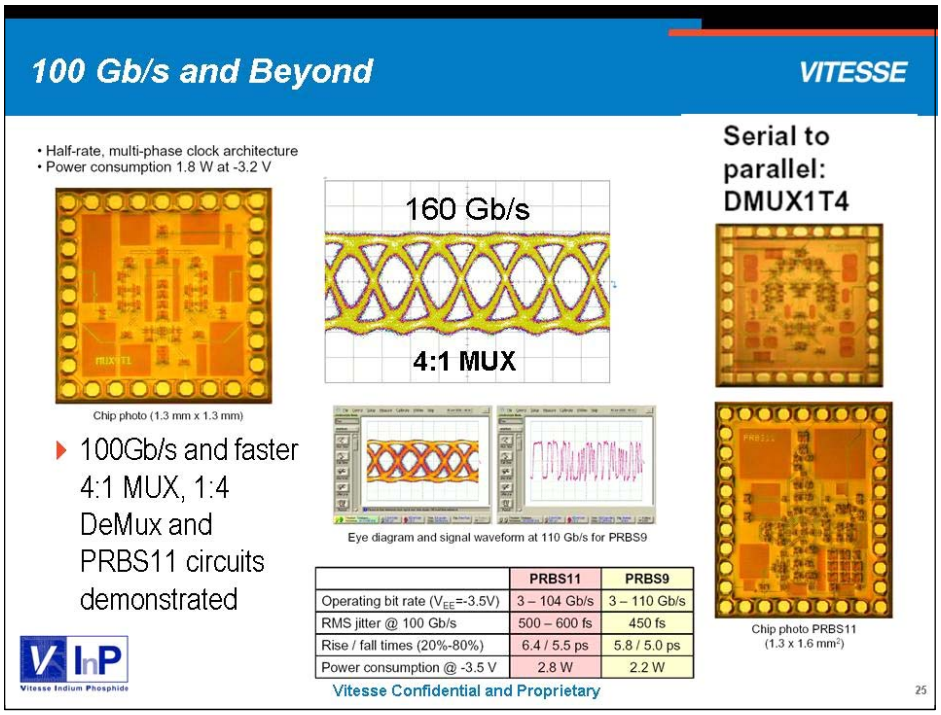

Figure 19: InP electronics with high breakdown voltage transistors for > 100 Gbits

(Courtesy of R. Milano, Vitesse – OIDA 100 Gbit Ethernet Forum)

The wafer scale approach for III-V photonics remains limited. The small volumes seen in the communication segment and issues of process capability coupled to wafer size are some of the issues that impede new developments. Alternative technology is typically used, such as hybrid integration, which involves 'packaging' of the discrete components on an optical 'breadboard.' Due to it nature as the most mature semiconductor technology, silicon is ideal for this application.

The current communications business climate and lack of a killer application have ensured that III-V photonic integration progresses at a relatively modest pace. As we investigate silicon photonics and the implications of light emission, we should review some of the basic concerns with III-V material which can provide the emission wavelengths of interest for silicon photonic solutions.

6.2 III-V long wavelength material issues

To achieve wavelengths in the 1100 nm to 1900 nm range, devices are grown on indium phosphide (InP) substrates and up to 1300 nm on gallium arsenide (GaAs). To achieve the wavelength and improve the optical power, the devices typically use band structure engineering.

The optical properties of III-V semiconductor compounds are very well understood. The theory of optical gain and the impact of dimensionality on optical emission or conversion stems from the density functional theory applied to microwave amplification by stimu-

lated emission of radiation (MASER). The practical application involves layers of material which are thin, i.e., on the order of the De Broglie wavelength of the electrons, coupled with carrier and optical confinement design.

The optical gain function is basically assumed to be a Taylor series expansion of the dipole moment wave functions. This leads to an optical gain which converts a many-body wave function Hamiltonian into a simpler representation. Essentially, we can view the optical gain of the semiconductor to be a function of the dipole moment $<\phi_1|\ e.\mathbf{r}|\ \phi_2>$, which is related to the band structure of the semiconductor through the band gaps and effective masses of the electronic states. Several papers by Adachi have used this relationship to provide insight into the optical gain of direct band gap semiconductors and the impact of dimensionality. This understanding has driven several of the significant developments in low dimensional structures for laser devices produced today.

Historically, temperature sensitivity has been a major issue for long wavelength devices for optical communications. There has been tremendous debate on the issues, which included discussion on the band structure, loss processes, optical gain, and current density. It is believed there are three main loss mechanisms today that impact the long wavelength devices:

1. Inter-valence band absorption
2. Auger recombination
3. Hetero-barrier leakage

All three mechanisms have a direct impact on the light emission of the device, either through heat, optical loss, carrier injection efficiency, or optical gain. As we discuss one of the approaches to silicon photonics, which involves wafer bonding of InP to a silicon resonator, the impact of these loss mechanisms needs to be considered.

6.2.1 Intervalence band absorption

The intervalence band absorption mechanism occurs in direct band gap semiconductors. It is a photon re-absorption process, which effectively increases the absorption coefficient (loss) of the optical cavity and active region material. From simple laser theory, the roundtrip gain of the laser cavity must equal the cavity losses. The optical cavity loss is increased in the presence of intervalence band absorption, i.e., $\alpha_i = \alpha_{material} + \alpha_{ivba}$, where α_i is the absorption coefficient for the material in the cavity. In a direct gap semiconductor, the emission wavelength is governed by the band gap of the semiconductor. The semiconductor has a conduction band and three valence band states called the heavy-hole, light-hole, and spin split-off. The four bands are analogous to the S, Px, Py, Pz electronic orbital discussed in coherent and ionic bond formation. In band structure theory, the conduction and valence bands are actually hybridized equivalents of the atomic orbitals, i.e., Bloch functions.

In the intervalence band absorption process, the laser light traveling in the cavity is re-absorbed by an electron-hole transition from the spin-orbit band (Figure 20). This effect

becomes more and more dominant as the band gap energy (E_g) becomes equivalent to the spin-orbit gap energy (Δ).

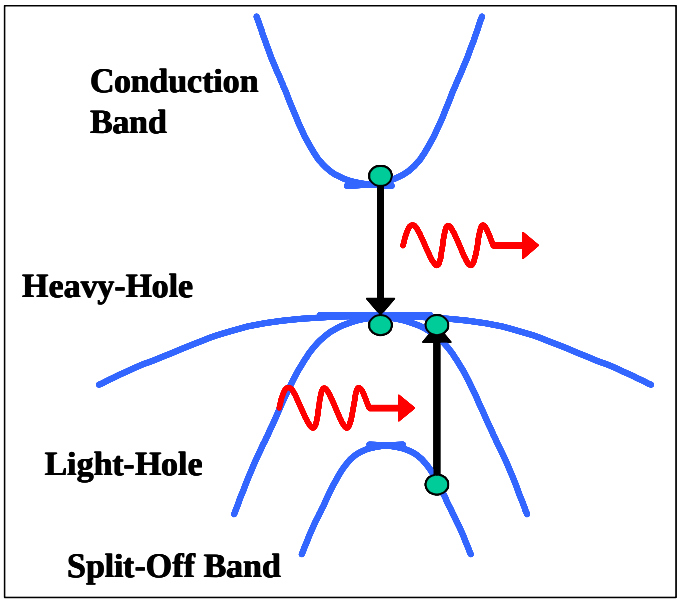

Figure 20: Emission and re-absorption process for semiconductor lasers

The overlap integral for the dipole moment is dependent on the k-vector in the band structure. The absorption coefficient will depend on the dipole moment strength and the density of holes available for re-absorption. As the quasi-fermi level for the holes moves further into the valence band the absorption rate increases. Modification of the band structure through stress or strain in the crystal lattice has been shown to alter the IVBA rate. In 1990 it was shown that IVBA was not the dominant temperature loss mechanism in InP quantum well lasers.

6.2.2 Auger recombination

Auger recombination is a non-radiative process involving either electrons, holes, or both. The current injected into the laser, instead of going to produce laser light or spontaneous emission, produces a non-radiative current instead. The process can be a direct band process or phonon assisted. It directly impacts the internal quantum efficiency through the relationship:

$$\eta_i = (1+ (\tau_{rad}/\tau_{\text{non-rad}}))^{-1}$$

There are several direct energy band processes. Each process is related to the energy gaps involved and the effective masses of the hole and electron states. In its simplest form, the Auger recombination is governed by the Boltzmann equation. The Auger recombination rate is exponentially related to the band gap and spin-orbit energy gaps. Several research papers have examined the impact of Auger in direct band gap semiconductors. The sim-

plest analysis utilizes the effective mass of k.p theory to calculate the transition overlap integrals and the activation energy. In materials where the spin-orbit gap is equivalent to the direct band gap, the CHSH process dominates. Auger recombination process can additionally occur by the interaction with the lattice vibrations (phonons). Figure 21 highlights the CHLH direct band process.

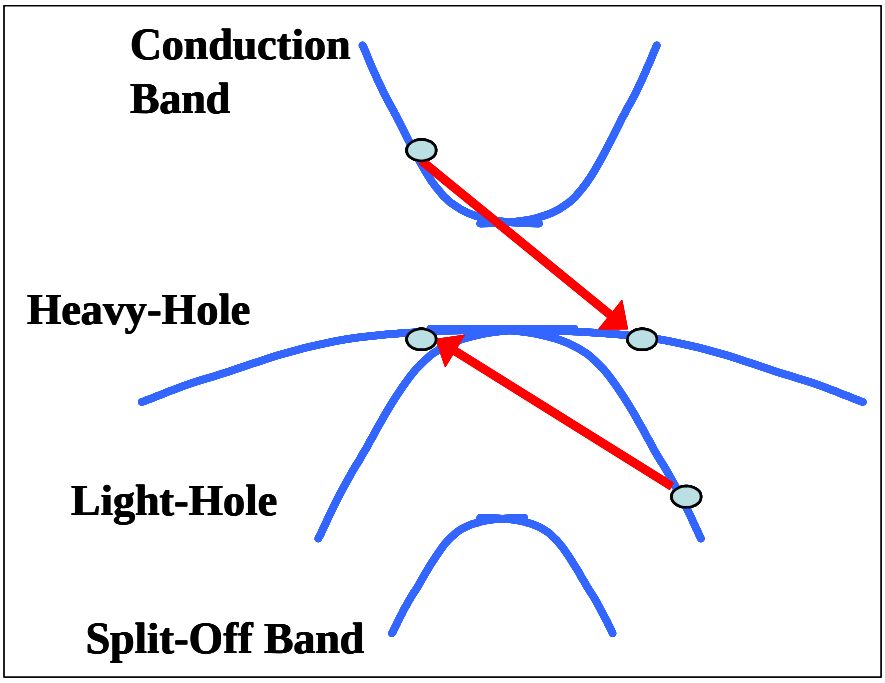

Figure 21: Auger recombination process for CHSH combination

As the direct band gap energy gets close to the spin-orbit energy gap, the Auger recombination rate increases rapidly. Additionally, as the energy gap decreases, the activation energy for the process lowers, again increasing the amount of non-radiative recombination in the material. Today, it is believed that the temperature dependence of semiconductor diode laser is dominated by the Auger process.

6.2.3 Hetero-barrier leakage

The third loss mechanism that can decrease the ex-facet efficiency and injection efficiency in the laser is hetero-barrier leakage. This basically involves two mechanisms. As the device is driven at high currents, the Fermi-level of the active region is effectively pinned, but the Fermi-levels for the cladding are not. This leads to a bending of the bands that can allow tunneling out of the active region. Additionally, depending on the material system, the electronic energy difference of the materials allows thermionic emission to occur. This process basically takes a portion of the injection current and prevents it from contributing to the laser current. As the laser is driven well above threshold, thermionic emission and tunneling current can increase, leading to a reduction in slope efficiency.

Figure 22 shows the concept of the band bending and electron excitation out of the quantum well.

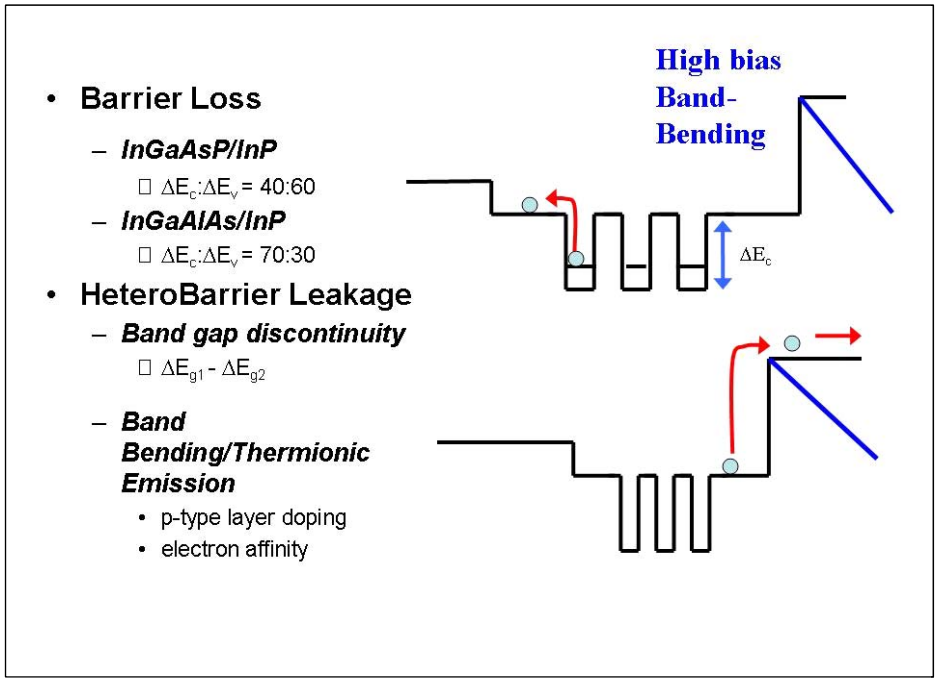

Figure 22: Leakage currents shown for InP-based lasers

There are research efforts underway that use InP-based material as the 'photon generator' for wafer based silicon lasers. This approach involves basically using the InP semiconductor structure as the point source, which is then coupled to a silicon resonator to provide feedback. This is discussed in more detail later.

7 Silicon photonic devices

A fundamental hurdle for silicon photonics is the inability of silicon to emit light through electrical injection. To overcome this issue, there are several approaches to provide light emission. Some of these are traditional and based on a hybrid approach; others involve more complex processing/structures or even band structure engineering. Silicon technology has been developed and implemented in the communications market. The next sections provide information on several of the adopted approaches.

7.1 Silicon bench and hybrid integration

Hybrid integration has traditionally involved different levels of packaging in the communications space. Silicon has always been viewed as a good platform for hybrid integration. Several major companies have developed and implemented versions of silicon photonics within the communications sector. The level of integration can be broken down into the three basic configurations:

1. Silicon sub-mount technology
2. Passive waveguide technology
3. Passive alignment technology

To best illustrate this, the following sections highlight some of the different types of development.

7.1.1 Silicon sub-mount technology

The silicon sub-mount technology is used in production today but mainly where an assembly is actively aligned. The best example of this is the famous Laser2000™ approach widely published in the late 1990s. Lucent Technologies developed this technology for mass production of laser modules. The silicon provides the sub-mount for the laser diode. It incorporates bond pads, lenses, and RF traces for high speed applications. The basic sub-mount employed a ball lens bonded to the sub-mount to provide mode expansion of the laser field. This basic method allows the optics designer to move the sub-mount within the package for optical alignment to the fiber that is outside of the package wall (Figure 23).

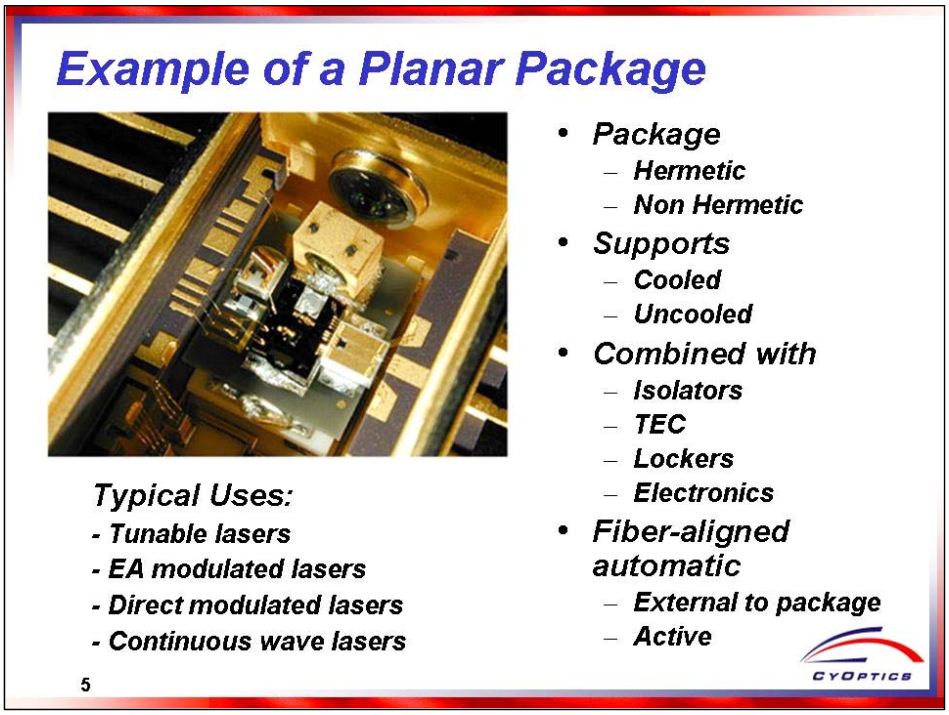

Figure 23: Integration of a silicon sub-mount in a discrete packaged module

(Courtesy of J. Dormer, CyOptics – OIDA Micropackaging Forum)

Essentially, this approach provides a mode expanded laser for easier coupling to a fiber ferrule.

7.1.2 Silicon/silica passive waveguide technology

There are different methods to make waveguides. These can involve complex processing or simple fabrication steps. To enable optical waveguides on silicon, there are two approaches currently in place. Silica waveguide technology has matured enough to enable commercial product. This type of waveguide for coupling and transmission between optical components has been designed and developed for wavelength discrimination and wavelength routing. In the communications industry, the approach is to manufacture an arrayed waveguide grating (AWG) to provide wavelength routing (Figure 24).

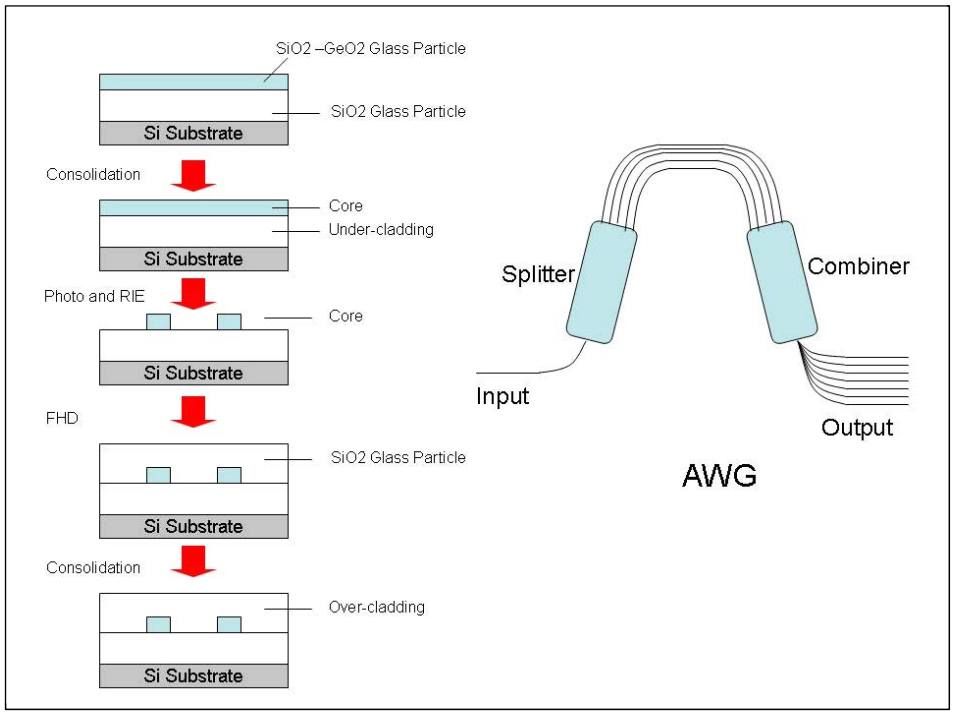

Figure 24: Arrayed waveguide diagram and process flow

The arrayed waveguide is an alternative to thin film interference filters for dense wavelength division multiplexing (DWDM) systems. To produce the waveguides, the key process is flame hydrolysis deposition (FHD).

The second approach is to use silicon–silicon dioxide silicon (Si-SiO2-Si) waveguides. The advantage of using silicon waveguides compared to silica is that direct integration with optical devices should be simpler (Figure 25).

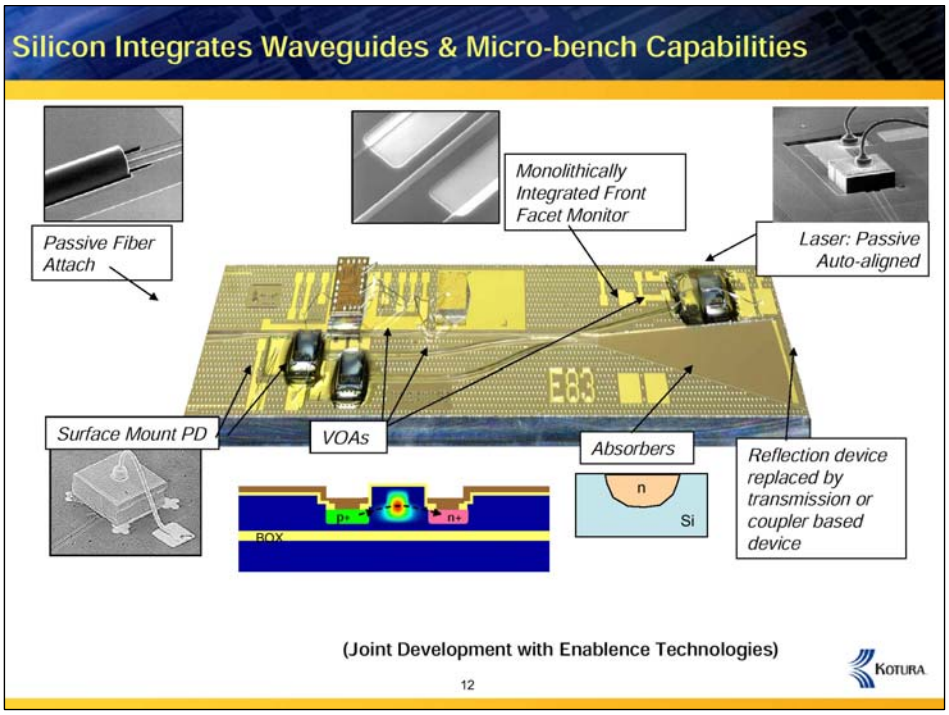

Figure 25: Example of a silicon optical bench with waveguides

(Courtesy of J. L. Malinge, Kotura)

The advantage of using waveguides is the ability to produce highly functional devices. It has the potential to become wafer scale and reduce the number of final components that need to be assembled.

7.1.3 Passive optical alignment

The silicon optical bench has been intensively investigated to enable a new optical platform in optical communications.

The solution of die bonding a III-V light emitter to a silicon substrate is the simplest and easiest solution to implement. The basic approach is to provide a bond pad, align it to a waveguide either actively or passively, and attach it with a gold–tin eutectic die bond (Figure 26). The electrical driver connection can be either by using a dual sided flip chipped device or wire bonding to the n-side contact.

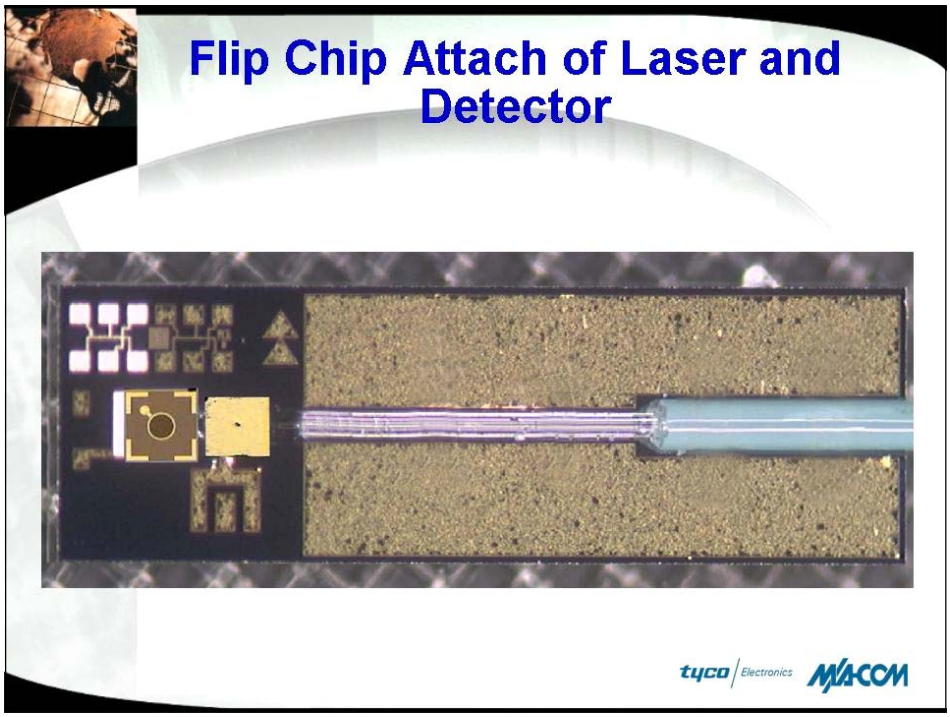

Figure 26: Example of a laser with back facet diode passively attached to silicon bench
(Courtesy of J. Goodrich, Tyco Electronics – OIDA Nitride LED Forum, May 2006)

Several companies have developed complex flip chip bonding machines that provide high accuracy placement. Two of the principal companies involved in this are Suss MicroTec and Toray Engineering. The placement accuracy of these machines is sub-micron. Intensive engineering of the alignment head and solder re-flow stages can provide a consistent placement tolerance of +/- 0.5 um, well within the 3 um window for coupling optical fiber to a single mode emitting device.

Optical bench technology is currently employed by several companies for the production of FTTH modules. The integration of spot-size converter die and silica waveguides provides simple integration of both diplexer and triplexer functions.

To provide a low cost hybrid approach, we would like to remove complex alignment and die bonding. One potential approach is passive realignment using solders. Several companies, including Tyco Electronics and the Heinrich Hertz Institute, have investigated this approach. The implementation in actual product shipping today has not been realized. The principle of realignment has been developed using a DAP sealer. The realignment has been shown to allow up to 20 microns of offset and still achieve realignment to within 1 um accuracy. This batch process is still an assembly process and not a wafer process.

To move to a wafer scale production, an integrated light source is required. Several approaches are currently under investigation within the industry and are reviewed next.

8 Silicon light emission

There are several approaches to provide light emission on a silicon wafer. There is the traditional approach that is based on die bonding devices to a silicon bench and those that are attempting to provide compatibility with a standard CMOS fabrication process. The next few sections highlight the alternative hybrid wafer processing research.

8.1 Wafer bonding

The concept of wafer bonding of semiconductor material is not new. It has been successfully employed in the LED industry for several years. During the 1990s when investigating long wavelength VCSEL technology, several companies pursued it as an approach to provide longer wavelength emission by fusing GaAs mirror structures to InP active regions. The preferred and most successful approach today is based on epitaxial growth. The introduction of nitrogen into the III-V material, i.e., InGAsN on GaAs, provides a low defect material which is highly reproducible. One company is today commercially shipping this type of device.

One of the distinct problems with light emission in a silicon structure is providing the photons through an electrical pumping scheme. One successful approach being pursued by researchers is to use III-V material as a photon source. The basic principle is to wafer bond an InP laser structure to the silicon surface and provide electrical contacts that inject the current to generate spontaneous emission. The laser cavity can then be formed either in the silicon or in the III-V material. Figure 27 highlights a promising approach being pursued at UCSB.

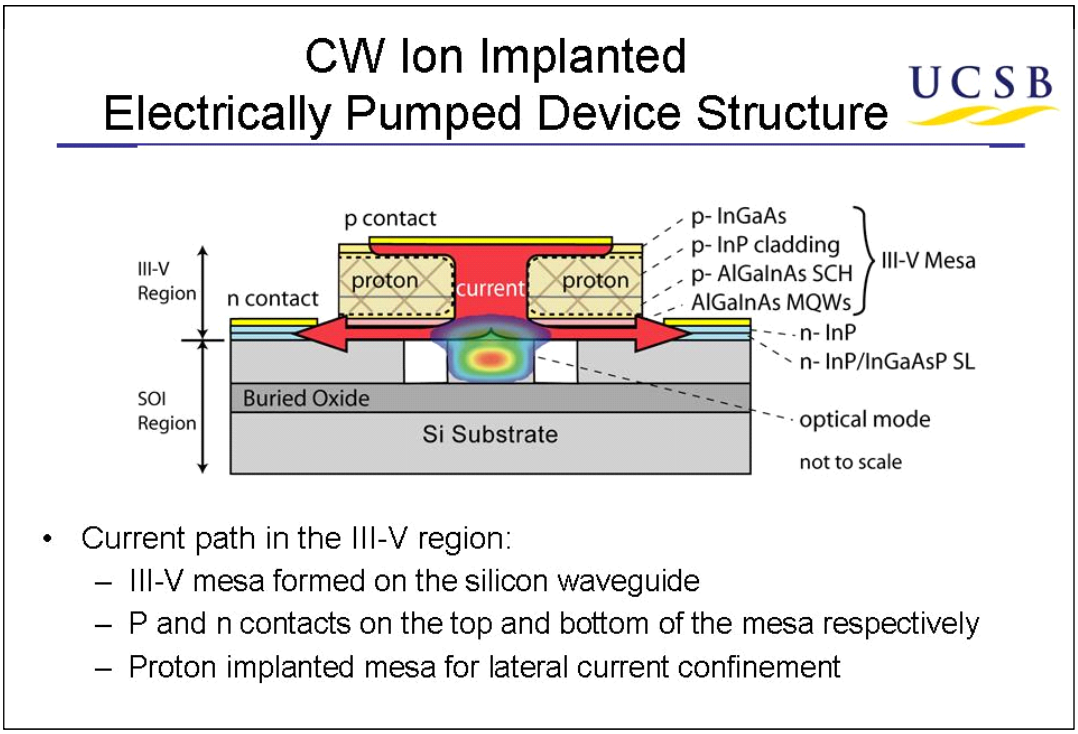

Figure 27: Wafer bonded InP silicon hybrid laser structure

(Courtesy of J. Bowers, UCSB)

The InGaAlAs multiple quantum well laser structure is wafer bonded to the surface of the silicon wafer. A laser cavity is formed between the InGaAlAs light emitting region and the silicon resonator. One of the key engineering requirements in this approach is optimizing the optical overlap of the photon-generating material with the silicon laser cavity to increase the optical gain. The optical mode essentially couples forward and backward through the quantum well, but the must use the silicon waveguide to provide the optical cavity and mirrors.

The basic laser equation for a cavity is approximated as:

$$\Gamma g = \alpha_m + \alpha_i$$

For a simple cavity with two reflecting facets, the mirrors have an associated loss defined by:

$$\alpha_m = 1/2L \ln (1/ r_1.r_2)$$

where L is the cavity length, r_1 and r_2 are the respective facet reflectivity, and α_m is the mirror loss.

In the silicon resonator, we need to increase the mirror reflectivity to reduce the cavity loss and increase the optical confinement factor (Γ). Both of these two factors lead to lower round trip gain, lower carrier density, and hence lower threshold carrier density.

The silicon waveguide approach must be balanced to achieve high gain, yet allow power out of the waveguide mirror. We must therefore balance the overlap integral of the photon generator section with the feedback from the cavity (Figure 28). The optical laser confinement factor (Γ) needs to provide enough threshold gain to achieve lasing action, but still provide output in to the optical waveguide.

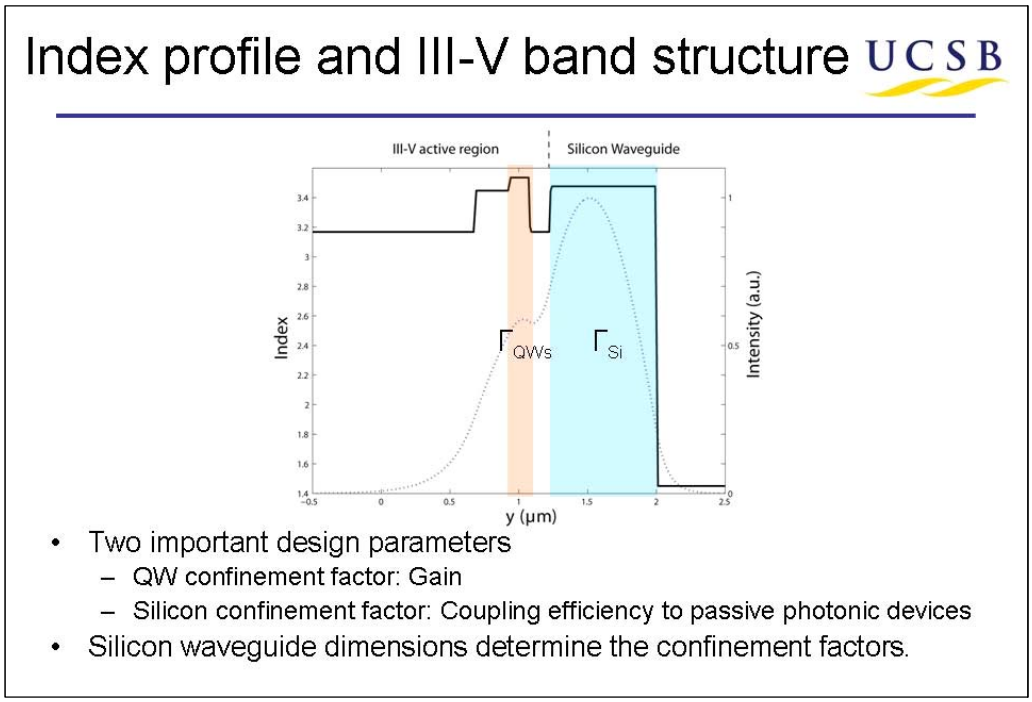

Figure 28: Index and optical waveguide overlap with the gain medium
(Courtesy of J. Bowers, UCSB)

Alternative designs using the same wafer bonding principle are being pursued today. The light generating material can be formed into different resonant cavity structures, which provide roundtrip gain. An example is the microdisc laser being developed under the Picmos program in Europe (Figure 29). The microdisc laser provides a smaller light output at much lower threshold currents than the linear resonator device. The microdisc laser has a very small active volume. This leads to lower values of the threshold current and light output power compared to the linear resonator device. The disadvantage is the increased carrier density in the active region of the device.

For example, the threshold current of the UCSB linear resonator approach is approximately 65mA, compared to 500uA for a disc laser. The basic equation for the threshold current is:

$$I_{th} = eN_{th}V/\tau_e + I_L + I_{Auger} + I_{IVBA}$$

where e= electronic charge, V= volume of the active, te is the carrier lifetime and I_L is a leakage current , I_{Auger} is the auger current, and I_{IVBA} is the IVBA current.

As the volume decreases, I_{th} decreases, but the N_{th} component increases due to the higher losses.

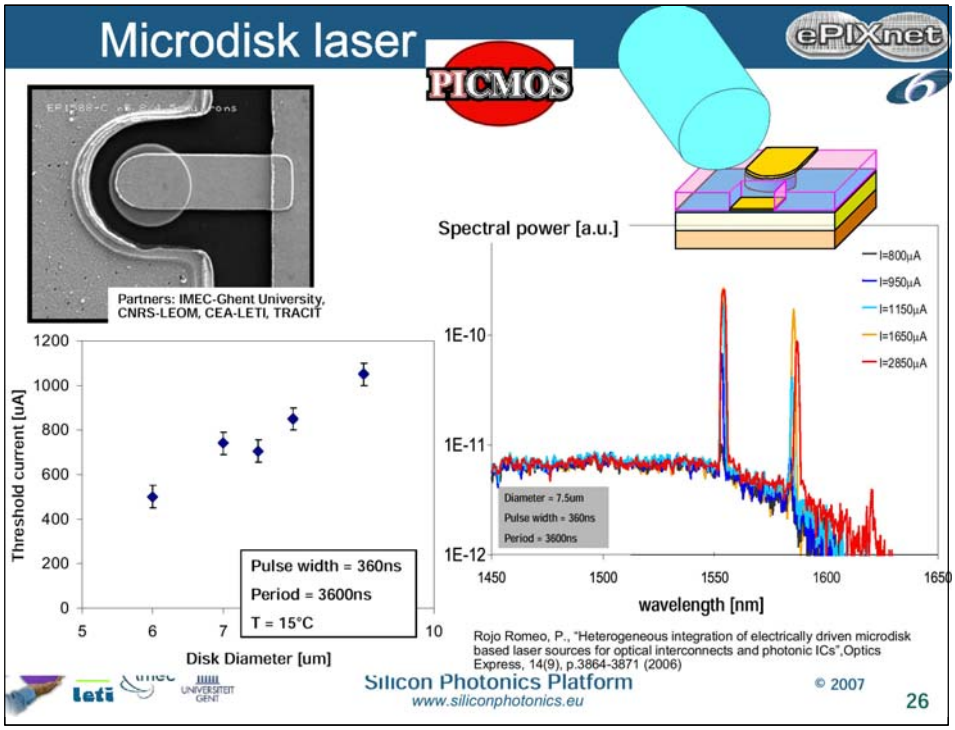

Figure 29: Microdisc laser structure formed by wafer bonding III-V die to silicon wafer
(Courtesy of P. Dumon, IMEC)

The impact of the carrier density and internal heating are easily seen in the linear resonator device. It has a larger active volume and lower carrier density than the micro-disc laser. The current demonstrated devices suffer from a low optical confinement factor for the MQW active region. This leads to higher carrier density. The UCSB device utilizes an InGaAlAs active region, which is currently believed to have a smaller temperature dependence than an equivalent InGaAsP active region. A standard approach for measuring the temperature dependence of a laser is to measure its T_o. In basic laser theory, the T_o is defined by the equation:

$$Jth\ (T_2) = Jth\ (T_1)\ .\ Exp\ ((T_2-T_1)/T_o)$$

In the communications industry, there several types of laser design. The basic approaches remain either ridge waveguide or buried heterostructure. The structure actually impacts the measured value of To, due to the optical confinement, carrier density, and leakage currents. It has been shown that moving to the InGaAlAs material system, the To can be increased to 70 Kelvin. This compares to 40 to 50 Kelvin for InGaAsP laser devices.

The impact of the higher losses in the silicon resonator waveguide increases the gain to enable laser operation. This raises the effective temperature of the electron gas in the active region, which can lead to thermal runaway issues as seen in Figure 30.

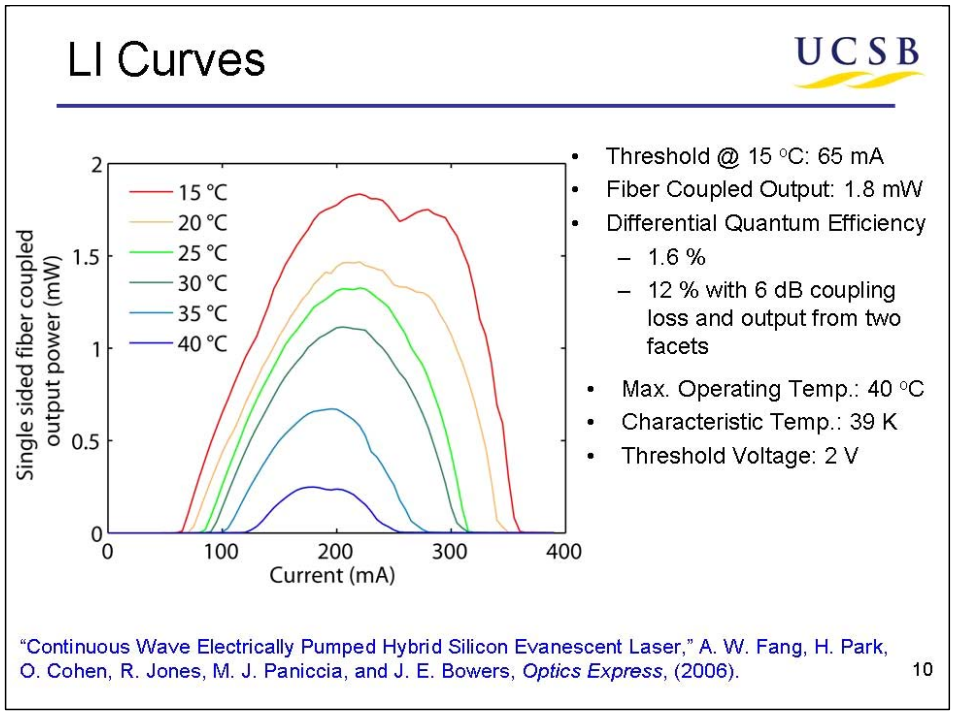

Figure 30: Light-current curves for a linear resonator using a silicon evanescent laser
(Courtesy of J. Bowers, UCSB)

For the linear cavity approach, the reported differential quantum efficiency is currently low. The measured characteristic temperature (T_o), is lower than would be expected with the InGaAlAs system indicating several issues could be combining to produce the current performance. Further design optimization and process development are required to meet threshold currents seen in standard 1310 nm material for communication lasers.

Both the microdisc and linear silicon resonator provide a DC source of light integrated into the silicon wafer. As this technology develops, several questions will need to be addressed as the technology matures, including the application requirements, reliability, device specifications, and power budgets.

8.2 Epitaxial growth and rare earths

The incorporation of rare earth atoms to generate light is an alternative that has distinct potential. If we look at optical communications, using atomic doping in glass has found real success in erbium-doped fiber amplifiers. These are mainstream products that are reliable and found in most telecommunication networks today. By optically stimulating the atomic levels of the atoms in the glass or silicon medium, light emission energy can be added to the traveling wave. Several researchers studying light emission in silicon utilize erbium to grow or dope the optical cavity. The advantages of erbium are compatibility with current wavelengths used in communication systems and the well understood properties of the atomic transitions.

Epitaxial growth of erbium oxide on the silicon is one route being pursued. Essentially, it places a light generating medium within two slabs of silicon (Figure 31).

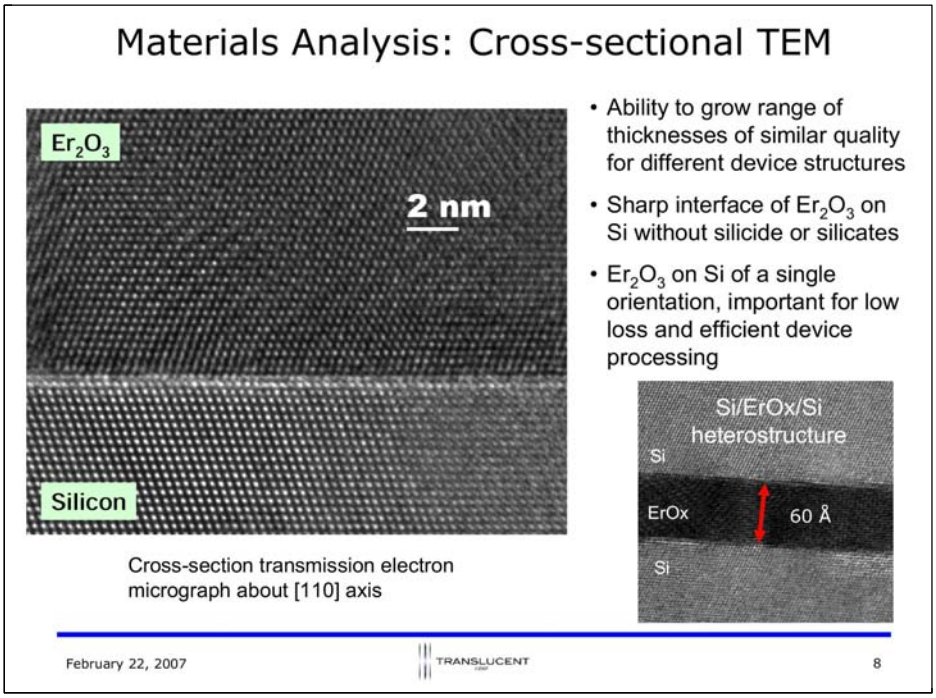

Figure 31: TEM cross section of epitaxial grown erbium oxide layer on silicon
(Courtesy of V. Sabnis, Translucent)

The basic idea would be to generate a p-n junction where n-type and p-type silicon provides the electrical carriers for the erbium oxide. How the electronic bands align and how to achieve significant electrical confinement are currently areas under investigation. Today, atomic luminescence of the erbium oxide layer has been observed at room temperature. This has been demonstrated by both photoluminescence characterization and electroluminescence. Further work on the materials is required to understand the electrical to optical efficiency and whether this can be incorporated into a standard silicon fabrication line.

8.3 Silicon nanocrystals

The ultimate goal of silicon would be to generate light emission without providing hybrid integration of III-V material or implanting or growing atomic level transition material. The major challenge is to engineer the band structure and overcome the indirect band gap of silicon.

One potential solution to achieve this is to use silicon nanocrystals. The basic idea is to form a silicon core inside an amorphous silicon oxide shell (Figure 32). The nanoparticles' properties are determined by both their size and the concentration of silicon oxide shell surrounding the nanoparticle. The idea is that the silicon oxygen bonds create addi-

tional energy states within the band structure of the material. The formation of the nanoparticle also localizes the excitation to the silicon nanocrystal surface.

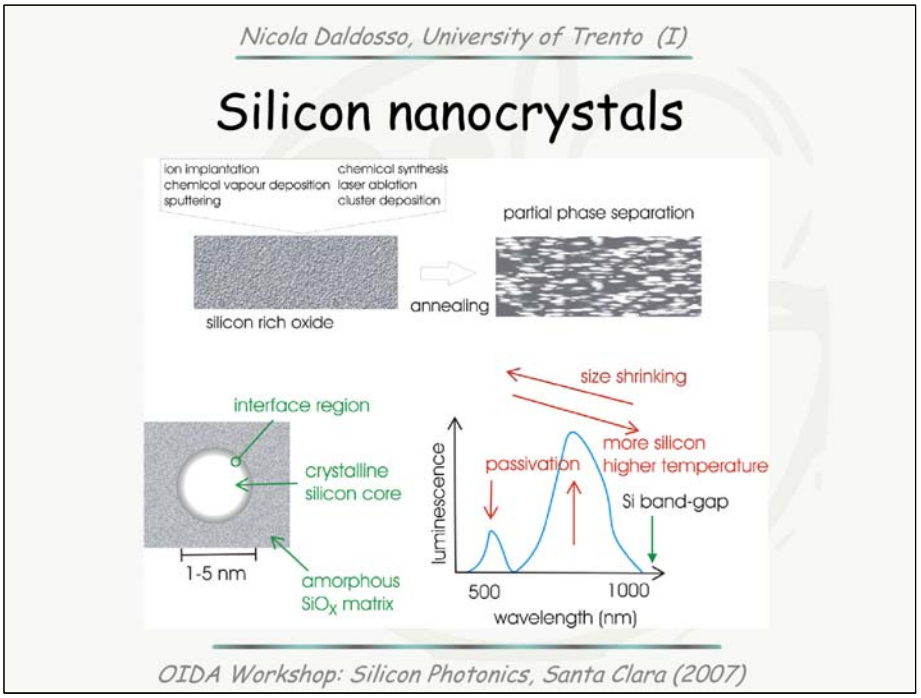

Figure 32: Formation of a silicon nanocrystal and the energy luminescence observed
(Courtesy of N. Daldosso, University of Trento)

As the nanocrystal can emit light and provide some form of optical gain, researchers developing this approach began looking at electrical injection of the nanoparticle to achieve light emission. By assuming that the band gap difference and oxygen states provide a 4 level system, the idea was to use tunneling to inject electrons and produce recombination. Fundamentally, this has been observed, but at a low conversion efficiency of around 1%.

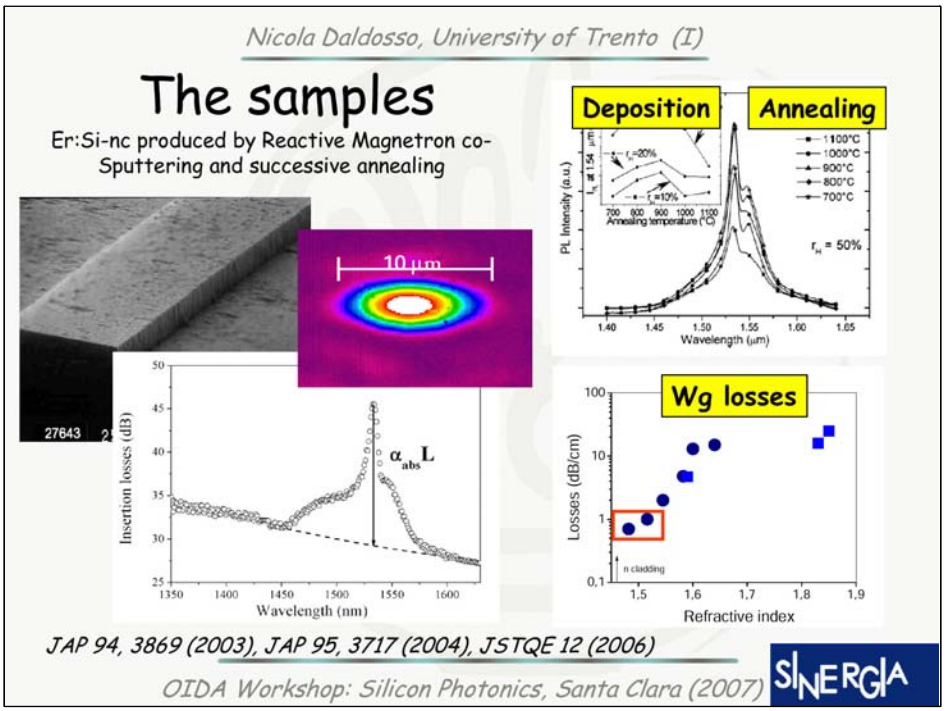

Figure 33: Formation of an erbium silicon nanocrystal and the energy luminescence observed

(Courtesy of N. Daldosso, University of Trento)

The goal of achieving true silicon light emission continues to follow a path of providing an atomic dopant as the light emitter (Figure 33). Essentially, the silicon is being used as an injection tool for the atoms. The tricks used to provide a direct band gap do not have strong enough dipole moments to form lasing action currently on their own. Further work in this area could eventually lead to silicon light emission. The question is whether or not it can be pursued to the level required within the industry today.

8.4 Status of current performance

A comparison of the different hybrid silicon photonic lasers was presented at the workshop by UCSB. Their summary is highlighted in Table 11.

Laser Type	Wavelength	Threshold	Output power	Cavity length	Comments
Monolithic integrated Raman silicon laser [1]	1686 nm	200 mW	30 mW	30 mm	CW optically pumped Raman laser, Room temperature operation
Periodic nano-patterned crystalline silicon laser [2]	1278 nm	12 W cm^{-2}	30 nW	1 mm	CW Optically pumped band-to-band emission 70K > operating temperature
InP/InGaAsP laser coupled to silicon waveguides [5]	1550 nm	180 mA	0.9 mW	.5 mm	Pulsed electrically pumped InP laser Fabry-Perot laser bonded to BCB on SOI, coupled with inverted taper.
Hybrid silicon evanescent laser [4]	1577 nm	65 mA	1.8 mW single fiber coupled 14.4 mW total	.8 mm	CW electrically pumped operation up to 40 C. Hybrid mode lies predominantly in silicon

Table 11: Comparison of different lasers presented at the workshop (neglecting die bonded devices)

(Courtesy of J. Bowers, UCSB)

When we look at the current devices in production in communications, threshold currents are on the order of a few milli-Amps and output power is on the order of several milli-Watts. This summary chart highlights the current infancy of the technology.

8.5 What about reliability?

One of the key requirements of any electronic or photonic system is reliability. In the communications market, the data rates increase and the costs decrease but the reliability is expected to remain constant. If we look at pump lasers or VCSELs, the median life expectancy at high temperatures is several years. For network applications, typically the 1% failure rate has to be greater than 7 years. For telecommunications applications, the service life expectancy is 25 years. In reality, the median life of typical telecom lasers is greater than 25 years.

Reliability and failure modes of optical components are understood today. As we look at the computer and server applications, the drivers are costs and volume. Two principal concerns are thermal effects and reliability. If we compare processors in production today, the heat generated by the transistors within the microprocessor has increased to the point where multicore has been adopted to reduce the thermal impacts. If we look at the application space for silicon photonics, we need to understand the environment and the reliability constraints. As we have discussed, the III-V material based on InP has distinct temperature issues that have been studied for more than 25 years. These are understood and designs for high power or high temperature operation are based on reducing these loss mechanisms. Complex 2-D and 3-D models of the laser component can be generated to optimize performance or modulation performance. The silicon photonic devices can leverage this understanding and modeling capability. The application will provide several distinct questions that need to be answered by the transmitter and receiver designer.

Should the reliability be based on communication specifications or electronic IC specifications? It is too early to ask these questions. If the optical integration is to proceed, reliability will be an important area as the integration of emitters and receivers is buried into the IC. This will be a challenging area for silicon photonics.

9 Economics for silicon photonics

The economics for the implementation of improved I/O connections is dependent on the health of the supply chain and the technology investment. It is important to understand both the needs of the end user and the capabilities of the current suppliers. Silicon photonics is in production today in many different industries and commercial segments. The actual type of silicon photonics we have been concentrating on is interconnects for the computer industry. This technology is still in the early stages of development. Products which integrate IC technology with optical devices are not novel or new. Parallel transceivers used in server applications utilize the same principles, i.e., VCSEL or photodiode devices die bonded to silicon IC technology. The economics for the server market require improved cost points compared to commercial devices available today. As we look at interconnects technology, there are several economic points that need to be considered.

Historically, the fiber optic and copper interconnects/cable markets have grown as communication demands increase. These links are either in the core, metro, access, or data center. The communications market has always assumed that fiber will increase in deployment as the data rate increases. Fiber optic components offer several advantages over copper cable solutions at higher data rates. As new standards and data rates have been released, we see that fiber cable and optic devices have found it difficult to displace copper solutions. Each time the optics community feels that it will gain improved share, the electrical community provides a new or better solution. For example, at 10 Gbit Ethernet, it was believed that a copper solution could not be achieved. Yet a 10 Gbit base-T standard has been developed and 100 Gbit Ethernet copper cable solutions have been proposed in the current IEEE HSSG study group. As we look at the relative health of the companies supplying these products, the copper connector and cable assembly companies are profitable, yet the fiber optic component companies remain unprofitable or are just beginning to cover their operating costs. This disparity plays into the economic challenges for high speed I/O and silicon photonics development.

The component vendors are unable to invest heavily in new technology and fail to see any advantages of traditional silicon optical bench technology. Several companies in the communications field have deployed silicon optical bench solutions or invested in passive alignment technology. Equipment manufacturers have developed die bonders with placement tolerances of +/- 0.3 um to enable III-V laser diodes to be attached directly to silicon components. The impact has been to move the cost of manufacture from one process step to the next. If we examine most components in mass production today in the communications field, active alignment is still “king.” Only in the FTTH market has there been potentially some advantage in moving to PLC technology. When we examine the computing and data center markets, the cost targets are very aggressive. This can directly impact the roadmap for fiber optic interconnects and number of companies willing to invest in the new versions of silicon photonics. A paradigm shift to a mass volume market must be enabled and driven from within the computer industry. The computer industry cannot rely on the communications companies to invest in technology where

return on investment (ROI) cannot be achieved within a two-year timeframe. This is a key issue in the economic argument today.

During the recent 100 Gbit Ethernet Workshop held in August 2006 by OIDA, it was observed by several companies that there is a real need to increase the I/O connection speed. This is becoming increasingly important in the high performance computer (HPC) market. Fiber optic deployment has occurred here mainly through the introduction of ribbon fiber and parallel transceiver technology. As optics penetrates the HPC market, it will migrate to the mid-range and low-end servers as component costs decrease. One of the key requirements to ensure successful deployment is cost. The estimated cost requirement per bit of transmitted data for the HPC environment is distance driven (Figure 34).

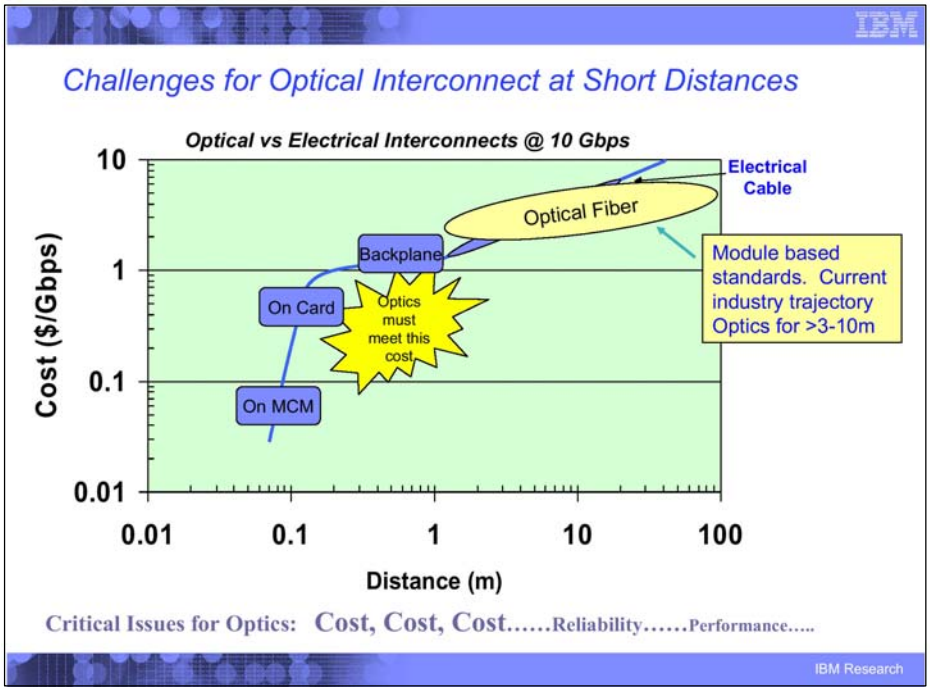

Figure 34: Distance vs. the cost per bit of transmitted data
(Courtesy of P. Pepeljugoski, IBM – OIDA 100 Gbit Ethernet Forum)

The question of how to achieve this with today's optical module technology is challenging. The cost of the modules, the optical sub-components, and the market volume play a significant role in the economics and ROI debate. The current cost of a 1 Gbit short reach (SR) optical module is nearly equivalent to the price of Cat5e cable a consumer can buy from Staples, i.e., $20 to $30 U.S. dollars. For the 10 Gbit/s duplex modules, the price is an order of magnitude larger and currently in the $300 range or above. Whether current switch vendors actually need the cost to be < $30 is questionable considering the captive market they have achieved by implementing digital diagnostics within their suppliers transceiver modules. As the data rate increases, the development of next generation modules has an even less attractive business case. Currently the forecast for a 100 Gbit

Ethernet transceiver for the Ethernet switch market is < 100,000 units in 2010. If the target cost is 2.5 times the current 10 Gbit Ethernet module cost, it equates to a sales prices of only $750. This essentially states the market is nominally around a $75M market. This is a relatively small market compared to the server market. Return on investment is an important question in communications. To examine the economic of current technology and the implications for silicon photonics, we should look at the current modules used today.

9.1 Today's transceivers

The cost of a duplex transceiver has seen incredible price erosion over the last 10 years. As new modules have been introduced, the price premium for each new introduction has been eroded. The price expectation is dependent on the market segment. For example, the expected price for the 40 Gbit transponder is about 2 to 2.5 times the 10 G transponder price. Meanwhile, the price for a 4.25 Gbit Fibre Channel transceiver is expected to be equivalent to the 2.125 Gbit Fibre Channel transceiver. The problem with this expectation is that the current transceiver vendors are struggling to obtain profitability. With no premium for new module introduction, there is very little money available to develop new transmitter and receiver technologies to enable the next generation of components. An example of the price erosion based on the cost per Mb/s per linear inch of face plate was presented at the OIDA micropackaging workshop (Figure 35).

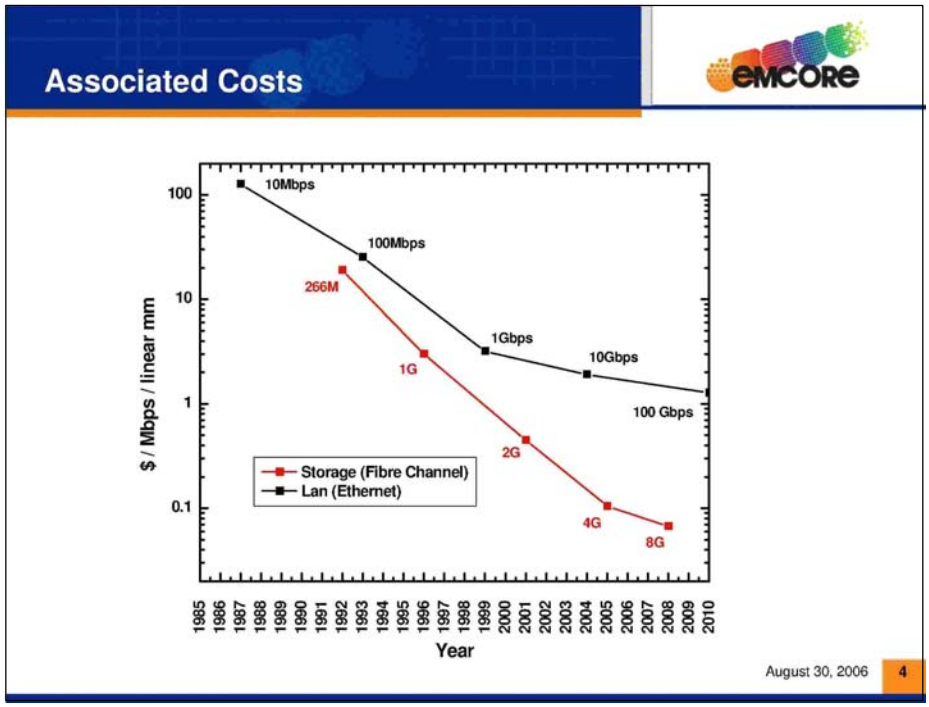

Figure 35: Price erosion for Ethernet and Fibre Channel

(Courtesy of K. Jackson, EMCORE)

The Fibre Channel market is fortunate in that most of the investment in 10 Gbit and 40 Gbit technology occurred during the 1990s and prior to the optical bubble bursting. As we move to higher data rates, the fundamental technology that was developed through the 1990s has not seen any radical change. Hermitic packages are preferred and TO cans remain a significant volume runner. The development of VCSEL technology has had a huge impact in the storage market, but long wavelength VCSEL technology has struggled to break ground. The promise of ubiquitous low-cost 1310 nm VCSEL technology is currently competing with low cost Fabry Perot (FP) and distributed feed back (DFB) laser technology. As the data rate requirements have increased, DFB and FP infrastructure, production, and yields have improved to enable lower manufacturing costs. As we move to high data rates above 10 Gbit/s, the external (lithium niobate) or internal (electro-absorption) modulator technology is used. For the enterprise and telecom markets, the fiber non-linearity and impairments make the standard NRZ serial solution unattractive for 40 Gbit/s long reach applications. Additionally, electronic driver technology is more expensive and large voltage swings are required. At lower data rates, low voltage swings and inexpensive IC technology provide a cost argument to implement parallel links over serial type solutions.

For current optical duplex transceivers, the construction and devices inside the 'box' provide significant cost challenges to meet a $/Gbit metric. There are several factors that make this difficult. These include the module construction, type of semiconductor device and manufacturing location. If we look at a duplex transceiver the basic components are not complicated (Figure 36).

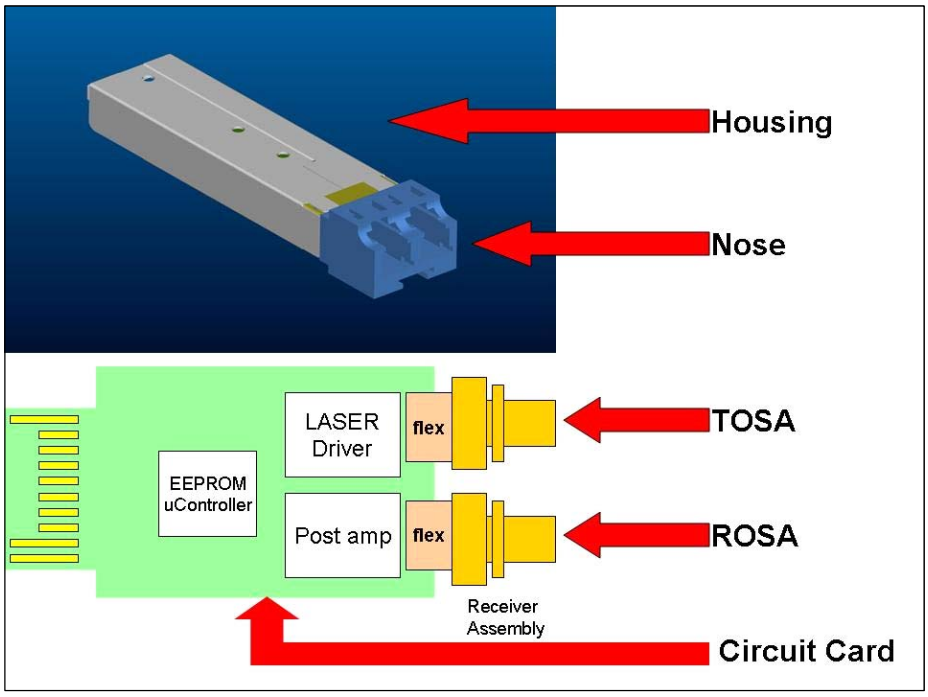

Figure 36: Basic components of a SFP transceiver
(Courtesy of W. Ring, WSR-ODS)

The cost of a transceiver can be broken down into several levels. At the macro level, the basic components are the electrical and optical sub-assemblies that are soldered together and put into the casing. The sub-components, i.e., transmitter optical sub assembly (TOSA) and receiver optical sub assembly (ROSA), are a large percentage of the cost in 1 Gb/s modules. At higher data rates, conversely the electronics are a larger part of the cost breakdown. This is one of the reasons that the SFP+ module is being developed.

With advances in semiconductor packaging and technology, alternative packaging and assembly are available to the transceiver manufacturers. Principally, they could leverage the technology utilized in LED packaging or IC manufacturing to reduce costs. LED packaging today utilizes lead frames with high thermal dissipation. To move to lead frame packaging requires development of non-hermetic VCSELs and laser/photodiode devices. A non-hermetic environment can drastically increase the infant mortality rate of active optical semiconductor devices. This would necessitate moving to several of the techniques initially adopted in the silicon industry.

9.2 Silicon photonics – is there a cost advantage?

When we look at the role of silicon photonics in the communications industry, the following have traditionally been discussed as the principal reasons for investment:

Passive alignment
Hybrid integration
On wafer die bond and burn-in
On wafer testing
Automation
Monolithic integration
Low cost

The question that governs many business decisions today is, “How do we achieve a low cost solution?” In the early 1990s, the concept of passive alignment technology was the key driver for cost reduction. Unfortunately this is not the complete argument. Fiber handling, optical coupling, wafer testing, and burn-in are other concerns that must be addressed.

Several different questions must be addressed to realize the low cost concept using silicon photonics:

What is the application?
Does the connection technology exist?
Is wafer scale processing achievable?
How do we package it?
Is there a volume application?
What about standards?
Can we do this at a foundry?
Are there standard design tools?

As we highlighted in the first few sections of the report, the drivers for the silicon industry are different to the traditional III-V semiconductor community involved in communications. Communications is a low volume market compared to the storage/DVD/CD laser market and even the electronic connector market. To achieve a low cost point, we need volume drivers and semiconductor processing as key elements. Integration is a great concept but it does not stand as a business case alone.

To achieve a major advantage over III-V devices and transceiver modules, silicon photonics must be able to present an integrated photonics IC that can be easily packaged in a low cost plastic platform. The optical connection must be repeatable with a simple physical interconnection.

9.3 Dilemma with the economics for optical component implementations

For optical interconnects to become more ubiquitous in the computing arena, there are several challenges for the optical industry including:

a) Cost
b) Performance
c) Reliability
d) Size
e) Thermal dissipation
f) Interconnection interface

A primary target for optical component implementation continues to be cost. Several companies from the computer and server markets stated that the target should be:

a) Board-to-board $1/Gbit
b) Chip-to-chip $0.25/Gbit
c) Intra-chip: <$0.01/Gbit

The current parallel optic transceiver manufacturers state that perhaps $4/Gbit is achievable today. The prices are aggressive for current technology and packaging approaches. In addition, testing is seen as a major obstacle. Alternative schemes such as those being pursued using silicon photonics or integrated III-V OEIC may be able to meet these targets, but will require intensive investment.

The server architecture today is not designed for optical interconnects. This needs to change for optics to make progress deeper in to the servers. The debate of the economics of a copper cable solution vs. a fiber optic solution is multi-faceted. It will continue to progress but slowly, as both economic factors change and technology advances.

The next section is a review of the input from the breakout session discussions.

10 Breakout session discussions

There were three breakout discussions held after the presentations. The working groups were given three key questions to debate and discuss. The objective was to raise concerns and provide insight into the topics reviewed. The three questions that were raised to the groups were:

1. What are the commercial and industry challenges for development and deployment of silicon photonics? What is the direction of silicon photonics and Group V devices?

2. What are the issues surrounding light generation and photonic transmitters in silicon? What is the best technology approach to solve this?

3. Does silicon photonics offer the best route to all optical processing and on chip optical communication? Is there an advantage over other photonics circuit material systems and approaches?

Each session produced several different outputs. The following sections offer a summary of the information that was produced.

Session 1: 'What are the commercial and industry challenges for development and deployment of silicon photonics? What is the direction of silicon photonics and Group V devices?'

When the group looked at this question, there were multiple opinions presented. The first question the group asked was 'What is the eco system?'

When we look at the implementation of silicon photonics, it is apparent that there are no standard interconnect packages on the board level. This is an issue for how silicon photonics can move forward. To enable the standard silicon package using optics, it was suggested that we need an optical equivalent of FR-4. How should this be handled? Do we need the involvement of IPC or NEMI?

To enable the silicon photonic implementation, is there a volume market that can be utilized?

The group suggested that the server market is the driver and that the market already exists.

The issue is that VCSEL technology is the solution currently being utilized. This may drive more optical interconnect technology interest, but the current company efforts are on high performance. There is no intermediate solution that is being addressed.

From an industry perspective, there is less vertical integration in the community today (e.g., Bell Labs). The industry for optics is fragmented. The government through DARPA invested heavily in Terabus and parallel optics to enable optics for computers. The forecast bandwidth demand was expected to drive optical technology innovation. The prob-

lem seems to be cost and standard device driven. Without a well defined commodity standard product the eco-system did not exist for implementation and the computer industry has stuck with the existing infrastructure.

The group then asked the question whether III-V photonics is preferred to silicon. When this question was posed, it was stated that the silicon photonics community is still too young and has not worked long enough with systems people. It was recognized that hybrid silicon photonic approaches increased test requirements and therefore cost. Some thoughts included the fact that the optical interconnect industry is very insular except for the telecommunications industry.

To enable silicon photonic proliferation is was suggested that there needs to be a computer optics alliance. Perhaps OIDA could initiate this consortium. The concern was that the consortium would require opposing views and need input from computer architects to understand the requirements. By including the computer architects, it would highlight the bottlenecks and concerns for optics that traditional device and module designers might not be aware of. It was suggested that optical component companies attend computer conferences. The silicon industry is not a radical industry so optical companies need to understand this and start with low tech approaches. The main issue the group realized with this suggestion is that the main optical component companies would need to investment heavily in this area. Several member of the group suggested that the optical component industry remains too fragmented even in its traditional existing markets. Several members of the group suggested that standard for computer optical interconnects would be needed.

Session 2: 'What are the issues surrounding light generation and photonic transmitters in silicon? What is the best technology approach to solve this?'

The group discussed the aspects of current state of the art silicon photonics and the issues moving forward. Initially, several metrics were raised as potential items that need to be discussed, including 'Do we need the wall plug efficiency of silicon based light emitter to reach 100%? Is this answer market and application driven?'

When reviewing the title, i.e., silicon photonics, it was discussed that the used of silicon in optics is not new. In fact, Lucent Technologies commercialized it in the 1990s as part of the LASER2000 product family. Several members of the group highlighted that the growth of silicon photonics was volume and cost driven. The main concern being that silicon photonics has application outside of computing and server interconnects, i.e., silicon photonic solutions are application dependent.

As we discussed, the light emission issue for silicon it was raised that perhaps LED like operation would be sufficient. For several sensing applications this seemed relevant. For on-board interconnects and inter-chip interconnects, perhaps laser transmission is preferred due to the high data rate requirements that are forecast.

Several of the key requirements imposed on a silicon photonic platform were discussed. The principal constraints agreed upon were:

a. Electrically pumped sources
b. CMOS compatible sources
c. High temperature operation of the sources

There are several different approaches to enable light emission in silicon. The following were highlighted:

a. Rare earths
b. Silicon nanocrystals
c. Hybrid silicon devices
    - Wafer bonded light emitters
    - Die bonded light emitters
    - Epitaxial grown light emitters

In an effort to gauge the relative merits of each technology approach, it was decided to rate the likely success and relative maturity. As part of this process, a discussion on the merits of each approach was discussed. The rating of each technology is highlighted in Table 12.

Technology	**Maturity** (Ranked)	**Likelihood of success** (5= high, 3 Average, 1= Low)
a. Rare Earths	5	3
b. Silicon Nano-crystals	4	1
c. Hybrid Silicon Devices		
Wafer Bonded light emitters	2	5
Die bonded light emitters	1	5
Epitaxial grown light emitters	3	5

Table 12: Relative merits of each technology approach as rated by the working group

Session 3: 'Does silicon photonics offer the best route to all optical processing and on chip optical communication? Is there an advantage over other photonics circuit material systems and approaches?'

The group suggested that the current market for communications is small in terms of volume. The ITRS roadmap suggested that optical devices for routing will be required.

It was suggested that silicon photonics has a larger market not directly related to computer interconnects.

In effect, the question remained unanswered as silicon photonics is too immature to address this question at this point in time.

11 Roadmaps

One of the objectives of the OIDA forum was to draw conclusions and develop a path forward for review with the industry, i.e., a roadmap. Several organizations develop roadmaps in technology to provide potential paths forward. The computer industry has been following Moore's law for microprocessors and as the dimensions become smaller, new effects and roadblocks appear. The ITRS regularly reviews the current trend in IC semiconductor nodes and development of new technology. As we have observed, the silicon industry has adopted new approaches to resolve signaling across chips and to improve signal integrity. We have seen the implementation of copper and low k dielectrics. As signaling requirements increase, 3-D stacking and silicon VIA technology to local memory chips has been developed. These methods continuously improve the performance of copper interconnects within chips and delay the implementation of O-E front ends at the output pins of the IC.

As we look forward, the microprocessor industry continues to advance and enable new applications. It is expected that terabit instructions per seconds will enable a new host of applications. The timeframe for this is the next 10 to 15 years. Figure 37 highlights the development objectives and potential applications moving forward.

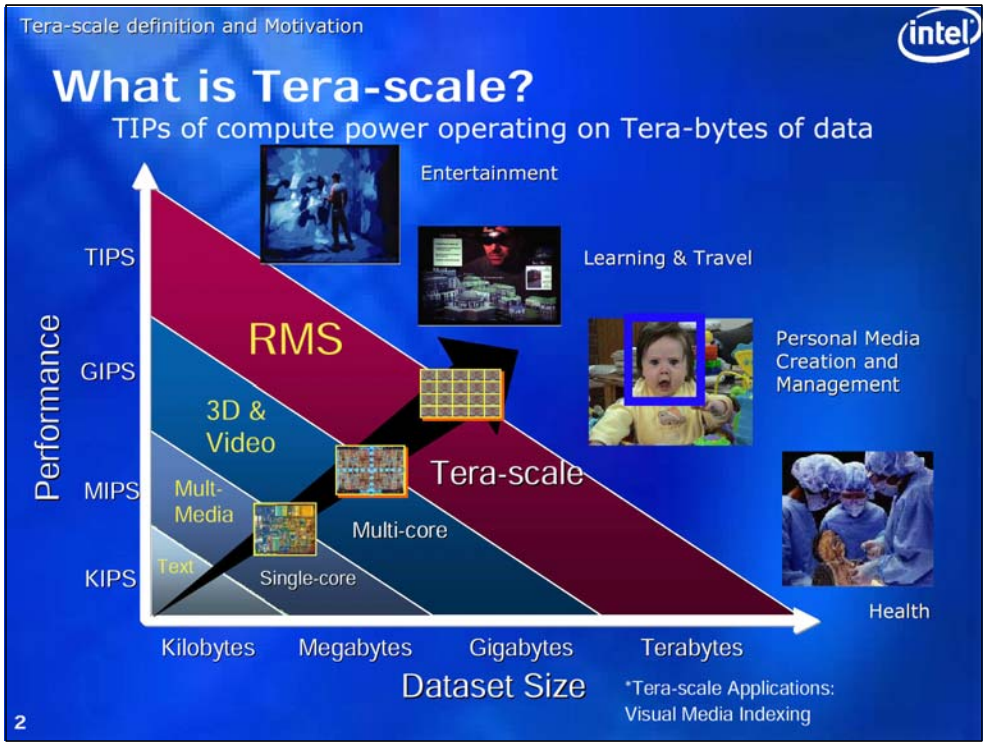

Figure 37: Integration of memory methodologies being pursued today

(Courtesy of J. Bautista, Intel)

As the industry pushes forward to multi-core processing and ‘tera-scale’ architectures in the future, both the parallel interconnection using copper and fiber need continued research effort.

Today, we are seeing several developments within the industry in optical communications. The reversal of OTN vs. Ethernet leadership in data rate is occurring as carriers are aligning their transport protocols to carrier class Ethernet.

As we look forward to the next generation of devices, components and technology, the economics of the industry directly impact the future development paths. Optical development of on-chip optical interconnects are expected to be delayed as silicon photonics is still immature and will require further development.

When we look at the future expectations the data rate is expected to increase and several bottlenecks currently occurring need to be resolved. The current report from iNEMI in 2007 suggests that optical component technology is too immature to provide optical interconnects even by 2017. For optical interconnects to impact board to board connections, the implementation of the optical back plane will need to overcome alternative lower cost technology options. It is expected optical back planes will be required for HPC environments.

From the meeting we can gather a few important points. Optical technology needs to drive to lower cost and be compatible with the silicon industry process to enable introduction in a co-packaged fashion. The E-O conversion needs to be low power and low cost. Based on the discussions at the forum we expect to see a push for high aggregate bandwidth either through a silicon photonic platform or a III-V semiconductor platform. Figure 38 highlights roadmap several expectations drawn from the OIDA meeting on optical interconnects that are relevant for silicon photonic development.

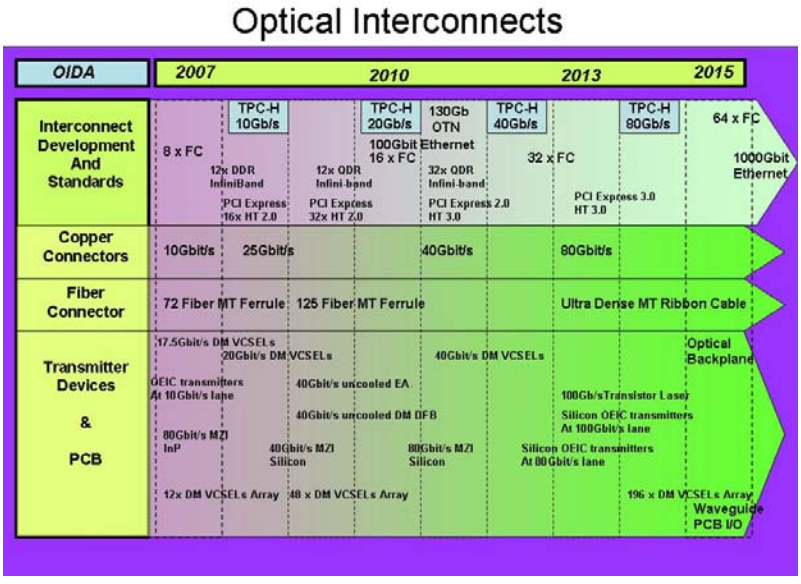

Figure 38: Evolution of optical components required for optical interconnects

One of the key issues moving forward with integration of photonic components is the lack of design rules and base technology platforms. In the silicon electronics arena the foundry model is well established. Many companies operate on a fables basis, their key advantage being in the design and integration into systems. The current III-V community has several foundry companies that exist today. The companies compete rather than provide platforms of common functionality. For silicon photonics and InP photonic integration to occur, a shift to a more fables model based on platform technology is essential. The formation of an Optical Foundry Consortium is inevitable as the pressure to develop cost effective volume integrated photonics solutions develop. This has started in Europe under the ePIXnet program.

12 Recommendations

Fiber optics offer clear advantages as we move to higher data rates within the computer industry. The question on how this is best resolved will require industry collaboration and greater interaction of the traditional optical community with the silicon semiconductor industry association. The silicon industry will need to address their interconnect roadblocks on the horizon, by providing a change in the architecture from electrical to optical. Today, several approaches are being developed to address this issue. In the following section we will provide some recommendations that are a result of the discussions at the meeting. The recommendations are a synopsis of several of the debates held during the breakout session.

- The server companies need to provide clear guidance on their fiber optic and optical circuit card technology requirements if they wish to enable adoption within the next 10 years.

- Silicon photonics has many challenges ahead. This includes standardization and platform technology. OIDA should aide in the formation of an Optical Foundry Consortium to develop technology platforms to enable the integrated photonics circuit industry.

- The cost of an optical module for the SAN and datacenter will require a new packaging technology implementation. Leveraging the LED packaging technology should be considered by the fiber optic supply base.

- The copper connector industry has defined the roadmap for next generation connectors up to 40 Gbit/s. The fiber optic industry need to understand how this fits into the transceiver module requirements and what additional connector technology should be developed in conjunction with module manufacturers.

- Current packaging of fiber optic transceivers has migrated to South East Asia; the U.S. government should recognize the lack of fiber optic packaging infrastructure in the U.S. and develop a program to improve American competitiveness in this area.

- The packaging and reliability of silicon photonic components will be a challenge. The computer network companies and the U.S. government need to recognize the challenges in developing optical IC packaging and industry reliability requirements.

13 Summary and conclusions

The forum held by the OIDA provided valuable insight in the current paths being developed for optical interconnects and the current status of silicon photonics development. Clearly, the importance of light emission on a wafer scale is essential to enable new technology development. Several different approaches are being developed today. The oldest and most reliable is the die bonding of qualified laser die onto the silicon optical bench. This approach is based on assembly processing and not wafer processing. The advantage of the silicon industry has been the integration of functions on a wafer scale semiconductor platform. The implementation of light sources into the silicon fabrication process will provide scale to the volume manufacture of integrated optical devices.

The lack of a III-V or photonic industry foundry is a hindrance to the development of Silicon photonics and InP photonic integration. Within Europe, the ePIXnet program is proposing a program for development of such a consortium. To enable success, joint work with U.S. semiconductor manufacturing is necessary. This raises the question whether a government enabled optical foundry program should be developed to enable competitiveness in the current global market. Some initial infrastructure similar to the MOSIS program could enable a new technology industry within the U.S.

Currently, the copper interconnect market remains healthy with every increasing performance improvements for short reach links. This market trend provides a wall that must be climbed before optical connections with the server environment can become main stream. Several key metrics were a continual theme through the meeting. Several server companies discussed the issue of the cost of optical links. Within the traditional communications market today, most optical component vendors are losing money. The computer industry members proposed concentrating on three key aspects, $/Gbit, $/W and a comparison to copper. The target of $1/Gbit is a factor of 4-8 lower than available today.

The government initiatives in Japan, Europe, and the U.S. are pushing for high performance and new technology for optical computing interconnects. Within the U.S., the Defense Advanced Research Projects Agency remains committed to funding new optical technology.

Continued emphasis on silicon photonics is a key area where potential change can be realized. The main issue will remain the development of a low cost reliable light source. III-V photonics offers this today, but is felt incompatible with the current silicon industry direction. Fitting III-V into a CMOS environment provides several challenges and commitment from silicon companies. A solution discussed at the meeting was the potential development of a silicon photonics foundry program, similar to MOSIS. This might enable the silicon photonics paradigm shift to increase development and research in this area.

The IC industry and copper interconnect manufacturers remain committed to pushing the boundary for electrical interconnects. The roadmap for electrical connectors currently

extends to 40Gbit/s. The introduction of silicon via interconnects and 3-D stacking of chipsets will extend the life of on-chip electrical interconnects. The current global wire interconnect problem and ‘red brick wall’ highlighted by the ITRS remain to be resolved. It is evident that the optical technology today for intra chip and inter chip signaling remains too immature for introduction. The implementation of silicon photonics into traditional communications space where they can add increased functionality for smaller package size, does not follow the current trend or philosophy of switch/router manufacturers. Today, companies, like Cisco Systems are pulling out CDR technology from the transceivers to reduce cost. Marketing of increased transceiver functionality is a gamble for silicon photonics companies.

Finally, silicon photonics has a promising future. As we move forward, the roadmap for this sector needs to be further refined. There definitely remains a need for higher speeds and development of highly reliable low cost interconnects. The challenge to the industry will be how to fund this requirement and standardize the output of the different technologies being pursued today.

Appendix A – Forum Agenda

Silicon Photonics: Challenges and Future

February 22, 2007 – Marriott Santa Clara, Santa Clara, CA

7.30 – 8.00 a.m.	Registration and Continental Breakfast
8.00 – 8.10	Welcome – *Michael Lebby* – OIDA
8.10 – 8.15	Introduction – *Bill Ring*, WSR Optical Device Solutions
8.15 – 10.05 a.m.	**Silicon Photonics**
8.15 – 8.35	Strategies Unlimited – *Tom Hausken*
8.35 – 8.55	Intel – *Mike Morse*
8.55 – 9.15	IBM – *Jeffrey Kash*
9.15 – 9.35	Ghent University – *Pieter Dumon*
9.35 – 9.55	University of Trento – *Nicola Daldosso*
9.55 – 10.05	*Moderated discussion*
10.05 – 10.30	**Coffee Break**
10.30 – 12.20 p.m.	**Silicon Photonics**
10.30 – 10.50 a.m.	Luxtera – *Cary Gunn*
10.50 – 11.10	Kotura – *Jean-Louis Malinge*
11.10 – 11.30	ARCH Venture Partners – *Patrick Ennis*
11.30 – 11.50	Sun Microsystems – *Ashok Krishnamoorthy*
11.50 – 12.10 p.m.	Infinera – *David Welch*
12.10 – 12.20	*Moderated discussion*
12.20 – 1.30	**Lunch**
1.30 – 3.20 p.m.	**Silicon Photonics**
1.30 – 1.50	National Research Council of Canada – *Siegfried Janz*
1.50 – 2.10	Massachusetts Institute of Technology – *Michael Geis*
2.10 – 2.30	Translucent – *Vijit Sabnis*
2.30 – 2.50	UCSB – *John Bowers*
2.50 – 3.10	UCLA – *Kannan Raj*
3.10 – 3.20	*Moderated discussion*
3.20 – 5.30 p.m.	**Breakout Discussions**
3.20 – 4.50	Breakout discussions
4.50 – 5.20	Reports from breakout leaders
5.20 – 5.30	Workshop summary and concluding remarks

Appendix B – Forum Attendee List

Giovanni Barbarossa
CTO and Sr. Vice President of Product Development
Avanex Corporation
40919 Encyclopedia Circle
Fremont, CA 94538
Tel: (510) 897-4176
Email: Giovanni_Barbarossa@avanex.com

Jerry Bautista
Director, Technology Management
Intel Corporation
SC12-303
2200 Mission College Blvd.
Santa Clara, CA 95054
Tel: (408) 765-8784
Email: jerry.r.bautista@intel.com

John Bowers
Professor
University of California, Santa Barbara
Room 5113, ECE Department
Santa Barbara, CA 93106
Tel: (805) 893-8447
Email: bowers@ece.ucsb.edu

John D'Ambrosia
Scientist, Components Technology
Force10 Networks
7701 Aynlee Way
Harrisburg, PA 17112
Tel: (717) 460-8535
Email: jdambrosia@force10networks.com

Nicola Daldosso
Senior Researcher
University of Trento
via Sommarive 14
Povo (Trento), 38050 Italy
Tel: 390461882037
Email: daldosso@science.unitn.it

Jon DeGroot
Associate Scientist
Dow Corning Corporation
2200 W. Salzburg Road
Midland, MI 48686
Tel: (989) 496-4764
Email: jon.degroot@dowcorning.com

Hongyu Deng
Finisar Corporation
41762 Christy Street
Freemont, CA 94538
Tel: (510) 979-3006
Email: hongyu.deng@finisar.com

Mark Donovan
Senior Director
Finisar Corporation
41762 Christy Street
Sunnyvale, CA 94538
Tel: (510) 979-3002
Email: mark.donovan@finisar.com

Pieter Dumon
Ghent University (Universiteit Gent)
St. Pietersnieuwstraat 41
Dept. of Information Technology
Gent, B-9000
Belgium
Tel: 32-92643448
Email: pieter.dumon@intec.ugent.be

Patrick Ennis
Managing Director
ARCH Venture Partners
1000 Second Avenue, Suite 3700
Seattle, WA 98104
Tel: (206) 674-3273
Email: pjennis@archventure.com

Michael Fogg
Member of the Technical Staff II
Tyco Electronics Corporation
M.S. 128-20, P O. Box 3608
Harrisburg, PA 17105-3608
Tel: (717) 986-5802
Email: mike.fogg@tycoelectronics.com

Veronique Francois
Professor
Ecole de Technologie Superieure
Electrical Engineering Department
1100 Norte-Dame St., West
Montreal, QC, H3C 1K3 Canada
Tel: (514) 396-8800 X7730
Email: vfrancois@ele.etsmtl.ca

Richard Gaughan
Contributing Editor
Photonics Spectra
P. O. Box 1589
Boulder Creek, CA 95006
Tel: (831) 338-1241
Email: rgaughan@mountainoptical.com

Richard Grzybowski
Director, Systems Engineering
Corning Incorporated
One Science Center Drive, SP-AR-02
Corning, NY 14831
Tel: (607) 974-0681
Email: grzybowsrr@corning.com

Michael Geis
Technical Staff
MIT Lincoln Laboratory
LL-I-300C Lincoln Laboratory
Cambridge, MA 02139
Tel: (781) 981-7875
Email: geis@ll.mit.edu

Peter Guilfoyle
Chairman, CEO
OptiComp Corporation
215 Elks Point Road, P.O. Box 10779
Zephyr Cove, NV 89448
Tel: (775) 588-4176
Email: peter@opticomp.com

Andreas Goebel
VP, Photonics Integration
Innolume, Inc.
3333 Bowers Avenue, Suite 190
Santa Clara, CA 95054
Tel: (408) 689-3702
Email: andreas.goebel@innolume.com

Cary Gunn
CTO
Luxtera
1819 Aston Avenue, Suite 102
Carlsbad, CA 92008
Tel: (760) 448-3520
Email: cary@luxtera.com

Joel Goergen
Chief Scientist/VP of Technology
Force10 Networks
350 Holger Way
San Jose, CA 95134
Tel: (408) 571-3694
Email: joel@force10networks.com

Mark Gustlin
Principal Engineer
Cisco Systems, Inc
170 West Tasman Drive
San Jose, CA 95008
Tel: (408) 527-2299
Email: mgustlin@cisco.com

Russ Granger
Business Development Manager
US Conec Ltd.
1555 4th Avenue SE
Hickory, NC 28602
Tel: (828) 267-6385
Email: russgranger@usconec.com

Atikem Haile-Mariam
Product Marketing Manager
Finisar Corporation
1389 Moffett Park Drive
Sunnyvale, CA 94089
Tel: (408) 243-0031
Email: atikem.haile@finisar.com

Martin Green
Group Leader, Electronic and Optpelectronic Materials
NIST
100 Bureau Drive MS 8520
Gaithersburg, MD 20899-8520
Tel: (301) 975-8496
Email: martin.green@nist.gov

Sadiq Hasnain
Head, Business Development
National Research Council of Canada
Institute of Microstructural Sciences
1200 Montreal Rd., Building M-50
Ottawa, Ontario, K1A 0R6 Canada
Tel: (613) 993-6040
Email: sadiq.hasnain@nrc-cnrc.gc.ca

Tom Hausken
Director, Optical Components
Strategies Unlimited
201 San Antonio Circle, Suite 205
Mountain View, CA 94040
Tel: (650) 941-3438 Ext. 28
Email: thausken@strategies-u.com

Pierre Herve
Director Enterprise
Intel Corporation
TB1, 8674 Thornton Avenue
Newark, CA 94560
Tel: (510) 578-5889
Email: pierre.m.herve@intel.com

Zhengyu Huang
VP, International Sales and Business Development
RSoft Design Group
400 Executive Boulevard, Ste. 100
Ossining, NY 10562
Tel: (914) 923-2164
Email: zhengyu@rsoftdesign.com

Bernd Huebner
OSA Development Manager
Finisar Corporation
41762 Christy Street
Sunnyvale, CA 94538
Tel: (408) 203-9308
Email: bernd.huebner@finisar.com

David Huff
VP, Marketing and Business Development
OIDA
1015 N. Trooper Road
Eagleville, PA 19403
Tel: (202) 741-9352
Email: huff@oida.org

Diana Huffaker
Associate Professor
University of New Mexico
Center for High Technology Materials
1313 Goddard, SE
Albuquerque, NM 87106
Tel: (505) 272-7845
Email: huffaker@chtm.unm.edu

David Iams
OIDA
1133 Connecticut Avenue, NW
Suite 600
Washington, DC 20036-4329
Tel: (202) 785-4426
Email: iams@oida.org

Osamu Ibarabi
Senior Engineer
NTT Advanced Technology Corporation
Neocity Mitaka Bldg.
3-35-1 Shimo-renjaku
Mitaka-shi 181-0013, Japan
Tel: 81 29 287 7010
Email: osamu.ibaragi@ntt-at.co.jp

Hideo Itoh
Nanoelectronics Research Institute
National Institute of Advanced Industrial Science and Technology
AIST Tsukuba Central 2
1-1-1 Umezono
Tsukuba, 305-8568, Japan
Tel: 81298615622
Email: hideo.itoh@aist.go.jp

Kenneth Jackson
EMCORE Fiber Optics
5314 Connemara Drive, NE
Rochester, MN 55906
Tel: (505) 349-0922
Email: kenneth_jackson@emcore.com

John Jaeger
Manager
Infinera
169 Java Drive
Sunnyvale, CA 94089
Tel: (408) 716-4812
Email: jjaeger@infinera.com

Bahram Jalali
University of California, Los Angeles
6531 Boelter Hall, Box 951595
Material Science & Engineering Dept.
Los Angeles, CA 90095-1595
Tel: (310) 825-4052
Email: jalali@ee.ucla.edu

Siegfried Janz
Group Leader, Optoelectronics Devices
National Research Council of Canada
1200 Montreal Road, Building M-50
Ottawa, ON K1A 0R6 Canada
Tel: (613) 990-0926
Email: siegfried.janz@nrc-cnrc.gc.ca

Pawan Kapur
Research Associate
Stanford University
CIS 100
Stanford, CA 94305
Tel: (650) 906-0844
Email: kapurp@stanford.edu

Jeffrey Kash
Manager and Research Staff Member
IBM Research
T.J. Watson Research Center - Room 29-149
P.O. Box 218
Yorktown Heights, NY 10598
Tel: (914) 945-1448
Email: jeffkash@us.ibm.com

Kenneth Kaufmann
Marketing
Hamamatsu Corporation
360 Foothill Road, Box 6910
Bridgewater, NJ 08807-0910
Tel: (908) 231-0960
Email: kkaufmann@hamamatsu.com

Chris Keller
Manager
Ibiden USA R&D
970 Knox Street, Suite A
Torrance, CA 90502
Tel: (310) 768-0519
Email: ckeller@ibiden-usa.com

Peter Kirkpatrick
Chief Architect
Aprius Inc.
440 North Wolfe Road
Sunnyvale, CA 94085
Tel: (408) 524-3166
Email: peter.kirkpatrick@aprius.com

Ashok Krishnamoorthy
Distinguished Engineer
CTO Physical Science Center
RAS Computer Analysis Laboratory
Sun Microsystems
Mailstop USAN10-107
9515 Towne Centre Drive
San Diego, CA 92121
Tel: (858) 526-9414 Ext. 55414
Email: ashok.k@sun.com

Victor Krutul
Director, Silicon Photonics Strategy
Intel Corporation
2200 Mission College Blvd., SC 12-326
Santa Clara, CA 95052
Tel: (408) 353-3333
Email: victor.krutul@intel.com

Greg Le Cheminant
Measurement Applications Engineer
Agilent Technologies
5301 Stevens Creek Blvd.
Santa Clara, CA 95051
Tel: (707) 577-6524
Email: greg_lecheminant@agilent.com

Michael Lebby
President and CEO
OIDA
1133 Connecticut Avenue, NW
Suite 600
Washington, DC 20036-4329
Tel: (202) 785-4426
Email: lebby@oida.org

Ansheng Liu
Principal Engineer
Intel Corporation
2200 Mission College Blvd.
Santa Clara, CA 95054
Tel: (408) 765-0271
Email: ansheng.liu@intel.com

Jean-Louis Malinge
President and CEO
Kotura
2630 Corporate Place
Monterey Park, CA 91754
Tel: (626) 236-4500
Email: jlmalinge@kotura.com

Jan Meise
Director of Strategic Marketing, Optics Division
Finisar Corporation
1389 Moffett Park Drive
Sunnyvale, CA 94089
Tel: (408) 548-1000
Email: jan.meise@finisar.com

Terry Morris
Fellow
Hewlett-Packard
3000 Waterview P:arkway
Richardson, TX 75080
Tel: (972) 497-4517
Email: terrel.morris@hp.com

Gary Moskovitz
President and Chief Executive Officer
Reflex Photonics Inc.
550 Sherbrooke Street West
Suite 680 West Tower
Montreal, QC H3A 1B9 Canada
Tel: (514) 842-5179 Ext. 226
Email: gmoskovitz@reflexphotonics.com

Ed Murphy
Group Chief Technology Officer
JDSU
45 Griffin Road South
Bloomfield, CT 06002
Tel: (860) 243-6642
Email: ed.murphy@jdsu.com

Maziar Nezhad
Graduate Researcher
University of California, San Diego
Tel: (858) 204-3918
Email: maziar@ucsd.edu

KC Noddings
Photonics Eng. 5
Boeing
901 N. Selby Street
W-S25-C572
El Segundo, CA 90245
Tel: (310) 662-8714
Email: kenneth.c.noddings@boeing.com

Jugnu Ojha
Strategic Marketing
Avago Technologies
350 W. Trimble Road, MS 90th
San Jose, CA 95131-1800
Tel: (408) 435-4270
Email: jugnu.ojha@avagotech.com

Prakash
Research Fellow
University of California, Los Angeles
420 Westwood Plaza
Los Angeles, CA 90095
Tel: (310) 206-4554
Email: prakash@ee.ucla.edu

Peter Pepeljugoski
Research Staff Member Optical Comm.
IBM
1101 Kitchawan Road
Yorktown Heights, NY 10598
Tel: (914) 945-3761
Email: petarp@us.ibm.com

Kannan Raj
Product Line Manager
Zarlink Semiconductor
3650 E. Wier Avenue
Phoenix, AZ 85040
Tel: (602) 414-1707
Email: kannan.raj@zarlink.com

Jaime Reloj
Vice President Worldwide Sales
ColorChip lnc.
1028 H llywood Avenue
Oakland, CA 94602
Tel: (510) 336-2447
Email: jaimer@color-chip.com

William Ring
Managing Director
WSR - ODS
2300 Rachel Terrace, Apt. 7
Pinebrook, NJ 07058
Tel: (908) 212-1923
Email: wsring@wsr-ods.com

Kent Rochford
Optoelectronics Division Chief
NIST
325 Broadway, MS 815
Boulder, CO 80305-3328
Tel: (303) 497-5375
Email: rochford@boulder.nist.gov

Haisheng Rong
Senior Research Scientist
Photonics Technology Lab
Intel Corporation
Corporate Technology Group
2200 Mission College Blvd., SC12-326
Santa Clara, CA 95054
Tel: (408) 765-0331
Email: haisheng.rong@intel.com

Vijit Sabnis
Senior Staff Scientist
Translucent, Inc
952 Commercial Street
Palo Alto, CA 94303
Tel: (650) 213-9311 x225
Email: vijit@translucentinc.com

Scott Schube
Strategic Marketing Manager
Intel Corporation
Optical Platform Division
8674 Thornton Avenue
Newark, CA 94560
Tel: (510) 578-5815
Email: scott.a.schube@intel.com

Mike Shahine
Principal Engineer
Ciena
920 Elkridge Landing Road
Linthicum, MD 21090-2917
Tel: (410) 865-8602
Email: mshahine@ciena.com

Masayuki Shigematsu
President
Innovation Core SEI, Inc.
2580 North First Street, Suite 400
San Jose, CA 95014
Tel: (408) 324-1804
Email: shigematsu-masayuki@sei.co.jp

Etsuji Sugita
Vice President
Hakusan Manufacturing Company
26-5, 2-chome
Minamiikebukuro, Toshima-ku
171-0022 Tokyo, Japan
Tel: 81 3 595 11211
Email: sugita@hakusan-mfg.co.jp

Michael Tan
Scientist
Hewlett-Packard
1501 Page Mill Road, MS 1123
Palo Alto, CA 94304
Tel: (650) 857-5794
Email: mike.tan@hp.com

Marek Tlalka
Vice President of Marketing
Luxtera
1819 Aston Avenue, Suite 102
Carlsbad, CA 92008
Tel: (760) 448-3520
Email: mtlalka@luxtera.com

Hugues Tournier
HW Advisor
Nortel Networks
3500 Carling Avenue
Ottawa, ON K2C 8H9 Canada
Tel: (613) 765-4748
Email: tournier@nortel.com

Peter Van Daele
Professor, Optical Interconnections & Packaging Group
Ghent University (Universiteit Gent)
INTEC Department
Gaston Crommenlaan 8 Box 201
Gent - Ledenberg
Belgium, B-9050
Tel: 32-9-331-49-04
Email: peter.vandaele@intec.ugent.be

Yuri Vandyshev
Senior Optical Engineer
Finisar Corporation
41762 Christy Street
Fremont, CA 94538
Tel: (510) 979-3044
Email: yuri.vandyshev@finisar.com

Rich Vodhanel
Research Manager, Optical Systems and Networks
Corning Incorporated
1 River Front Plaza
SP-AR-02-4
Corning, NY 14831
Tel: (607) 974-2401
Email: vodhanelrs@corning.com

Guangxi Wang
Graduate Student
CALTECH
Caltech MS 136-93
Pasadena, CA 91125
Tel: (626) 395-2269
Email: wangg@caltech.edu

Winston Way
CTO and Founder
OpVista
870 N. McCarthy Blvd.
Milpitas, CA 95035
Tel: (949) 923-1117
Email: wway@opvista.com

Jan Weem
Principal Engineer
Aprius Inc.
440 North Wolfe
Sunnyvale, CA 94085
Tel: (408) 507-5217
Email: jan.peeters.weem@aprius.com

David Welch
Chief Technology and Strategy Officer
Infinera
169 W. Java Drive
Sunnyvale, CA 94089
Tel: (408) 572-5364
Email: dwelch@infinera.com

Jim Weldon
Chief Operating Officer
Translucent, Inc
952 Commercial Street
Palo Alto, CA 94303
Tel: (650) 213-9311
Email: jim@translucentinc.com

Charles White
Vice President, Strategic Relations
Tessera, Inc.
3099 Orchard Drive
San Jose, CA 95134
Tel: (408) 952-4343
Email: cwhite@tessera.com

Michael Wiemer
PhD Student
Stanford University
P. O. Box 17416
Stanford, CA 94309
Tel: (650) 725-2774

Tom Willis
GM, Optical Interconnects
Intel Corporation
Tel: (503) 957-7567
Email: tom.willis@intel.com

Gregory Wojcik
VP, Engineering
Innolume, Inc.
3333 Bowers Ave., Ste. 190
Santa Clara, CA 95054
Tel: (408) 689-3710
Email: greg.wojcik@innolume.com

Dan-Xia Xu
Senior Research Officer, Optoelectronics Div.
National Research Council of Canada
1200 Montreal Road, Building M-50
Ottawa, ON K1A 0R6 Canada
Tel: (613) 998-8826
Email: Danxia.Xu@nrc-cnrc.gc.ca

Andrew Yang
Consultant
OIDA
3041 N. Pollard St.
Arlington, VA 22207-4137
Tel: (703) 243-2231
Email: acyang@aol.com

Jong-Souk Yeo
Research Scientist
Hewlett-Packard
1000 NE Circle Blvd.
Corvallis, OR 97330
Tel: (541) 715-1641
Email: jong-souk.yeo@hp.com

Homan Yuen
Staff Scientist
Translucent, Inc
952 Commercial Street
Palo Alto, CA 94303
Tel: (650) 213-9311 Ext. 224
Email: homan@translucentinc.com

Eric Zbinden
Director
Aprius Inc.
440 North Wolfe Road
Sunnyvale, CA 94085
Tel: (650) 796-1608
Email: eric.zbinden@aprius.com