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WOCSDICE 2000 put together an excellent program covering a wide range of compound semiconductor issues.

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of Michigan

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WOCSDICE 2000

24ᵗʰ Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe

May 29 – June 02, 2000

Aegean Sea Greece

Sponsored by

ONREUR   EOT   OTE   INTRACOM

WOCSDICE 2000

24th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe

May 29 – June 02, 2000

Aegean Sea, Greece

Welcome Address

Welcome to the 24th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE 2000).

It is my great pleasure to be your host for this year's event and I am excited to see that it attracted an excellent group of people from all over the word. I am particularly happy to host WOCSDICE 2000 in Greece, the place where I had the honor to organize it again in 1981, almost 20 years ago in the small and picturesque island of Spetsai. Greece has changed a lot since then, reflecting clearly its European Union character in numerous aspects. Most important for our field, it has a sound electronic infrastructure that was only in its beginning at the time of the Spetsai event. This is evidenced by the participation and help in the organization of the two local universities, the University of Crete, Foundation for Research and Technology, Hellas in Heraklion and the National Technical University of Athens. Two major Greek telecommunication enterprises, INTRACOM and OTE have also proved their strong commitment in our field by sponsoring our Workshop. I would like to take this opportunity to thank them all, as well as, the European Research Office (ERO), the Office of Naval Research (ONR) and EOT, the Hellenic Tourist Organization for their support.

As you all know, WOCSDICE has a long-standing tradition and was established in 1973. Since then it has been regularly held in different places in Europe. I am very happy to see that my dream came finally true and this year's event is held aboard a cruise ship in the Aegean Sea. I would like to thank all of you for your continuous support throughout the difficult times of the organization. We have attracted several high quality invited talks and splendid contributed papers thanks to the help of the advisory committee. We were lucky to have the continuous support and strong commitment of Dr. Andreas Eisenbach and Mrs. Liliana Bertola-Pavlidis throughout the year of its organization. Thanks also go to my wife for her contributions to the endless unsolved organization issues and for her patience. Manos Travel S.A. has played a key role in providing a solution to my demanding requests for a conference aboard a cruise ship. Finally, it is thanks to you all, participants of WOCSDICE 2000 that we were able to put together an excellent program covering a wide range of compound semiconductor issues.

This year's event was planned for the first time so that it takes place in the same European country over two consecutive weeks with its sister meeting "5th International Workshop on Expert Evaluation & Control of Compound Semiconductor Materials & Technologies" (EXMATEC). The program has 63 papers, 12 of which are invited. Participants come from 12 European countries, Australia, Canada, Japan and the US, a truly international group of experts representing a multitude of disciplines from material growth to electronic, optical devices and integrated circuits. Please make the best out of our meeting by discussing your latest results and interacting with other participants. This is a great chance for technical exchange and networking opportunities in addition to enjoying the Aegean Sea!

I look forward to a very successful meeting. Welcome aboard

Dimitris Pavlidis
WOCSDICE Chair

INTRACOM

Founded in 1977, INTRACOM is the largest manufacturer of telecommunication equipment and information systems in Greece. In 1990, the company is listed on the Athens Stock Exchange and, by accelerating growth, establishes a strategic position within the European market. In cooperation with its subsidiaries and affiliates, the company provides products and services to the Greek public and private sectors, while developing significant international presence.

INTRACOM provides products as well as integrated services for the design, manufacturing, turn-key project implementation and support in the following areas: Public Telecommunication Networks; Telecommunication Systems Software; Integrated Business Networks; Network Management Systems; Payphones and Terminals; Energy Management Systems; Satellite Applications; Integrated Wagering Networks.

In the Greek market, INTRACOM is the main supplier of telecommunications hardware and software to the Hellenic Telecommunications Organization (OTE). The five year Frame Agreement, signed in December 1997 and budgeted at GRD 223 billion, is aimed at the further modernization, expansion and digitalization of OTE's network and constitutes an important milestone in the company's 22 year history.

The INTRACOM Group is comprised of a network of autonomous companies specializing in the design and delivery of integrated telecom projects, the development of application software and integration for large data networks, the manufacture of steel structures and electromechanical equipment for fixed and mobile telephony networks, energy systems, airport systems, as well as in integrated wagering networks and training services. Additionally, INTRACOM strengthens its international presence through the establishment of joint ventures and subsidiaries in Central and Eastern Europe (Bucharest, Sofia, Moscow, Budapest, etc). Since 1997, INTRACOM is also targeting the markets of the Middle East, North Africa and Asia.

Investing systematically in Research and Development, INTRACOM has established advanced research facilities for new product development and participates in numerous European cutting-edge research programs. It is the first Greek company to be certified under the ISO 9001, AQAP 110 and AQAP 13 international standards.

INTRACOM employs today more than 2100 highly qualified and specialized professionals, while the INTRACOM Group has a total work force of approximately 4200. The company's facilities cover a total area of 55,000 sq.m. that will soon be expanded to 70,000 sq.m.

INTRACOM's prospects in the coming years are particularly promising. While total sales for the period 1995-1999 reached GRD 360 billion, for the period 2000-2004 they are expected to reach GRD 1250 billion. Exports, for the same period (1995 - 1999), amounted to GRD 100 billion (29% of total sales in 1999). INTRACOM's objective is to boost sales from exports up to 40% of total sales in the next five years (2000-2004), reaching GRD 500 billion.

INTRACOM S.A.
Hellenic Telecommunications and Electronics Industry
Markopoulou Ave.
19002 Peania / Athens
GREECE
Tel: + 30 1 6860000 or + 30 1 6690000
Fax: + 301 6644379 or + 30 1 6643718
E-mail: intracom@intracom.gr
URL: www.intracom.gr

Workshop Chair

Prof. Dimitris Pavlidis
The University of Michigan
Department of Electrical Engineering and Computer Science
Solid State Electronics Laboratory
1301 Beal Avenue
Ann Arbor, MI 48109-2122, U.S.A.

Tel: +1 (734) 647-1778
Fax: +1 (734) 763-9324
E-mail: pavlidis@umich.edu

Local Chairs

Prof. Nikolaos K. Uzunoglou
National Technical University of Athens
Department of Electrical and Computer
Engineering
Division of Electroscience
157 73 Zografou, Athens, Greece

Phone: +30 (01) 772-3556
Fax: +30 (01) 772-3557
E-mail: nuzu@cc.ece.ntua.gr

Dr. Konstantinos Zekentes
Foundation for Research & Technology - Hellas
Institute of Electronic Structure and Laser
Microelectronics Research Group
Vassilika Vouton, PO Box 1527
711 10 Heraklion, Crete, Greece

Phone: +30 (81) 394-108
Fax: +30 (81) 394-106
E-mail: trifili@physics.uch.gr

Workshop Secretary

Dr. Andreas Eisenbach
The University of Michigan
Department of Electrical Engineering and Computer Science
Solid State Electronics Laboratory
1301 Beal Avenue
Ann Arbor, MI 48109-2122, U.S.A.

Tel: +1 (734) 936-1599
Fax: +1 (734) 763-9324
E-mail: eisenbac@engin.umich.edu

Internet

URL: http://www.eecs.umich.edu/dp-group/Wocsdice.html

E-mail: wocsdice@eecs.umich.edu

Advisory Committee

Prof. Werner Bächtold, Eidgenössische Technische Hochschule Zürich (Switzerland)

Prof. Lester F. Eastman, Cornell University (U.S.A.)

Prof. Fausto Fantini, Università degli Studie di Parma (Italy)

Prof. Hans L. Hartnagel, Technische Universität Darmstadt (Germany)

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Prof. Erhard Kohn, Universität Ulm (Germany)

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Prof. Elias Muñoz Merino, Universita Politécnica de Madrid (Spain)

Prof. David V. Morgan, Cardiff University (Wales)

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Dr. Jean-Luc Pélouard, Centre National de la Recherche Scientifique (France)

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Prof. Hartwig W. Thim, Johannes Kepler Universität Linz (Austria)

Prof. Theo G. van de Roer, Eindhoven University of Technology (The Netherlands)

Dr. Joachim Würfl, Ferdinand-Braun-Institut für Höchstfrequenztechnik (Germany)

Invited Speakers

Dr. Jean-Charles Garcia
"GaAs-based Materials for HBTs"
Picogiga
5, Rue de Réunion
Z.A. de Courtaboeuf
91940 Les Ulis, France

Prof. Pierre Gibart
"To what extent should we reduce the defect density for
GaN devices?"
Centre National de la Recherche Scientifique (CNRS)
Centre de Recherche sur l'Hétéroépitaxie et ses Applications
(CRHEA)
Sophia-Antipolis
06560 Valbonne, France

Prof. George I. Haddad
"Recent Advances in Two-Terminal Devices for mm-
Wave and THz Applications"
The University of Michigan
Department of Electrical Engineering and Computer Science
1301 Beal Avenue
Ann Arbor, MI 48109-2122, U.S.A.

Prof. Hideki Hasegawa
"Prospects and Key Issues of Compound Semiconductor
Nanoelectronics"
Hokkaido University
Research Center for Interface Quantum Electronics (RCIQE)
N13, W8
Sapporo 060-8628, Japan

Dr. Daniel Hofstetter
"Mid-IR emission/absorption from GaN-based
heterostructures"
Université de Neuchâtel
Institut de Physique
Physique mésoscopique
1, rue A.-L. Breguet
2000 Neuchâtel, Switzerland

Prof. Arvydas Matulionis
"Fluctuations and ultrafast processes of dissipation in
2DEG channels"
Semiconductor Physics Institute
A. Goštauto 11
2600 Vilnius, Lithuania

Dr. Miroslav Micovic
"GaN/AlGaN HEMTs Grown by RF-Assisted MBE for
Robust Low Noise and High Power Amplifiers"
HRL Laboratories LLC
3011 Malibu Canyon Rd
Malibu, CA 90265, U.S.A.

Prof. Takashi Mizutani
"Potential Profile Measurements of III-V Devices and
Materials Using Kelvin Probe Force Microscopy"
Nagoya University
Department of Quantum Engineering
Furo-cho, Chikusa-ku
Nagoya 464-8603, Japan

Prof. Manfred H. Pilkuhn
"VISIBLE LASERS: InGaP and GaInN"
Universität Stuttgart
Physikalisches Institut
Pfaffenwaldring 57
70569 Stuttgart, Germany

Prof. Hermann Schumacher
"Recent Results on SiGe HFETs and HBTs"
Universität Ulm
Department of Electron Devices and Circuits
Albert Einstein Allee 45
89069 Ulm, Germany

Dr. Didier Théron
"HEMT structures on GaAs and InP substrates for
millimeter wave power amplification"
Institut d'Electronique et de Microélectronique du Nord
(IEMN)
Département Hyperfréquence et Semiconducteurs
Avenue Poincaré, B.P. 69
59652 Villeneuve d'Ascq, France

Dr. Colin E.C. Wood
"US Navy Research Progress in Wide Gap
Semiconductors & NICOP International Opportunities
in Wide Gap Semiconductors"
Office of Naval Research
Electronics Department
800 N Quincy St
Ballston Tower One
Arlington, VA 22217-5660, U.S.A.

HELLENIC TELECOMMUNICATIONS ORGANISATION CORPORATE PROFILE

The Hellenic Telecommunications Organization (OTE) is the key player in the Greek telecommunications sector, with an instrumental role in the greater Balkan region. OTE provides its customers with a full range of telecommunication services and is the exclusive public switched telephony operator in Greece, until 1/1/2001. OTE has approximately 5.5 million customers in Greece and 300,000 shareholders.

OTE operates in the most rapidly developing sector of the Greek economy, with the highest profitability. In June 1999, OTE successfully completed its fourth public offering of shares. On November 2nd 1998, OTE became the first Greek company to enter the largest stock exchange of the world, the New York Stock Exchange.

As part of its international investment strategy and in order to become a leading telecommunications operator in Southeastern Europe, OTE has acquired 20% of Telecom Serbia, 90% of ArmenTel (Armenia) and recently 35% of Romtelecom (Romania), obtaining also control of its management. Furthermore, OTE, jointly with KPN (Royal Dutch Telecom) is under final negotiations for the acquisition of a 51% stake of the state-owned Bulgarian Telecom Company (BTC).

OTE is modernizing its organization and network. Through intensive efforts, OTE managed to raise the percentage of digitalization to approximately 92 % of the total available lines in 1999. OTE is increasing the capacity and quality of the local and trunk network, offering more high-speed lines to cover new demands as well as a wide range of new services, such as ISDN, ATM and Intelligent Network Services.

Nowadays, OTE forms a dynamic group of companies, already facing increased competition in its markets with great success. OTE's subsidiary, OTENET is among the dominant Internet Service Providers, while COSMOTE, in just 18 months of operation, has captured more than 25% of the mobile telephony market share. Other subsidiaries are: OTE CONSULTING, OTE SAT, Hellascom International, Maritel, OTE Leasing, OTE ASFALISI and OTE ANTALLAKTIRIA SYNALAGMATOS.

OTE is successfully transforming from a state-run monopoly to a customer-oriented corporation in the telecommunications industry, according to the expectations and demands of a free economy.

Hellenic Telecommunications Organization S.A.
99, Kiffisias Ave.
151 24 Maroussi, Athens, Greece
E-mail: ote@ote.net
URL: www.ote.gr

Session Chairs

Prof. Lester F. Eastman

Cornell University
School of Electrical Engineering
425 Philipps Hall
Ithaca, NY 14853-5401, U.S.A.
Tel: +1 (607) 255-4369
Fax: +1 (607) 255-4742
lfe@iiiv.tn.cornell.edu
http://www.iiiv.cornell.edu

Dr. Jean-Charles Garcia

Picogiga
Place Marcel Rebuffat – Parc de Villejust
91971 Courtaboeuf Cedex, France
Tel: +33 (01) 6931-6111
Fax: +33 (01) 6931-6178
picogiga@worldnet.fr

Prof. George I. Haddad

The University of Michigan
Dept. of Electrical Engineering & Computer Science
Solid State Electronics Laboratory
1301 Beal Avenue
Ann Arbor, MI 48109-2122, U.S.A.
Tel: +1 (734) 764-7139
Fax: +1 (734) 763-9324
gih@eecs.umich.edu

Prof. Hans Ludwig Hartnagel

Technische Universität Darmstadt
Institut für Hochfrequenztechnik
Merckstr. 25
64283 Darmstadt, Germany
Tel: +49 (06151) 16-2162
Fax: +49 (06151) 16-4367
hfmwe001@hrz2.hrz.tu-darmstadt.de

Prof. Hideki Hasegawa

Hokkaido University
Research Center for Interface Quantum Electronics
N13, W8
Sapporo 060-8628, Japan
Tel: +81 (011) 757-1163
Fax: +81 (011) 757-1165
hasegawa@rcige.hokudai.ac.jp

Dr. Daniel Hofstetter

Université de Neuchâtel
Institut de Physique, Physique mésoscopique
rue A.-L. Breguet 1
2000 Neuchâtel, Switzerland
Tel: +41 (32) 718-3545
Fax: +41 (32) 718-2901
Daniel.Hofstetter@iph.unine.ch
http://www.unine.ch/uer/uer_physique.hun

Prof. Didier Lippens

Université des Sciences et Technologies de Lille 1
Institut d'Electronique et de Microélectronique du
Nord (IEMN)
Département Hyperfréquences et Semiconducteurs
Avenue Poincaré, BP 69
59652 Villeneuve d'Ascq Cedex, France
Tel: +33 (03) 2019-7877
Fax: +33 (03) 2019-7892
Didier.Lippens@IEMN.univ-lille1.fr

Prof. Arvydas Matulionis

Semiconductor Physics Institute
A. Goštauto 11
2600 Vilnius, Lithuania
Tel: +370 (2) 618-101
Fax: +370 (2) 627-123
matulionis@uj.pfi.lt

Dr. Miroslav Micovic

HRL Laboratories LLC
3011 Malibu Canyon Rd
Malibu, CA 90265, U.S.A.
Tel: +1 (310) 317-5302
Fax: +1 (310) 317-5450
mirmico@attglobal.net

Prof. David Vernon Morgan

Cardiff University
School of Engineering
Queen's Buildings, The Parade, PO Box 925
Cardiff, Wales CF24 OYF, UK
Tel: +44 (0) 1222-874424
Fax: +44 (0) 1222-874292
morgandv@cardiff.ac.uk
http://www.cf.ac.uk/

Prof. Elias Muñoz

Universita Politécnica de Madrid
ETSI Telecomunicación, IEL
Ciudad Universitaria
28040 Madrid, Spain
Tel: +34 (91) 336-7321
Fax: +34 (91) 336-7323
elias@die.upm.es

Prof. Hermann Schumacher

Universität Ulm
Department of Electron Devices and Circuits
Albert Einstein Allee 45
89069 Ulm, Germany
Tel: +49 (0731) 502-6152
Fax: +49 (0731) 502-6155
hschu@ieee.org
http://www-ebs.e-technik.uni-ulm.de

Dr. Didier Théron

Institut d'Electronique et de Microélectronique du
Nord (IEMN)
Département Hyperfréquence et Semiconducteurs
Avenue Poincaré, B.P. 69
59652 Villeneuve d'Ascq, France
Tel: +33 (03) 2019-7826
Fax: +33 (03) 2019-7888
Theron@iemn.univ-lille1.fr

Prof. Hartwig W. Thim

Johannes Kepler Universität Linz
Microelectronics Institute
Altenbergerstr. 69
4040 Linz, Austria
Tel: +43 (0732) 2468-9300
Fax: +43 (0732) 2468-9316
h.thim@jk.uni-linz.ac.at

Dr. Colin Wood

Office of Naval Research
Electronics Department
800 N Quincy St
Arlington, VA 22217, U.S.A.
Tel: +1 (703) 696-4218
Fax: +1 (703) 696-2611
woodc@onr.navy.mil

Program

Monday, May 29, 2000	
9.00am	**Embarkation begins**
11.00am	**Departure**
11.15am	**Compulsory Emergency Drill**
11.30am	**Opening and Welcome (Prof. Dimitris Pavlidis, Chair WOCSDICE 2000)**
11.35am – 12.25pm	**Session I** **Growth of III-V Nitride Materials** **(Chair: Dr. Colin Wood, Office of Naval Research)**
11.35am	I.1 "To what extent should we reduce the defect density for GaN devices?" (INVITED) P. GIBART *CRHEA-CNRS, Valbonne, France*
11.55am	I.2 "A Single Step Nucleation Process for Growth of GaN-Based Materials by OMVPE" J.A. SMART and J.R. Shealy *Cornell University, Ithaca, USA*
12.10pm	I.3 "Nanoheteroepitaxy of GaN on Si" S.D. HERSEE, D. Zubia, S.H. Zaidi, and S.R.J. Brueck *University of New Mexico, Albuquerque, USA*

12.25 – 12.45pm	**Session II** **Characterization of Heterostructure Devices and Transport**
	      Properties, Part 1
	      (Chair: Prof. Hideki Hasegawa, Hokkaido University)

12.25pm	II.1 "Potential Profile Measurements of III-V Devices and Materials Using Kelvin Probe Force Microscopy" (INVITED) T. MIZUTAN, and Y. Eguchi *Nagoya University, Nagoya, Japan*
12.45 – 1.45pm	**Lunch (Restaurant)**

2.00 – 2.30pm	**Session II** **Characterization of Heterostructure Devices and Transport**
	      Properties, Part 2
	      (Chair: Prof. Hideki Hasegawa, Hokkaido University)

2.00pm	II.2 "Electrical transport in highly resistive GaN layers" M. Morvic,[a] J. Betko,[a] P. Javorka,[b] J.M. Van Hove,[c] and P. KORDOS[b] [a]*Slovak Academy of Sciences, Bratislava, Slovakia* [b]*Research Centre Jülich, Jülich, Germany* [c]*SVT Associates, Eden Prairie, USA*

Monday, May 29, 2000, continued	
2.15pm	II.3 "Characterisation of 2DEG transport properties using Quantitative Mobility Spectrum Analysis" D.A. Redfern, J. Antozsewski, J.M. Dell, and L. FARAONE *The University of Western Australia, Nedlands, Australia*
2.30 – 3.15pm	**Session III Processing and Packaging** **(Chair: Prof. David V. Morgan, Cardiff University)**
2.30pm	III.1 "One-Step Patterning of Asymmetric Gate Recess for InP HEMTs using Genetic Algorithms" F. Robin, A. ORZATI, E. Moreno, M. Spühler, O. Homan, and W. Bächtold *Swiss Federal Institute of Technology (ETH) Zürich, Zürich, Switzerland*
2.45pm	III.2 "Damage of InP Surfaces by RIE Processing" H.C. NEITZERT[1], R. Fang[2], M. Kunst[3], and N. Layadi[4] [1]*Università di Salerno, Fisciano, Italy* [2]*Centro Studi e Laboratori Telecomunicazioni, Torino, Italy* [3]*Hahn-Meitner-Institut, Berlin, Germany* [4]*Lucent Technologies, Orlando, USA*
3.00pm	III.3 "3D. Ultra Thin Chip Stacking: Methods and Results" J.P. BAILBÉ, S.Pinel, J.Tasselli, and A.Marty *Laboratoire d'Analyse et d'Architecture des Systèmes du CNRS, Toulouse, France*
3.15 – 4.05pm	**Session IV GaAs, InP-based HEMTs and Ballistic, Hot Electron Effects,** **Part 1 (Chair: Prof. Lester F. Eastman, Cornell University)**
3.15pm	IV.1 "HEMT Structures on GaAs and InP substrates for millimeter wave power amplification" (INVITED) D. THÉRON, Y. Cordier, X. Wallart, S. Bollaert, M. Zaknoune, M. Boudrissa, B. Bonte, C. Gaquière, F. Mollot, A. Cappy, R. Fauquembergue, and J.C. De Jaeger *University of Lille 1, Villeneuve d'Ascq Cedex, France*
3.35pm	IV.2 "Enhancement-mode metamorphic $Al_{0.67}In_{0.33}As/Ga_{0.66}In_{0.34}As$ HEMT on GaAs substrate" M. BOUDRISSA, E. Delos, Y. Cordier, D. Théron, and J.C. De Jaeger *Université des Sciences et Technologies de Lille, Villeneuve d'Ascq Cedex, France*
3.50pm	IV.3 "MODFET channel conductivity with high doping level" K. Pozela, J. POZELA, and V. Jucienė *Semiconductor Physics Institute, Vilnius, Lithuania*
4.05 – 4.25pm	**Afternoon Tea Time (Riviera Lounge)**
4.25 – 4.55pm	**Session IV GaAs, InP-based HEMTs and Ballistic, Hot Electron Effects, Part** **2 (Chair: Prof. Lester F. Eastman, Cornell University)**
4.25pm	IV.4 "Two-stream ballistic instability in two-channel field-effect transistors" Z.S. Gribnikov, N.Z. Vagidov, and V.V. MITIN *Wayne State University, Detroit, USA*
4.40pm	IV.5 "Hot Electron Injection Field Effect Transistor" E. Kolmhofer[*], K. Luebke[*], H. THIM[*], A. Lugstein[+], and E. Bertagnolli[+] [*]*University of Linz, Linz, Austria* [+]*Technical University of Vienna, Vienna, Austria*

Monday, May 29, 2000, continued	
4.55 – 6.00pm	**Session V Noise in Electronic and Optical Devices** **(Chair: Prof. Hermann Schumacher, Universität Ulm)**
4.55pm	V.1 "Fluctuations and ultrafast processes of dissipation in 2DEG channels" (INVITED) A. MATULIONIS, J. Liberis, V. Aninkevičius, L. Ardaravičius, and I. Matulionienė *Semiconductor Physics Institute, Vilnius, Lithuania*
5.15pm	V.2 "Low frequency noise behavior of microwave active devices and their related phase noise performances" M. Regis[1,2,3], J. GRAFFEUIL[1,3], O. Llopis[1] M. Borgarino[1] and R. Plana[1,3] [1]*LAAS-CNRS, Toulouse, France* [2]*SiGe Microsystems Inc, Ottawa, Canada* [3]*Université P. Sabatier, Toulouse, France*
5.30pm	V.3 "Quantum 1/f Noise in GaN Materials and Devices" P.H. HANDEL *University of Missouri-St. Louis, St. Louis, USA*
5.45pm	V.4 "Current Noise Suppression in Quantum Well Infrared Photodetectors at Low Bias Voltages" A. CARBONE and P. Mazzetti *Università del Politecnico di Torino, Torino, Italy*
6.00pm	**Optional: Disembarkation at Mykonos**
8.00 – 10.00pm	**Dinner / Open seating (Restaurant)**
9.15pm	**Last tender boat from shore to ship**
10.30pm	**Welcome Aboard Show (Dress code: Casual)**
	Tuesday, May 30, 2000
6.00 – 8.30am	**Breakfast Buffet (Sun Deck)**
7.00am	**Optional: Shore Excursions at Kusadasi**
11.30am	**All Aboard Time**
11.30am	**Departure from Kusadasi**
12.00 – 1.15pm	**Lunch (Restaurant)**

Tuesday, May 30, 2000, continued	
1.30 – 2.15pm	**Session VI** **Large-Signal Properties of FETs** **(Chair: Prof. Didier Lippens, Université de Lille)**
1.30pm	VI.1 "MOCVD delta-doped GaAs structures for power microwave transistors" V.L. Gurtovoi, V.V. Valyaev, S.Yu. SHAPOVAL, S.V. Morozov, S.V. Dubonos, and A.N. Pustovit *Russian Academy of Sciences, Chernogolovka, Russia*
1.45pm	VI.2 "Comparison of the RF Large Signal Performance of Common-Source, -Drain, and -Gate Amplifiers using GaAs MESFETs" F. ELLINGER, D. Treyer, R. Vogt, and W. Bächtold *Swiss Federal Institute of Technology (ETH) Zürich, Zürich, Switzerland*
2.00pm	VI.3 "10GHz load-pull measurement for a $0.3\mu m$-N-HIGFET" M. TOUIRAT, M. Roger, E. Delos, L.T. Nuyen*, and G. Salmer *Institut d'Electronique et de Microélectronique du Nord (IEMN), Villeneuve d'Ascq, France* *Picogiga, Courtaboeuf Cedex, France*
2.15 – 3.20pm	**Session VII** **GaAs and InP-based HBTs** **(Chair: Dr. Jean-Charles Garcia, Picogiga)**
2.15pm	VII.1 "GaAs-based Materials for HBTs" (INVITED) J.-C. GARCIA *Picogiga, Courtaboeuf, France*
2.35pm	VII.2 "Investigations on the Impact of the InGaP Ledge on HBT-Performance" V. Palankovski*, R. SCHULTHEIS**, A. Bonacina**, and S. Selberherr* *TU Vienna, Vienna, Austria* **Infineon Technologies AG, Munich, Germany*
2.50pm	VII.3 "The Influence of the Emitter Orientation on the Noise Characteristics of InP/InGaAs(P) DHBTs" A. HUBER, I. Schnyder*, M. Rohner*, H. Jäckel*, C. Bergamaschi, and K. Schenk *FH Aargau, Windisch, Switzerland* *Swiss Fedeal Institute of Technology, Zürich, Switzerland*
3.05pm	VII.4 "Development of a Novel InP/InGaAs(P) DHBT Process for Power Applications" I. SCHNYDER, M. Rohner, D. Huber, C. Bergamaschi*, and H. Jäckel *Swiss Fedeal Institute of Technology, Zürich, Switzerland* *FH Aargau, Windisch, Switzerland*
3.30pm	**Optional: Disembarkation at Patmos** **Optional: Shore Excursion Departure** (NOTE: Please dress modestly with knees and shoulders covered for monastery visit)
6.30 – 8.55pm	**Session VIII** **GaN-based HEMTs and HBTs, Oxide-based and SiC Devices** **(Chair: Prof. Hans L. Hartnagel, Technische Universität Darmstadt)**
6.30pm	VIII.1 "US Navy Research Progress in Wide Gap Semiconductors & NICOP International Opportunities in Wide Gap Semiconductors" (INVITED) C.E.C. WOOD *Office of Naval Research, Arlington, USA*

Tuesday, May 30, 2000, continued	
6.50pm	VIII.2 "GaN/AlGaN HEMTs Grown by RF-Assisted MBE for Robust Low Noise and High Power Amplifiers" (INVITED) M. MICOVIC, W.-S. Wong, P. Janke, P. Hashimoto, L.M. McCray, and C. Nguyen *HRL Laboratories, LLC, Malibu, USA*
7.10pm	VIII.3 "Performance Limits of AlGaN/GaN HEMTs" L.F. EASTMAN *Cornell University, Ithaca, USA*
7.25pm	VIII.4 "Growth and Characterization of AlN/GaN MISFETs" A. EISENBACH, E. Alekseev, S.M. Hubbard, and D. Pavlidis *The University of Michigan, Ann Arbor, USA*
7.40pm	VIII.5 "Silicon nitride passivation effects on GaN MESFETs" C. GAQUIÈRE, B. Boudart, R. Amokrane, Y. Guhel, Y. Crosnier, J.C De Jaeger, and F. Omnes[*] *Institut d'Electronique et de Microélectronique du Nord, Villeneuve d'Ascq Cedex, France* *Centre de Recherche sur l'Hetero-Epitaxie et ses Applications, Valbonne, France*
7.55pm	VIII.6 "Simulations of AlGaN/GaN HEMTs" R. ANHOLT *Gateway Modeling, Inc., Minneapolis, USA*
8.10pm	VIII.7 "Evaluation of AlGaN/GaN HBTs" S. Fathpour and D.L. PULFREY *University of British Columbia, Vancouver, Canada*
8.25pm	VIII.8 "Oxide-based pHEMTs and HBTs; what are they and why bother?" J. Champlain, C. Zheng, U.K. MISHRA *University of California, Santa Barbara, USA*
8.40pm	VIII.9 "Electrical characterization of $4H$-SiC p^+-n-n^+ Avalanche Diodes" K. Vassilevski[1,2], K. ZEKENTES[1], E. Bogdanova[2], and A. Zorenko[3] *[1]Foundation for Research and Technology-Hellas, Heraklion, Greece* *[2]Ioffe Institute, St. Petersburg, Russian Federation* *[3]State Scientific & Research Institute "Orion", Kyiv, Ukraine*
9.30 – 10.30pm	**Dinner (Restaurant)**
10.45pm	**Greek Night (Dress code: Blue & White – Dress as Greek as possible!)**

Wednesday, May 31, 2000

7.00 – 8.00am	**Breakfast Buffet (Sun Deck)**
8.00am	**Optional: Shore Excursions: Rhodes & the Acropolis of Lindos** (NOTE: Participants can only take option RHO-A; Companions may choose option RHO-B, which includes lunch)
12.30pm	**WOCSDICE Participants Aboard Time**

Wednesday, May 31, 2000, continued

12.45 – 2.00pm	**Lunch (Restaurant)**	

2.15 – 2.50pm	**Session IX**	**SiGe-based FETs and HBTs** **(Chair: Dr. Didier Théron, IEMN)**
2.15pm	IX.1	"Recent Results on SiGe HFETs and HBTs" (INVITED) H. SCHUMACHER[1] and U. König[2] *[1] University of Ulm, Ulm, Germany* *[2] DaimlerChrysler Research Center, Ulm, Germany*
2.35pm	IX.2	"SiGe BiCMOS Progress and Evolution at IBM" G. FREEMAN *IBM Microelectronics, Hopewell Junction, USA*

2.50pm – 4.35pm	**Session X**	**Electronic and Optoelectronic Integrated Circuits** **(Chair: Dr. Miroslav Micovic, HRL Laboratories LLC)**
2.50pm	X.1	"Low noise dielectric resonator PHEMT oscillator" S. VITUSEVICH[a], N. Klein[a], M. Winter[a], D. Schemion[a], K. Schieber[b], and M. Klauda[b] *[a] Research Center Juelich, Juelich, Germany* *[b] Bosch Telecom GmbH, Backnang, Germany*
3.05pm	X.2	"CAD-simulation results of an X-band MMIC Up-Converter" P.S. TSENES[1], G.E. Stratakos[1], N.K. Uzunoglu[1], D. Brikas[2], and I. Giouzelis[2] *(1) National Technical University of Athens, NTUA* *(2) INTRACOM S.A.*
3.20pm	X.3	"An X-band MMIC Down-Converter" P.S. TSENES[1], G.E. Stratakos[1], N.K. Uzunoglu[1], M. Lagadas[2], and G. Deligeorgis[2] *(1) National Technical University of Athens, NTUA* *(2) Foundation for Research & Technology-Hellas, FORTH*
3.05pm	X.4	"Advances in Integrated Six Port Direct Digital Millimetre Wave Receivers" T.M. Visan, J. Beauvais[*], Y. Xu, P. Jacquet and R.G. BOSISIO *Ecole Polytechnique de Montreal* *[*] Université de Sherbrooke, Sherbrooke, Canada*
3.50pm	X.5	"Vertically Integrated Transistor-Laser Structure, take 2" R.C.P. Hoskens, V.I. Tolstikhin[*], A. Förster[**], and T.G. VAN DE ROER *Eindhoven University of Technology, Eindhoven, The Netherlands* *[*] Optiwave Corp., Nepean, Canada* *[**] I.S.I. Jülich, Germany*
4.05pm	X.6	"Optimised Transceiver for Fiber to the Home Applications" J. HARARI[1], D. Decoster[1], F. Mallecot[2], J. Jacquet[2], A. Leroy[2], A. Plais[2], C. Chaumont[2], F. Doukhan[3], Y. Arnaudin[3], F. Laune[4], and A.L. Convert[4] *[1] IEMN, Villeneuve d'Ascq, France* *[2] OPTO+, Marcoussis, France* *[3] ALCATEL OPTRONICS, Nozay, France* *[4] RADIALL, St. Quentin Fallavier, France*
4.20pm	X.7	"Design and fabrication of a new optical switch for the synthesis of large time delays" Y. HERNANDEZ, J.P. Vilcot, J. Harari, D. Decoster, M. Schaller[*], and J. Chazelas[*] *Institut d'Electronique et de Micro-électronique du Nord, Villeneuve d'Ascq, France* *[*] THOMSON DETEXIS Photonics, Elancourt Cedex, France*

Wednesday, May 31, 2000, continued	xix

4.35 – 5.00pm	**Afternoon Tea Time (Riviera Lounge)**

5.00 – 5.30pm	**Session XI**	**Reliability of HEMTs and HBTs (Chair: Prof. George I. Haddad, The University of Michigan)**
5.00pm	XI.1	"Characterization and reliability of InP-based HEMTs implemented with different process options" G. MENEGHESSO, R. Luise, D. Buttari, A. Chini, H. Yokoyama*, T. Suemitsu*, E. Zanoni *Università di Padova, Padova, Italy* *NTT Photonics Laboratories, Kanagawa, Japan*
5.15pm	XI.2	"Reliability of GaInP/GaAs HBTs for Power Applications" H. BLANCK, K.J. Riepe, W. Doser, and D. Pons *United Monolithic Semiconductors GmbH, Ulm, Germany*

5.30 – 6.35pm	**Session XII**	**THz Sources, Diodes, and Receivers (Chair: Prof. Hartwig W. Thim, Johannes Kepler Universität Linz)**
5.30pm	XII.1	"Recent Advances in Two-Terminal Devices for mm-Wave and THz Applications" (INVITED) H. Eisele and G.I. HADDAD *The University of Michigan, Ann Arbor, USA*
5.50pm	XII.2	"Development of GaN-based Gunn-Effect Millimeter-Wave Sources" E. Alekseev, A. Eisenbach, D. PAVLIDIS, S.M. Hubbard, and W.E. Sutton *The University of Michigan, Ann Arbor, USA*
6.05pm	XII.3	"Challenges for a Terahertz solid state heterodyne receiver" D. LIPPENS, T. David, F. Podevin, X. Mélique, M. Fernandez, T. Akalin, P. Mounaix, and O. Vanbésien *Université de Lille1, Villeneuve d'Ascq Cedex, France*
6.20pm	XII.4	"$Al_{0.7}Ga_{0.3}As/GaAs$ HBV for 255 GHz Tripling Operation" M. SAGLAM[1], M. Bozzi[2], C. Domoto[3], M. Rodriguez-Girones[1], L. Perregrini[2], and H.L. Hartnagel[1] *[1]Technical University of Darmstadt, Darmstadt, Germany* *[2]University of Pavia, Italy* *[3]ATR Adaptive Communications Research Laboratories, Japan*

6.35 – 7.25pm	**Session XIII**	**Nanoelectronics (Chair: Prof. Arvydas Matulionis, Semiconductor Physics Institute)**
6.35pm	XIII.1	"Prospects and Key Issues of Compound Semiconductor Nanoelectronics" (INVITED) H. HASEGAWA *Hokkaido University, Sapporo, Japan*
6.55pm	XIII.2	"Fabrication of Nano-Structure for Room Temperature Single Electron Devices" K. MATSUMOTO *Electrotechnical Laboratory MITI, Japan*

Wednesday, May 31, 2000, continued	
7.10pm	XIII.3 "Resonant-Tunnelling 3-Terminal Devices for High-Speed Logic Application" W. Prost, P. Velling, G. Janssen[1], U. Auer, A. Brennemann, P. Glösekötter[2], K.F. Goser[2], and F.-J. TEGUDE *Gerhard-Mercator-Universität Duisburg, Duisburg, Germany* *[1]Technical University Eindhoven, Eindhoven, The Netherlands* *[2]University of Dortmund, Dortmund, Germany*
7.25 – 8.00pm	**Session XIV Lasers, LEDs, Detectors, and Photonic Bandgap Approaches, Part 1 (Chair: Dr. Daniel Hofstetter, Université de Neuchâtel)**
7.25pm	XIV.1 "VISIBLE LASERS: InGaP and GaInN" (INVITED) M.H. PILKUHN *Stuttgart University, Stuttgart, Germany*
7.45pm	XIV.2 "Blocklayers for AlGaInP-Lasers Emitting at 670nm" W. WAGNER, R. Butendeich, M. Ost, F. Scholz, and H. Schweizer *Universität Stuttgart, Stuttgart, Germany*
8.30pm	**Captain's Cocktail Party and Dinner (Dress code: Gala)**
10.45pm	**Gala Show**
	## *Thursday, June 01, 2000*
6.00 – 8.00am	**Breakfast Buffet (Sun Deck)**
7.10am	**Optional: Shore Excursions: Cretan Exploration or Palace of Knossos**
8.00am	**Optional: Visit of FORTH**
11.00am	**Embarkation**
11.00am – 12.00pm	**Settle your accounts at the Purser's Office (Promenade Deck)**
12.00 – 1.00pm	**Lunch (Restaurant)**
1.15 – 2.30pm	**Session XIV Lasers, LEDs, Detectors, and Photonic Bandgap Approaches, Part 2 (Chair: Dr. Daniel Hofstetter, Université de Neuchâtel)**
1.15pm	XIV.3 "Heterobarrier Leakage in InGaAsP Based Laser Diodes" H.C. NEITZERT and S.Massetti *Centro Studi e Laboratori Telecomunicazioni, Torino, Italy*
1.30pm	XIV.4 "The Reliability of AlGaInP Visible Light Emitting Diodes" D.V. MORGAN and I. Al-Ofi *Cardiff University, Cardiff, UK*

Thursday, June 01, 2000, continued	
1.45pm	XIV.5 "Pb-La-Zr-Ti-O/Sr-Ti-O Multilayered Structures on GaAs Substrates for Tunable Photonic-bandgap Applications" D. Young and A. CHRISTOU *University of Maryland, College Park, USA*
2.00pm	XIV.6 "Quantum-dot infrared detector: high sensitivity due to barrier-limited photoelectron capture" V. MITIN[1], V. Pipa[1], A. Sergeev[1], M. Dutta[2], and M. Stroscio[2] *[1]Wayne State University, Detroit, USA* *[2]U.S. ARO, Research Triangle Park, USA*
2.15pm	XIV.7 "New type AlGaAs X-ray detector with optical response" K. POZELA, J. Pozela, V. Jasutis, L. Dapkus, and A. Silenas *Semiconductor Physics Institute, Vilnius, Lithuania*
2.30 – 3.50pm	**Session XV** **Nitride-Based Optical Devices** **(Chair: Prof. Elias Muñoz, Universita Politécnica de Madrid)**
2.30pm	XV.1 "Mid-IR emission/absorption from GaN-based heterostructures" (INVITED) D. HOFSTETTER, J. Faist, and D.P. Bour[1) *University of Neuchâtel, Neuchâtel, Switzerland* *[1)XEROX Palo Alto Research Center, Palo Alto, USA*
2.50pm	XV.2 "(Al,Ga)N Ultraviolet Photodetectors on sapphire and Si substrates" E. MUÑOZ[1], E. Monroy[1], J.L. Pau[1], F. Calle[1], M.A. Sánchez[1], E. Calleja[1], F. Omnes[2], B. Beaumont[2], and P. Gibart[2] *[1]Univ. Politécnica de Madrid, Madrid, Spain* *[2]CNRS-CRHEA, Valbonne, France*
3.05pm	XV.3 "Ultra-Low-Noise Avalanche Photodiodes and $Al_xGa_{1-x}N$/GaN Photodetectors" J.C. CAMPBELL, A.L. Holmes, Jr., and R.D. Dupuis *University of Texas, Austin, USA*
3.20pm	XV.4 "Highly selective GaN/AlGaN/GaN UV photodiodes" D.L. PULFREY[1], M.P. Leslie[1], J.J. Kueck[2], B.D. Nener[2], G. Parish[3], U.K. Mishra[3], P. Kozodoy[4], and E.J. Tarsa[4] *[1]Univ. of British Columbia, Vancouver, Canada* *[2]Univ. of Western Australia, Perth, Australia* *[3]Univ. of California, Santa Barbara, USA* *[4]Nitres Inc., Goleta, USA*
3.35pm	XV.5 "Green SQW InGaN light-emitting diodes on Si(111) by metalorganic vapor phase epitaxy" E. Feltin, S. Dalmasso, H. Larèche, B. Beaumont, P. de Mierry, M. Leroux, and P. GIBART *Centre de Recherche sur l'Hétéro-Epitaxie et ses Applications, Valbonne, France*
4.00pm	**Optional: Disembarkation at Santorini**
4.00pm	**WOCSDICE Participants Aboard Time**
6.15 – 8.15pm	**Session XVI LATE NEWS and OVERFLOW PAPERS**
9.15pm	**Dinner (Restaurant)**

Thursday, June 01, 2000, continued	
10.45pm	**Farewell Showtime (Alassio Lounge)**
Friday, June 02, 2000	
6.00 – 7.00am	**Breakfast Buffet (Sun Deck)**
7.00am	**Arrival in Piraeus**

Session I

Growth of III-V Nitride Materials

Chair:
Dr. Colin Wood
Office of Naval Research, Arlington, VA, U.S.A.

To what extend should we reduce the defect density for GaN devices?

Pierre GIBART

CRHEA-CNRS, Sophia-Antipolis
F-06560 Valbonne

Abstract

Current heteroepitaxial GaN, grown on sapphire or 6H-SiC, is of poor quality. Numerous defects are identified:

- Residual donors (10^{16}cm^{-3}), O, Si, Ga$_i$, H, V$_N$
- Deep states: E1 (0.264 eV), E2 (0.580eV), E3 (0.665 eV) and the Yellow Luminescence around 2.2 eV
- Extended defects, Threading dislocation (TDs) (10^8-10^{11}cm^{-2}), Inversion domains, domain boundaries, stacking faults, nanotubes
- Native defects, V$_{Ga}$, N$_i$.

As a consequence of this huge density of defects the crystallographic and optical properties of such GaN are poor (FWHM of XRRC of about 300 arcsec, of PL ~3 meV). In spite of these drawbacks, efficient optoelectronic devices (LEDs, LDs and photodetectors) were fabricated and are presently on the market.

The limited effect on GaN-based high efficiency light emitting diodes of a surprisingly high density of TDs has led to considerable interest in determining their fundamental properties. Do these TDs introduce states in the gap? Do they limit the electron mobility? Do they limit device performances and lifetimes? are basic questions to be addressed.

Indeed, with the implementation of Epitaxial Lateral Overgrowth (ELO), which reduces the TDs density by 2 to 3 orders of magnitude, LDs with 10,000 hours lifetime were demonstrated. However, fabricating LEDs on ELO GaN does not improve their efficiency compared to standard GaN/sapphire or 6H-SiC.

Homoepitaxial GaN grown on GaN single crystals (obtained from high temperature-high pressure solution growth) exhibits extremely narrow PL linewidth (<0.1 meV). However, the present production of such crystals is too limited for the future industrial needs.

The required quality of GaN, in conclusion, is linked to the final device to be fabricated.

A Single Step Nucleation Process for Growth of GaN-Based Materials by OMVPE

J.A. Smart, and J.R. Shealy

Cornell University, Department of Electrical Engineering, Ithaca New York 14850, USA

Device quality GaN-based materials are grown by Flow Modulation Organometallic Vapor Phase Epitaxy. A novel single-step, high temperature nucleation process has been developed that produces planar films within the first several hundred Angstroms of growth on both sapphire and SiC substrates. Establishing a 2-dimensional growth front as early as possible is crucial to achieving insulating GaN films. Transistor structures are grown using undoped AlGaN barriers placed on top of the insulating GaN buffers, exploiting the strong polarization effects present at the heterostructure. A room temperature 2-dimensional electron mobility of 1695 cm^2/Vs with 1.1 x 10^{13} cm^{-2} sheet density has been measured on optimized structures.

Introduction

The synthesis of GaN and related alloys is accomplished by flow modulation techniques in a custom-built, cold-wall organometallic vapor phase epitaxial (OMVPE) reactor. A unique high temperature nucleation process using thin AlGaN films as been developed that produces atomically flat growth fronts on both sapphire and SiC substrates [1]. The introduction of aluminum in the high temperature nucleation layer aids in the uniform wetting of the substrate surface as opposed to three dimensional growth observed at similar temperatures with just GaN. This process simplifies the growth by eliminating large temperature ramps, while producing insulating GaN films with low background carrier concentrations ($\leq 10^{13}$ cm^{-3}).

Experimental

Undoped AlGaN/GaN heterostructures were grown on either *c*-plane sapphire or SiC (both 4H semi-insulating and 6H n$^+$) substrates, by flow modulation OMVPE at 76 torr. Flow modulation is accomplished by rotating the wafers through a group-III rich growth zone resulting in roughly a 25% duty cycle, while a background of ammonia is supplied for the remaining rotation period. By using this growth technique, our process is easily scalable for multi-wafer runs. Substrates were degreased in acetone and methanol, with the SiC additionally cleaned by the RCA method. All substrates were then subjected to an 1100°C anneal for 10 minutes under H$_2$ just prior to growth. Deposition temperatures were monitored by an optical pyrometer and fixed at 1040°C for sapphire and 1010°C for SiC. The V/III ratios were maintained at 900 and 1800 for AlGaN and GaN respectively. Reactant species used were triethylgallium, trimethylaluminum, and NH$_3$ with H$_2$ used as the carrier gas.

Results and Discussions

Conditions for successful nucleation varied substantially between sapphire and SiC substrates. A minimum Al content in the nucleation layer is required to create sufficient nucleation sites on the substrates to wet the entire surface. Compositions of at least 6 % and 15 % Al in the solid is required on SiC and sapphire respectively for smooth growth. Figure 1 shows a 4 μm x 4 μm plan view atomic force microscopy (AFM) image of a 200 Å thick Al$_{0.06}$Ga$_{0.94}$N nucleation layer on SiC. A 2-dimensional surface with atomic steps is easily observed with a rms roughness of approximately 0.4 nm. A threading dislocation density of 5 x 10^8 cm^{-2} is estimated from features in this image. This dislocation density is similar to those counted on GaN films subsequently deposited on the AlGaN nucleation layers, indicating that the threading dislocation density is determined by the nucleation layer. Similar images are observed using sapphire substrates with higher aluminum content.

When the minimum Al content in the nucleation layer is not achieved, 3-dimensional "island" growth occurs. The islands will eventually coalesce, resulting in a planar film. However, native defects from the meeting surfaces of the islands will contribute free carriers (electrons) to the epitaxial film. Figure 2 gives the derived carrier concentration profiles from capacitance-voltage (C-V) measurements of two different AlGaN/GaN/AlGaN/sapphire transistor structures. The profile depicted by the solid line is of a structure below the minimum require Al content in the nucleation layer, showing buried charge in the first 0.5 µm of the GaN buffer. The inset shows a nomarski micrograph of the GaN buffer layer with growth suspended in the charge region where voids indicating incomplete coalescence are clearly seen. For comparision, a structure using an optimized nucleation layer is shown by the dashed line without evidence of free carriers in the GaN layer.

Figure 1. Plan view AFM image of a 200 Å thick AlGaN nucleation layer on a SiC substrate

With optimized nucleation structures, uniform device quality epitaxial films are grown across 50 mm diameter SiC and sapphire substrates. Thickness uniformity of less than 10 % is measured across the entire wafer, and less than a 1% variation is seen in Al composition in AlGaN films. Large uniform areas of GaN-based epitaxial materials are necessary for large periphery devices and circuit applications. With optimized undoped AlGaN/GaN transistor structures, room temperature 2-dimensional electron gas mobilties of 1695 cm^2/Vs with 1.1×10^{13} cm^{-2} sheet density has been measured. The excellent electron transport properties at high sheet charge give low channel sheet resistances of around 325 Ω/square.

Figure 2. Carrier concentration profile derived from C-V measurements. Buried charge is evident in structure with below minimum Al content in the nucleation layer.

Conclusion

Insulating AlGaN nucleation layers and GaN buffers layers have been grown at high temperatures on both SiC and sapphire substrates. A simplified nucleation process using AlGaN thin films result in device-quality AlGaN/GaN heterostructure with high electron mobilities and 2-dimensional electron gas densities suitable for high power, high frequency transistor applications.

[1]   J. A. Smart, A.T. Schremer, N.G. Weimann, O. Ambacher, L.F. Eastman, and J.R. Shealy, Appl. Phys. Lett. 75, 388 (1999).

Nanoheteroepitaxy of GaN on Si

S. D. Hersee, D. Zubia, S.H. Zaidi, S.R.J. Brueck

University of New Mexico
Center for High Technology Materials
Albuquerque, New Mexico

Abstract for WOCSDICE 2000

This paper will discuss the theory and practice of Nanoheteroepitaxy (NHE), which is a new approach to the heterogeneous integration of III-V materials and devices with silicon. NHE theory [1] indicates that the combination of 3D stress relief (available to nanoscale islands [2]) and strain partitioning (between an epitaxial layer and a substrate) can dramatically extend the thickness of defect-free growth in mismatched heterostructures. NHE theory predicts that with the ~ 20 nm scale of patterning now available using advanced lithography [3]) we can eliminate strain related defects in heterostructures that are mismatched by up to ~4%.

Figure 1: The generic nanoheteroepitaxy sample exhibits partitioning of mismatch strain between the epilayer and substrate. The exponential decay of strain away from the heterointerface results from the 3-D stress relief mechanisms that are available to nanoscale islands.

In the generic NHE sample (figure 1) the substrate is patterned to produce nanoscale islands that are separated by a second material which promotes selective epitaxy. Heteroepitaxy begins as selective epitaxy onto the nanoscale islands. The 3D strain in both the epilayer and substrate quickly decays exponentially on both sides of the heterointerface. Importantly [1] the characteristic range of this decay is similar in size to the diameter of the nanoscale island, which is in the range 10 to 100 nm. Beyond this range, strain free epitaxial material is achieved and the growth conditions can then be modified to promote coalescence of the epilayer.

We are currently testing the NHE approach using GaAs/Si (4.2% mismatch) and GaN/Si (20% mismatch) heterostructures. In the case of GaN/Si the extreme mismatch (20%)

does not permit complete elimination of mismatch defects. However, the unique NHE sample configuration significantly modifies the defect structure at the heterointerface, creating "in-plane" defects rather than the conventional threading type dislocations.

This paper will describe the application of nanoheteroepitaxy to the growth of GaN on Si, and will include new results showing coalescence and will describe photoluminescence characterization of coalesced GaN films on Si (Figure 2).

Figure 2: Room temperature photoluminescence intensity versus thickness of GaN layer for three sample types. Nanoheteroepitaxial GaN on Si exhibits a significantly higher intensity that is sustained as the film thickness is increased.

Nanoheteroepitaxy is applicable to a wide range of strategically important semiconductor heterostructure materials, including; GaAs/Si, Ge/Si, GaN/Al_2O_3, GaN/SiC, GaN/Si, In-GaAs/InP. In each case the large lattice mismatch between the constituent materials currently places severe limits on the thickness of films or on the minimum defect concentration that can be achieved. NHE promises to remove these constraints and allow a much wider range of heterostructure materials to be grown on inexpensive, widely available substrates such as silicon.

[1] *"Nanoheteroepitaxy: A New Approach to the Heteroepitaxy of Mismatched Semiconductor Materials"*, D. Zubia, S.D. Hersee, J. Appl. Phys., **85** (1999) 6492-6496
[2] S. Luryi, E. Suhir, "New Approach to the High Quality Epitaxial Growth of Lattice-Mismatched Materials", Appl. Phys. Lett., 49 (1986) 140
[3] Saleem H. Zaidi and S. R. J. Brueck, *Nonlinear Process to Extend Interferometric Lithography,* Proc. SPIE, **3676** (1999) 371-378

NOTES
Session I: Growth of III-V Nitride Materials

NOTES
Session I: Growth of III-V Nitride Materials

Session II

Characterization of Heterostructure Devices and Transport Properties

Chair:
Prof. Hideki Hasegawa
Hokkaido University, Sapporo, Japan

Potential Profile Measurement of III-V Devices and Materials Using Kelvin Probe Force Microscopy

Takashi Mizutani and Yasuyuki Eguchi

Department of Quantum Engineering, Nagoya University, Nagoya, 464-8603 Japan
Tel: +81-52-789-5230, Fax: +81-52-789-5232, e-mail:tmizu@nuee.nagoya-u.ac.jp

Two-dimensional potential profile of InAlAs/InGaAs HEMTs and AlGaN/GaN epitaxial layers were measured using Kelvin probe force microscopy. High-field region at the gate edge of the drain side and inhomogeneous potential profile around the surface defect of the epitaxial layer were observed.

Introduction

The shrinkage of semiconductor devices to the submicrometer level has led to the need for the direct measurement of two-dimensional potential profile with nanometer scale resolution. Recently, we have demonstrated that Kelvin probe force microscopy (KFM) was successfully applied to the measurement of two-dimensional potential profiles of the GaAs devices under bias voltage [1],[2] and InAlAs/InGaAs heterostructures [3].

In this report, we describe the results of the potential profile measurement of InAlAs/InGaAs HEMTs and AlGaN/GaN epitaxial layers using Kelvin probe force microscopy.

Experimental

Figure 1 shows a schematic diagram of the KFM system [1]. KFM is similar to noncontact-mode atomic force microscopy (AFM). The system is equipped with two feedback loops to measure atomic force (z feedback) and the electrostatic force (V feedback: contact potential measurement).

Figure 2 (a) and (b) show the contour lines of the measured two-dimensional potential profile of the InAlAs/InGaAs HEMT at V_{GS} = -0.5 V. The sample used for the measurement was prepared by cleavage. The drain voltages V_{DS}'s are 0.2 and 1.2 V, which correspond to linear and saturation regions of the HEMT I-V characteristics, respectively. Even though relatively symmetric contour lines were obtained in the linear region, high-density contour lines were observed in the saturation region at the gate edge of the drain side, showing the formation of the high-field region at the gate edge. The results are similar to the previous results of GaAs HEMTs [1]. The formation of the high-field region was not so pronounced in the case of MESFETs, which was explained by taking into account the surface states [2].

Figure 3 shows the measured topographic image (a) and the corresponding contact potential image (b) of the wafer surface of AlGaN/GaN epitaxial layers on SiC. Concentric contact potential image with 1-2 μm diameter was obtained at the area where the surface defect was observed as shown in the figure. The potential around the surface defect is lower than other area except the center of the surface defect where potential peak is observed. These results suggest that the electronic properties of the area surrounding the surface defect are different from those of other area because the contact potential obtained by KFM reflects the work function of the material. Figure 4 shows the measured contact potential image of the cleaved surface. Even though the topographic image of the cleaved surface was sufficiently flat, inhomogeneous contact potential image which extended to the substrate was obtained as shown in the figure. This suggests that the concentric potential image of the wafer surface originates from the substrate, presumably being caused by the threading dislocations. Strain and/or stoichiometry change around the dislocation might be responsible for this inhomogeneous contact potential profile.

The KFM will become a powerful technique for microscopic characterization of various heterostructures and devices.

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Fig. 1 Schematic diagram of KFM measurement system.

(a)

(a)

(b)

Fig. 3 Measured images of AlGaN/GaN on SiC:
(a) topographic image and (b) the corresponding
contact potential image.

(b)

Fig. 2 Contour lines of measured potential profile of
InAlAs/InGaAs HEMT at V_{GS}= -0.5V for V_{DS}'s of (a)
0.2V and (b) 1.2V.

Fig. 4 Contact potential image of the cleaved surface
of AlGaN/GaN on SiC.

Electrical transport in highly resistive GaN layers

M. Morvic,[a] J. Betko,[a] P. Javorka,[b] J.M. Van Hove,[c] and P. Kordos[b]

[a]Institute of Electrical Engineering, Slovak Academy of Sciences, SK-84239 Bratislava, Slovakia
[b]Institute of Thin Film and Ion Technology, Research Centre Jülich, D-52425 Jülich, Germany
[c]SVT Associates, Eden Prairie, Minnesota 55344, USA

Four highly resistive MBE GaN layers, ρ_{300}=32–4.2×10^6 Ω cm, are characterized by temperature dependent conductivity and Hall effect measurements and analyzed considering band conduction, various types of hopping among defect centers, dislocation scattering and potential barriers at grain boundaries.

Introduction

There is a lack of information on the preparation and properties of highly resistive GaN layers. Carrier concentration and mobility data on samples with ρ_{300} >10^2 Ω cm are not present in literature, because of conductive substrates used [1], or no measurable Hall coefficient [2]. Hopping conduction is assumed to be responsible for the latter case. Additionally, models were proposed taking into account scattering on charged dislocations [3] and potential barriers at grain boundaries [4].

Experimental

The undoped GaN layers were grown on sapphire substrates by MBE using an RF atomic nitrogen plasma source. The layers are 2 μm thick and their crystallinity is nearly the same; the (0002) x-ray rocking curve FWHM is $\cong$7 arcmin. Samples of about 6×6 mm^2 were cut from each wafer and In-contacts were alloyed at 850 °C. The ohmic behavior of the contacts was confirmed by J–V characteristics. Accurate temperature dependent conductivity and low magnetic field (B=0.5 T) Hall effect measurements were carried out using a high-impedance system.

Results

Results obtained from the temperature dependent conductivity and Hall effect measurements on four highly resistive GaN layers are shown in Figs. 1–3. Data obtained can be well fitted considering ρ=C$_\rho$exp(E_ρ/kT), n_HT$^{-3/2}$=C$_n$exp(-E_n/kT) and μ_H=C$_\mu$T^x (the full lines), where C$_\rho$, C$_n$ and C$_\mu$ are temperature independent constants, E_ρ and E_n are activation energies evaluated from the resistivity and Hall concentration data, respectively, and x is a Hall mobility power.

For the sample 1 (ρ_{300}=32 Ω cm, n_H=6×10^{14} cm^{-3}, μ_H=305 cm^2/V s) activation energies E_ρ= 0.24 eV and E_n = 0.23 eV are obtained. Similar value of 0.20 eV has been reported recently for defect states in ion implanted GaN [5]. The Hall mobility power x = -1.4 follows from the fitting, which indicates that phonon scattering dominates in this sample. From the hopping analysis it cannot be determined whether single phonon (nearest-neighbor and variable range) or multiphonon hopping dominates.

For the samples 2 (ρ_{300}=2.3×10^3 Ω cm, n_H=7×10^{13} cm^{-3}, μ_H=32 cm^2/V s) and 3 (ρ_{300}=3.7×10^3 Ω cm, n_H=8×10^{13} cm^{-3}, μ_H=22 cm^2/V s) the same activation energies are found, E_ρ=0.29 eV and E_n =0.23 eV. The mobility power is positive, x=0.5 and 0.89 for the sample 2 and 3 respectively, which indicates a strong influence of dislocations on the electrical transport (x=1 for the scattering on charged dislocations [3]). Good agreement with experimental data can be also obtained considering the model of potential barriers at grain boundaries. In such a case the carrier concentration and mobility are thermally activated. An activation energy of 0.26 eV and barrier height of 0.02 eV are obtained. The hopping analysis does not gave satisfactory results.

Fig.1. Resistivity vs. 1/T for n-GaN layers.

Fig.2. $n_H T^{-3/2}$ vs. 1/T for n-GaN layers.

The sample 4 (ρ_{300}=4.2×10^6 Ω cm, n_H<1×10^{12} cm^{-3}, μ_H<1 cm^2/V s) shows very low Hall effect, not measurable seriously at room temperature. The activation energies are E_p= 0.50 eV and E_n = 0.36 eV. However, the mobility power is x=3.3, i.e. much higher than expected for the dislocation scattering. Further, also for this sample no reasonable results are obtained applying the hopping analysis. The best explanation of the electrical transport is that potential barriers at grain boundaries exist in this sample. An activation energy of 0.41 eV and barrier height of 0.11 eV are obtained. These values are in agreement with those reported previously on MBE GaN [4]. Indeed, AFM and REM diagnostics show crystallites with average diameter of 100 nm in this sample.

Fig.3. Hall mobility vs. T (log-log scale) for n-GaN layers.

Conclusions

Four highly resistive GaN samples were analyzed by temperature dependent conductivity and Hall effect measurements. Electrical transport in the samples 1, 2 and 3 can be well described by band conduction and the same donor-like defect level of 0.23 eV is found. However, in the two higher resistive samples a strong influence of dislocations (mobility power x=0.5 and 0.89) is observed. Transport in sample 4 is influenced by potential barriers at grain boundaries (crystallites with average diameter of 100 nm are observed using AFM and REM). Thus, the electrical transport of all the GaN layers investigated cannot be explained by the same model.

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Characterisation of 2DEG transport properties using Quantitative Mobility Spectrum Analysis

D. A. Redfern, J. Antozsewski, J. M. Dell and L. Faraone

Department of Electrical and Electronic Engineering,
The University of Western Australia, Nedlands, WA, 6907, Australia
email: redfe-da@ee.uwa.edu.au

Magnetic field dependent Hall and resistivity measurements contain information about the mobilities and carrier concentrations of all carrier species contributing to the conductivity. In recent years work on analysis techniques has matured to the stage where quantitative algorithms have proven extremely reliable, particularly mobility spectrum based procedures such as the Quantitative Mobility Spectrum Analysis (QMSA) of Vurgaftman, *et al* [1]. These techniques convert the experimental magnetic field dependent data into a continuous spectrum of constituent mobilities containing peaks for each of the electron and hole species present in the sample.

This work describes the application of mobility spectrum techniques to practical device structures in which two dimensional electron gases (2DEG) are known to contribute to the total conductivity. In particular, specific device structures will be considered that inhibit measurement of the Hall coefficient, such as FET structures, or modulation doped field effect transistors (MODFET's) typified by the emerging AlGaN/GaN HEMT technology for advanced high power and high temperature applications. In FET structures the Hall coefficient is not available for measurement and so electrons or holes responsible for the conductivity cannot be distinguished. However it is often known *a priori* that only electrons, or only holes, contribute to the transport mechanisms. Hence the Hall coefficient is not really necessary, and so magnetic field dependent resistivity measurements are all that are required to extract the mobilities and concentrations of each carrier within the channel and/or other carriers in associated layers.

The problem then becomes one of obtaining the conductivity density function, $s(\mu)$, representing the mobility spectrum of carriers, that satisfies the following integral equation.

$$\frac{1}{\rho(B)} = \sigma(B) = \int\limits_{0}^{\infty} \frac{s(\mu)}{1 + \mu^2 B^2} d\mu,$$

where $\rho(B)$ is the channel magnetoresistance. We use an algorithm similar to that outlined in [1], but modified to operate only on the conductivity tensor σ_{xx} and its derivative, to do the analysis. The mobilities of each of the carriers present can be read off the spectra and carrier densities are then easily obtained [2].

Figure 1 shows the results of an application of the technique to an $Al_{0.3}Ga_{0.7}As/GaAs$ HEMT at 300K. The advantage of using QMSA is highlighted by the appearance of low mobility carriers which correspond to transport in the n^+ donor layer which is not fully depleted in this sample. The ability to determine the presence of such donor layer parallel conduction without prior assumption or the need to test FET performance is an important advantage for the QMSA approach [3].

The application of this technique to an $Al_{0.25}Ga_{0.75}N/GaN$ MODFET at 233K is shown in Figure 2 which clearly shows the typical relationship between sheet concentration of the 2DEG and its associated mobility. The lower than expected mobilities have since been shown to be a result of high interface roughness.

Acknowledgements

Figure 1: Channel conductivity versus magnetic field and associated mobility spectrum, in sheet density format, for the $Al_{0.3}Ga_{0.7}As/GaAs$ HEMT at 300K.

Figure 2: 2DEG mobility versus 2DEG density for $Al_{0.25}Ga_{0.75}N/GaN$ MOD-FET at 233K.

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Session II: Characterization of Heterostructure Devices and Transport Properties

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Session II: Characterization of Heterostructure Devices and Transport Properties

Session III

Processing and Packaging

Chair:
Prof. David V. Morgan
Cardiff University, Cardiff, Wales, UK

One-Step Patterning of Asymmetric Gate Recess for InP HEMTs using Genetic Algorithms

Franck Robin, Andrea Orzati, Esteban Moreno, Michael Spühler, Otte Homan and Werner Bächtold

Swiss Federal Institute of Technology (ETH) Zürich
Laboratory for Electromagnetic Fields and Microwave Electronics
CH-8092 Zürich, Switzerland, e-mail: robin@ifh.ee.ethz.ch

For the first time, a canonical genetic algorithm was used to optimize the resist profiles for T-gate fabrication. An e-beam lithography simulation tool was elaborated that calculates the two-dimensional resist profile as a function of the electron dose. A resist profile was optimized for asymmetric gate recess fabrication of InP HEMTS to enhance the breakdown voltage.

Introduction

The reduced dimensions of semiconductor devices for high-frequency applications necessitate the use of e-beam lithography steps for the submicron T-shaped gate definition of FETs [1]. T-gates allow high cutoff frequency f_T and low gate resistance. Methods have been devised to fabricate FETs with an asymmetric gate recess in order to enhance the power performances of GaAs HEMTs [2]. Simulation tools of the e-beam lithography step for gate fabrication have been developed [3]. To date, however, few studies have been done to optimize the resist profiles. We used a genetic algorithm (GA) to improve the resist exposure and development process.

The 4-layer resist system was as follows (from bottom to top): 100 nm-thick PM(MA/AA) copolymer, 120 nm-thick PMMA-950K, 350 nm-thick PM(MA/AA) and 80 nm-thick PMMA-50K.

Resist profile simulation of a symmetric T-gate

The electron dose corresponding to a given exposure pattern was first determined by taking the backscattered electrons into account. The backscattered electrons efficiency on InP substrates was 1.35. Fig. 2 shows the input 1D e-beam scan pattern expressed in dwell time for a symmetric T-gate definition and the associated dose. The resist profile was computed by calculating the local solubility for each point of the development front (Fig. 1) and propagating the development front (initially set at the top of the outermost resist layer) through the resist stack. Fig. 3 shows the resulting symmetric T-gate resist profile.

Optimization of an asymmetric gate recess with Genetic algorithms

A "canonical" GA was used to find optimal dwell time distributions for a goal resist profile [4]. A starting random population of 100 dwell distributions was used. SEM-related physical constraints (min. and max. dwell times) were introduced. A target profile was defined and the fitness of each individual after development was calculated as the reciprocal of the euclidian distance between goal and calculated profiles. For each iteration of the GA, two offsprings were generated by choosing two individuals from the population with a selection probability proportional to the fitness. N-point crossover and a mutation probability of 1 bit/string were implemented. Fig. 4 shows the fitness evolution for an asymmetric gate structure after 23000 generations and Fig. 5 and 6 show the scan pattern and the associated developed resist profile of the best individual after optimization, respectively. The optimization yields a resist profile in very close agreement with the specifications.

Conclusion

We designed a resist development simulation tool using genetic algorithms to optimize the resist profiles. This new tool promises to greatly facilitate the design of exposure patterns for complex structures such as asymmetric T-gates.

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Fig. 1: Measured development rate vs. dose for the PMMA 950 K, PMMA 50 K and PM(MA/AA) resists

Fig. 2: Example of dwell time and corresponding dose along the gate length

Fig. 3: Developed structure obtained with the dose shown on Fig. 1. Lines represent the developed structure with 5 s intervals

Fig. 4: Fitness evolution for an asymmetric gate optimization after 23000 iterations (two offsprings/ iteration). Each point represents an offspring

Fig. 5: Scan pattern of the best individual. The exposure is composed of four superposed main patterns (boxes are guides for the eyes only)

Fig. 6: Optimized resist profile and target profile (solid line)

DAMAGE OF InP SURFACES BY RIE PROCESSING

H. C. Neitzert[1], R. Fang[2], M. Kunst[3], and N. Layadi[4]

[1] *Università di Salerno, DIIIE, Fisciano, Italy,*   [2] *Centro Studi e Laboratori Telecomunicazioni, Torino, Italy*
[3] *Hahn-Meitner-Institut, Berlin, Germany,*   [4] *Bell Laboratories, Lucent Technologies, Orlando, USA*

Combined electrochemical capacitance-voltage (C-V), current-voltage (I-V) and noninvasive transient microwave conductivity (TRMC) measurements have been performed to assess RIE (CH_4:H_2 - plasma) induced damage on InP. For n-InP after RIE an increased electron concentration is found in a thin surface layer and a 50% reduced electron mobility is measured. On a RIE treated p-InP sample an n-type behavior at the surface, indicated also by a sharp mobility increase has been found due to the formation of a surface inversion layer. TRMC measurements enabled to draw the same conclusions as obtained by C-V and I-V measurements.

Introduction

Reactive Ion Etching (RIE) has been used as a main etching technique for processing InP based devices. Due to its working mechanism, damages may be induced during the etching process which compromises device performance [1,. There has been evidence that InP is more sensitive to plasma etching induced defect creation than GaAs [2] and the characterization of the RIE induced surface modifications is therefore of high importance for the optimization of etching and annealing processes. Many studies on RIE induced damages have been reported, including investigations on surface chemistry [1], carrier concentrations near the surface[1,3] carrier mobilities [4] and junction leakage current [5]. Here we compare results regarding the surface modification as determined by charge carrier profiling using electrochemical capacitance-voltage (C-V) measurements to changes of charge carrier mobility kinetics obtained by transient reflected microwave conductivity (TRMC) measurements after RIE processing of InP samples using CH_4 and H_2 etching chemistries. The TRMC technique [6] is based on the change of the microwave reflection of a semiconductor due to changes in the free carrier concentration as induced by the absorption of photons. It enables to determine the excess charge carrier mobility and additionally gives information regarding the charge carrier kinetics. In an earlier study this latter technique has already been employed to assess the damage of Si surfaces after He and H_2 plasma exposures [7].

Experimental and Results

The characterized samples were <001> epi-ready n-InP (S-doped to 1-2 10^{18}/cm^3) and p-InP (Zn- doped to 2 10^{18}/cm^3) substrates for electrochemical C-V measurements. The samples for TRMC measurements were semi-insulating InP:Fe substrate and CBE grown n-InP and p-InP with both the doping levels in the order of 10^{17}/cm^3. The samples were etched by RIE using a CH_4:H_2 (5:20 sccm) mixture, at a reactor pressure of 10mTorr and an input RF power of 150W, for 10min.

The results of the electrochemical C-V measurements measured on n-InP substrate (Fig.1a) show that compared to a unetched reference sample the electron concentration after RIE treatment is increased in an approximately 25nm thin surface layer. This can be attributed to a depletion of phosphorous atoms near the surface. The voids of phosphorous atoms act like "donor" and contribute to the increase of electron concentration. A 1min anneal of the RIE processed sample at 400°C in Ar, reduces the electron accumulation layer width from 25nm to less than 10nm. The I-V characteristics before and after RIE treatment (Fig.1b) - as monitored during C-V profiling - shows that the contact barrier height for the dry-etched sample is lower than that of the reference sample, caused by the increase of the electrons concentration near the surface. To study the modifications of carrier concentrations and mobilities after the RIE process, we measured the TRMC signals with an exciting laser wavelength of 532nm, which is strongly absorbed at the sample surface (Fig.2b). The effective electron mobility of the reference sample is 1500 cm^2/s. After 10 min dry-etching, the electron mobility is reduced to 1200 cm^2/s. The effective electron mobility is reduced further down to 750 cm^2/s, after an 1min, 400°C anneal in Ar ambient. After RIE treatment, a fast initial decay can be observed that is absent on the reference sample transients up to 40ns The 1min Ar anneal leads again to a decay behavior (< 50ns), very similar to the one observed for the reference sample. On a longer time-scale, however, the RIE treated sample shows a much slower decay rate compared to the as grown and to the annealed sample. This can be explained by the suppression of fast surface recombination due to the strong band bending at the surface after RIE treatment.

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The TRMC signals measured on p-InP samples are presented in Fig.2a. The effective mobility of the reference sample is about 50 cm^2/s; after RIE process, the effective mobility is increased up to 700 cm^2/s and after a subsequent annealing for 1min at 400°C in an Ar ambient it is again reduced to 75 cm^2/s. After annealing the inversion layer is removed, the material recovers at the surface as a weakly p-doped sample and the effective mobility again reflects the lower hole mobility. This has also been confirmed by C-V measurements, where a surface depletion layer with a width exceeding 25nm has been found after RIE treatment and by I-V measurements, where the contact barrier height for the dry-etched p-InP sample is higher than that of a reference sample due to the decrease of the hole concentration near the surface.

In summary, electrochemical C-V and I-V and TRMC measurements have been performed to assess the RIE induced damages on InP samples. The measured results indicate that after RIE process: (a) the surface carrier concentrations have been changed, which also has influence on the contact barrier, as determined by I-V measurements. For example, on a dry-etched n-InP sample there is an accumulation of electrons (thus a lower contact barrier) while on a dry-etched p-InP sample there is a depletion of holes near the surface (thus a higher contact barrier). (b) the charge carrier mobilities and kinetics have been modified. On a dry-etched n-InP sample the electron mobility is reduced to 50% of its original value. On a dry-etched p-InP sample a weakly n-type behavior at the surface after RIE has been observed. After a 1min Ar anneal the p-type behavior is restored.

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Fig.1 a) Charge carrier concentration measured by electrochemical C-V technique (a) and I-V characteristics (b) as measured on RIE treated and not etched reference n-InP samples

Fig.2 a) TRMC-transients after excitation with a 532nm pulse laser, measured on an unetched reference sample, a RIE treated sample and a RIE treated and subsequently Ar annealed sample. a) for p-InP and (b) for n-InP

3D. ULTRA THIN CHIP STACKING : METHODS AND RESULTS

J.P. Bailbé, S.Pinel, J.Tasselli, A.Marty

Laboratoire d'Analyse et d'Architecture des Systèmes du CNRS
7,Avenue du colonel Roche 31077 TOULOUSE Cedex – France
E-mail : bailbe@laas.fr

Abstract : 3D integration of chips to form multi-chip stacks is a very active area of research all over the world. One possible way is the ultra-thin stacking technology that is of interest for all electronic industries where size and weight are important for product acceptance.(telecom, portables computer, medical implant, avionics, aerospace etc..). This new integration technique can be described as follows: chips are thinned down to 10µm and then, using planarisation techniques as used in semiconductor processing, the 3D stack is formed on a silicon substrate by depositing layers of dielectric onto which a metallisation pattern is formed. The thinned chips are placed on top of each dielectric layer and the vertical interconnection is achieved with metallized vias. (Figure1)

1)Introduction

In this paper we present the method we have developed to thin dice up to 10 µm and to transfer them onto host substrates for further applications. This opens up new domains for MCM structures as devices weight and volume can be decreased so increasing the 3D yield, and offers possibilities to use flexible substrates for applications such as artificial skins for example. (The main benefit of the presented technique is that it can be applied irrespective of the devices, circuits or materials used). After a detailed description of the thinning method, we present examples of electrical results obtained on thinned conventional devices such as MOS transistors or bipolar devices, on Si or GaAs material.

2)Thinning method

The problem is to mechanically lap semiconductor materials until thickness around 20 µm avoiding chipping of the die edges. So, the thinning method to be used has to secure the die while ensuring a thickness uniformity of +/-1µm over the wafer. To satisfy these requirements, we have developed a technique where the dummy device is glued through its front side into a cavity firstly etched on a 3'' silicon wafer, acting as a chip carrier, and not directly glued on the specific chuck of the lapping machine. The cavity depth is typically fixed to 20 µm and its role is to protect the edges of the sample when the lapping reaches low thickness. Mechanical lapping is stopped when the edges of the cavity start getting etched thus showing the expected 20 µm are reached on the die. The remaining microns of material are then removed by Reactive Ion Etching (RIE), until a final thickness of about 10 µm, depending on the different devices processed. The next step is the transfer of the thinned die onto a host substrate. The principle of the thinning and report is shown on figure 2 .

3) Transfer of the thinned device

A 10 µm-thick sample cannot be easily handled. Thus the cavity-wafer acts as a holding tool allowing the transfer of the die onto the host substrate without damaging it. After polishing, the cavity wafer is sawed around the die. To make the attachment on the host substrate (Silicon for example), it is necessary to use a glue which thermal properties in terms of curing temperature are different from those of the wax used for lapping. This insures a perfect selectivity and allows attachment on the glue side while ungluing on the wax side. We have used several low viscosity epoxy and polymer those can be spun to reach thickness of 2 to 3 µm.

The transfer procedure is as follows: the host substrate first covered by epoxy or polymer is placed on the heating chuck of the die transfer machine : curing is performed. The sample and its carrier are placed on the holding head of the machine and transferred to the epoxy layer with a constant pressure applied thereby hardening the epoxy .The whole temperature is then raised in order to melt the wax and detach the cavity-wafer from the die. A simple acetone cleaning removes the wax residues on the front side of the die without affecting the epoxy layer.

4) Electrical results

The thinning process that we have developed was first optimized on bulky silicon samples. We then performed thinning on devices and circuits. The first tests made on MOS transistors were satisfactory. Output characteristics first measured before the thinning process (Figure 3.a) were not really altered after the thinning and transfer process as shown in Figure 3.b.

The process was also tested on power GaAs-heterojunction bipolar transistors (HBT's). In this case, the main difficulty is related to the non planar GaAs technology used i.e. delimitation of the different junctions by mesa and thick Au-air bridge onto the emitter. After the transfer procedure, no degradation was observed optically on the 15 µm-thick HBT structure. The (I_C, V_{CE}) characteristics measured under probes before and after thinning do not show significant changes in terms of current gain and offset voltage (see Figures 4.a and 4.b).

5) Conclusion

The original presented method allows to thin down to 10 µm, handle and transfer onto host substrates various commercial or not devices with a reduced equipment. First results obtained on thinned Si-MOS transistors and GaAs-HBT's did not show electrical degradation and highlighted the achievability of this technique. Complementary studies have to be done to evaluate the reproducibility and the reliability of the presented method, and define with much more accuracy the impact on the electrical performance.

Figure 1:Principle of UTCS

Figure 2 : Principle of the thinning and report method

a)   b)   a)   b)

Figure 3 : output characteristics (Id,Vds) of
(a) an Si-MOS transistor before thinning,
(b) (b) a 9 µm thick MOS

Figure 4: output characteristics (Ic,Vce) of
(a) an power GaAs HBT before thinning,
(b) a 15 µm thick HBT

Figure5 : View of a 10µm-thick silicon wafer through a glass support

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Session III: Processing and Packaging

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Session IV

GaAs, InP-based HEMTs and Ballistic, Hot Electron Effects

Chair:
Prof. Lester F. Eastman
Cornell University, Ithaca, NY, U.S.A.

HEMT structures on GaAs or InP substrates for millimeter wave power amplification.

D. Théron, Y. Cordier, X. Wallart, S. Bollaert, M. Zaknoune, M. Boudrissa, B. Bonte, C. Gaquière, F. Mollot, A. Cappy, R. Fauquembergue and J.C. De Jaeger.

Institut d'Electronique et de Microélectronique du Nord, UMR CNRS 8520
University of Lille 1
Avenue Poincaré, B.P. 69
59652 Villeneuve d'Ascq Cedex, FRANCE

This paper reviews the status of HEMT structures deposited on GaAs or InP for millimeter power amplification. Starting from AlGaAs/InGaAs PHEMTs, the recent innovations concerning materials and technologies will be described such as metamorphic devices or the use of phosphides.

Introduction.

Today, double heterostructure AlGaAs/InGaAs HEMT's on GaAs substrates are most widely used for power amplification in millimeter wave range. Among the best results published in the literature, you can find a 0.3×70 μm^2 device demonstrating 1 W/mm at 33 GHz with 38 % power added efficiency (P.A.E.) and 3.7 dB power gain [1]. At 60 GHz a device with 0.15 µm gate length and 50 µm gate width ($0.15 \times 50 \ \mu m^2$) [2] has shown 0.84 W/mm, 37 % power added efficiency and 5.9 dB power gain. At 94 GHz this device has shown 0.43 W/mm, 19 % P.A.E. and 3.2 dB power gain. These HEMTs present the best power density above 30 GHz (figure 1a) and have a gain which is limited by the electron dynamics in the channel (figure 1b).

Any improvement in the gain will require the use of higher indium content in the channel. This can be achieved with AlInAs / GaInAs on InP where lattice matched InGaAs contents 53% indium. Thus with a gate length of 0.15 µm, 0.4 W/mm with 3 dB power gain were obtained at 59 GHz [3]. This structure uses AlInAs strained in tension with 60 % aluminum in order to ensure a good Schottky barrier height and breakdown. A better result has been obtained on a 0.1 µm gate length HEMT with 0.41 W/mm, 8 dB power gain and 45 % P.A.E [4]. With a double heterostructure pseudomorphic channel structure (67% indium in the channel) the results are 0.48 W/mm, 4.4 dB power gain and 30 % P.A.E. [4]. Since then, to our knowledge, these results have not been improved.

Figure 1 : Power density and gain versus frequency for different microwave power FETs.

Present breakthroughs.

The reason for lower output power of AlInAs / GaInAs HEMTs on InP is the low drain bias they can withstand [5]. This is due to the lower on-state breakdown voltage of these devices as compared to PHEMTs on GaAs. This comes from the increase of impact ionization in the InGaAs channel as the indium content rises. A lot of work has been performed on breakdown in these devices [6,7] in order to have a better understanding of the physical mechanisms. It shows that the compromise between frequency capability and output power can be overcome by carefully optimizing the device structure (barrier layer, channel) and technology (recess, passivation).

A first approach to increase the gain of PHEMTs on GaAs consists in using metamorphic material in order to have the freedom to choose the indium content in the device structure. This technology presents the advantage of combining high electron velocity and high breakdown voltage [8]. However the interesting indium rates for power are in the range 30 to 40 % which means that InAlAs will be Al rich and very sensitive to oxidation. Moreover these devices can hardly be biased at high drain voltage if the gate technology is not carefully optimized. Nevertheless excellent results have been recently demonstrated in the US [9] at 35 GHz using AlGaInAs as a barrier layer and double recess. These HEMTs present a great potential for power amplification (figure 2).

On InP, composite channel have been used for improved power capability [10]. The addition of an InP back channel under the InGaAs layer aims to reduce the impact ionization of hot electrons by forcing them to travel in InP. This concept allows to increase the on state breakdown voltage [11,12]. 380 mW/mm have been achieved at 60 GHz with 4 dB gain and 30% P.A.E. [13].

Another way of investigation is the incorporation of phosphide semiconductors in the HEMT structure on GaAs. AlGaInP used as barrier layer presents several advantages over AlGaAs or AlInAs. Its wide band gap can be adjusted to be higher or lower than the AlInAs gap depending on the Al and In composition (figure 3). It will present a large valence band offset with InGaAs. This will prevent holes created by impact ionization in the channel from going towards the gate. From a technological point of view the excellent etching selectivity between arsenides and phosphides allows a careful control of the recess depth and width which is important for multi finger power device realization. Some results have been obtained up to now in this field. For instance, we have realized GaInP/GaInAs single heterojunction HEMTs with single recess [14]. At 60 GHz 560 mW/mm have been measured with 22.5 % P.A.E. and 4.6 dB power gain. This is the best result obtained at 60 GHz on this structure. Further optimization should be possible using double heterostructures or metamorphic material.

Figure 2 : Comparison of PHEMTs on GaAs and InP substrates with metamorphic HEMTs.

Perspectives.

Power devices still require many improvements for operation at millimeter wave frequencies. Careful investigation is needed due to the large number of critical parameters. Metamorphic material has already opened new ways of structures. Other innovative semiconductor technology could help to progress in that field such as the use oxides or antimonides.

Figure 3 : The band gap of phosphides in comparison to arsenide semiconductors.

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Enhancement-mode metamorphic $Al_{0.67}In_{0.33}As/Ga_{0.66}In_{0.34}As$ HEMT on GaAs substrate

M. Boudrissa, E. Delos, Y. Cordier, D. Théron, and J.C. De Jaeger

Institut d'Electronique et de Microélectronique du Nord (IEMN)
Département Hyperfréquence et Semiconducteurs
Université des Sciences et Technologies de Lille
59652 Villeneuve d'Ascq Cedex-France

We present an experimental quantification of improvements provided by combination of Enhancement-Mode (E-mode) with metamorphic growth of $Al_{0.67}In_{0.33}As/Ga_{0.66}In_{0.34}As$ HEMT structure on a GaAs substrate. The devices, which are the first reported for Enhancement-Mode $Al_{0.67}In_{0.33}As/Ga_{0.66}In_{0.34}As$ MM-HEMT's, exhibits good dc and rf performance. The Schottky characteristics have a forward turn-on voltage of 0.9 V and a typical reverse gate to drain breakdown voltage of 16 V. The 0.4µm gate length devices have a saturation current of 335 mA/mm at 0.6V gate voltage.

We have used an inverse step-graded buffer of AlInAs [1,2] and we benefit of the indium composition close to 30%. The high ΔE_c of 0.7 eV leads to high sheet carrier density and good confinement [3]. The high bandgap of InAlAs and InGaAs as compared to higher indium content, allows respectively a good Schottky barrier height which improves breakdown voltage and reduces the impact ionization.

The layers were grown on (100)-oriented GaAs substrate using a Riber 32P Molecular Beam Epitaxy machine. By increasing Al content in the upper Schottky layer, we aim at increasing the gate Schottky barrier height, thus improving the gate-to-drain diode breakdown voltage. A cross section of the material layer structure is shown in figure 1. Hall effect measurements are used to determine the sheet carrier density n_H and electron mobility μ_H. They are, respectively, $3.9 \times 10^{12} cm^{-2}$ and $7000\ cm^2/V.s$ at room temperature (300K).

The fabrication started with the realization of source and drain ohmic contacts. For the ohmic contact formation, using Ge/Au/Ni/Au metalisation and rapid thermal annealing at 340°C during 60s under N_2/H_2. TLM (Transmission Line Model) measurements show a typical ohmic contact resistance R_c of 0.20 Ω. Device isolation was performed by non selective chemical mesa etching down to the AlInAs buffer layer with $H_3PO_4/H_2O_2/H_2O$ (5:1:40) etchant. The T-gate was defined using a bilayer resist (PMMA/P(MAA-MAA)) to improve lift-off. After the chemical recess using a selective etchant (succinic acid:H_2O_2), the gate metallization is e-beam evaporated and consists of Ti/Pt/Au sequence. The etching selectivity ratio of InGaAs over AlInAs was greater than 500. Typical Schottky characterization gives an ideality factor η of 1.7 and a Schottky barrier height Φ_b of 0.75 eV. As the final step, thick Ti/Au contacts were deposited for microwave probing pads. The good results in the Schottky diode are in a large part attributed to well controlled recess process. The devices present no kink effect. DC and microwave characteristics of 100µm wide MM-HEMT's were measured on wafer. The I-V characteristics are given in figure 2. The devices exhibit a drain-to-source current I_{ds}= 335mA/mm at a gate-to-source voltage V_{gs} = 0.6 V. The pinch-off voltage V_p is -0.3V. Typical extrinsic transconductance and output conductance are 510 mS/mm and 13.5 mS/mm which gives an extrinsic gain voltage gm/gd of 38. S-parameter measurements were carried out and current gain cut-off frequency f_T were estimated. An extrinsic current cut-off frequency f_T of 62GHz and cut-off frequency f_{MAG} of 72GHz are achieved with the 0.4µm gate length device. They have been obtained at maximum transconductance bias condition (Vds = 2 V and Vgs = 0.3 V). The Schottky characteristic curve for device with L_g = 0.4 µm is shown at figure 3. A forward turn-on voltage of 0.9 V and a typical gate–to-drain voltage of –16 V at the gate current of 0.5 mA/mm were obtained. We also obtain (figure 4), for different source to drain extension, a maximum output power versus input power. The larger is the extension, the higher is the maximum output power. We obtain 110mW/mm for a large extension while we have only 40mW/mm for a narrow extension. We have also 65mW/mm for a medium extension.

Metamorphic devices exhibit good Schottky diode breakdown voltage. Our results strongly suggests that the optimization of the gate to drain extension will improve output power. The enhancement mode (E-mode) device is more interesting since it eliminates the need for a negative voltage supply on a chip. These results are the first reported for an Enhancement-Mode MM-HEMT's with this indium composition and present

better results as compared to those with an indium composition of 50% [4] in term of breakdown voltage. So it confirms the great interest of MM-HEMT over PM-HEMT by the superiority of the electron transport properties due to the high relaxation rate and the good filtering of dislocations.

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Figure 1 : Schematic of Simple Heterostructure-HEMT structure on GaAs substrate with the indium composition profile

Figure 2 :DC I-V characteristic of a normally-off MM-HEMT with a gate of 0.4x100µm. Gate voltage maximum is 0.6V and gate voltage step size is 0.2V.

Figure 3 : Schottky characteristic of a normally-off MM-HEMT. The devices width is 100µm with T-shaped gate length L_g = 0.4µm. The inset represents the forward Schottky characteristic.

Figure 4 : Load-pull power characteristic at 10GHz for three source to drain extensions of a E-mode MM-HEMT (V_{ds}=3V and V_{gs}=0.4V)

MODFET channel conductivity with high doping level

K. Pozela, J. Pozela, V. Juciene

Semiconductor Physics Institute. A. Gostauto 11, 2600 Vilnius. Lithuania

A strange effect: the decrease of MODFET channel conductivity with increasing the electron concentration due to the great increase of the electron–polar optical phonon scattering rate is observed

Introduction

In modulation-doped field-effect transistor (MODFET) structures, a spatial separation of carriers from their parent donors increases electron mobility and enables a modulation doping level with donors and, consequently, electron concentration in a MODFET channel to be enhanced.

In this paper, the factors responsible for limitation of MODFET channel conductivity enhancement with increasing sheet electron concentration are considered.

Electron mobility limited by electron–polar optical phonon scattering

Using the dielectric continuum approximation [1], the calculations of scattering rates of confined electrons by confined polar optical (PO) phonons depending on sheet electron concentration in the $Al_{0.25}Ga_{0.75}As/GaAs/Al_{0.25}Ga_{0.75}As$ QW are performed. Taking into account the electron degeneration, the scattering rate of an electron from the initial state in subband i with the energy E to final states in subband f with the energy $E \pm \hbar\omega_v$ is written as

$$W_{if}(E) = \sum_v W_{ifv}^e \frac{1 - f(E - \hbar\omega_v)}{1 - f(E)} + W_{ifv}^a \frac{1 - f(E + \hbar\omega_v)}{1 - f(E)} , \qquad (1)$$

where $f(E)$ is the Fermi-Dirac distribution function, the superscripts e and a correspond to the phonon emission and absorption, respectively. The inverse electron life time τ_i in the state E of subband i limited by optical phonon scattering can be determined as

$$\frac{1}{\tau_i(E)} = \sum_f W_{if}(E) . \qquad (2)$$

For estimation of the electron mobility limited by PO phonon scattering we involve the life time $\tau_i(E)$ as momentum relaxation time. Then the mobility in subband i is determined as

$$\mu_i = \frac{e}{m} \left\langle \frac{1}{\tau_i(E)} \right\rangle^{-1} , \qquad (3)$$

where the brackets $\langle \; \rangle$ mean the averaging over energy. The electron mobility in the QW is

$$\mu = \sum_i \mu_i \frac{n_{si}}{n_s} , \qquad (4)$$

where n_{si} is the concentration of electrons in subband i and the sheet electron concentration $n_s = \sum_i n_{si}$.

In Fig. 1 the calculated electron mobility μ as a function of sheet electron concentration n_s in the $Al_{0.25}Ga_{0.75}As/GaAs/Al_{0.25}Ga_{0.75}As$ QW is presented.

One can see that taking into account only electron–PO phonon scattering the decrease of electron mobility at 100 K exceeds the sheet electron concentration increase in the range of $n_s =(6-10)\times10^{15}\text{m}^{-2}$. As a result, the heterolayer conductivity (represented in Fig. 1 as the mobility multiplied by the electron concentration: $\mu\, n_s$) decreases with increasing the electron concentration in the layer.

The alternate increase and decrease of the calculated channel conductivity $\mu\, n_s$ with increasing n_s are observed. The channel QW conductivity of MODFET can be increased by increasing the doping level. The conductivity when $n_S = 2.5\times10^{16}\ \text{m}^{-2}$ exceeds the conductivity at $n_S = 6\times10^{15}\ \text{m}^{-2}$.

Each cycle of the alternate decrease-increase conductivity change with increasing n_S corresponds to the change of the Fermi level position E_F with respect to the QW subband energy level E_s In the $Al_{0.25}Ga_{0.75}As/GaAs/Al_{0.25}Ga_{0.75}As$ QW at 100 K, the Fermi level crosses two subband energy levels when the sheet electron concentration changes from $n_S =10^{15}\ \text{m}^{-2}$ to $n_S =10^{17}\ \text{m}^{-2}$. Correspondingly, two conductivity increase-decrease cycles are observed (see Fig. 1).

Fig. 1. Mobility μ and conductivity $\mu\, n_s$ in $Al_{0.25}Ga_{0.75}As/GaAs/Al_{0.25}Ga_{0.75}As$ QW with inserted thin barrier (solid lines) and without it (dashed lines) at 100 K as functions of sheet electron concentration n_s

The insertion of a thin AlAs barrier into the GaAs QW center changes the electron subband energies. This admits a possibility for increasing the doping level and the maximal channel conductivity (see Fig 1).

Conclusions

These calculated maximal doping limits determinate the possibilities of enhancement of high-speed parameters for $Al_{0.25}Ga_{0.75}As/GaAs/Al_{0.25}Ga_{0.75}As$ MODFETs.

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Two-stream ballistic instability in two-channel field-effect transistors.

Z. S. Gribnikov , N. Z. Vagidov, and V. V. Mitin

Department of Electrical and Computer Engineering, Wayne State University,
Detroit, Michigan 48202, USA

In this study we investigate in detail dispersion relations $\omega(k)$ of two-stream plasma waves in modulation doped gate-controlled current-conducting channels. To protect two-stream instability and two-stream induced generation regime for high electron concentrations we suggest and analyze two-channel structures with separately contacted parallel current-conducting channels and separated electron currents in them. These separated currents in the channels appear as the streams to develop oscillatory regimes. Electron-electron pair interaction between different channel electrons is attenuated since the channels are spatially distanced. (It is similar to attenuation of electron-ion interaction as a result of modulation doping.)

Two groups of current carriers naturally coexist in the quasineutral regions (QRs) of the base of ballistic diodes and field-effect transistors (FETs). They are : 1. traversing ballistic current carriers emitted by a source and absorbed by a drain, and 2. nontraversing (nonparticipating in a current flow) carriers, which are in the equilibrium with the drain current reservoir. As a result of interactions between these carrier streams a two-stream instability appears and develops in such diodes and FETs if they have appropriate material and geometrical parameters.

The 2-SI is a result of collective plasma oscillations of both above-mentioned carrier groups. In this work we study analytically dispersion relations for the 2-SI in the QRs of the ballistic diodes and FETs and consider numerically development of this instability in the short-base diodes and FETs.

We show that both for diodes with bulk bases and for diodes with conducting channel bases development of the 2-SI leads to oscillating regimes with oscillation frequencies > 1 THz (up to $2.5 \div 3$ THz) if the base length is or of order $0.15 \div 0.2$ μm. Both for the diodes and for the FETs there are threshold voltages V_{max} , which limit above voltage ranges of oscillations. For FETs this threshold voltage is close to the saturation voltage (that is , the 2-SI oscillatory regimes are possible at the saturation).

The main problem which must be solved to implement 2-SI terahertz generators is blocking pair electron-electron interactions between electrons from different streams (groups). We have to protect their collective plasma interaction and to avoid their pair (fluctuative) interaction (scattering). This scattering leads to energy and momentum exchange and transforms two streams into a single united stream. As a result we lose the 2-SI. To avoid this undesirable fact we suggest to reconstruct a design of ballistic FET: to replace metallic gates by semiconductor gates with electron concentration which is approximately equal to the concentration of mobile (traversing) carriers in the main channel at saturation regime. This design allows obtaining a certain FET structure with mobile (traversing) electrons only in the main channel (the 1-st stream) and with immobile electrons in the additional channel (that is, in the semiconductor gate). These nontraversing electrons form the 2-nd stream. Plasma interaction between streams occurs across the barrier layer of width d, and it is effective for $kd < 1$, if the base length is much greater than d, and it is sufficiently effective for all actual k. The pair scattering is of shorter range and can be suppressed (similarly to the well-known suppression of electron-ion scattering at the modulation doping). The dependence of the interlayer electron-electron scattering on the distance d is known in great detail from the works on interchannel electron-electron drag. The inverse characteristic time τ_D^{-1} of this scattering decreases with d at least as d^{-4}.

The simplest dispersion equation describing the studied two-stream interaction for the considered two-channel structure has the form (for the saturated regime):

$$\frac{G_I}{(\omega(k) - kv)^2} + \frac{G_{II}}{\omega^2(k)} = \frac{\tanh kd}{k}\left(1 + \frac{k^2 G_I G_{II}}{(\omega(k) - kv)^2 \omega^2(k)}\right),$$ (1)

where k is a wave number of the oscillation, $G_{I,II} = e^2 N_{I,II} / 2\kappa_D m_{I,II}$, and indexes I and II relate to the main and the additional channels, respectively. Voltages V_D and V_G redistribute concentration N_I and N_{II}. Only their sum $N = N_I + N_{II}$ is constant and is determined by the summary doping. For $kd << 1$ the complex conjugate roots of Eq. (1) have the approximate form:

$$\omega_{(1,2)}(k) \cong k\sqrt{\overline{G}}d\sqrt{1 - \left(\frac{\delta G}{\overline{G}}\right)^2}\left(\sqrt{1 - \left(\frac{\delta G}{\overline{G}}\right)} \pm i\sqrt{3/2 + \left(\frac{\delta G}{\overline{G}}\right)}\right),$$ (2)

where $\overline{G} = \frac{1}{2}(G_I + G_{II})$, $\delta G = \frac{1}{2}(G_I - G_{II})$, and the instability disappears only if $G_I = 0$ or $G_{II} = 0$.

For presaturated regimes in such structures three different streams (groups) of electrons participate in plasma oscillations: mobile electrons in channel I and immobile electrons from both channel II and channel I, and we deal with three-stream oscillations.

„Hot Electron Injection Field Effect Transistor"

E. Kolmhofer [*], K. Luebke [*], H. Thim [*],
A. Lugstein [+] and E. Bertagnolli [+],

[*] Microelectronics Institute, University of Linz, Austria
[+] Solid State Electronics Institute, Technical University of Vienna, Austria

Abstract: New experimental results obtained with newly designed 'Hot Electron Injection Field Effect Transistors' are presented and discussed.

The purpose of the work reported is to present new experimental results obtained with GaAs hot electron injection field effect transistors (HEIFETs). In this device [1] a hot electron injection contact of the type used in the planar injection limited Gunn diode or „FECTED"[2] replaces the highly doped source contact used in conventional MESFETs. The injection limiting contact which consists of an ohmic contact and an overlapping Schottky gate injects hot and, hence, fast electrons into the FET-channel thereby reducing the total transit time throughout the channel. A cross sectional view of the HEIFET is shown in figure 1.

figure 1: cross section of a HEIFET

In conventional MESFETs the time needed to accelerate electrons leaving the highly doped source region can be as large as a few picoseconds due to the slow energy transfer (energy relaxation) time. This is in our opinion the reason why 0,5μm gate-MESFETs exhibit a rather low f_T although the time electrons take to travers a distance of 0,5μm at saturated velocity ($\approx 10^7$cm/s) is only around 5ps which is one third of the RF cycle at 60GHz and which should be short enough to allow efficient operation of a 0,5μm gate-MESFET at 60GHz.

While the results presented last year at WOCSDICE'99 [1] have been measured using HEIFETs with a symmetric coplanar layout featuring one central drain electrode and all other electrodes surrounding it symmetrically, we now have chosen an asymmetric layout as shown in figure 1. This layout is embedded into a coplanar circuit in order to facilitate measurements using a HP8510C VNA on a Cascade Microtech waverprober. By using this new layout we were able to reduce the overall size of the transistor and its periphery thereby achieving much more accurately measured values of the S parameters.

Compared to the results presented last year [1] our new transistors exhibit a significantly improved frequency behaviour. Figure 2 shows the current gain of such a HEIFET operated at a drain voltage of $U_D = 5V$ in the frequency range from 45 MHz to 50 GHz. From this plot the transit frequency is determined to be $f_T \approx 27,5$ GHz which is a very good value for a device with a gate length of 0,5 μm.

figure 2: current gain of a HEIFET

In order to further improve the transit frequency it is in our opinion necessary to reduce the distance between the overlapping gate and the control gate which is presently 0,5 µm. We believe that a reduction down to about 0,2 µm would be a good first try. There are three possible approaches to do this. The first is to deposit both the overlapping gate and the control gate in one step. Afterwards a 0,2µm wide trench separating them is etched using for example a Focused Ion Beam (FIB). This method is presently applied at the Solid State Electronics Institute in Vienna. However, this process might cause damage to the active semiconductor layer so a way to avoid that must be found. The second method we are trying is a self-aligned deposition process using a T-gate structure. While the use of a T-gate as a mask for ion implantation processes is quite common, using the T-gate as a mask for metal deposition is more complicated. A third way to define the small gap beween the two gates is to employ the sidewall technique using SiO_2 as a spacer layer of the appropriate thickness. Results obtained with the three methods will be presented at the conference.

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NOTES
Session IV: GaAs, InP-based HEMTs and Ballistic, Hot Electron Effects

NOTES
Session IV: GaAs, InP-based HEMTs and Ballistic, Hot Electron Effects

Session V

Noise in Electronic and Optical Devices

Chair:
Prof. Hermann Schumacher
Universität Ulm, Ulm, Germany

Fluctuations and ultrafast processes of dissipation in 2DEG channels

A. Matulionis, J. Liberis, V. Aninkevičius, L. Ardaravičius, and I. Matulionienė

Semiconductor Physics Institute, Vilnius, Lithuania

Experimental data on relaxation time of dissipation processes are given for quantum well channels containing two-dimensional electron gas. The obtained values are compared to those for Ge, Si, GaAs and InP. The cut-off frequencies of the physics-based equivalent sources of noise are estimated.

Fluctuations serve as 'fingerprints' of the underlying dissipation processes. Thus, investigation of hot-electron fluctuations provides with information on the associated fast and ultrafast kinetic processes. This possibility was demonstrated first on Ge, Si, GaAs and InP (see, for example, [1]). The estimated relaxation time values were in agreement with those available from microwave mixing and hot-electron luminescence experiments. We report on application of the fluctuation technique to two-dimensional electron gas (2DEG) channels for field-effect transistors.

Energy relaxation is one of the most universal dissipation processes responsible for the hot-electron fluctuations. Table 1 presents the data on the effective energy relaxation time for 2DEG channels subjected to an electric field applied in the plane of electron confinement. The data are compared to those for GaAs and InP channels and for lightly doped Ge, Si, and GaAs.

Hot-electron transfer from occupied to empty quantum wells is another important process in the 2DEG channels. This interwell (or real-space) transfer leads to the occupancy fluctuations similar to those due to the intervalley transfer in GaAs and InP. Table 2 gives a comparison of the interwell and intervalley relaxation times estimated by applying the fluctuation technique to different structures.

The data of Tables 1 and 2 provide with an estimate for the cut-off frequency of the physics-based equivalent sources of noise associated with the corresponding dissipation processes (Fig. 1).

Table. 1. Effective energy relaxation time in 2DEG channels estimated from experimental data on hot-electron fluctuations. Data for Ge, Si, GaAs, InP are attached for comparison.

#	Channel composition	Electron density (cm^{-2}, cm^{-3})	Lattice temp. (K)	Electric field range (kV/cm)	Relaxation time (ps)	Ref.
	$InAlAs/In_xGa_{1-x}As/InAlAs/InP$:					
1	x = 0.53	$2.4 \cdot 10^{12}$	300	<1	0.5	2, 3
2	x = 0.7/0.53	$2.3 \cdot 10^{12}$	300	<2	0.9	2, 3
3	x = 0.7	$4.1 \cdot 10^{12}$	300	1.5—3.5	1.5	2, 3
4	x = 0.8—0.53	$1.5 \cdot 10^{12}$	300	<1	1.7	3
5	x = 0.53	$3.3 \cdot 10^{13}$	300	<2	1.9	4
6	$InP/In_{0.67}Ga_{0.33}As/InP$	$1.7 \cdot 10^{12}$	300	<2	0.85	3
7	$Al_{0.25}Ga_{0.75}As/GaAs$	$5.7 \cdot 10^{11}$	80	<0.04	40	5
8	AlGaAs/GaAs	$3.8 \cdot 10^{11}$	17	<0.2	50	6
9	n-type GaAs	$3 \cdot 10^{17}$	300	<2	0.25	3
10	n-type InP	$1 \cdot 10^{17}$	300	<4.6	0.3	3, 7
11	p-type Ge	$1.4 \cdot 10^{14}$	80	0.05—2	33—2.3	1
12	p-type Ge	$1.4 \cdot 10^{14}$	80	0.2	17	8
13	p-type Si	$5 \cdot 0^{14}$	80	0.1—4	18—0.6	8
14	n-type GaAs	$3 \cdot 10^{15}$	300	<2	0.7	8

Table. 2. Interwell/intervalley relaxation time for 2DEG channels and for Ge, Si, and GaAs estimated from experimental data on microwave fluctuations.

#	Channel composition	Dissipation mechanism *)	Electron density (cm^{-2}, cm^{-3})	Lattice temp. (K)	Electric field (kV/cm)	Relaxation time (ps)	Ref.
15	$InAlAs/In_xGa_{1-x}As$, x = 0.53	h-$e\,j\,o\,b$	$2.4 \cdot 10^{12}$	300	>2	100	9
16	$InAlAs/In_xGa_{1-x}As$, x = 0.53	$t\,t\,a\,e$	$3.3 \cdot 10^{13}$	300	<1	70	4
17	AlGaAs/GaAs/AlAs/GaAs	h-$e\,t\,t$	$1.3 \cdot 10^{12}$	80	1	10	10
18	$Al_xGa_{1-x}As/GaAs$, x = 0.33	h-$e\,j\,o\,b$	$1.9 \cdot 10^{11}$	80	1	5	5
19	n-type Si	i-$v\,t$	$3 \cdot 10^{13}$	80	0.2	50	1
20	n-type Ge	i-$v\,t$	$1.5 \cdot 10^{14}$	80	2	17	8
21	n-type GaAs	$r\,i\,s$	$3 \cdot 10^{17}$	300	2.5	0.05	11
22	n-type GaAs	$\Gamma - L$	$3 \cdot 10^{17}$	300	20	0.4	
23	n-type GaAs	$\Gamma - X$	$3 \cdot 10^{17}$	300	100—200	0.06—0.03	12

*)The dissipation mechanism includes the interwell transfer (i-$w\,t$) supported by: h-$e\,j\,o\,b$—hot-electron jumps over barrier, $t\,t\,a\,e$—transverse tunneling at equilibrium, h-$e\,t\,t$—hot-electron transverse tunneling. Γ—L and Γ—X stand for the intervalley transfer (i-$v\,t$) in GaAs, $r\,i\,s$ stands for the resonant impurity scattering.

Fig. 1. The estimated cut-off frequencies for the equivalent noise sources plotted against the applied electric field. The plot is based on the experimental data for the effective relaxation time estimated using fluctuation techniques (symbols are numerated in the order given by Table 1 and Table 2).

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e-mail: matulionis@uj.pfi.Lt

Low frequency noise behavior of microwave active devices and their related phase noise performances

M.Regis[1,2,3], J.Graffeuil[1,3], O.Llopis[1] M.Borgarino[1] and R.Plana[1,3]

[1] LAAS-CNRS and Université P. Sabatier, 7 Avenue du Colonel Roche 31077 Toulouse Cedex04 France
[2] SiGe Microsystems Inc, 1500 Montreal Road, Building M50-IPF, Ottawa ON, K1A OR6, Canada
[3] Université P. Sabatier, Toulouse, France
email : plana@laas.fr

Abstract

In order to improve the capacity, the sensitivity and the bit error rate in modern wireless digital telecommunication systems, the minimization of the transceiver local oscillator (LO) phase noise is gaining actually more importance. This presentation will firstly compare the potentialities of the different microwave solid state devices available for LO design in term of their phase noise and of their low frequency noise (LFN) under small or large signal conditions.

Since LFN is the major parameter that can be accounted for in LO design, bipolar microwave transistors on silicon, which today feature the lowest LFN, are the best suited devices for the design of low phase noise (PN) microwave oscillators up to K-band : an SSB X-band phase noise approaching -120 dBc/Hz at an offset of 10 kHz is becoming a standard performance for a free running conventional bipolar DRO. Further enhancements will necessitate embedding circuit refinements.

1-Introduction

For a long time, the spectral purity of microwave sources has played a minor role and was only related to some sensitive applications such as Doppler radar. Today the trends are changing with the coming of numerous wireless RF and microwave applications which must be able to provide good services for a large number of users. Digital phase modulations schemes, involving an increasing number of phase states, are being used in order to get the best spectral efficiency. Within this concept, the low phase noise (PN) performance of the transceiver local oscillator (LO) is gaining more and more importance in order to fit the specified bit error rate. In order to be able to meet with the requirements of this "new age" electronic, it is very important to well assess how the PN is generated in an oscillating network in order to propose some rules leading to its minimization. It is further well established that the main source of phase fluctuations in a microwave solid state LO comes from the low frequency noise sources of the microwave oscillating active device which are up-converted into phase fluctuations through the non-linearity (NL) of the device. Of course using this LO into a PLL will translate into a LO PN which, in fact, is the PLL reference PN and which is therefore independent from the active device LFN at carrier offsets within the PLL loop bandwidth.

Unfortunately actual conventional references, based on multiplied quartz, do not provide a sufficiently low phase noise at carrier offsets larger than some kHz. Therefore, to fit future PN requirements at some kHz off the carrier, firstly the PLL loop bandwidth must not be taken in excess of some kHz in order to get rid from the reference phase noise. Secondly it must be stated that a multiplied quartz to 10 GHz provides a phase noise not better than about -130 dBc/Hz whatever the offset above about 1 kHz : therefore there is a need to design a 10 GHz free running LO featuring a phase noise better than -130 dBc/Hz at offsets of 10 kHz or more.

Figure 1 shows that the best single side band (SSB) PN performance of an X-band free running resonator stabilized LO is actually not better than -120 dBc/Hz @ 10kHz. Indeed this SSB PN is roughly given by [2]: $L(f_m)_{dBc/Hz} = 10 \log [K_f^2 \, S(f=f_m) / 2 / f_m^2]$ where f_m is the offset from the carrier, $S(f)$ is the input referred LFN voltage spectral density at a frequency f in V^2/Hz, and K_f is the conversion coefficient of LFN into PN expressed in Hz/V : it is essentially offset frequency independent and can either be measured on the oscillating device or be computed from a non-linear circuit simulator as long as an accurate NL active device model is available. It depends on the device non linear behavior, on the embedding circuit configuration and on the resonator Q and coupling coefficients.

Figure 1 after [1] : Phase noise performance (@10 kHz off carrier, measured or predicted) of different LO (0.1 GHz to 100 GHz)

For a moderate resonator Q of about 200. Kf@10GHz is more than 10^6 Hz/V for a FET device and more than 10^7 Hz/V for a bipolar device that is several times higher as a consequence of exponential non-linearities in the later device. At a 10 kHz offset. S(f) is essentially contributed by thermal and shot noise in a bipolar device and is in the range of 10^{-18} V^2/Hz: in a FET device, S(f) is mostly contributed by 1/f noise, experiences strong variations between devices but is hardly better than 10^{-13} V^2/Hz.

Therefore it can be inferred from previous relationship that L(f=10 kHz)@10 GHz will be higher than -90 dBc for FET's and -120 dBc for bipolar DRO which closely fits the data of Figure 1. Further enhancement needs a higher Q : Q=2000 can easily be obtained with dielectric resonators and translates into a PN enhancement of about 20 dBc. Much higher Q's need very specific arrangements such as ambient or low temperature sapphire resonators which do not fit with today commercial requirements.

The goal is therefore to refine oscillator design techniques in order to improve the PN at offsets above a few kHz. This can be done either with embedding circuit optimization in order to decrease K(f) or with active device LFN noise reduction in order to decrease S(f) : this point is addressed in the next section.

II- Active devices for low phase noise LO design

The different solid state technologies today available for high frequency signal generation are: PHEMT's on GaAs and InP and HBT's on GaAs. InP up to W-band or Si up to a few GHz or Si/SiGe up to 30 GHz or more. Figure 2 shows different typical LFN spectra observed on most of these devices. It can be seen that HBT's devices feature a major advantage in term of LFN over FET's and Si or Si/SiGe bipolar transistors feature the lowest LFN among the different available solid state devices as long as a decoupling baseband input capacitor is used [4] to get rid of the low frequency current noise which, otherwise, can be high with respect to voltage noise in bipolar devices. Even if bipolar devices feature larger Kf. their very low LFN translates into the lowest PN available. A very important feature of Figure 2 is the increase of LFN as long as the device is set into oscillation or set into large signal conditions when driven by an external generator. Under these circumstances, using a single input referred LFN source is probably not correct and additionally extra LFN sources grow up. A further advantage of HBT's is that this growing up is usually reduced with respect to FET's. Finally it must be mentioned that the LFN noise of bipolar devices is white noise contributed by thermal and shot noise above 1 kHz : any further reduction of this noise will therefore be very hard to complete. Therefore future PN enhancements in bipolar oscillators will probably be obtained mostly from the optimization of the embedding circuit in order to reduce K_f.

Figure 2 *(using some data are from [3]) : different LFN typical spectra measured on FET on GaAs and bipolar on GaAs or Si; dashed plots refer to non oscillating devices and full plot to oscillating devices*

III-Conclusion

Bipolar microwave transistors on silicon are today the best choice for the designing of very low phase noise oscillators up to K-band : an SSB X-band phase noise better than -120 dBc/Hz at an offset of 10 kHz is today a very reasonable goal [5,6]. Therefore such a performance shows that bipolar DRO can compete with multiplied BAW or SAW for future applications. Further LFN reduction of the active device is not an easy task. Future enhancements will probably be obtained from circuit refinements : increasing resonator Q. using emitter feedback resistors to reduce K_f [7] or implementing a noise cancellation circuit using a discriminator [8].

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Quantum 1/f Noise in GaN Materials and Devices

Peter H. Handel

Department of Physics and Astronomy, University of Missouri-St. Louis, St. Louis, MO 63121, USA

Abstract. 1/f noise was evaluated in GaN bulk and thin film samples, as well as in FET – type and junction-type devices and is much smaller than in GaAs. For impurity scattering in small n-type samples, the conventional quantum 1/f formula predicts a quantum 1/f parameter of $6 \cdot 10^{-9}$ compared with $1.8 \cdot 10^{-8}$ for impurity scattering in n-GaAs. In P-type samples we obtain $1.5 \cdot 10^{-9}$, to be compared with $2.4 \cdot 10^{-9}$ in GaAs. For phonon scattering we get $7.5 \cdot 10^{-7}$ and $4.7 \cdot 10^{-8}$ while GaAs had $6.5 \cdot 10^{-6}$ and $1.2 \cdot 10^{-7}$. This allows 1/f noise optimization in any samples, devices and systems.

Due to the importance of gallium nitride (GaN) for both the solid-state microelectronics and the opto-electronics of the future, a calculation of the fundamental 1/f noise in this material is of primary importance and is long overdue. We start with (1) an evaluation of the conventional quantum 1/f effect in impurity or defect scattering, continue with (2) the calculation of the same effect in acoustic phonon scattering and in (3) the particularly important optical phonon scattering. On this basis we calculate then (4) the resulting conventional quantum 1/f effect. This calculation will be done both for n-type and p-type devices approximately, by neglecting corrections introduced by the energy distribution of the electrons and the author's cross-correlations formula. The errors introduced by this approximation are estimated to be in the 10-20% interval. We then include the coherent quantum 1/f effect, and provide on this basis (5) a final result for GaN samples of any size and any nature.

1. Impurity or defect scattering. The conventional quantum 1/f effect in a scattering cross section σ or recombination rate Γ is given by

$$S_{\delta\sigma/\sigma}(f) = S_{\delta\Gamma/\Gamma}(f) = 2\alpha A/fN \tag{1}$$

Here S(f) is the spectral density of fractional (quantum) fluctuations in the current, $\delta j/j$, in the scattering or recombination cross section $\delta\sigma/\sigma$, or in any other process rate, $\delta\Gamma/\Gamma$. Note that, $\alpha = e^2/\hbar c = 1/137$ is Sommerfeld's fine structure constant. $A = 2(\Delta v/c)^2/3\pi$ is essentially the square of the vector velocity change Δv of the scattered particles in the scattering, recombination or tunneling process whose rate fluctuations we are considering. Finally, N is the number of particles used to define the notion of current j, of cross section σ or of process rate Γ.

For impurity or defect-caused scattering we obtain therefore the quantum 1/f coefficient

$$2\alpha A = (4\alpha/3\pi)(\Delta v/c)^2 = (4\alpha/3\pi)(\Delta p/m_{eff}c)^2 , \tag{2}$$

which is evaluated assuming a thermal energy 3kT/2 for the motion of the current carriers. Note that $4\alpha/3\pi$ is $3.1 \cdot 10^{-3}$. Thus,

$$2\alpha A = (4\alpha/3\pi)<(\Delta v/c)^2> = (4\alpha/3\pi)(6kT/m_{eff}c^2) = 1.2 \cdot 10^{-9} \, (T/300K)(m_o/m_{eff}) \tag{3}$$

and we obtain for electrons with effective mass $m_{eff} = 0.2m_o$ in n-type GaN

$$2\alpha A^{(e)} = 6 \cdot 10^{-9}. \tag{4}$$

For holes with effective mass $m_{eff} = 0.8m_o$ in p-type GaN

$$2\alpha A^{(h)} = 1.5 \cdot 10^{-9}. \tag{5}$$

For comparison, we note that for n-type GaAs with $m_{eff} = 0.068m_o$ we had $2\alpha A_e = 1.8 \cdot 10^{-8}$ and for p-type GaAs with $m_{eff} = 0.5m_o$ we had $2\alpha A_h = 2.4 \cdot 10^{-9}$. Here m_o is the free electron mass.

2. Normal phonon scattering. In this case we put in Eq. (2) $|\Delta p| = \Delta E/s$, where $<\Delta E> \approx kT$ is the energy change of the acoustical phonon in the scattering process and s is the speed of sound. We get

$$2\alpha A = (4\alpha/3\pi)(kT/m_{eff}cs)^2 = 3 \cdot 10^{-8} (T/300K)^2 (m_0/m_{eff})^2. \tag{6}$$

Therefore, for electrons with effective mass $m_{eff} = 0.2m_0$ in n-type GaN

$$2\alpha A^{(e)} = 7.5 \cdot 10^{-7} \tag{7}$$

and for holes with effective mass $m_{eff} = 0.8m_0$ in p-type GaN

$$2\alpha A^{(h)} = 4.7 \cdot 10^{-8}. \tag{8}$$

3. Optical phonon scattering. In this case, the fractional quantum 1/f fluctuation $\delta\Gamma/\Gamma$ of the electron scattering rate Γ on a polar optical phonon of momentum $\hbar q$ and energy $\hbar \omega_q \approx \omega_0$ is described by the quantum 1/f coefficient

$$2\alpha A = (4\alpha/3\pi)<(\hbar q/m_{eff}c)^2> = (4\alpha/3\pi)2<(\hbar k/m_{eff}c)^2>$$
$$= (4\alpha/3\pi)(6kT/m_{eff}c^2) = 1.2 \cdot 10^{-9} (T/300K)(m_0/m_{eff}), \tag{9}$$

the same as for impurity or defect scattering, and we obtain as before for electrons with effective mass $m_{eff} = 0.2m_0$ in n-type GaN

$$2\alpha A^{(e)} = 6 \cdot 10^{-9} \tag{10}$$

and for holes with effective mass $m_{eff} = 0.8m_0$ in p-type GaN

$$2\alpha A^{(h)} = 1.5 \cdot 10^{-9}. \tag{11}$$

For comparison, we note that for n-type GaAs with $m_{eff} = 0.068m_0$ we had $2\alpha A^{(e)} = 1.8 \cdot 10^{-8}$ and for p-type GaAs with $m_{eff} = 0.5m_0$ we had $2\alpha A^{(h)} = 2.4 \cdot 10^{-9}$.

4. Resulting conventional quantum 1/f coefficient and spectral density. Both for electrons and holes, the resulting quantum 1/f coefficient of conventional fluctuations in the mobility μ is given by the relation

$$2\alpha A^{(e,h)} = \Sigma_i(\mu/\mu_i)^2 \; 2\alpha A_i^{(e,h)}, \tag{12}$$

where $2\alpha A_i$ is the quantum 1/f coefficient calculated for the scattering process #i which contributes to limiting the observed mobility according to the relation $1/\mu = \Sigma_i(1/\mu_i)$. If both electrons and holes contribute to the conductivity $\lambda = e(p\mu_h + n\mu_e)$, the spectral density of conventional quantum 1/f fractional fluctuations in λ is

$$S_{\delta\lambda/\lambda}(f) = 2(e^2\alpha/ f\lambda^2)[(p\mu_h)^2 A^{(h)}/N_h + (n\mu_e)^2 A^{(e)}/N_e]. \tag{13}$$

This defines 1/f noise in any small sample, giving smaller noise than in GaAs due to larger effective masses.

5. The inclusion of the coherent quantum 1/f effect yields the final result

$$S_{\delta\lambda/\lambda}(f) = 2(e^2\alpha/ f\lambda^2)[(p\mu_h)^2 B^{(h)}/N_h + (n\mu_e)^2 B^{(e)}/N_e], \quad \text{with} \quad B^{(e),(h)} = [A^{(e),(h)} + s^{(e),(h)}/\pi]/[1 + s^{(e),(h)}]. \tag{14}$$

Here $s = N' \times 5.7 \; 10^{-13}$ cm is the Q1/f coherence parameter. N' is the number of electrons (or holes, depending on the $^{(e),(h)}$ superscript) per unit length along the current path. For example, for a GaN/Al_xGa_{1-x}N doped n-channel HFET this yields the spectral density of V_{DS} in terms of device width Z, current I_{Ch}, thermal voltage kT/q

$$<(\delta V_{DS})^2>_f = (I_{Ch}/fZ^2 D_{eff}qV_{th}) \int_{X_0}^{X_1} (\alpha_H / \mu_n)[dX/(X-1)\ln^2 X], \; \text{with} \; X \equiv 1 + \exp(\frac{V_{GS} - V_T - V}{V_{th}}), \tag{15}$$

where X_0 and X_1 are the values of X at the source (V=0) and at the drain (V=V_{DS})., while $\alpha_H = 2\alpha B^{(e)}$.

In conclusion, the noise is an order of magnitude lower, brightening the future for GaN even more.

Current noise suppression in quantum well infrared photodetectors at low bias voltages

A. Carbone and P. Mazzetti

*Dipartimento di Fisica and Istituto Nazionale di Fisica della Materia,
Unita` del Politecnico di Torino, Corso Duca degli Abruzzi 24,
I-10129 Torino, Italy*

The power spectrum of current noise in Quantum Well Infrared Photodetectors (QWIP) is calculated considering the smoothing effect of electron Coulomb interaction on the noise to account for the noise suppression observed in QWIP's at low external bias. Actually, when the external voltage is low, it has been shown that the potential at the collector is inverted with respect to the emitter. Such potential distribution gives rise to a longer electron transit through the interelectrodic region. As a result, each electron emitted at the cathode, during the longer transit time through the device, reduces the transmission probability of the emitter barrier and thus increases the waiting time for a subsequent electron emission, which results in a low frequency current noise reduced with respect to the equivalent vacuum tube shot noise 2eI, in agreement with the experimental findings.

Introduction

Quantum Well Infrared Photodetectors (QWIPs) are photoconductive devices whose structure can be tailored to detect infrared radiation of a given wavelength (1). Under ideal operating conditions, QWIPs should behave linearly with incident infrared power, and the figures of merit should be independent of infrared light power, applied voltage and number of wells. However, nonlinearities have been observed, mainly at high excitation power or in QWIPs with a small number of wells. These nonlinearities have been related to the nonuniform distribution of the electric field through the quantum well (QW) structure and, in particular, to the voltage drop on the injection emitter barrier. Actually, since the mechanisms ruling the carrier injection from the contacts (thermionic field emission or thermionic field assisted tunneling) and the carrier drift through the QW structure have a different dependence on the electric field, the first wells must deplete in order to supply the charge required to maintain equilibrium between the current injected from the emitter and the total current flowing through the QWIP (2,3). The behavior of noise gain observed in QWIPs has been also related to the nonuniform distribution of electric field in the QW structure. The excess noise was ascribed to a modulation noise component related to the effect on the emitter barrier potential of the depletion of one electron from the first QW (4,5). It has been shown that, at low bias voltages, the electric field at the collector contact may disappear $V_c=0$, or even change its sign $V_c<0$ (2,3). The main consequence is that the escape of injected electrons from the QW structure is hampered. The electrons injected from the contacts not having enough energy to reach the other electrode, remain longer in the interelectrodic region, where the potential takes its minimum value. The excess negative charge lying in the QW structure decreases the potential drop across the contact barriers resulting in a long range Coulomb repulsion between the injected charges. On account of this, it should be expected that the probability of a further electron injection decreases during the transit of each electron instead of being constant, as in the case of fully uncorrelated pulses.

Theory

At low bias voltages, the random electron transport through a QWIP structure can be modeled as follows: consider first the elementary stochastic event corresponding to the emission of one electron from the contacts to the QW structure. If the repulsion effect were absent, the probability distribution of the time interval t_e between two emission events would be Poissonian, with average value τ_e, and the

noise would be full "shot noise". When the electric field is inverted, two main concerns should be considered: (a) while transiting through the device the electron exerts a Coulomb repulsion on the next electron ready to enter, (b) the exit of an electron from the QW structure is stochastic, instead of being a deterministic event. Let t_{in} indicate the stochastic time beween two electron emissions from the interelectrodic region. For the sake of simplicity, let us assume that the probability distribution function of the time intervals t_{in} is Poissonian, with average value τ. On the basis of the previous considerations, it can be expected that the time interval t between subsequent emissions from the contacts into the QW structure is lengthened with respect to t_e. This delay due to Coulomb repulsion can be assumed of the order of t_{in}. Therefore, the time interval t can be expressed as $t_e + t_{in}$, where both t_e and t_{in} are Poisson-distributed random variables. The distribution function $Q(t)$ of the random variable t, sum of the two random variables t_e and t_{in}, can be calculated by the convolution of those of t_e and t_{in}, and results (6):

$$Q(t) = \frac{\tau_e \tau_{in}}{(\tau_e - \tau_{in})} \cdot \left[\exp\left(-\frac{t}{\tau_e}\right) - \exp\left(-\frac{t}{\tau_{in}}\right) \right]$$

which leads to the following expression of low frequency current noise:

$$S_1(0) = 2eI \cdot \left[1 - 2 \cdot \frac{\tau_e \tau_{in}}{(\tau_e + \tau_{in})^2} \right]$$

To compare the results of the present model with noise data of real QWIP devices, the quantities τ_e and τ_{in} should be related to phenomenological parameters, depending on the actual conditions under which the device operates, in particular, the capture probability of the QW p_c. The inverse τ_{in} can be evaluated as the inverse drift time τ_d in a period L_p plus the inverse capture time τ_{QW} of each electron in the QW, while τ_e can be assumed equal to τ_{QW}. In this case, the noise gain g_n for the single QWIP device can be written:

$$g_n = \frac{1}{2} \cdot \frac{(p_c^2 + 1)}{(p_c + 1)^2}$$

Note that when $p_c \rightarrow 1$ the noise gain $g_n \rightarrow 1/4$. Compared to $g_n \rightarrow 1/2$, obtained by using the expression developed in (5), the present model seems to be in better agreement with the data reported in (3), showing a noise gain much lower than one in the range of applied voltages where $V_c < 0$.

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NOTES
Session V: Noise in Electronic and Optical Devices

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Session VI

Large-Signal Properties of FETs

Chair:
Prof. Didier Lippens
Université des Sciences et Technologies de Lille 1, Villeneuve d'Ascq Cedex, France

MOCVD delta-doped GaAs structures for power microwave transistors

V.L. Gurtovoi, V.V. Valyaev, S.Yu. Shapoval, S.V. Morozov,
S.V. Dubonos, A.N. Pustovit

*Institute of Microelectronics Technology, Russian Academy of Sciences,
142432 Chernogolovka, Moscow region, Russia.*

Delta-doping is very promising in applications for power field-effect transistors (FET). Among advantages of delta(δ)-doped FETs in comparison with standard MESFETs are high current density level due to channel carrier concentration easily being in the range 10^{12}-10^{13} cm^{-2}, high linearity, transconductance (because of small distance between the electron channel and the gate) and breakdown voltage. Nevertheless, it is difficult to achieve improved characteristics in real structures, since with decreasing the gate-channel distance (for δ-doped FET of the order of 30-50 nm) the local relief after gate recess should be less than 3-5 nm, moreover, etching homogeneity for the whole substrate should also be very high.

In this work we compare three types of δ-doped FETs: standard δ-doped FET with single δ-doped layer; single δ-doped channel with undergate AlGaAs layer (15 nm thickness) to increase breakdown voltages; and double δ-doped layers (interlayer distance 15 nm) instead of single δ-doped channel for transconductance improvement. The net delta-doped channel concentration was 5×10^{12} cm^{-2} for both single and double δ-doped FETs. Contact cap layer consisted of 10 δ-doped layers in order to improve contact resistance. Transistor structures had gate 2.2×50 μm^2 and source-drain distance of 10 μm.

The samples were grown on semi-insulating and n$^+$ (Te-doped, 2×10^{18} cm^{-3}) GaAs substrates by low-pressure (100 mbar) metalorganic chemical vapor deposition at 600°C and 650°C. Thrimethylgallium, 10% arsine in hydrogen and silane (1500 ppm) diluted in argon were used. High concentration of the silane doping source allowed a doping time of only 5 sec, which in combination with a growth rate of 21 nm/min resulted in a rather short period of time (7 min) the δ-doped layers were kept at growth temperature. This was done to minimize the thermal diffusion of Si atoms. The capacitance-voltage profile of a δ-doped layer with n=5×10^{12} cm^{-2} (after cap layer etching) showed the full width at half maximum (FWHM) of 5.5 nm, which corresponds to spreading of impurity atoms of 3.0 nm (growth temperature 650°C). SIMS profiling was carried out on a Cameca IMS4f using 3 keV I_2^+ primary ions. The FWHM for double δ-doped layers is 3.0-3.5 nm (Fig.1), which with taking into account the resolution of the SIMS technique for I_2^+ ions of 1 nm results in width of impurity distribution of less than 2.0 nm (growth temperature 600°C).

Saturation current for all transistors was in the range 120-200 mA/mm and pinch-off voltage 1.5-2.0 V. For single and double δ-doped FETs satisfactory breakdown voltage of 8 V was achieved. Drastic increase of breakdown voltage up to 25 V was observed for transistor with undergate AlGaAs layer (Fig.2a), which could be explained by increase of the barrier under the gate and reduction of tunneling and thermal-field components of the gate current, which became essential for gate-channel distance of 30-40 nm. The FET with a single δ-doped layer revealed extrinsic transconductance of 140 mS/mm, the FET with undergate AlGaAs layer - 120 mS/mm and that with double δ-doped layer - 200 mS/mm for the gate length 2.2 μm (Fig.2b). 40% improvement of transconductance for double δ-doped FET in comparison with single δ-doped FET is due to mobility and conductivity increase, which results from transition of a part of electrons from delta-doped planes to undoped spacer between them. This results in spatial separation of carriers and ionized impurities and reduction of scattering. The transconductance improvement is achieved via spatial rearrangement of doping atoms in two layers without increase of the doping concentration.

A detailed investigation of conductivity dependence of high quality double δ-doped structures as a function of distance between δ-doped layers (concentration 3×10^{12} cm^{-2} per layer) is shown in Fig. 3. At optimized spacer thickness of 190 Å, maximum in conductivity is observed both at 300 K and 77 K. The maximum exceeds the conductivity of the single δ-doped layer (n=6×10^{12} cm^{-2}) by 30 and 20 % at 300 K and 77 K, respectively.

Parameters of transistors could be further improved by optimizing concentration of δ-doped layers and distance between them, changing the thickness and improving quality of undergate AlGaAs layer.

Fig.1. SIMS profile of a double delta-doped structure with the spacer thickness of 9.6 nm.

Fig. 2. I-V characteristics of 2.2 μm delta-doped transistors with (a) undergate AlGaAs layer and (b) double δ-doped channel.

Fig.3. Spacer thickness dependence of conductivity of double delta-doped structures.

Summary WOCSDICE 2000

Comparison of the RF Large Signal Performance of Common -Source, -Drain and -Gate Amplifiers using GaAs MESFETs

Frank Ellinger, Daniel Treyer, Rolf Vogt and Werner Bächtold
Swiss Federal Institute of Technology (ETH) Zürich
Laboratory for Electromagnetic Fields and Microwave Electronics
CH-8092 Zürich, Switzerland, Tel. +41 1 632 55 52, e-mail: ellinger@ifh.ee.ethz.ch

Abstract- **The RF large signal performance (-1 dB compression point and third order intercept point) of LC matched common -source, -drain and -gate amplifiers in class A operation is compared at 5 GHz. Simulations were performed with a harmonic balance simulator using our modified TOM II large signal model for 0.6 μm GaAs low power enhancement MESFETs. The model is verified by linear and nonlinear measurements.**

Especially for amplifiers in wireless LAN receivers it is important to choose the right circuit configuration (common source (CS), -drain (CD) or –gate (CG)) to achieve optimum large signal performances at low supply power. This work compares the compression and intermodulation behavior of these basic circuit configurations in class A operation at 5 GHz to illustrate their different performances.

Our modified TOM II large signal model [1], which allows excellent predictions both in the linear (resistive) and in the saturation region of MESFETs [2,3], is used in a HP libra harmonic balance simulator. Fig. 1 and Fig. 2 show a comparison of simulated and measured S-parameters and harmonics of the used enhancement FET in common source configuration (E-FET, Triquint TQTRx, transit frequency ≈ 18 GHz, threshold voltage ≈ 0.14 V). Fig. 3 shows the simplified equivalent RF circuits of the investigated amplifiers. The E-FETs are biased with bias chokes at a gate source voltage of 0.4 V (class A operation) and are reactively matched to 50 Ω to obtain return losses of better than -10 dB at 5 GHz. RC feedbacks are applied to enable unconditional stability.

Fig. 4 shows the simulated power gain and supply current of the circuits versus the supply voltage. The highest power gain can be reached with the CS configuration. At a supply voltage of 3 V and a supply current of 4 mA, the achieved power gain is 10.8 dB, 10.2 dB and 6.3 dB for the CS- (voltage and current gain), CG- (voltage gain, no current gain) and CD- amplifier (current gain, no voltage gain).

Fig. 5 and Fig. 6 show the simulated −1 dB output compression point and the third order intercept point at the output of the circuits. The CS and CD configuration are superior for supply voltages of less than 1.2 V, the CG configuration is significantly better for higher supply voltages. At a supply voltage of 3 V the −1 dB output compression point is −1.5 dBm, 1 dBm and 6 dBm for the CD, CS and CG amplifier, respectively.

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Fig. 1: S-parameters of E-FET in common source configuration, w=300μm, V_{ds}=3V, I_{ds}=6.5mA, 0.4GHz - 27GHz, simulated (solid) and measured (dotted)

Fig. 2: Harmonics of E-FET in common source configuration, w=300μm, V_{ds}=1V, I_{ds}=3mA, f=5GHz, simulated (solid) and measured (dotted)

Fig. 3: Equivalent RF circuit of the common source (CS)-, common drain (CD)- and common gate (CG)- amplifier using E-FETs with a gate width of 150μm

Fig. 4: Simulated power gain and supply current of the common source (CS)-, common drain (CD)- and common gate (CG)- amplifier, f=5GHz, V_{gs}=0.4V

Fig. 5: Simulated -1dB output compression point (P_{-1dB}) of the common source (CS)-, common drain (CD)- and common gate (CG)- amplifier, f=5GHz, V_{gs}=0.4V

Fig. 6: Simulated IP3 at the output (OIP3) of the common source (CS)-, common drain (CD)- and common gate (CG)- amplifier, f=5GHz, V_{gs}=0.4V

10GHz load-pull measurement for a 0.3μm-N-HIGFET

M. TOUIRAT, M. ROGER, E. DELOS, L. T. NUYEN*, Y. CROSNIER and G. SALMER

Institut d'Electronique et de Microélectronique du Nord (**IEMN**), Avenue Poincaré, B.P. 69
59652 Villeneuve d'Ascq cedex, France, UMR CNRS 8520, e-mail : miloud.touirat@iemn.univ-lille1.fr
* PICOGIGA, 5 Rue de la Réunion, Z. A. De Courtaboeuf, 91940 Les Ulis, France

Complementary GaAlAs/GaInAs/GaAs Heterostructure Insulated-Gate Field-Effect-Transistor's (C-HIGFET's) offers the prospect of high speed and low power dissipation IC's [1], [2]. Moreover, N-HIGFET is a good candidate for new microwave power applications (wireless) thanks to his low supply voltage (less than 4V) and his good linearity performance [3]. In this paper, N-HIGFET fabrication process and typical power device results are presented.

HIGFET device structure is shown in Fig. 1. The main steps of sidewall technology are refractory gate definition, first implantation self-aligned to the gate, sidewalls definition, second implantation self-aligned to the sidewalls and ohmic contact evaporation [4]. In Fig. 2, cross section SEM photography of the resulting structure is presented. Gold is deposited on the gate in order to reduce its parasitic resistance. Typical distance between drain and source contacts is 1.8μm. Interconnect metallization is made by Ti/Au. Device is finally passivated with Si_3N_4.

Typical I-V characteristics of $2*25*0.3\mu m^2$ (number of fingers×gate width×gate length) N-channel is shown in Fig. 3. High values of drain-to-source current density and transconductance are obtained: 460mA/mm at Vds=Vgs=2V and 480mS/mm at Vds=2V and Vgs=1.2V, respectively (fig. 4). Gate thickening makes it possible to reduce its resistance considerably: for a 0.3μm gate length, thickening allows to obtain 0.2kΩ/mm instead of 6kΩ/mm. This improves the dynamic performance of the device, in term of maximum oscillation frequency (Fmax) and maximum available gain (MAG). Fmax increases from 31GHz to 55GHz and MAG at 10GHz from 10dB to 15dB for typical DC bias condition of Vgs=1.2V and Vds=2.5V. In addition, the gate turn on voltage is 1.4V (@ Igs = 1 μA/μm). The threshold voltage is 0.4V and its standard deviation on a 2-in wafer is equal to 50mV.

Power results: Fig. 5 shows load-pull power performance at 10GHz and at two supply voltages: at Vds=2.5V, the output saturated power was 10.5dBm, the power density was 220mW/mm, and the corresponding gain was 4.5dB. At Vds=3V, we obtained an output saturated power of 11.8dBm, a power density of 300mW/mm, and a corresponding gain of 5.8dB. Moreover, the maximum power added efficiency is 65% for the both polarization. These results are quite interesting compared, for example, to a power density of 270mW/mm and a linear gain of 7dB obtained for a 0.25μm-DC-HFET [5].

More investigations are planed in a close future to optimize the HIGFET Heterostructure for high power applications.

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10nm	GaAs
25nm	$Ga_{0.25}Al_{0.75}As$
15nm	$Ga_{0.80}In_{0.20}As$
	Si
	GaAs

Fig. 1 : Cross-section of HIGFET epitaxy

Fig. 2 : SEM photography of a 0.3µm WSi gate with SiO_2 sidewall and gold.

Fig. 3 : I-V measurement of 0.3µm-N-HIGFET. Vgs max = 1.6 V. Step Vgs = 0.2 V.

Fig. 4 : Variation of transconductance and current versus Vgs for a $2\times25\times0.3\mu m^2$ at 2V.

Fig. 5 : Swept power measurement of an $2\times25\times0.3\mu m^2$ at 10GHz for two supply voltage.

NOTES
Session VI: Large-Signal Properties of FETs

NOTES
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Session VII

GaAs and InP-based HBTs

Chair:
Dr. Jean-Charles Garcia
Picogiga, Courtaboeuf Cedex, France

GaAs-based Materials for HBTs

Jean-Charles Garcia

PICOGIGA, Place Marcel Rebuffat – Parc de Villejust, 91971 Courtaboeuf Cedex, France

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Investigations on the Impact of the InGaP Ledge on HBT-Performance

V. Palankovski *, R. Schultheis **, A. Bonacina **, and S. Selberherr *

Institute for Microelectronics, TU Vienna, Gusshausstr. 27--29, A-1040 Vienna, Austria
Tel: +43/1/58801-36017, Fax: +43/1/58801-36099, E-mail: Vassil.Palankovski@iue.tuwien.ac.at
***Infineon Technologies AG, Wireless Systems WS TI S MWP, Otto-Hahn-Ring 6, D-81730 Munich, Germany*

It is well known that GaAs-HBTs with InGaP emitter material can be improved with respect to reliability if the emitter material remains over the complete p-doped base layer [1]. Outside the active emitter area remains the so-called InGaP ledge. In this paper we study by means of two-dimensional device simulation the influence of the ledge thickness and of presence of surface charges on the device performance and its impact on reliability.

Introduction

The two-dimensional device simulator MINIMOS-NT deals with different complex materials and structures such as binary and ternary alloys with arbitrary material composition profiles. Various physical effects, such as band gap narrowing, surface recombination, and self-heating, are taken into account. The efficiency of the models was proven by hydrodynamic DC-simulations with self-heating of forward, reverse and output characteristics of one finger AlGaAs/GaAs and InGaP/GaAs-HBTs [2], furthermore, by small-signal RF-simulation [3]. Simulation results are in good agreement with measured data. However, so far the particular influence of the InGaP-ledge on InGaP/GaAs-HBTs on the device performance has not been studied in detail.

Impact of the InGaP Ledge

In Fig.1 we show the measured and simulated collector and base currents of a one finger InGaP/GaAs-HBT operating under forward gummel plot conditions with $V_{BC} = 0$ V. Measurement refers to a device with 40 nm thick ledge. So far for simulation no surface charges at any of the device interfaces have been introduced. As can be taken from Fig.1 simulated and measured base currents differ significantly in the case of a 40 nm thick ledge. Only simulation with a ledge thickness less than 20 nm delivers a good match. This is due to the fact that at this bias the depletion region is only approximately 20 nm thick and enables a leakage path for electrons on top of it as shown in Fig.2. However, this leakage path could be overcome by means of electrically isolated base contacts.

The influence of fixed negative surface charges, which are homogeneously distributed along the interface between ledge and passivation, was investigated. As can be taken from Fig.3, where simulation refers to a device with 40 nm ledge, base current can be reduced if more negative surface charges are introduced. The upper part of the ledge is also depleted [4] and the leakage is reduced (Fig.4). Thus, with a surface charge density of 10^{12} cm^{-2} the measured base current can be simulated very well.

Device Reliability

Based on these investigations it is possible to explain the base current degradation (see open triangles in Fig.3) of a device which was strongly stressed under conditions far from normal operating conditions. In this case the base current degradation in the middle voltage range can be explained by decreasing surface charge density along the interface between ledge and passivation from 10^{12} cm^{-2} to 4.10^{11} cm^{-2}. This might be due to compensation of the negative surface charges by H+ ions, which are known to be present in the device due to the epitaxial manufacturing processes [5].

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Figure 1: Dependence of I_B on the InGaP ledge thickness compared to measurement.

Figure 2: Electron current density $[A/cm^2]$ at $V_{BE}=1.2V$. Simulation without surface charges.

Figure 3: Dependence of I_B on the charge density at the ledge/nitride interface compared to measurement. Measured degraded I_B included.

Figure 4: Electron current density $[A/cm^2]$ at $V_{BE}=1.2V$. Simulation with surface charge density of 10^{12} cm^{-2}.

The Influence of the Emitter Orientation on the Noise Characteristics of InP/InGaAs(P) DHBTs

A. Huber, I. Schnyder*, M. Rohner*, H. Jäckel*, C. Bergamaschi, and K. Schenk

Zentrum für Mikroelektronik, FH Aargau, CH-5210 Windisch, Switzerland

* Electronics Laboratory, Swiss Federal Institute of Technology, CH-8092 Zürich, Switzerland

Abstract

The authors report on the noise properties of InP/InGaAs(P) double heterojunction bipolar transistors (DHBT) having emitters in directions [011] and [010] of the InP crystal. The higher small signal current gain of the [010] transistors results in an improved noise performance of 1 dB of F_{min}.

1   Introduction

InP/InGaAs HBTs have excellent high frequency performance and are therefore widely used for RF circuits. Considering the noise performance, these devices are generally inferior to MESFETs or HEMTs. To reduce this deficiency, we can either try to reduce the base series resistance or to increase the current gain resulting in a decrease of the base current noise. Devices with the same vertical layer structure but different current gains can be fabricated by varying the direction of the emitter with respect to the InP crystal. The two emitter directions which were investigated are the [011] and [010] directions, respectively. These two arrangements are depicted in Figure 1. For the [010] direction, we can

Figure 1: Schematic respresentation of the directions of the emitter mesa under investigation

observe an emitter under-cut which is about 150 nm larger on each side than for the [011] direction. This leads to a smaller effective emitter area at the emitter mask width W_{Em} [1]. As will be demonstrated in Section 2, an increase of the current gain β will be observed which has a direct positive impact on the noise properties of the devices.

2   Measurement Results

RF S-parameter and noise parameter measurements were carried out in the frequency range from 0.04 to 40 GHz and 0.3 to 6 GHz, respectively. The small signal current gain β ($h_{21}(f \rightarrow 0)$) was calculated from the measured S-parameters. Figure 2 shows the maximum β, which is reached at $J_C = 1.5 \cdot 10^5 \, A/cm^2$ and $V_{CE} = 2\,V$, versus emitter width W_E. The [010] de-

Figure 2: Maximum small-signal current gain β versus emitter width W_E for devices with [011] and [010] emitter directions

vices have a small signal current gain up to 100 whereas the [011] devices only reach 50. The effect of the higher current gain of the [010] transistors is still more pronounced for smaller emitter width W_E. We observe a decrease of β of only 20 % when the emitter width W_E is reduced from $3.2\,\mu m$ to $0.4\,\mu m$ for the [010] devices compared to the [011] transistors which show a reduction of β by a factor of 2 for a reduction of W_E from $2.5\,\mu m$ to $0.7\,\mu m$.

The influence of the different emitter directions on the noise performance of the HBTs is shown in the Figures 3 and 5 for a collector current density of $10^5 A/cm^2$. The minimum noise figure F_{min} of the [010] devices is more than 1 dB smaller than of the [011] devices. This significant improvement is obtained without a degradation of the RF properties of the DHBT which is demonstrated in Figure 4. We can only observe the higher h_{21} of the [010] transistors toward DC. At higher frequencies, the gain curves are almost identical. Values for f_T and f_{max} of 115 GHz and 170 GHz (from Mason's unilateral gain), respectively, can be ex-

Figure 3: Measured minimum noise figure F_{min} of a [011] direction transistor ($A_E = 1.5 \times 8 \, \mu m^2$) and a [010] direction transistor ($A_E = 1.2 \times 8 \, \mu m^2$) at a collector current density $J_C = 10^5 \, A/cm^2$

Figure 4: Measured h_{21} and maximum available gain MAG versus frequency of a [011] direction transistor ($A_E = 1.5 \times 8 \, \mu m^2$) and a [010] direction transistor ($A_E = 1.2 \times 8 \, \mu m^2$) at $I_C = 12 \, mA$

trapolated for both device types.

The optimum source reflection coefficients Γ_{opt} of the [010] devices depicted in Figure 5 is located farther away from $50 \, \Omega$ than Γ_{opt} of the [011] devices which may render noise matching more difficult. However,

Figure 5: Measured optimum source reflection coefficient Γ_{opt} of transistors with [011] and [010] emitter directions at a collector current density $J_C = 10^5 \, A/cm^2$

the noise figure for a source impedance of $50 \, \Omega$ is still

lower for the [010] transistors than for the [011] devices.

We further investigated the noise performance of the two emitter directions for different emitter widths W_E, which is shown in Figure 6 at a collector current of $8 \, mA$. For emitter widths larger than $1.5 \, \mu m$, F_{min} in-

Figure 6: Measured minimum noise figure F_{min} versus emitter width W_E for [011] direction devices and [010] direction devices with an emitter length of $L_E = 8 \, \mu m$ at $I_C = 8 \, mA$

creases for both emitter directions due to the larger base series resistance. For smaller emitter width, F_{min} increases significantly for the [011] emitters due to the drop of the small signal current gain. This effect cannot be observed for the [010] devices. This is an additional advantage since the smaller devices can be operated at smaller currents resulting in a reduction of the power consumption.

3 Conclusion

An investigation of the RF noise properties of InP/InGaAs(P) double heterojunction bipolar transistors having two different emitter directions with respect to the InP crystal was carried out. The small signal current gain β of DHBTs with an emitter in direction [010] is more than twice as high as the β values of transistors having emitters in the [011] direction. This increase of β improves the minimum noise figure F_{min} of more than 1 dB without degrading other device properties. For small emitter widths, the improvement is even better which offers the potential for low noise and low power applications.

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Development of a Novel InP/InGaAs(P) DHBT Process for Power Applications

I. Schnyder, M. Rohner, D. Huber, C. Bergamaschi*, and H. Jäckel

Electronics Laboratory, Swiss Federal Institute of Technology. CH-8092 Zürich, Switzerland

*Zentrum für Mikroelektronik, FH Aargau, CH-5210 Windisch, Switzerland

Abstract

We present an InP/InGaAs/InGaAsP double heterojunction bipolar transistor technology with a quaternary step graded base collector structure based on an existing InP SHBT process. The devices achieve a DC current gain of $\beta = 70$ and a breakdown voltage of $BV_{CE0} = 10.5$ V. A transit frequency of $f_T = 115$ GHz and a maximum oscillation frequency of $f_{max} = 170$ GHz have been extrapolated.

1 Introduction

Using an established InP-SHBT process [1] with $\beta = 40$, $f_T = 130$ GHz and $f_{max} = 230$ GHz, several state of the art circuits for opto-electronic applications have been demonstrated [2]. Nevertheless for laser and modulator driver applications, this SHBT process suffers from its low breakdown voltage of less than 2.3 V at a current density of 10^5 A/cm^2. To overcome this problem, a quaternary step graded InP/InGaAs(P) DHBT process was developed with a breakdown voltage of more than 5 V at a current density of 10^5 A/cm^2. Besides the higher breakdown voltage, the InP collector offers the potential to under-etch the InGaAsP grading and base layers selectively, resulting in a higher maximum oscillation frequency (f_{max}) by minimizing the base collector capacitance.

2 Device - Structure and Fabrication

The optimized design of the base-collector layer structure is one of the main aspects to suppress the current blocking effect at the base-collector junction due to the conduction-band spike resulting from the larger bandgap of InP compared to InGaAs. Based on a quaternary step grading [3] and an electron launcher structure concept [4], a novel base-collector layer structure has been implemented (see Table 1). For base and emitter we used the same layers as in our SHBT process. Fig. 1 shows the simulated band-diagram of the optimized structure under thermal equilibrium.

Layer	Material	Thickness (nm)	Dopant	Doping (cm^{-3})
Cap	InGaAs	75	Sn	$2.2 \cdot 10^{19}$
Cap	InGaAs	325	Sn	$2 \cdot 10^{19}$
Emitter	InP	50	Si	$1 \cdot 10^{19}$
Emitter	InP	150	Si	$4 \cdot 10^{17}$
Spacer	InGaAs	5	-	-
Base	InGaAs	50	Zn	$3.5 \cdot 10^{19}$
Spacer	InGaAs	20	-	-
Grading	InGaAsP	20	-	-
Grading	InGaAsP	20	-	-
Collector	InP	20	Si	$4 \cdot 10^{17}$
Collector	InP	480	-	-
Subcoll.	InGaAs	30	Sn	$1 \cdot 10^{19}$
Subcoll.	InP	340	Si	$1 \cdot 10^{19}$
Buffer	InP	100	-	-
Substrate	InP	375 μm	Fe	-

Table 1: DHBT-layer structure

Figure 1: Simulated band diagram of our DHBT layer structure under thermal equilibrium.

The layer structure was grown by low pressure MOVPE [5]. To enable the desired underetch of the base and grading layers, the edges of the emitter and collector mesa were aligned along the [010] direction of the crystal instead of the [011] direction which is used for the SHBT process. Starting by wet etching the emitter mesa for the self-aligned base and emitter contacts, this new orientation results in a larger emitter undercut of 200 nm in the [010] direction instead of 50 nm in the [011] direction. Then the base and emitter metallization (Pt/Ti/Pt/Au) was evaporated. The base collector mesa was first dry etched using reactive ion etching (RIE) and finally selectively wet etched to achieve the desired lateral base undercut [6]. The collector contact metalization (Ti/Pt/Au) was applied before wet etching the InP sub-collector to isolate the devices. Benzocyclobutene (BCB) was used for passivation and planarization. Finally the emitter, base and collector contacts were opened by dry etching before the final metalization (Cr/Au) was evaporated.

3 Experimental Results

DC and RF S-parameter measurements were carried out. The output characteristic of a transistor with an emitter size of $1.2 \times 8 \, \mu$m^2 (Fig. 2) demonstrates a higher output resistance and an improved breakdown behavior compared to SHBT devices. Also the breakdown voltage BV_{CE0} increased from 7 V to 10.5 V (see Fig. 4). In contrast to the SHBT devices, the base current of the DHBT transistor shows a nearly ideal behavior (Fig. 3) caused by the larger emitter undercut of 200 nm instead of an emitter undercut of 50 nm for the SHBT devices. This results in a much wider range of constant current gain.

The AC characterisation was carried out up to 110 GHz. Fig. 5 depicts the small signal characteristics of a transistor with an emitter size of $1.2 \times 8\,\mu m^2$. A transit frequency of $f_T = 115$ GHz and a maximum oscillation frequency of $f_{max} = 170$ GHz were extrapolated. Which are state-of-the-art values.

Figure 2: Comparison of the measured output characteristics of a DHBT with an emitter size of $1.2 \times 8\,\mu m^2$ and a SHBT with an emitter size of $1.5 \times 8\,\mu m^2$.

Figure 3: Comparison of the measured Gummel plots of a DHBT with an emitter size of $1.2 \times 8\,\mu m^2$ and a SHBT with an emitter size of $1.5 \times 8\,\mu m^2$.

Figure 4: Measured breakdown behaviour ($I_B=0$) of a DHBT with an emitter size of $1.2 \times 8\,\mu m^2$ and a SHBT with an emitter size of $1.5 \times 8\,\mu m^2$.

Figure 5: Measured Mason's unilateral gain (MUG) and h_{21} of a DHBT transistor with an emitter size of $1.2 \times 8\,\mu m^2$ ($U_{CE}=2$ V, $I_C = 11$ mA).

4 Conclusions

A novel InP DHBT process with a quaternary step graded base collector junction based on an existing InP SHBT process was developed. The new DHBT devices show improved DC characteristics compared to the SHBT devices with $\beta = 70$ and $BV_{CE0}=10.5$ V, which are excellent results compared with other InP DHBT devices. The promising small signal characteristics and the feasibility of a large base and emitter undercut due to the transistor orientation along the [010] direction offer the potential for a further increase in f_T and f_{max} by enhancing the not yet optimized lateral base undercut and using a thinner collector and nevertheless maintaining an excellent output voltage swing.

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NOTES
Session VII: GaAs and InP-based HBTs

NOTES
Session VII: GaAs and InP-based HBTs

Session VIII

GaN-based HEMTs and HBTs, Oxide-based and SiC Devices

Chair:
Prof. Hans Ludwig Hartnagel
Technische Universität Darmstadt, Darmstadt, Germany

US Navy Research Progress in Wide Gap Semiconductors & NICOP International Opportunities in Wide Gap Semiconductors

Colin Wood

Office of Naval Research, Arlington, VA, U.S.A.

paper not available at time of print

GaN/AlGaN HEMT's Grown by RF-Assisted MBE FOR ROBUST LOW NOISE AND HIGH POWER AMPLIFIERS

M. Micovic, W-S. Wong, P. Janke, P. Hashimoto, L. M. McCray, and C. Nguyen

HRL Laboratories, LLC,
3011 Malibu Canyon Road,
Malibu, CA 90265

Remarkable advances in performance of GaN High Electron Mobility Transistor (HEMT) provide clear evidence that this device will revolutionize the field of microwave power electronics. At the time of writing of this abstract several groups had reported continuous wave RF power density exceeding 5 W/mm [1, 2, 3], and the first GaN HEMT with f_t over 100 GHz has been demonstrated [4]. While high power amplifier continues to be the most obvious application for this device, our recent results [5] suggest that GaN HEMT may also be a device of choice for robust low-noise amplifiers because it eliminates need for front-end protection circuitry and, hence, improves system performance and design simplicity. A noise figure of 0.60 dB at 10 GHz that we measured for a GaN HEMT with gate to drain breakdown voltage exceeding 60 V is approaching the lowest noise figures reported for a GaAs P-HEMT. This is the best combination of noise figure and breakdown voltage ever reported for a solid state device in this frequency range. The recent advances of GaN HEMT performance were almost exclusively achieved by improvement of GaN material quality. During the previous year we demonstrated that RF assisted Molecular Beam Epitaxy (MBE) is a good production tool for fabrication of GaN HEMT epilayers on 50 mm diameter SiC wafers. A typical 0.25 µm gate length devices fabricated from our material produced 5 W/mm to 6 W/mm of maximum output power density at 10 GHz.

The maximum output power of these devices scales well with gate width [3]. The maximum output powers of 1.2 W, 6.3 W and 10.3 W were measured, respectively, at 10 GHz for transistors with 0.2 mm, 1 mm and 2 mm of total gate periphery. This is to the best of our knowledge the best scaling of output power with gate width ever reported in literature for a GaN HEMT.

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Performance Limits of AlGaN/GaN HEMT's

Lester F. Eastman

Cornell University, School of Electrical and Computer Engineering, Ithaca, NY 14853-5401

The strong electrical polarization present in undoped pseudomorphic Al_xGa_{1-x}/GaN structures grown on the Gallium face, induces a two-dimensional electron gas (2DEG) near 1×10^{13}/cm^2 sheet density for $.3 < x < .4$ values. High performance microwave HEMT's are fabricated from such undoped structures. This undoped structure has clear advantages over doped HEMT structures, such as higher electron mobility, orders of magnitude lower $1/f$ noise, and lower electric field under the gate at the pinch off condition. These HEMT's on SiC have intrinsic f_t values up to 106 GHz for .15 μm gate length and 250 Å thick barriers, depending reciprocally on the effective gate length. This represents an average electron transit velocity of 1.32×10^7 cm/s in the presence of low 10^8/cm^2 dislocations. On sapphire, where dislocations are about four times as dense, the intrinsic f_t for this gate length is 94 GHz, and the average transit velocity is $1.18 \times 1\ 10^7$ cm/s. Their drain-source breakdown voltage rises in proportion to the gate length, being ~ 100 V for .40 μm gate length and 2 μm gate-drain spacing. These results give rise to a figure of merit representing HEMT electrical limits of performance.

$$P_A\, f_{10}^2\, Z_L = 1.2 \times 10^{23} \text{ W Hz}^2\ \Omega$$

Where P_A is the class A saturated power, f_{10} is the frequency for 10 db power gain, and Z_L is the load resistance. Non-linear three-dimensional heat flow simulations have been made to yield the limit of normalized heat dissipation required to cause 300°C channel temperature limit. In cases where heat dissipation has caused permanent degradation of small signal properties of HEMT's the simulations show channel operating temperature exceeds 300°C. The frequency response has only dropped 15% for 300°C operation, compared to room temperature operation. Large periphery HEMT's, with 50 μm pitch between parallel channels, can dissipate 2.2 W/mm heat with 300 μm sapphire substrates, and 17 W/mm with 300 μm SiC substrates all within the 300°C limit. Structures grown by OMVPE have yielded as low as 300 Ω/square 2DEG sheet resistance (1,700 cm^2/V-s mobility and 1.2×10^{13}/cm^2 sheet density) with similar results by MBE. GaN buffer layers have $< 10^{14}$/cm^3 net donors and the AlGaN barriers have $< 10^{17}$/cm^3 net donors. Compensation from ~ 10^9/cm^2 dislocations occurs in the buffer layer, and the unfilled dislocation states contribute, along with surface states, to carrier trapping and current slump during high voltage operation. Illumination by photons of > 2.2 eV sharply reduces

this current slump. These undesirable drain current transients are also suppressed by passivating the exposed surface with a Si_3N_4 layer. The HEMT's are processed using Cl_2 ECR etching for mesa isolation, Ti/Al/Ti/Au ohmic contacts annealed at 800°C for 60 seconds, and Ni/Au Schottky gates fabricated by electron-beam lithography. Ohmic contacts have .3-.5 Ω-mm transfer resistance and the knee voltage is ~ 3 V at 300°K. Drain current ranges up to $\geq$ 1 A/mm depending on the barrier thickness and passivation. The surface potential of Al_3Ga_7N is ~ 1.6V, causing depletion in addition to the localized depletion near the dislocations. Small periphery single-gate HEMT's on 300 µm sapphire have yielded up to 4 W/mm microwave output power. Large periphery (12 x 125 µm) HEMT's on sapphire have yielded 78% power-added efficiency at 1.8 W/mm normalized output power. Results for large periphery for HEMT's on SiC substrates have been much less consistent in their performance, yielding only 5-6.5 W/mm in C.W. operation and somewhat higher in pulsed operation, limited electrically. Severe gate leakage, along with a rise in drain current, occurs at higher drain voltage. This limits the efficiency at higher drain voltage and causes excessive heating. It is expected that 10-12 W/mm will be reached with improved SiC substrates. It is clear that it is necessary to advance the technology of the materials, especially that of the SiC substrates. It is also necessary to study and understand the physical effects causing current slump, leading to more control of the problem.

Growth and Characterization of AlN/GaN MISFETs

A. Eisenbach, E. Alekseev, S.M. Hubbard, and D. Pavlidis

The University of Michigan, Department of Electrical Engineering and Computer Science
Solid State Electronics Laboratory, 1301 Beal Avenue, Ann Arbor, MI 48109-2122, U.S.A.
Tel.: +1 (734) 936-1599, Fax: +1 (734) 763-9324, E-mail: eisenbac@engin.umich.edu, pavlidis@umich.edu

AlN/GaN MISFET layers have been grown by MOVPE at The University of Michigan and devices were fabricated. The maximum drain current of these MISFETs was greater than *700mA/mm*, while drain-source breakdown was *30V* and drain-gate breakdown was *40V*. Devices with a gate length of *2μm* exhibited a peak transconductance of *136mS/mm* at $V_{GS}=1V$, which exceeds previously reported results.

Most of the research effort on GaN-based electronics is currently focused on AlGaN/GaN HFETs and excellent high frequency and high power performance has been demonstrated. Increasing the Al fraction in the donor layer allows higher electron mobility and increased density of the 2DEG at the interface of Al(Ga)N and GaN and can enhance the power capability. [1] Another promising candidate for high-power broadband operation is the AlN/GaN MISFET. MISFETs offer attractive features for power applications such as high ON-state breakdown and high frequency and thus broad bandwidth operation capability. Additionally, the channel can be placed very near the metal gate, leading to increased intrinsic transconductance. The authors recently reported very encouraging results on such devices. [2],[3] Success of AlN/GaN MISFET approaches critically depends on material with good structural properties. Moreover, results reported so far suggest mediocre interface roughness probably related to inter-diffusion between Al and Ga. [4] This paper reports on good crystalline properties of the grown AlN/GaN heterostructures and very promising electrical performance from AlN/GaN MISFETs.

The GaN and AlN layers were grown by MOVPE at The University of Michigan in a home-built horizontal quartz reactor at low pressure on c-plane sapphire substrates using TMGa, TMAl, and NH_3 as precursors. First, a thin, ~20nm thick GaN buffer layer was grown at *515°C*, followed by the high-temperature growth of the bulk GaN and/or AlN layers at *1120°C*. Smooth and transparent thin AlN layers could be grown on top of thicker GaN bulk layers. Hall measurements on thicker AlN layers could not be performed since the layers were too resistive. Following AlN growth, subsequent growth runs manifested poorer morphology and electrical characteristics and part or all of the sapphire substrate was covered with large crystallites. Therefore, a reactor re-conditioning procedure has been developed to overcome this problem by removing the deposited AlN.

Following this reactor re-conditioning procedure, a GaN reference layer was grown and compared to previous samples grown before any AlN growth, and with exactly the same growth parameters. At this point, both surface morphology and electrical characteristics are normally acceptable. However, XRD measurements still show a strong "memory"-like effect of the AlN growth as can be seen in Figure 1. The peaks for the GaN *(0002)* plane shown in this figure are due to multiple wavelengths emitted by the X-ray source. Fortunately, this difference in the GaN *(0002)* XRD spectra disappears by further GaN growth. Reactor conditioning approaches of the above described type are essential for growth of high quality AlN/GaN material and have also been utilized by other groups for MOCVD growth of AlN/GaN structures on sapphire.

The MISFET heterostructures consisted of a thin low-temperature GaN buffer layer, a *0.5μm*-thick undoped GaN channel, and a thin AlN barrier layer. The device layer structures had specular surface morphology and good structural properties

Figure 1: XRD spectra of GaN (0002) peak before AlN growth and after the reactor-reconditioning procedure.

as evaluated by XRD measurements. Figure 2 displays the XRD spectra of two MISFETs, one with *7.5min* AlN growth and one with *6min* AlN growth, corresponding to nominal AlN thicknesses of *110* and *88Å* , respectively. Both samples show a distinctive AlN peak even for very thin AlN layers, indicating the good crystalline quality of the grown MISFET structures.

Theoretically, the AlN *(0002)* peak should be at *2θ≈36.04°*. For both samples, the GaN *(0002)* peak centers around *34.6°* in good agreement with the theoretical value. However, the AlN *(0002)* peak centers around *35.75°* for the thinner and around *35.85°* for the thicker AlN sample, respectively. There are two different possibilities:

Figure 2: XRD spectra of two MISFET samples with different AlN thickness.

1. The AlN is not completely relaxed despite the fact that it is thicker in both samples than the critical thickness for AlN on GaN,. The fact that the thinner AlN layer is closer to GaN agrees well with this assumption, since it might be still more strained than the thicker AlN layer.

2. The AlN contains a small fraction of Ga. Assuming a linear dependence of the peak position between GaN and AlN as a function of the Al content x, this would result in an $Al_{0.81}Ga_{0.19}N$ layer for the thinner and in an $Al_{0.87}Ga_{0.13}N$ layer for the thicker grown AlN layer, respectively. This difference could be explained by a compositional gradient, which might be the result of the relatively high growth temperature of *1120°C* leading to interdiffusion of Ga and Al, or because of some memory effect in the reactor.

The AlN/GaN layer design was optimized by evaluating the mobility dependence on AlN layer thickness as obtained by Hall measurements. When the growth time of AlN was *450sec* corresponding to a thickness of *~110Å* for the AlN layer, the combined bulk-2DEG electron mobility was *320cm²/Vs* and the associated 2DEG density was $2×10^{13}cm^{-2}$, respectively. This growth time was used for growing the MISFET device layers. AlN/GaN MISFETs were fabricated on these structures using Cl-based dry etching for device isolation and Ti/Al/Ti/Pt metals for ohmic contacts deposited directly on the top AlN layer. Gate contacts were made using Pt/Ti/Au metals. The maximum drain current was greater than *700mA/mm*. Devices with a gate length of *2μm* exhibited a peak transconductance of *136mS/mm* at $V_{GS}=1V$, which exceeds previously reported results [5].

AlN/GaN heterostructures using thin epitaxially grown AlN barrier layers have been investigated for the purpose of developing III-N-based MISFETs. The high quality of the heterostructures is confirmed by very high values of transconductance and current density obtained from the fabricated MISFETs. These results indicate a high potential of AlN/GaN MISFETs for microwave power applications.

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Silicon nitride passivation effets on GaN MESFET's

C. Gaquiere, B. Boudart, R. Amokrane, Y. Guhel, Y. Crosnier, J.C. De Jaeger, and F. Omnes*

*Institut d'Electronique et de Microélectronique du Nord, U.M.R. - C.N.R.S. 9929
Département Hyperfréquences et Semiconducteurs, Avenue Poincaré B.P. 69
59652 VILLENEUVE D'ASCQ CEDEX – FRANCE, Gaquiere@IEMN.Univ-Lille1.fr*

** Centre de Recherche sur l'Hetero-Epitaxie et ses Applications
Parc de Sophia Antipolis, Rue bernard Gregory06560 VALBONNE- FRANCE*

Introduction:

It is widely predicted that GaN-based devices make it possible to obtain higher microwave power performance than GaAs or InP usual FET's. However, for these devices an important discrepancy is noted between the measured microwave power performance and the prediction based on the DC characteristics which is mainly due to trap effects. In this frame, MESFET's GaN devices achieved in our labs have been studied. In a first time, studies under pulsed conditions have been carried out to localize the trapping phenomena. In a second time, silicon nitride dielectric passivation layers (SiNx) have been deposited under different conditions (temperature, thickness) to investigate the influence of these layers on the surface states and as well to check if these layers could give rise to strain and hence piezoelectric effects.

Results

The devices studied have a gate width of $2*50\mu m$ and a gate length of $0.5\mu m$. The source drain spacing is $2.5\mu m$ with a gate to drain spacing of $1\mu m$. Under static conditions, the device exhibits a drain current density of 160 mA/mm at Vds=18 V and Vgs=1 V. The pulse widths used in our experiments are 400 and 380 ns respectively for Vgs and Vds[1]. The trailing and leading edges are 50 ns for both and the frequency of the pulses is 100 kHz. The quiescent bias point is Vds0=18 V and Vgs0=-9 V. In these conditions, the device can be considered as cold [2]. The device exhibits a drain current density of 48 mA/mm at Vds=18 V and Vgs=1 V. The difference between the static and the pulsed drain current can be explained by the existence of electrical traps localized in the GaN material or/and at the surface (Fig.1). The measurement conditions are changed, by heating the device with a chuck at a temperature of 150 °C, at the same quiescent bias point (Vds0=18 V and Vgs0=-9 V). The drain current obtained is two times higher than at room temperature. By changing the quiescent bias point at Vds0=18 V and Vgs0=-2 V (class A), the drain current value also doubles due to the fact that the device is heated in these polarization conditions and the quiescent trap states are not the same. When the device is strongly illuminated during the pulse measurements (Vds0=18 V and Vgs0=-9 V) the drain current is also affected (104 mA/mm at Vds=18V, Vgs=1V). All these experiments prove the existence of electrical traps. The trapped electrons can be untrapped with light or temperature and so participate to the electrical conduction. The main trap densities could be expected to be located at the surface because the pinch off voltage for both conditions of measurement is identical. See an example figure 2.

Then, SiNx coatings with thickness of 800 and 1600Å were done at temperature samples of 200, 250 and 300°C in a plasma-enhanced chemical vapor deposition (PECVD) reactor. The different cases are summary in the table I. The deposition times of these layers are about 450 and 900 second for the 800 and 1600Å respectively. The reactants were 3% SiH_4 diluted in N_2, and NH_3. The fluxes were 600 and 20 cm^3 min^{-1} respectively. The RF power was 10W and the pressure was 1 Torr. No sample pretreatment was applied before SiN_x deposition. The main information are an increase of the maximum drain current (Fig. 3) and problems to pinch off the devices which are more en more important with the silicon nitride deposition temperature. The reference compounds have been heated

in the same conditions at 200, 250 and 300°C and any evolution has been noted. Hence these evolutions are directly correlated with the silicon nitride layers. Isolation deteriorations are also observed as soon as an dielectric layer is deposited this degradation is more and more important accordingly the temperature deposition increases The strain effects of SiN_x deposition on GaN have been investigated using UV Raman spectroscopy. No significant Raman shift as a results of strain induced from the dielectric deposition was observed in the GaN material, whatever the thickness and temperature deposition used in the technical process. During the presentation pulsed measurement DC, RF and pulsed RF small signal will be presented according to the temperature and thickness nitride deposition layers.

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Acknowledgement

Figure 1 : I-V characteristics without light for Vgs from –9 to 1V (step 2 V). DC (plain line) and pulsed (Vgs0=-9V and Vds0=18V : dotted line)

Figure 3 : Drain current densities behaviour at Vds=15V and Vgs= 1V versus silicon nitride deposition temperature (thickness = 800Å)

Figure 2 : static and class A pulsed current drain at Vds=10 V without light.

	Ref	Case A	Case B	Case C	Case D
Temp	-	200°C	250°C	300°C	250°C
Thick	-	800 Å	800 Å	800 Å	1600 Å

Table I: Summary of the studied devices.

Simulations of AlGaN/GaN HEMTs

Robert Anholt

Gateway Modeling, Inc. 1604 East River Terrace, Minneapolis, MN 55414
612-339-4239; fax: 612-339-3995; anholt@ieee.org

Shur [1] has estimated 24A/mm for the maximum currents possible for AlGaN/GaN HEMTs. Starting with simulations of a measured HEMT that produced peak currents of 0.4A/mm, we examine possible methods to increase the currents, such as reducing the thermal impedances to reduce IV curve droop, reducing the gate length and contact resistances, increasing the piezoelectric charge near the channel, and increasing the mobilities. With all of these improvements, we find that it may be possible to increase the peak I_{dss} to 2.7A/mm.

The device simulations were done using G-PISCES-2B, a Poisson, current-continuity equation solver based on drift diffusion [2], incorporating the piezoelectric charge models of Ambacher et.al.[3] and the velocity-field models of Albrecht et.al.[4]. We simulated the AlGaN/GaN HEMTs measured by Binari et.al.[5] which had a gate area of $1 \times 150 \mu m^2$ in two fingers, and a 300A undoped $Al_{0.3}GaN$ layer. Computations of average thermal impedances were done using PETS [2] for several layouts. Using the average thermal impedance and PISCES simulations at three fixed temperatures, the self-heating corrected IV curves were obtained, using a method similar to that described for HBTs [6]. Figure 1 compares measured and modeled curves at $V_g=0$. Unlike for most GaAs or InGaAs-based devices, I_{ds} at fixed bias is a nonlinear function of temperature, so non-linear interpolation methods are used in solving self consistent equations for temperature rise vs power and power or I_{ds} vs temperature. The simulations here are a fit; we used 70% lower mobilities than modeled [4], a large contact resistance 2×10^{-5}ohm-cm^2, and 1.2×10^{13} instead of 1.68×10^{13}cm^{-2} for the piezo charge, all being consistent with previous observations.

We then examined the question of what can be done to improve the currents. First we examined what happens when the full mobilities, full piezocharge, and smaller contact resistances of 10^{-6}ohm-cm^2 are used. Piezo and contact resistance improvements increase the peak currents to 800mA/mm. Next we examined methods of reducing the self heating. PETS gives a thermal impedance of 31K-mm/W for the HEMT on sapphire versus 7.4K-mm/W for the HEMT on SiC (Table I). Another possible method is to flip-chip mount device, as shown in Fig.2. With the flip-chip mount, the thermal impedance is not as low as on SiC (Table I). We next considered reducing the gate length, which increases the currents because I_{ds} is mobility-limited in these devices (not v_{sat}-limited as in most GaAs MESFETs) so reducing the gate length increases the fields and velocities. Figure 3 shows IV curves using the best possible parameters; undoped 300A $Al_{0.3}GaN$ layers, $L=0.15 \times 150 \mu m^2$, SiC substrates, $\rho_c=10^{-6}$ohm-cm^2. We get peak currents around 2.7A/mm. Although the theoretical piezocharge extrapolates to $\sim 5 \times 10^{13}$cm^{-3} for AlN/GaN [1], only $\sim 2 \times 10^{13}$cm^{-2} has been achieved thus far [7].

Finally we back up to the question: are Poisson calculations adequate given the fact that the electron profiles are so narrow for these devices? Figure 4 shows POSES [2] computations using a newly developed fully-self consistent 1d Poisson-Schroedinger equation solver that employs numerical wavefunctions. We compare QM and Poisson CV curves for several $Al_{0.3}GaN$ thicknesses. For donor thicknesses of 200 and 300A, the QM and Poisson capacitances are indistinguishable and the maximum difference occurs for 100A donor thicknesses and less. We conclude that for the present generations of AlGaN devices (and future ones?) QM is not required, thus the 2d Poisson-current-continuity solution methods are adequate.

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Table I. Modeled thermal impedances ($1 \times 75 \times 2 \mu m^2$)

Layout	T.I.
Sapphire substrate 625um	31.1 K/-mm/W
SiC substrate	7.4
Top sink on gate	19.8
Top sink on drain	13.0
Top sink on source	15.9
Source pillars between gates	14.5
5um thick Au	15.4

Fig.1. Measured [5] IV curves and models at three fixed temperatures plus a self-consistent self-heating corrected (SHC) curve.

Fig.2. Cross section of HEMT on a coplanar layout with a source-pillars-thermal shunt. Gate: black, Drain: diamonds fill, Source and shunt: white. The chip is flipped so a (perfect) sink is on top.

Fig.3. Simulated HEMT using optimal parameters

Fig.4. QM and Poisson CV curves for AlGaN/ GaN HEMTs with varying donor thicknesses. (The top curve at $V_g=0$ for each pair is the QM one.)

Evaluation of AlGaN/GaN HBTs

S. Fathpour and D.L. Pulfrey

Department of Electrical and Computer Engineering
University of British Columbia
Vancouver, BC V6T1Z4, Canada

GaN is regarded as a promising material for making high-temperature electronic devices. This hypothesis is examined by using compact models to predict the current gain of AlGaN/GaN HBTs at temperatures up to 600K. In addition, the effects on HBT performance of two unusual features of GaN, *i.e.*, spontaneous polarization and incomplete acceptor ionization, are examined by numerical modeling.

Introduction

The large bandgaps of materials within the AlGaN ternary system have led to speculation that GaN devices could be candidates for electronic applications in high-temperature environments. Here we consider AlGaN/GaN HBTs, and examine their current gain as a function of temperature up to 600K. The most recent values from the literature of the temperature dependence of relevant material parameters have been incorporated into a comprehensive compact model, from which the collector and base currents are predicted. Both abrupt- and graded-emitter devices have been studied over a range of aluminum mole fractions (0.1-0.3) and emitter doping densities (0.5-5.0E18 cm^{-3}).

The spontaneous polarization inherent to AlGaN materials may be a factor in HBT performance as the sheet charge densities in abrupt-junction devices, and the distributed charge densities in graded devices, can significantly affect the potential profile at the critical emitter-base junction. This effect is examined here by numerical modeling using MEDICI.

The deep nature of the ground-state level of the Mg acceptor in p-type GaN means that the ionization of this dopant is not necessarily complete, and will depend on the position, *i.e.*, the band bending, in the device. The effect that this has on the free-carrier densities and, consequently, on the signal delay time, is investigated using MEDICI.

Results and Discussion

At a given temperature, the devices studied exhibit a range of behaviour of J_C *vs.* V_{BE}, depending on whether the bottleneck for transport is at the emitter-base junction or in the base. The latter region controls the current for the graded-emitter devices, while the former region dictates the current in the abrupt-junction devices, with a diode ideality factor that depends strongly on the emitter doping density. The base current is determined by diffusion in the quasi-neutral base and, for a given device, exhibits the same ideality factor as the collector current. This is because the current is driven by ($V_{BE}-\Delta E_{fn}$), where the quasi-Fermi-level splitting ΔE_{fn} depends on the collector current. At higher temperatures, the emitter-base junction presents less of a barrier to charge flow, and the characteristics of abrupt- and graded-devices tend to merge. It appears that current gains of around 50 should be possible at 600K.

The sign of the net spontaneous polarization charge at the emitter-base junction will depend on the substrate polarity. If conditions are such that this charge is negative, our simulations indicate that the emitter-base barrier will be enhanced to such a degree that the current gain will be severely degraded.

Usually, in estimating the signal-delay time (and thus f_T) by the charge-control method, it does not matter whether the change in charge of the electrons or the holes is considered. However, when ionization of the acceptors is incomplete and position dependent, as is the case here in the GaN base region, the calculated value of f_T depends on which carrier is considered. This phenomenon is currently being investigated and will be reported on at the conference.

Oxide-based pHEMTs and HBTs; what are they and why bother?

J. Champlain, C. Zheng, and U.K. Mishra

ECE Department, UCSB, Santa Barbara, CA.93108, USA

paper not available at time of print

Electrical characterization of *4H*-SiC *p⁺-n-n⁺* Avalanche Diodes

Konstantin Vassilevski[1,2], Konstantinos Zekentes[1], Elena Bogdanova[2], Alexander Zorenko[3]

[1]*Foundation for Research and Technology-Hellas, P.O. Box 1527, Vassilika Vouton, 711 10 Heraklion, Greece*
[2]*Ioffe Institute, St.Petersburg, 194021,Russian Federation*
[3] *State Scientific & Research Institute "Orion", Kyiv, 252057, Ukraine*

Low capacitance (≈ 4.5 pF at zero bias) *4H*-SiC *p⁺-n-n⁺* diodes with moderately doped base region ($\sim 10^{17}$cm^{-3}) were fabricated. The diodes exhibited a differential resistivity of $\sim 5\times10^{-5}\Omega\cdot$cm^2. This value is the lowest published for *4H*-SiC *p⁺-n-n⁺* diodes until now. The diodes had a homogeneous avalanche breakdown at voltage of 270 V. They were capable to dissipate a specific d.c. power of 130 kW/cm^2 and pulsed power of 3.7 MW/cm^2 in avalanche mode of operation. Diode noise were measured at d.c. avalanche current density up to 10 A/cm^2.

Introduction

The advantage of silicon carbide (SiC) as a semiconductor for use in ultra high frequency (UHF) diodes is based on its fundamental properties: high breakdown field, excellent thermal conductivity, capability to operate at elevated temperature [1]. Nevertheless, fabrication of UHF SiC diodes was not extensively addressed up to now, although outstanding results were obtained in the development of high power/low frequency rectifying diodes. Namely, SiC IMPATT diodes were not fabricated, although electrical characteristics of these diodes were predicted by numerical modelling [2] and SiC diodes capable to operate at high avalanche current density of $\cong 60$ kA/cm^2 were fabricated [3,4]. This fact may be attributed with necessity to combine a low series resistance and a low capacitance in the same diode structure to fabricate UHF diode.

This paper reports on the fabrication and electrical characterization of *4H*-SiC *p⁺-n-n⁺* diodes having low capacitance and low series resistance and capable to operate at high avalanche current density.

Experimental

4H-SiC *p⁺-n-n⁺* epitaxial structures grown on *n*-type wafers were purchased from Cree, Inc. The *n* layer had a donor concentration of $N_D= 1.3\times10^{17}$cm^{-3}, and its thickness, $w_n=2$ μm, was chosen to be close to the thickness of space charge region at avalanche breakdown in an abrupt *4H*-SiC *p⁺-n* junction having this donor concentration. The acceptor concentration in the *p⁺* layer having the thickness 1 μm was equal to $N_A = 6\times10^{18}$cm^{-3}.

Nickel of 200 nm thickness annealed at 1000°C for 120 sec was used as the back ohmic contact. The metals were deposited in a single run in the following sequence: Al(50 nm)/Ti(100 nm)/Pt(25 nm)/Ni(50 nm) to form the contacts to *p⁺*- type *4H*-SiC epitaxial layer. After excess metal removal by lift-off procedure, the anneal process was repeated. A commercial plasma system was used to form the mesa structures having 100 μm diameters. Uncovered SiC was etched away down to the *n⁺* epitaxial layer. Simultaneously, structures for measurements of resistivity of the contact to *p*- SiC by the TLM method were fabricated. After the control of contact resistivity and on-wafer characterization, the wafer was scribed and cut into chips. The chips were mounted on standard packages for UHF diodes. Packaged *4H*-SiC *p-n* diode is shown in Figure 1.

Figure 1. *4H-SiC diodes assembled in the standard UHF diode holders optimized for X (8.2 - 12.4 GHz) frequency band.*

Results

The fabricated diodes had a capacitance $C_0 \approx 4.5$ pF at zero bias. The dependence $C^{-2}(U)$ was well fitted by linear function with built in

Figure 2. I-V characteristics of the 4H-SiC p^+-n diode at high current densities under forward and reverse biases obtained from a Tektronix 370 curve tracer.

Figure 3. Nose power density of the 4H-SiC p^+-n diode depending on d.c. avalanche current.

voltage of 2.8 V. This value is close to the theoretical limit for ideal 4H-SiC p^+-n diodes. I-V characteristics of the diode at high current densities under forward and reverse biases are shown in Figure 2. The diode differential resistivity decreased with the increase of the forward bias reaching the value $R_D = 5.4 \times 10^{-5} \Omega \cdot cm^2$ at current density $j > 25$ kA/cm². The diodes had avalanche breakdown at 270 V and revealed stable operation under avalanche breakdown conditions. Figure 2 shows the I-V characteristic of the diode at avalanche current density up to 430 A/cm² corresponding to the power density up to 130 kW/cm². This power density may be considered as dissipated by the diode in d.c. mode of operation. The pulse measurements were performed at forward and reverse bias to avoid the effect of diode structure self heating on measured parameters. The diodes had the isothermal series resistivity $R_D = 1 \times 10^{-4} \Omega \cdot cm^2$ and were capable to dissipate a specific pulsed power of 3.7 MW/cm² in avalanche mode of operation at 100 ns pulse duration.

Noise characteristics of the diodes at d.c. avalanche current densities up to 10 A/cm² were measured also. The noise power density depending on the avalanche current is shown in Figure 3. The sharp decreasing of noise power at frequency about 6 GHz is clearly seen. To a first approximation, this frequency may be associated with avalanche frequency of the diode structure.

Conclusion

Recently developed Al/Ti/Pt/Ni based contact to p^+ 4H-SiC was used to fabricate the 4H-SiC p^+-n-n^+ diodes with moderately doped base region ($\sim 10^{17}$cm^{-3}). The diodes had extremely low series differential resistivity $\sim 5.4 \times 10^{-5} \Omega \cdot cm^2$ at d.c. forward current density $j > 25$ kA/cm². They revealed a homogeneous avalanche breakdown at voltage $U_b \approx 270$ V and were capable to dissipate the power density of 130 kW/cm² at d.c. avalanche current. In a pulse mode of operation, the diodes were capable to dissipate the power of 3.7 MW/cm² at avalanche current up to 1.1 A. Low capacitance (≈ 4.5 pF at zero bias), low series resistance (≈ 3.5 Ω), and capability to operate at high avalanche current make the fabricated 4H-SiC diodes very suitable for UHF testing as IMPATT diodes and as varactors for electrical frequency tuning of the UHF power sources.

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Session IX

SiGe-based FETs and HBTs

Chair:
Dr. Didier Théron
Institut d'Electronique et de Microélectronique du Nord, Villeneuve d'Ascq Cedex, France

Recent Results on SiGe HFETs and HBTs

Hermann Schumacher [1] and Ulf König[2]

[1]*University of Ulm, Dept. of Electron Devices and Circuits, 89069 Ulm, Germany*
Phone: +49 731 502-6152, Email hschu@ieee.org
[2]*DaimlerChrysler Research Center, Wilhelm-Runge-Straße 11, 89013 Ulm*
Phone: +49 731 505-2050, Email ulf.koenig@daimlerchrysler.com

New consumer-oriented wireless service concepts demand a dramatic expansion of the frequency range used for consumer applications beyond 2 GHz upto 60 GHz. The challenge for the semiconductor industry is to respond to this with affordable microwave IC solutions. Si/SiGe heterostructure devices can stand up to this challenge. The authors report on recent developments in the emerging field of SiGe heterostructure field effect transistors (HFETs) where both n- and p-channel devices show cutoff frequencies in the millimeterwave range, and on progress in improving the useable range of SiGe heterojunction bipolar transistors (HBTs).

Heterostructure Field Effect Transistors

In SiGe HFETS, the well known principle of III/V high-electron mobility transistors (HEMTs) is being transferred to Si microelectronics. High low-field carrier mobilities up to 2900 cm^2/Vs for n-channels and up to 1900 cm^2/Vs for p-channels have been found, 5 to 10 times above doped Si with a corresponding carrier concentration [1]. In addition, there is evidence for an increased velocity overshoot due to strain in the channels.

For Schottky- or MOS-gate devices IBM and DaimlerChrysler have reached transconductances around 300 mS/mm for depletion mode and around 500 mS/mm for enhancement mode n-channel HFETs [2]. HFETs with p-channels showed around 250 mS/mm [3]. High currents above I_{DSS}=600 mA/mm have been obtained for p-MOS HFETS. Both n- and p- HFETs have demonstrated maximum frequencies of oscillation (f_{max}) around 120 GHz and transit frequencies (f_T) up to 70 GHz . In n-HFETs this is achieved already with a gate length of 0.25 µm, see **Fig. 1** [4]. For p-HFETs, the gate length has to be reduced to 0.1µm for comparative performance (**Fig. 2**) [5]. Recently the performance at cryogenic temperatures has been investigated. 195 GHz was measured for n-HFETs at 50 K, 180 GHz for p-HFETs at 35 K (**Fig. 3**). The pronounced frequency increase is related to the dramatic improvement in the 2-dimensional electron or hole transport in the Si- or Ge-channels, respectively, at low temperatures due to the reduction in phonon scattering. While a gate length dependence is visible for all frequency data reported so far, the range below 0.2 µm is hardly exploited. Better self-aligned layouts with lower parasitics are needed to reach the simulated cutoff frequencies around 300 GHz.

Fig. 1: Current gain |h$_{21}$| and maximum available gain (MAG) vs. frequency for an L$_g$=0.25 µm n-channel Si/SiGe HFET

Fig. 2: Current gain |h$_{21}$| and maximum available gain (MAG) vs. frequency for an L$_g$=0.1 µm p-channel Si/SiGe HFET

Fig. 3: Maximum frequency of oscillation vs. gate-source voltage for n-channel and p-channel Si/SiGe HFETs

Fig. 4: RF sweep of an active mixer using Si/SiGe HBTs for 20 GHz [9]

Concerning noise, Siemens has established corner frequencies below 200Hz for p-SiGe MOSFETs [6]. These excellent values are due to the buried-channel layout of HFETs. Conservative semi-quantitative simulations for the high-frequency noise predict a minimum noise figure 0.5 dB at 20 GHz in properly designed devices. If finally a new CMOS generation can be created, consisting of a Si-channel nHFET and a Ge-channel pHFET the power-delay product can even reach values below 1fJ.

Heterojunction Bipolar Transistors

State-of-the-art SiGe HBT processes close to production show cutoff frequencies (f_T and f_{max}) of around 80-90 GHz. These performance figures allow for analog circuits up to about 20 GHz - higher only in special cases where low gain is sufficient, e.g. in oscillators. The extension of the useable frequency range of SiGe HBTs is therefore still an issue. At DaimlerChrysler, a new record in transit frequency, f_T=156 GHz, has been set in a transistor where f_{max} was as high as 81 GHz, a unique combination. This transistor has a self-aligned double-mesa structure with an aggressively scaled base: the layer thickness is 15 nm with an 8 nm thick region doped to $8 \times 10^{19} cm^{-3}$ and a Ge mole fraction of 35%. The structure was grown by MBE [7].

In an experiment closer to production, optimization of the lateral layout of the Temic commercially available SiGe1 technology has resulted in an improvement of the maximum frequency of oscillation from 50 GHz to 85 GHz, while maintaining an f_T of 50 GHz. The modification involves a moderate reduction of the emitter width to 0.8 µm, optimization of the contact geometry and interdigitated collector contacts [8].

Recent MMIC Results

Using the optimized SiGe HBTs fabricated at Temic, we have realized several MMICs in the 16-23 GHz range, in a production technology on standard 20 Ωcm Si substrates, see e.g. **Fig. 4**. Details of these circuits (oscillators, an active mixer and a low-noise amplifier) will be presented at the workshop. They strongly suggest that SiGe heterojunction devices are a viable technology for future consumer products in the Ku and Ka bands.

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SiGe BiCMOS Progress and Evolution at IBM

Greg Freeman

IBM Microelectronics, Hopewell Junction New York

Designers and chip producers have clearly adopted SiGe HBT devices, considered an interesting lab development less than a decade ago. This talk briefly describes the critical aspects making large scale SiGe BiCMOS integration achievable and covers recent technology improvements and market successes at IBM.

Introduction

SiGe BiCMOS has arrived just in time to win a significant part of the booming communications marketplace. The high-speed SiGe HBT is the centerpiece of the technology, and integration with a large set of accompanying CMOS and passive devices enables high-speed integrated designs attainable in few, if any, other technology. Integration capability, together with a set of favorable device characteristics, demonstration of successful designs and products, and a more apparent market position, are drawing a growing number of designers to SiGe BiCMOS. With new designs from IBM designers and as foundry for customers around the world, a significant percent of the IBM Burlington Vermont fabrication facility is now dedicated to SiGe BiCMOS production, and is growing daily. Clearly, SiGe BiCMOS has made it out of the laboratory and into the mainstream.

Of particular note is that this technology competes with other compound semiconductor technologies, but on 8-inch wafers processed with standard silicon processing techniques. With chip sizes ranging from about 1mm to 11mm on a side, a single 8-inch wafer can yield in the range of 1,000 to 30,000 chips. With the low costs, repeatability, and high yields associated with a high-volume silicon manufacturing facility, economics of the SiGe business is no longer hard to justify.

Integration

Central to the fabrication process are the epitaxial base deposition, the self-aligned base definition, and the method of HBT integration with the CMOS devices (maintaining the CMOS device characteristic established for an IBM CMOS-only technology). Through three generations of SiGe BiCMOS technology, the HBT device structure has changed very little (only to shrink the device dimension), and the method for integration with CMOS has changed only in going from the first to second generation technology [i] to accommodate thermal cycle differences in the base CMOS technology. Maintaining such similarities between generations has, as in the CMOS model, enabled IBM to rapidly put forth successive generations of SiGe BiCMOS technologies.

Going to the third generation (characterized by its 0.18μm lithography), performance improvements have been established through aggressive lateral and vertical scaling of the device [ii, iii]. With 0.18μm CMOS deep-UV lithography, lateral shrinks were readily achieved, and resulted in reduced parasitic capacitances and resistances. Vertical scaling of the SiGe base profile, coupled with increased collector doping (Figure 1), increases the f_T performance of the device by reducing transit time and increasing Kirk-effect current density. Combining vertical with lateral scaling, both f_T and f_{MAX} values are routinely achieved at or above 90GHz in a

Figure 1: HBT vertical scaling

manufacturable SiGe BiCMOS process. Such high speed, together with smaller sizes, lower base resistance (0.4dB NF_{MIN} @ 2GHz) [iv] and low capacitances, provides an attractive device for low power (Figure 2) or low noise applications as well as high speed digital logic.

Passive devices

Even with the outstanding high-frequency gain available from the HBT device, it is often the availability of suitable passive devices that make a given design achievable in a technology. Included in this list are low TCR, tight tolerance resistors, linear high-

Figure 2: f_T across 3 SiGe BiCMOS generations

density capacitors, and high Q varactors. Probably the most leverage comes from the inductors. While inductor Q values in the range of 5 – 10 are achievable with standard CMOS interconnect, designers often require Q values above 15. Such values are realistically achievable only through low resistance (~2 mΩ/sq) metal lines, thick dielectric, and relatively high (>10 Ohm-cm) substrate resistance to minimize resistive and eddy-current losses and maximize resonant frequencies [v]. IBM has incorporated an add-on module, comprised of a thick dielectric film followed by a thick low resistance metal, in each if its technologies. This module provides both high-Q inductors and low-loss transmission lines, enabling a variety of analog designs as well as high frequency digital logic.

Enabling the Designers

The breadth of applications served by SiGe BiCMOS (including analog and digital applications at a variety of frequencies), variants in design styles and design environments required from design groups, and the extensive device offerings within the technology make providing suitable design environments a significant challenge. Products as wide ranging as single device low noise HBTs, to integrated LNAs and VCOs, to direct-conversion GPS receivers [vi] characterize the 1-2GHz RF space, and must be well predicted by this design environment. A somewhat different challenge is presented in the digital space, with products already in place which include 2.5 and 10Gbit/sec SONET, expanding into 40Gbit/sec SONET. To ensure first-pass design successes, a design environment must support schematic entry, layout verification, parasitic extraction, and accurate statistical models, and be robust enough to encompass this wide range of applications.

Challenges are substantially greater with full mixed-signal designs, which aim to combine digital CMOS ASIC logic with the high-speed analog portion of the circuit. Mixing these disparate design methodologies – high-level design with auto place and route for digital logic and highly custom design for the analog portion – is an immense challenge. Success in this arena however can put a design above the competition. A design by Intersil Corp. for 11 Mbit/sec 802.11 wireless LAN, fabricated in IBM's SiGe BiCMOS technology is one instance where chip count, power consumption, and cost is dramatically reduced from prior generation designs [vii].

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Session X

Electronic and Optoelectronic Integrated Circuits

Chair:
Dr. Miroslav Micovic
HRL Laboratories, LLC, Malibu, CA, U.S.A.

Low noise dielectric resonator PHEMT oscillator.

S. Vitusevich[a], N Klein[a], M. Winter[a], D. Schemion[a], K Schieber[b], and M. Klauda[b]

[a]Institute for Thin Film and Ion Technology, Research Center Juelich, 52425 Juelich, Germany
[b]Bosch Telecom GmbH, 71520 Backnang, Germany

An all-cryogenic oscillator based on an ultrahigh Q resonator (an unloaded quality factor $Q = 6 \times 10^6$) working in free-running regime at 23 GHz with a PHEMT amplifier was designed. The low frequency (LF) noise sources in the pseudomorphic PHEMT amplifiers were investigated at different temperatures and gate voltages under saturation bias conditions (at drain voltage Usd = 2V). The characteristics are used for the analysis of the oscillator phase noise. The measured phase noise level of the oscillator is below −110dBc/Hz at 1 kHz offset frequency.

Introduction.

Minimization of the phase noise in free-running oscillators is an important requirement in the design of microwave oscillators. Low frequency noise sources [1] in transistor amplifiers modulate the oscillation frequency and create the phase noise. In order to reach a minimum the phase noise oscillator circuit should contain a high quality resonator and a low noise amplifier with high output power. The low loss tangent of sapphire (below 10^{-7} at 77K at microwave frequencies) provides superior performance oscillators. The improvement in phase noise of a dielectric oscillator compared to the phase noise of conventional microstrip oscillator is approximately the ratio of the dielectric resonator unloaded quality factor Q to the Q of the microstrip resonator. The improvement can be as high as 30 dBc/Hz at the same offset frequency.

Experimental results and discussion.

We have developed and investigated the properties of an 23 GHz oscillators based on pseudomorphic AlGaAs/InGaAs/GaAs PHEMT amplifier and a Whispering Gallery(WG) mode resonator of 1.34 cm diameter sapphire operating at 78K. The resonator has an unloaded Q of 6×10^6 that is determined almost completely by the sapphire properties due to strong field confinement of the WG mode. A two-step electric frequency tuning consisting of a dielectric plunger moved by a piezomechanical transducer and a integrated varactor phase shifter is introduced to compensate frequency drift with temperature. A mechanical tuning range is 60 MHz and the piezomechanical fine tuning range is 50 kHz. The phase shifter allows a phase shift of 60° and can be used for phase locking and fine tuning of the oscillator.

The noise characterization of the amplifier is very important for the analysis of oscillators because phase variations of the loop which generate the phase noise arises as a result of the low frequency noise conversion by active device nonlinear elements. Our measurement of the low frequency noise spectra show that pseudomorphic PHEMT CFY 67 have better noise properties in comparison with commercial MESFET NE 710 structures at low temperatures. LF noise of the PHEMT at 100Hz and 1 kHz frequency shows about 5 dB better noise level at a temperature of 77K at Vgs = 0V. The results agree with previous measurements [2]. Therefore, the PHEMT devices have been selected for oscillator design and phase noise investigation.

Low frequency (1Hz-100kHz) noise spectra of PHEMT were measured at three temperatures 300K, 77K and 7K for various gate biases with using of a low-noise amplifier and dynamic signal analyser HP 35670A. The measurements were carried out for the onset of the saturation region of operation corresponding to a drain-source voltage Vds = 2V. The obtained results show that the intrinsic excess noise sources are 1/f flicker noise and a small Lorentz-shape generation-recombination (g-r) noise. The slope of 1/f flicker noise is very close to one and shows low oscillating dependence

with increasing gate bias. At high negative gate biases up to -0.5V the increase in noise spectral density became smaller and the slope is about the same value (equal 1). The LF noise dependence on the voltage Ugs can be due to contribution of traps from the bottom InAlAs layer to the channel transport phenomena. Contribution of the g-r noise shifts toward the low frequency range at low temperature at constant gate-source voltage Ugs. As a result, the g-r noise contribution on the phase noise at baseband frequencies above 100Hz will decrease with lowering temperature.

The sensitivity of the carrier frequency with respect to the gate bias can be minimized to a minimum phase noise by using a high Q resonator. A cryogenic two-stage PHEMT amplifier including a semiconductor varactor phase shifter and a 10 dB output coupler was designed in conjunction with a transmission mode high Q resonator. The amplification of the device was measured to be 11 dB, this value exceeds the total loss of the feedback circuit. The insertion loss of the resonator is the dominant loss in the feedback circuit and its value was optimized by tuning and coupling of the resonator to a value not higher than 9 dB. The coupling coefficient of the resonator is about 0.3-0.5, at this condition the loaded quality factor has the optimal value equal to half of the unloaded Q.

The phase noise measurement are carried out using the HPE5500 Phase noise measurement system. The figure shows the measured phase noise of the 23 GHz oscillator, amplifier biased at Uds = 2V and Ugs= -0.5V. The measurement frequency range of the phase noise is limited by thermal

fluctuations below 100Hz. As can be seen the measured phase noise of 23 GHz oscillator was -78 and -108 dBc/Hz at 100Hz and 1 kHz offset frequencies, respectively. Phase noise measurements above offset frequencies of 1kHz indicate values superior to the quartz reference source of the downconverter. Comparative measurements of two identical oscillators are in progress with temperature stability of $\pm$ 3mK. The noise in the range 100Hz - 1kHz has a slope of close to 30 dB/decade, which follows the $1/f^3$ relation due to upconversion of ideal 1/f noise dependence of the PHEMT amplifier[3].

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'CAD-simulation results of an X-band MMIC Up-Converter'

Petros S. Tsenes, Ph.D Student [1], Dr. Giorgos E. Stratakos, S. Researcher [1],
Prof. Nikolaos K. Uzunoglu [1],
Dimitris Brikas, RF Engineer [2], Ioannis Giouzelis, VLSI Engineer [2]

(1) National Technical University of Athens, NTUA
Institute of Communications and Computer Systems, ICCS
Department of Electrical and Computer Engineering
Microwave and Fiber Optics Laboratory
(2) Research and Development Division, INTRACOM S.A.

Abstract- CAD-simulation results of an active X-band MMIC Up-converter (mixer) are presented. The Up-converter was designed in the form of a double balanced mixer using the topology of the Gilbert cell and single-gate p-HEMTs. Except for the Gilbert cell, the integrated circuit contains the LO and RF baluns, which are necessary for every double balanced mixer, the dc-bias and the matching subcircuits. The input and output return losses are very low, the isolation between ports is extremely good and the mixer's conversion gain is about 2 dB.

Introduction

Although early MMICs occasionally used single-device mixers, the logical way to realize a monolithic mixer is as a balanced structure. Balanced mixers may need more devices than a single–device mixer, but the inherent isolation and spurious-response rejection of them reduces the need for filters or diplexers [1]. In an up-converter the LO frequency normally is close to the output signal band, is not rejected by the output balun of a single balanced mixer and can not be filtered. As a result a double balanced mixer is the best way to design an up-converter.

Designing

Figure 1 shows the topology of a double balanced, single-gate mixer that it is used. In the cause of simplicity the dc-bias and matching subcircuits are not shown. The RF balun is a 180-deg coupler and more specifically a reduced size "rat race" or ring hybrid. A typical ring hybrid would occupy quite a large area and as a result would be unsuitable for a MMIC design. In MMICs lumped capacitors can be easily realized and have become attractive in reducing the size of passive components [2]. Using this technique the quarter-wave sections of impedance Z_o can be replaced by sections which comprise transmission lines of characteristic impedance Z ($Z>Z_o$) and electrical length θ ($\theta<\pi/2$) and shunt capacitances C at either end (Figure 2). The size of such a hybrid is about 70% smaller than that for a conventional hybrid. Given that the LO balun, which is used to drive the upper p-HEMTs out of phase, does not need to achieve broad bandwidth we designed it in the form of an active balun (Figure 3) and as a result it occupies a much smaller area. Using the appropriate dc-bias and matching subcircuits we designed an active balun with very good phase and amplitude balance for a bandwidth over 1 GHz. The circuit does not include an IF balun due to the large area that it would occupy.

Results

Figure 4 shows the input and output return losses (s_{11} and s_{44} for IF ports, s_{22} for LO port and s_{33} for RF port). For a LO signal of $f_{LO}=9.5$ GHz and $P_{LO}=5$ dBm the 1 dB input compression point is $P_{IF}=5$ dBm where $f_{IF}=0.95$ GHz. As we have already said the conversion gain is about 2 dB and the isolation between the ports are more than 40 dB. Figure 5 shows the final layout of the Up-converter. The chip is expected to be fabricated by September 2000 through the Europractice action in the H40 GaAs MMIC process of GEC-Marconi and the occupied area is approximately 3.86 mm^2.

Figure 1. Double balanced mixer using single-gate p-HEMTs.

Figure 2. (a) Quarter-wave-long transmission section.
(b) Reduced-size circuit equivalent to quarter-wave section.

Figure 3. Active balun

Figure 4. s_{11} and s_{44} for IF ports, s_{22} for LO port and s_{33} for RF port.

Figure 5. Layout of the Up-converter.

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'An X-band MMIC Down-Converter'

Petros S. Tsenes, Ph.D Student [1], Dr. Giorgos E. Stratakos, S. Researcher [1],
Prof. Nikolaos K. Uzunoglu [1],
Dr. Michalis Lagadas, Assistant Researcher [2], G. Deligeorgis [2]

(1) National Technical University of Athens, NTUA
Institute of Communications and Computer Systems, ICCS
Department of Electrical and Computer Engineering
Microwave and Fiber Optics Laboratory
(2) Foundation for Research & Technology-Hellas, FORTH
Institute of Electronic Structure & Lasers, IESL
Microelectronics Research Group, MRG

Abstract- In this paper a MMIC mixer for RF front-end applications is described. The integrated circuit contains two p-HEMTs which are connected as a dual-gate p-HEMT, the dc-bias and matching subcircuits and a low-pass filter. It was fabricated through the Europractice action in the H40 GaAs MMIC process of GEC-Marconi and the occupied area is approximately 0.78 mm^2. The mixer's conversion gain is about 3 dB, the input and output return losses are very low and the isolation between the ports is very good.

Introduction

Mixers are the most basic elements of the superheterodyne receivers. They are used to shift signals to frequencies where they can be amplified and demodulated more effectively. In order to achieve small size, low cost fabrication and uniform performance in large quantities, microwave mixers are often realized as Monolithic Microwave Integrated Circuits. In a down-converter the LO frequency normally is far away from the output signal band therefore it can be filtered easily and as a result a balanced structure is not necessary. Although a single-gate HEMT mixer could be a design solution, a dual-gate HEMT mixer has one major advantage: the LO and RF signals can be applied to separate gates and because the capacitance between the gates is low, such a mixer has good RF-to-LO isolation [1].

Designing

Given that the H40 GaAs MMIC process of the GEC-Marconi can not support the dual-gate HEMT technology we used two single-gate p-HEMTs which are connected as a dual gate p-HEMT. Figure 1 shows the topology of the dual-gate mixer where in the cause of simplicity the dc-bias and matching subcircuits are not shown. It has been well established [2] that the best mode of operation of a dual-gate mixer is one in which the LO drives the lower HEMT into and out of current saturation over the LO cycle. The upper HEMT is in current saturation over most of the LO cycle and operates simultaneously as a source-follower amplifier for the LO and a common-gate amplifier for the IF.

Measurements

A coaxial test-jig was developed in order to perform measurements which otherwise would need several microwave probe heads in on wafer probe testing environment. The substrate which was used is the low cost R4003 Rogers teflon-like material, gold plated, on which thermosonic gold ball wirebonding was performed at 100°C by a Wedge Border. High purity (99.9999%), 25 μm in diameter Au wire have been used for making the appropriate connections. Figure 2 shows the input return losses (s_{11} for LO port and s_{22} for RF port). Figure 3 shows the conversion gain vs. the power of the LO signal and it is obvious that for P_{LO}=3.5 dBm the conversion gain reaches its maximum value. The conversion gain vs. the power of the RF signal is shown in Figure 4 and it can be seen that the 1 dB input compression point is P_{RF}=-7 dBm. Moreover it was measured that IIP3=-1 dBm and NF(SSB)=11 dB. The results are shown in Table 1 and in Figure 5 a photo of the chip is presented.

Figure 1. Dual-gate HEMT mixer

Figure 2. s_{11} for LO port and s_{22} for RF port

Figure 3. Conversion gain vs. P_{LO}

Figure 4. Conversion gain vs. P_{RF}

Figure 5. Photo of the chip

Conversion gain	3.5 dB
1 dB input compression point	-7 dBm
IIP3	-1 dBm
NF (SSB)	11 dB
Input return losses at RF port (9.95 GHz<f_{RF}<10.65 GHz)	<-10 dB
Input return losses at LO port (8.00 GHz<f_{LO}<10.65 GHz)	<-10 dB
Output return losses at IF port (f_{IF}<2 GHz)	<-10 dB
LO-IF isolation	>28 dB
RF-IF isolation	>15 dB

Table 1. Down-converter's specifications

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Advances in Integrated Six Port Direct Digital Millimetre Wave Receivers

Tiberiu M. Visan, Jacques Beauvais*, Yansheng Xu, Philippe Jacquet and Renato G. Bosisio

*Centre de Recherches Avancees en Microondes et en Electronique Spatiale (Poly-Grames)
Departement de Genie Electrique et de Genie Informatique Ecole Polytechnique de Montreal
Montreal , Qc. Canada, H3V1A2 e-mail: rbosisio@grmes.polymtl.ca*

**Groupe de Recherche sur les Semiconducteurs
Departement de genie electrique, Universite de Sherbrooke
Sherbrooke, Qc. Canada, J1K2R1*

Abstract

This paper provides technical results and describes fabrication means used to design, fabricate and test new MMIC six port direct digital millimetre wave receiver in a work environment equipped with appropriate circuit design and test means, in-house thin film MHMIC fabrication facility and standard commercial (external) MMIC foundry services. However, the latter services were in general found unsatisfactory, for the development of new MMIC chips, mainly due to slow runs with minimum turn around times of 6 months. The approach now adopted is first to simulate new direct digital six port receiver architecture in system and circuit simulators (e.g. SPW and MDS), followed by rapid in-house MHMIC runs and new in-house (breadboard) MMIC fabrication using electron microscope e-beam lithography in combination with commercially available lattice engineered GaAs wafers. Results are given on a new six port receiver architecture, and in-house HEMT processes to provide breadboard MMICs for use in receiver demonstrator modules targeting mass market applications.

Introduction

Six-port cicuits at first introduced for instrumentation and measurement purposes (1) have recently been shown to posses interesting features as direct digital millimetre wave receivers (2,3,4,5). A rapid and successful integration of six ports and ancillary circuits into a MMIC chip/ demonstrator module can offer six port technology (SPT) an opportunity to penetrate mass market millimetre wave applications including telecommunications, imagery, radar, signature recognition, sensors, built-in tests and so forth. The six port circuit is a relatively simple linear network with two RF input ports and four RF output ports (6).The four output ports are terminated by power level measuring means to satisfy response time, frequency range and power level requirements in any given application. Schottky diodes are often used for power level measurements, and these diodes are integrated to the six port circuit along with other RF and base band operating circuits to achieve a high level of integration as may be needed for receiver front ends, etc. The four power levels are measured simultaneously, and these values are used to calculate the vector relationship between an **unknown** RF signal introduced at one RF input port and a **known** RF signal introduced at second RF input port. The six-port and ancillary circuits are designed with standard circuit simulators based on micro-strip or CPW transmission lines. A bench top six port direct digital receiver, designed and fabricated in hybrid technology, has been recently operated with digital signal processing, at carrier frequencies of 20Ghz and 30Ghz with receiver bandwidths of several GHz and channel bandwidths of 40 MHz using QPSK modulation at bit rates of up to 80 Mbps. (7). A new six port architecture given in Fig 3 provides a means to operate receiver with simple and rapid analogue signal processing means. Initial results obtained with hybrid circuit design (fig.1 & 2) validate this approach. In addition, SPT offers a means to incorporate in this receiver a means to suppress adjacent channel interference(8). Successful breadboard MMIC processes on PHEMT GaAs lattice engineered material obtained from Picogiga

including HEMT devices, CPW transmission lines (fig 4) will provide the capability to enhance overall performances in terms of LO to RF leakage, dynamic range and noise figure over the classic architecture. The final objective in this research program is to develop a Rx/Tx chip based on SPT for use at millimetre wave frequencies (e.g. 30GHz, 60GHz).

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Fig.1 Planar 6-Port (K_a Band 26-30 GHz)
(Branch-Line Variant)

Fig.2 Planar 6-Port (K_a Band 26-30 GHz)
(Rat-Race Variant)

Fig.3

MMIC 6-Port
Small size 1.4 x 1.6 mm
K Band (16-20 GHz) Six-Port

Fig.4 a

Fig.4 b

PHEMT Device
4a. T-Shape Layout for GaAs Phemt (f_t ~90 GHz)
4.b Detailed View For Gate Deposition (0.2 um)

Vertically Integrated Transistor-Laser Structure, take 2

R.C.P. Hoskens, V.I. Tolstikhin*, A. Förster**, T.G. van de Roer,

*Eindhoven University of Technology, Faculty of Electrical Engineering,
P.O. Box 513 - EH8, NL-5600 MB Eindhoven, The Netherlands.
E-mail: t.g.v.d.roer@tue.nl, R.C.P.Hoskens@tue.nl
*Now at: Optiwave Corp., Nepean, Ont., Canada
**I.S.I Jülich, Germany*

1. Introduction

The purpose this project is to realise carrier temperature modulation in a laser by means of a novel vertically integrated transistor-laser structure in which the electrons are injected into the active region of the laser via the emitter-base part of a bipolar transistor and heated in a high-field region before entering the active layer. At WOCSDICE99 the results of the first design were presented [1], revealing several weaknesses in the design. To correct this several changes were made and a new wafer was grown at the ISI in Jülich and processed in Eindhoven.

2. Modeling and Design

The previous results required a redesign of the epitaxial layer stack, to increase the injection efficiency of the carriers into the Active Layer and to prevent holes in the AL from leaking through the Launcher into the p-Base. The thickness of the launcher is reduced to 50 nm and it is split up into three separate layers:

1. Pre-Launcher, graded AlAs mole fraction from 10 to 30 %: increases the electron injection efficiency by decreasing the conduction band potential barrier from Base towards Launcher
2. Launcher, AlAs fraction increased to 30 %: controlled acceleration of the electrons going from Base towards Active Layer by using most of the applied collector-base voltage to increase its transversal electric field
3. Post-Launcher, AlAs fraction increased to 30 %: decreasing the hole leakage current by increasing the valence band potential barrier from Active Layer towards Launcher

Fig. 1. Left: *Simulated Energy Band diagram at I_E=75mA & V_{CB}=1.25V. Left: Collector.*
Middle: BAL (0.34μm), Launcher (0.38-0.43μm) & Base (0.46μm). Right: Emitter.
Right: *Simulated L-I curves $L(I_E)$ [V_{CB}=0, 0.1, 0.2, 0.5, 1.0 & 1.25V]. Length FP cavity=500μm, internal losses=2.5 cm^{-1}, $R_{ES,BS}$=2 Ω, R_{CS}=2 Ω*

The composition of the Active Layer is changed from GaAs to InGaAs with 8% InAs to increase the valence band potential barrier. The longer emitted wavelength of approximately 945nm at 300K decreases the optical absorption inside the base. A higher AlAs fraction of 10% in the AlGaAs base decreases the conduction band potential barrier towards the Launcher.

To model the electrical characteristics extensive use was made of the commercial simulator LASTIP. Results are shown in Fig. 1. Since this cannot model carrier heating effects the transport problem for electrons travelling over the high electric field region is solved as before by the Monte Carlo technique [2].

3. Device Technology
Up to this moment it was not possible to make good ohmic contacts to the p-type base, perhaps because the base doping has been considerably reduced compared to the first wafer.

4. Optical measurements
At room temperature only spontaneous emission was observed. The spectrum showed one peak corresponding to the InGaAs bandgap. This means that radiative recombination in the base is negligible, contrary to the first design where a large part of the injected electron current was lost by recombination in the base.

At 80 K laser action was observed with a threshold current density of about 1.3 A/cm^2. This indicates an unknown source of excess optical absorption. The spectrum is shown below.

Fig. 2. *Spectrum of the lasing device at 80 K, centered at 892 nm.*

5. Electrical measurements
The results of electrical characterisation are in reasonable agreement with the predictions of LASTIP. In particular there was no sign of holes leaking from the active region across the launcher into the base.

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OPTIMISED TRANSCEIVER FOR FIBER TO THE HOME APPLICATIONS

J. Harari, D. Decoster
IEMN, Av. Poincaré, Villeneuve d'Ascq, France

F. Mallecot, J. Jacquet, A. Leroy, A. Plais, C. Chaumont
OPTO+, Alcatel Alsthom Recherche, Route de Nozay, Marcoussis, France

F. Doukhan, Y. Arnaudin
ALCATEL OPTRONICS, Route de Villejust, Nozay, France

F. Laune, A.L. Convert
RADIALL, ZI Chesne Tharabie, St Quentin Fallavier, France

Until now, the technology used to design the optical modules to be used in a service access network was those of the long haul applications. Indeed, each module is inserted in the network far from the user and its final cost is supported by all users. But this situation is strongly modified by the actual need to use optical modules closer to the end user in the frame of Fiber To the Home Applications. In these conditions, the module fabrication cost is supported by a single user and the necessary effort to reduce this cost leads to consider the integration of the different photonic and optoelectronic devices on a single substrate. At the same time, a set of common specifications was established by the Full Service Access Network (FSAN) group [1] in order to intensify the production of equipments and decrease the costs. These specifications are, in particular, a transmitter emitting close to 1.3μm wavelength while the receiver operates around 1.55μm wavelength. The different solutions merging actually to satisfy these requirements are the Planar Lightwave Circuit (PLC) and the Photonic Integrated Circuit (PIC). In the first case the different optoelectronic devices are flip-chip mounted on a Silicon board with Silica waveguides. The performances are high as [2] there is no compromise between the components but the necessary difficult alignment manipulations limit the fabrication cost decrease. In the second case, all components and needed waveguides are monolithically integrated on a single InP substrate. A technological effort has to be carried out in order to reduce the interactions between the different devices and get sufficiently high performances.

Among the different PIC transceivers already reported, the in-line device is promising because of its compactness. The device presented in this paper has been optimised in the frame of the french RNRT (Réseau National de Recherche en Télécommunication) project TANIA (Terminal d'Accès Numérique InterActif). As showed in Figure 1, it is constituted of a 1.3μm DFB laser, a 1.3μm absorber with the same epitaxial structure, and a photodetector for 1.55μm wavelength with a but-coupled transition [3].

Figure 1. Structure of the optimised integrated transceiver

The active region of the laser and absorber uses nine strained layers multiquantum well. The laser is a Buried Ridge Structure while the absorber and the photodiode are only ridge structures. The photodiode epitaxial structure is independent of the laser structure and has been optimised in order to absorb the whole optical signal at 1.55µm wavelength, and also to minimize the optical losses occuring at the but-coupling transition. The ridge width (the same for the absorber and the detector) has been chosen in order to minimize lateral perturbation due to the transition between the BR structure and the ridge structure. This optimisation done by Beam Propagation Method allowed to obtain a receiver responsivity of 0.3 A/W from light in fibre with a low sensitivity to optical polarisation, the transceiver being mounted in a TO connectorized module [4]. At 1.3µm wavelength, the problem is to reduce the optical signal issued from the laser and perturbing the photodiode. The 1.3µm signal due to stimulated recombinations is guided in the ridge absorber and absorbed. The absorber of the device is used as a monitoring diode. However the 1.3µm non-guided signal due to spontaneous recombinations and the non-guided optical beams due to the laser-absorber transition must be absorbed. This is why we introduced GaInAs epilayers below and on top of the epitaxial structure. Thanks to this optimisation, the FSAN class C sensitivity (-33 dBm) was reached in Full-Duplex operation at 155 Mbit/s, using a laboratory module. This is a promising performance obtained for the first time with a PIC approach.

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Design and fabrication of a new optical switch for the synthesis of large time delays

Yves HERNANDEZ, Jean Pierre VILCOT, Joseph HARARI,
Didier DECOSTER, Michel SCHALLER*, Jean CHAZELAS*

*Institut d'Electronique et de Micro-électronique du Nord
U.M.R. C.N.R.S. 8520, Avenue Poincaré B.P. 69
59652 VILLENEUVE D'ASCQ, France.
Tel: +33 320 197 991 yves.hernandez@ienm.univ-lille1.fr*

**With THOMSON DETEXIS Photonics & Advanced Technologies Department
La clef de Saint-Pierre, 1Bd Jean-Moulin
78852 ELANCOURT Cedex, France.*

Abstract :

A current concern in optical systems (such as active antennas, optical communication networks,…) is to dispose of an optical switch with low electrical consumption, low optical losses and crosstalk. We focus on the fabrication of a 1 to N optical switch that will be the principal element of a final matrix for the synthesis of high dynamic true time optical delays.

We will present the design and the fabrication of an original electro-optical 1 to 2 Cascade Switch based on InP technology. The Cascade Switch (CS) principle of operation allows 1 to N architectures with only one single current injection for the selection of the optical path.

The first characterisation results, especially the low electrical consumption (about 50mA for a 13dB crosstalk and 20dB in the passive state), show that this device is promising for low electrical power consumption and so far its integration in complex optical systems such as optical switching matrixes.

The Cascade switch design and operation mode :

These components are made on a n+ doped InP substrate, which is transparent around the working wavelength of 1.55µm. An InGaAsP ($\lambda c = 1.15$µm) layer is deposited by MBE (Molecular Beam Epitaxy) as the core of the guides with a refractive index of 3.315 between two InP cladding layers (refractive index: 3.17). The optical mode profile of our passive guides has been calculated using a 2 dimensional modal analysis and is illustrated in the figure1. Rib dimensions are 4.5µm wide and 0.3µm height.

Figure 1: optical mode profile of a passive guide

Figure 2: Schematic view of 1 to 2 Cascade Switch

The easiest CS to describe is the 1 to 2 switch. It is composed of three parallel optical waveguides. The first and the third ones (thinner on Figure 2) are passive guides, whereas the central one is a current injection zone, which enables or disables the optical coupling between the two other guides. When no current is injected in the central waveguide, the light is coupled from the top to the bottom waveguide. To prevent this passive coupling, current is injected in the middle waveguide: so, the refractive index decreases with the carrier injection and the light continues on the top waveguide. This topology can be applied to the realisation of 1 to N switches without increasing the number of electrical polarisation points with the number of optical paths.

Modelling of the Cascade switch:

The light propagation is modelled using a 2D and 3D FD-BPM. The 2D FD-BPM coupled with an effective index method allows a fast simulation of our components and can be coupled with optimisations methods as genetic algorithms. In the figures 3a & 3b are shown the two operation states of our component simulated with a 2D FD-BPM,

**Figure 3a: Passive coupling between guides
No current injected in central guide**

**Figure 3b: Coupling cancelled by current
injection in central waveguide**

Technological process:

The technological process consists of 4 lithography levels : an e-beam direct writing (waveguides definition) and three UV photo lithography levels (electrodes definition, optical isolation holes and first metallization).

1 to 2 cascade switches have been made in compact configuration : all waveguides are side joined in the coupling region. This topology is almost simply fabricated since it looks like the one of the a Multi-Mode Interferometer.

Characterisation:

The device has been characterised at 1.55µm wavelength. Without any injected current, a crosstalk around 20dB is obtained; in this case light is coupled such as in figure 3a. For an injected current close to 50 mA, light is no more coupled and goes on straight such as shown in figure 3b, crosstalk is then around 13dB. In between these 2 extreme values the switch behaves as a variable rate coupler. As an example, 50/50 power divider is obtained for 18 mA of injected current.

**Figure 4 : Optical crosstalk versus injection current in central waveguide
Insets: output beams (@ 1.55µm) corresponding to the switching state of device**

Conclusion:

1 to N optical switches have been fabricated based on a « cascade » design. Example of 1 to 2 switch is reported from design to fabrication. Crosstalk around 13 dB has been obtained for 50 mA control current.

NOTES

Session X: Electronic and Optoelectronic Integrated Circuits

NOTES
Session X: Electronic and Optoelectronic Integrated Circuits

Session XI

Reliability of HEMTs and HBTs

Chair:
Prof. George I. Haddad
The University of Michigan, Ann Arbor, MI, U.S.A.

Characterization and reliability of InP-based HEMTs implemented with different process options

G. Meneghesso, R. Luise, D. Buttari, A. Chini, H. Yokoyama*, T. Suemitsu*, E. Zanoni

Dipartimento di Elettronica e Informatica and INFM, Universita di Padova, Via Gradenigo 6/A 35131 PADOVA, Italy; tel. +39-049-8277653, fax: +39-049-8277699, e-mail: gauss@dei.unipd.it
*NTT Photonics Laboratories, 3-1, Morinosato-Wakamiya Atsugi-shi, Kanagawa 243-01, Japan

The high performances properties of InAlAs/InGaAs/InP High Electron Mobility Transistors (HEMTs) are already well known in particular for very high frequency and low noise applications [1,2]. Unfortunately, quite often, these devices suffer from parasitic phenomena like kinks in the output I-V curves and of parametric degradation after aging at high bias regime [3,4].

In this paper we will present a study concerning InAlAs/InGaAs HEMT devices with different process properties. All the studied devices, which structure is described in [5], were lattice matched HEMTs grown on InP with a standard recess region width $L_{gC} = 0.1 \mu m$ (distance between CAP and gate contact). We have investigated five types of devices characterized mainly by the following differences: **A)** Devices WITH the InP etch stopper layer; **A1)** The InP stopper layer is present in the whole device active area and the gate is placed over the InP, or **A2)** the InP stopper is present in the whole device active area but not under the gate that contacts the InAlAs barrier layer. **B)** Devices WITHOUT the InP etch stopper layer; **B1)** The InP stopper has not been grown during the device processing, using a $L_{gC} = 0.02 \mu m$. A previously grown InP stopper layer, between the CAP and the barrier, has been removed in the access region by a subsequent etching process step. By using two different etching times, devices with standard L_{gC} **B2)** or $L_{gC} = 0.02 \mu m$ **B3)** have been obtained.

Kink effect is observed in devices with the removed InP stopper and standard L_{gC} (Fig. 1), while in devices with the InP stopper layer or those with $L_{gC} = 0.02 \mu m$ the kink effect is strongly reduced (Fig. 2, 3).

The typical bell shape in the I_G vs V_{GS} curves due to impact-ionization is observed in all the devices, see for instance Fig. 4. This result confirms that hole pile-up at the source side alone can not induce kink effect and that, as discussed in [6], if both hole pile-up and traps in the access region are present, kink effects are observed in the output I-V curves. In devices having a standard L_{gC} and without the InP etch stopper layer, traps in the gate-source and gate-drain access region can become negatively charged due to capture of electrons. This negative charge reduces I_D at low V_{DS}. At increasing V_{DS} the modification of potential profile in the source-gate recess region, caused by the compensation of the negative trapped charge by holes generated by impact ionization and/or field assisted electron detrapping, leads to a recovery of the drain current thus originating the kink effect. Devices adopting the InP etch stopper layer or with $L_{gC} = 0.02 \mu m$ are almost free from surface traps, and therefore kink effects are strongly reduced even in the presence of impact ionization.

Transconductance frequency dispersion has been observed only in the devices showing kink effects (see Fig. 5). By means of $g_m(f)$ measurements carried out at different temperatures an activation energy of $0.28 \pm 0.03 eV$ has been obtained.

Hot electron stress tests also demonstrate that the InP stop etch layer improves the long-term stability of HEMTs. Enhancement of the kink effects (Fig. 6) and increase in the $g_m(f)$ dispersion (not shown) were observed in devices without the InP etch stopper and standard L_{gC} after hot electron life tests, indicating surface states enhancement in the access region as degradation mechanism. These degradation effects were not observed in devices with the InP etch stopper layer, see for instance Fig. 7. Devices without the InP etch stopper layer and with $L_{gC} = 0.02 \mu m$ present a slight degradation (without appearance of any remarkable kink) after hot-electron stress test (see Fig. 8). The degradation is completely recovered after few hrs of unbiased storage at room temperature. It must be stressed, however, that to suppress kink effects and degradation phenomena, the use of the InP stop layer must be preferred to the use of narrow ($L_{gC} = 0.02 \mu m$) recess region, due to the negative effects on the breakdown properties of the narrow gate recess region [7].

In conclusion data presented here show that the free InAlAs surface is responsible for the observed instabilities (kink effects, $g_m(f)$ dispersion), and that the InP "passivating" layer contributes to suppress kink effects and to improve the long term stability of in InP-based HEMT's.

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Fig.1: Output I-V curves obtained in a **B2** device (removed InP).

Fig.2: Output I-V curves obtained in a **A2** device.

Fig.3: Output I-V curves obtained in a **B3** device (removed InP and $L_{gC} = 0.02\mu m$).

Fig.4: I_G vs V_{GS} curves in a typical device.

Fig.5: Normalized trasconductance vs frequency dispersion.

Fig.6: Output characteristics before (solid line) and after (dashed) hot electron stress test in a **B2** device (removed InP).

Fig.7: Output characteristics before (solid line) and after (dashed) hot electron stress test in a **A2** device.

Fig.8: Output characteristics in a **B1** device (without InP and $L_{gC} = 0.02\mu m$). Before stress: solid lines. After stress: dashed lines. After stress and few hours of recovery: dash-dotted lines

Reliability of GaInP/GaAs HBTs for Power Applications

H. Blanck, K. J. Riepe, W. Doser, and D. Pons

*United Monolithic Semiconductors GmbH,
Wilhelm-Runge-Straße 11, 89081 Ulm, Germany*

A reliable HBT process has been developed for the very demanding operating conditions required for high power X-Band applications. Due to its intrinsic qualities this process can naturally also be used for other applications, including low-frequency amplifiers for mobile communications, low phase-noise oscillators or mixed-signal circuits for optical communications. The process is based on commercial GaInP-emitter structures, and the fabricated device life-time has been extensively tested. Aging tests on power devices at Tj=250°C and Jc=40kA.cm-2 are still running after 3000 hours without degradation. A conservative extrapolation with an activation energy of 1eV yields an MTF above 1 million hours for Tj=125°C and Jc = 20kA.cm-2..

Experiment

The reliability of the transistors has first been evaluated on single-finger devices through on-wafer, strongly accelerated stress tests. This allowed for a much faster feed-back on process step optimization, and contributed to a rapid convergence to a reliable technology. A special test bench has been developed for this purpose (fig. 1). It features a thermally regulated chuck for high junction temperature stress, and dedicated probe cards allowing the simultaneous test of 6 devices. The probe cards include special biasing network to guaranty a stable operation of the devices. This is especially important for on-wafer testing of RF devices, which have a natural tendency to oscillate. Nevertheless, for each test the absence of parasitic oscillations was controlled with a spectrum analyzer.

Figure 2 shows the evolution of the current gain measured during a test at a junction temperature of 250°C and a current density of 80kA.cm-2 for an AlGaAs-emitter HBT. The figure shows the typical catastrophic degradation mechanism observed on this type of devices. In comparison, Figure 3 shows the evolution of the current gain measured during a test at a junction temperature of 275°C and a current density of 120kA.cm-2 for an GaInP emitter HBT. Aside from the emitter etching the two types of devices were fabricated using the same process steps. No catastrophic degradation has been observed showing the excellent quality of the material as well as the technology. InGaP-emitter HBTs have long suffered from the poor quality of the material commercially available, but similar tests on material from different suppliers did not result in any catastrophic degradation. This shows the good maturity now reached by this material system. However, some differences could be observed on transistors fabricated on material from different origins, especially in the early stage of the tests (Figure 4, Note that all wafers were processed in the same batch, excluding any difference related to the process).

To confirm the results obtained on-wafer, and to verify the reliability of the transistors for power applications, regular stress tests were performed on large power devices. The devices were mounted in carriers able to dissipate the necessary power, and were then placed in an oven at a regulated ambient temperature. Tests are running at junction temperatures ranging from 175°C to 250°C with current densities of 40 to 80kA.cm-2, and have reached up to 3000 hours (fig. 5 and 6). It was up to now not possible to extract an activation energy. However, a worse-case extrapolation with a conservative 1eV yields an MTF above 1 million hours for Tj=125°C and Jc = 20kA.cm-2.

Figure 1: On-wafer accelerated stress test set-up.

Figure 2: On-wafer aging test. Single-finger AlGaAs/GaAs HBT. Tj = 250°C - Jc = 80kA.cm-2. Material supplier A.

Figure 3: On-wafer aging test. Single-finger GaInP/GaAs HBT. Tj = 275°C - Jc = 120kA.cm-2. Material supplier A.

Figure 4: On-wafer aging test. Single-finger GaInP/GaAs HBT. Tj = 275°C - Jc = 120kA.cm-2. Material supplier C.

Figure 5: On-carrier aging test. 8-finger GaInP/GaAs power HBT. Tj = 200°C - Jc = 80kA.cm-2. Material supplier A.

Figure 6: On-carrier aging test. 8-finger GaInP/GaAs power HBT. Tj = 250°C - Jc = 40kA.cm-2. Material supplier A

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Session XI: Reliability of HEMTs and HBTs

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Session XI: Reliability of HEMTs and HBTs

Session XII

THz Sources, Diodes, and Receivers

Chair:
Prof. Hartwig W. Thim
Johannes-Kepler-Universität Linz, Linz, Austria

Recent Advances in Two-Terminal Devices for mm-Wave and THz Applications

H. Eisele and G. I. Haddad

Center for High Frequency Microelectronics
Solid-State Electronics Laboratory
Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, Michigan 48109-2122

Abstract

Systems for rapidly emerging applications at millimeter-wave and THz frequencies such as upper atmospheric imagery, remote sensing, high-resolution near-object analysis, and ultra wide bandwidth intersatellite communications require reliable and compact RF sources with low DC power consumption as one of their key components. This paper reviews the power generation capabilities and basic properties of different two-terminal devices as fundamental RF sources as well as various approaches to CW RF power generation at submillimeter-wave and THz frequencies. As shown in Figures 1–3, CW RF power generation at frequencies above 200 GHz has been demonstrated with Si and GaAs IMPATT diodes, InP Gunn devices, GaAs TUNNETT diodes, superlattice electronic devices as well as resonant tunneling diodes. At frequencies up to 300 GHz, Si IMPATT diodes yielded the highest power levels from any fundamental source with solid-state devices, but are considered to be too noisy for some system applications. InP Gunn devices, however, demonstrated excellent noise performance and generated more than 1 mW around 315 GHz, which are the highest RF power levels from any single solid-state device above 300 GHz. Operation as an efficient self-oscillating frequency multiplier resulted in RF power levels of more than 10 mW from a low-noise TUNNETT diode at 202 GHz. The potential of these and other two-terminal solid-state devices for power generation at these frequencies will be discussed and compared with the performance of frequency multipliers, which is shown in Figure 3.

For example, improved heat dissipation in InP Gunn devices resulted in RF power levels exceeding 200 mW, 130 mW, 80 mW, and 25 mW at oscillation frequencies of around 103 GHz, 132 GHz, 152 GHz and 162 GHz, respectively. Power combining increased the available RF power levels to more than 300 mW at 106 GHz, around 130 mW at 136 GHz, and more than 125 mW at 152 GHz. These RF power levels were generated in the fundamental mode and are the highest reported to date from any Gunn device. Due to their fast primary carrier injection mechanism, TUNNETT diodes are another prime candidate for RF generation at millimeter-wave and THz frequencies. RF power levels of 100±5 mW at 100–107 GHz in the fundamental mode were obtained from GaAs TUNNETT diodes. As shown in Figure 4, GaAs TUNNETT diodes yielded the lowest FM noise measure compared to any other oscillator with two-terminal devices at W-band frequencies.

Fig. 1. Published state-of-the art results from Si and GaAs transit-time diodes under CW operation in the frequency range of 30–400 GHz. Numbers next to the symbols denote dc-to-RF conversion efficiencies in percent.

Fig. 2. Published state-of-the art results from GaAs and InP Gunn devices under CW operation in the frequency range of 30–400 GHz. Numbers next to the symbols denote dc-to-RF conversion efficiencies in percent.

Fig. 3. Published state-of-the-art results from frequency multipliers with GaAs Schottky-barrier or InP-based heterojunction-barrier varactor diodes in the 100–1000 GHz frequency range in comparison with published state-of-the-art results from GaAs TUNNETT diodes, InP Gunn devices, and RTDs above 200 GHz.

Fig. 4. Comparison of the FM noise measure in free-running oscillators with different two-terminal devices at millimeter-wave frequencies of 75–155 GHz.

Development of GaN-based Gunn-Effect Millimeter-Wave Sources

E. Alekseev, A. Eisenbach, D. Pavlidis, S.M. Hubbard, and W. Sutton

Department of Electrical Engineering and Computer Science,
The University of Michigan, Ann Arbor, MI 48109-2122, USA
Tel: (734) 647-1778, Fax: (734) 763-9324, E-mail: yegor@umich.edu, pavlidis@umich.edu

Theoretical and experimental studies conducted for the purpose of development and optimization of GaN-based Gunn diodes for THz are reported. GaN Gunn-diode oscillators with *0.3μm*-thick GaN diodes are expected to have fundamental frequency of *750GHz* and power density of $3 \times 10^5 W/cm^2$. GaN In an effort to verify the experimental characteristics of GaN Gunn diodes, device layers were grown by MOCVD and special device patterns have been developed. On-wafer characterization of the fabricated GaN negative differential resistance (NDR) diodes revealed increased power capability compared with GaAs Gunn devices The processing necessary for realization of such diodes with increased power handling is also addressed.

Theoretical and experimental studies of electron transport in GaN-based semiconductors indicate that electron *v-F* characteristics in these materials exhibit inter-valley electron transfer at high electric fields [1,2]. The threshold field in GaN is much higher than that of GaAs (~*150KV/cm* vs. *3.5KV/cm*) promising increased power and frequency capabilities for GaN-based Gunn-effect devices. Based on the above considerations it is attractive to explore the use of III-V Nitrides in Gunn devices for THz signal generation.

A first analysis of microwave potential of GaN-based Gunn diodes was recently reported by the authors and demonstrated significant power and frequency improvements over conventional III-Vs due to increased electrical strength, reduced relaxation times, and increased electron velocity in GaN [3]. This work further extends these studies of GaN Gunn diodes to include studies of the possibility of THz generation using GaN. Recent progress in the development of GaN-based Gunn devices using GaN layers grown by MOCVD at the University of Michigan is also presented in this work.

The frequency and power capability of GaN-based millimeter-wave sources was evaluated using large-signal harmonic analysis based on energy-balance device simulations. GaN material parameters used for this purpose were based on previously reported characteristics of GaN-based devices [3,4].

Figure 1. Schematics of GaN Gunn source and its power spectrum showing fundamental operation at *750GHz*

A schematic of a proposed THz source based on GaN Gunn diode is shown in Figure 1. The design features a thin and highly doped active layer (*0.3μm, $8 \times 10^{17} cm^{-3}$*) and, thus, it is expected to operate at a much higher frequency than currently available using GaAs devices. A power spectrum of

the THz GaN Gunn oscillator was obtained by harmonic analysis showed fundamental frequency of ~750GHz and a conversion efficiency of ~1%. This high frequency capability of GaN is due to short relaxation times, high electron velocity, and large threshold field in this material.

A GaN diode with $3\mu m$-thick active layer and doped at $1 \times 10^{17} cm^{-3}$ designed to operate a W-band frequency range was selected for the purpose of experimental verification. GaN Gunn layers were grown on sapphire substrates in the in-house MOVPE system at an ambient temperature of $1120°C$ and a growth rate of $1.4\mu m/hour$. Integrated devices for on-wafer testing were fabricated on isolated circular mesas using dry etching techniques and Au plating for airbridge interconnects and heat sinks as shown in Figure 2a. The fabricated GaN devices were characterized using pulsed I-V measurement system to eliminate influence of self-heating due to presence of sapphire substrates. Characteristics of GaAs Gunn diodes were also measured and shown in Figure 2b for comparison purposes. Obtained results indicated that current and voltage capabilities of GaN Gunn diodes significantly exceed that of GaAs devices, but a more efficient heat-removal techniques, such as substrate removal or flip-chip bonding on AlN substrates are necessary for complete RF testing.

Figure 2. (a) SEM photograph of a fabricated GaN Gunn diode and (b) pulsed IV characteristics of GaN Gunn diodes demonstrating increased voltage and current capabilities compared with GaAs devices.

Overall, large-signal numerical simulations were performed to investigate a possibility of THz signal generation using GaN-based Gunn diodes. Based on the results of the large-signal simulations, GaN NDR layer structures were designed and grown by MOCVD at the University of Michigan. On-wafer characterization of the fabricated GaN NDR diodes revealed increased power capability compared with GaAs data. More efficient heat removal techniques necessary for reliable RF operation are currently under development.

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Challenges for a Terahertz solid state heterodyne receiver

D. Lippens, T. David, F. Podevin, X. Mélique, M. Fernandez, T. Akalin, P. Mounaix, and O. Vanbésien

Institut d'Electronique et de Microélectronqiue du Nord
Université de Lille1
Avenue Poincaré, BP 69, 59 652 Villeneuve d'Ascq Cedex, France
Corresponding author: Didier.Lippens@IEMN.univ-Lille1.fr

Abstract: **The theoretical and experimental works carried out at IEMN towards the realisation of a heterodyne receiver in the Terahertz gap are presented. From the theoretical side, this concerns mainly the ability of the devices to operate at such ultra high frequencies, studied through quantum and Monte Carlo calculations. From the technological view point, the challenges for planar integrating the devices in a discrete or distributed fashion within the circuit block are more specially addressed.**

1. Introduction:

The interest in the Terahertz gap is dramatically increasing nowadays with potential applications in the medical, environment, space and telecommunication fields. Up to now, two routes have been investigated for reaching the far infrared spectrum namely a full electronic solution or an opto-electronic one [1]. For the former, impressive results have been obtained recently at mm- and sub-mm wavelengths notably with the emergence of highly non linear devices fabricated from semiconductor heterostructures. However serious bottlenecks still exist towards the development of a solid state transceiver which can operate, at room temperature, at frequencies as high as 1 THz. In this communication, we investigate the main challenges we are facing towards this goal on the basis of theoretical and experimental works carried out at the University of Lille.

2. Theoretical issues

For illustration of the effort carried in this field let us consider the two generic functions of up- and down-conversion of a mm or sub-mm heterodyne receiver. For the former, the so-called Heterostructure Barrier Varactor (HBV's) appears quite attractive for high frequency-moderate-power triplers starting from a Gunn source or from a multiplied stabilised source. Its advantages with respect to Schottky varactor counterpart are now widely recognised in terms of functionality and power handling afforded by the intrinsic symmetry in the C-V curve and the ability to stack several barriers during epitaxial growth. We thus demonstrate recently the highest output power reported so far for such a device operating at 250 GHz [2]. In order to further increase such a performance by pushing as an example the frequency of operation, the doping level becomes a key figure of merit. In fact, increasing further the displacement current via a frequency increase leads to saturation effects which can be alleviated via a doping increase. These saturation effects have been early studied in injection and transit time devices and were recently revisited for HBV's [3]. Monte Carlo simulations, which take into account non stationary dynamic effects, are found particularly suitable for analysing such limitations. Based on the simulations performed at Lille University, it was demonstrated that an efficient modulation of the depleted zone can be preserved at Terahertz frequency On the other hand it could be helpful to see whether a full displacement current mode could more adapted to ultra-high frequency operation. Such an operation relies on the displacement of charges in a closed system in a manner similar to charge coupled devices (Fig. 1). with however critical time dependent behaviour as a function of trapping and escaping processes. For devices in the conductive mode such as those employed in down conversion through heterodyning the main limitations stem from tunnelling processes [4]. In order to illustrate such an issue we studied the ideality factor and built-in potential for a Metal/InAlAs/InGaAs mixing structure as a function of the InAlAs barrier thickness. Intrinsically, various quantum conduction regimes can be found explaining an optimum at ~10 nm.

Technological challenges

One of the main requirements for fabricating the devices aimed at operating at Terahertz frequency is the shrinking in their dimensions. On the other hand, the parasitics elements have to be maintained at the lowest level possible taking advantage of finger shaped patterning, T-shaped contacts and deep etching [4]-[5]. It is also

imperative to interconnect the devices to the circuitry via low capacitance air bridges. Also, transfer or membrane-like techniques could be useful for alleviating all the undesirable effects (multimoding-energy trapping) related to the high refractive index of semiconductor materials. In the following, we illustrate these various issues with first of all the effort carried out on the discrete devices. For illustration, Figure 2 is a Scanning Electron Micrograph of a Schottky device in a back-to-back configuration for subharmonic mixing at 500 GHz. In agreement with the aforementioned design rules, we used here a T-gate technology making use of bi-layered PMMA/MMA moulding stage. On the other hand, the active region $(0.1 \times 10 \ \mu m^2)$ was connected to the external pad via an air bridge-type interconnect fabricated in a one stage by e-beam writing. At last a deep etch using isotropic chemical etching was implemented. Such technological stages are representative of the generic technologies involved at Terahertz frequencies. They can be applied to a large variety of devices which involve Schottky and/or ohmic contact-type devices [5].

From the circuit side, surface- and bulk- micromachining techniques are also of great help for alleviating most of the drawback resulting from the frequency increase. Therefore epitaxial lift-off (ELO) followed by transfer techniques on host quartz substrate [6] and moulding techniques fabricating the waveguide in a monolithic fashion have been found suitable for the fabrication of Terahertz devices. On the other hand, it becomes more and more difficult to match the devices with conventional techniques such as sliding backshorts, to couple the electromagnetic energy to devices by using E-plane transitions and to filter the undesirable frequency components while preserving low insertion losses. Several routes exist for overcoming such difficulties. This includes the choice of a distributed approach with transmission lines periodically loaded by non linear elements [7] in association with fin lines and Vivaldi or Ridge-type transitions (Figure 3) and at last Photonic Band Gap filters. This also means that a global synthesis of the circuit have to be implemented based on electromagnetic and electrical codes [8].

4. Conclusion

Terahertz Technology is at the front-edge of research with exciting challenges in terms of theoretical and fabrication issues. Analysis codes based on probabilistic approaches (Monte Carlo and quantum transport) are now available for assessing the device capability. Advanced fabrication techniques permit us to now face most of the difficulties which result from a Terahertz operation. Also, it is believed that more prospective routes such as Photonic Band gap and fin lines can be explored.

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Fig. 1: Quantum well varactors   Fig. 2 SEM of Schottky's (500 GHz)   Fig. 3 NLTL approach with HBV's

$Al_{0.7}Ga_{0.3}As/GaAs$ HBV for 255 GHz Tripling Operation

M. Saglam[1], M. Bozzi[2], C. Domoto[3], M. Rodriguez-Girones[1], L. Perregrini[2], H. L. Hartnagel[1]

[1] *Technical University of Darmstadt, Institute of High Frequency Electronics, Germany*
[2] *University of Pavia, Department of Electronics, Italy*
[3] *ATR Adaptive Communications Research Laboratories, Japan*

$Al_{0.7}Ga_{0.3}As/GaAs$ HBV diodes with different mesa diameters have been fabricated and their DC characteristics have been measured. These characteristics are used by a combined genetic algorithm/harmonic balance simulator to calculate the optimum impedance and output power at 255 *GHz*. A comparison of the conversion efficiencies is presented for the different structures.

Introduction

The heterostructure-barrier varactor (HBV) diode is an ideal device for direct tripling since the C–V characteristic is evenly symmetric and the I–V characteristic is anti–symmetric, so that only odd harmonics are generated at the output. These varactor devices require less design complexity compared to Schottky diode triplers since no DC bias circuitry and no idler circuit at the second harmonic are required [1,2].

Fabrication of AlGaAs HBVs

The $Al_{0.7}Ga_{0.3}As/GaAs$ HBV structure is grown with Molecular-Beam Epitaxy and fabricated using standard photolithography techniques for isolation and ohmic contact patterning, and wet chemical etching of mesa isolation. The Ni/AuGe/Ni ohmic contact is evaporated and annealed for 1 min at 480°C. The HBVs with diameters of 10, 20 and 40 μm are fabricated in the form of two columns with a total of four barriers, as shown in Fig. 1. The measured I–V characteristics of the HBVs are also presented in Fig. 2.

Analysis of HBV Tripling Performance

A novel circuit simulator, based on the combination of the genetic algorithm and the harmonic balance technique [3], has been used for the characterization of the tripling performance of the HBVs. The analysis permitted one to determine the maximum tripling efficiency along with the optimal embedding impedance.

It is observed that the smallest HBV (with a diameter of 10 *μm*) exhibits the best conversion efficiency (more than 4%) in the considered range of pump power (up to 30 *mW*). Conversely, the other devices (with diameters of 20 and 40 *μm*) present a lower series resistance R_S but very poor conversion efficiencies in the power range up to 30 *mW*. Fig. 3 reports the maximum tripling efficiency and the output power at 255 *GHz* of the HBVs with 10 and 20 μm diameters, versus the available pump power level at the fundamental frequency (85 *GHz*). The device with diameter of 40 μm, not reported here, presents an extremely low conversion efficiency in the considered power range.

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Fig. 1: SEM picture of the two-column four-barrier AlGaAs/GaAs HBVs fabricated at TU Darmstadt.

Fig. 2: Measured I–V characteristics of the AlGaAs/GaAs HBVs.

Fig. 3: Maximum conversion efficiency and output power at 255 *GHz* of two HBVs with different diameters versus the pump power level at the fundamental frequency (85 *GHz*).

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Session XII: THz Sources, Diodes, and Receivers

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Session XIII

Nanoelectronics

Chair:
Prof. Arvydas Matulionis
Semiconductor Physics Institute, Vilnius, Lithuania

Prospects and Key Issues of Compound Semiconductor Nanoelectronics

Hideki Hasegawa

Research Center for Interface Quantum Electronics (RCIQE) and
Graduate School of Electronics and Information Engineering, Hokkaido University,
Kita-13, Nishi-8, Sapporo 060-8628, Japan, E-mail:hasegawa@rciqe.hokudai.ac.jp

Prospects and key issues of the compound semiconductor nanoelectronics are discussed, introducing the results recently obtained at RCIQE.

Introduction

Recent rapid progress of the nanofabrication technology has opened up exciting possibilities of constructing novel quantum devices based on artificial quantum structures such as quantum wells, wires and dots. Although extensive efforts are being made in Si nanoelectronics, III-V semiconductors posses attractive features such as availabilities of highly controllable epitaxy techniques, superb heterointerfaces, superb electron transport and large quantum effects, that are not shared with Si.

The purpose of this paper is to discuss the prospects and key issues of the compound semiconductor nanoelectronics by introducing the results recently obtained by the author's group at Research Center for Interface Quantum Electronics (RCIQE), Hokkaido University.

Quantum nanostructure formation

Standard approaches for nanostructure formation include; (1) Si nanostructures by use of EB lithography, dry etching, oxidation on silicon or silicon-on-insulator(SOI) wafers, (2) nanostructures on III-V multi-layer hetero-epitaxial wafers by EB lithography and etching, (3) selective depletion of 2DEG in III-V hetero-epitaxial wafers by split gates, (4) III-V nanostructures by selective growth on patterned substrates, (5) III-V nanostructures by area-selective growth using insulator masks and (6) nanostructures by scanned probe-induced atom-manipulation or surface reaction.

At RCIQE, MBE-based nanostructure arrays are formed on GaAs and InP by using the above approaches (2) and (4)[1]. The former utilizes EB lithography and wet chemical etching on AlGaAs/GaAs 2DEG wafers and gives the minimum feature sizes of 70-100nm. The latter utilizes selective MBE growth of InAlAs/InGaAs/InAlAs heterostructures on InP and realizes completely embedded nanostructures with the minimum feature sizes of 10-30 nm or below. With the latter, arrays of wires, dots, wire-dot coupled structures and honeycomb wire networks have been successfully formed. This approach realizes sizes smaller than the lithography sizes which are independent of lithography size and its fluctuation. The position and size of the nanostructure can be precisely controlled. Interfaces are defect-free high quality heterointerfaces with steep and high potential barriers.

Quantum Devices

Although III-V quantum devices are candidates of building blocks of next-generation high-speed, low-power and high density ULSIs, previous devices fabricated using the split-gate geometry operated only below a few K due to weak electron confinement. The more recent vertical structure with side gates gives stronger confinements, but the structure is not suitable for high-density planar integration.

At RCIQE, quantum wire transistors (QWTrs) and single electron transistors (SETs) are fabricated by forming novel Schottky in-plane gate (IPG) and wrap gate (WPG) structures on GaAs-based and InP based nanowires. Both gate structures can realize much stronger lateral confinement than split gates and are suited for high density planar integration. QWTrs show excellent gate control

characteristics both at RT and low temperatures. The first quantized conductance step was visible up to 100K. By switching between conductance steps with gate charging by a few electrons, switching near quantum limit can be realized[2]. Recently, a novel memory device using Schottky metal dots and IPG QWTr has been successfully demonstrated.

By forming short and multiple IPGs, single- and multi-dot SETs operating up to 30-40 K can be formed. Low voltage gain below unity has been a problem for SETs for logic applications. Three WPG gate GaAs SETs showed voltage gains larger than unity due to FET-like tight control. Using the WPG technology, an logic inverter circuit consisting of a SET driver and a QWTr active load was successfully fabricated, and showed inverter action with transfer gain larger than unity [3]. Complimentary SET logic inverters using two WPG SETs have also been demonstrated.

Key Processing Issues - control of surfaces and interfaces

Even on clean III-V surfaces freshly MBE grown in UHV environments, the so-called Fermi level pinning takes place, and it is difficult to remove it by subsequent processing steps. Control of Fermi level pinning is a key issue for nano-devices. At RCIQE, attempts are being made to remove Fermi level pinning at metal-semiconductor nano interface by electrochemical process[4], and to remove Fermi level pinning on free surfaces with the use of silicon interface control layer[5].

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Fabrication of Nano-Structure for Room Temperature Single Electron Devices

Kazuhiko Matsumoto

Electrotechnical Laboratory MITI, Japan

Abstract

The single wall carbon nanotube atomic force microscopy (AFM) tip was introduced into the AFM nano-oxidation process, which oxidized the titanium (Ti) metal film on the atomically flat α-Al2O3 substrate and formed the ultra narrow oxidized titanium (TiOx) line of 5nm width. The single wall carbon nanotube was grown directly onto the Si AFM tip. This TiOx lines was used as the tunnel junctions of the single electron transistor (SET), and the SET fabricated by this process showed the room temperature Coulomb oscillation with the periods of 1V. This technique is also applicable to the silicon and compound semiconductors.

Carbon Nanotube AFM Cantilever

For the fabrication and observation of the nanostructure, the small apex of the AFM cantilever is indispensable. The apex of the conventional Si cantilever is as large as 20~30nm. Using this conventional cantilever, the size of the fabricated structure is as large as more than 20nm. In order to get the smaller nanostructure less than 10nm, the single wall carbon nanotube is introduced in the AFM cantilever. The growth method of the single wall carbon nanotube to the Si cantilever is as follows: After the chemical catalyst was coated on to top of the conventional Si cantilever, the cantilever was set in the furnace and hydro-carbonate gas was flowed at high temperature. The single wall carbon nanotube then started to grow from the catalyst as an origin, and followed up the wall of the silicon tip to the top, and then protruded from the silicon tip. Figure 1(a) is the TEM image of the single wall carbon nanotube AFM tip, and Fig. 1(b) the schematic structure of the cantilever. The size of the single wall carbon nanotube is as small as 1~2nm, and is more than ten times smaller than the conventional Si tip.

AFM Nanooxidation Process for Single Electron Transistor

Using this single wall carbon nanotube AFM cantilever, the nanostructure was fabricated for the SET.

Fig. 1, (a) TEM image of single wall carbon nanotube grown on to Si cantilever by CVD.

Fig. 1, (b) Schematic figure of single wall carbon nanotube grown on to Si AFM cantilever.

Figure 2 shows the schematics drawing of the fabrication process. The single wall carbon nanotube AFM cantilever was used as an ultra small electrode with the bias applied between the cantilever and the 2.5nm thick titanium (Ti) thin film on the atomically flat α-alumina (α-Al2O3) substrate, and the surface of the Ti metal was anodized to form the oxidized titanium line (TiOx) which works as a tunnel junction for the single-electron devices. Figure 3 shows the cross section of the two TiOx lines. The line width is as narrow as 5nm for both lines, and the height is 1nm.

Figure 4 shows the schematic structure of the single electron transistor formed by the AFM nano-oxidation process. The transistor has two tunnel junctions made by TiOx lines between the source and drain electrode, and the island region between them. These two TiOx tunnel junctions were made by the carbon nanotube AFM cantilever. The gate electrode are set near the island region. Figure 5 shows the gate bias dependence of the drain current of the SET at room temperature. The drain bias is set at 0.3V and 0.25V. The drain current clearly shows the Coulomb oscillation characteristics even at room temperature with the period of ~2V because of the small size of the device.

Fig. 2, Schematic diagram of pulse-mode
AFM nano-oxidation process on atomically
flat Ti/Al2O3 substrate.

Fig. 3, Cross section of oxidized titanium (TiOx) line.
Line width is as narrow as 5nm, and height 1nm.

Fig. 4, Schematic structure of single electron
transistor made by the AFM nano-oxidation process.

Fig. 5, Coulomb oscillation characteristics of the SET
at room temperature by AFM nano-oxidation process.

Resonant-Tunnelling 3-Terminal Devices for High-Speed Logic Application

W.Prost, P.Velling, G.Janssen[1], U.Auer, A.Brennemann, P.Glösekötter[2], K.F.Goser[2],
F.-J. Tegude

*Solid-State Electronics Department, Gerhard-Mercator-Universität Duisburg, Lotharstr. 55, D-47048
Duisburg, Germany, prost@hlt.uni-duisburg.de, [1]Technical University Eindhoven, Electronic Devices
Group, The Netherlands, [2]University of Dortmund, Department of Electronic Devices, Germany*

Abstract: Resonant tunnelling diodes (RTD) are well suited for future nano-scale integrated circuits. Their negative differential resistance (NDR) can be exploited to reduce the logic depth and the number of devices for high-speed digital circuit components. Recently, the MOBILE concept has been proposed as a basic logic module. The MOBILE is a monostable-bistable transition logic element which combines a dynamic latch with 3-terminal (HFET) input branches [1]. Its function is based on a current balance between parallel 3-terminal input devices and the series connected RTD latch.

The MOBILE concept has been improved by using a series connection of HFETs and RTDs as the input branches such that the HFET acts as a switch and the RTD as a current limiter. This way the current balance depends on the RTD area ratio, only, and homogeneity variations in terms of lithography, etching or epitaxial growth are substantially ruled out [2]. The homogeneity and reproducibility of a standard RTD-fabrication process using the MBE-method has been checked experimentally. Obviously, the impact of layer data was overestimated in the past, especially if the device dimensions are shrinking according to low-power digital circuit applications. Using our technology, the maximum (worst case) tolerable peak current fluctuation Δ in dependence on the number n of input stages is $\Delta = 1/(4n-2)$ showing that more than seven inputs of one gate (NAND, NOR,...) is allowable which is much more than needed for most applications. The functionality of a programmable NAND/NOR-Gate based on the improved MOBILE concept working at ultra-low voltages $V_{DD} = 0.8$ V and with high noise margin $V_{H/L} = 0.7/0.1$ V, high fan-out and short gate-delay time will been demonstrated.

The traditional MOBILE concept is very difficult to realise with bipolar transistor input terminals due to its exponential transfer characteristic ($I_C = f(V_{BE})$), and a couple of other digital circuit concepts are under discussion in combination with HBTs [3]. However, all concepts demand a very precise control of current-voltage data of two independent devices.

We will report on the applicability of the novel MOBILE to HBT/RTD digital circuits on s.i. InP substrate. A HBT with a RTD emitter (RTBT) was realised in a combined MOVPE/MBE growth process and with a wet chemical process technology. The RTBT reaches small signal transit frequencies up to $f_T = 40$ GHz. The experimental device characteristics (Fig. 1a) are implemented in commercial circuit simulation software HP-MDS and are modelled as series combination of an HBT and a RTD. The modelled RTBT characteristics fits precisely to the experimental data (Fig. 1b).

Novel NAND/NOR Boolean logic Gates are designed based on the RTBT device and the MOBILE concept (Fig. 2). At high input levels the RTBT characteristics are RTD-type. Hence, the peak-to-valley current ratio of the parallel combination of the driver RTD and the input stages device is retained. Hence, the driving capability of the circuit is increased compared to conventional 3-terminal input branches. In Fig. 3 the timing diagram obtained by H-SPICE simulations based on the experimental data are given. The functionality of the NAND gate is proven indicating possible multi Gb/s operation with robust logic levels.

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Fig. 1: *Measured (a) and modelled (b) common emitter output characteristics of the RTBT (12μm²) on s.i. InP substrate at room temperature.*

Fig.2: *NAND-gate based on RTBT devices and a series connected RTD latch: a) gate design with active clock V_{EE} and RTBT inputs. Both, the RTBT and RTD device current is proportional to the device area which is normalised to A = 1. b) schematic description of the gate function with different driver lines. A low output "0" is achieved if both inputs are open. Under this condition the total peak driver current (driver+a+b: A=3) is larger than the peak load current (A = 2.5).*

Fig. 3: *H-SPICE modelled timing diagram of the NAND latch gate of Fig. 2:*
(V_{ee}:= 0 V / -2.8V; $V_{a,b}$:= -0.9 V/ -1.9 V; V_{out} high-level: -0.3V up to 0.05V, low-level: -1.9V; RTD I_p=4 mA; V_p=0.7V; PVCR = 7; HBT: β = 99.6, R_b=3.2 Ω, R_e=5.1 Ω, R_c=3 Ω, n_C =1.3, n_E=1.8).

NOTES
Session XIII: Nanoelectronics

NOTES
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Session XIV

Lasers, LEDs, Detectors, and Photonic Bandgap Approaches

Chair:
Dr. Daniel Hofstetter
Université de Neuchâtel, Neuchâtel, Switzerland

VISIBLE LASERS: InGaP and GaInN

M. H. Pilkuhn

Physics Institute
Stuttgart University
Germany

The development of visible lasers benifited from the improvement of materials technology leading to single mode DFB lasers, surface emitting lasers, and even high power lasers. Laser pointers are the biggest application at present, but future development aimes at DVD-lasers.

Vapor Phase Epitaxy with Metal-Organic Compounds (MOVPE) has become the prevailing technology for the production of thin films of III/V semiconductors, particularly for applications in optoelectronics.

The high degree of control and reproducibility has recently led to new developments in the case of phosphides and nitrides for visible LEDs and lasers.

InGaP and AlInGaP films on GaAs substrates are the basis for red to yellow emitting devices,and their MOVPE technology will be discussed in detail.

The quarternary alloys AlGaInP belong presently to the most important optoelectronic materials for lasers and LEDs in the visible (yellow/red) range. They can be grown by MOVPE with very high quality in 2 forms: A "disordered" phase where the group III elements are distributed randomly on their zinkblend lattice sites. An "ordered" phase where the group III elements form a "natural superlattice" leading to changes in the optical properties and electronic band structure. Recent results on superbright multicolour light emitting diodes and on low threshold lasers will be reported. In particular, the "T_0-problem" i.e. the temperature dependence of the threshold current density, is an important issue. Distributed feedback lasers with first order grating exhibit single mode emission at wavelengths down to 630nm.

Moderate lattice mismatch leads to compressive or tensile strain, and the influence on the properties of quantum films will be discussed. At strong lattice mismatch, the Stranski-Kastranov growth takes place with island formation. Recently, quantum islands with interesting optical properties could be obtained using thin InP films (several monolayers) on InGaP substrates. With multiple films the first quantum island laser emitting in red spectral range could be produced.

For visible lasers in the blue and violet spectral range, the nitride system, GaInN and AlGaN has received very much attention recently.

MOVPE on either sapphire or SiC substrates has established itself as the most successful technology, and the materials problems related to GaInN quantum well structures will be discussed. Distributed feedback lasers for these short wavelengths imply extremely short grating periods. They can be attained, e.g. by e-beam lithography, and first results for single mode index coupled DFB lasers are presented.

Blocklayers for AlGaInP-Lasers Emitting at 670 nm

Wolfgang Wagner, Rainer Butendeich, Markus Ost, Ferdinand Scholz and Heinz Schweizer

Abstract— For semiconductor lasers emitting at 670 nm the most commonly used cladding material is $(Al_{0.66}Ga_{0.34})_{0.5}In_{0.5}P$ because of its large direct bandgap. An alternative is AlInP with an indirect bandgap of approximately $E_g^X = 2.35$ eV [1], [2]. Due to the higher bandgap we expect a higher barrier for electron leakage and therefore a better temperature stability. Because of the low refractive index of AlInP the cladding has to be modified in respect to waveguiding properties in order to avoid a large diffraction angle $\theta_\perp$ of the emerging laser beam.

Keywords— AlGaInP, Blocklayers, Leakage Current.

I. INTRODUCTION

FOR semiconductor lasers emitting at 670 nm the most commonly used combination of waveguide and cladding material are $(Al_{0.33}Ga_{0.64})_{0.5}In_{0.5}P$ for the waveguide and $(Al_{0.66}Ga_{0.34})_{0.5}In_{0.5}P$ for the cladding. The latter is used because of its large direct bandgap. The barrier for electron leakage is approximately 225 meV [3] (for $\lambda = 680$ nm), the direct bandgap $E_b^\Gamma = 2.28$ eV [1], [2].

An alternative for the cladding material is AlInP, with an indirect bandgap of approximately $E_g^X = 2.35$ eV. This modification should result in a reduction of electron current leakage. Due to the lower refractive index of AlInP the waveguiding properties will be changed, i.e. a larger confinement factor Γ but also a larger diffraction angle.

II. THEORY

In order to use the advantage of the larger bandgap of AlInP, the waveguide is confined by AlInP cladding layers instead of $(Al_{0.66}Ga_{0.34})_{0.5}In_{0.5}P$ cladding layers. Due to the high refractive index step

Fig. 1. Schematic diagram of the modified epitaxially grown layers. The dashed line represents the ground mode.

W. Wagner is with the 4. Institute of Physics, University of Stuttgart, Germany. E-mail w.wagner@physik.uni-stuttgart.de

between waveguide material and cladding material, the optical mode is quite well confined for waveguide widths of 2 × 80 nm up to 2 × 420 nm. This leads to a large diffraction angle $\theta_\perp$ of the emerging laser beam. In order to reduce this effect only a part of the cladding material is substituted by AlInP, see figure 1. The minimum thickness of the AlInP layer is 25 nm in order to suppress any tunneling of thermally activated electrons through that barrier.

The waveguiding properties are optimized by calculating the confinement factor Γ, the diffraction angle $\theta_\perp$ and the penetration depth of the mode into the highly doped cladding regions. The calculations are based on calculating the optical modes by the 'Transverse Resonance Methode'.

Fig. 2. Calculated properties of the modified structure with a fixed blocklayer width of 2 × 120 nm. The triangles are indicating the 'standard structure'.

Figure 2 shows the results of the calculations for a fixed blocklayer width of 120 nm. For comparison the triangles show the results of a single quantum well 'standard structure' with a waveguide of 2 × 80 nm and $(Al_{0.66}Ga_{0.34})_{0.5}In_{0.5}P$ cladding layers. This structure was optimised for low threshold current [4]. All the above mentioned properties improve for the modified structure with a waveguide width of 2 × 110 nm up to 2 × 130 nm.

Figure 3 shows the calculation for a fixed waveguide width of 2 × 120 nm. In every respect, the combination of that waveguide width and blocklayers with a width of 75 nm up to 125 nm show better results than the 'standard structure'.

III. EXPERIMENTAL

The device structure is shown schematically in Fig. 1. The material is grown by organometallic vapor phase epitaxy [4], [5], [6] on misorientated GaAs substrates [7]. The active region is a single 6 nm

Fig. 3. Calculated properties of the modified structure with a fixed waveguide width of 120 nm. There is an improvement in every respect compared to the 'standard structure'.

$Ga_{0.41}In_{0.59}P$ quantum-well. The quantum-well is centered in an $(Al_{0.33}Ga_{0.67})_{0.5}In_{0.5}P$ confining region of 2×120 nm width. The cladding layer consisted of Al-InP blocklayers with a width of 120 nm and 900 nm $(Al_{0.66}Ga_{0.34})_{0.5}In_{0.5}P$. The thicknesses of the epitaxial layers were controlled by SIMS (not shown here).

In order to determine the intrinsic losses α_i and the internal quantum efficiency η_i, broad area oxide confined lasers of width $16\,\mu m$ and different length were fabricated and tested under pulsed conditions (0.1 % DC). The measured differential quantum efficiency η_d versus length gave the following results: $\alpha_i \approx 8.7\,cm^{-1}$ and $\eta_i \approx 81\,\%$. While α_i is slightly higher, the latter value is similar to the result obtained from the 'standard structure'.

Fig. 4. Measured threshold current density and differential quantum efficiency for a $16 \times 906\,\mu m^2$ laser device. These data are used to determine the electron barrier hight.

Figure 4 shows the result for the characteristic temperature T_0 where we have assumed the standard exponential temperature dependence of $J_{th}(T)$. In the range of $-10^{\circ}C$ up to $+35^{\circ}C$ we obtain a value of $T_0 \approx 173\,K$, which is approximately a factor of 1.6 higher than for the 'standard structure' $(T_0 \approx 110\,K)$.

In order to determine the barrier height for electron leakage we follow the procedure described in [3]. The result is shown in figure 5. As expected, the barrier height of the novel structure ($\approx 256\,meV$) is higher than for the 'standard structure' which is about

225 meV. This is attributed to the higher bandgap of AlInP.

Fig. 5. Arrhenius plot used to determine the electron hetero-barrier height.

The measured diffraction angle $\theta_\perp$ was about $31^{\circ} \pm 0.5^{\circ}$, i.e. in good agreement with the expected calculated value, see figure 3. The error of calculation is in the same order of magnitude and mainly based on uncertainties of material data like refractive indices.

IV. SUMMARY

We showed that for AlGaInP/GaInP-lasers the partial substitution of the $(Al_{0.66}Ga_{0.34})_{0.5}In_{0.5}P$ cladding layer by AlInP results in an increase of the barrier height of electron leakage, hence in a higher characteristic temperature T_0. A careful design of the blocklayer is neccesary in order to get a small diffraction angle $\theta_\perp$.

ACKNOWLEDGMENTS

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HETEROBARRIER LEAKAGE IN InGaAsP BASED LASER DIODES

H. C. Neitzert[1] and S.Massetti[2]

Centro Studi e Laboratori Telecomunicazioni, Torino, Italy
present address: [1]Università di Salerno, Fisciano, Italy, [2] Alenia Spazio, Torino, Italy

Monitoring the optical emission at a wavelength of 950nm which is due to recombination within the confining InP layers has been demonstrated to be a helpful technique for the evaluation of InP/InGaAsP type laser diodes [1,2]. Here we apply this technique to the characterization of current leakage in 1570nm InGaAsP MQW laser diodes with semiisolating InP:Fe lateral current blocking layers.

The investigated lasers were Fabry-Perot type InGaAsP MQW lasers grown by MOCVD on n-type InP substrates with top p-contact and lateral confinement by a semiisolating InP:Fe layer. We performed electroluminescence mapping of the investigated laser diodes using a cooled silicon CCD camera and achieved wavelength selectivity by by the use of interferencial optical filters with 70nm wide bandpass characteristics. There was no need for a blocking filter of the fundamental emission, because of the use of a silicon detector, not sensible around 1550nm. In Fig.1, where the integral and the maximum light emission as a function of the center wavelength of the bandpass filters are shown, two peaks are observed: A 950nm peak due to recombination in the confining InP layers and a second peak around 750nm due to second harmonic generation (SHG) within the laser cavity [3]. In the following we used a combination of two bandpass filters to suppress efficiently the SHG emission when monitoring the 950nm emission and viceversa. Measuring the laser current dependence of the integral of the 950nm emission with a calibrated power meter (Fig.2), we find two kinks in the characteristics (indicated by the arrows). At the first kink - coincident with the laser threshold - the dependence of the 950nm integrated emission on the laser current changes from a power law dependence below laser threshold to an exponential increase of the 950nm emission intensity above threshold. For laser currents exceeding 38mA, a further enhanced 950nm emission can be observed. Calculations show that there is a direct correlation above threshold between the intensity of the 950nm emission and the "missing" current compared to an ideal P-I characteristics obtained by linear extrapolation of the slope just above threshold. Similar findings have already been reported on 1300nm lasers [4,5]. A typical image of the 950nm emission above threshold is shown in Fig.3, where the laser top layer is located at the left hand side. In the center two distinct emission peaks can be seen. The more intense peak on the left is due to electron leakage from the active InGaAsP MQW region into the upper InP cap-layer and the small peak is due to hole leakage into the lower n+ InP epilayer. Additionally we see widely extending emission regions due to lateral leakage. If we use 750nm bandpass filters we observe a single emission peak situated in between the formerly observed 950nm emission maxima. The intensity of this peak - that allows us to identify the position of the active lasing region - increases quadratically with the fundamental optical power and this holds for various temperatures (Fig.4). By calculating the integral intensity in different regions of the 950nm emission image (Fig.5), we find that for the investigated laser the heterobarrier electron leakage is dominant around threshold. For bias current values exceeding twice the threshold current, in coincidence with a decreasing differential efficiency (see Fig.2), lateral leakage becomes more important. After stressing the laser for 25h at 100mA at 60°C, a 50% increase of the threshold current and a large increase of the reverse bias current has been found. The increase of the 950nm emission in the high bias current regime (Fig.4) indicates an increase of the lateral leakage current as the main degradation mechanism.

In conclusion, wavelength selective electroluminescence imaging with a cooled silicon CCD allowed us to identify various problems related to leakage currents in InGaAsP based MQW laser diodes. We could clearly reveal recombination losses due to electron leakage into the upper p-type InP cladding and and hole leakage into the bottom n-type InP cladding. For laser currents well above the threshold lateral current losses are dominating.

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Fig.1 Integral and maximum values of the light intensities detected by the CCD camera with insertion of optical bandpass filters with different center frequencies, biasing the laser with 60mA at 20°C

Fig.2 Optical emitted power at 1570nm and 950nm as a function of the laser diode current

Fig.3 a) Image of the 950nm light emission at 20°C and linescan (along the white line on the left) for a laser diode current of 60mA

Fig.4 Second harmonic emission as a function of the fundamental optical power measured at different temperatures

Fig.5 950nm light emission intensity as a function of the bias current in different areas of the laser, corresponding to InP recombination due to the indicated leakage mechanisms

Fig.6 950nm light emission as a function of the laser current before and after high current stress at an elevated temperature

The Reliability of AlGaInP Visible Light Emitting Diodes

D V Morgan & I Al-Ofi
School of Engineering, Cardiff University
PO Box 925, Cardiff CF24 OYF, UK

ABSTRACT

High brightness visible LEDs have attracted considerable interest for applications that include automobile indicators, traffic lights and outdoor display systems. In this paper we report on a preliminary study of the reliability of AlGaInP devices stressed under elevated temperatures up to 125°C and at operating current levels. Devices of two basic kinds have been studied (figure 1), those with an ITO spreading layer and those without. The degradation has been recorded by observing the light output as a function of time. In parallel with these measurements the changes in device terminal (current voltage) performance was also noted.

The early studies[1] concentrated on the basic device structure as shown in figure 1, but without the inclusion of the ITO spreading layer. The present paper concentrates on devices which do include ITO. Figure 4 shows the current voltage characteristics stressed at 100 mA and 125°C with (c) and without (b) ITO. From this data the major changes occur in the low voltage region of the characteristic. These occur at current and voltage value well below those for operation as an LED and are associated with diode bypass leakage. In the operational region above the emitting threshold very little charge is observed. It should be noted that the introduction of ITO greatly reduces the diode leakage.

The introduction of an ITO spreading layer did not introduce any new degradation mechanism over those recorded for the basic device structure [1]. The degradation curve exhibits two basic regimes. During the period 0-300 hours there is a rapid and erratic degradation, followed by a slower exponential like degradation process (figure 2). From the data obtained for a range of temperatures the two regions are characterised by different activation energies Ea (i.e. Ea = 0.45eV and 0.8eV respectively - figure 3).

It is proposed that the early and erratic degradation corresponds to interdiffusion between the metal contact and the semiconductor surface. This has a relatively low activation energy of around 0.45 eV. Over a longer period of time degradation occurs through the diffusion of non radiative defects into the active region of the DH structure. Associated with this process is the activation energy of 0.8 eV.

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**Figure 1
Schematic diagram of LED structure**

With ITO

Without ITO

**Figure 2
Current voltage characteristic for LED (figure 1) stressed at 100mA and 125°C with and without ITO**

Figure 3
Normalised Light Output versus Time for LED showing the two distinct regions of degradation

Figure 4
Degradation coefficient β versus (l/T) for the two regions discussed in figure 3

Pb-La-Zr-Ti-O/Sr-Ti-O Multilayered Structures on GaAs Substrates for Tunable Photonic-bandgap Applications

D. Young and A. Christou

Materials Science and Engineering and Materials Research and Engineering Center
University of Maryland
College Park, MD 20742

ABSTRACT

Double-layer perovskite $Pb_{0.91}La_{0.09}Zr_{0.65}Ti_{0.35}O_3/SrTiO_3$ heterostructures have been grown by pulsed laser deposition (PLD) onto (001) MgO/GaAs substrates. The perovskite layers are single phase with 35nm RMS roughness on the top surface. Electrically induced birefringence in the PLZT layers, applied through surface interdigitated electrodes, resulted in both optical phase and optical amplitude modulation. The application of a purely sinusoidal electric field across the PLZT layers resulted in optical modulation at both the primary and first harmonic frequencies, and direct evidence of the non-linear electro-optic effect. We demonstrate the feasibility of multilayer, electro-optic, perovskite heterostructures which could act as electrically and optically tunable photonic bandgap devices.

INTRODUCTION

The family of Pb-La-Zr-Ti-O (PLZT) perovskite oxide ceramics has been the focus of considerable research efforts due to their many unique properties [1,2,3] including ferroelectric and electro-optic effects. While other perovskite oxide materials have recently supplanted PLZT as the material-of-choice for many ferroelectric, piezoelectric and electrostrictive applications [4,5] PLZT ceramics continue to receive attention as a promising electro-optic oxide material [6,7]. The large quadratic electro-optic coefficient, high optical transparency and extensive knowledge of basic material properties along with an established processing technology for PLZT continue to make it an attractive electro-optic material [8,9,10]. Electro-optical devices have been successfully fabricated from bulk PLZT [11, 12]. Thin film PLZT structures are even more attractive for many electro-optic applications, due to the potential waveguide and interference devices that may only be realized in a thin film configuration [13,14].

Recent advances in pulsed laser deposition (PLD) and molecular beam epitaxy, and the application of in-situ monitoring techniques to oxide film growth, has advanced the understanding of oxide epitaxy [19, 20, 21, 22]. These developments promise to improve the quality and complexity of available thin film oxide heterostructures of devices. Considering the expected improvements in the epitaxial perovskite growth [29, 30] and acted as a chemical diffusion barrier between semiconductor and perovskite oxide materials. PLZT/BST/PLZT structures were also grown with $La_{0.5}Sr_{0.5}CoO$ (50/50 LSCO) layers between the MgO and first PLZT layer, in order to demonstrate integration with an oxide eletrode material.

OXIDE GROWTH AND PHYSICAL CHARACTERIZATION

The present investigation successfully demonstrates the use of multilayer perovskite oxide structures for optical modulation. Standard pulsed laser ablation techniques [28] were used to grow two discrete layers of (9/65/35) PLZT, sandwiched between $SrTiO_3$ (STO) or $BaSrTiO_3$ (BST) layers. These structures were grown on GaAs substrates using an MgO buffer layer, that capped the GaAs to prevent As loss during higher temperature growths. The MgO also provided a suitable surface for subsequent without the LSCO layer, polycrystalline perovskite grew on the (001) MgO and all subsequent perovskite layers were also polycrystalline. Typical layer thicknesses were 50nm for MgO and 100nm for LSCO, STO, BST and PLZT. The STO and PLZT stochiometries were further confirmed by Rutherford Backscattering spectroscopy. Transmission electron microscopy studies indicates the presence of an abrupt interface with very little interdiffusion occurring during

growth. Optical characterization shows the ability to modulate both amplitude and phase, with amplitude modulation resulting in a contrast of over 20dBm.

CONCLUSIONS

In conclusion, the present investigation demonstrates the fabrication of multilayer (9/65/35) PLZT thin film device structures on GaAs substrates with an MgO buffer layer. Both electro-optical amplitude and phase modulation have been demonstrated. Significant modulation harmonic content was detected, which is explained by the nonlinear optical effects in the PLZT layers and the GaAs substrate. The addition of PLZT layers increased amplitude modulation, but not phase modulation. Phase modulation may be increased by optimizing layer thickness, by increasing the number of layers and by increasing the index of refraction difference between adjacent layers. The present investigation shows the possibility of attaining a wide variety of novel photonic devices on GaAs substrates.

Quantum-dot infrared detector: high sensitivity due to barrier-limited photoelectron capture

V. Mitin[*1], V. Pipa[1], A. Sergeev[1], M. Dutta[2] and M. Stroscio[2]

[1]*Department of ECE, Wayne State University, Detroit, MI 48202*
[2]*U.S. ARO, P.O.Box 12211, Research Triangle Park, NC 27709*

Department of ECE, Wayne State University, Detroit, MI 48202, US
Tel. + 1-313-577-8944, Fax: +1-313-577-1101, [*]Email: mitin@ece6.eng.wayne.edu

We present results of modeling of quantum-dot infrared photodetector with high sensitivity and raised operating temperature. Our innovative idea is to create potential barriers surrounding quantum dots by optimized interdot doping. In this design, the localized ground state and continuum conducting state of the electron turn out to be spatially separated by potential barriers. Due to small probability of indirect (in real space) transitions, the photoelectron capture time and photoconductive gain significantly increase. The large gain results in high responsivity, which in turn will improve the detectivity and raise the device operating temperature to room temperatures.

A wide range of novel properties, unattainable in bulk materials, is now being realized through manipulation of the doping level and length scales associated with quantum-dot structures. One of most promising applications of these structures is a quantum dot infrared photodetector (QDIP). Due to the atom-like localized electronic states, QDIPs ideally have advantages over quantum wells such as sensitivity to the normal incidence radiation, higher photoconductive gain and low dark current. Initial experiments [1] have already shown the advantages of QDIPs over quantum well structures. At the same time, the operating regimes of QDIPs are still very far from optimum. To design a sensitive QDIP with a comparatively high operating temperature, we investigate a structure with QDs surrounded by repulsive potential barriers.

The basic detector parameters such as the gain, the responsivity and detectivity depend significantly on the lifetime of excited electrons [2], which is mainly determined by electron capture into the quantum dots. We suggest a design that allows us to increase the electron capture time and improve basic detector parameters.

The cross-sectional view of the potential relief with electron band structure is shown in Fig. 1. The schematic energy-band diagram with potential barriers in the QD plane is presented in Fig. 2. The barriers are created by electrons bound in the dots and by ionized donors outside the dots. The barriers separate the bound state and excited continuum states of electrons and prevent fast capture of electrons into the dots.

Fig. 1. Potential relief of QD array.

Fig. 2. Energy band diagram in QD plane.

The charge and potential distributions (form of the potential barriers) are obtained by solving the

Poisson and Schrödinger equations self-consistently. Then we calculate the probability of an excited electron to be captured into the quantum dots.

We optimize a set of parameters (size of the dot, interdot distance, and doping level) to reach maximal sensitivity of the detector. The bias voltage also will be optimized: On the one hand, the large voltage is required to decrease the transit time and increase the responsivity. On the other hand, the large electric field facilitates the tunneling of electrons from the virtual states of quantum dots, thus reducing the detectivity.

Due to the barriers, the capture time in the InAs QD structure is shifted from picosecond to nanosecond range. Slow photoelectron capture results in significant improvement of detectivity at compatible temperatures, or alternatively the operating temperature may be raised.

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New type AlGaAs X-ray detector with optical response

K.Pozela, J.Pozela, V.Jasutis, L.Dapkus, A.Silenas

Semiconductor Physics Institute, Gostauto 11, Vilnius 2600, Lithuania

The X-ray imaging detectors based on graded gap $Al_xGa_{1-x}As$ semiconductor structures are designed.

Introduction

The most important problems of ionized particle and X-ray imaging computerized systems are the spatial resolution, leakage current and homogeneity of pixel type detectors. We propose the X-ray imaging detectors based on graded gap $Al_xGa_{1-x}As$ semiconductor structures. The spatial resolution of X-ray image and detection parameters obtained with this detector are higher than in conventional Si and GaAs pixel detectors.

The optical response and image spatial resolution

The experimental set up of the X-ray AlGaAs detector is shown on Fig. 1. The part of electron- hole pairs generated by X-ray in the AlGaAs volume recombine with infrared light radiation. Because of the graded gap structure the wide gap side of the AlGaAs layer is transparent for the photon generated in the volume of crystal (Fig. 2). The x-ray image converts to the light image. The imaging system is monocrystal AlGaAs layer without the array of the pixel detectors. That allows us to obtain the high spatial image resolution (better than 15 lines/mm). Using optical signal transmission the detector can be performed without any electronics in irradiated area.

Fig. 1. X-ray image converted in AlGaAs crystal to optical image is detected by CCD camera.

X-ray - light conversion efficiency

The efficiency of the conversion of X-ray absorbed in an AlGaAs to the emitted light energy is equal to

$$\alpha = \beta \, \eta \, \gamma \, ,$$

where β is the part of X-ray power used to generate the electron-hole pair with energy of emitted photon, η is the part of electron-hole pairs recombined with light radiation, γ is the efficiency of light output from the crystal.

For AlGaAs semiconductor $\beta \approx 0.4$ and is higher comparing with conventional X-ray - light converters (luminophores and scintillators). The value of the $\eta \approx 0.7$ is achieved experimentally.

The light output efficiency from semiconductor plate is

$$\gamma \approx \sin^2 \frac{\Theta}{2} \, ,$$

where Θ is the total internal reflection angle. The parameter γ reduces the X-ray conversion to light efficiency α most strongly. For the transmission from AlGaAs to air the $\gamma \approx 2 \cdot 10^{-2}$. The special geometry and treatment of the surface of detector increases the efficiency γ.

Fig. 2. The graded gap structure and light transmission to the wide energy gap side.

Conclusions

The AlGaAs X-ray detector with optical response and external efficiency $\alpha > 5\%$ is designed.

This type of detectors can be widely used in high energy physics (detectors in particle accelerators etc.), medical instruments (X-ray, β radiation detectors) and environment monitoring (ionizing radiation detectors).

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NOTES
Session XIV: Lasers, LEDs, Detectors, and Photonic Bandgap Approaches

NOTES

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Session XV

Nitride-based Optical Devices

Chair:
Prof. Elias Muñoz
Universita Politécnica de Madrid, Madrid, Spain

Mid-IR emission/absorption from GaN-based heterostructures

Daniel Hofstetter, Jérôme Faist, and David P. Bour[1]

University of Neuchâtel, Institute of Physics, 1 Rue A.-L. Breguet, Neuchâtel, CH 2000, Switzerland
[1] XEROX Palo Alto Research Center, 3333 Coyote Hill Road, Palo Alto, CA 94304, USA

We present results on the mid-infrared emission of violet, blue, and green InGaN light-emitting diodes and the intersubband absorption of AlGaN-based quantum cascade structures. For the light emitting diodes, we found that the diode with the highest In composition in the active region had the shortest mid-infrared emission wavelength and vice versa.

Introduction

In recent years, there has been an increasing interest in mid-infrared (mid-IR) quantum cascade (QC) light sources, especially for applications in environmental sensors. Up to this point, QC lasers fabricated from the InGaAs/InAlAs and the GaAs/AlGaAs material systems have been demonstrated. Nevertheless, there is an ongoing interest for the identification and implementation of new material systems other than the ones mentioned above. The so far shortest QC laser wavelength (3.4 µm) was achieved with strain-compensated InGaAs/InAlAs, which has a conduction band discontinuity of 740 meV. Since there is already a substantial amount of strain in such a structure, further progress towards shorter wavelengths using this technology will be very challenging. For the III-nitrides however, the combination of GaN and AlGaN could offer more than 1 eV conduction band discontinuity which could become very attractive for short wavelength QC lasers. These are reasons enough to investigate the potential of III-nitrides for short wavelength QC light emitters.

Experimental results

The LEDs we investigated have an InGaN-based active region and emit violet (λ = 400 nm), blue (λ = 475 nm) and green (λ = 525 nm) light. For comparison, we studied also the behavior of a red InGaP (λ = 670 nm) LED. The visible emission spectra of these samples have been measured using a Jobin-Yvon grating spectrometer and a silicon photo-detector. The violet, blue and green LEDs were pumped at 80, 160, and 240 mA and the red one at 20, 40, and 60 mA. The emission spectra of all LEDs are reported in figure 1. For the blue/green InGaN-based LEDs, we see a substantial shift towards higher energies when driving the devices at higher injection currents, whereas the violet and the red LEDs exhibit a small wavelength shift towards lower energies. The high-energy shift of the blue and green LEDs is essentially understood as a band-filling effect. If the active region were an ideal QW, then the density of states would be constant and the effect should be much weaker. The red-shift of the luminescence peak in the red and violet LEDs can be explained by an almost complete absence of band-filling and the dominance of bandgap shrinkage. The difference in the spectral width of the red and the violet/blue/green devices is also an indication for the different density of states in the two sorts of active regions. Since the bands of the red InGaP and the

Fig. 1 - Visible emission spectra of the interband electro-luminescence measured on violet, blue, and green InGaN-based, and red InGaP-based LEDs. The injection currents were 80, 160, 240 mA for the InGaN LEDs, and 20, 40, and 60 mA for the red LED.

Fig. 2 - TM and TE-polarized mid-IR emission spectra of violet, blue, and green InGaN-based, and red InGaP-based LEDs. The top figure shows a Planck curve at 300 K and a differential Planck curve for 330 K / 300 K.

violet InGaN LED do not fill quickly, there will be mainly band-edge to band-edge recombination which results in a narrow energy range of the luminescence. On the other hand, the more quantum box-like density of states of the blue/green InGaN LEDs leads to rapid band-filling and thus to a much larger variety of possible transition energies.

For spectral measurements in the mid-IR, the devices were placed into an N_2 flow cryostat. The light from the edge was collected by f/0.8 optics and fed into a high resolution Fourier transform spectrometer, where we detected it using a liquid nitrogen-cooled HgCdTe detector. For these experiments, we used current pulses of 5 µs, and a pulse repetition frequency of 100 kHz. In figure 2, we present the TM and TE-polarized mid-IR edge emission spectra of all four LEDs. The InGaN-based devices showed a decreasing TM:TE polarization ratio with higher In content. While the violet LED exhibited a polarization ratio of about 3.5 : 1, this number dropped to 2.75 : 1 for the blue and to 2.25 : 1 for the green LED. This decreasing TM polarization is an indication for an intersubband emission originating from quantum boxes rather than QWs. In contrast to this, the red InGaP QW LED exhibited a significantly stronger TM polarization, at a ratio of about 10 : 1, as dictated by the polarization selection rule. In order to rule out simple device heating as the cause of the observed mid-IR radiation, we compare in figure 2 the room temperature mid-IR emission spectrum of all LEDs with a Planck spectral distribution at 300 K and a differential Planck curve, which was achieved by subtraction of two Planck curves at 330 K and at 300 K.

Finally, we show in figure 3 an example of an intersubband absorption in an AlGaN-based QC structure. The absorption is centered right at the absorption edge of sapphire (1700 cm^{-1}) which allows us to see only one half of the signal. From the size of the absorption signal, a calculation of the sheet carrier density is possible. The resulting carrier density of $1 \times 10^{17} \text{ cm}^{-3}$ is close to the background doping level in $Al_{0.4}Ga_{0.6}N$ and explains why our luminescence measurements were hampered by an excessively high device resistance of 1 kΩ.

In conclusion, we have presented a comparison between InGaN/GaN-based LEDs with a different In content of the active region. Peak wavelengths of those emissions followed the In-content of the structures. We also

Fig. 3 – TM and TE-polarized absorption spectra in an AlGaN-based QC structure. Please note that the spectral range below 1700 cm^{-1} is, due to sapphire absorption, not accessible.

showed successfully intersubband absorption in AlGaN-based QC structures.

(Al,Ga)N Ultraviolet Photodetectors on sapphire and Si substrates

E. MUÑOZ[1], E. Monroy[1], J.L. Pau[1], F. Calle[1], M. A. Sánchez, E. Calleja[1], F. Omnes[2], B. Beaumont[2], and P. Gibart[2]

[1]*IEL, ETSI Telecomunicación, Univ. Politécnica de Madrid, Ciudad Universitaria, 28040-Madrid, Spain*
[2]*CNRS-CRHEA, Parc Sophia Antipolis, rue Bernard Gregory, 0650 Valbonne, France*
Tel: 34-91-3367321, Fax: 34-91-3367323,
e-mail: elias@die.upm.es

ABSTRACT

AlGaN-based photoconductive, Schottky, MSM, and p-n photodetectors have been fabricated. AlGaN layers were grown by MOVPE on sapphire substrates, and by GS-MBE on Si (111) substrates. Detection cutoff wavelength shifts with Al content from 362 nm (x = 0) to 295 nm (x = 0.35). A visible rejection of more than 10^3 is always obtained. Photodiode time response is usually limited by its intrinsic RC product. Noise studies in the various photodetector structures will also be presented.

INTRODUCTION

UV detectors have a very broad range of applications, from flame detection to scientific instrumentation, astrophysics, environmental, biological and medical studies. The Sun is the major UV source, and the so called solar blind detectors refer to the detection of wavelengths shorter than 280nm. Visible-blind devices are usually related to stratospheric ozone layer research (ozone and solar UV monitoring).

AlGaN alloys are excellent candidates for the detection of the UV radiation. They are direct gap semiconductors, and a proper choice of the Al mole fraction allows the fabrication of photodetectors with threshold energies from 3.4 eV (GaN) up to 6.2 eV (AlN). Hence, solar blind and visible blind devices are feasible.

EXPERIMENTAL AND RESULTS

To fabricate wurtzite AlGaN epitaxial layers for solar UV detectors, two approaches have been followed. On one hand, AlGaN alloys were grown on sapphire substrates by low-pressure metalorganic vapour phase epitaxy (LP-MOVPE) at CRHEA-CNRS. On the other hand, AlGaN alloys were grown on Si(111) substrates by gas-source molecular beam epitaxy (GS-MBE), using an RF plasma source for the nitrogen supply, at UPM. This technology aims to obtain low cost UV detectors. Photoconductive detectors early attracted much interest because of their simplicity and high responsivity. However, present devices show very high DC responsivities that are very dependent on the incident power and on temperature, and extremely slow and non-exponential transient responses (persistent photoconductivity effects, PPC). All samples show a significant response below bandgap.

AlGaN Schottky and p-n photodiodes have also been fabricated. These devices show excellent linearity with optical excitation, fast responses and a visible rejection of more than 10^3 . Figure 1 shows how the detection cutoff wavelength shifts with Al content in Schottky photodiodes, whereas the responsivity decreases with Al%. It has been shown that the use of ELOG substrates allows to improve both the device responsivity and the UV/visible rejection ratio. Figure 2 shows the responsivity of Au-$Al_{0.35}Ga_{0.65}N$ photodetectors grown on Si and sapphire by plasma-assisted MBE. Schottky metal-semiconductor-metal (MSM) photodetectors on AlGaN layers have also been fabricated, and a very good UV/visible contrast ($>10^4$) obtained [1-3]. Photodiode time response is usually limited by their intrinsic RC product. PPC effects appear to be a key issue in AlGaN-based UV photodetectors. They are also present in photodiodes showing poor quality Schottky barriers. Dislocations are also key 1/f noise sources.

Concerning applications, there is today a significant interest on the effects of the solar UV radiation on the biological ecosystem. Some examples of AlGaN detectors in this area will be

discussed [4].

Figure 1.- Spectral response of AlGaN Schottky photodiodes as a function of Al mole fraction..

Figure 2.- A comparison of spectral response of $Al_{0.35}Ga_{0.65}N$ photodiodes grown

(a) on sapphire and on Si(111), (b) before and (c) after breakdown.

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Ultra-Low-Noise Avalanche Photodiodes and Al$_x$Ga$_{1-x}$N/GaN Photodetectors

J. C. Campbell, A. L. Holmes, Jr., and R. D. Dupuis

University of Texas
Austin, TX 78712

Resonant-cavity In$_{0.52}$Al$_{0.48}$As/ In$_{0.53}$Ga$_{0.47}$As APDs with separate absorption, charge, and multiplication regions (SACM structure) that operate near 1.58 μm have been demostrated. These APDs achieved very low excess noise factors (k equivalent to 0.18). In the low gain regime (M<10) the bandwidth was >20 GHz; at higher gains a gain-bandwidth-product of 290 GHz was achieved. Recently, even lower noise has been achieved with thin (~0.1 to 0.2 μm) Al$_x$Ga$_{1-x}$As (x>0.8) and with impact ionization engineered multiplication layers. These devices have exhibited the lowest excess noise reported for any avalanche photodiodes (including Si APDs). Al$_x$Ga$_{1-x}$N photodetectors have been developed for solar blind imaging. To date, the PIN photodiodes have achieved high quantum efficiency (~75%), low dark current (<0.3 nA/cm^2), and high speed (f$_{3dB}$>5 GHz). In addition, initial GaN APDs have been demonstrated.

Using APD structures with very thin multiplication regions we have demonstrated the lowest excess noise and the highest gain-bandwidth products reported for any APD. For example, with Al$_x$Ga$_{1-x}$As (x>0.8) multiplication regions excess noise less than that of Si APDs for gains <10 and comparable noise for higher gains has been achieved. Recently, we have demonstrated an impact-ionization-engineered structure. By enhancing the control of the impact-ionization position, the structure achieved high gain, low dark current, and very low noise. In the low gain regime, the noise is less than twice the shot noise. To put this in perspective, in terms of McIntyre's local-field model (which we have shown is not applicable for these structures) a theoretical fit would require negative values of k, a widely accepted figure of merit for multiplication noise. We have demonstrated, both experimentally and theoretically, that the low noise is due to the nonlocal nature of the impact ionization process and the fact that nonlocality becomes a dominant effect in very thin high-field regions.

For long-wavelength operation (λ~ 1.58 μm), a 200 nm In$_{0.52}$Al$_{0.48}$As layer was used as the multiplication layer in a resonant-cavity APD with separate absorption, charge, and multiplication regions (SACM structure). These APDs achieved very low excess noise factors (k equivalent to 0.18). For comparison, the k factor of commercially-available III-V compound APDs is typically greater than 0.5. These APDs also achieved record bandwidths. In the low gain regime (M<10) the bandwidth was >20 GHz; at higher gains the response was characterized by a gain-bandwidth-product of 290 GHz. The unity-gain external quantum efficiency was ~65% at λ=1.58μm. In addition, the bias voltage was in the range 20 to 25V.

The detection of light in the ultraviolet (UV) portion of the electromagnetic spectrum is critical to a number of applications. Until very recently, the primary means of light detection in the UV was with either silicon photodiodes or photomultiplier tubes, both of which have serious drawbacks. With the advent of optoelectronic devices fabricated in the ternary alloy of AlGaN, the possibility exists to produce high-performance solid-state photodetector arrays sensitive to the visible-blind and solar-blind regions of the spectrum. However, in order for Al$_x$Ga$_{1-x}$N/GaN photodetectors to surpass the performance of PMT's, it is critical to improve the sensitivity of nitride-based photodetectors since PMT's are capable of achieving very high sensitivity through high internal gain and low noise.

To date, many of the published GaN p-i-n photodiodes have been plagued by relatively low external quantum efficiency and their spectral responsivity frequently shows a peak near the band-edge, with a precipitous decline in quantum efficiency at the shorter wavelengths. Previously, we have modeled the quantum efficiency of GaN-based p-i-n photodiodes and shown that these characteristics are the result of an "optical dead space" at the top surface of the photodiodes. This dead space is hypothesized to be a consequence of the internal electrical field underneath the surface of the p-GaN layer. Since the absorption coefficient in GaN is $> 10^5$ cm^{-1} for $\lambda < 360$ nm, the thickness and material composition of the p-layer become important design parameters in a front-surface illumination configuration in order to mitigate the deleterious impact of the optical dead space on the quantum efficiency. One way to reduce the optical absorption and subsequent carrier recombination in the p-type layer is to reduce the thickness of this layer with a recessed window structure. A schematic cross section of this device structure is shown if Fig. 1.

Figure 1. Cross-section of Al$_x$Ga$_{1-x}$N/GaN recessed window photodiode

Figure 2. External quantum efficiency of Al$_x$Ga$_{1-x}$N/GaN recessed window photodiode

At a reverse bias of 4 V, the efficiency was ~75% for 350nm $< \lambda < 360$ nm. At shorter wavelengths, the optical signal was absorbed in the p-type Al$_{0.13}$Ga$_{0.87}$N window layer. It is clear that the quality of p-type Al$_x$Ga$_{1-x}$N material needs to be improved but the efficiency is still ~ 30% at 280 nm. For imaging applications, R$_o$A is an important figure of merit, where R$_o$ is the differential resistance near 0 bias and A is the device area. The measured value of Ro is 5×10^9 W-cm^2, which yields a detectivity of D* $= 1.23 \times 10^{14}$ cm·Hz$^{1/2}$·W^{-1} Arrays of 32x32 GaN photodiodes (90 μm x 90 μm) have been fabricated and characterized. The characteristics of all the devices in the arrays were measured and Figure 3 shows a histogram of the dark current distribution. The mean dark current was < 1pA. Similar plots of the responsivity and the detectivity will be presented.

Figure 3. Dark current distribution of 32x32 GaN PIN array.

GaN avalanche photodiodes were successfully fabricated and characterized. Current-voltage characteristics indicated a gain higher than 20. The photoresponse was independent of the bias voltage prior to the onset of avalanche gain which occured at an electric field of ~4MV/cm. The breakdown showed a positive temperature coefficient that is characteristic of avalanche breakdown.

Highly selective GaN/AlGaN/GaN UV photodiodes

D.L. Pulfrey[1], M.P. Leslie[1], J.J. Kueck[2], B.D. Nener[2], G. Parish[3], U.K. Mishra[3],
P. Kozodoy[4] and E.J. Tarsa[4]

[1]Dept. ECE, Univ. of British Columbia, Vancouver, BC V6T1Z4, Canada
[2]Dept. EEE, Univ. of Western Australia, Perth, WA 6907, Australia
[3]Dept. ECE, Univ. of California, Santa Barbara, CA 93106, USA
[4]Nitres Inc., 107 S.Patera Lane, Goleta, CA 93117, USA

$Al_{0.33}Ga_{0.67}N$ has a highly desirable bandgap for UV photodetection purposes, but fabricating photodiodes from this material is presently hindered by difficulties in growing high-quality doped layers. A recent solution to the doping problem has involved the fabrication of *p-i-n* diodes in which an undopded AlGaN layer is sandwiched between layers of doped GaN. An analysis of this structure is presented, with emphasis on how the unwanted photocurrent generated in the low-bandgap window layer can be suppressed.

Introduction

$Al_{0.33}Ga_{0.67}N$ is a promising material for solar-blind photodetectors because its band-edge absorption occurs at a wavelength of 300 nm. However, the growth of thick, doped layers of this material is proving to be difficult. In a paper submitted to *Applied Physics Letters* in February, 2000, Kozodoy and Tarza report on a UV photodiode that circumvents these practical problems by using $Al_{0.33}Ga_{0.67}N$ only in undoped form, and creating a *p-i-n* diode by sandwiching this layer between layers of more easily doped GaN. To make this structure work, some way has to be found of suppressing the photocurrent due to absorption in the lower bandgap GaN layers, particularly that of the *p*-type window. Several methods for accomplishing this goal are analyzed here via simulations using MEDICI.

Results and Discussion

The ratio of the UV photoresponse (at 295 nm) to the solar photoresponse (at 305 nm) is referred to here as the rejection ratio (RR): a value of around three orders of magnitude is considered to be a minimum requirement for a useful device.

For the doping densities and regional thicknesses considered here, the basic device with no features for diminishing the solar response yields an unacceptable value of RR=3. An improvement of two orders of magnitude can be achieved by suppressing the photocurrent generated in the bottom *n*-GaN layer by introducing a deep quantum well at the AlGaN/GaN interface to trap the photogenerated holes. A suitable material for this quantum well appears to be $In_{0.2}Ga_{0.8}N$. A further improvement of one order of magnitude results from placing an additional $In_{0.2}Ga_{0.8}N$ quantum well at the interface between the *p*-GaN window layer and the *i*-AlGaN layer. These results indicate the effectiveness of the quantum wells in creating sites for minority-carrier recombination.

Another possibility for reducing the photocurrent generated in the window layer is to introduce tunneling barriers in the window layer. The effect of a δ-doped, *p*-type, $Al_{0.33}Ga_{0.67}N$ quantum "pillar" was investigated and found to be effective only if it was merged with the undoped $Al_{0.33}Ga_{0.67}N$ layer. In this manner it thickens the tunneling barrier for the unwanted electrons that are photogenerated in the window layer. If the quantum pillar is positioned in the window layer itself, electrons can be trapped between the pillar and the *p-i*-interface, thereby increasing the electron concentration from which the undesirable tunneling occurs.

The best results obtained to date involve a device with $In_{0.2}Ga_{0.8}N$ quantum wells in each of the GaN layers, and a δ-doped, *p*-type, $Al_{0.33}Ga_{0.67}N$ layer at the top surface of the *i*-$Al_{0.33}Ga_{0.67}N$ absorber. In this case a value of RR=5000 is predicted.

Green SQW InGaN light-emitting diodes on Si(111) by metalorganic vapor phase epitaxy

Eric Feltin, S. Dalmasso, H. Larèche, B. Beaumont, P. de Mierry, M. Leroux and P. Gibart

Centre de Recherche sur l'Hétéro-Epitaxie et ses Applications, Centre National de la Recherche Scientifique, Rue B. Grégory, Sophia-Antipolis, 06560 Valbonne, France

We report the fabrication of InGaN green light-emitting diodes (LEDs) on Si(111) substrates using metalorganic vapor phase epitaxy. A single quantum well of InGaN has been used. The LEDs start emitting light at 3.5 V with an electroluminescence (EL) peak at 508 nm, and a FWHM of 52 nm. The turn on voltage is 6.8 V and a current of 20 mA could be driven with an operating voltage of 10.7 V.

Most of III-N optoelectronic devices commercially available are fabricated on sapphire or SiC substrates. On the other hand, research on development of devices on silicon substrates is only beginning, in spite of the several advantages offered by this substrate (the possibility of electronic integration, the large size available, the low cost and the good thermal conductivity). It could be partly explained by the difference in lattice mismatch between nitrides and silicon substrates (17%), leading to high defects density. These structural defects are known to degrade the efficiency of devices. But a more important problem comes from the difference in thermal expansion coefficient between GaN and Si, which is responsible for the apparition of cracks for thick layers (typically about 1.4 μm). Despite these problems, some ultraviolet and blue LEDs on silicon substrates, fabricated using metalorganic chemical vapor deposition (MOCVD) (Tran *et al.*) as well as molecular beam epitaxy (MBE) (Guha *et al.*) have been reported. In this letter, we now report the growth of a green InGaN light-emitting diode made by MOVPE on Si(111).

The growth of LEDs on Si(111) was carried out in a home-made vertical reactor at low pressure (30 kPa). The LED structure consists of a 0.5 μm thick n-type (2.10^{18} cm^{-3}) GaN:Si layer, a 0.1μm thick undoped GaN layer, a single InGaN quantum well (with an indium mole fraction of about 20% in stress free conditions) and an $Al_{0.1}Ga_{0.9}N$ barrier of 7nm, followed by a p-type ($\sim 5.10^{17}$ cm^{-3}) GaN:Mg layer of 0.2 μm. A planar geometry, similar to the one used usually on sapphire substrate was used, with mesas made by reactive ion etching down to the n-type layer, because the buffer layer under the LED structure is insulating. Ti/Al/Ni/Au (15 nm/80 nm/20 nm/100 nm) and Ni/Au (20 nm/100 nm) ohmic contacts were made on n-type and p-type layers respectively with a semitransparent contact on the top (3 nm Ni).

fig.1 : PL spectra of InGaN layers on sapphire and Si at room temperature.

As seen on fig. 1, comparison of the photoluminescence intensity at room temperature of an InGaN layer grown on silicon has shown that InGaN with optical quality similar to that expected on sapphire could be obtained on Si(111). As it was reported for sapphire and ELOG substrates by Mukai *et al.*, the density of dislocations, higher for GaN on silicon than on sapphire, does not seem to significantly affect the band edge emission of InGaN layer. However the p-doping efficiency of GaN seems to be lower on silicon than on sapphire probably due to a higher density of defects. We have usually a dislocations density of 8×10^9 cm^{-2} for GaN layers on silicon (determined by atomic force microscopy images in tapping mode) compared to mid 10^8 cm^{-2} for GaN on sapphire. For this structure, the

estimated hole concentration of the GaN:Mg layer (about $5x10^{17}$ cm^{-3}) is lower than the hole concentration expected for the same process on sapphire ($\sim 3x10^{18}$ cm^{-3}).

fig. 2 : I(V) characteristics of a LED

We present on fig. 2 the I(V) characteristics at room temperature of a diode. A current of 20mA is obtained for a forward bias of 10.7 V. The turn on voltage is 6.8 V, which is higher than that for a similar LED on sapphire. This is at least partly explained by the high series resistance of LEDs grown on Si probably due to unoptimised Mg doping. There is also a high shunt resistance in forward bias due to a high density of threading dislocations present in these materials.

The diodes start emitting light for a forward bias in the 3-4 V range. Fig. 3 shows the electroluminescence spectra of a LED grown on Si for different bias. The EL spectra is dominated by InGaN luminescence visible at 508nm (2.44 eV) with a width at half maximum of 52 nm (250 meV). Oscillations in the spectra came from the interferences in the structure. For an applied current higher than 20 mA, recombinations in GaN layers at 367 nm (3.37 eV) appear.

fig.3 : EL spectra of a LED for different currents.

In conclusion, the first green light-emitting diodes (508 nm) with a single InGaN quantum well grown on silicon substrates was demonstrated using an MOVPE process. Although photoluminescence and electroluminescence are comparable to that expected on sapphire, the electrical characteristics remain inferior to what is expected on sapphire, due in part to a higher density of dislocations. Improvement of the performances of the diodes grown on Si(111) should be obtained with an optimisation of the growth of GaN and with a better control of the p doping on silicon.

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