TOWARD THREE DIMENSIONAL CIRCUITS FORMED BY MOLTEN-ALLOY DRIVEN SELF-ASSEMBLY

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ABSTRACT

Self-assembly opens new possibilities in three-dimensional (3-D) device structures, and here we report on our progress toward a self-assembling 3-D circuit. A major challenge to such a system has been the fabrication of large numbers of free-standing, microfabricated parts, and we have overcome this challenge by developing a new wafer-bond and release process. We present this process on 100 mm diameter wafers, and finally show initial assembly results.

1. INTRODUCTION

Self-assembly, or the spontaneous organization of parts into larger structures via energy minimization, is an attractive solution to overcome manufacturing challenges for the integration of small devices from incompatible processes, or for integration in three dimensions. Self-assembly opens new possibilities in three-dimensional (3-D) material and device structures (Morris et al. 2005), and allows the manufacture of microsystems by assembling pre-microfabricated parts in different ways. The use of these methods enable many defense applications such as microsensors, microrobotics, and high performance computing, without having to customize a wafer-scale manufacturing process for each individual application.

One class of self-assembly methods is based on capillary forces, and the use of molten alloys for self-assembly readily allows electrical connections between assembled components. Earlier studies employing molten-alloy based self-assembly involve large, millimeter scale parts such as those made of polyurethane and manually-applied mercury droplets (Terfort; Whitesides 1998), or hand-fabricated PDMS parts with electronic or electrical components glued to them for the self-assembly of 3D circuits (Gracias et al. 2000). At the microscale, many researchers demonstrate the utility of assembling micrometer-scale parts at specified regions on planar templates using molten alloys (Jacobs et al. 2002; Stauth; Parviz 2006), including (Morris; Parviz 2008) where filled-to-available binding site yields exceed 97%.

Figure 1 shows a model system for the investigation of 3-D, self-assembled circuit elements. The triangular parts in Fig. 1A) contain several features designed to insure correct assembly. A slotted geometry and solder alloy deposited on the interior region of the slot allow complimentary shapes to insure correct orientation upon assembly. The geometry of the slot and location of the solder alloy ideally prevent any overlap of the alloy on one part with the alloy on another part encountered in an "upside down" orientation. Electrical vias near the exterior of the slot provide alloy-wetable binding sites on the underside, so that upon assembly in the correct orientation, the alloy and binding site overlap and a capillary bond forms. The interconnect metal, which connects vias, alloy bumps and any embedded circuitry is not wetable by the alloy, to prevent incorrect alloy binding. Figure 1B) shows 3-D self-assembled structures, and a cross sectional detail of the 3-D electrical interconnects. The parts are intended to be entirely compatible as a post process to any CMOS or wafer-scale packaged MEMS device, and generally do not involve temperatures greater than those associated with photolithography steps.

One motivation for this model system comes from the growing interconnect delay in modern integrated circuits (Brown et al. 2004), requiring either replacement of on chip metal interconnects with optical waveguides (Oktyabrsky et al. 2002) or new 3-D circuit architectures in order to enable continued increases in computing performance. Approaches to 3-D circuit architectures involve pseudo 3-D chip stacking with

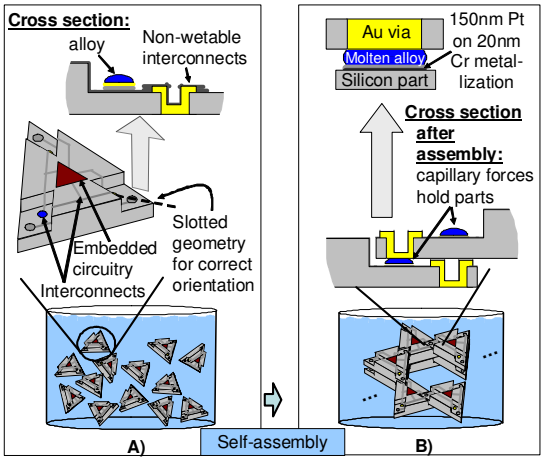

Fig. 1. Schematic showing capillary force based self-assembly using a molten alloy to form three dimensional electrical connections.

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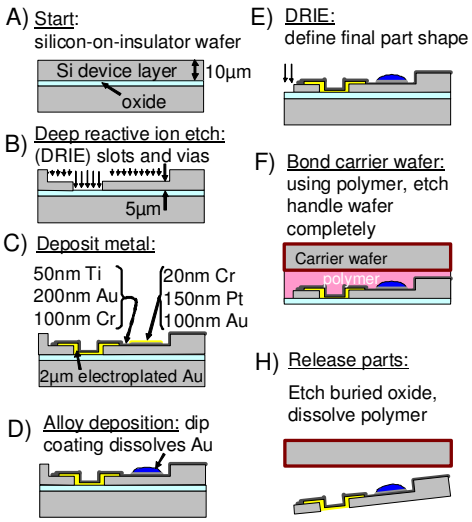

Fig. 2. Fabrication process for parts shown in Fig. 1 (for simplicity, only half of one part is shown in each cross sectional view).

solder bumps allowing up to 10^5 3-D vias/cm^2 (Kripesh et al. 2005), or damascene copper via processes yielding up to 10^8 vias/cm^2 (Topol et al. 2005). A second approach to fabricate stacked, 3D circuits is epitaxial-style growth of single-crystal materials over existing circuit features (Chan et al. 2001; Pae et al. 1999). However, the serial method of adding each additional layer in either of these two approaches limits the total number of layers and 3D interconnects. We are investigating self-assembly as a way to form many layers of circuitry in a parallel fashion.

2. METHODS

2.1. Part Fabrication

To fabricate the parts in Fig. 1, we started with a silicon-on-insulator (SOI) wafer having a 10 µm device layer as shown in Fig. 2A). We defined slotted features with a 5 µm deep reactive ion etch (DRIE), and 20 µm wide vias with another 5 µm DRIE step in Fig. 2B). Figure 2C) shows several metallization layers, starting with 2 µm of electroplated Au partially filling the vias. The electroplating seed layer was 200 nm Au followed by a protective 50 nm Ti layer, both deposited by DC sputtering. After photoresist patterning and prior to electroplating, we etched the Ti layer with a 25:1:1 H_2O:HF:H_2O_2 solution to expose the Au layer. Then we electroplated 2 µm Au in a commercially-available bath (Technigold 25, Technic, Inc., Pawtucket, RI) at 49°C, 3 mA/cm^2, 1:10 duty cycle (1 ms on, 10 ms off), and for a time of 25 minutes. After photoresist removal, the same Ti etch solution and a Au etch solution (GE-8110, Transene, Danvers, MA) removed the seed layers. The other metal layers shown in Fig. 2C) included a sputtered interconnect multilayer of 50 nm Ti, 200 nm Au, and 100 nm Cr, and an evaporated multilayer consisting of 20 nm Cr, 150 nm Pt, and 100 nm Au for solder underbump metallization. A lift-off procedure in acetone patterned both of these layers.

Next, we deposited a lead-free, eutectic Bi-Sn alloy with a 138°C melting point shown in Fig. 2D). First, we evaporated 100nm of Au to insure that the alloy would wet the entire substrate. We dipped the wafer substrate through a 160°C ethylene, and the Au quickly dissolved allowing the alloy to react with the Pt layer. Upon removal of the substrate through this glycol/molten alloy interface, the alloy dewetted from all Si and Cr areas, leaving the alloy only at the prescribed locations. Without the additional Au deposition step, the alloy tended to not wet contact pads located in the recessed, slotted features, and attempts at using ultrasonic agitation to encourage such wetting did not work.

The final steps included Fig. 2E), where DRIE defined the final part shape, and Figs. 2F) 2H). In order to produce large numbers of free-standing, microfabricated parts, we developed a wafer bond and release process. Although early examples of microscale self-assembly used wafer bond and release processes (Talghader et al. 1995; Tu et al. 1995), process details are not readily available, and most studies since then have used conventional oxide etches for parts release. Unfortunately, these processes are too corrosive to all but a small subset of materials, and the solder alloy is not part of that subset. Therefore, we developed the process in Figs. 2F) by bonding a carrier wafer to the devices using a spin-on polymer (ProTEK A2, Brewer Sciences, Inc., Rolla, MO) and a wafer bonding tool set for 1 Torr, 150°C, and 1 atm applied pressure. We then etched away the handle layer of the SOI wafer using DRIE followed by a XeF_2 etch for approximately the last 20µm. At this point the oxide layer tended to crack, so we also pre-patterned crack sites in the oxide between parts immediately following the DRIE step in Figs. 2E) but using a different mask (not shown). Finally, we etched the exposed buried oxide in 49% hydrofluoric acid, and dissolved ProTEK in a dodecene-based solvent (ProTEK Remover 200, Brewer Sciences). The parts quickly sank to the bottom of the ProTEK Remover 200 container, allowing us to dilute the solvent with IPA by a factor of 10^3, followed by dilution with DI water by another factor of 10^3.

2.2. Self-Assembly

For self-assembly, we suspended approximately 10^4 parts in approximately 4 ml glycerol with 0.1 mM HCl to insure that Bi-Sn binding sites remain free of surface oxides and able to properly wet and bind with intended part binding sites. We placed the vial in a

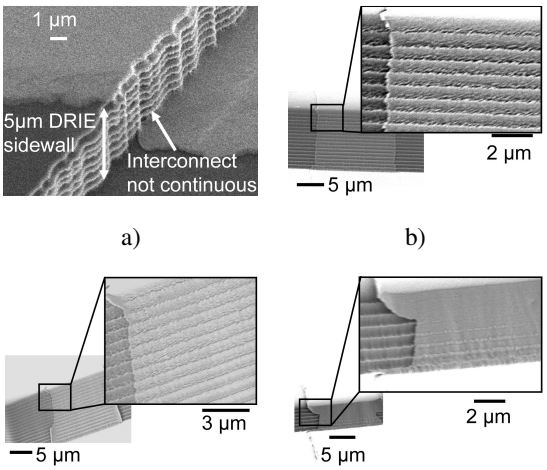

Fig. 3. SEM images of interconnects over sidewalls. a) 400 nm evaporated Cr. b) 200 nm DC sputtered Ti. c) 200 nm DC sputtered Cr. d) 200 nm DC sputtered Au, sandwiched by Ti.

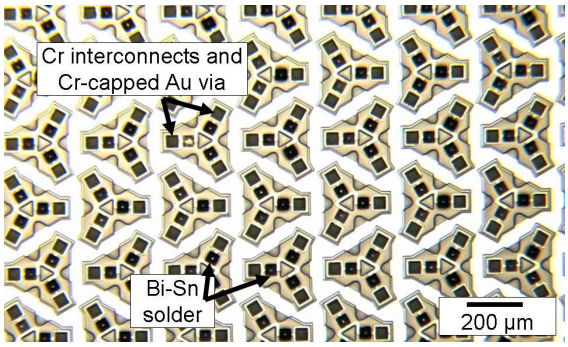

Fig. 4: Parts attached to wafer following the completion of the step in Fig. 2e).

180°C glycerol bath, and began applying fluidic flow pulses of approximately 1 ml discharged through a Pasteur pipette every 1 s to stir the parts, continuing this agitation for 3 min. Whenever a part contacted a liquefied Bi-Sn binding site, capillary forces from the alloy held the part in place.

3. RESULTS

3.1. Completed Parts

There were several interesting processing issues to address along the way to achieving fully released parts for three-dimensional circuit self-assembly. One example was the deposition of continuous interconnect features over deep reactive ion etch (DRIE) sidewalls. Figure 3 shows different interconnect metallization combinations. Figure 3a) shows that 400 nm of evaporated Cr did not fill in the gaps between the scallops resulting from the DRIE Bosch process., even

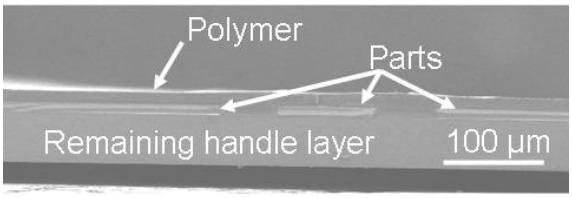

Fig. 5. Cross-sectional SEM view of parts on a partially-etched handle layer, with good contact between parts and polymer encapsulant (carrier wafer has been removed and is not shown).

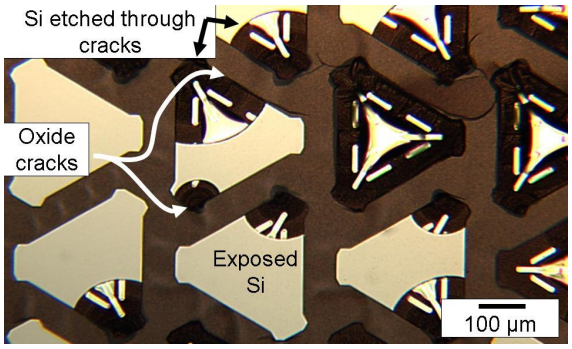

Fig. 6. Cracks in oxide layer causing parts to etch during handle etching step.

though the evaporation was done with constant substrate rotation between ±60°. The SEM image shows visible breaks in the film, and electrical resistances were on the order of 30×10^9 Ω (up from only 100-200 Ω for a similar interconnect what was completely contained in a single plane). In Fig. 3b), a sputtered Ti layer at 22 mTorr did not provide good continuity over a 10 µm deep DRIE sidewall either, with measured electrical resistances on the order of 10^3 times higher. Figure 3c) shows that a 200 nm sputtered Cr layer was close to being continuous, but measured electrical resistances were still 10 times higher when going over a sidewall. The 50 nm Ti, 200 nm Au, and 100 nm Ti layer in Fig. 3d) was continuous, with nearly identical electrical resistances between cases where a sidewall was present or not. Thus, Ti alone did not produce a good interconnect, but the combination of Ti, Au, and Ti did. A layer of Ti-Au-Cr also resulted in an electrically-connected interconnect (not shown). Using the Ti-Au-Cr given section 2.1, and continuing with process steps depicted in 2a) through 2e), we obtained the devices shown in Fig. 4.

The primary process challenge was to release parts from the handle wafer in a manner which was compatible with materials already on the devices. We found that it was necessary to bond carrier wafers under vacuum, because any trapped air pockets could later caused excessive cracking of the oxide, parts, and polymer layers. The use of low ambient pressure and a

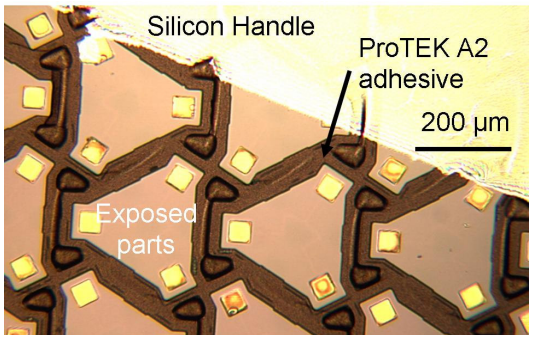

Fig. 7. Undersides of parts exposed as handle wafer was etched (Fig. 2f).

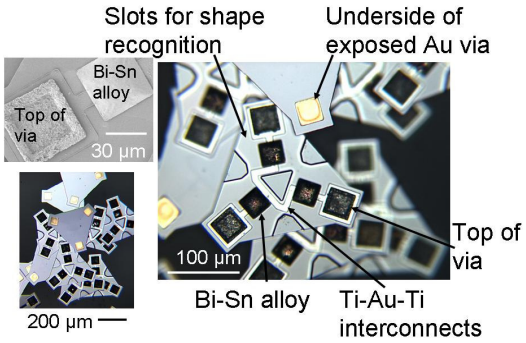

Fig. 8. Released and fabricated parts ready for the assembly shown in Fig. 1.

consistent bonding force resulted in good bonds between the parts and polymer as shown in Fig. 5. However, as shown in Fig. 6, cracks still occurred in the thin oxide layer once it was exposed and lost the structural support provided by the handle layer. These cracks allowed the highly permeable XeF_2 gas etchant to etch the Si parts away at a wafer edge before all of the handle was etched away, resulting in the partial devices shown in Fig. 6. But by pre-patterning the oxide layer with the features shown in Fig. 7, much of this oxide cracking was minimized, allowing the silicon handle to be etched away without damaging the underlying parts.

3.2. Self-Assembly

Following the successful release of these parts from the carrier wafer, a collection of free-standing parts is shown in Fig. 8. Figure 9 shows our initial attempts at a 3-D self-assembling circuit. For this particular case, slot heights and part thicknesses were too small for the Bi-Sn solder features used, so the slotted features were not able to prevent incorrect assembly and parts assembled in uncontrolled ways. Still, the SEM image in Fig. 9 shows the promising result that the molten alloy functioned as intended by binding to neighboring parts.

4. Conclusion and Future Work

We have demonstrated a fabrication process which resulted in the first set of sub-millimeter scale, single-crystal semiconductor parts which are able to participate in a self-assembly process to form 3-D circuits. We are currently fabricating a set of wafers starting with a 20 µm thick device layer in order to end up with 20 µm thick parts, which should enable the intended self-assembly shown in Fig. 1.

Also, the newly developed release process opens up new possibilities for different materials to be incorporated on the parts, including microscale, patterned permanent magnets which we are currently

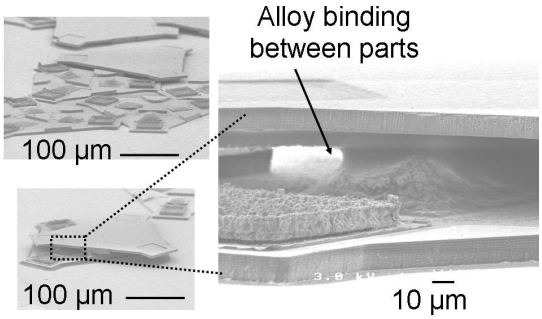

Fig. 9. Initial results for self-assembling circuit parts. The close-up image clearly shows binding by capillary forces.

developing at ARL. Such materials, in combination with electrical connectivity provided by the solder alloys described here, should enable new types of self-assembling circuits and structures.

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References

Brown, J., R. Packer, J. Prasad, K. Kofford, T. Dye, and B. Kirk, 2004: Hybrid approach to structured ASICs for minimizing the impact of reticle costs and interconnect delay. Custom Integrated Circuits Conference (CICC), IEEE, 427-429.

Chan, V. W. C., P. C. H. Chan, and M. Chan, 2001: Multiple layers of CMOS integrated circuits using recrystallized silicon film. IEEE Electron Device Letters, 22, 77-79.

Gracias, D. H., J. Tien, T. L. Breen, C. Hsu, and G. M. Whitesides, 2000: Forming electrical networks in three dimensions by self-assembly. Science, 289, 1170-1172.

Jacobs, H. O., A. R. Tao, A. Schwartz, D. H. Gracias, and G. M. Whitesides, 2002: Fabrication of a cylindrical display by patterned assembly. Science, 296, 323-325.

Kripesh, V., S. W. Yoon, V. P. Ganesh, N. Khan, M. D. Rotaru, W. Fang, and M. K. Iyer, 2005: Three-Dimensional System-in-Package Using Stacked Silicon Platform Technology. IEEE Transactions on Advanced Packaging, 28, 377-386.

Morris, C. J., and B. A. Parviz, 2008: Micro-Scale Metal Contacts for Capillary Force-Driven Self-Assembly. Journal of Micromechanics and Microengineering, 18, 015022.

Morris, C. J., S. A. Stauth, and B. A. Parviz, 2005: Self-assembly for micro and nano scale packaging: steps toward self-packaging. IEEE Trans. Adv. Packag., 28, 600-611.

Oktyabrsky, S., J. Castracane, and A. E. Kaloyeros, 2002: Emerging technologies for chip-level optical interconnects. Optoelectronic Interconnects, Integrated Circuits, and Packaging, J. R. Louay A. Eldada and Randy A. Heyler and Rowlette Sr, Ed., Proceedings of SPIE, 213-224.

Pae, S., J. P. Denton, and G. W. Neudeck, 1999: Multi-layer SOI island technology by selective epitaxial growth for single-gate and double-gate MOSFETs. Proc. IEEE International SOI Conference, 108-109.

Stauth, S. A., and B. A. Parviz, 2006: Self-assembled single-crystal silicon circuits on plastic. Proc. Natl. Acad. Sci., 103, 13922-13927.

Talghader, J. J., J. K. Tu, and J. S. Smith, 1995: Integration of fluidically self-assembled optoelectronic devices using a silicon-based process. IEEE Photonics Technology Letters, 7, 1321-1323.

Terfort, A., and G. M. Whitesides, 1998: Self-assembly of an operating electrical circuit based on shape complementarity and the hydrophobic effect. Advanced Materials, 10, 470-473.

Topol, A. W., and Coauthors, 2005: Enabling SOI-Based Assembly Technology for Three-Dimensional (3D) Integrated Circuits (ICs). International Electron Devices Meeting (IEDM) Digest, Washington D.C., 363-366.

Tu, J. K., J. J. Talghader, M. A. Hadley, and J. S. Smith, 1995: Fluidic self-assembly of InGaAs vertical cavity surface emitting lasers onto silicon. Electronics Letters, 31, 1448-1449.