Evaluation of a 10 kV, 400 kA Si SGTO at High dI/dt

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***Abstract* – The evaluation of each 10 kV, 400 kA Si SGTO included a visual inspection and high-potting of each component module prior to pulsing. The complete unit was then switched in a low inductance RLC circuit to test voltage and current capabilities and maximize dI/dt. Devices were switched as many as 70 times without failure. Voltage sharing between the layers was within ± 2%, and current sharing between the modules was ± 5% of ideal sharing. The peak rate of current rise attained was 40 kA/µs, and the 50% pulse width of the current was 26 µs. The peak power switched was 1.06 GW, and the action of the forward current pulse reached 6.4 MA^{2}s. This report includes details on the methods for evaluating the 400 kA SGTO, challenges faced and peak performance of the devices under single shot pulsing conditions.**

I. INTRODUCTION

The U. S. Army Research Laboratory (ARL) is evaluating high current, modular silicon Super GTOs (SGTOs) for single-shot and repetitive pulse applications [1]. These devices are designed and fabricated by Silicon Power Corporation (SPCO), and their switching capabilities and limitations are tested by a team at ARL. These solid state switches are being studied as replacements for bulkier vacuum switches and SCRs because of the proven potential for higher power switching, higher dI/dt, greater current densities, and increased reliability [2, 3]. The cell-based SGTO design is intended to improve turn-on time and reduce gate drive requirements compared to traditional single-wafer thyristors. By developing modular switches using the SGTO cells, high rate of current rise and action can be attained in the most compact and reliable switch possible.

II. DESIGN

The 10 kV, 400 kA SGTO (Fig. 1) is comprised of twenty-four smaller modules joined six in parallel and four layers in series. Each of these component modules (Fig. 2) is rated for 3.5 kV holdoff and 80 kA of forward conduction [3]. The overall 400 kA units are over-designed for voltage and current capabilities in order to minimize stress on the devices and maximize reliability but still stay compact. Voltage is distributed to the four anode layers of the device by a resistor network of 900 kohm per layer. Gate current is applied to all twenty-four modules in parallel via printed circuit boards.

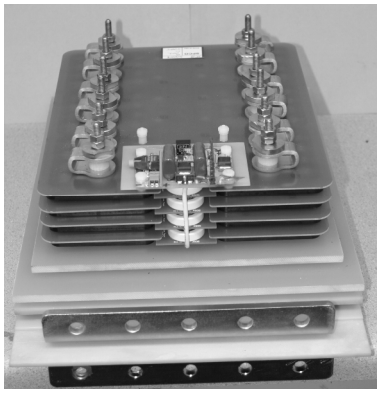

Fig 1. Four-layer SGTO with fast gate driver.

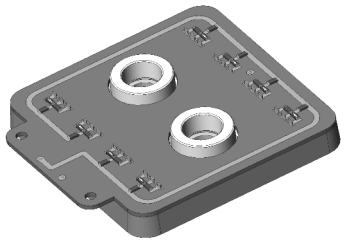

Fig. 2. Individual SGTO module, cathode side up.

Negative voltage at each gate was initially clamped by board-mounted diodes G→K, but they were later removed and replaced with external circuit clamping. The full switch is supported by heavy copper buss bars that are designed to bolt to other circuit components and carry high current into and out of the switch. The overall dimensions of each 400 kA SGTO are 17.0" x 10.5" x 6.34".

The first gate driver used to trigger the Si switches in this study provides a 480 A, 9 µs pulse. It operates at 24 V and is switched via a fiber optic receiver. It is isolated from the rest of the switch by a pulse transformer on each level, resulting in one primary wire and four secondary wires. For maximum safety, batteries were used for the driver's supply voltage. During the course of this research, SPCO also developed a faster gate driver designed to reduce the conduction delay by 300 ns. The faster driver only requires a 12 V input and includes a DC/DC converter and voltage regulator to step up

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14. ABSTRACT

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the board voltage as high as 100 V. This increases the amount of current at the output to well over 600 A, but more importantly increases the slope of the initial rise of the gate current.

III. Evaluation

Six 400 kA SGTOs were evaluated in this study. Initial evaluation of each SGTO started with disassembling the unit and visually inspecting the gate driver board and individual modules for any loose solder joints or damage incurred during shipping. High voltage insulation within the assembly layers was inspected as well. A handheld ohm meter was used to check for shorted gates and for good conductivity at points where gate current was distributed to each individual module. Each module was high-potted beyond the 3.5 kV rating, and after reassembly, the whole switch was high-potted on the bench top to 10 kV. Without any anode voltage applied, gate driver functionality was verified using a Rogowski coil at the primary of the pulse transformer and confirming a current level in the hundreds of amps during triggering.

A ring down RLC circuit (Fig. 3) was designed with minimum inductance to test for peak dI/dt of anode-cathode flowing current. A single 860 µF capacitor was charged to a chosen high voltage, then the power supply was disconnected and the switch was triggered to rapidly discharge the voltage across a resistive load of 0.015 ohm. Probes monitored voltage drops across the layers of the switch, total current at the anode and current carried by each stack of modules. The switch was pulsed at increasing 500 V intervals so that any possible problems could be caught at the lowest voltage or current at which they may be incurred. Most of the 400 kA units were tested up to 9.8 kV and 350 kA. The first device tested was switched all the way up to 10.2 kV, resulting in a 376 kA current pulse with a 10%-90% rise time of 7.6 µs and a dI/dt of 40 kA/µs.

Rather than push the applied voltage beyond 10.2 kV in this RLC circuit, the 400 kA SGTO and resistive load were next moved to a larger energy storage bank to help reach higher peak current. The bussing for the assembled circuit added extra inductance, so the dI/dt never exceeded the 40 kA/µs that it reached with the lower inductance setup. The switch was pulsed at a single shot rate up to 8.8 kV and 400 kA. During the one 8.8 kV test shot, a failure elsewhere in the circuit caused the forward current pulse width to expand to about 65 µs and then ring negative to -60 kA. When the SGTO switch was retested at 2 kV, the voltage and current waveforms all looked normal, but it was later discovered that

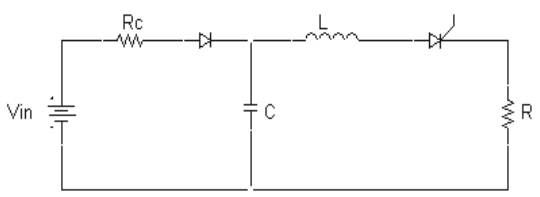

Fig. 3. Generic ring down RLC circuit for pulsing SGTO.

many of the protective diodes mounted across each gate had failed shorted. They were likely overheated by the unexpected wide negative current pulse. The shorted diodes stressed the modules during subsequent test shots because gates with failed diodes were shorted to the cathode and not being triggered to the on-state. The forward current of the switch was then being carried by fewer devices. It was determined that for future testing, the gate clamping diodes at the modules should be removed and a large, external diode clamp should be used to limit negative current seen by the switch's anode and gates.

If any SGTO modules showed signs of failure during testing, they were replaced with spare modules, and the whole switch was again high-potted and tested at 500 V intervals up to peak current. After each unit successfully switched 350 kA, 10 kV was applied at the anode for several minutes to assure continuing voltage holdoff. Voltage balance across the layers was also double-checked to make sure there was approximately 2.5 kV across each layer.

The two types of driver that SPCO designed were evaluated on the bench top by comparing the gate currents that the drivers provided at the primary and secondary coils. The rise in voltage across the gate-cathode junction was also monitored. During high current switching, the time delay between the trigger input to the gate driver board and the fall of the high voltage at the anode was recorded.

IV. Results and Discussion

All six 400 kA SGTOs were successfully switched at least four times at 9.8 kV and 350 kA with a 50% pulse width of 26 µs. At this current level, the rate of current rise was typically about 35 kA/µs. The maximum dI/dt of 40 kA/µs was achieved at 376 kA (Fig. 4). The action for this test shot was 2.7 MA^2s, and the peak power switched was 1.06 GW.

When the switch and load were moved to the larger capacitor bank, the current pulse reached 400 kA (Fig. 5). The resulting forward action experienced by the switch was 6.4 MA^2s, and the reverse action was 0.10 MA^2s. Because the 400 kA SGTOs are being evaluated for forward flowing anode-cathode currents, and because SPCO rates the gates for a maximum reverse G→K voltage of -9 V [4], it was decided that negative voltages and currents should be clamped by

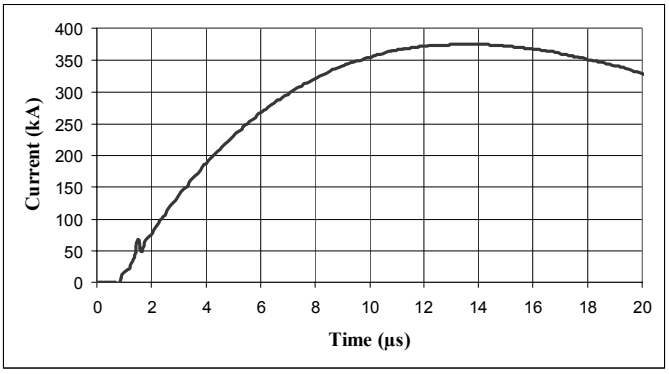

Fig. 4. Peak di/dt of 40 kA/µs during 376 kA pulse.

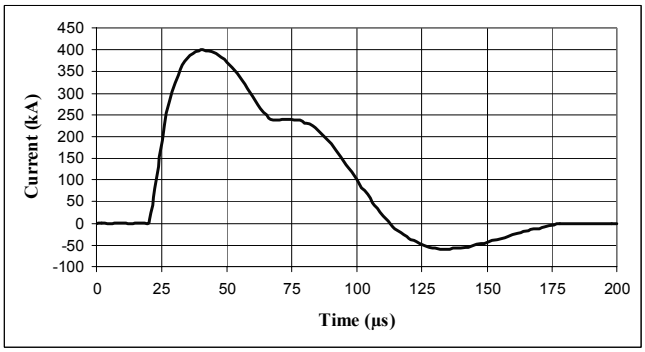

Fig 5. Peak forward current of 400 kA with slow rise time.

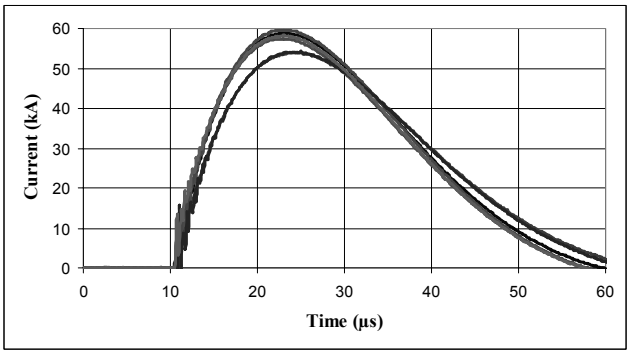

Fig. 7. Current balance between six modules, ±5% of equal sharing at peak.

external diodes in the circuit. An unpublished tangent study by the team testing how much negative current each module could handle unclamped suggested that a negative swing of greater than 30% of the forward current may irreversibly damage devices.

Careful attention was paid to how well the four layers of the switches shared voltage and how anode-cathode current was distributed among six parallel modules. An earlier version of the 400 kA SGTO delivered in 2004 failed to reach high voltages and currents because of harmful imbalances [5]. With 9.8 kV applied at the anode, each layer of the switch typically dropped 2.4 kV, or about 25% (Fig. 6). If voltage seen across a layer ranged beyond 22-28%, it was likely that one module nearby had excessive leakage current or had become shorted A→K. Two of the six switches in this study required module replacements before successfully switching at peak voltage and current, though one of those switches had sustained some earlier damage from the 400 kA shot that shorted many of its gate diodes.

Current balance between the modules was monitored with Rogowski coils at the cathodes of the six modules on the top (lowest voltage) layer. Ideally, each module would carry 1/6 of the total current, or 58.3 kA at peak. Minor variation in sharing does not affect the overall performance of the switch until the rating of 80 kA per module is neared. The best sharing seen during the 350 kA pulse had each module carrying within ± 5% of 58.3 kA (Fig. 7). The modules in the four corner positions typically carried slightly more current, while the two middle modules carried less, likely because of interacting fields between the parallel current paths.

Waveforms for the primary current were taken while varying the voltage on the gate driver. The initial slope of the current appears to be limited by the inductance in the wires but can clearly be improved by raising the voltage and the resulting peak current (Fig. 8). With 80 V on the driver board, the initial rise of the current was twice as fast as when only 25 V were used. The slope was affected very little when the voltage was increased from 80 V to 100 V. Improved rise time can also be seen with the voltage monitored directly at the gate (Fig. 9 and Fig. 10).

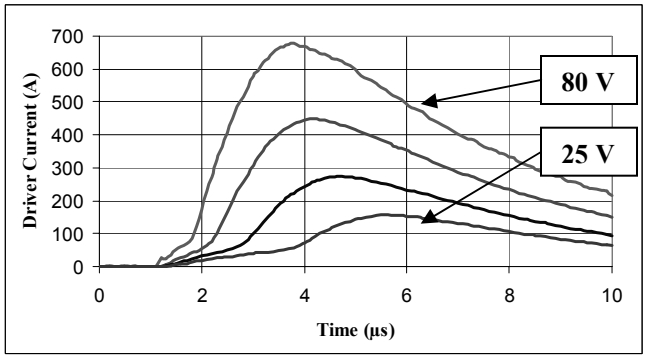

Fig. 8. Increase in driver current and initial di/dt as a result of increasing driver board voltage.

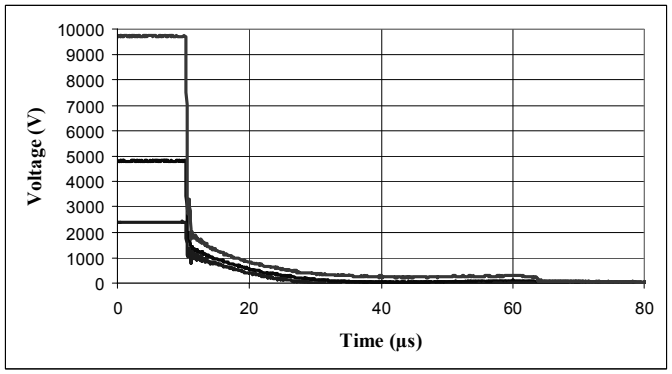

Fig 6. Voltage balance across four layers (100%), two layers (49.8%) and one layer (24.9%).

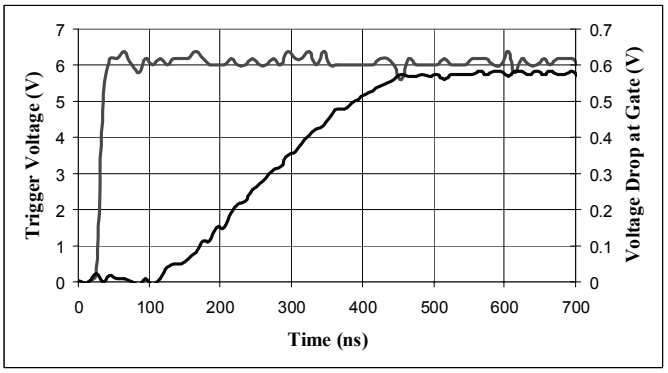

Fig. 9. Gate voltage rise time of about 270 ns with 25 V driver.

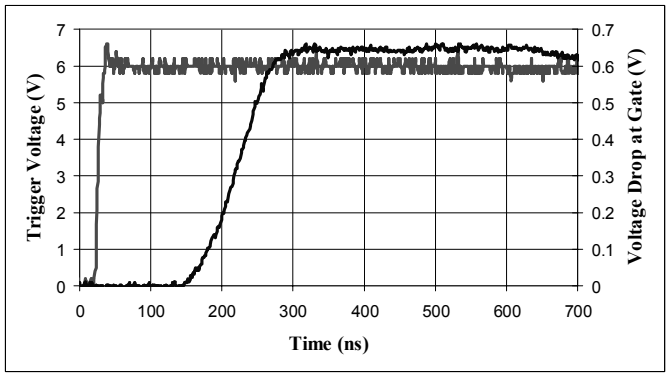

Fig. 10. Gate voltage rise time of about 100 ns with 100 V driver.

During peak current switching, a Tektronix oscilloscope with high density data capture and isolated channel inputs was used to view the time delay between the fiber optic trigger to the driver board and the point at which the high voltage on the anode began to fall. This time difference was found to be about 450 ns with the second, faster driver (Fig. 11).

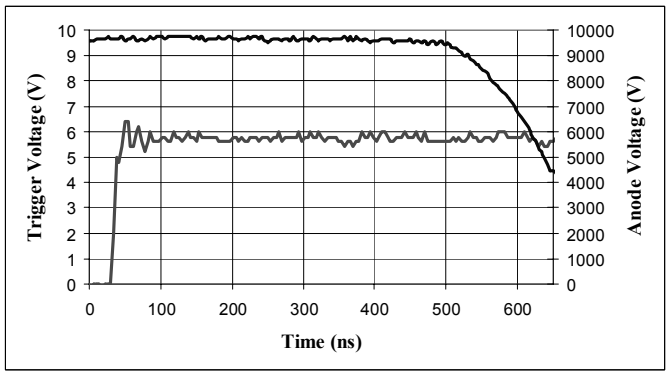

Fig 11. Time delay of about 450 ns between fiber optic trigger to driver and anode voltage drop.

V. Conclusions

This evaluation of the 10 kV, 400 kA SGTO shows that these units are capable of greater than 10 kV holdoff and as much as 400 kA of current and 40 kA/μs. One switch has been pulsed at 350 kA ten times and at lower currents an additional sixty times without failure. The switch can handle a positive action greater than 6.4 MA^2s, but is limited in the reverse. It is recommended that negative currents and voltages are clamped with external diodes to avoid damaging the switch.

The higher voltage driver succeeds in delivering gate current more quickly to the modules, decreasing the time delay between triggering and anode-cathode current flow. Driving the gates harder and faster results in a delay of only 450 ns.

Acknowledgment

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