Challenges in Imaging, Sensors, and Signal Processing

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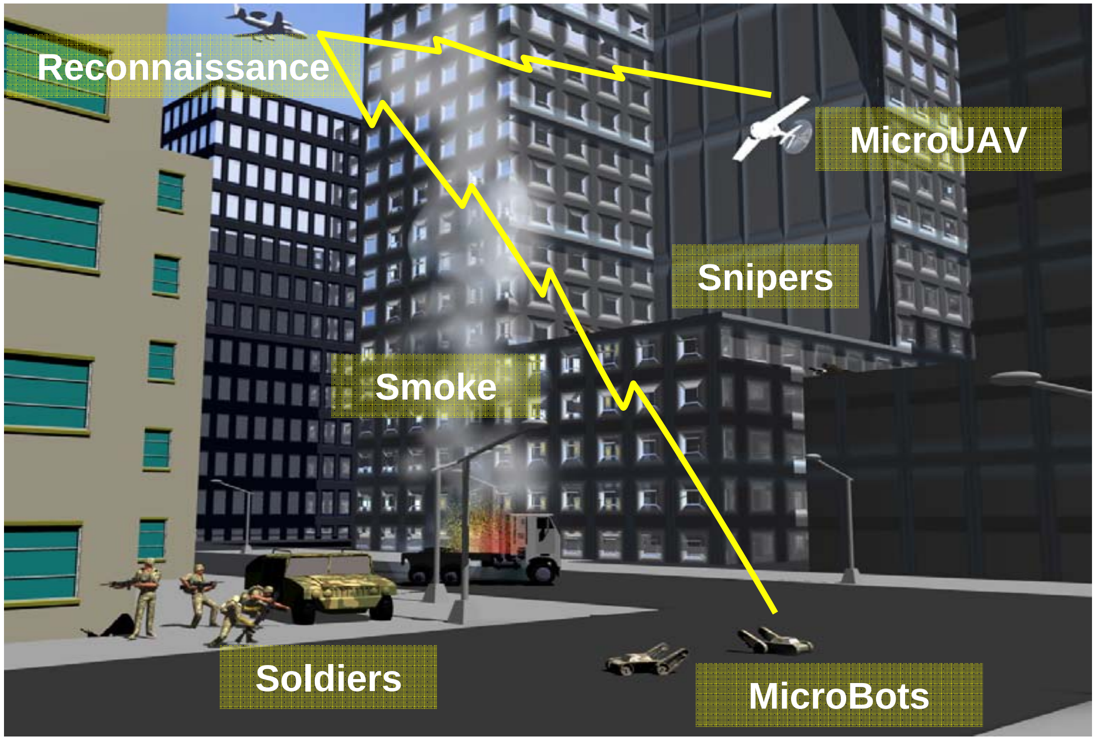
Outline

Challenges in Imaging, Sensors, and Signal Processing:

- The 3D FPA
- On-Focal Plane Processing
- Room Temperature Imaging
- Next Generation Multi-color &
  Adaptive Hyperspectral Sensors
- Sensor-on-a-Chip – Heterogeneous Material Integration
- Noiseless Imaging

Imaging & Sensing Technology Urban Scenario



Sensing technology for New Platforms:

- Next generation Micro-vehicles
  - ❖ Air and Ground
- Integrated sensing in multiple bands
- Operation in day / night
- Wide area persistent surveillance
- Information available on the ground
- Information available when needed
- Decisions-aids for critical information

Warfighter Will Have Inputs from Multiple Sources

Integration of these inputs into a common picture to provide:

❖ Threat location

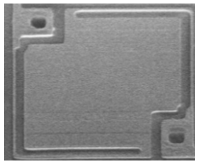
❖ Situational awareness – friend and foe

❖ Assets available from other units / platforms

❖ Effect of operations

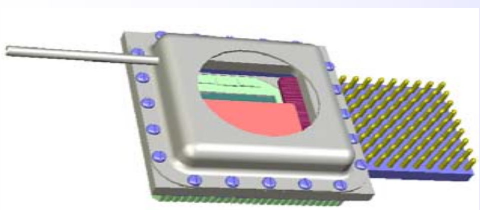
Imaging Micro-System Technology

Room Temperature Imaging



Current Programs

- New Thermal Structures
- Photon Detection



Integrated Multi-function Detector with Integral Processing

- Spectrally Adaptive FPAs
- Two-Level 3-D Stack at the Detector

Technology Enablers Bridging the Gap to New Capability

Integrated Multiple spectral bands

Decision making at the sensors

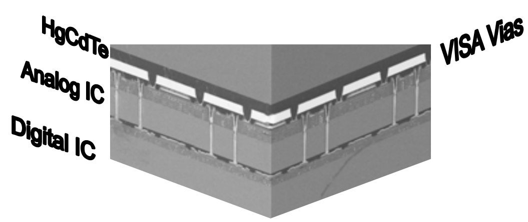
High density 3D Interconnections

Noiseless gain at the detector

New Capability

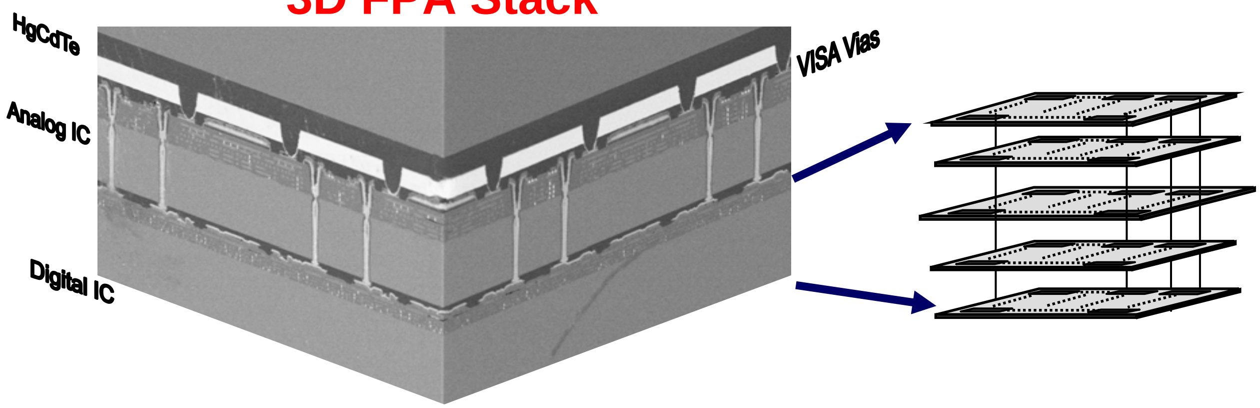
- Autonomous vehicles with intelligent sensing
- Sensors for micro/nano vehicles
- Panoramic multi-spectral
- Imaging in all-environments
- De-graded visibility imaging

3D Sensor Signal Processing



Three-Dimensional Infrared Focal Plane Array

3D FPA Stack



Combines Digital / Analog Technologies at the FPA

VISA Program will demonstrate signal processing at each pixel

Potential for Multi-level "Smart" FPA

Two-level Stack

- High Dynamic Range > 20 bits
- High Operating Temperature
- Increased Integration Time
- Higher Performance Two-Color Detectors

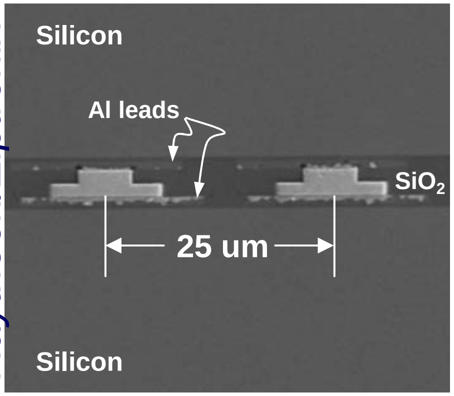
New Capabilities with Multi-level FPA

- Smart Spectral Processing
- FPAs adaptive to the environment
- On-chip Decision Making

The Next Generation FPA
Three-Dimensional Architecture

3D Silicon Read-out Integrated Circuits

Raytheon/Ziptronix



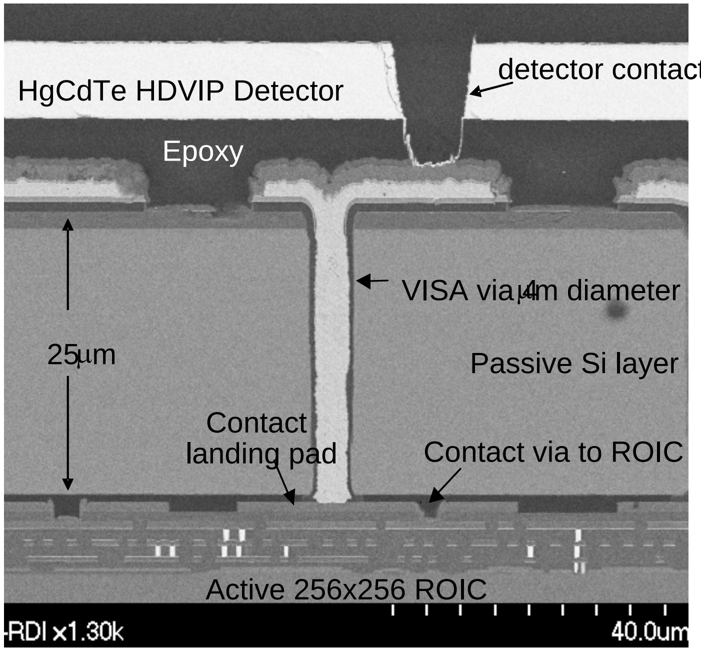
Direct Silicon Bonding

Results:

- **2 Layer Chain:**
- **1 Silicon (7μm)**
- **1 ROIC**
- **(10^6 vias; 8μc-c)**

99.998% Operability

DRS/RTI



Thin Epoxy Bond

Results:

- **2 Layer Stack:**
- **1 Silicon (20μm)**
- **1 ROIC**

  (256x256; 30μc-c)

99.98% Operability

The Next Challenges

- Higher Density Vias – < 1 um
- Multiple Wafer Stacks
- FPA 3D Architecture

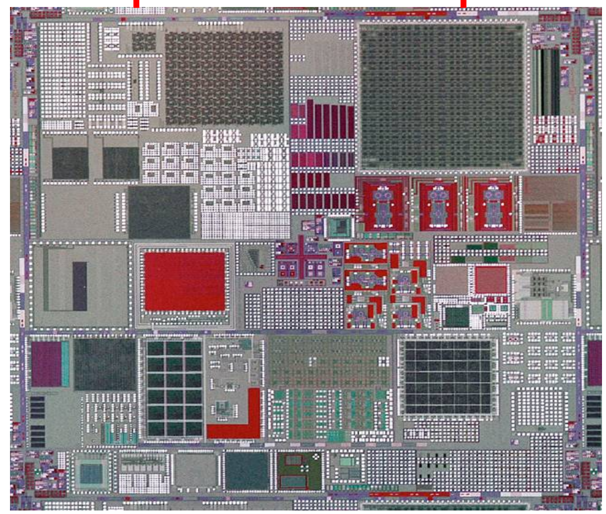
High interconnect operability Achieved between Silicon and FPA ROIC / Verified with Imaging from Analog Chip

Three Dimensional Multi-Project Run
Lincoln Laboratory

Wide Range of 3D Circuit Designs Completed in First Multi-project Run

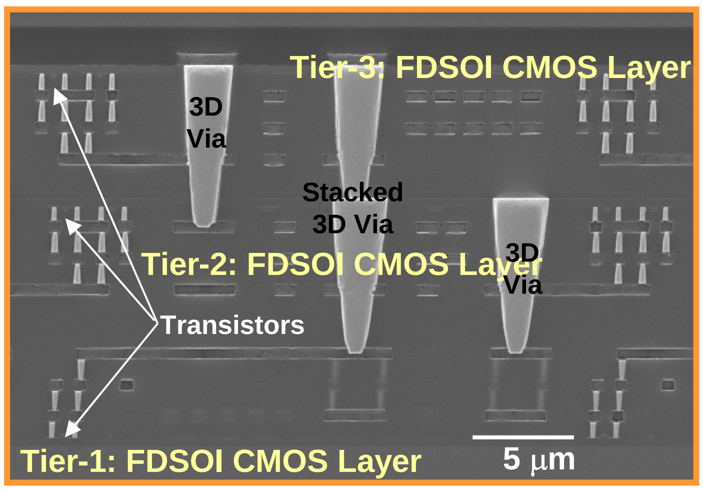
- 3D FPGAs, digital, and digital/mixed-signal/RF ASICs exploiting parallelism of 3D-interconnects
- 3D analog continuous-time processor
- 3D-integrated S-band digital beam former
- Stacked memory (SRAM, Flash, and CAM)
- Self-powered CMOS logic (scavenging)
- Integrated 3D Nano-radio and RF tags
- Intelligent 3D-interconnect evaluation circuits
- DC and RF-coupled interconnect devices
- Low Power Multi-gigabit 3D data links
- Noise coupling/cross-talk test structures and circuits
- Thermal 3D test structures and circuits

Completed 3DL1 die photo



22 mm

3D Ring Oscillator Cross-Sectional

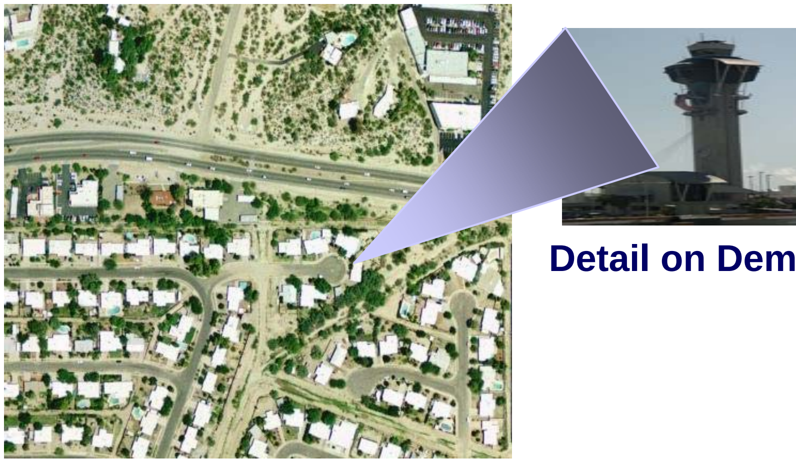


Three Level Silicon Stack using Silicon On Insulator (SOI)

- Functional 3-tier, 3D-integrated ring oscillator
  - Uses all three active transistor layers, 10 levels of metal and experimental stacked 3D-vias
  - Demonstrates viability of 3D integration process

Advanced Imaging Applications
Large Continuous Data Streams

From ChartTiff Urban Area Aerials

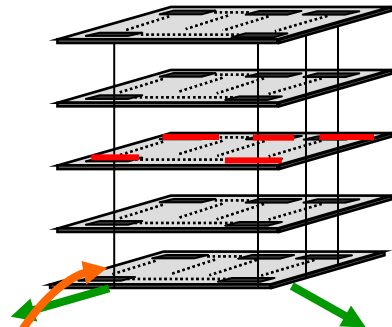


Detail on Demand

Imaging Arrays for Large Area Surveillance

Day Night Persistent Surveillance

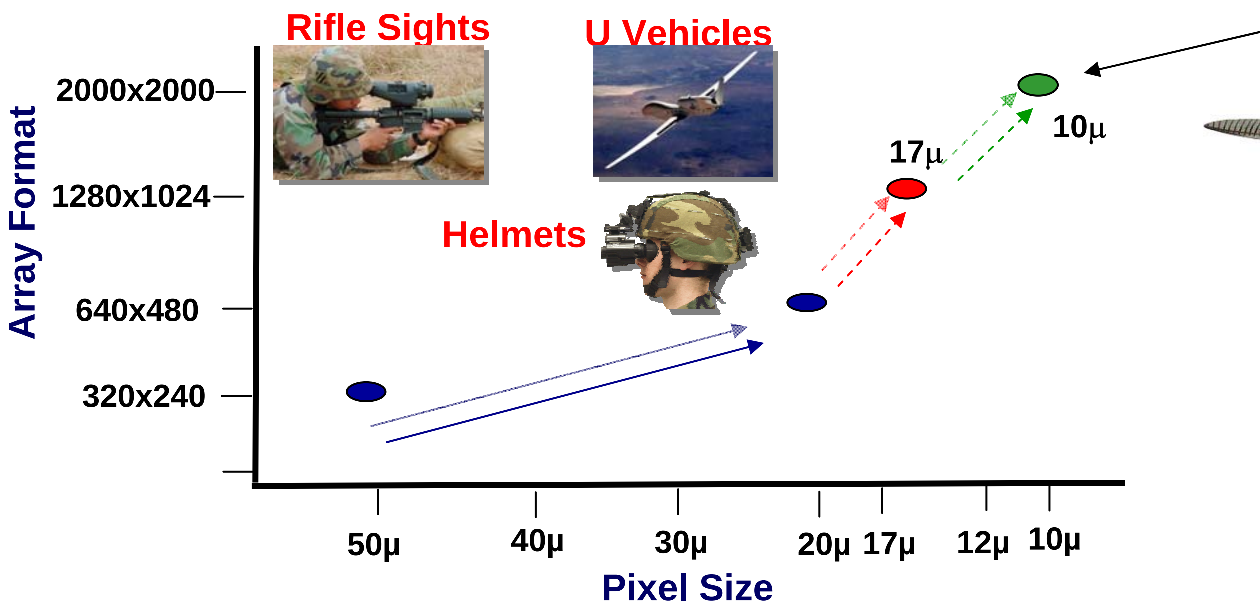
Issues:



Sensor Pre-Processing

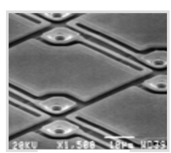
- Change Detection
- Feature / Edge Extraction
- Adaptive Spatial Filters
- Preliminary Decision Making
- Thermal Management / Heat Extraction

Room Temperature Infrared

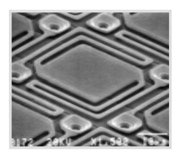


HDTV IR:

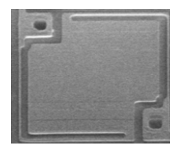
- Multiple Bands
- Electronic Processing at the Sensor



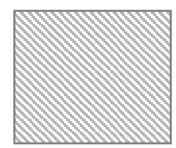
50μ



20μm pixel



17μm pixel

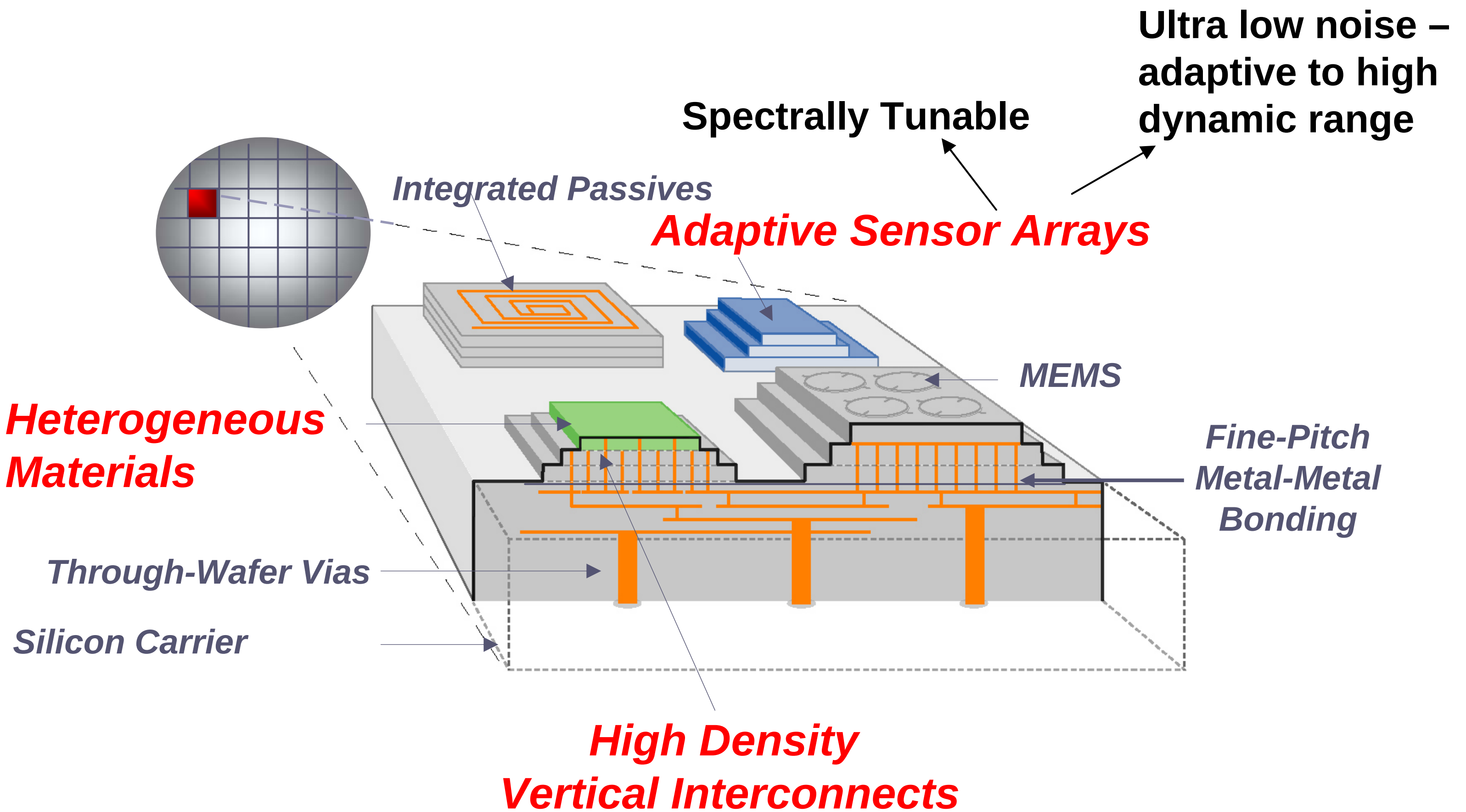


λ-detection

High Density Array Formats Lead to New Capabilities:

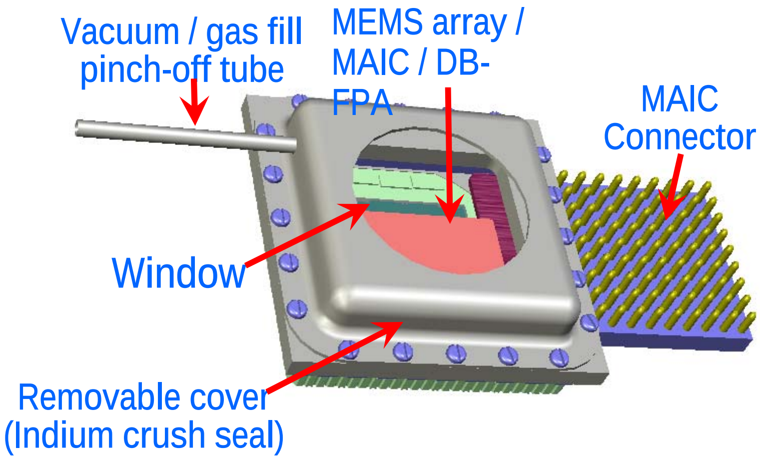
- Micro Sensors- Reduced Weight, Smaller Optics, Size &Volume
- High Definition Arrays
- Increased Range

Sensor on a Chip Concept

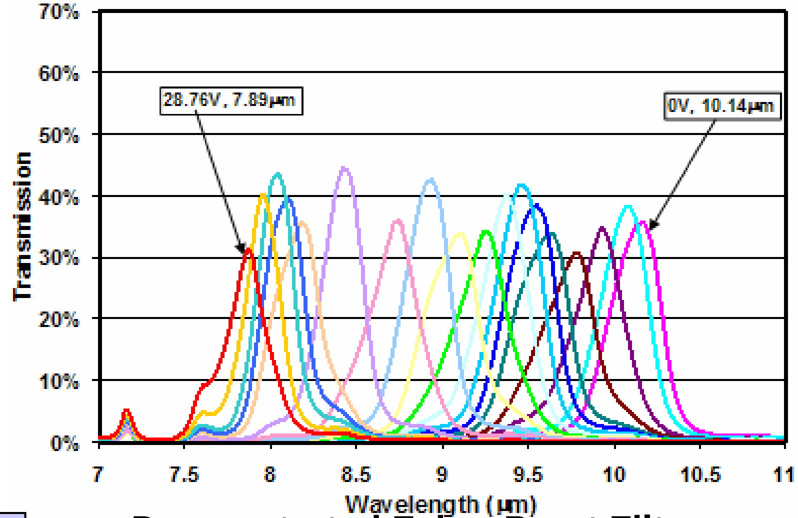


Adapted from Sensor Integration Concept RTI / DRS IR Technologies

Spectrally Adaptive Focal Plane Array



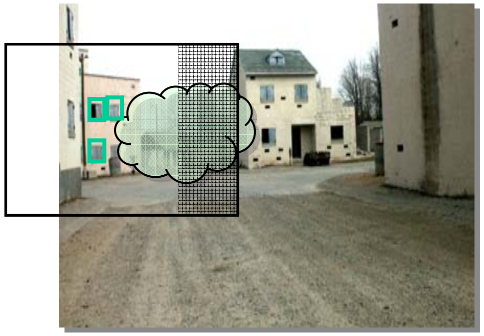
Prototype Integrated Tunable FPA Planned in FY 07



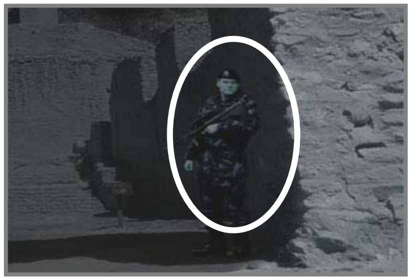
Demonstrated Fabry Perot Filters Tunable from 8 – 10 um

- **Future tunable FPAs will:**
- **Adapt to the environment**
- **Autonomously detect anomalies**
- **Select spectral band to optimize contrast**
- **Analyze scene content**
- **New Ideas ?**

Chemical Detection



Low Contrast LWIR



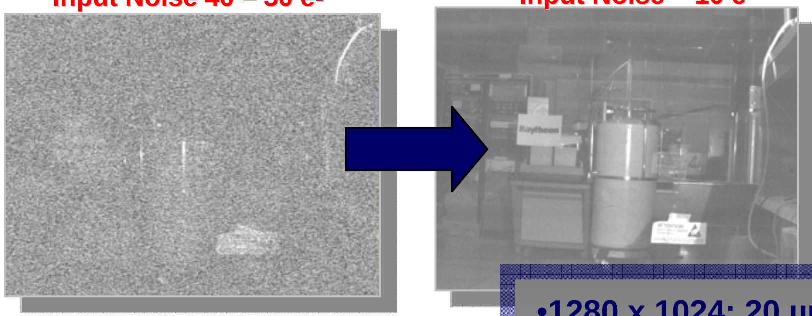
Camouflage SWIR

Noiseless Room Temperature FPA

Raytheon

State of the Art SWIR Camera
Input Noise 40 – 50 e-

High Gain Input Circuit
Input Noise ~ 10 e-

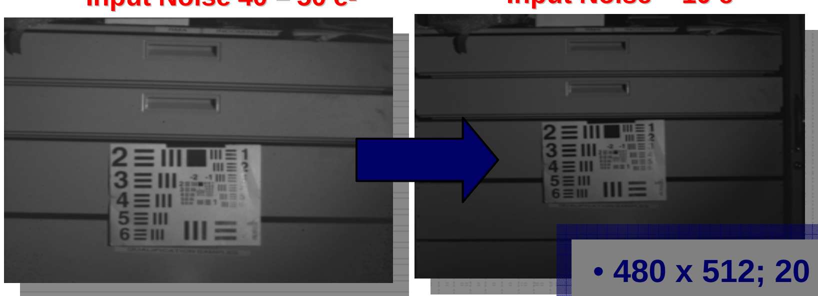


- 1280 x 1024; 20 µm pixels
- Short Integration 1.8 msec.
- F/13 Optics
- Temperature -18 C

Goodrich – Sensors Unlimited

State of the Art SWIR Camera
Input Noise 40 – 50 e-

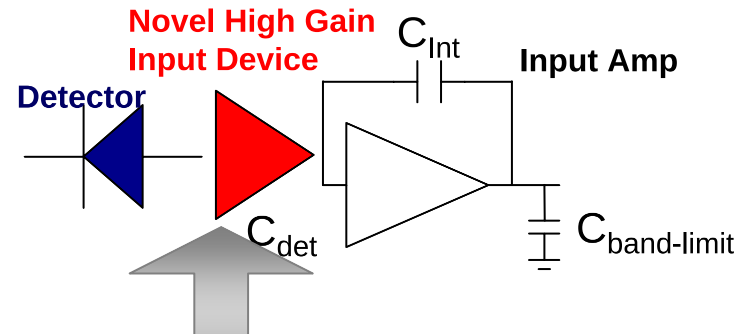
High Gain Input Circuit
Input Noise ~ 10 e-



- 480 x 512; 20 µm pixels
- Integration Time: 16 msec
- F/2.8 Optics
- Temperature +18°C

Demonstration of Low Read-out Noise SWIR

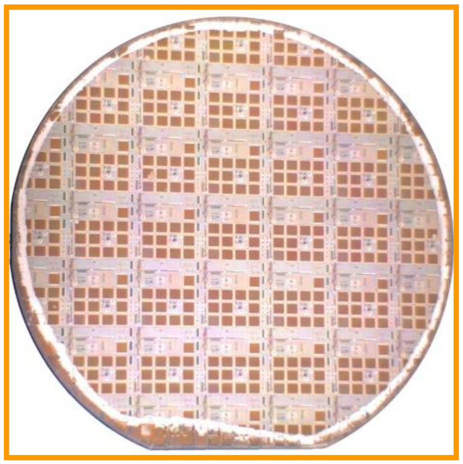
Improvements in Imaging with Low Noise Input SWIR 20 µm unit cell



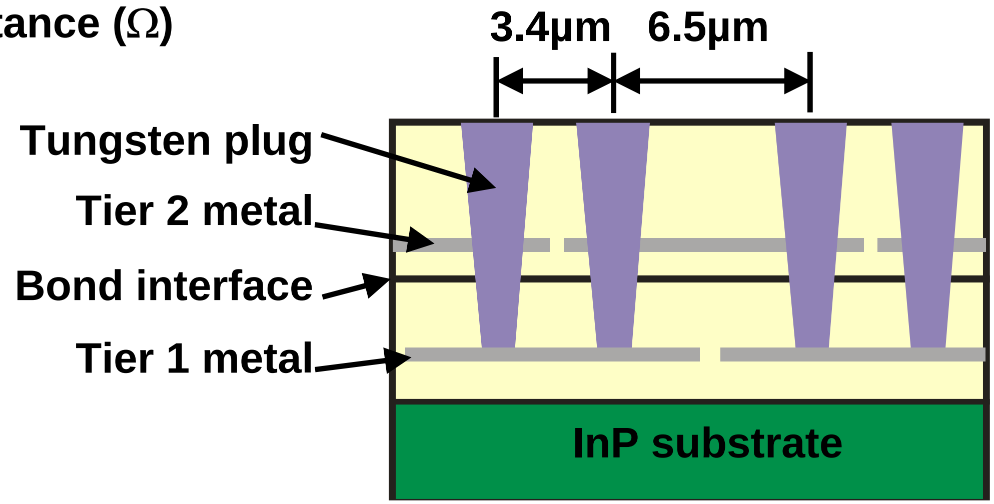
- High Gain / Low (zero) Excess Noise
- Uniformity in Large Arrays
- Unit cell ~ λ
- High Dynamic Range
- Adaptable to high Illumination

Wafer Bonding Heterogeneous Materials

Wafer Die Map of Average 3D-Via Resistance (Ω) for 10,000-via Chains < 1 ohm



Photograph of 150-mm InP Wafer with Aligned and Bonded Tier



Lincoln Laboratory:

First Steps toward Heterogeneous Integration of Imaging Materials

Wafer Level Integration Photonic Materials with Silicon:

- Narrow band detectors integrated with state of the art CMOS processing
- Extremely large arrays – potentially wafer level
- Higher density, smaller size pixels

Summary

- **Three dimensional FPAs and signal processors provide the basis for future imaging technology**
- **First steps taken through development of high operability interconnections, new ideas needed for:**
  - ❖ High density vias
  - ❖ Architecture
  - ❖ Heat extraction
- **Room temperature imaging has advanced significantly, but future advances needed in:**
  - ❖ Single electron noise
  - ❖ Broad-band Imaging
- **Demonstration of hyper / multi-spectral imaging at the sensor provides first steps toward FPAs that interaction / adapt to the environment**
- **Sensor system-on-a-chip concepts bring together information from multiple sensor modes**