Future of Power Efficient Processing

MTO
DARPA
MICROSYSTEMS TECHNOLOGY OFFICE

Dr. Michael Fritze
Microsystems Technology Symposium
San Jose, CA
March 5-7, 2007

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE **06 MAR 2007**

2. REPORT TYPE **N/A**

3. DATES COVERED **-**

4. TITLE AND SUBTITLE **Future of Power Efficient Processing**

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **DARPA**

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR’S ACRONYM(S)

11. SPONSOR/MONITOR’S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT **Approved for public release, distribution unlimited**

13. SUPPLEMENTARY NOTES **DARPA Microsystems Technology Symposium held in San Jose, California on March 5-7, 2007. Presentations, The original document contains color images.**

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT **unclassified**	b. ABSTRACT **unclassified**	c. THIS PAGE **unclassified**	**UU**	**12**	

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std Z39-18

Power Efficient Electronics are Critical to Many DoD Missions

Soldiers carry packs in 70-120 lbs range
Frequently 10-20 lbs are batteries!

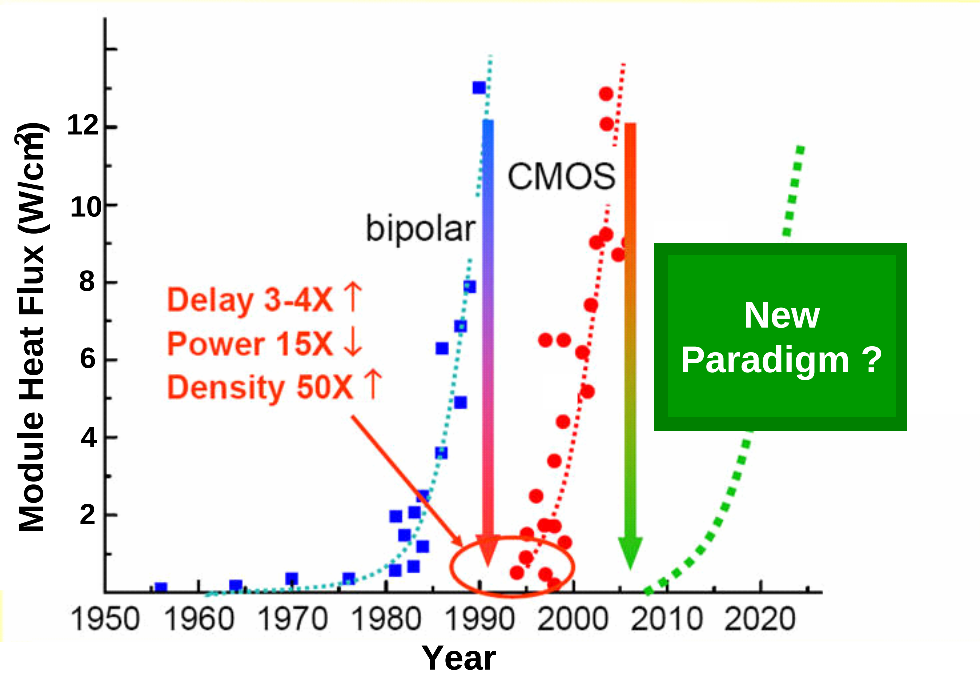
Power is frequently scarce and expensive: UAVs, remote sensor networks, space, etc.

DSRC Summer 2006
Low Power Workshop

Getting rid of dissipated heat
is often a major problem by itself!

Heat pipes

Electronics History:
Power Efficiency Perspective



Power = Dynamic + Static

$$= 0.5CV_{dd}^2f + I_{leak}V_{dd}$$

Ultimate Goals:

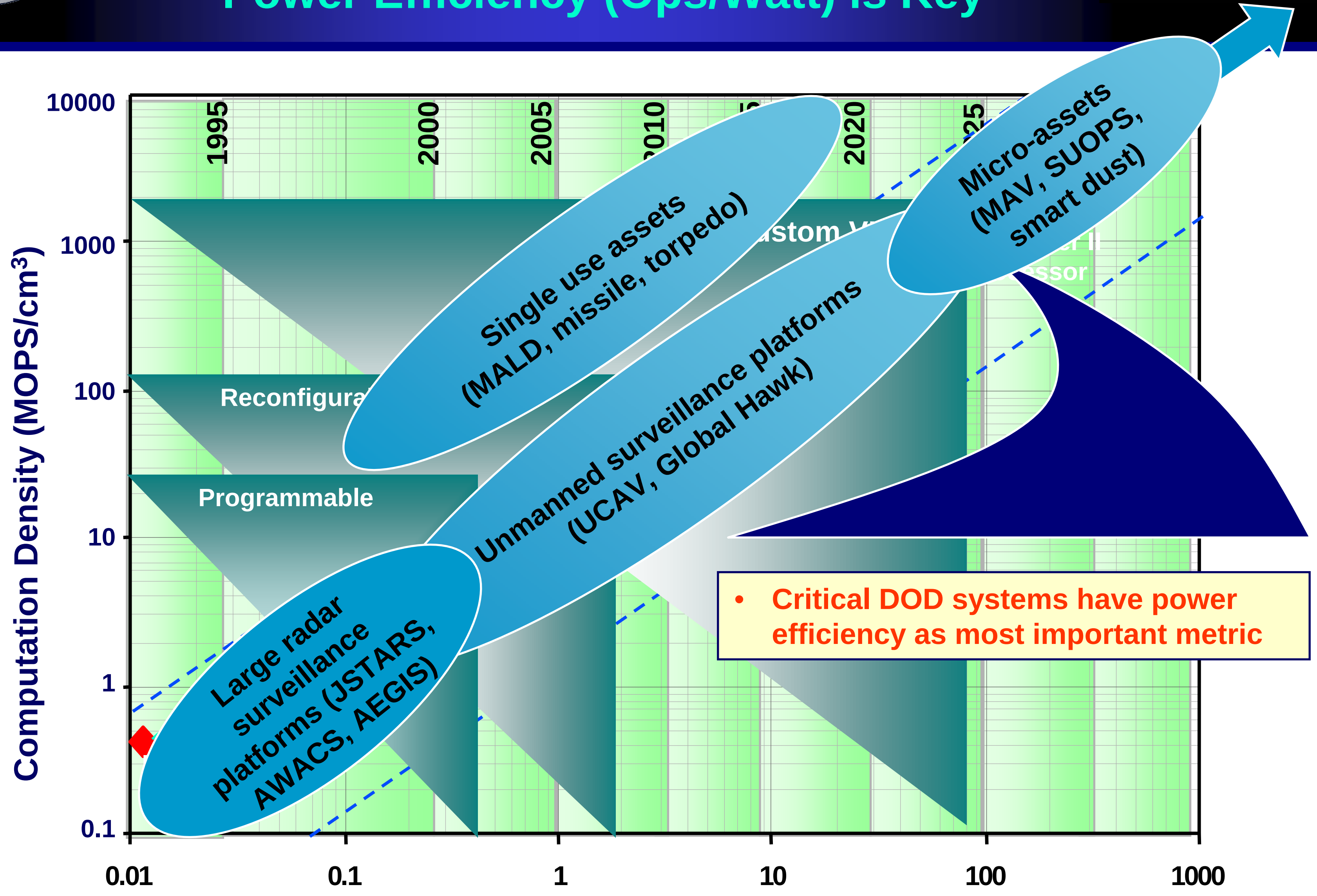
Decades power reduction
No performance penalty

- ***Each technology ultimately reaches integration density limited by power dissipation***
- ***Quantum jump then occurs to new technology with lower power***

Time for the next paradigm change ?

Embedded Computing for DoD

Power Efficiency (Ops/Watt) is Key



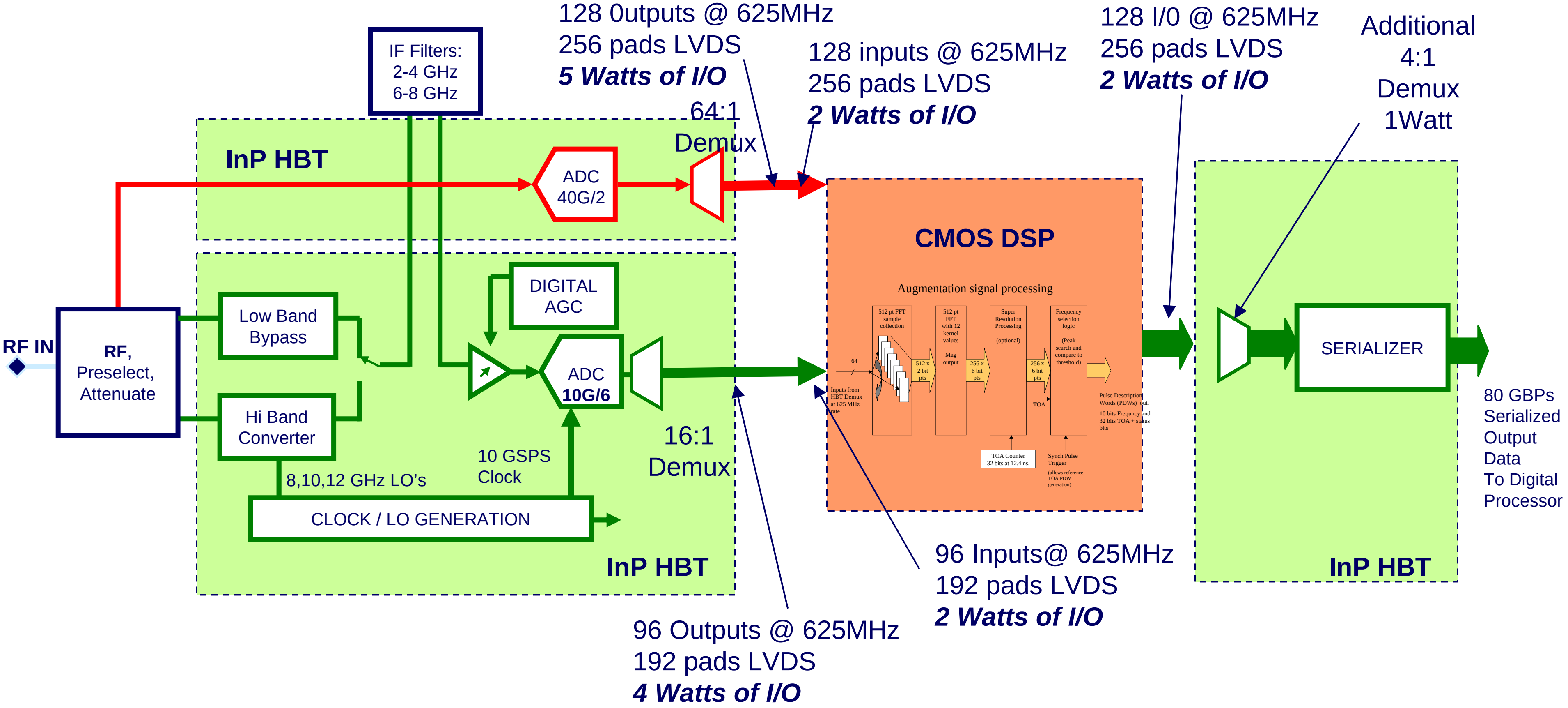
- Critical DOD systems have power efficiency as most important metric

J. Anderson, MITLL Gp 102
HPEC Conference '04-'05

Some Paths Forward:
Power Efficiency

- I) Densely integrated RF technology
  - RF SOC vs MCM implementation
  - ‘TEAM’
- II) Novel Architecture/Design
  - Power management
  - Sub-threshold , Parallelism, 3D
  - ‘ESE’, ‘3D-IC’
- III) Ultra-low power CMOS
  - Tunable threshold
  - Steeper sub-threshold slope (< 62 mV/dec)
  - ‘STEEP’ BAA coming out
- IV) Beyond Silicon
  - Carbon electronics
  - Graphene, Nanotubes
    - Workshop in early April

Power Benefits of Integration: RF-SOC vs. MCM



128 0utputs @ 625MHz
256 pads LVDS
5 Watts of I/O

128 inputs @ 625MHz
256 pads LVDS
2 Watts of I/O

128 I/0 @ 625MHz
256 pads LVDS
2 Watts of I/O

Additional
4:1
Demux
1Watt

80 GBPs
Serialized
Output
Data
To Digital
Processor

96 Inputs@ 625MHz
192 pads LVDS
2 Watts of I/O

96 Outputs @ 625MHz
192 pads LVDS
4 Watts of I/O

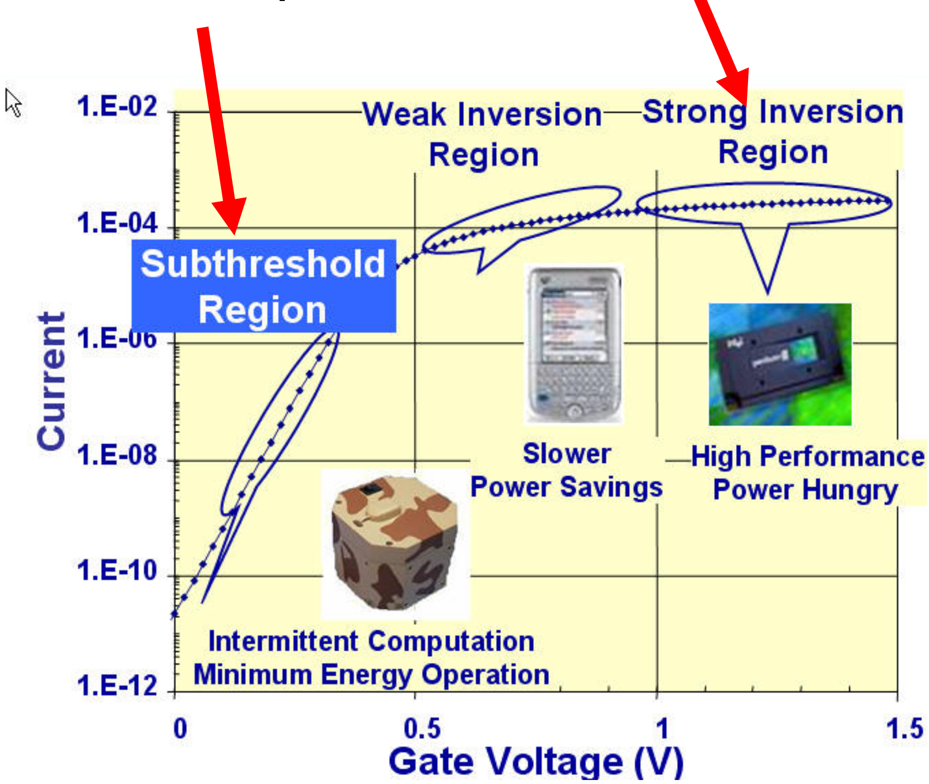
All four ICs can be implemented in a single SiGe IC

… 16 Watts of additional power due to intra-chip I/O in multi-chip approach over a monolithic implementation

Sub-threshold Digital Design:
Energy Starved Electronics (ESE) Program

Slower, low power

Fast, high power



- **<u>Goal</u>: Enable ultra-low power digital circuits operating in the *sub-threshold regime* while maintaining adequate performance. Energy consumption savings > 10X.**

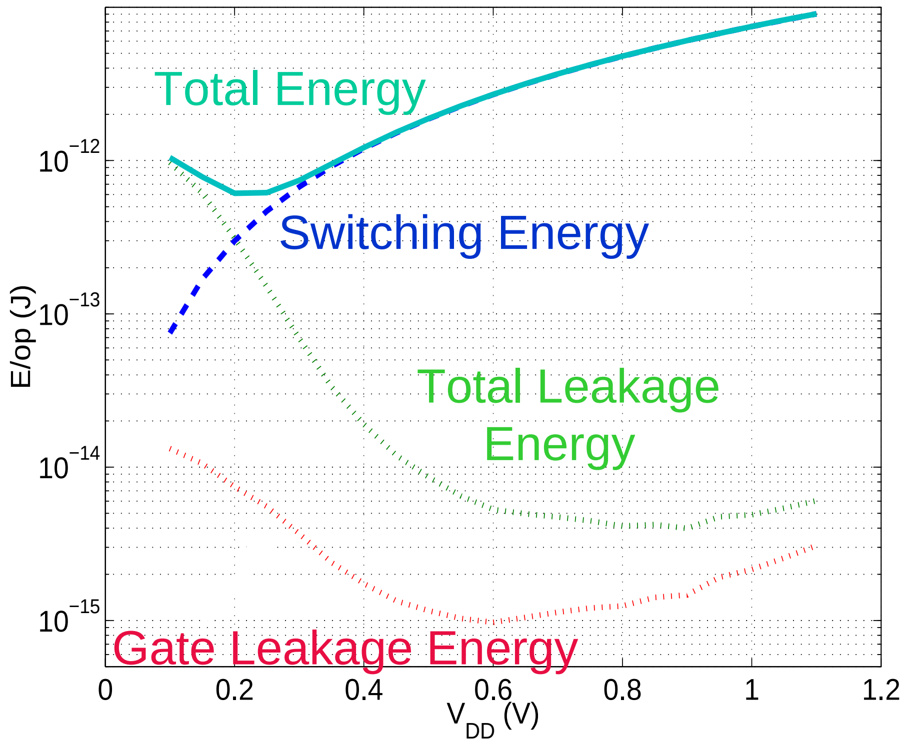
- **<u>Technical Challenges</u>:**
  - **Develop standard cells operating at V_{dd} < 300 mV; esp. SRAM**
  - **Achieving adequate performance (through parallelism)**
  - **Addressing high sensitivity to variations (via ECC)**

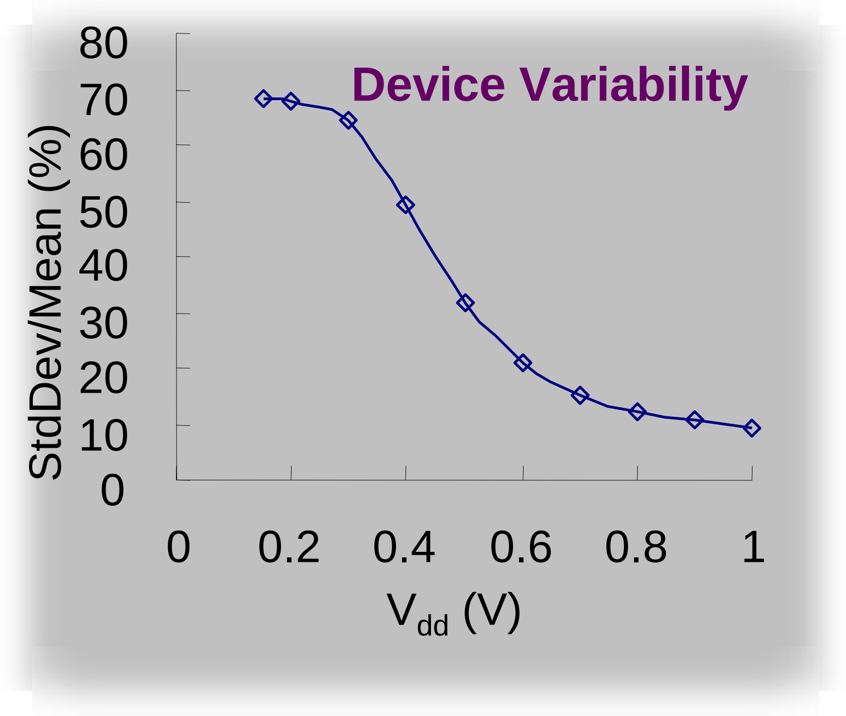
- **<u>Design Only Approach</u>:**
  - **No device technology changes**
  - **Exploits massive investment by industry for DoD benefit**

PI: Prof. Anantha Chandrakasan, MIT
Fab: TI, Dr. Dennis Buss, 65-nm CMOS

Minimum Energy Point:

Switching vs. Leakage





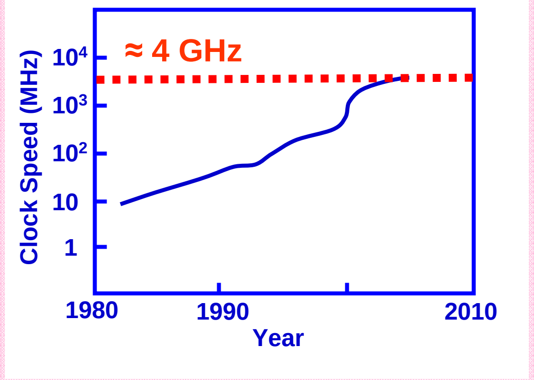
- **Minimum energy point ≈ 200 mV (sub-threshold regime)**
  - **Must be compensated for (e.g., parallelism and threshold control)**
  - **Optimum voltage V_{dd} varies with circuit activity**

- **Leakage energy increases at extremely low voltages (long delay times)**
- **Increased variability requires wider margins, reduced performance**

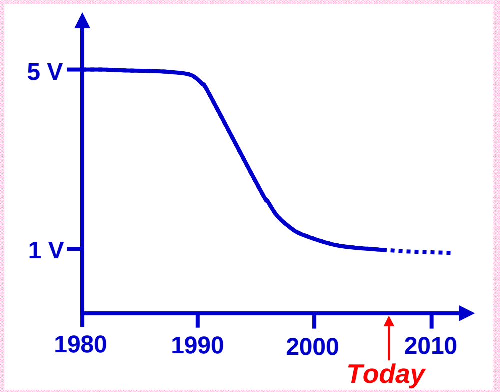
Steep-subthreshold-slope Transistors for Electronics with Extremely-low Power (STEEP)

Problem: Device Scaling alone will no longer meet DoD needs!

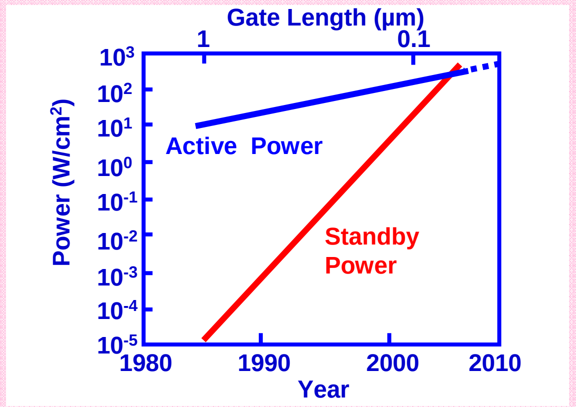
Processor speed stalled



Supply voltage stalled

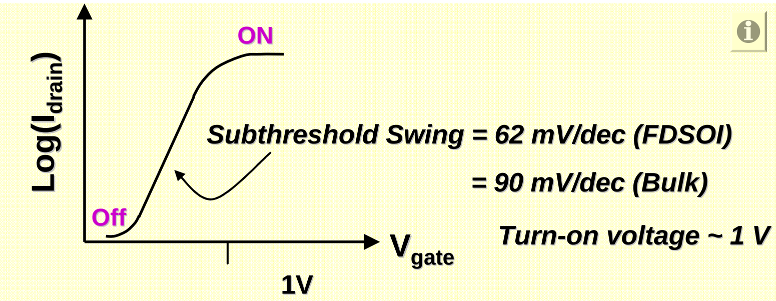


Large leakage current increase



Proposed Solution: Steep-subthreshold-slope Transistors

Today



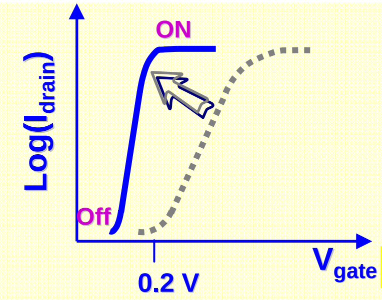
Subthreshold Swing = 62 mV/dec (FDSOI)

= 90 mV/dec (Bulk)

Turn-on voltage ~ 1 V

Theoretical minimum of the subthreshold swing of MOSFET is ln10(kT/q) or 60 mV/dec

STEEP Vision

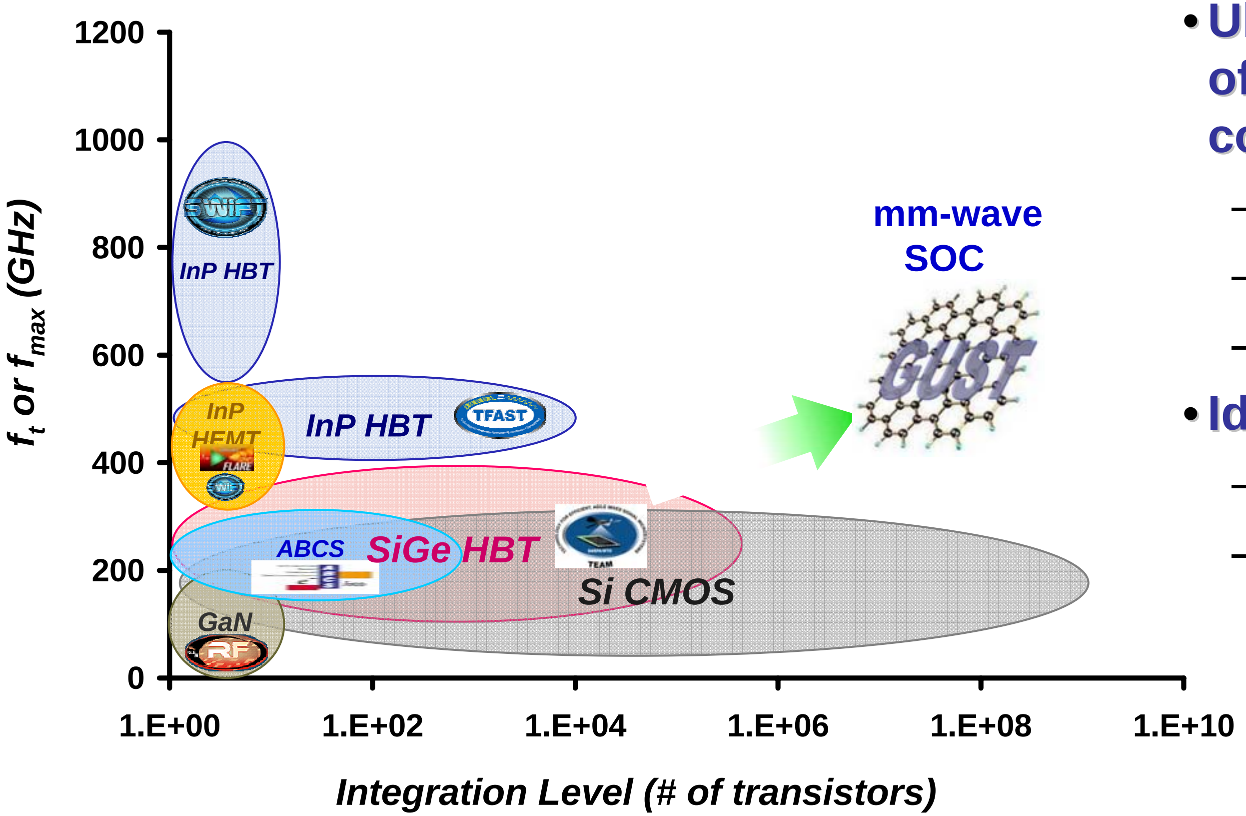


Program Goals

- *Subthreshold Swing ≤ 20 mV/dec*
- *Turn-on voltage: ≤ 0.2 V*
- *5X lower V_{DD}*
- *100X lower $P_{standby}$*
- *25X lower P_{active}*
- *No performance penalty!*

Develop ideal transistor switch for ultra-low power electronics

Carbon Electronics:
High Performance & Integration for RF-SOC’s

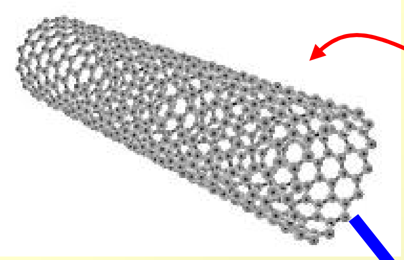


- **Ultimate performance limits of mm-wave devices (radar, comms, etc):**
  - ***Higher speeds***
  - ***Improved power efficiency***
  - ***Lower “SWAP”***
- **Ideal mm-wave device**
  - ***Key parameters***
  - ***Integration path with Si***

New Opportunity: Carbon-based mm-wave SOC’s

New Approach For Ideal mm-wave Material: Planar Carbon (Graphene)

Carbon Nanotube

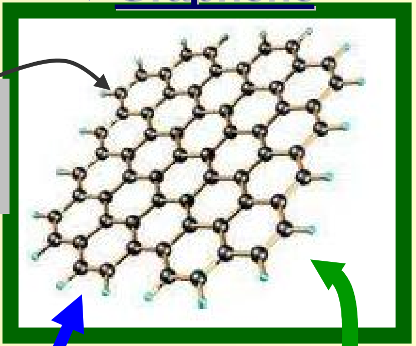


Challenges:

Placement & Uniformity

unroll

Graphene

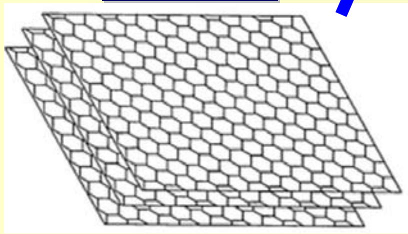


Planar system

sp^2 hexagonal
a=0.25nm, c=0.67nm
2D physics

"scrape"

Graphite



Planar form has most of the desirable properties of nanotubes

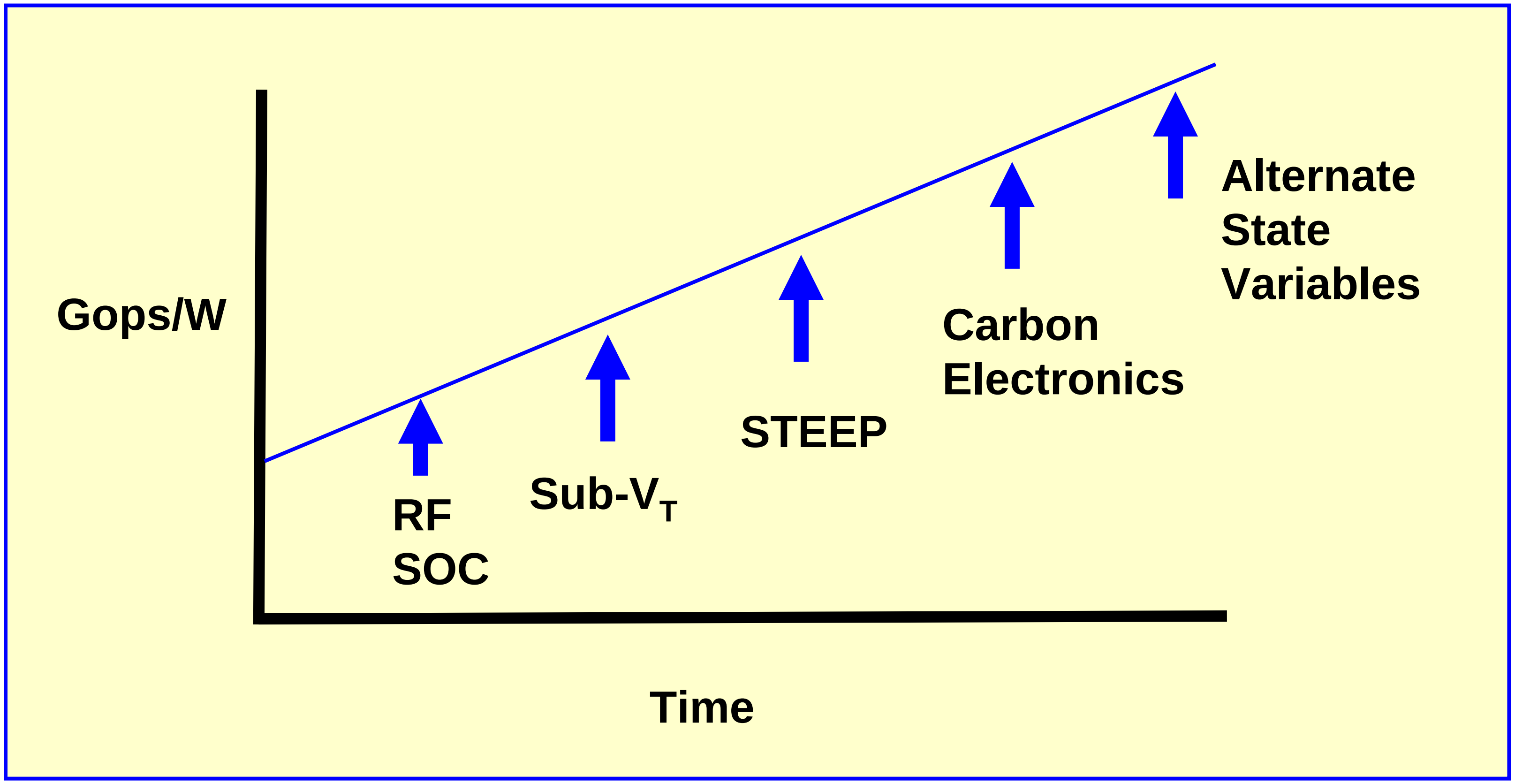
Graphene Properties:

- High mobilities for both ***electron & hole*** (> 10X silicon)
  - *$\mu \geq 15{,}000$ cm^2/Vs, $m^* = 0.06m_0$*
  - *mm-wave & low power potential*
  - *High current density*
- Ideal electrostatics ("monolayer-on-insulator")
  - *Sub-nm thickness*
    - *< Debye screening length*
  - *Enables aggressive scaling*
- Planar processing can be used
  - *Standard paradigm*
  - *Straightforward integration with CMOS*

Semimetal band structure
  - *I_{on}/I_{off} ~ 30, useful for RF devices*

Graphene is very promising material for mm-wave RF-SOC technology

A Possible Path Forward



Gops/W

RF
SOC

Sub-V_T

STEEP

Carbon
Electronics

Alternate
State
Variables

Time