

# The Integration of Molecular Electronic Devices with Traditional CMOS Technologies

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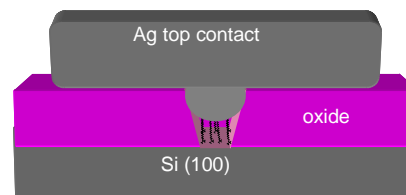
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**Abstract**-This work describes the development of hybrid circuits composed of silicon-based molecular electronic devices and traditional CMOS technology. In the development of these circuits, we first fabricated individual CMOS-compatible molecular electronic devices and established their effectiveness. We then designed and used traditional VLSI tools to layout a hybrid circuit that includes CMOS for the on-chip characterization of the molecular devices, as well as a platform composed of the contacts and interconnects for the molecular electronic devices. Finally, we developed the procedures for the post-processing fabrication of the molecular electronic devices based on CMOS-compatible techniques. This work is an important step towards the realization of hybrid molecular/traditional circuits. It both advances novel “beyond CMOS” molecular electronic technology, and enables hybrid circuits for the on-chip characterization of the molecular electronic devices via CMOS instrumentation.

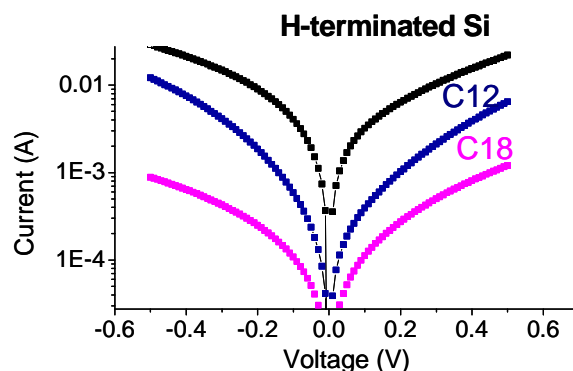
## I. INTRODUCTION

We have successfully fabricated and electrically characterized molecular electronic devices with CMOS integration potential and then developed the design and procedures for the integration of these devices with CMOS by using traditional VLSI layout tools and CMOS fabrication techniques. The hybrid molecular device/CMOS chips were designed not only to show that such integration is possible, but also to enable the on-chip characterization of the molecular devices by using CMOS circuitry. These developments are critical to the realization of molecular electronics, a field based on using organic molecules with functional electrical properties in devices.

The field of molecular electronics has been focused on the characterization of electron transport through molecular monolayers, much of which has been performed by using methodologies and materials that are not compatible with conventional integrated circuit technologies. For example, much of the work thus far has used gold as a bottom substrate material due to the ease and reliability of self-assembly of organic monolayers on gold [1-10]; however, gold is not compatible with traditional silicon (Si) technologies due to its propensity to form energy traps in Si. Also, because evaporated metal device top contacts have been shown to degrade and/or displace molecular monolayers in junctions [11,12], characterization techniques have mostly consisted of indirect contacts (such as STM probes) or devices that rely on “soft” top contacts (mercury drops, carbon nanotubes, or



(a)



(b)

Fig. 1. (a) Cross section of the molecular electronic device, (b) Representative current-voltage (I-V) curve results for the molecular electronic devices. In these I-V curves the longer chained molecules assembled in the device were less conductive than the shorter chained molecules, demonstrating the effectiveness of the molecular electronic device.

electrolytes) [13-15]. Since the electrical behavior of the molecular monolayer is extremely dependent on the materials and characterization methodology used, it is essential for groups to begin to characterize monolayers in devices that have increased technological potential. Because it is also likely that the first step to the realization of molecular electronic devices will be the integration of molecular electronics with existing technologies to form hybrid molecular electronic/CMOS circuits, it is imperative to begin designing and fabricating CMOS-compatible molecular electronic devices and hybrid circuits.

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## II. THE FABRICATION AND CHARACTERIZATION OF CMOS-COMPATIBLE MOLECULAR DEVICES

The first step in the realization of the hybrid circuit with on-chip characterization potential was the fabrication and characterization of CMOS-compatible molecular electronic devices. Fig. 1(a) shows an enclosed molecular electronic device with a “hard” Ag top contact. We avoided displacing the molecular monolayer during the top metal evaporation by using Ag, which has been shown not to displace the molecular monolayer in the junction, as the top contact material [11]. The bottom contact was highly doped Si (100), due to its compatibility with CMOS. Because prior to this work most of the monolayer assembly/characterization that had been performed was on Si (111) [16-23], we performed extensive characterization to ensure that the monolayers assembled on Si (100) were comparable in quality to those assembled on Si (111) [24]. Additionally, prior work by our group was performed with a lightly doped Si substrate [16]; however, we have switched to highly (degenerately) doped Si in order to ensure that the electrical characteristics observed from the devices are dominated by inherent molecular properties, rather than depletion in the substrate due to the work function mismatch between the lightly doped bottom Si contact and the Ag top contact [24-25].

In order to characterize the degenerately doped Si (100) molecular device (fig. 1 (a)), we applied a bias across the top and bottom contacts and measured the current through the junction. We performed these measurements on devices with various chainlengths of organic molecules self-assembled in the junctions [24]. Because the method of transport through alkanethiol molecules has been found to be quantum mechanical tunneling, one would expect longer molecules to have a longer tunneling barrier and thus, devices with longer molecules assembled to exhibit less current. The current vs. voltage curves from the devices with no organic monolayer (hydrogen terminated Si), with octadecanethiols (molecules 18 carbons long), and with dodecanethiols (molecules 12 carbons long) are shown in Fig. 1(b). Our experimental results confirm an inverse dependence of device current on molecular chainlength. This trend is consistent with what is expected for alkanethiols in a Si-metal junction [13], establishing that a molecular dependence is observed from the devices; i.e. they are effective.

## III. HYBRID CHIP PLATFORM DESIGN

Once the electrical characteristics of the devices were established, hybrid Si-molecular circuitry was designed. Part of the concept of the design was that first, the CMOS components plus the contacts and interconnects for the molecular device would be fabricated on-chip; then, via post-CMOS/interconnect processing, the active components of the molecular electronic devices would be fabricated on-chip.

A schematic of the basic hybrid chip layout, including the contact and interconnect platform for the fabrication of

molecular electronic devices, is shown in Fig. 2(a). The platform area for the molecular electronic devices consists of a 4 x 4 array of highly doped areas, to be used as bottom contacts for the devices, connected through output interconnect to a bus to the CMOS area of the chip. The contact and interconnect fabrication was performed by using the same VLSI layout tools, representations, and fabrication techniques as are used for the fabrication of traditional CMOS and at the same time as the fabrication of the on-chip CMOS. For example, the highly doped areas were fabricated by using the same VLSI layout representation and process steps as were used for the n-type wells of the NMOS circuitry (the “active” areas).

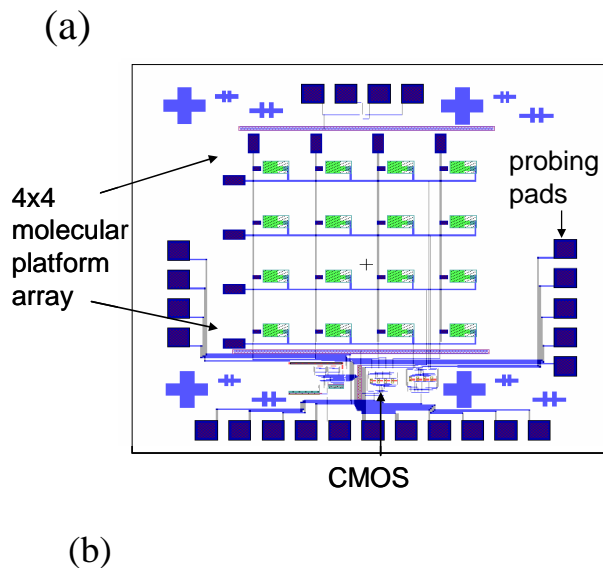
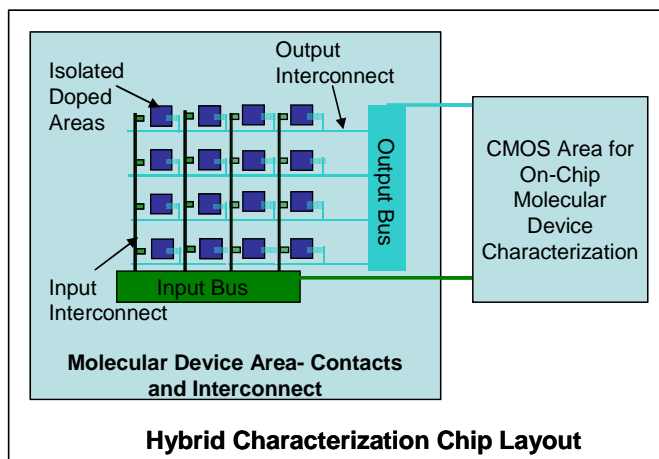


Fig. 2. (a) A schematic overview showing the layout of the hybrid chip including the area for CMOS and the area for the interconnects and contacts (platform) of the molecular electronic devices, (b) The actual VLSI layout of the hybrid chip including the CMOS area (not clearly visible due to small size), the molecular electronic device platform, and the probing pads.

## V. ENABLING ON-CHIP CHARACTERIZATION

The final VLSI layout for the chip is shown in Fig. 2 (b). The on-chip CMOS circuitry is not easily identifiable in the design, due to the relative scale of the molecular electronic device platform relative to the CMOS. The CMOS circuitry design and layout were simulated and checked for functionality prior to fabrication. The VLSI layout was used for the fabrication of the entire chip, including the molecular electronic device platform, using traditional CMOS techniques.

## IV. POST-CMOS PROCESSING INTEGRATION OF MOLECULAR ELECTRONIC DEVICES

After the CMOS and the molecular device platform (contacts and interconnects as shown in Fig. 2 (a)) are fabricated on-chip with traditional CMOS tools and methodologies, the integration of the molecular electronic devices is completed by using post-processing techniques. The top and side views of a completed molecular electronic device are shown in Fig. 3 [16]. The molecular electronic devices are fabricated by first etching through the oxide covering the embedded highly doped “contact areas” using standard photolithography or e-beam lithography wet etching, or dry etching methods. After etching, UV-assembly techniques (as described in Section II) are used to assemble the molecular monolayer. Finally, the top Ag contact is formed by using an evaporation mask that aligns with the bottom contact areas and the input interconnects to “wire-up” the molecular junction to the rest of the circuitry. Alternatively, this top contact could be fabricated by using a standard photolithography method with chemical or physical etching, or with a “liftoff” procedure, depending on the top contact metal used. After this final top metallization, the molecular electronic device is complete.

Once the fabrication is complete, the chip is ready for verification of the CMOS and molecular components, as well as for the on-chip characterization of the molecular devices via the CMOS. The CMOS circuitry on the chip is designed to function as on-chip instrumentation for the electrical characterization of the molecular electronic devices. These on-chip characterization capabilities were accomplished by including multiplexers in the hybrid chip design between the molecular electronic and CMOS areas so that the rows and columns of the molecular electronic device array could be accessed by the CMOS instrumentation circuitry for the on-chip molecular device characterization. Additionally, in order to verify the individual electrical characteristics of each molecular electronic device, the hybrid chip includes two on-chip probing pads per device for individual off-chip characterization.

## VI. SUMMARY

This work advances the field of molecular electronics by establishing CMOS-compatible molecular electronic devices and by developing the methodologies for integrating these novel “beyond CMOS” devices with traditional CMOS technology. Future work will include the use of the hybrid chip for extensive on-chip characterization of molecular electronic devices for traditional electrical properties, as well as for properties that may be difficult to accurately measure using traditional off-chip characterization techniques. Due to the flexibility in the design of the integrated chip, the basic concepts and processes could be extended for the integration of other nanotechnologies with CMOS.

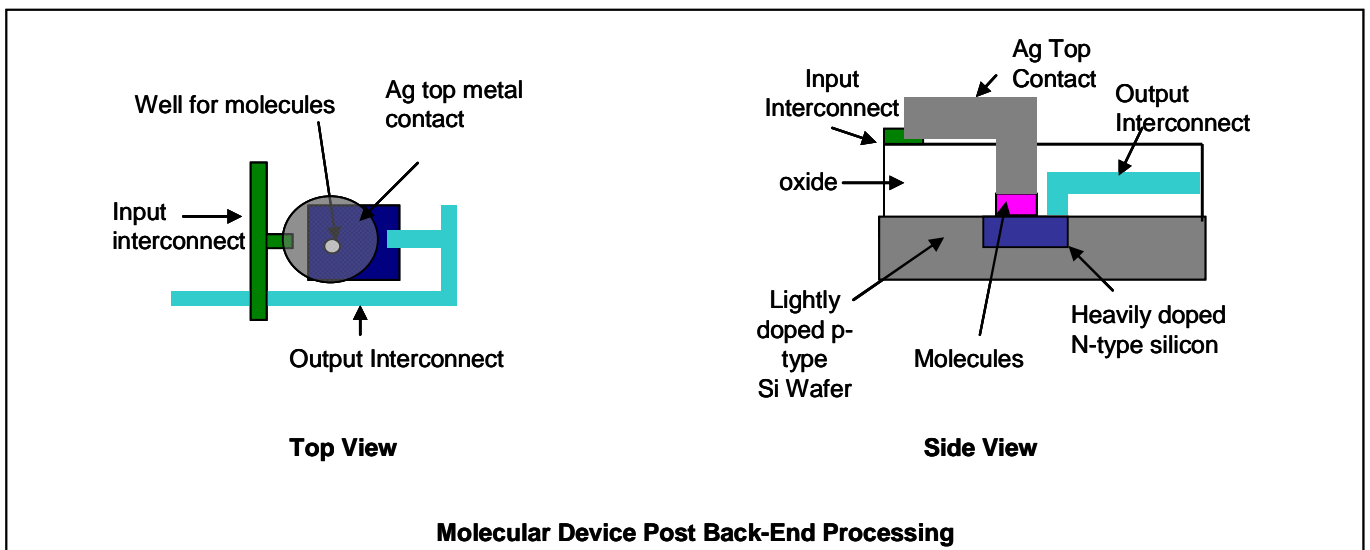


Fig. 3. The top view and side view of a complete molecular electronic device post CMOS processing. The post-processing consists of: milling a well in the oxide above the heavily doped silicon contact, using UV-assisted self-assembly to assemble the molecular monolayer in the well, and capping with a metal top contact which also connects the device to the “metal 2” CMOS interconnects [16].

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