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14. ABSTRACT

The research efforts to develop a high-efficiency, moderate power THz device are discussed. The device structure is based upon the crystalline properties of GaN and its ability to handle large power and high fields. Physical device models were developed that include thermal and electrical simulations. Several device structures were produced in conjunction with the model development. Initial negative differential conduction results from fabricated devices are presented as are the designs of co-planar resonant structures suitable for THz emission.

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Lester F. Eastman, Barbaros Aslan, Quentin Diduck

Abstract:

The research efforts to develop a high-efficiency, moderate power THz device are discussed. The device structure is based upon the crystalline properties of GaN and its ability to handle large power and high fields. Physical device models were developed that include thermal and electrical simulations. Several device structures were produced in conjunction with the model development. Initial negative differential conduction results from fabricated devices are presented as are the designs of co-planar resonant structures suitable for THz emission.

1. Underlying - Fundamentals:

Electron energy versus its wave number, in GaN, is shown in Fig.1. The electrons that are in the Γ-valley have effective mass equal to 0.2 times free space electron mass. The electrons can be ballistically accelerated in the first Brillouin zone, up to the 2.7V limit in the Γ-A direction and approximately 3.0V in the Γ-M direction.

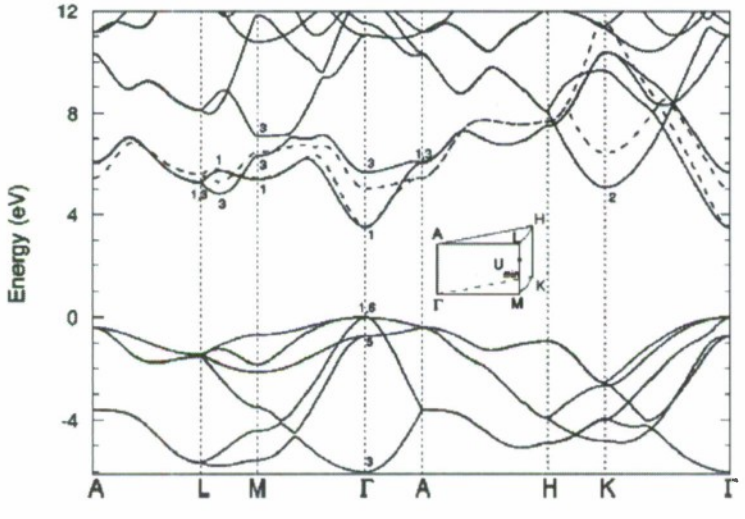


Fig. 1. Energy versus wave number diagram for GaN material

The maximum electron group velocity, seen in Fig. 2 varies with its energy, at 1 eV energy it is ~8.5×10^7cm/s in the Γ-A direction, and is 8.0×10^7cm/s in the Γ-M direction. If a 320kV/cm electric field is applied in either direction; it takes ~ 50fs to reach 1 eV energy, beyond which the electrons can begin to scatter into the upper L-Valley. Using an optical pulse probe method, Wraback [1] has formed an electron accumulation layer, just inside n-type GaN, and has measured its position during its transit

through an undoped drift region 1 micron thick. Various electric fields were applied to the device in the drift region, and the electron velocity versus time was determined.

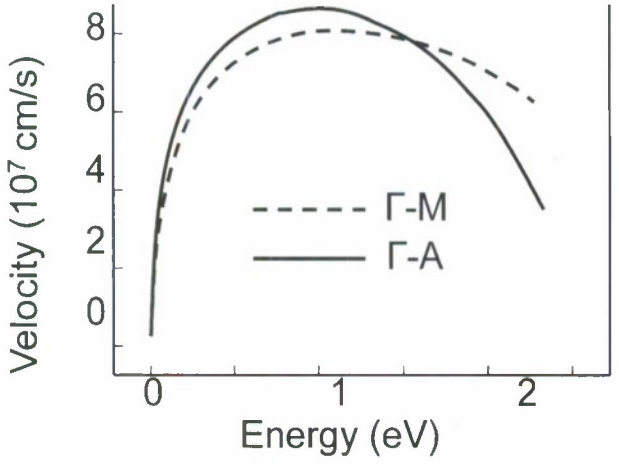


Fig. 2. Velocity of electrons versus energy in GaN material.

The average electron velocity rises at lower electric fields, less than 320,000V/cm, and falls at higher device field strengths. Thus the average induced current rises and then falls as electric field is increased in a 0.25 micron long device, as shown in Fig.3, based on Wraback's data. The negative slope condition gives rise to a negative differential conductivity, which will cause oscillations in a resonant circuit. This circuit has an inductive susceptance in parallel with the device's capacitive susceptance, yielding a desired resonant frequency. A designed load conductance is also placed in parallel with the device during simulation described below, that yielded a transit time (500fs) transit time oscillation in the terahertz frequency range.

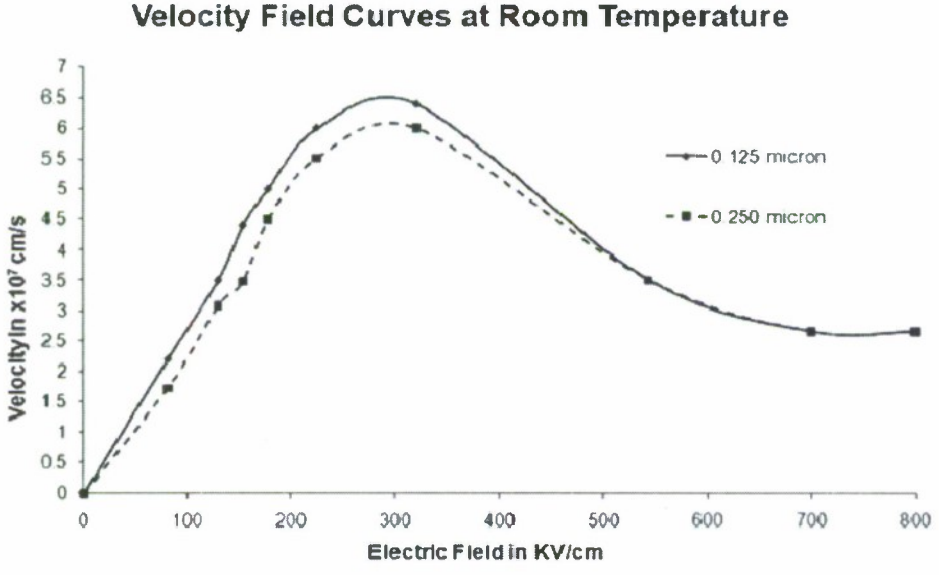


Fig. 3. Velocity Field Curve at room temperature for 0.125 micron and 0.250 micron devices based upon Wraback's [1] results

The important time transients, involved with electrons and phonons, were experimentally determined by Wu [2]. The application of those time transient data to our experiments, are represented in Fig.4. In Fig.4 time scale is coincident with the distance scale over the 500fs, .25micron drift distance.

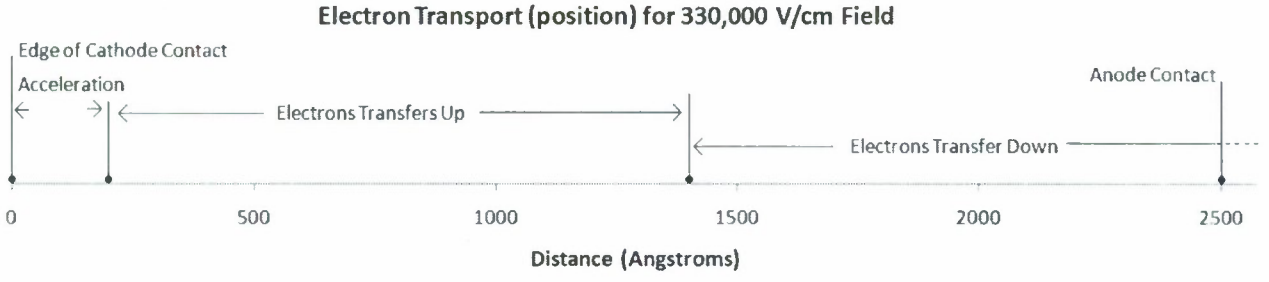


Fig. 4. Time scale of electron transport in a 0.25 micron device

We calculate the acceleration time to 1 eV energy at 320kV/s, as 50fs. Wu has determined that it takes 170fs for 1 eV electrons to transfer to the upper, L-Valley and that it takes 1,022fs for them to transfer back to the Γ-valley. Energetic electrons take 290fs to launch a longitudinal optical phonon in the Γ-valley. Based on Wraback's data, it will take 500fs for electrons to transit 0.25 microns in this electric field. The transit time will only allow one or two phonons to be launched, for each electron, in operation under bias. Thus the ballistic acceleration negative differential conductivity operation will have a limited effect from phonons scattering in the drift space. The hot electrons will lose their energy in the anode. Separate thermal probe profiles have shown that the anode is hotter than the cathode in experiments on longer drift distances, even with 0.5 micron spatial resolution for the thermal probe.

In the accumulation layer mode of operation, the fast rising electric field at the cathode draws out the accumulation layer of electrons. As this accumulation layer moves in the drift region, the field behind it is lower than the field in front of it. The following simulations shown below, terahertz oscillation occurs.

1.1 Space Charge Instability Conditions:

When the average bias field in the channel rises above the threshold value and the inequalities (3), (4) and (5) are satisfied, exponentially growing electron accumulation layers (EAL) nucleate at the cathode and propagate toward the anode.

An insightful analytical expression n(x,t,k) as an approximate solution the equations which describe the electrodynamics inside the channel is given by:

$$n(x,t,k) \propto \exp\left(-t/\tau_\varepsilon\right)\exp\left(-D_0 k^2 t\right)\exp jk(x-v_a t) \qquad (1)$$

where τ_ε is the dielectric relaxation time, and:

$$\tau_{\varepsilon}=\frac{\varepsilon_r \varepsilon_0}{qN_D\left(\frac{\partial v_d}{\partial E}\right)} \qquad (2)$$

Here, n is the electron concentration, N_D is the doping in the channel, D_0 is the diffusion coefficient, v_a is the drift velocity of the EAL, and k is the wave number. It is clear from (1) and (2) that negative values of $\partial v_d / \partial E$ imply the growth, rather than dissipation, of disturbances in the neutral space-charge distribution.

The periodic nucleation and collection of these EALs at the anode creates current-voltage oscillations at the terminals of the diode at a frequency which is, to first order, determined by the average transit time of the EAL across the channel. Furthermore, at steady state, there is always an ac voltage superimposed on the dc bias voltage and thus the amplitude and phase of these oscillations depend strongly upon the external circuit.

In order to create the electro-dynamic behavior described above, certain design criteria, given by (3), (4) and (5), must be considered [4].

$$N_D L > \frac{2v_0 \varepsilon \varepsilon_0}{e\left|\frac{\partial v}{\partial E}\right|} > 2.1 \times 10^{12}\ cm^{-2} \tag{3}$$

$$N_D L^2 > \frac{\varepsilon \varepsilon_0 D \pi^2}{e\left|\frac{\partial v}{\partial E}\right|} > 0.3 \times 10^{7}\ cm^{-1} \tag{4}$$

$$N_D d > 2 \times 10^{11}\,\mathrm{cm}^{-2} \tag{5}$$

In these equations, L is the channel length, d is the thickness of the channel, N_D is the channel doping, D is the diffusion coefficient, e is the electronic charge and $\partial v / \partial E$ and v_0 are the average negative differential mobility and the average EAL velocity at the operating bias point, respectively. Calculated values for GaN for the 125 nm diode as follows: $N_D L$=12.5×10^{12} cm^{-2}, $N_D L^2$=1.56×10^{8} cm^{-1} and $N_D d$=2.0×10^{12} cm^{-2}. Also for 0.5×10^{18} cm^{-3}.

Satisfaction of condition (3) is necessary for the EALs to grow to maturity. Condition (4) is related to the diffusion effects. Indicated by (1), the diffusion causes distortion in the shape of the EAL. When (3) is satisfied, the accumulating force of the negative dielectric relaxation time will dominate over the dispersing force of the diffusion so that EALs may grow.

It should also be noted that the electric field outside the channel, produced by an EAL inside, acts to restore the charge distribution to a uniform state, opposing the formation of the EAL. For a sufficiently thin channel the effect is important, and the criterion is given in equation (5)

2. Vertical THz Device Research

We fabricated vertical diodes with 30 nm and 60 nm ballistic transit regions with and without an AlGaN/GaN interface for launching electrons with finite energy. This interface, due to conduction band offset, injects electrons in to the ballistic region with finite energy. We have investigated both negative effective mass and transferred electron phenomena through studying both short active regions for ballistic transport and relatively long (0.25um) lightly doped active regions for transferred electron

effect. We have also considered a process for submicron rectangular devices due to their superior thermal performance as explained below.

2.1 Cylindrical Devices

We have fabricated and studied both n+-i-n+ and AlGaN/GaN (0.4eV launching energy) heterostructure devices with cylindrical active regions (fig. 5a) on sapphire and SiC substrates. However no negative differential conductivity has been observed due to challenging engineering problems. The main problem was heating as a result of high current densities that permanently destroyed the top contact at and above a certain power level. At that power level, the amount of potential drop across the active region was still not enough to accelerate the electrons beyond the *E(k)* inflection point, where the electrons have negative effective mass. The other problem was the development of a new ohmic contact metallization for highly doped GaN surfaces. We have studied the d.c. parasitic resistances associated with different specific contact resistances; some of the results are presented in fig. 5b.

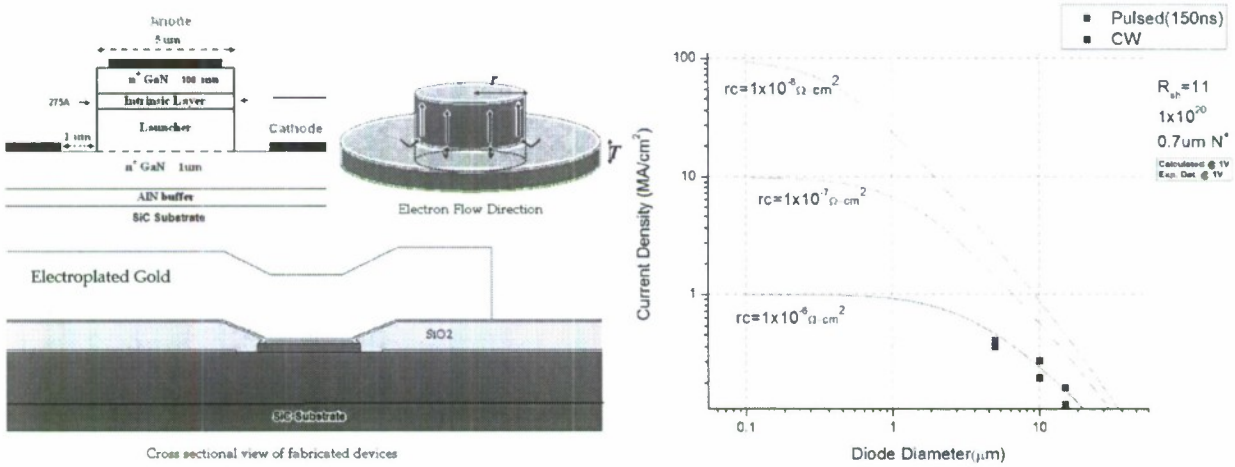


Fig. 5 a) Device Geometry. b) Parasitic Resistances. Blue and Red squares are experimental data measured @1V bias voltage. Continuous curves are calculations that assume a 1V bias voltage.

2.1.1 Thermal Simulations

Below we show the thermal simulation results of a five micron (diameter) cylindrical device. The improvement in heat dissipation due to SiC substrate can clearly be seen.

These results agree with what has been experimentally observed with five micron diameter devices which began to exhibit unstable ohmic behavior around the same power level (V=2.8V, J=0.66MA/cm^2). According to these simulation results, the channel temperature at this power level is above 750C (see Fig. 6). This is in agreement with the experiments because the ohmic contacts, which were annealed at 750°C, became thermally unstable - indicating that the operating temperature exceeded the anneal temperature.

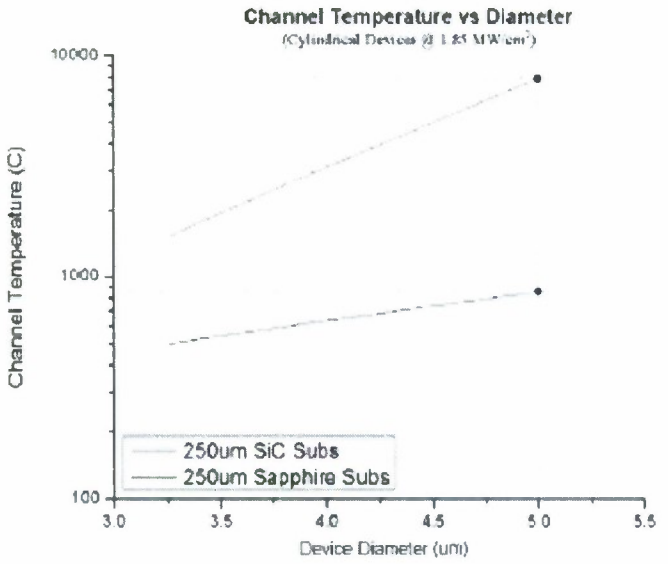


Fig. 6. The dot on the lower curve represents a fabricated device, at 1.848 MW/cm^2 power level, this resulted in ohmic metal instability and eventual failure of the device.

Simulations of ultra-narrow and long rectangular devices using the same code, on the other hand, showed a significant reduction of the channel operating temperature while maintaining the impedance level (see Fig. 7) through keeping the same surface area.

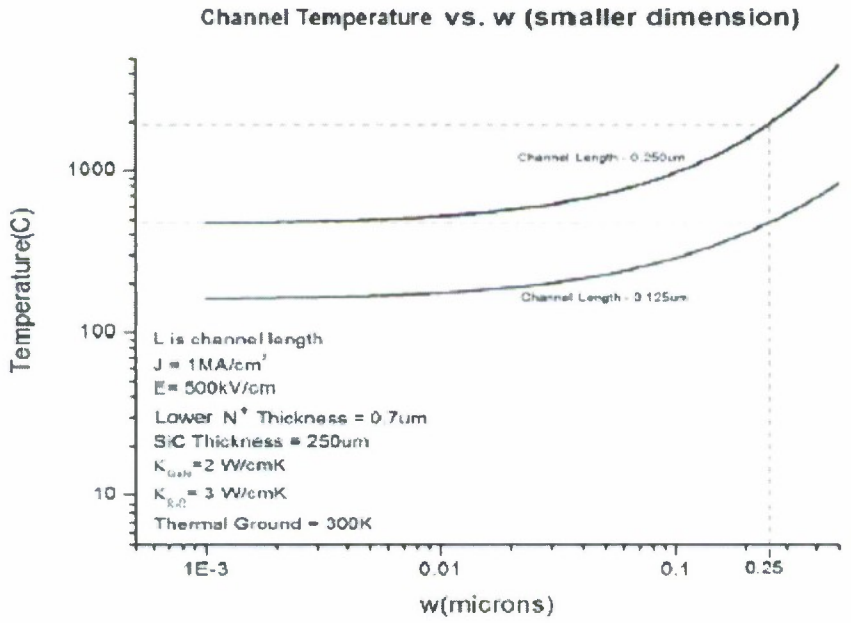


Fig 7. SiC substrate thermal simulation of rectangular wall structure - 'w' is the smaller dimension and the channel temperature is independent of the length of the mesa

2.2 Vertical Wall Type Device Considerations

We have tested many different epilayer thickness and doping combinations with the cylindrical design when we considered a change in direction of our research from the cylindrical geometry to ultra narrow 'wall type' rectangular devices despite challenging process development requirements. With major design challenges for these narrow submicron devices such as methods to make a good electric and thermal contact to the anode while passivating the walls, the much stronger benefits of a horizontal device lead us to eventually abandon all vertical structures designs.

3. Horizontal Ballistic Electron Acceleration Negative Differential Conductivity (BEAN) Device Design

Fig. 3 shows electron velocity versus applied electric field for 0.125 micron and 0.25 micron transit regions in GaN, based on Wraback's data. The shapes of these v(E) curves are reminiscent of those in long regions with dynamic equilibrium, based on electron transfers to upper valleys in the band structure. This has led some researchers to propose ultra short transferred-electron (Gunn) devices using the long channel velocity variation with applied electric fields, [4]. Monte Carlo simulations of such a long-channel have yielded peak velocity values of $3x10^7$cm/s, which have never been reached. The fastest electrons in 0.25 micron gate length GaN HEMT's is at or well under $1x10^7$cm/s. This long channel approach is completely inconsistent with regard to electron velocity values for ultra short transit distances in thin doped regions. All the real electrons transport physics, including the GaN band-structure, are covered, for short structures, by the Wraback optical pulse-probe measurements [2] of the velocity variations of these electron sheets shown in Fig. 1. The measured peak average electron velocity reaches about $6.5x10^7$cm/s value, for the 0.125 micron long channel. In preliminary measurements, a peak velocity of approximately $6.5x10^7$cm/s in the Γ-M direction was estimated in our 0.13 micron long structure tested recently (see figure 3).

To understand the operation of such devices, simulations of the oscillation in such a BEAN device has now been made, using the appropriate v(E) curve in the short drift region. The active layer was a 400A thick n-type with $1x10^{18}/cm^3$ electrons. The simulations showed that the operation is in the accumulation layer transit-time mode. The circuit is composed of the slot device cold capacitance in parallel with an external circuit inductance, and the electronic properties of the active layer. As well as the negative differential conductance, there is an extra electron capacitance from the accumulation layer formation and transit, lowering the operating frequency a small amount below the cold resonant frequency.

3.1 Material Structure

Thin (100-400A) MBE n-type approximately $1x10^{18}/cm^3$ GaN on semi-insulating substrates of SiC, and bonded to a thin diamond, have been used. This GaN active layer is covered with a 2000A n+ type GaN ($1x10^{20}/cm^3$) contact layer. Generally Ge has been used as the dopant, the contact transfer resistances as low as 0.1 ohm-mm has been obtained. Low contact transfer resistances are required to prevent

longitudinal optical phonons from being generated before the electrons enter the high electric field in the horizontal channel. These un-scattered electrons will enable the ballistic electron acceleration in the channel required for device operation.

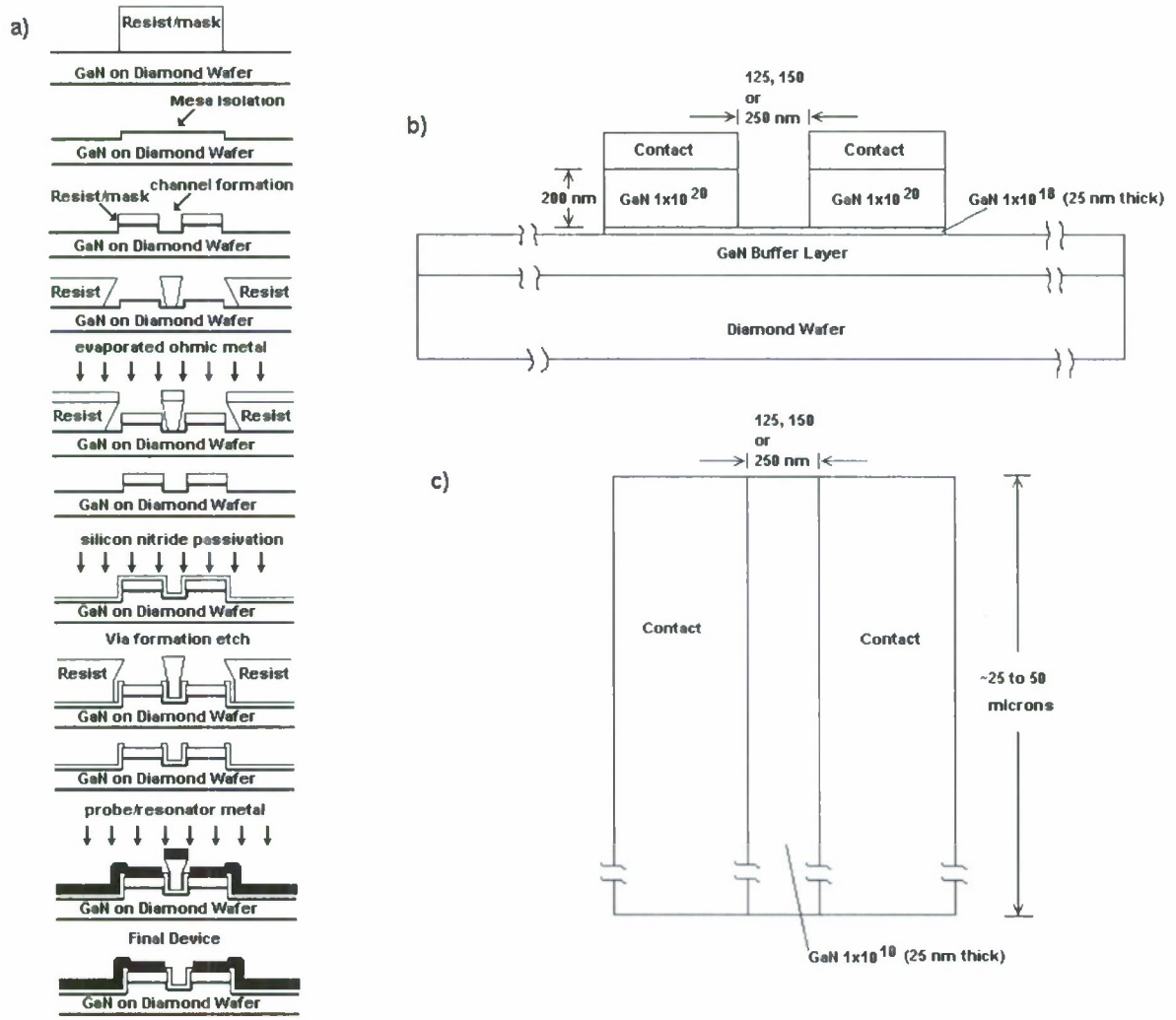


Fig 8. Fabrication method for the horizontal device, cross section, and device geometry

3.2 Fabrication and Characteristics

Several horizontal devices have been fabricated on both diamond and SiC based substrates. The most difficult part of the fabrication process has been achieving a precise etch through the N+ layer of the material structure. As stated above the material stacks used generally contain approximately 200nm of N+ material and between 20 to 40 nm of lightly doped N-type. A combination of inexact layer thickness and difficulty in targeting an exact etch depth to an error tolerance of less than 5% has made these devices challenging to fabricate. Nonetheless a couple devices have been successfully fabricated and tested on a diamond substrate. The fabrication method is described in Fig. 8. First the mesa is patterned using e-beam lithography and is formed using an ICP RIE etch. Then a channel is patterned and etched using an Ion Mill. During the etch using the Ion mill, several measurements are taken to

ensure the proper etch depth is achieved. Upon achieving the required etch depth the resist is removed and ohmic contacts are patterned. The patterned regions are cleaned using an O2 plasma, then the sample is dipped in a buffer oxide etch solution, this is followed by a water rinse and an isopropanol dip and then blown dry in dry nitrogen. These steps are necessary to ensure the features of the ohmic pattern are retained and that the material surface is sufficiently clean for proper ohmic formation. Ohmic metals consisting of either Ta-Ti-Al-Mo-Au or Ti-Al-Mo-Au are deposited. The sample is then covered in Si_3N_4 using plasma enhanced chemical vapor deposition. Via through holes are patterned and etched and the sample is then annealed. By using this sequence the ohmic metals are fixed in place during the anneal and this prevents shorts due to metal creep. Contact pads and/or resonator circuits are patterned and deposited using an electron beam evaporation of Ti-Au.

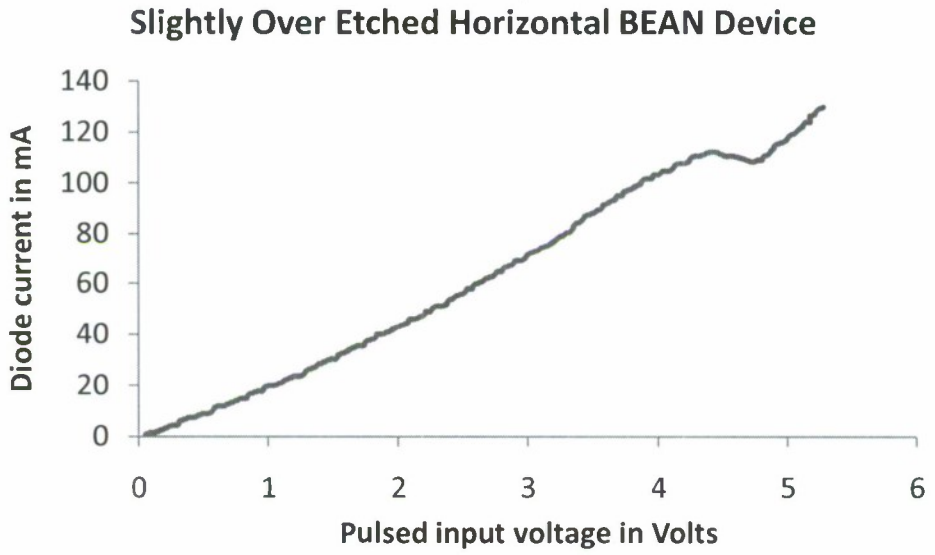


Fig 9. Initial measured I(V) results, showing negative differential conductivity in a slightly over etched device.

Two devices produced IV responses that were correspond to theory under pulse measurement conditions. One device appeared over etched or close to over etched (Fig. 9). The other device was under etched with a thin N+ layer (Fig. 10). The GaN epi layer on the diamond was severely cracked and this compounded the difficulty in achieving an accurate etch of the sample. The cracked structure lead to a slight rotation of all the devices to different z-angles resulting in different etches. Fortunately two devices worked providing initial verification to the theory. The deeper etched device resulted in a longer channel but otherwise the device structure was the same. The longer channel, combined with the over etch resulted in a less significant negative differential conductivity being expressed due to the reduced carrier density – length product (see equation 3). As well, it required a larger bias to get to the negative differential conductivity region (due to increased channel length). Both devices show the requisite reduction in current followed by an increase in current, and while it is believed both were producing THz radiation during testing, the devices failed prior to us being able to verify it. The failure mechanism was heating and the cause of the heating is believed to be related to the cracked epi. Poor

thermal paths from the epi to the diamond (due to the cracks) combined with high input power resulted in device failure. Subsequent experiments will be conducted on better material as much has been learned from these experiments, and material growth has been improved significantly.

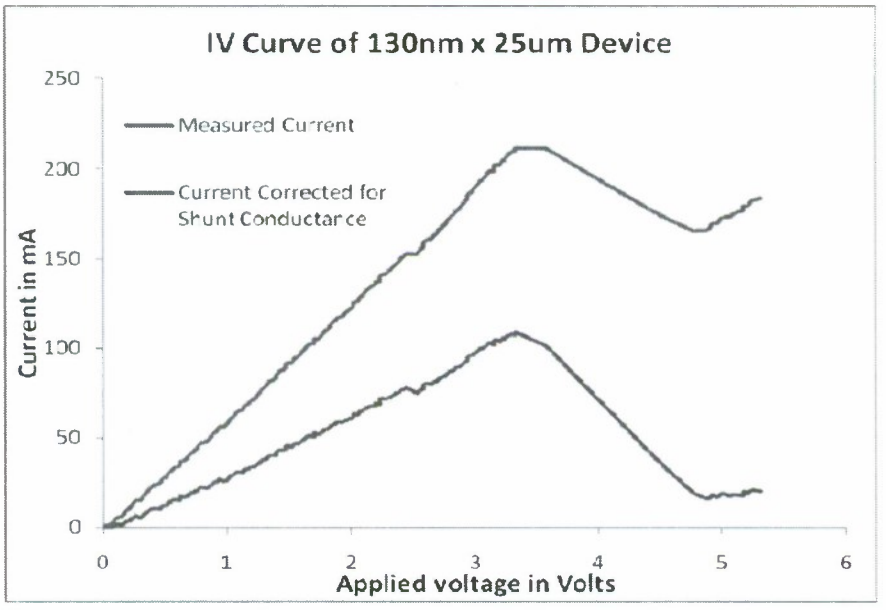


Fig 10. Initial measured I(V) results, showing NDC, and corrected for the presence of a positive current in the heavily doped region.

3.3 Electrical and Thermal Simulations of the Horizontal Device

The geometry of the GaN diode studied in the simulations is shown in Fig. 11. For computational efficiency and separation of the large geometric capacitive current I_{CD} from that of the electronic current I_D, the diode was modeled as a one dimensional (1D) n^+-n-n^+ structure in parallel with its geometric capacitance. The capacitance values for the selected 125 and 250 nm diodes are calculated from a two-dimensional (2D) small-signal finite element analysis of the corresponding geometries and found to be 4.22 and 3.45 fF respectively. These capacitance values are dominated by the fringing fields penetrating the undoped GaN as a result of its high dielectric constant compared to air.

The n^+ regions in the design facilitate good ohmic contacts with the physical diode and, at the cathode-side, provide the necessary electron concentration gradient for the periodic nucleation of the electron accumulation layers (EAL).

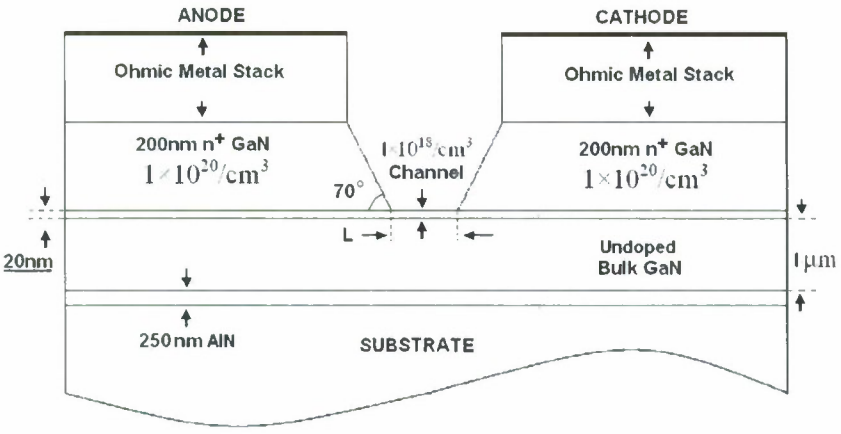


Fig. 11. Cross section of the simulated diode geometry.

This model is then placed in a circuit in parallel with an inductor and a load resistor as shown in Fig. 12. Simultaneous solution of Kirchoff's equations in nodal form follows (with zero initial conditions) and, for each instantaneous value of the anode voltage of the diode (which constitutes a boundary condition for the internal transport equations), simultaneous solutions of the Poisson and current continuity equations, (6) and (7), are obtained within the diode using the physics-based "Atlas" device simulator (Silvaco Inc.)

$$\frac{\partial E}{\partial x} = q\frac{(n - N_D)}{\varepsilon_r \varepsilon_0} \tag{6}$$

$$\frac{\partial J}{\partial x} = -\varepsilon_r \varepsilon_0 \frac{\partial E}{\partial t} \tag{7}$$

$$J = qnv_D(E) - qD_n \frac{\partial n}{\partial x} \tag{8}$$

The spatial and temporal mesh sizes were chosen according to (9) and (10) in order to ensure the accuracy of the solutions. [5].

$$\Delta t \ll \tau_\varepsilon \tag{9}$$

$$\Delta x \ll v\tau_\varepsilon \tag{10}$$

Here τ_ε is the dielectric relaxation time and v is the electron velocity in the cell. Inequality (9) implies that the time steps should be much shorter than the dielectric relaxation time characterizing the exponential growth rate of the EAL. Similarly (10) ensures the spatial resolution of the EAL within a dielectric relaxation time.

Note that this is a quasi-static approximation which assumes that the drift velocity instantaneously follows the local electric field. In reality, velocity-field characteristics are always a function of the displacement current due to the finite kinetic relaxation times associated with the intervalley

transitions. In collision dominated transport, this dependence is particularly important at frequencies approaching

$$f = \frac{1}{\tau_{ER} + \tau_{ET}} \tag{11}$$

Here, τ_{ER} is the energy relaxation time and τ_{ET} is the inter-valley relaxation time. [6]

However, in the ultra-short BEAN diodes, not only are there apparent ballistic electrons involved in the transport [2, 7-9], but also, the electrons transferred to the satellite valley are not likely to have enough time to scatter back to the Γ valley [2] before being collected at the anode, eliminating the longer component of the inter-valley transition delay. Thus, the quasi-static approximation is justified, giving these devices a tremendous potential for efficient THz generation.

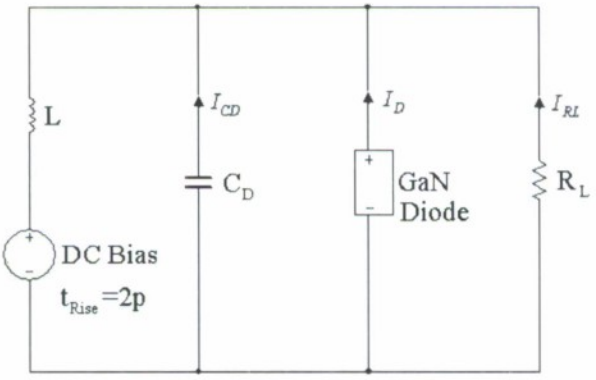


Fig. 12. Parallel resonant circuit - dc bias rise time is 2ps. C_D represents the geometric capacitance and R_L is the load resistance.

3.3.1 Discussions on the Simulation Results Of A Particular Oscillator Design of a 125 nm Diode

Numerous bias voltage and load resistance combinations for 125 and 250 nm devices have been studied and collective results will be presented in this section. In Fig. 13, only the important internal parameters for a particular 125 nm diode design are shown and discussed. The diode and circuit parameters used for this simulation are tabulated in Table I.

TABLE I - SIMULATION PAREMETERS

Parameter	Value
Channel length	125 nm
Channel thickness	20nm
Channel doping	1×10^{18} cm^{-3}
Device Width	50 microns
Load Resistor	220 Ω
Bias	10 V
Fundamental Frequency	2.9 THz

ac output power	0.5 W/mm
dc power dissipation	22.5 W/mm
Phase angle difference	72°
Efficiency	2.2%
Quality factor (4.2fF // 0.6pH)	18.3
VD peak to peak	6.7 V
ID peak to peak	2 A/mm
ICD (geometric capacitance) pp	10.5 A/mm

Fig. 13(a) illustrates the nucleation and propagation of the EAL s (for one oscillation cycle) as a function of time. The EAL is, on average, two room-temperature Debye lengths wide with its peak density saturating at ~2×10^{19} cm^{-3}. The insert shows the average velocity of the EAL over time; the peak velocity in this case is rather small compared to the material velocity field characteristics due to the high bias voltage. Furthermore, the maximum field strength in the vicinity of the anode region is ~3.0 MV/cm; however, the concern of the avalanche breakdown is mitigated due to the narrow spatial extent of these fields as shown in Fig. 13(b). In order for breakdown to occur, the total energy absorbed by the ballistic electrons, $E\times\lambda_m$ (λ_m is the approximate mean free path and E is the electric field) should exceed the band gap energy of 3.4 eV roughly by 50%, which is ~5.1 eV.

In Fig. 13(c), it is also seen that the number of cycles required to build up the oscillations is approximately equal to the quality factor of ~18. Shown in Fig. 13(d) is the phase plane plot of the I_D and V_D as a function of time. The current contribution due to injected space charge is more pronounced for the shorter diode.

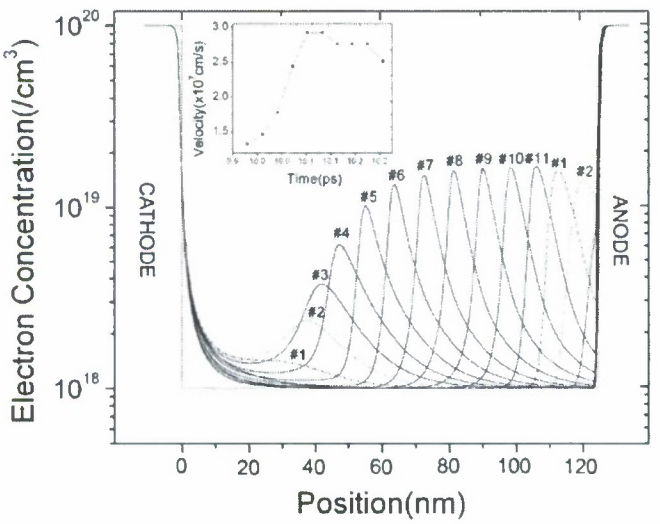


Fig. 13. a) Electron concentration vs. position at successive instances of time showing EALs in transit moving towards the anode. Background doping is shown dashed. Insert shows the average EAL velocity as a function of time. Each numbered curve represents an instant of time that are 30 fs apart.

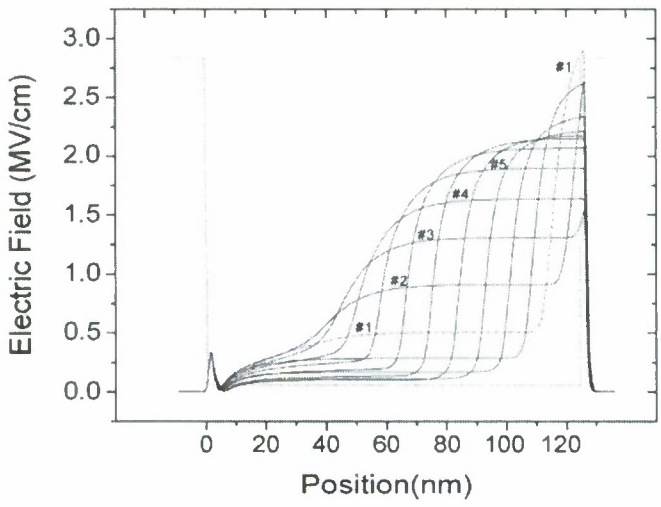


Fig. 13. b) Electric field vs. position - each numbered curve represents an instant of time that are 30 fs apart.

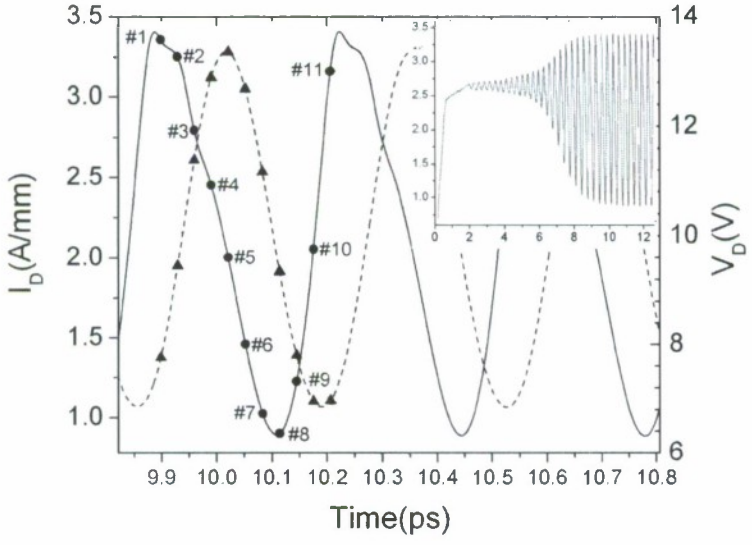


Fig. 13. c) Anode current-voltage waveforms as a function of time . Insert shows the build up of the current oscillations.

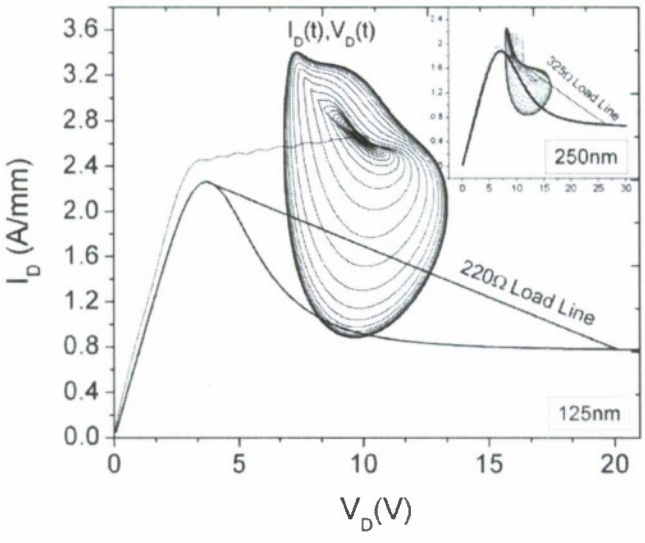


Fig. 13. d) Phase plane plot on the dynamic load line. Insert shows a 250 nm diode.

TABLE II - HARMONIC CONTENTS OF THE OSCILLATOR OUTPUT

Harmonic (THz)	I (A/mm)	V(V)	P (W/mm)	Theta
2.88 (1st)	0.98	3.34	0.5	72.1
5.76 (2nd)	0.26	0.1	3×10-3	76.6

Harmonic content of the ac power output has been analyzed using the Fast Fourier Transform (FFT) technique with a Kaiser Window function of (Table II) [10]. The sampling and fundamental frequencies were chosen to be 50 THz and 2 GHz, respectively, in order to satisfy the Nyquist criterion. As indicated in Table II, the current has a rather significant second harmonic, while voltage is nearly sinusoidal, consistent with the well known characteristics of high-Q oscillators.

3.3.2 Collective Results and Discussions

NDC oscillators based on space-charge instabilities present an extremely nonlinear mathematical problem. With today's computational resources however; a brute-force approach of simulating selected combinations of parameters to identify trends and understand the diode operation as part of the circuit environment is possible. In this section, results of such selected combinations of bias-load parameters are presented for both diode lengths. For each combination, the efficiency was maximized through many iterations tuning the parallel inductor. The bias-load combinations were chosen based on a load line analysis using an IV curve constructed by scaling the corresponding velocity field relation. A comparison of the NDC diode characteristics for the two diode lengths is shown in Table III.

TABLE III - NDC DIODE CHARACTERISTICS WIDTH A 50 μm DEVICE WIDTH

Parameter	125 nm	250 nm
Threshold Bias Voltage	3.7 V	7.2 V
Peak to Valley Ratio	2.8	2.7
Low Field Conductance	0.037 S	0.017 S
Max. Negative Conductance	0.020 S	0.009 S

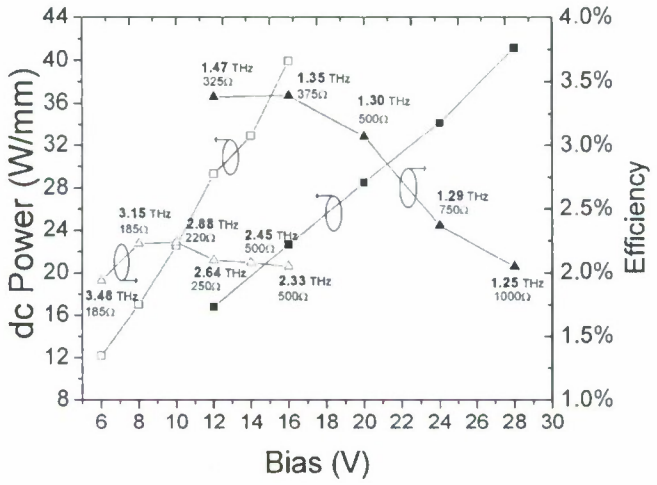


Fig. 14. Efficiency and dc power dissipation comparison between 125 (open) and 250 nm (closed) diodes as a function of bias voltage. All the diodes are 50 μm wide. Each load-bias combination is tuned with the parallel inductance for maximum efficiency. Corresponding oscillation frequencies (fundamental) and load resistance values are also labeled on each data point.

3.3.2.1 Efficiency monotonically decreases with increasing bias voltage

When bias is increased, the efficiency decreases despite the increasing ac power output. This is caused by the faster increase in the dc power dissipation. The conversion efficiency here is defined as the ratio of ac power delivered to the load and the dc power dissipated in the GaN diode. Consistent with the load line perspective, the trend is that, as the bias voltage is increased, the optimum load resistance yielding the maximum efficiency also increases; this, in turn, increases the peak-to-peak amplitude of the voltage and current swings despite the fact that the phase difference monotonically approaches 90 degrees from below, at which no power can be generated. The amount of dc power dissipation is considered critical for the important role it plays in determining the channel temperature from a practical point of view and, transient thermal presentations will be presented and discussed in section VII.

3.3.2.2 Oscillation frequency decreases with increasing bias voltage

As shown in Fig. 15, decrease in frequency is a result of the higher (average) electric field across the diode, effectively slowing the EALs in transit. This trait of bias tunability is very desirable. Moreover, cold circuit resonance frequencies calculated from

$$f_R = \frac{1}{2\pi\sqrt{LC}} \tag{12}$$

are also shown in Fig. 15. The contribution from the non-linear capacitance of the channel is apparent from the EAL dynamics; however, the difference between cold resonance calculations and actual oscillation frequencies remain approximately constant.

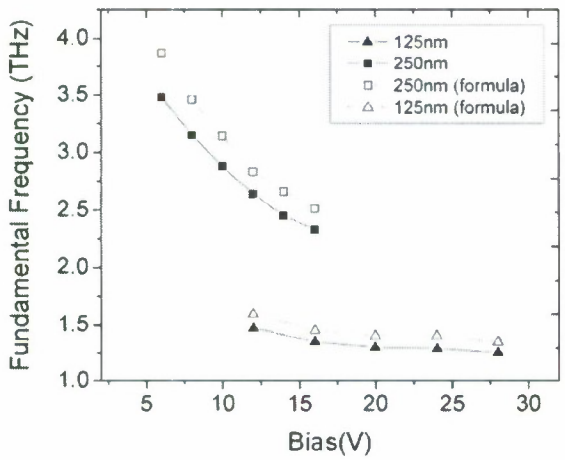


Fig. 15. Fundamental oscillation frequency vs. bias voltage and cold resonance frequency calculations for 125 (open square) and 250nm (open triangle). Comparison illustrates the influence of the nonlinear capacitance of the channel.

3.3.2.3 DC Power dissipation levels are similar for both 125 and 250 nm diode lengths

The 250 nm diode requires about twice the bias voltage compared 125 nm; however, the dc Power dissipation levels are quite similar. The increased space-charge limited current is is responsible for this through compensating for the lower threshold voltage in the P=IV power expression.

3.3.3 Thermal Dynamics of the Horizontal BEAN Device

One of the challenges in electronic THz power generation using GaN-based NDR diodes has proven to be the reconciliation of the high current density and high electric field operation requirement with an efficient heat dissipation strategy to prevent excessive heating or, more severely, permanent destruction of the diodes. Substrate thickness (typically several hundreds of microns) and its thermal conductivity plays a very important role in determining the channel temperature. Due to the lack of native substrates, materials such as sapphire and SiC are popular as host substrates for GaN epilayers. Despite its inexpensive price, sapphire is not considered appropriate for the fabrication of BEAN diodes with its room temperature thermal conductivity being 0.35 $W\text{-}cm^{-1}K^{-1}$, an order of magnitude less than

that of SiC. Even SiC of usual ~ 300-400 μm thickness appears to be excessive based on the following thermal simulation results. GaN on chemical vapor deposited (CVD) polycrystalline diamond substrates on the other hand have received a lot of attention recently and have already been experimentally demonstrated to operate significantly cooler than GaN on SiC with its more than 10 $W\text{-}cm^{-1}K^{-1}$ room temperature thermal conductivity [24].

In this section, transient thermal simulation results of the proposed BEAN diodes on 25 μm (thick) back-side thinned SiC and 40 μm thick CVD diamond substrates is compared in terms of channel temperature rise. The (2D) finite element thermal simulations of the geometry (Fig. 1) were performed using the "Giga" module of the "Atlas" device simulator and simulation parameters are tabulated in table IV. These parameters are tested against experimental measurements (time-resolved raman thermography) and verified by simulating the identical structure reported in [11].

TABLE IV - THERMAL PARAMETERS OF MATERIALS USED IN SIMULATIONS

Parameter	GaN	SiC	Diamond
Thickness	1μm	25μm	40μm
Cp(J/g/°C)	0.49	0.69	0.50
p(g/cm^3)	6.09	3.21	3.515
κ($Wcm^{-1}K^{-1}$)	$2\times(T/300)^{-0.6}$	$3.5\times(T/300)^{-1}$	$10\times(T/300)^{-1}$

Cρ is the specific heat, ρ is the mass density and κ is the thermal conductivity

In the following thermal simulations, only heat diffusion from the bottom of the substrate is taken into account and heat removal along the contacts has been ignored. For the bottom of the substrate, an isothermal boundary condition of 0 °C has been applied corresponding to the case of a perfect heat sink. Thermal boundary resistance at the epilayer-substrate interface, measured by Kuball et al. [11] has not been modeled. Peltier or Thomson effects are also ignored. The duty cycle of the pulsed power source is set low enough for the diode to cool down near the ambient temperature before the rise of the next pulse.

Simulation results presented in Fig. 17 indicates that 40 μm CVD diamond substrate performs better than back-side thinned 25 μm SiC as a heat sink. Note that the thermal load of the substrate does not show up in the channel temperature up until between 20 ns and 50 ns pulse time. The oscillator design utilizing the 125 nm long diode discussed dissipates 22.5 W/mm dc power at 2.2% efficiency and, from Fig. 14, the channel temperature rise for this diode is predicted ~300 °C on diamond and ~350 °C on SiC with 50 ns pulsed biasing. Moreover, the same diode can be operated at 12W/mm dc dissipation with 1.8% efficiency and the temperature rise for this case would be ~165 °C on diamond and ~200 °C on SiC for the same pulse length (Fig. 16).

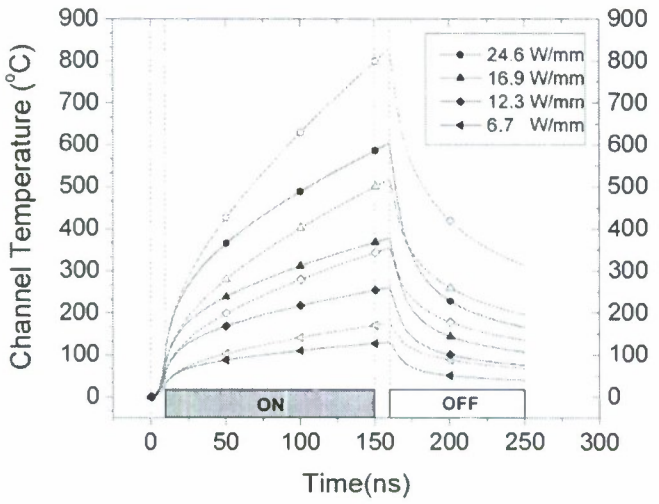


Fig. 16. Temperature rise in the channel as a function of time and dc power dissipation. The temperature is probed at the center of the 50 µm wide, 125 nm long channel on 25 µm thick SiC (dotted) and 40 µm thick diamond (solid) substrate. Pulse duration is 150 ns with 10 ns rise and fall times.

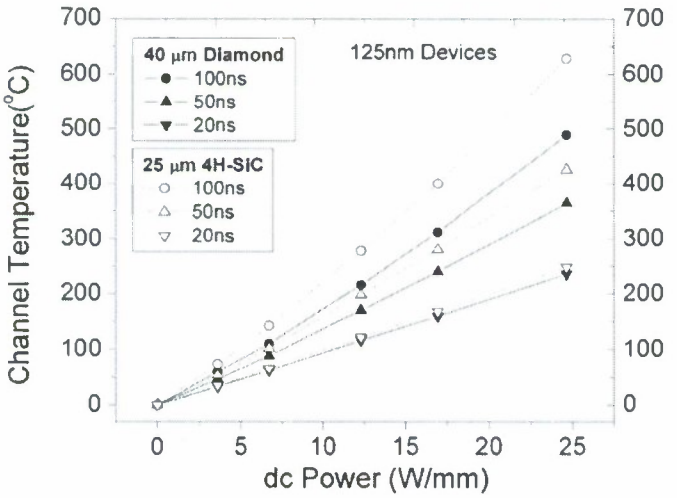
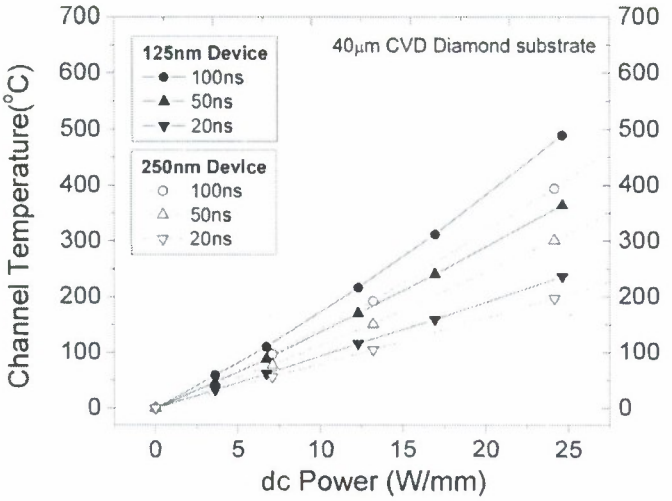


Fig. 17. a) Temperature rise as a function of dc power dissipation - comparing CVD diamond and SiC host substrates.



(b)

Fig. 17. b) Temperature rise as a function of dc power dissipation - 125 nm and 250 nm diodes on CVD diamond substrate.

In the simulations presented above, the power dissipation was assumed to be ohmic. In these ultra-short diodes however, the spatial extent of the hot electron energy relaxation will be longer if we assume the optical phonon emission to be the only energy loss mechanism for the hot electrons. For a ballistically accelerated electron to dissipate 2 eV of kinetic energy for instance, ~20 optical phonons emissions are needed each with 92 meV energy. If we assume a mean free path of ~20 nm, a total of ~400 nm transit distance is necessary to dissipate all kinetic energy. This will lead to a reduction in the power density per square centimeter and thus a cooler operation. See Fig. 17(b) to compare the temperature rise of 125 and 250 nm diodes when dissipating the same amount of dc power.

3.4 Resonators and Test Structures

Although the BEAN device is believed to produce direct radiation from the device slots, determined by the channel length, the fabrication of devices with a diagnostic on-chip resonator is useful. To better understand the devices characteristic we designed a structure to help control the frequency and the output coupling (see Fig. 18). The diagnostic structure has been designed that uses two BEAN devices centered in a coplanar transmission line, with nearly a ¼ wavelength distance from the center of the active devices to each of the sides with short circuits at the ends. In order to allow a DC bias and still have a THz capacitor short, the top and the bottom electrodes will be overlapped at the ends, with a thin Silicon Nitride dielectric between them. The two BEAN devices will be formed, back to back, with a negative central bias and the two side electrodes grounded. This design forces the two channels to be in opposite phase, limiting radiation above and below, but allows an antenna or other load to be connected. The ground electrodes, with larger surface area, will be used to dissipate the higher heat power, caused by the collection of hot electrons. The designed structure has a THz load impedance that is expected to be close to 47 ohms. This is coupled with a device expecting to yield on the order of 10 mW power at approximately 3 THz at near 2% electronic efficiency, based on simulations.

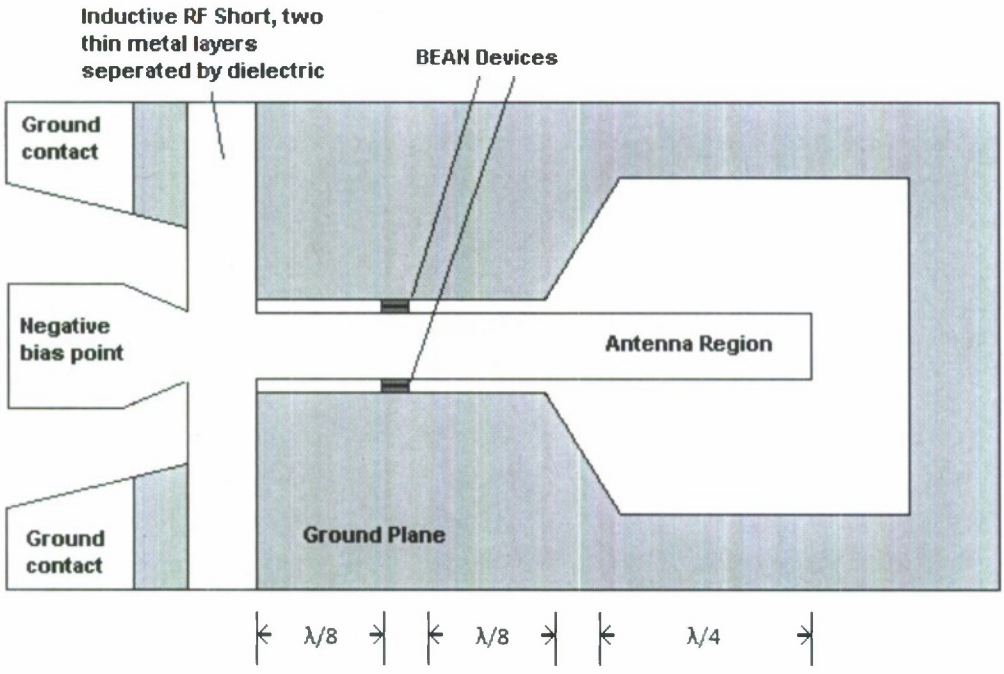


Fig. 18. Diagnostic device with coplanar interface, inductive short, and output antenna. Metal layers under coplanar short are separated by dielectric, devices and pads are connected to both metals by via regions not visible.

4. Enhanced Transistor Performance via High Speed Electrons

Currently GaN transistors are limited in performance by low electron velocities of approximately 0.8×10^7 to 1×10^7 cm/s, and high contact resistance. This can be greatly improved by utilizing the ballistic electron velocity effects observed in GaN [1, 12]. Currently HEMT material systems have high carrier densities confined to a narrow channel region. As the carrier density increases phonon production increases non-linearly creating many more phonons at high electron densities. The material system proposed for the BEAN device is suitable for producing both a MESFET and a MISFET/MOSFET structure. This material system has the carriers distributed over a larger volume which is expected to support the high velocities over the short channel regime. For long channel devices HEMT material systems are generally superior. However, for short channel applications they may be limited by high phonon build, essentially reducing the ballistic mean free path and limiting electron velocities.

GaN channels with lengths of the order of 1 micron have been shown to yield average electron velocities on the order of 4×10^7 cm/s which is approximately 4 times faster than what has been observed in HEMT's [12]. Using the expression:

$$f_t = \frac{V_e}{2\pi L_e} \tag{13}$$

Where V_e is the carrier velocity (4x10^7 cm/s) and L_e is the effective gate length (determined by channel thickness and measured gate length, approximately 75 nm), we have estimated that an intrinsic f_t of 850 GHz is possible for a transistor with a 35nm gate length placed in a 500 nm source drain region. A 35 nm gate in such a channel has already been successfully used to pinch off the current in an initial experiment at Cornell University. It is expected that the high velocity electrons produced as a result of short channels can be utilized to overcome some of the frequency limitations in GaN. This research is expected to produce extrinsic f_t values in excess of 300 GHz with additional performance possible with scaling.

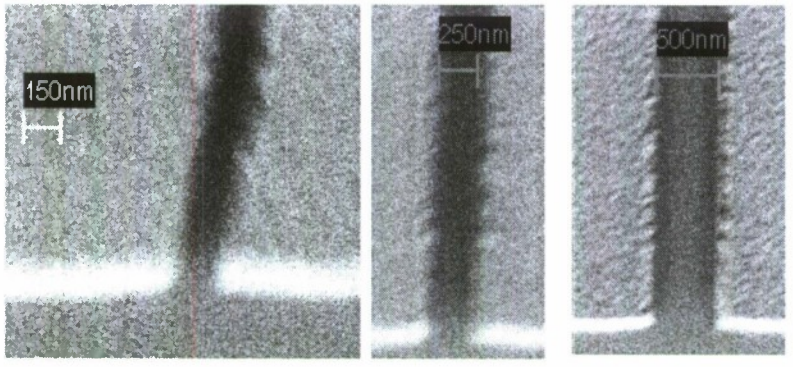


Fig. 19. Narrow gap ohmic contacts for BEAN devices and Transistors – A thin film of silicon nitride was applied prior to anneal to prevent the flow of the ohmic metals.

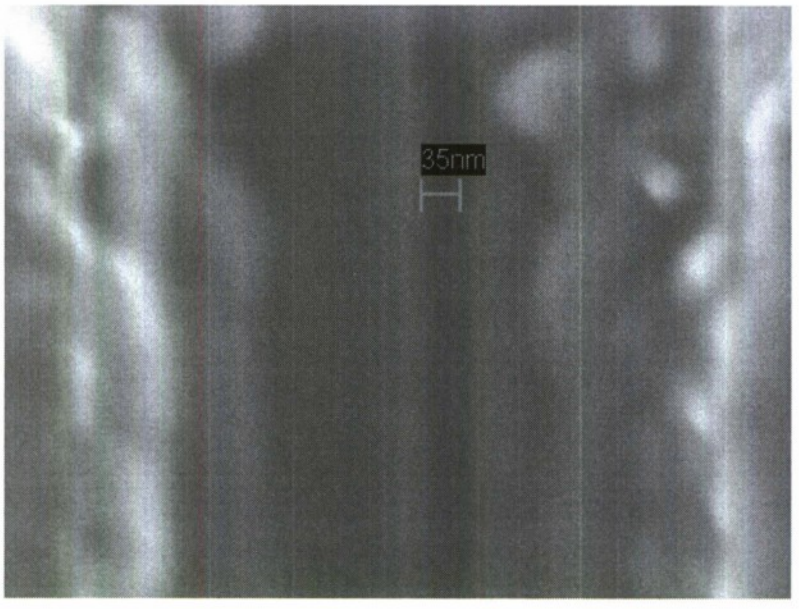


Fig. 20. A sub-35 nm gate recess etch into silicon nitride in a 250 nm source-drain spacing.

By extending the fabrication methods of the BEAN device to transistors (see Fig. 19 and 20) it is possible to realize these types of devices. Initial data suggests that only close proximity to the source contact is necessary to achieve high f_{Max} values.

5. Summary

To summarize the BEAN device is a novel concept expected to produce THz radiation. Initial experiments have verified negative differential conductivity effects in GaN, but have also shown that heat is a serious challenge. The vertical structure initially investigated has been determined to be non-feasible due to these heating effects. The horizontal structure on SiC or preferably diamond substrates have much better thermal characteristics. Two devices have been successfully fabricated, but it will take more research effort to verify the expected THz emission. Additionally several proto-type structures to enhance transistor performance have been fabricated. We have verified that it is currently possible to fabricate the geometries necessary to use ballistic electrons in GaN. This is expected to achieve much higher frequency response than is currently considered possible with HEMT techniques.

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