Evaluation of 10 kV, 80 kA Si SGTO Switching Components for Army Pulsed Power Applications

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***Abstract*- The U.S. Army Research Lab (ARL) is investigating the switching capabilities of advanced silicon devices for high current pulsed power applications. These solid state switches are intended to replace more traditional vacuum switches. The benefits of these switches are higher dI/dt, peak power levels and current densities, increased reliability and lifetime, and smaller switch volume [1]. The peak current achieved by the device was 83.3 kA, with a 10% to 90% rise time of 3.5 µs while a 0.263 MA^2 s without failure. The peak power of the device during this test shot was 78.7 MW. ARL is collaborating with Silicon Power Corp. (SPCO) to evaluate Super-GTO performance and improve upon switch/buss bar packaging for pulsed power applications.**

I. INTRODUCTION

The basic layout of Si modules from SPCO that ARL evaluated consists of eight SGTO die in parallel. The die arrangement is setup such that the module has two cathode rings, each with four die tied to them (Fig. 1). The two cathode rings are connected at the base of the module so that each ring is essentially the same point on the module. Fig. 2 shows a single module with eight dies, the two cathode rings and the modules' buss system.

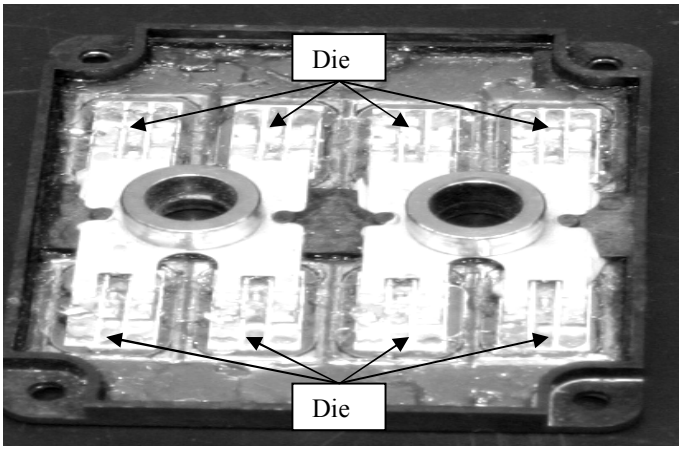

Fig. 1. A shot of inside the module showing each cathode ring being connected to four die. This separation creates two halves of the module.

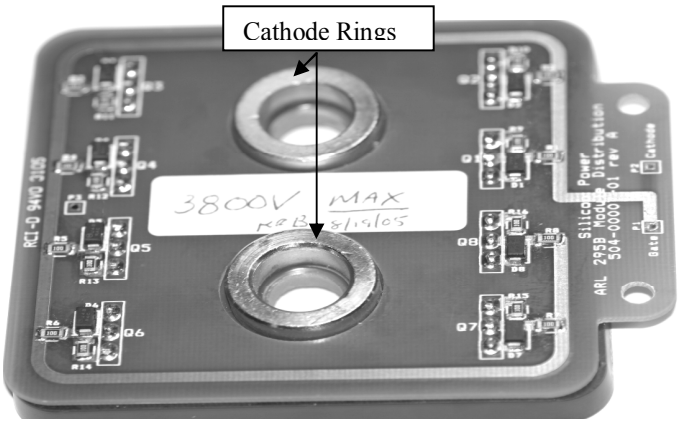

Fig. 2. Si module showing the 8 individual die with cathode rings and gate current buss system.

As you can see in Fig. 3, during testing the rings can be monitored via current loops located at the top of the cathode rings on the 80 kA switch to make sure that the switch is sharing current equally between each set of cathode rings. Each individual die is rated for 3.5 kV blocking and 10 kA conduction.

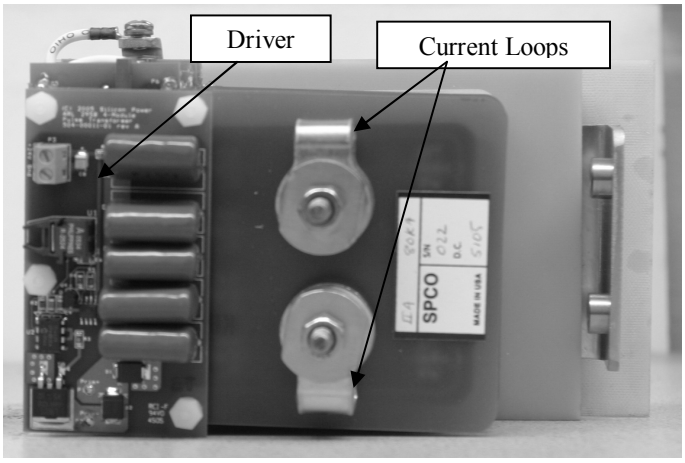

Fig. 3. Top view of 80 kA, 10 kV switch with driver and current loops attached.

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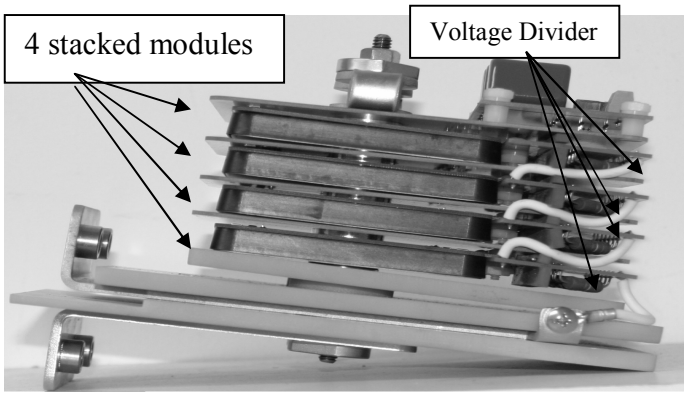

Fig. 4. Side view of 80 kA, 10 kV switch showing the four layers of modules, the voltage divider connections between each level, and the buss bar.

Therefore, each module can handle 3.5 kV blocking and 80 kA conduction. They are composed of a fine integrated gate structure that allows the switches to reach full conduction faster than conventional thyristors, optimizing them for fast turn-on and high dI/dt [2]. The gate driver is mounted to the top of the switch and is composed of 5 capacitors that are charged by a 24 V battery. The trigger signal is sent via a fiber optic link from the function generator to the switch itself. Depending upon the pulse width of the trigger signal, a percentage of all five capacitors will discharge their stored current. This in turn controls the pulse width of the gate driver. If all five capacitors are discharged to their full ability, then the pulse width of the gate driver is around 16 µs. For the 16 µs gate driver pulse to occur, a trigger pulse of 15 µs or more is needed. Usually a pulse width of 20 µs is used to make sure the gate driver is triggered fully.

The 10 kV, 80 kA switches detailed in this report are built by combining four SGTO modules, each with eight parallel die per module, in order to withstand specific applied currents and voltages. The switch itself is comprised of four layers, with one module per layer. A voltage divider network has been attached to each level such that each level shares one quarter of the applied voltage when the switch is in the "OFF" state (Fig. 4). During testing, voltage probes are attached to monitor each of the four levels' performance. These four layer switches are based off of an earlier version of switches which were two layers that held off 7 kV and 80 kA [1]. The extra two layers were added so that the SGTO could be tested up to 10 kV without failure. Although adding one layer would have allowed the SGTO to block 10 kV, a second layer was added for extra protection against high voltage and for a safe voltage operating margin.

II. Evaluation

Before the 80 kA, 10 kV Si SGTO switch is pulsed, a visual inspection and high voltage-potting (HVP) is done to ensure the unit is ready for low to medium level switching. At this point the anode to cathode current leakage is checked (typically around 2mA), as well as the voltage sharing of each level of the device. After each switch has been verified via high-potting, it is then put in the ring down RLC circuit for testing. The reason

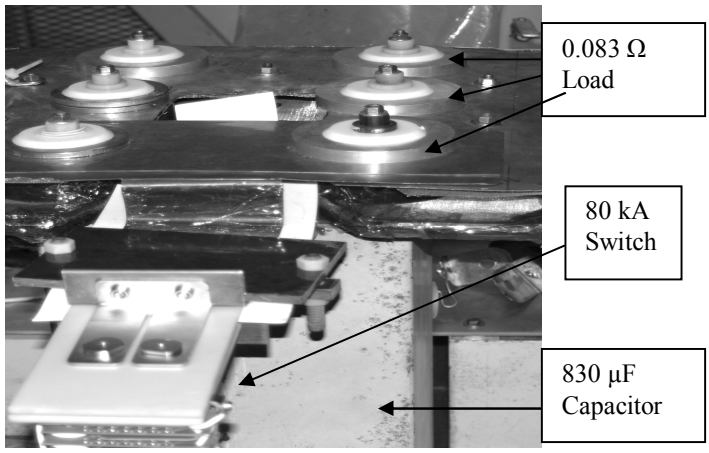

Fig. 5. RLC ring down test circuit with 80 kA switch attached.

for the ring down circuit being used prior to testing on the pulse forming network (PFN) is to verify that the switch can handle a high peak current at a shorter pulse width. Therefore, less action is put on the switch since action (A) is defined by equation (1).

$$A = I^2t \quad (1)$$

Whereas I stands for current and t represents time. The total current, current sharing, voltage and voltage sharing between levels are recorded to verify operation and so that each switch can be compared to find out which switches are capable of the best performance. The ring down RLC circuit is composed of a single 830 µF capacitor with a load of 0.083 ohms and a copper buss that extends to the 80 kA switch (Fig. 5). If, during low to medium level testing, it is noticed that the sharing between the two current loops of the device do not share within 5% of one another, then the switches are removed from the test circuit. The four layer switches are then disassembled and each individual gate is checked for proper anode to cathode and gate to cathode impedance, as well for possible shorts on the module. If a die in one of the modules is leaky, the voltage drop across that module will be lower than the voltage drop in the other series connected modules. Therefore, the four levels will not share the total applied voltage evenly. Once all problems have been corrected, the switch is then reassembled and checked to make sure that the clamping of the four modules is tight and then reinserted into the ring down for further testing.

After evaluation in the RLC circuit, the switch is then inserted into our 5 stage parallel PFN. Before any testing is done, a simulation of our test circuit is created in PSpice and run (Fig. 6). If the data from the simulation is agreeable, then the initial testing of the switch begins. After a few test shots of the PFN the data collected is compared to the simulation data to make sure that the simulation data is valid. If there is a difference between the simulation data and the data collected both, the PFN and the simulation circuits are checked to see why the discrepancy exists. The reason for the PFN being setup in parallel instead of in series is to ensure that the test setup can handle all 80kA. Each PFN is setup to handle 40 kA, so two PFNs were setup in parallel such that the full 80 kA could be achieved without overdriving the test circuit.

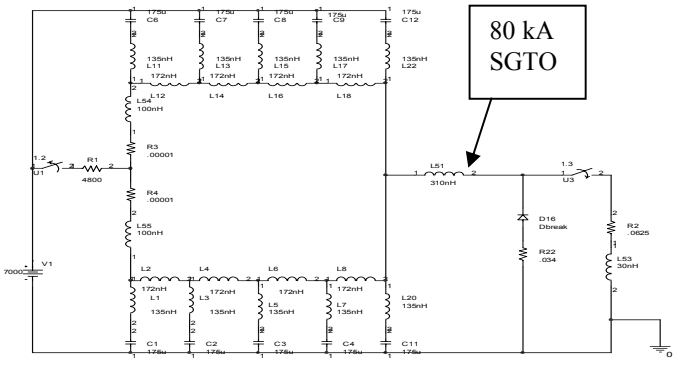

Fig. 6. A Pspice schematic of the 5 stage parallel PFN used to test the 80 kA, 10 kV switch.

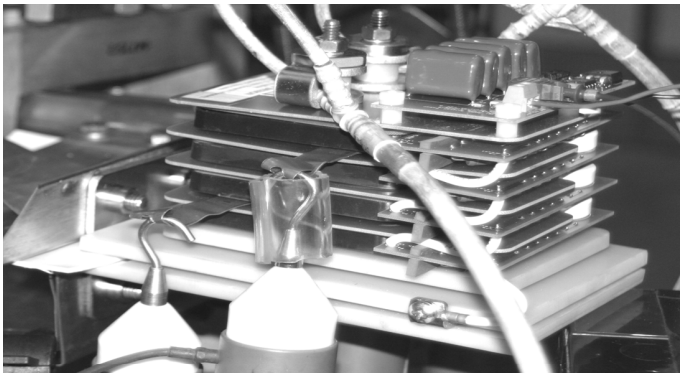

Fig. 7. 80kA switch attached to the PFN test bed with voltage and current probes attached.

The paralleled PFN has is comprised of 175 μF capacitors, each with an internal inductance of 100 nH (Fig. 6). The extra inductance comes from the copper and steel bars that attach the anodes of each capacitor to one another. The switch is started at a low voltage (200 V) and increased incrementally until the desired current is reached (approximately 7.5 kV). During testing the device is monitored for its total current, each current loop attached to the top cathode rings of the device, the voltage across the load and the voltage on all four layers of the device (Fig. 7). The requirements of the switch were to have the first flat region of the total current waveform occur at 80 kA (Fig. 9). The initial peak of the current waveform was not seen as significant because it was instantaneous, creating very little action. Although the requirements were initially met using five rows of capacitors (ten capacitors total), it became necessary to go down to four rows of capacitors for a shorter pulse width. The action of the device with five rows of capacitors was 0.61 MA^2s. By removing the fifth row of capacitors, the pulse width dropped from 120 μs to 71.9 μs. Simultaneously, the current was dropped such that only the peak reached 80 kA. Consequently, the action dropped down from 0.61 MA^2s to 0.37 MA^2s. The result was a similar current wave form with a smaller pulse width but the switches no longer failed after switching the 80 kA, 6 kV test shot.

III. RESULTS

A. Ring down Circuit

The test bed was setup to achieve 83.3 kA at 8 kV, with peak 10% to 90% rise time of 18.4 kA/μs and a pulse width of 57.1 μs without failure. Pulse widths are measured from the points which are 50% of the total current's peak. For example, if the total current's peak occurs at 80 kA, then the pulse width would be measured from the two points at which the total current waveform crosses 40 kA. At those points the time is recorded, subtracted from one another and the absolute value of the remainder is the pulse width of the waveform. Due to the max current of 83.3 kA being reached at 7.5 kV (Fig. 8), and since the switches are high-potted to 10 kV before and after being tested, it was unnecessary to go to higher voltages/currents on the test bed. The total action was 0.263 MA^2s. Five test shots were taken at this action to show that the switch could handle repeated shots and continue to function properly. The current sharing between the current loops of the device was +/-1% of sharing equally. Also, the voltage seen on each of the four layers was approximately +/- 1% from one quarter of the total voltage. Voltage sharing can be skewed by the fact that the resistors used in each divider network have a +/- 5% variance from theoretical to actual value. Each level of the voltage divider is composed of seven resistors each with the value of 160 kΩ. They are combined in series such that each of the four layers has 1.12 MΩ of resistance. Also, the slight differences in the internal resistance of each die, as well as the rate the switches are being triggered, can change how much voltage each level of the switch draws. After each successful round of tests the switches were then high-potted at 10 kV to make sure that their voltage hold-off capabilities had not been compromised.

B. *Pulse Forming Network*

For the pulse forming network setup the 10 kV, 80 kA devices were tested with a single shot rate to as high as 7 kV and 91.4 kA, with peak 10% to 90% rise-time of 16.83 kA/μs and a pulse width as wide as 119.7 μs. We tested the SGTO beyond 80 kA because the first flat region of the PFN needed to be above 80 kA, since that is what the modules would be tested at when put

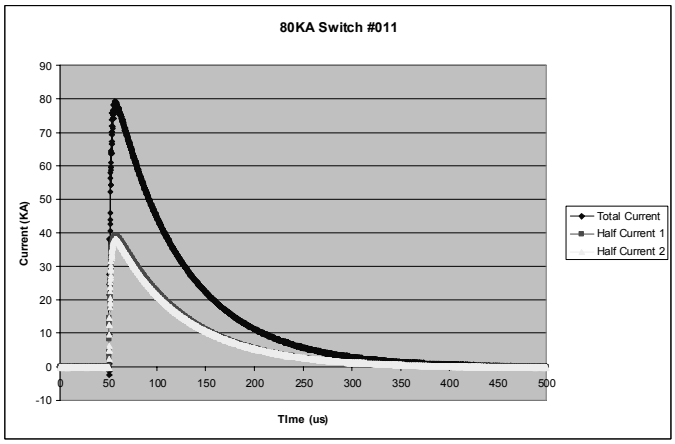

Fig. 8. Data from the ring down circuit at 80 kA and 7.5 kV. This graph shows the total current as well as how well each of the two cathode current loops shared the total current.

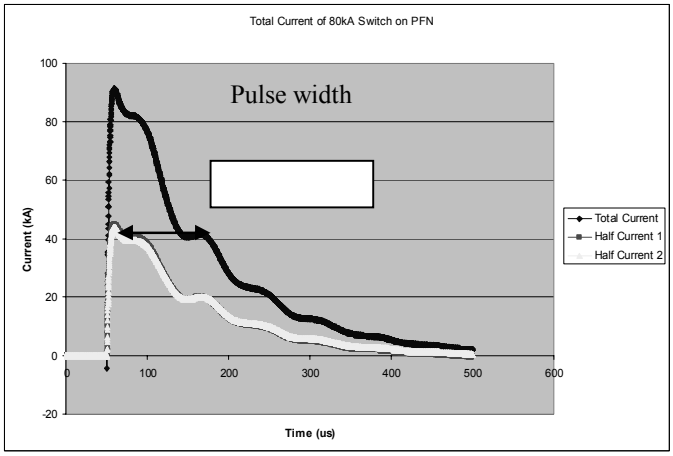

Fig. 9. Data from the failure on the PFN test shot with the total current waveform as well as how well each half of the module shared the total current.

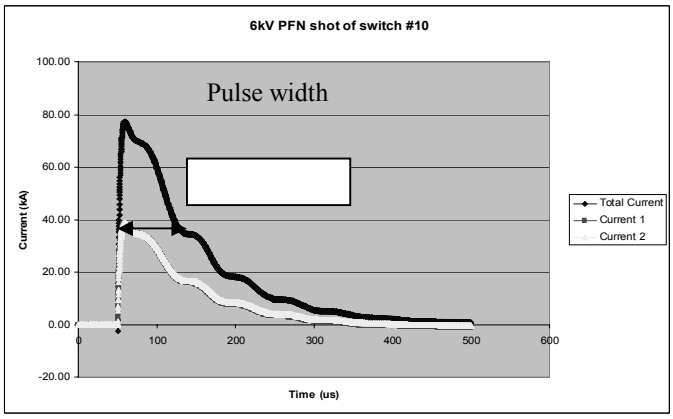

Fig. 10. Data from the successful PFN test shot with the total current waveform as well as how well each half of the module shared the total current.

into other circuits. Pulse widths are measured from the points which are 50% of the first flat region of the total current. Since it was desired for the first flat region to occur at 80 kA, we raised the input voltage until it was reached. Therefore, the pulse width was measured from the time it took for the total current waveform to cross 40 kA (Fig. 9). The total action on one device was 0.61 MA^2s. The current sharing within the modules was +/- 1% with respect to sharing the total current equally. Simultaneously, the voltage seen on each of the four layers was approximately +/- 1% from one quarter of the total voltage. Although this test shot occurred successfully, repeated shots were unsuccessful due to a short across the switch from anode to cathode caused by the strain of the 7 kV, 91.4 kA shot. This was caused by the total action on the device over the 119.7 µs pulse (0.61 MA^2s). When the pulse width was lowered to 71.9 µs and the current lowered to 77.3 kA, the action became 0.37 MA^2s (fig. 10). The rise time was 15.24 kA/µs and the peak power dissipated by the switch was 58.8 MW. To show that the device was capable of operation after the test shot, it was fired five times at this pulse width and total current successfully.

IV. Conclusions

The peak current achieved by the switch in the RLC ring down was 83.3 kA, with a 10% to 90% rise time of 3.5 µs while a 0 .263 MA^2 s without failure. The peak power of the device during this test shot was 78.7 MW (Fig. 8). On the PFN, when the pulse width was lowered to 71.9 µs and the current lowered to 77.3 kA, the action became 0.37 MA^2s (fig. 10). The rise time was 15.24 kA/µs and the peak power dissipated by the switch was 58.8 MW. Other switch tests show that if the pulse width is decreased, higher current and voltage values can be acheived In the same respect, if the total current is lowered then a longer pulse width can be achieved since the length of the pulse width is a factor in equation of action. Test beds have been assembled to better examine these theories.

V. References

[1] R.L. Thomas, H. O'Brien, W. Shaheen, S.B. Bayne, "Evaluation of a 7 KV, 80kA SGTO Module," 15th IEEE International Pulsed Power Conference, June 13-17, 2005.

[2] V. Temple, "Super' GTO's Push the Limits of Thyristor Physics," 35th Annual IEEE Power Electronics Specialists Conference, June 20-25-2004.