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THESIS

PHOTONIC FRONT-END AND COMPARATOR PROCESSOR FOR A SIGMA-DELTA MODULATOR

by

Kenny E. Escobar

September 2008

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Taking the characteristics of the real components and the experimental results, a pulse to pulse computer simulation of an oversampled first-order single-bit ΣΔ modulator was accomplished using RSoft OptSim. The performance characteristics of this subsystem were compared with the narrow-band results produced in the laboratory. In addition, a comparator processor circuit for the signal oversampling subsystem was designed and simulated in SIMUCAD SmartSpice. The analysis of the comparator processor circuit was evaluated. The lack of high-speed components limited the experimental and simulation results. With the system integrated with high-speed components, a wide-band direct digital antenna architecture can be demonstrated.

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EXECUTIVE SUMMARY

This thesis examines the role of photonics and integrated optics (IO) for use in analog-to-digital conversion in electronic warfare (EW) intercept receivers. The IO approach uses a continuous wave (CW) distributed feedback (DFB) laser diode at a peak wavelength of 1550 nm to oversample two Mach-Zehnder interferometers (MZIs). The MZIs are part of sigma-delta (ΣΔ) modulator-based analog-to-digital converter (ADC) architecture. A ring resonator accumulator is embedded within a feedback loop in the modulator to spectrally shape the quantization noise of the system. A narrow-band photonic sigma-delta digital antenna is described as a system intended to provide a proof of concept for the use of photonics technology in the sampling of wide-band radio frequency (RF) signals.

The ability to sample wide-band RF signals is an important requirement in modern electronic warfare (EW) systems where a determination of the existence of complex and often difficult to detect signals is sought. As an example, the class of signals referred to as low probability of intercept (LPI) is becoming increasingly common-place with the evolution of modern radar and communication systems. The emergence of this class has led to a concomitant demand for receivers that can provide the necessarily high sensitivity to detect these signals thereby enabling their classification in an electronic intelligence (ELINT) database or jamming using electronic attack (EA) [1].

The principal objective of the project is to study and aid in the future development of a prototype of a photonic sigma-delta wide-band cueing receiver. The prototype will digitally sample a RF signal typical of LPI emitters directly from an antenna source. By eliminating the signal down conversion stage it decreases the bothersome spurious signals, nonlinearities, and image frequencies that the mixing and filtering operations cause. The architecture features oversampling the RF signal by modulating it onto a photonic carrier followed by single bit quantization by passing the output of a total internal reflection mirror ring resonator to a high-speed comparator. The resonator, which acts as a coherent integrator, is being developed by University of California Santa

Barbara (UCSB). The modulator-resonator-comparator combination is embedded within a feedback loop which allows the quantized output to track the input RF signal as the output undergoes decimation and filtering. In this way, the advantage of sigma-delta in spectrally shaping the quantization noise outside the bandwidth of the RF input signal is maintained [1].

Taking the characteristics of the real components and the experimental results, a pulse to pulse computer simulation of an oversampled first-order single-bit ΣΔ modulator is accomplished with RSoft OptSim. The performance characteristics of this subsystem were compared with the narrow-band results produced in the laboratory. In addition, a comparator circuit for the signal oversampling subsystem was designed and simulated in SIMUCAD SmartSpice. The analysis of the comparator circuit was evaluated at narrow-band. The lack of high-speed components limited the experimental and simulation results. With the system integrated with high-speed components, a wide-band direct digital antenna architecture can be demonstrated.

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I. INTRODUCTION

A. PHOTONIC OVERSAMPLING

The transmission of coherent light through optical waveguides has been of great interest ever since the late 1960s. Through this interest emerged the concept of integrated optics, in which wires and radio links are replaced by light-waveguiding optical fibers and conventional electrical integrated circuits are replaced by miniaturized optical integrated circuits. Optical components offer a number of advantages over their electronic counterparts. The advantages include large bandwidth, use of optical sources capable of high-speed switching, low power consumption, improved reliability, insensitivity to vibration, and electromagnetic interference (EMI) [2].

Analog to digital converters (ADCs) are an essential link between analog sensor systems, such as RADAR, electronic warfare (EW), and signal intelligence (SIGINT), and high-speed digital signal processing systems in providing global information access to the warfighter. Military utilization of high performance ADC technology is diverse, spanning a wide range of sample rate and bit resolution values [3].

Electronic ADC technology has evolved and will continue to provide higher sample rates and bit resolution, but progress in advancing the electronic ADC modules has been slow, due in large part to the difficulties in fabricating the complex electronic circuitry required for very high resolution, and high sampling rate converters. Future war fighting capabilities could be severely compromised unless dramatic improvement in ADC modules is made. The photonic ADCs have several key advantages, which include more precise sampling times, narrower sampling apertures, and the ability to sample without contaminating the incident signal. They also have the potential to improve on the sample rate and bandwidth performance in present ADCs [3].

One byproduct of ADCs is quantization noise. One way to reduce quantization noise is through oversampling. It is well know that to recover a sampled analog signal the signal must be sampled at a rate greater than or equal to twice the signal frequency.

Oversampling refers to sampling the signal at a rate much greater than twice the signal frequency. Increasing the sampling frequency spreads the quantization noise over a larger bandwidth because the total amount of quantization noise remains the same over the different sampling bandwidths. Thus, oversampling reduces the quantization noise in the bandwidth of interest [4].

One ADC architecture that uses oversampling is the sigma-delta (ΣΔ) modulator based ADC. An integrated optical ΣΔ ADC uses a pulsed laser to oversample an input signal using two Mach-Zehnder interferometers (MZIs). A ring resonator accumulator is embedded within a feedback loop around a single-bit quantizer to spectrally shape the quantization noise to fall outside the signal band of interest. Decimation filtering is used to remove the high frequency quantization noise without affecting the signal and to construct the input signal with high resolution [2].

ADCs are critical components in the development of advanced digital receivers. Wide bandwidth and high resolution ADCs will allow direct quantization of the sensor signal at RF frequencies, thereby eliminating the need for analog down conversion stages. Direct conversion also allows the ADC to be placed closer to the receiver front-end. With the digital interface closer to the antenna in military receivers, costly temperature sensitive components that introduce distortions and require considerable calibration will be reduced [3]. Photonic ADCs utilizing ΣΔ modulator based technology have been extensively studied and are documented in [3], [7]. The initial documentation used in this thesis came from a conference paper [5] of work performed at the Naval Postgraduate School. This thesis examines the construction and experimental testing of the photonic processors at the antenna. In addition, the design and simulation results of the post-detection mixed-signal comparator circuit are shown.

B. PRINCIPAL CONTRIBUTIONS

The first step in this thesis was to experimentally characterize the distributed feedback (DFB) laser. The characterization of the laser consisted of determining the peak wavelength, output power, and frequency linewidth. Additionally, the MZIs parameters were gathered experimentally to confirm the manufacture's specifications. These

parameters were incorporated in the simulation to better replicate the experimental results. Due to limitations in processing power and memory constraints, experiments were conducted at narrow-band. The sampling frequency was reduced to a manageable level down to the Megahertz region for a sampling frequency of $f_s \simeq 5MHz$.

Next, a computer simulation of the ΣΔ modulator architecture was desired. MATLAB SIMULINK was first considered, but shortly abandoned. OptSim is an optical simulation software package produced by RSoft which was examined to simulate the photonic components of ΣΔ modulator. The software was installed and its capabilities evaluated. The software was used to construct the front-end oversampling architecture. Using a continuous wave (CW) laser model to represent a DFB laser with the parameters gathered in the laboratory, a laser model was constructed. Models of the MZIs, optical beam splitters, and photodetectors were also developed in OptSim to match the devices used in the laboratory. The results of the computer simulation were compared to the experimental results gathered in the laboratory.

Subsequently, the design of the post detection comparator processor was started. The comparator processor circuit design consist of two high-speed comparators, four *nor* gates, and a set-reset (S-R) latch. This comparator processor is a hybrid design in that its output is a digital signal but its inputs are continuous analog signals. Time was spent evaluating high-speed comparators and emitter coupled logic (ECL) *nor* gates from various manufactures. Real component parameters were desired for the simulation. A SPICE macromodel of a high-speed comparator was obtained from Maxim Integrated Products. A circuit model for the *nor* gate was developed using SPICE switches. The processor was designed and simulated in SIMUCAD SmartSpice. The circuit design serves as a proof of concept model for future development in wide-band sampling. Results of the simulation are presented.

C. THESIS OUTLINE

In Chapter II, a photonics overview of the ΣΔ ADC architecture is presented, theory of oversampling is discussed, and each optical component of the ΣΔ modulator ADC is discussed in detail.

In Chapter III, the means in which the parameters of the laser and MZIs were obtained are examined. The parameters gathered in the laboratory experiment were used for the proper simulation of the optical components discussed in Chapter IV.

In Chapter IV, a computer simulation of the oversampled integrated optical ΣΔ modulator is developed, and the components are discussed. In addition, the simulation results are compared to the laboratory results.

In Chapter V, a simulation of the mixed signal comparator processor circuit is developed and the simulation results observed. A generic input signal is constructed as proof of concept to confirm the viability of the circuit model for wide-band applications.

Finally, Chapter VI offers recommendations for improving the performance of the system and for ongoing development of the wide-band receiver.

II. PHOTONIC SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER

A. OVERSAMPLING THEORY

1. Introduction

Oversampling methods have recently become popular because they avoid many of the difficulties encountered with conventional methods for analog-to-digital (A/D) and digital-to-analog (D/A) conversion [6]. Conventional ADC and DAC are often difficult to implement in fine line very large scale integration (VLSI) technology. These difficulties arise because conventional methods need precise analog components in their filters and conversion circuits and because their circuits can be very vulnerable to noise and interference. The virtue of the conventional methods is their use of a low sampling frequency, usually the Nyquist rate of the signal. The Nyquist sampling theorem is the conventional approach to sampling analog signals at the signal bandwidth or, in other words, at twice the highest frequency contained in the signal of interest.

Oversampling converters can use simple and relatively high tolerance analog components to achieve high resolution, but they require fast and complex digital signal processing stages. These converters modulate the analog signal into a simple code, usually single bit words, at a frequency much higher than the Nyquist rate. Additionally, oversampling converters make extensive use of digital signal processing; taking advantage of the fact that fine line VLSI is better suited for providing fast digital circuits than for providing precise analog circuits. Because their sampling rate usually needs to be several orders of magnitude higher than the Nyquist rate, oversampling methods are best suited for relatively low frequency signals. Another important difference between conventional converters and oversampling ones is that with conventional converters there is a one-to-one correspondence between input and output sample values. Hence, one can describe their accuracy by comparing the values of corresponding input and output samples [7].

Such limitations can be addressed using an oversampling approach which samples above the Nyquist rate. One approach that involves the use of oversampling methods is known as ΣΔ modulation. ΣΔ modulators employ oversampling and integration and feedback in iterative loops to obtain high resolution ADCs. The idea is to digitize the signal through the use of a coarse quantizer, and cause the output to oscillate between the quantized levels at high-speed so that its average value over the Nyquist interval was an accurate representation of the sampled value. The quantizers for these interpolating converters utilize a noise-shaping technique that measures the quantization error in one sample and subtracts it from the next input sample value [2].

The sampling theorem states that the sampling frequency of a signal must be at least twice the signal frequency in order to recover the sampled signal without distortion. When a signal is sampled its input spectrum is copied and mirrored at multiples of the sampling frequency f_S. Figure 1a shows the spectrum of a sampled signal when the sampling frequency f_S is less than twice the input signal frequency $2f_0$. The shaded area on the plot shows aliasing which results when the sampling theorem is violated. Recovering a signal contaminated with aliasing results in a distorted output signal. Figure 1b shows the spectrum of an oversampled signal. The oversampling process puts the entire input bandwidth at less than $f_S/2$, thus avoiding aliasing [8].

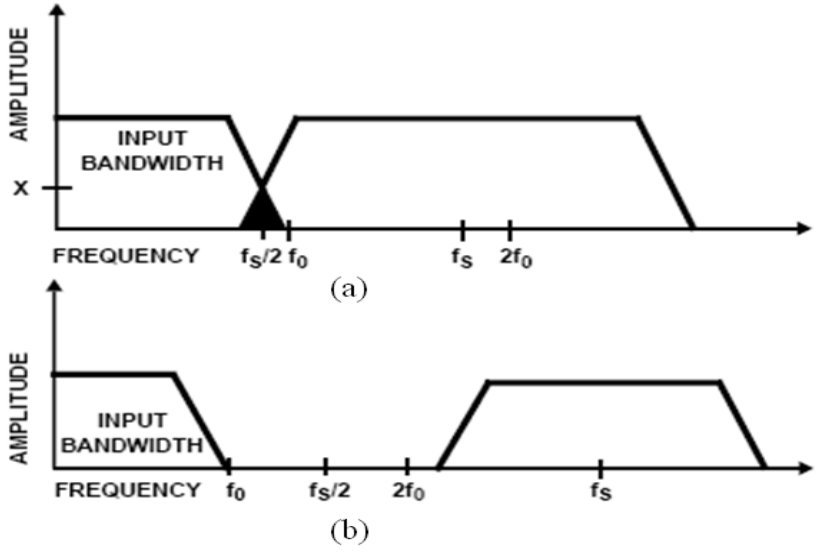


Figure 1. Spectrum of (a) Undersampled signal, (b) Oversampled signal. From [8].

In practice, by selecting a suitably large sampling frequency a broader range of emitters can be sampled with narrow-band emitters at high oversampling ratio (OSRs) and wide-band emitters at lower OSRs [1]. The following two sections present a brief overview of quantization noise theory and signal sampling theory for a ΣΔ modulator.

2. Quantization

At the heart of all digital modulators is amplitude quantization and sampling in time. Periodic sampling above the Nyquist rate is not necessarily a source of distortion. But, quantization is a source taken into account when designing modulators.

Consider a uniform quantization that rounds off a continuous amplitude signal x to odd integers in the range $-5 \le x \le 5$. For convenient illustration, assume a level spacing of $\Delta = 2$. The quantized signal y can be represented as a linear function Gx with an error e, such that:

$$y = Gx + e \tag{1}$$

The slope G is a gain term passing through the center of the quantization characteristic such that for non-saturating signals input to the quantizer (i.e., $-6 \le x \le 6$), the error is bounded by $\pm\Delta/2$.

The error is completely defined by the input. If the input changes randomly between samples with amplitude comparable or greater than the level spacing, and without causing saturation, then the error is uncorrelated from sample to sample and has equal probability of taking any value in the range $\pm\Delta/2$. If it is further assumed that the error is statistically independent of the signal, then it can be considered as noise, allowing some important properties of the modulator to be deduced. In many cases, experimental measurements have confirmed these properties, but there are two important possible exceptions: constant input, and regularly changing input based on multiples and factors of the step size between sample times as can happen in feedback circuits.

For a uniformly distributed quantization error e having equal probability of taking any value in the range $\pm\Delta/2$, its mean square value is:

$$e^2{}_{RMS} = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 \, de = \frac{\Delta^2}{12} \tag{2}$$

When a quantized signal is sampled at frequency $f_s = 1/T_s$, all of its power folds into the frequency band $0 \le f \le f_s/2$ (assuming the one-sided power spectral density representation where all the power is in the positive range of frequencies).

For white quantization noise, the power spectral density of the sampled noise is:

$$E(f) = e_{RMS}\sqrt{\frac{2}{f_s}} = e_{RMS}\sqrt{2T_s} \tag{3}$$

This result can be applied to analyze examples of oversampling modulators. For example, consider pulse code modulation (PCM). A signal extant in the frequency band, $0 \le f < f_0$, to which a dither signal contained within the band $f_0 \le f < f_s/2$ is added, is pulse code modulated at f_s. The OSR is the integer ratio of the sampling frequency f_s to the Nyquist frequency $2f_0$:

$$\text{OSR} = \frac{f_s}{2f_0} = \frac{sampling\ \ frequency}{Nyquist\ \ frequency} \tag{4}$$

If the dither signal is sufficiently large and variable to whiten and decorrelate the quantization error, the noise power that falls into the signal band will be given by:

$$n_0^2 = \int_0^{f_0} e^2(f)df = e_{RMS}^2(2f_0T_s) = \frac{e_{RMS}^2}{\text{OSR}} \tag{5}$$

This is the well-known result that oversampling reduces the in-band RMS noise from ordinary quantization by the square root of the oversampling ratio. Hence, each doubling of the sampling frequency decreases the in-band noise by 3dB and increases the resolution by one half of a bit [1], [7].

3. Sigma-Delta Modulation

The work on sigma-delta modulation was developed as an extension to the well established delta modulation. A more thorough description on delta modulation is found in [9]. The name sigma-delta modulator comes from putting the integrator (sigma) in front of the delta modulator, as shown in Figure 2. Figure 2 shows a simple block

diagram of a first order sigma delta ADC. The input signal X comes into the modulator via a summing junction. It then passes through the integrator which feeds a comparator that acts as a one-bit quantizer. The comparator output is fed back to the input summing junction via a one-bit DAC, and it also passes through the digital filter and emerges at the output of the converter. The feedback loop forces the average of the signal W to be equal to the input signal X [8].

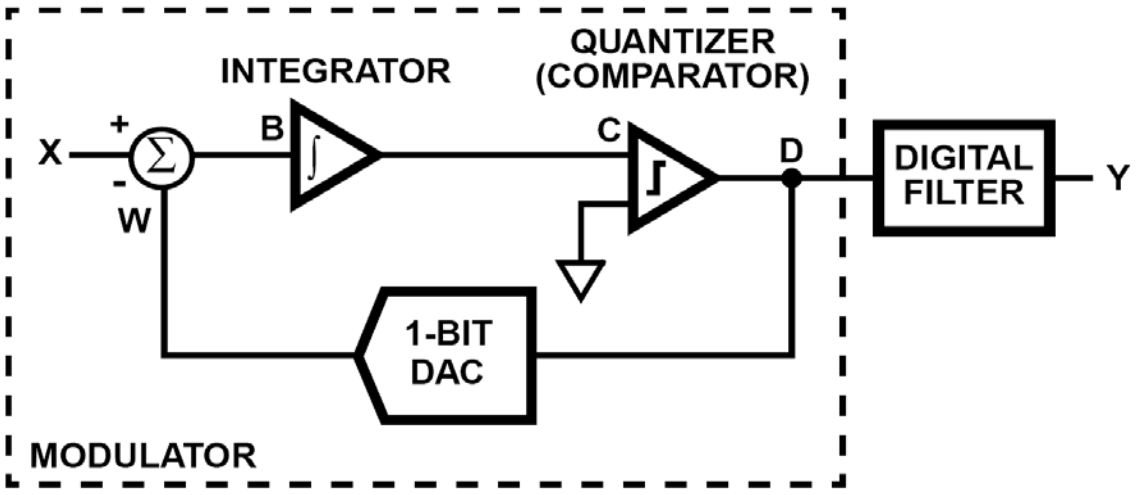


Figure 2. First Order ΣΔ ADC Block Diagram. From [8].

A ΣΔ modulator employing first-order feedback is a more efficient oversampling quantizer. Assume a uniform quantizer with unity gain *G*. The input signal is integrated prior to quantization where the output is fed back through a DAC to be subtracted from the input signal. The feedback forces the average value of the quantized signal to track the average input. Any persistent difference between them accumulates in the integrator and eventually corrects itself. A time-varying input signal, such as a ramp will be quantized over number of levels. The quantized signal oscillates between two adjacent quantization levels that are adjacent to the input value in such a way that the local quantized average equals the average input value [1].

Using the nomenclature of equation (1) with unity quantization gain *G* and quantization error *e*, the ΣΔ modulator can be analyzed. In a sampled-data circuit, integration by accumulation in a ΣΔ modulator has unit gain. The output of the accumulator *w* is the delayed input signal minus the signal's quantization error.

$$w_i = x_{i-1} - e_{i-1} \tag{6}$$

The quantized signal is

$$y_i = x_{i-1} + (e_i - e_{i-1}) \tag{7}$$

From these expressions, it is apparent that the ΣΔ modulator differentiates the quantization error, making the modulation error the first difference of the quantization error while leaving the signal unchanged, except for delay.

The effective resolution of the modulator requires a sufficiently variable input signal such that the error *e* behaves as uncorrelated white noise. The spectral density of the modulation noise

$$n_i = e_i - e_{i-1} \tag{8}$$

may then be expressed as

$$N(f) = E(f)\left|1 - \varepsilon^{-j\omega T_s}\right| = 2e_{RMS}\sqrt{2T_s}\,\sin\left(\frac{\omega T_s}{2}\right) \tag{9}$$

where $\omega = 2\pi f$.

The total noise power in the signal band is

$$n_0^2 = \int_0^{f_0} \left|N(f)\right|^2 df \approx e_{RMS}^2 \frac{\pi^2}{3}(2f_0T_s)^3, f_s^2 >> f_0^2 \ , \tag{10}$$

and its RMS value is

$$n_0 \approx e_{RMS}\frac{\pi}{\sqrt{3}}(2f_0T_s)^{3/2} = e_{RMS}\frac{\pi}{\sqrt{3}}(\mathrm{OSR})^{-3/2} \tag{11}$$

That is for each doubling of the oversampling ratio in this modulator, the quantization noise is reduced by 9dB and the resolution is increased by 1.5 bits.

The improvement in resolution requires that the modulated signal is decimated to the Nyquist rate with a precisely tuned digital filter. Without decimation, high frequency components of the noise will corrupt the achievable resolution when the noise is sampled at the Nyquist rate. There are various schemes for achieving decimation filtering where the achievable noise rejection generally varies inversely with ease of implementation [1], [7]. Decimation filtering will be covered in the next section.

4. Decimation Filter

The output of the ΣΔ modulator consists of out-of-band components, modulation noise, circuit noise, and interference. The decimation filter shown in Figure 3 serves to attenuate the entire out-of-band energy of the modulator signal so that it may be resampled at the Nyquist rate without incurring significant noise penalty due to aliasing. The decimation filter removes all the modulation noise and extracts the digitized signal. A fairly simple filter would suffice to remove the modulation noise; however, low pass filters are often needed to remove out of band components of the signal. This is best accomplished in multiple stages of filtering and resampling [7]. The first stage of decimation removes the modulation noise, which dominates at higher frequencies and down samples the signal to some intermediate sampling frequency. A second low pass filter is then used to attenuate the out-of-band components before the signal is again resampled at the Nyquist rate. As the signal propagates through the filters and resampling stages, the word length increases to preserve the resolution of the modulator [10]. A more detailed description can be found in [6], [7].

B. PHOTONIC ΣΔ OVERVIEW

The block diagram of a first-order, single-bit, integrated optical ΣΔ ADC architecture is shown in Figure 3.

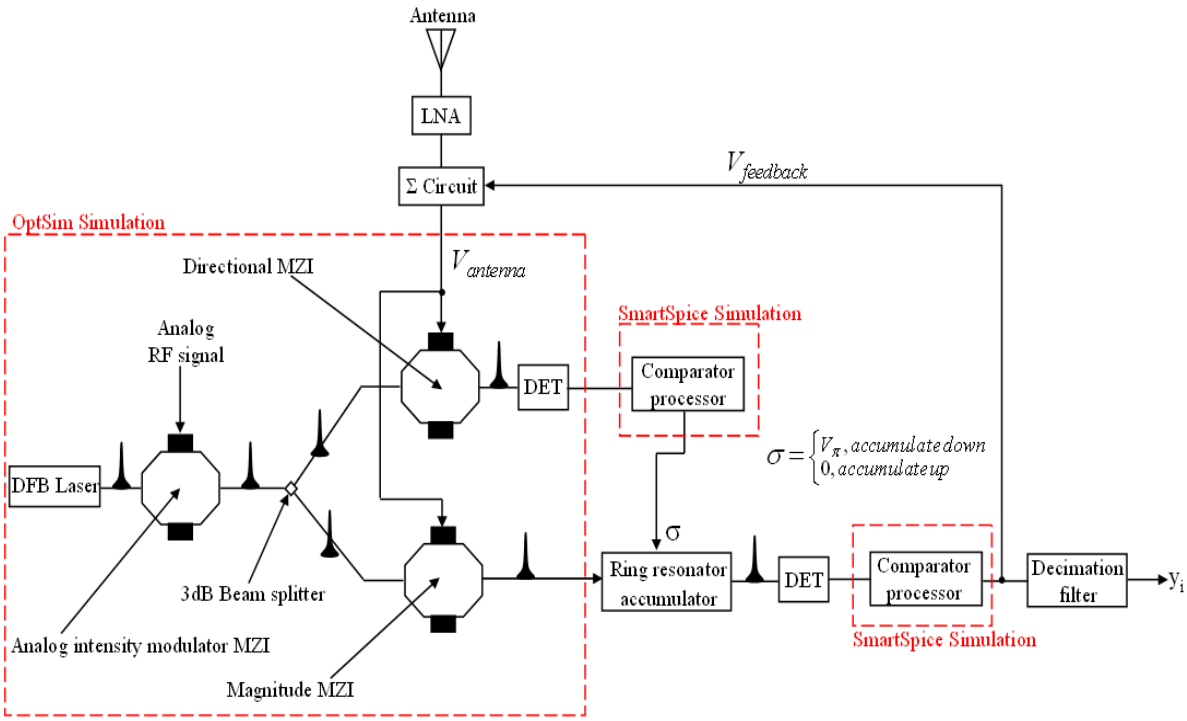


Figure 3. Integrated optical first-order single-bit ΣΔ Modulator ADC.

The ADC is a coherent device that relies on oversampling an antenna signal $V_{antenna}$ at two MZIs with a high pulse repetition frequency (PRF) laser. The RF antenna signal detection is noise limited by the largest of either the noise added by the low noise amplifier (LNA) or the photonic detector's noise equivalent power. The dynamic range for a first-order optical ΣΔ modulator is defined by equation (12). For a single-bit ΣΔ modulator n would equal 1 and the OSR is defined by equation (4)

$$SNR = 2^{n-1}\sqrt{\left(\frac{18OSR^3}{\pi^2}\right)}. \tag{12}$$

Expressed in decibels

$$SNR(dB) = 6.02(n) - 3.41 + 30\log(OSR). \tag{13}$$

An advantage of the MZIs is that they have a large power handling capability with a maximum RF input of 27dBm (0.5Watts) with a 50Ω load. The accumulation of the sampled signal occurs prior to the output detector and quantizer (comparator) using a ring resonator. Since light intensity can only be positive, one MZI is used to sample and encode the antenna signal magnitude for accumulation in the resonator. The other MZI is

used to sample the antenna signal polarity, the sampled signal's direction for accumulation. The MZIs are also used to subtract the output comparator's feedback signal $V_{feedback}$ from the antenna signal $V_{antenna}$, via the summing circuit. The accumulation of the optical pulse from the magnitude MZI is accomplished via recirculation through the ring resonator and coupling the polarity information σ from the direction MZI. For σ = 0, constructive interference occurs within the accumulator, accumulate up. For $\sigma = V_{\pi}$, destructive interference occurs, accumulate down [2]. The output pulse from the ring resonator is detected and amplitude analyzed with a high-speed comparator. The decimation filter is then applied to the comparator output, to construct the signal with high resolution sampled at the Nyquist frequency. In the section that follows, the optical components of the ΣΔ ADC are described. Optical components include the laser, MZIs, optical beam splitter, ring resonator, and photodetector.

C. OPTICAL COMPONENTS

The following is a detailed description of the individual components of the optical ΣΔ modulator ADC.

1. Laser

a. Distributed Feedback Laser

The laser type used for initial laboratory experiments and software simulations was a DFB laser diode (LD). The DFB continuous wave (CW) semiconductor laser is a single mode devices operating at 1550nm. There are favorable properties at this wavelength including low fiber attenuation, applicability of dense wavelength division multiplexing techniques, and erbium-doped fiber amplifiers (EDFAs). These DFB laser devices are also useful in microwave photonic signal processing for the same reasons. In addition, they manifest Gaussian power probability distribution, which is required to represent the statistical nature of target cross-section in electronic warfare (EW) receivers. One drawback in the utilization of DFB laser devices

in microwave photonic signal processing is that they are coherent, *i.e.* they have narrow linewidth. Optical linewidth refers to the optical phase fluctuation of the lasing longitudinal modes.

Unlike telecommunication applications, photonic processing of microwave signals based on differential delays requires an incoherent optical carrier. To be absolutely accurate, the coherence time of the optical carrier must be shorter than the shortest differential delay in the photonic signal processor. Therefore, in order to utilize DFB laser devices in microwave photonic signal processing, their linewidth has to be broadened to reduce their coherence [11].

b. Mode-Locked Laser

Mode-locked lasers have been the laser of choice for previous thesis research projects in this area. The reason has been that in a typical mode-locked laser cavity there are many modes operating simultaneously. The relative phase of these modes is often random and incoherent causing the light from the laser to fluctuate as the modes interact constructively and destructively. Mode-locking is achieved when distinct longitudinal modes of a laser, all having slightly different frequencies, are combined in phase. The peak amplitudes of these oscillating modes, together in phase, periodically combine constructively to form a mode-locked pulse [10]. The pulses are formed when sine waves in multiples of 2π are added in phase with one another so all their phases are zero at the same spatial locations. When added together they produce a total field amplitude. Squaring the amplitude gives the intensity and characteristic pulsed nature of a mode-locked laser pulse [10].

2. Mach-Zehnder Interferometers

The MZIs are used to efficiently couple the RF antenna signal into the optical domain and to subtract the feedback signal coming from the comparator $\left(V_{antenna} - V_{feedback}\right)$. The optical input to the MZIs is the pulsed laser output. Figure 4, shows a schematic diagram of an MZI. The MZI consists of a 3-dB intensity beam splitter, two optical waveguides, electrodes, and an intensity combiner. The 3-dB

intensity beam splitter separates the laser pulses into the two separate waveguides. The electrodes, which are positioned along the optical waveguide lengths, receive the antenna, feedback, and DC bias voltages and create electric fields in the optical waveguide. Each path of the MZI is affected separately, so that, when the pulses are recombined at the MZI output, an interference occurs. The voltages are applied separately to each path with opposite polarity (push-pull configuration), creating a voltage difference operation (for example, that antenna voltage is applied to one waveguide and that feedback voltage is applied to the other). The applied electric field changes the propagation coefficient of the laser pulse by changing the index of refraction of the optical waveguides as a function of the voltage. The two waveguides are then recombined at the output, resulting in an output laser pulse that is amplitude modulated by the analog voltage due to the constructive and destructive interference. If no voltage is applied to the electrodes, the pulses recombine coherently for a maximum output.

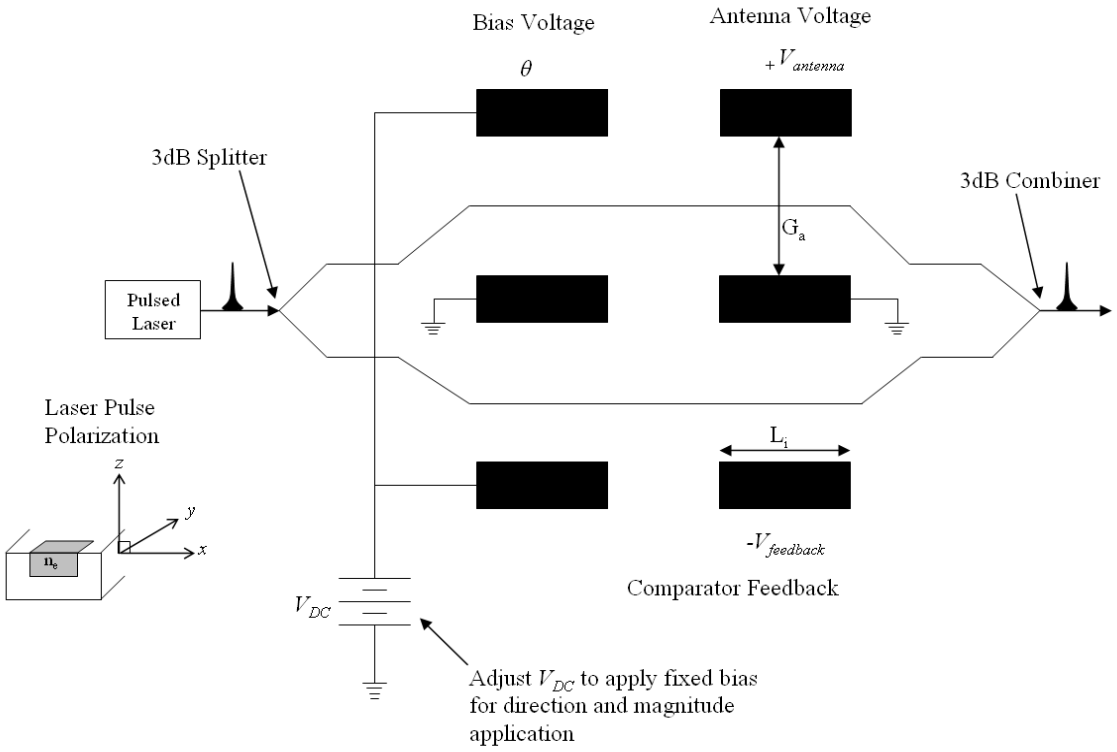


Figure 4. Schematic diagram of a transverse $LiNbO_3$ MZI subtracting the antenna signal from the comparator feedback. After [5].

The transmissivity of an MZI, ratio of output intensity to input intensity, is a function of the phase difference $\Delta\phi$ between the waveguide paths:

$$H_{MZI} = \frac{I_{out}}{I_{in}} = \frac{1}{2} + \frac{1}{2}\cos\left[\Delta\phi(v) + \theta\right], \tag{14}$$

where I_{out} and I_{in} are the output and input light intensities, respectively. The phase angle θ is a DC bias term that is used to adjust the quadrature point of the interferometer. A DC bias is applied separately to create both the magnitude and direction MZI transmissivity functions. As shown in Figure 4, the pulsed laser light is assumed to be polarized along the crystallographic z axis, so the laser pulse sees the extraordinary index of refraction n_e and the strong electro-optic tensor coefficient r_{33}. Consequently the optical device is characterized as a transverse interferometer vice a longitudinal interferometer. For lithium niobate, $n_e^3 r_{33} = 3.28x10^{-4}\ \mu m/V$. This configuration allows a smaller voltage to affect the maximum phase change of π, making the device more efficient. The expression often used for the voltage-dependent phase shift in a transverse lithium niobate push-pull interferometer is

$$\Delta\phi(v) = \frac{2\pi\, n_e^3\, r_{33}\, \Gamma\, L_i\, v(t)}{G_a\, \lambda_L}, \tag{15}$$

where $v(t) = V_{antenna} - V_{feedback}$, Γ is the electro-optic overlap parameter, G_a is the interelectrode gap (m), L_i is the electrode (m), and λ_L is the laser wavelength (m). In terms of V_π (the voltage required to shift the phase by π radians), the phase shift is

$$\Delta\phi(v) = \frac{\pi\, v(t)}{V_\pi}, \tag{16}$$

where

$$V_\pi = \frac{G_a\, \lambda_L}{2\, L_i\, n_e^3\, r_{33}\, \Gamma}. \tag{17}$$

For example, Table 1 shows the values for a typical $LiNbO_3$ modulator.

G_a	Interelectrode gap	3μm
λ_L	Wavelength of laser	1550nm
L_i	Electrode length	14mm
n_e	Index of refraction	1.001
r_{33}	Electro-optic coefficient	30.8 x 10^{-12} m/V
Γ	Electrical optical overlap parameter	0.5

Table 1. Typical $LiNbO_3$ Modulator Parameters.

Using the device parameters in Table 1 $V_\pi = 10.78\,V$ the value of V_π closely resembles the DC port V_π parameter of 10.6 V specified by the manufacturer.

3. Optical Beam Splitter

Beam splitters are optical components that split incident beams into reflected and transmitted rays [12]. In the architecture presented in Figure 3 a Y-splitter is used. The function of the Y-splitter waveguide is to feed each guide of the directional and magnitude MZI with optical waves that are exactly equal in amplitude and phase. If these waves are exactly equal, then all even order derivatives are zero at zero voltage applied to the modulator, and thus all even order harmonics and even order intermodulation products are identically zero. However, if the Y-splitter is not exactly symmetric, there can be a fractional difference delta in the intensities of the two waves and a difference in their phases [13]. This component is critical for proper modulation.

4. Ring Resonator

The design and test of an integrated photonic dual-coupler micro-ring resonator in *indium gallium arsenide phosphide / indium phosphide* (InGaAsP/InP) is intended to replace the bulky fiber lattice accumulator presented on previous thesis projects [10], [14]. The ring resonator is being investigated by Dr. Nadir Dagli at the University of California Santa Barbara. The ring resonator design layout being studied is shown in Figure 5.

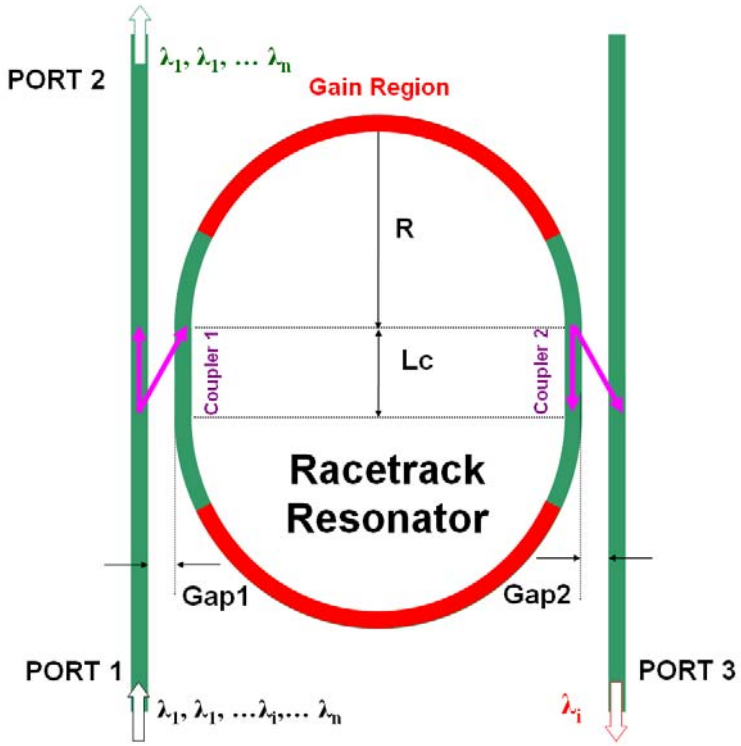


Figure 5. Ring Resonator Accumulator Design Model Presented by Dr. Nadir Dagli.

As shown in Figure 5, multiple wavelengths input into port 1 will be partially coupled into the ring through coupler 1. The optical wave in the ring will be partially coupled into the straight waveguide through coupler 2 and outputs from port 3.

If the wavelength, for example, λ_i satisfies the resonant condition, that is,

$$n_{eff} L = m\lambda_i \tag{18}$$

the coupling of the wave with wavelength λ_i will be enhanced and all others will be suppressed. In the resonator design only λ_i will be dropped from port 3, while the rest of the wavelengths will pass through and output from port 2. In equation (18), n_{eff} is the effective index of the bending waveguide, L is length of the ring, and m is an integer.

Free spectral range (FSR) is one of the key specifications of the ring resonator. It is defined as:

$$FSR = \frac{\lambda_i^2}{n_{eff} L} \simeq \frac{\lambda_i^2}{n_{eff}\left(2\pi R + 2L_c\right)} \tag{19}$$

where R is the ring radius and L_c is the coupler length. Because the FSR is inversely proportional to the size of the ring resonator, the ring must be small in order to achieve a high FSR. For instance, the ring radius should only be approximately 8μm if its is build on *InGaAsP/InP* $\left(n_{eff} \sim 3.3\right)$ with $FSR = 10nm$ and $\lambda_i = 1550nm$, assuming the coupler length is about 10μm each. A more in-depth look at the ring resonator can be found in [15].

5. Photodetectors

When the light exits the ring resonator structure, the electric field of the laser pulse must be detected and converted into a voltage before entering the output comparator circuit. The architecture presented in Figure 3 depicts two photodetectors, one at the output of the directional MZI, and the other at the output of the ring resonator. A photodetector converts photons to electric current. That is, a photon strikes a semiconductor and frees a hole or electron for conduction. The absorption of photons by a material results in higher energy level then mobile charges carriers are created. An external electric field produces a current [12].

The photodetectors used in the laboratory are high-speed photodetectors with a rise time of 12ps, a bandwidth of 26GHz, and a maximum continuous wave input power of 1mW.

D. SUMMARY

There are two techniques important to the operation of ADCs, oversampling of the analog signal and ΣΔ modulation. The first, technique, oversampling, spreads the quantization noise over a wider frequency band thus reducing the in-band quantization noise. The second technique, ΣΔ modulation, has the added benefit of shaping the

quantization noise such that a majority of the remaining in-band quantization noise is greatly attenuated. The second technique is the basis behind the design of the electro-optical ΣΔ modulator ADC architecture.

III. CHARACTERIZATION OF DFB LASER AND MZI

A. DISTRIBUTED FEEDBACK LASER DIODE

The EM4 (part number EM253-080-053) high power DFB is a CW *InGaAsP/InP* multi-quantum well (MQW) laser diode. The module is ideal in applications where high power, low input resistance and stable polarization maintaining (PM) fiber properties are needed. The laser diode is housed within an integrated circuit (IC) of the butterfly configuration which also contains a monitor photodiode, thermistor, and inputs for a thermo-electric cooler (TEC). For more information on the EM4 DFB laser a datasheet can be found in Appendix B.

The first parameter needed for the simulation of the DFB laser was the peak wavelength of the laser output. The specifications of the laser state the wavelength to be 1550nm. This parameter was confirmed in the laboratory using an optical spectrum analyzer. Figure 6 shows the spectrum of the laser output, the x-axis is in (nm) and the wavelength λ is shown to be 1549.9nm.

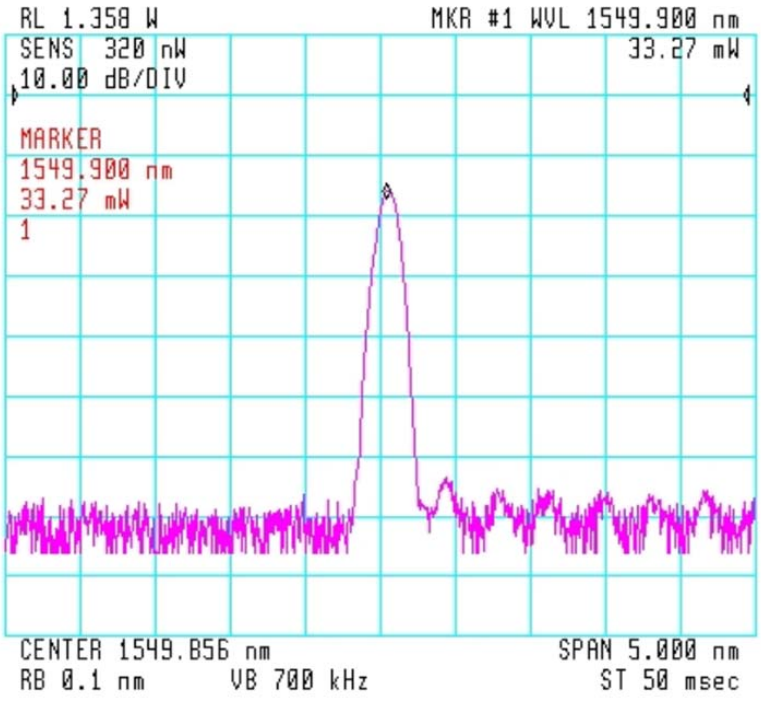


Figure 6. Optical Spectrum of the DFB Laser Output.

In order to verify the maximum optical output power of the DFB laser. The output power was measured by gradually increasing the input drive current of the laser and tabulating the output power of the laser diode. The output connector of the laser was connected to a photodetector that was connected to an digital multi-meter. The photodetector converts light energy to electric power. Thus, the output of the photodetector was displayed on a digital multi-meter. A plot of the tabulated results, optical output power versus drive current, is shown in Figure 7. These values are within the expected range of the laser based on the manufacturer's specifications.

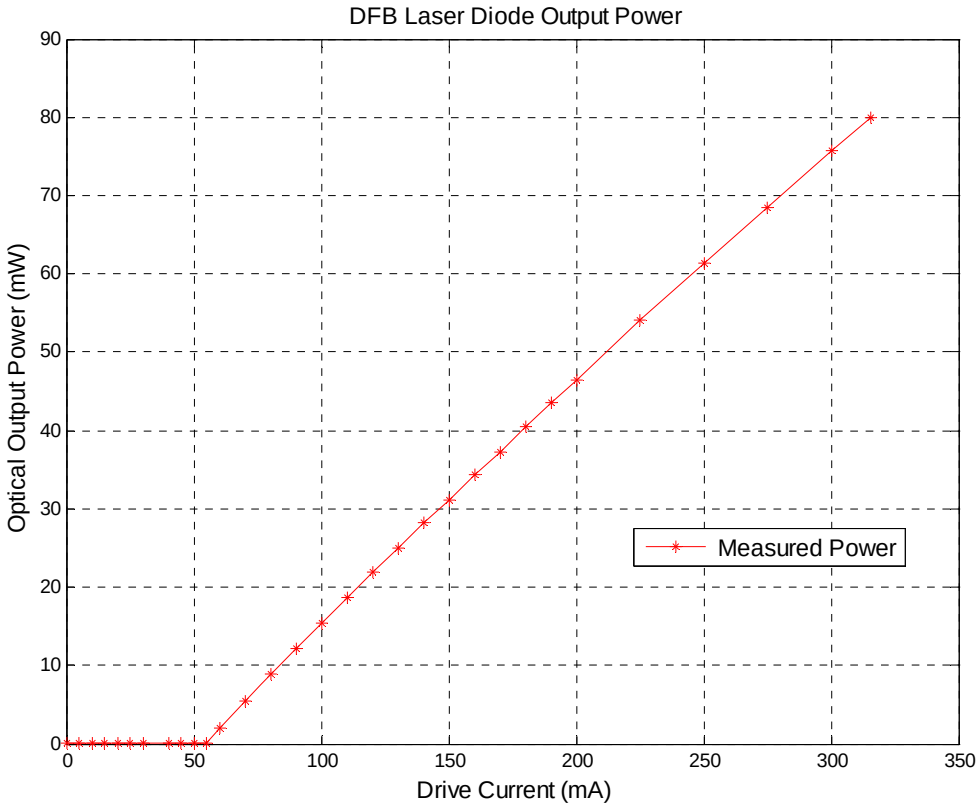


Figure 7. DFB Laser Diode Optical Output Power versus Drive Current.

The next key parameter needed for proper simulation of the laser was the full width half maximum (FWHM) frequency linewidth, $\Delta\nu$. The linewidth of a DFB diode laser is generally too narrow to measure directly using an optical spectrum analyzer. Instead this parameter is measured indirectly using an RF spectrum analyzer. The setup for this measurement is shown in Figure 8.

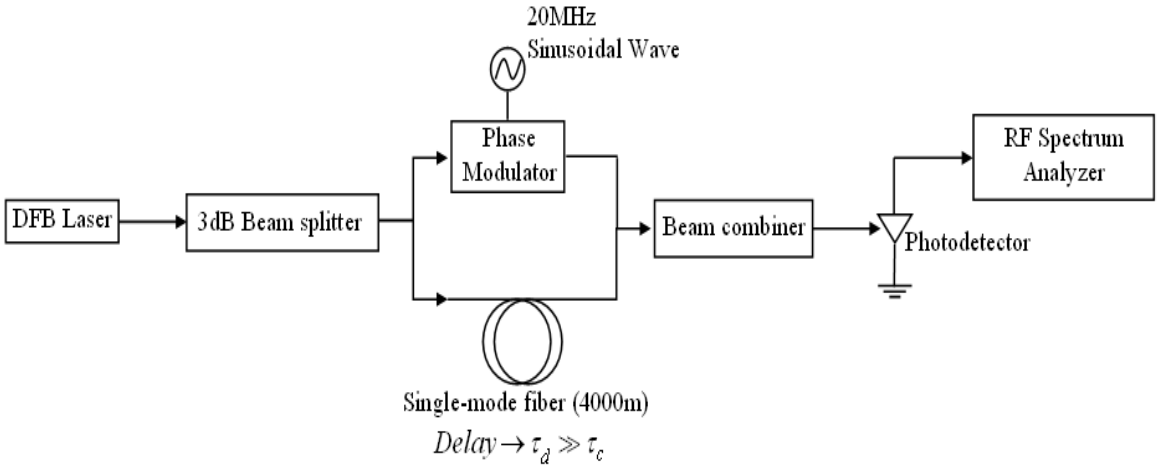


Figure 8. Block Diagram of Delayed Self Heterodyning Interferometer Linewidth Measurement Technique.

The CW output of the DFB laser is input to 3dB optical beam splitter with one path fed through a long fiber delay (4000m) and the other fed through a lithium niobate (LiNbO3) travelling wave phase modulator. The two paths are recombined (50/50) and then fed to a high-speed photodetector. The electronic output of the photodetector is fed to an RF spectrum analyzer which displays a power spectrum of the interfering waves. The FWHM of this power spectrum is equivalent to the spectral linewidth of the laser. The power spectrum represents a Lorentzian distribution of the photons undergoing spontaneous emission inside the laser, which is the principle cause of linewidth broadening in a laser [1].

The set-up shown in Figure 8 is known as a delayed self heterodyning interferometer (DSHI). Numerous other examples of this measurement technique may be found in the scientific literature [11], [16].

The phase modulator as shown in Figure 8 is used to inject a high frequency component onto the optical carrier to enable the power spectrum to be shifted away from DC, where the FWHM cannot be accurately measured. In the measurements described here, the phase modulator was supplied a 20MHz sinusoid. The long delay is chosen to be larger than the expected value of coherence length, such that delay time is much

greater than the coherence time $(\tau_d \gg \tau_c)$ [1]. This ensures the delayed waves at the input of the combiner are uncorrelated with the direct waves.

A linewidth measurement is illustrated in Figure 9. From Figure 9 it can be seen that the measured FWHM frequency linewidth was 130kHz for the DFB laser. The video trace of the spectrum analyzer was averaged over 999 samples and applied over a span of 10MHz. Resolution, video bandwidth, and sweep time was all automatically configured.

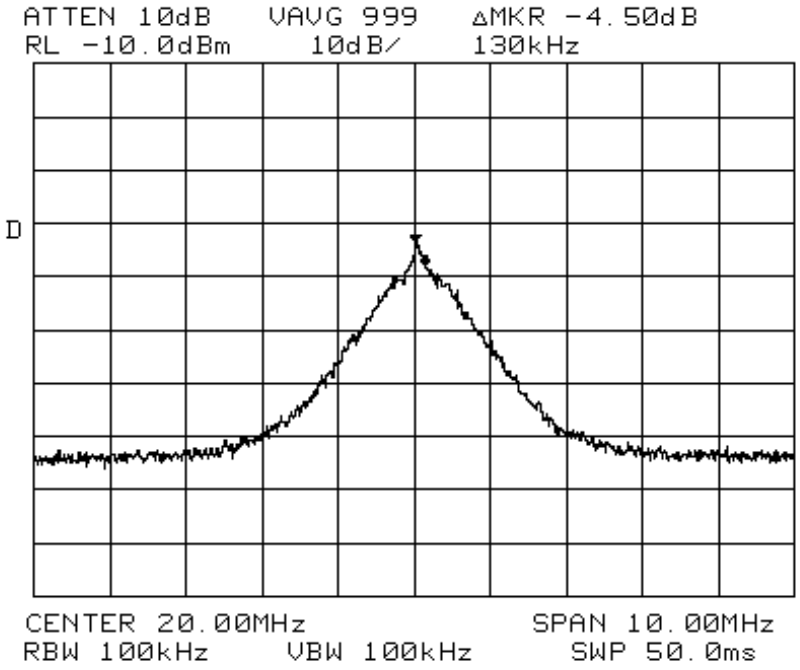


Figure 9. Linewidth measurement using DSHI technique as displayed on RF Spectrum Analyzer.

B. MACH-ZEHNDER INTERFEROMETERS

Three MZIs are used in the ΣΔ modulator architecture illustrated in Figure 3. In the architecture, the first MZI functions as an analog intensity modulator (AIM) and is used to externally switch the CW laser *on* and *off*. The other two MZIs function as Mach-Zehnder Modulators (MZMs) and are used to modulate the sampled RF signal.

The first characteristic parameter needed for simulation of the MZIs is the voltage required to drive the signal from its minimum to its maximum value. This voltage swing is refer to as V_π.

The second characteristic is the ability of the MZI to pulse the CW laser. This is a critical step in the ΣΔ modulation process as pulsing the laser is required to sample the incoming RF signal. This is referred to as the on-off extinction ratio of the modulator.

The third characterization of the MZIs was done by applying a DC bias voltage to the magnitude and direction components of the RF signal in order to achieve the desired transmissivity. The bias configuration for the MZI # 2, the direction quantization, is preset. Bias configuration of MZI # 3 requires shifting by $V_\pi/2$ for magnitude quantization. Table 2 shows the characteristics of the three MZIs. For a detailed explanation of the characterization process of the MZIs used in the laboratory, refer to [17].

Parameters	Specified			Measured		
S/N 443383 is #1 S/N 148163D is #2 S/N 148163E is #3	AIM 1	MZM 2	MZM 3	AIM 1	MZM 2	MZM 3
Insertion Loss at quadrature (dB)	6	6.9	6.8	6	5.2	5.6
On-Off Extinction Ratio (dB)	20 (min.) 27 (typ.)	27	27	20 (min.) 26 (typ.)	24	24
RF port V_π (V)	4.2 (DC) 5.3 (1GHz)	2.9	2.9	4.2 (20KHz) 4.6 (1MHz) 4.8 (5MHz)	3.0 ±0.2	3.0 ±0.2
DC port V_π (V)	10.6	5.8	5.9	12.0	5.8 ±0.2	5.8 ±0.2
Test Source	1557nm DFB	1557nm DFB	1557nm DFB	1550nm DFB	1550nm DFB	1550nm DFB

Table 2. MZIs Characterization Parameters.

C. SUMMARY

The characterization of the DFB laser diode and the MZIs were successfully gathered experimentally. The results were vital for the simulation of the front-end electro-optical ΣΔ modulator presented in the next chapter.

IV. PHOTONICS OPTSIM SIMULATION

A. OVERVIEW

This chapter presents a pulse to pulse simulation of an oversampling integrated optical first-order single-bit ΣΔ modulator in OptSim. The electro-optical ΣΔ modulator uses an externally modulated pulsed laser to oversample an input at two MZIs.

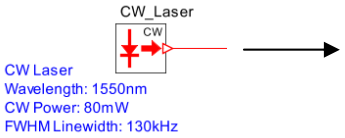
OptSim is proprietary software of Rsoft Design Group. The simulation package is used to design optical systems, simulate the results, and to compare the performance of the system given various hardware component parameters. The simulation software is used to design and simulate the ΣΔ system by using an interconnected set of blocks. Given various hardware component parameters each block represents a component or subsystem in the ΣΔ system.

B. DISTRIBUTED FEEDBACK LASER

Semiconductor lasers are quickly becoming the laser of choice for low power applications because of their small size and solid-state construction. The DFB laser used in the laboratory is a high power CW laser diode constructed out of *InGaAsP/InP* alloy semiconductor material system. With an output power of 80mW and a wavelength of approximately 1550nm this laser was used in conjunction with an analog intensity modulator (AIM) to externally switch the laser off and on. In laboratory experiments the laser linewidth was found by using a delayed self heterodyning method in which the FWHM frequency linewidth was 130kHz. A detailed explanation of the self heterodyning method is found in [16].

In the OptSim simulation software the laser model used was a simplified CW laser. Laser phase noise is taking into account by generating a Lorentzian emission line shape whose FWHM is specified by the parameters and chosen to be 130kHz as measured in the laboratory experiment. Figure 10 shows the parameter list for the CW laser model used in OptSim. The CW power was specified in the model to be 80mW

which corresponds to the specification of the laser. Two options are available for laser phase noise bandwidth, ideal which has infinite bandwidth, and realistic bandwidth limited. Ideal was chosen for the model.



CW_Laser

Parameter	Value	Units	Range
Center emission frequency	193.41449	THz	[193.36449, 193.46449]
Center emission wavelength	1550.0	nm	[1549.59941, 1550.4008]
Source Status	1		[0, 1]
CW Power	19.0309	dBm	[-3000, 3000]
CW Power	80	mW	(0, Inf)
FWHM Linewidth	0.130	MHz	[0, Inf)
-20 dBm Linewidth	1.29348	MHz	[0, Inf)
Initial Phase	"Random"		
Deterministic Initial Phase	0.0	rad	[0, 6.28319]
Noise Type	"Ideal"		
Relaxation Oscillation peak Frequency	5.0	MHz	(0, Inf)
Relaxation Oscillation Peak Overshoot	7.0	dB	(0, Inf)

Figure 10. CW Laser Model and Parameter List.

C. ANALOG INTENSITY MODULATOR

The CW laser pulses were externally modulated by an analog intensity modular (AIM) to switch the laser *on* and *off*. The AIM used for the simulation represents an MZI that consists of a 3dB optical beam intensity splitter, two optical fiber waveguides, electrodes, and an intensity combiner. Figure 4 shows a general schematic diagram of an MZI.

The component model implements a single arm Mach-Zehnder amplitude modulator with sin^2 electrical shaped input-output characteristics. The transfer function is typical for a Mach-Zehnder external modulator based on the electro-optic effects in the $LiNbO_3$ devices. Basic attributes of MZI could be chosen such as on-off extinction ratio, excess loss, transmissivity offset voltage and the value for V_π. The value for V_π determines the voltage swing needed to switch over between the minimum and maximum

transmission states as represented by equation (14). Figure 11 depicts the parameter list of the AIM-MZI as presented by the simulation software [18].

AIM_MZI

Parameter	Value	Units	Range
Excess loss	0.0	dB	[0, Inf)
Maximum Transmissivity Offset voltage: Von	4.7	V	
Extinction Ratio Type	"Realistic"		
Extinction Ratio	26.0	dB	[0, Inf)
Chirp Factor	0.0		
V pi	4.8	V	(0, Inf)
Electrical Filtering with SIN(f/Bw)/pf Law	"No"		
-3 dB bandwidth	10.0	GHz	(0, 44.29465)
First filter notch	= 22.57609	GHz	

Figure 11. Parameter Section of the AIM-MZI.

In order to confirm the functionality of the AIM-MZI model, in particular the V_π parameter a 5MHz sawtooth wave signal was positioned as the RF electrical signal input V_{in} to the MZI and used to modulate the CW laser optical signal. The modulated optical signal at the output of the AIM-MZI was observed in order to verify that the modulator indeed had a voltage swing of V_π needed to switch over between minimum and maximum transmission states. When the semi-difference between input voltages V_{in} is equal to V_{on}, the power of the optical signal is attenuated by the excess loss only, so the modulator is in the maximum transmission state. To switch to the minimum transmission state a V_π voltage must be added or subtracted to V_{on}. Figures 12 and 13 show a pictorial explanation of the transmissivity characteristics and the OptSim schematic used to verify that the AIM-MZI used indeed produced a v_π shift, respectively.

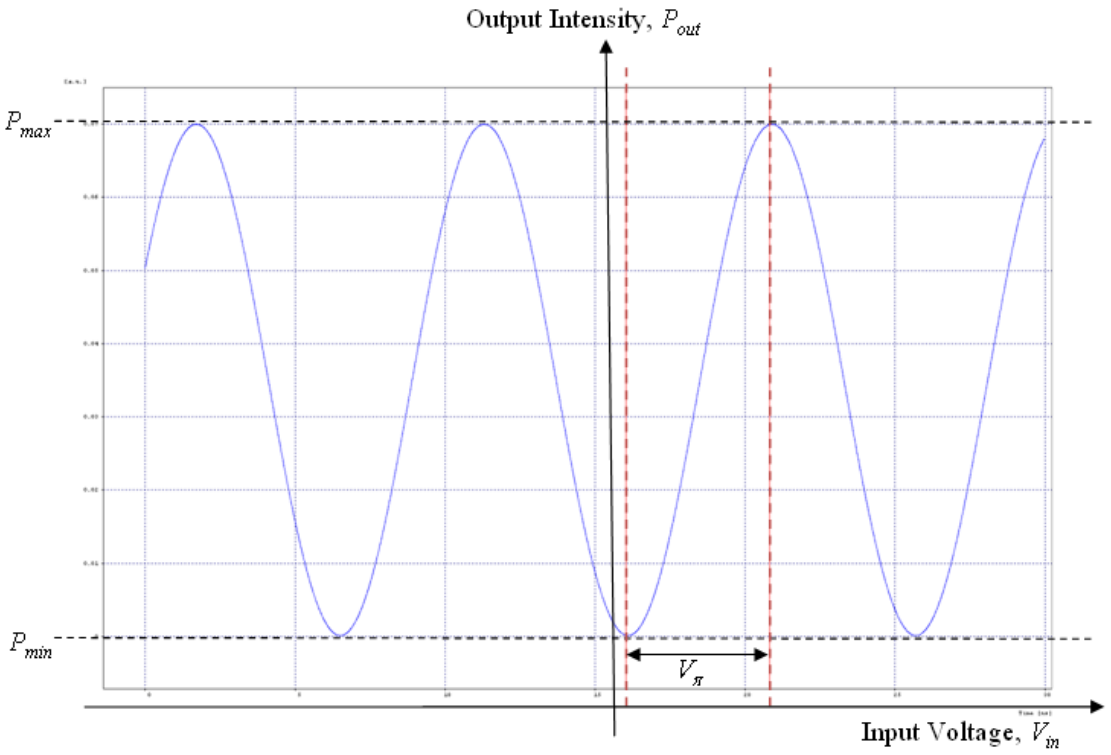


Figure 12. Transmissivity characteristic of the device.

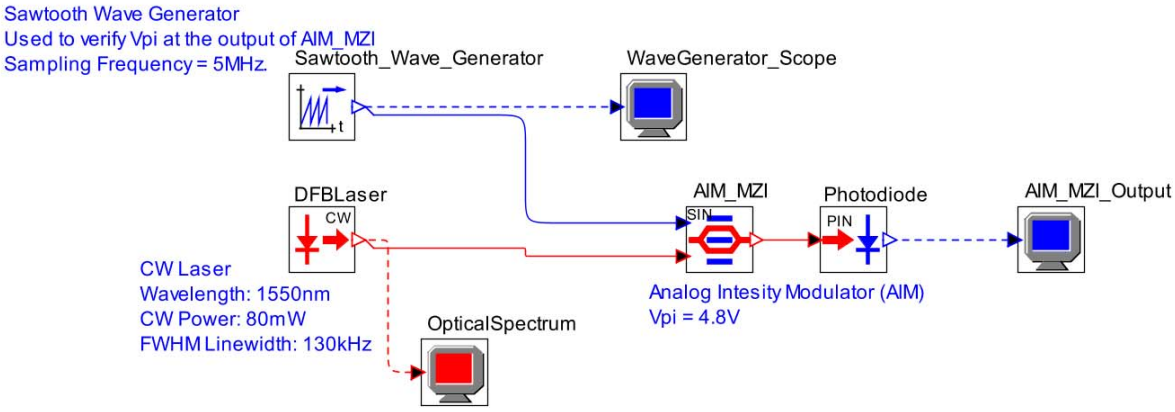


Figure 13. OptSim schematic diagram developed for V_{π} confirmation.

D. MACH-ZEHNDER INTERFEROMETERS

Once the external modulation of the DFB laser was correctly achieved by the model, a 5MHz square wave pulse signal with a 20% duty cycle replaced the sawtooth waveform as the electrical RF input to the AIM.

Direction and magnitude MZI were added at the output of the AIM with an optical splitter. The optical splitter component implements a balanced splitter with the same attenuation on each output. A simulated RF input (triangle waveform) of 20kHz with amplitude of 3V was added to the electrical input of both the magnitude and direction MZIs. The 3V amplitude matched the 3V (V_π) inserted into the parameter list of the MZIs. A DC bias of 1.5V $(V_\pi/2)$ was added to the electrical input of the magnitude MZI for magnitude quantization. Since the direction MZI is already preset for direction quantization there was no need to insert a bias into the direction MZI. In the model shown in Figure 14 the parameters for both direction and magnitude MZI were identical, replicating similar findings in the laboratory experiment.

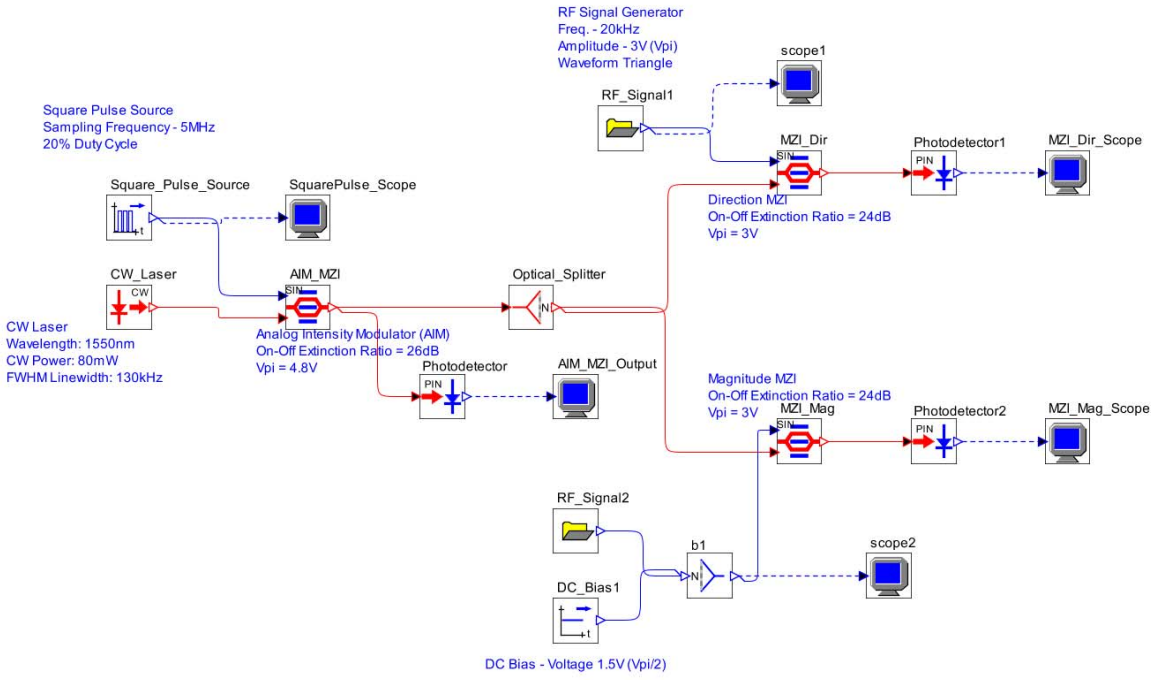


Figure 14. OptSim system simulation schematic.

Since one of the advantages of this type of architecture is being able to oversample wide-band signals directly at the antenna. The OSR was calculated as

$$OSR = \frac{f_s}{2f_o} = \frac{5MHz}{2(20kHz)} = 125 \tag{20}$$

where f_s is the RF antenna sampling frequency and f_0 is the signal bandwidth being sampled at the Nyquist rate. Figure 15 shows the direction MZI output waveform depicting 25 samples per division given a total of 125 samples which matches the experimental results.

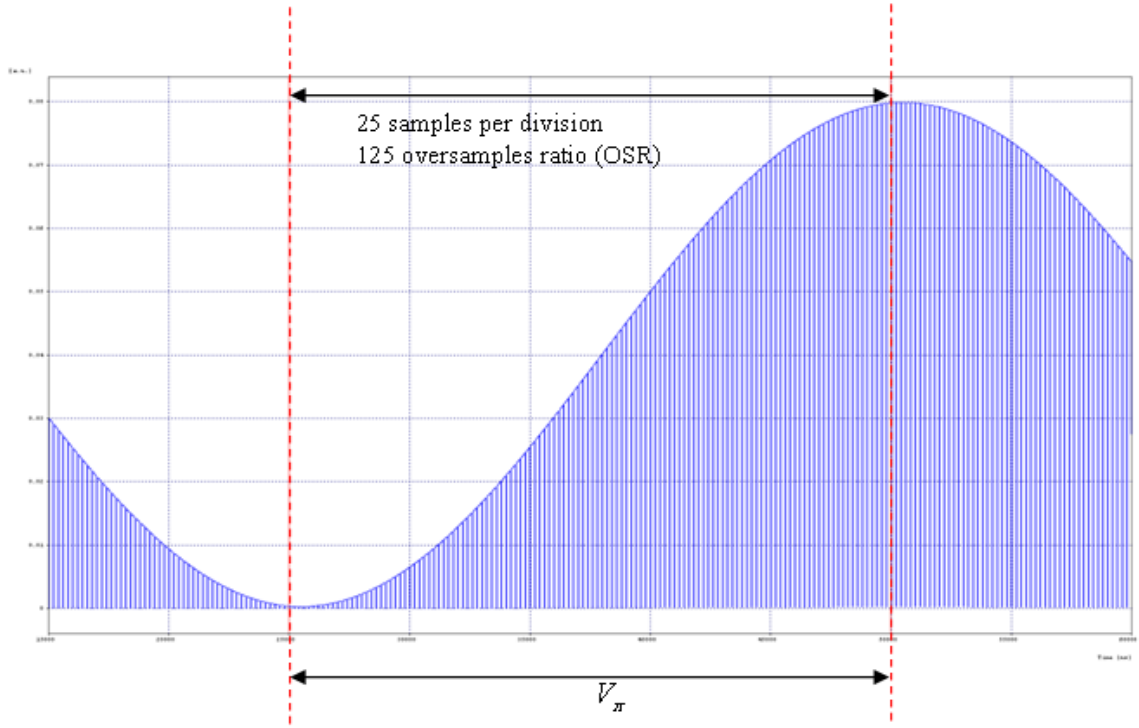


Figure 15. Direction MZI output waveform.

The intensity transfer function for both the direction and magnitude MZIs are shown in Figure 16. These results compare rather well to the laboratory results shown in Figure 17.

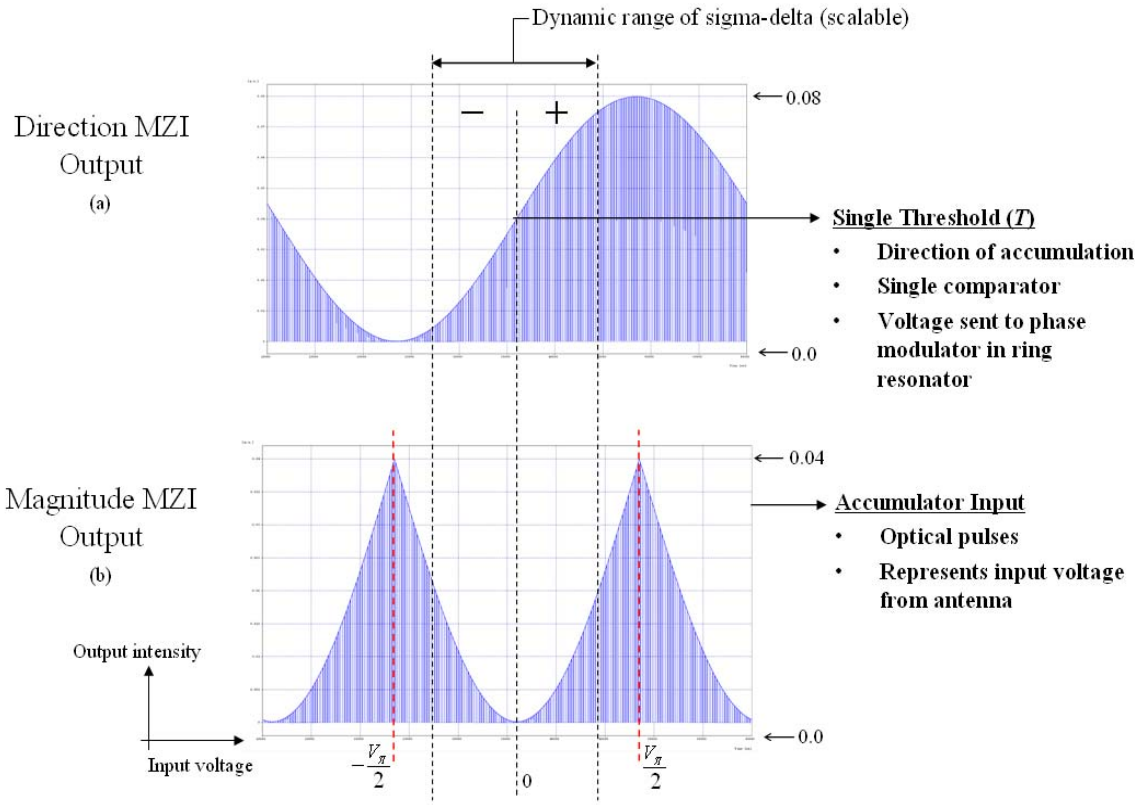


Figure 16. Transmissivity Function output waveforms of (a) Directional MZI, and (b) Magnitude MZI.

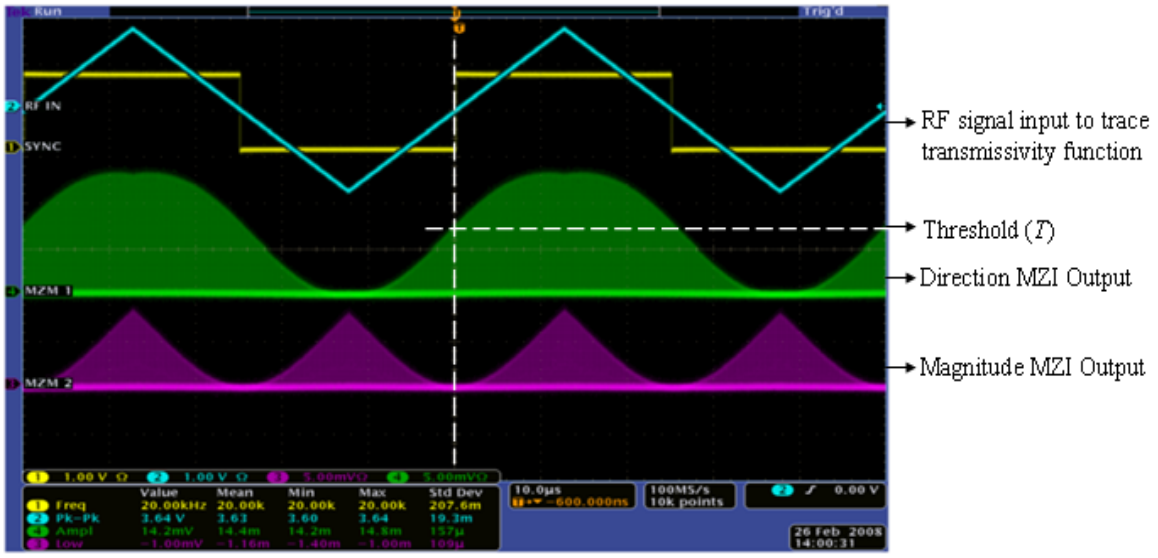


Figure 17. Laboratory Results of Transmissivity Function.

E. OPTICAL BEAM SPLITTER

This component simulates an *ideal* optical splitter. The component implements a balanced splitter with the same attenuation on each output. To better mimic the real component used in the laboratory a 3dB attenuation loss was inserted on each output parameter.

F. PHOTODETECTOR

The OptSim model used to implement the photodetector was a PIN photodiode. As stated in chapter II, the photodetector converts photons to electric current (optical input, electrical output). The electrical output is then connected to a simulated electrical oscilloscope which displays the outputs of the MZIs. The photodiode finite bandwidth was modeled using a single-pole transfer function of -3dB bandwidth. The filtering parameter was turned off allowing the device to have ideally an infinite bandwidth.

G. SUMMARY

The OptSim simulation results show the phase coherent nature of the MZIs. The MZI characteristics were also evaluated with the software model design. In order to compare the performance of the laboratory equipment a simulation was developed to verify the voltage required by the MZI to drive the signal from its minimum to maximum value. This was accomplished by externally modulating an AIM-MZI with a simulated RF signal source. The results confirmed the performance of the MZI model provided by OptSim.

Due to limitations in the capabilities of modeling the ring resonator, the model was only developed to the output of the directional and magnitude MZI arms. The results were compared to the laboratory experiments. Utilizing a CW laser pulse model, signal generator sawtooth model, and an AIM model the laser pulse was used to externally modulate the two arms of the MZIs. In this configuration the laser pulse was able to be switched *on* and *off*. The voltage swing needed to switch between transmission states was confirmed. All simulation results confirm the correct operation of the integrated optical model in comparison to the laboratory test results.

V. COMPARATOR PROCESSOR CIRCUIT SIMULATION

A. COMPARATOR PROCESSOR CIRCUIT DESIGN

The ΣΔ ADC diagram shown in Figure 3 depicts two comparator processor circuits in the diagram. One comparator processor is located after the directional MZI and it delivers an appropriate voltage, σ, to an input of the ring resonator. The second comparator processor circuit is designed to quantize a signal in the loop and provide the output of the modulator. The architecture of the two comparators are the same, the only difference are the inputs and threshold levels.

The architecture model consists of two high-speed comparators, *nor* gates, and a set-reset (S-R) latch, as shown in Figure 18. The circuit was modeled in SmartSpice an analog circuit simulator by SIMUCAD. A spice macromodel of the MAX9602 comparator was obtained from Maxim Integrated Products. The comparator model simulates a dual positive emitter coupled logic (PECL) featuring extremely low propagation delay (500ps). PECL is nothing more than standard emitter coupled logic (ECL) devices run off of a positive power supply [19]. In addition to the comparators, nor gates were modeled using switches and a first order resistor-capacitor (RC) circuit, as shown in Figure 19. The *nor* gates were designed to operate in the PECL transition region and provide edge detection to the circuit. An S-R latch was designed with two cross-coupled *nor* gates providing stability of the signal.

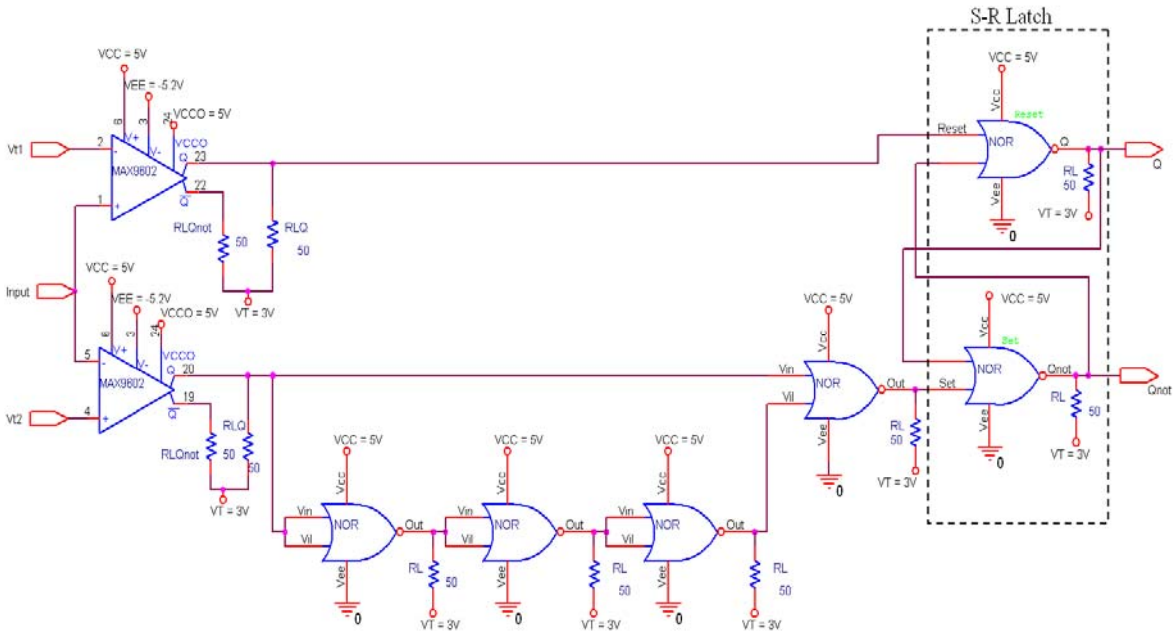


Figure 18. Schematic of Comparator Processor Circuit Design.

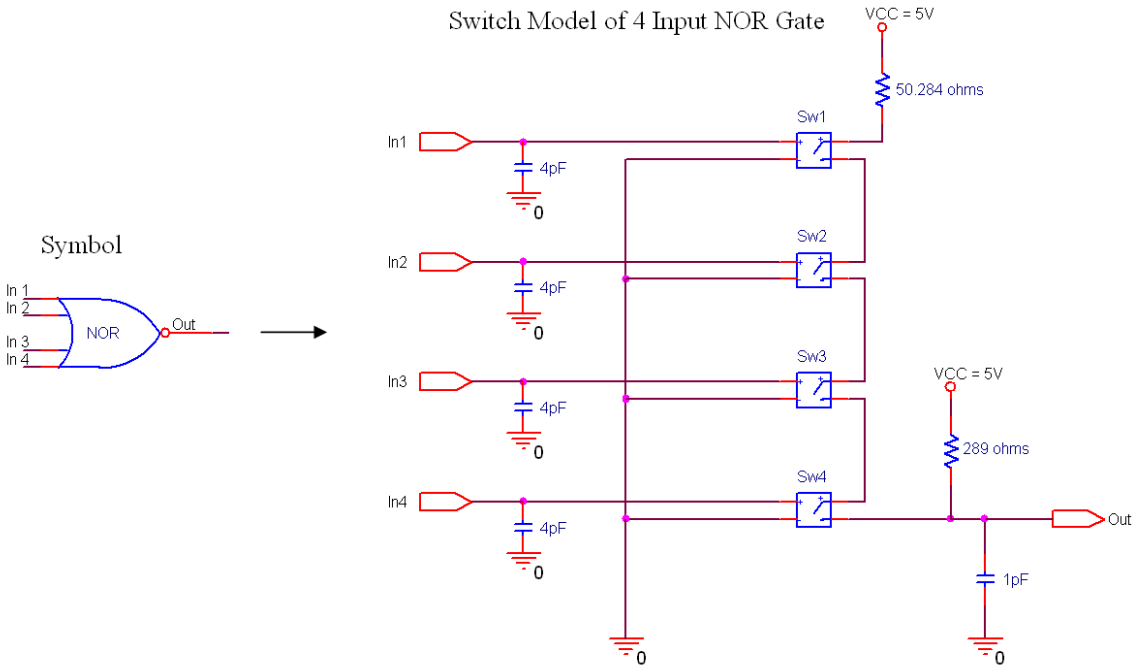


Figure 19. Schematic of 4-Input NOR Gate Model.

The high-speed comparator processor design is a proof of concept model of mixed signals architecture. A spice model netlist was developed and is displayed in appendix A. The spice model netlist are organized as a group of subcircuits. In each subcircuit model netlist, the model name is followed by a list of node interconnects.

The input of the comparator was configured to simulate an input signal with V_{max} equal to 60mV with a noise level V_{noise} at 20mV. The comparator has two threshold levels V_{th1} set at 50mV and V_{th2} set to 15mV. The purpose of V_{th2} is to identify the quantized noise floor and cancel it. If the path voltage, V_{in}, exceeds the threshold value of the comparator circuit, V_{th1}, the output of the circuit is PECL logic high, the output at Q is high, and the latch is said to be in the *set* state. Otherwise, the latch is said to be in the *clear* state setting the output of the comparator to Q low. Simulation results are shown in Figure 20. Figure 20 shows the simulated input signal with threshold levels V_{th1} and V_{th2}, as well as, the true Q output of the comparator circuit showing the latch in *set* and *reset* states.

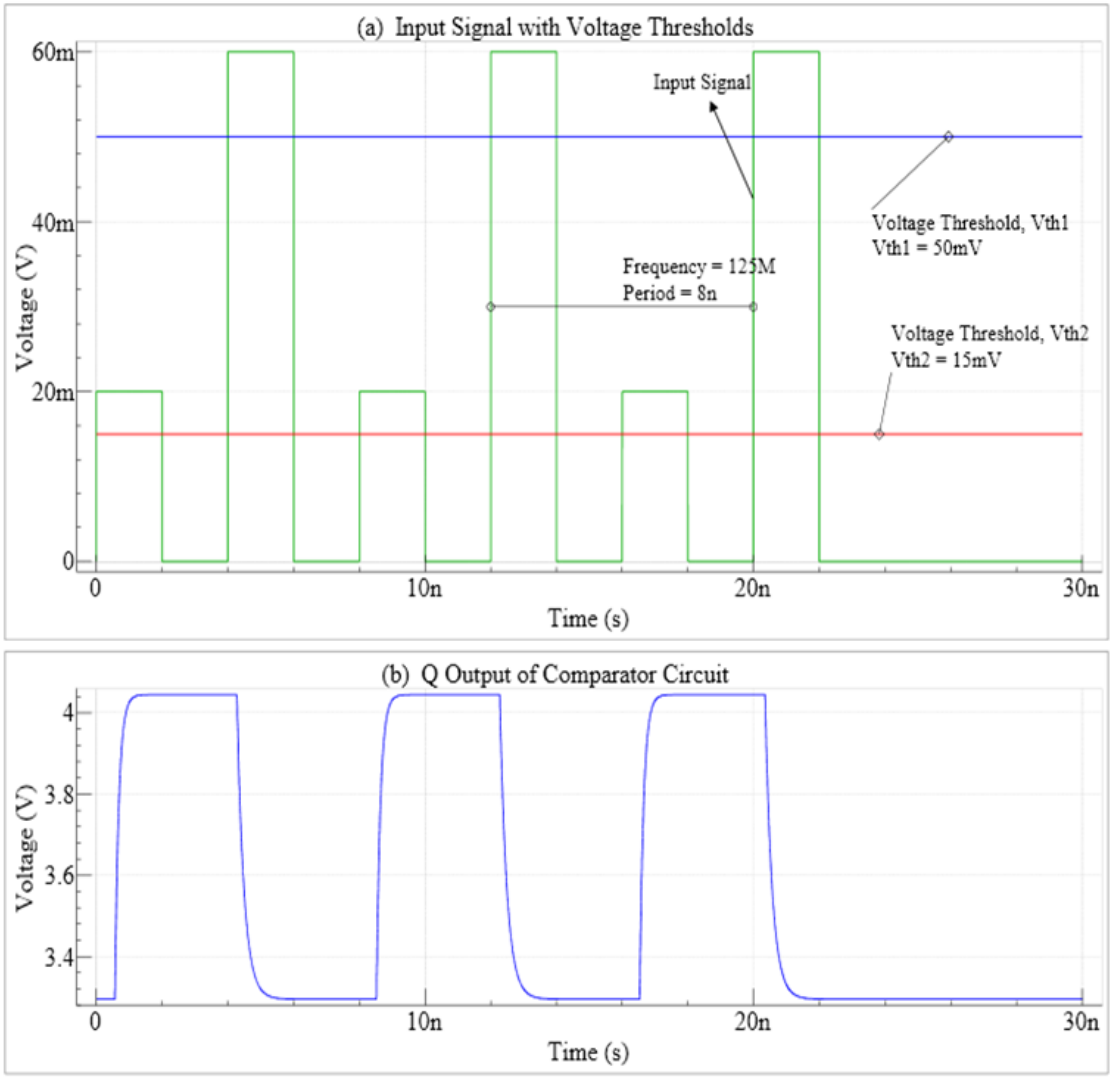


Figure 20. (a) Input Signal with Voltage Thresholds Waveform, and (b) Comparator Processor Output waveforms.

B. SUMMARY

The construction of a high-speed comparator processor circuit has been demonstrated with promising results. A simulated input signal was constructed with a replicated noise floor and the signal was injected into the comparator. Two threshold voltage levels were set for the input signal. One threshold level is designed to identify the input signal, and the other to eliminate the noise in the signal. This comparator circuit serves as a proof of concept model. However, it is not ready to be fully integrated in a

photonic ΣΔ ADC. In a photonic ΣΔ ADC, a sampling rate of 10 Gsamples/sec (GSPS) would need to be demonstrated. Several papers produced by the Air Force Research Laboratory (AFRL) [13], [20] suggest that an *indium phosphide* (InP) hetero-junction bipolar transistor (HBT) technology would need to be demonstrated for an on-chip integrated circuit design.

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VI. CONCLUSION, LIMITATIONS, AND RECOMMENDATIONS

A. CONCLUSION

The coherency of the optical ΣΔ ADC design was simulated. A working reliable computer model was developed using RSoft OptSim, an optical circuit simulator. The results confirm the correct operation of the MZIs, transmissivity characteristics, and functionally for future integration. Additionally, the simulation showed the capability to oversample a signal directly at the antenna.

A dual comparator circuit with signal and noise threshold levels was simulated for proper operation in the presences of an input signal with a noise floor. In the ΣΔ modulator design the comparator will be able to take signals from the directional MZI or from the output of the ring resonator accumulator. The comparator processor circuit design worked properly with a simulated input, a high-speed comparator model, and generic switching *nor* gate S-R latch circuit. However, the comparator processer circuit does not operate fast enough for the high sampling rates that are the ultimate goal of this project.

In conclusion, it is noteworthy to state that photonics is by nature wideband (THz) and well suited for high-speed signal conversion. Specifically, photonic ADCs have the advantage of precise sampling times, narrow optical sampling apertures, and the ability to sample without contaminating the incident signal. Signal sampling with optical pulses could eliminate the need for a sample and hold circuit, performance limiting components in conventional high-speed ADCs [3]. These factors make photonic ΣΔ ADCs a promising fit in digital receiver systems.

B. LIMITATIONS

Although the computer models were successful, certain parameters associated with the realities of this type of device were not addressed or simulated. These include signal losses associated with the optical fiber and components, undesired crosstalk within

the directional couplers, laser jitter, and the length of optical fiber required to affect the proper optical delay within the ring resonator accumulator. The ring resonator design is still an ongoing process as is integration of that device with the ΣΔ system.

This thesis, demonstrated that photonics has many attributes that can impact and enhance the performance of high-speed ADCs. Conceptually, a problem with ΣΔ modulator based ADCs is the oversampling requirement, that is, the circuitry of the ADC must be designed to operate at a significantly higher frequency than the maximum frequency of the analog signal that is converted by the ADC. The greater the required accuracy of the ΣΔ modulator ADC, the larger the sampling frequency must be. Limitations in circuit capabilities have, therefore, limited the use of the single channel ΣΔ ADCs to relatively low signal frequencies. However, as one source suggests [4], the sampling frequency may be reduced by using multiple ΣΔ modulators.

In addition, the single bit electro-optical ΣΔ modulator depicted in Figure 3 is designed for wide-band sampling frequency signals. This thesis focused on evaluating the wide-band system in narrow-band.

C. RECOMMENDATIONS

Further efforts include the continued optimization of the first order integrated optical model, by expanding the architecture to withstand the ring resonator architecture. Once the ring resonator is introduced into the setup, precision delay devices may be required to match the optical path lengths for the two interferometers. Another introduction to the photonic architectures would have to be a mode-locked fiber laser with stable femto-second pulses as a timing reference. The mode-locked laser can overcome the timing jitter presented in the sampling apertures of the ADCs.

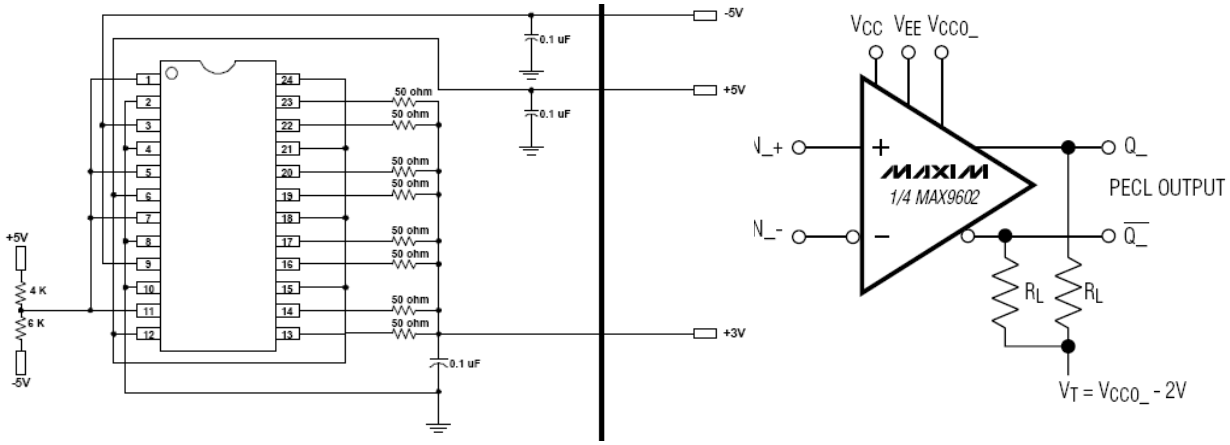
Additionally, signal analysis needs to be modeled and conducted on the oversampled optical ΣΔ outputs at various oversampling ratios to show the increased signal to noise ratio and bit resolution obtained using the decimation filter.

A more thorough wide-band analysis needs to be conducted on the entire ΣΔ ADC architecture.

APPENDIX A. SMARTSPICE SIMULATION SCRIPT

MAX9602 SPICE MACROMODEL

This section of Appendix A shows the Spice Macromodel for the MAX9602 high-speed comparator.




```
*MAX9602 MACROMODEL
* ------------------------------
* Revision 0, 11/2003
* ------------------------------
* MAX9602 is a ultra-high-speed quad comparator with extremely low
* propogation delay(500 ps). The outputs are complimentary digital
* signals, compatible with PECL systems.
* ------------------------------
* Connections
*   1  = INA+
*   2  = INA-
*   3  = VEE
*   4  = INB+
*   5  = INB-
*   6  = VCC
*   7  = INC+
*   8  = INC-
*   9  = VEE
*  10  = IND+
*  11  = IND-
*  12  = VCC
*  13  = QD_
*  14  = QD
*  15  = VCCOD
*  16  = QC_
*  17  = QC
```

```
*  18  = VCCOC
*  19  = QB_
*  20  = QB
*  21  = VCCOB
*  22  = QA_
*  23  = QA
*  24  = VCCOA
*****************
* NOTE1: OUT_ IS ACTUALLY COMPLIMENTED OUT.
* NOTE2: OUTPUT IS MEASURED WITH RESPECT TO VCC0
* NOTE3: INCLUDE
*          .OPTIONS ITL4=50
*                       TO ENHANCE CONVERGENCE.
*****************
****************************************
.SUBCKT MAX9602 1 2 3 4 5 6 7 8 9
+             10 11 12 13 14 15 16
+             17 18 19 20 21 22 23 24
X1 1 2 6 3 24 23 22 MAX9602CMP
X2 4 5 6 3 21 20 19 MAX9602CMP
X3 7 8 12 9 18 17 16 MAX9602CMP
X4 10 11 12 9 15 14 13 MAX9602CMP
.ENDS
****************************************

*****************
.SUBCKT MAX9602CMP 1 2 3 4 5 6 7
*INPUT STAGE
*****************
RPC 3 0 181.159
RPE 4 0 138.298
*****************
CIN 2 5 2P
*****************
VOS 99 1 1M
*****************
IEE 3 11 400U
Q1 12 2 11 QX
Q2 13 99 11 QY
RC1 12 4 129.3
RC2 13 4 129.3
*****************
*INTERMEDIATE STAGE
GA 5 14 12 13 1
RA 14 5 100K
CA 14 5 1E-18
D1 14 15 DX
VOH 15 5 -0.94
D2 16 14 DX
VOL 16 5 -1.72
**************
EOUT 19 5 14 5 1
**************
ECCL 33 5 15 5 1
EEEL 44 5 16 5 1
```

```
M1 21 19 33 33 PMOS
M2 21 19 44 44 NMOS
**************
*DELAY,RISE AND FALL TIME
EDELQ 102 5 19 5 1
T1Q 102 5 17 5 ZO=50 TD=166P
RTERMQ 17 5 50
CTERMQ 17 5 0.185P
GRISEQ 5 23 17 5 1M
RRISEQ 23 5 1K
C23 23 5 0.15P
****
EDELQB 103 5 21 5 1
T1QB 103 5 18 5 ZO=50 TD=166P
RTERMQB 18 5 50
CTERMQB 18 5 0.185P
GRISEQB 5 24 18 5 1M
RRISEQB 24 5 1K
C24 24 5 0.15P
****************
E1 6 5 23 5 1
E2 7 5 24 5 1
****************
*MODELS USED
.MODEL QX PNP(BF=34.188)
.MODEL QY PNP(BF=32.52)
.MODEL DX D(N=0.001 TT=1E-15)
.MODEL NMOS NMOS(KP=1 TOX=100U VTO=0.39 W=1U L=1U)
.MODEL PMOS PMOS(KP=1 TOX=100U VTO=-0.39 W=1U L=1U)
****************
.ENDS
****************
```

COMPARATOR PROCESSOR SPICE MODEL SCRIPT

This section of the Appendix A shows the Spice simulation script developed for the comparator circuit design.

```
Comparator/NOR gates/SR Flip-Flops

* Included Files
.INCLUDE MAX9602.txt

*Voltage Controlled Switch model statement
.model pull_up_sw sw (vt=3.6675 ron= 1G roff=1)

*ECL  NOR gate subcircuit
.subckt nor2 Vcc Gnd In1 In2 In3 In4 Out
r1 Vcc 10 50.284
s1 10 20 In1 Gnd pull_up_sw
s2 20 30 In2 Gnd pull_up_sw
s3 30 40 In3 Gnd pull_up_sw
s4 40 Out In4 Gnd pull_up_sw
r2 Vcc Out 289.0
c1 In1 Gnd 4pf
c2 In2 Gnd 4pf
c3 In3 Gnd 4pf
c4 In4 Gnd 4pf
c5 Out Gnd 1pf
.ends nor2

**Main Circuit**
*DC supplies: Comparators/NOR gate
VCC Vcc Gnd DC +5.0
VEE Vee Gnd DC -5.2
VCCO Vcco Gnd DC +5.0
Vterm Vtt Gnd DC +3.0
Vinlow Vil Gnd DC +3.357

*Input Signal Source            V1   V2  td    tr    tf    PW   T
*Vinput In Gnd DC 0.0 PULSE(4.045 3.295 500p 380p 380p 1000p 2760p)
Vinput  In  Gnd  DC  0.0  PWL(1ps  0mV   1.00001ps 20mV   2.0ns   20mV   2.00001ns 0mV   4ns  0mV
4.00001ns 60mV  6.0ns 60mV  6.00001ns 0mV
+ 8.0ns 0mV  8.00001ns 20mV  10.0ns  20mV  10.000001ns  0mV 12.0ns  0mV 12.00001ns  60mV  14ns
60mV  14.00001ns 0mV
+  16.0ns 0mV  16.00001ns 20mV  18.0ns  20mV  18.000001ns  0mV 20.0ns  0mV 20.00001ns  60mV
22.0ns  60mV  22.00001ns 0mV )

Vref1 Vth1 Gnd DC +50.0mV
Vref2 Vth2 Gnd DC +15.0mV

*First MAX9602 Comparator
* IN+ IN- VCC VEE VCCO Q Qnot
X1  In Vth1 Vcc Vee Vcco Q1 Q1not MAX9602CMP
```

```
RLQ1  Q1 Vtt 50
RLQ1not  Q1not Vtt 50
*Second MAX9602 Comparator
* IN+ IN- VCC VEE VCCO Q Qnot
X2  Vth2 In Vcc Vee Vcco Q2 Q2not MAX9602CMP
RLQ2  Q2 Vtt 50
RLQ2not  Q2not Vtt 50

* NOR gates
* Buffer signal with 3 NOR gates in series to make input signal more realistic.
* VCC VEE In1 In2 In3 In4 Out
xnor1 Vcc Gnd Q2 Vil Vil Vil 10 nor2
r1 10 Vtt 50
xnor2 Vcc Gnd 10 Vil Vil Vil 20 nor2
r2 20 Vtt 50
xnor3 Vcc Gnd 20 Vil Vil Vil 30 nor2
r3 30 Vtt 50
xnor4 Vcc Gnd Q2 30 Vil Vil 40 nor2
r4 40 Vtt 50

*SR Latch (Flip-Flop)
*1st NOR gate: Input 1 to Vin, Input 2 to output of 2nd NOR gate, 2 remaining inputs to Vinlow
*2nd NOR gate: Input 1 to output of 1st NOR gate, Input 2 to Vin, 2 remaining inputs to Vinlow
* VCC VEE In1 In2 In3 In4 Out
xset Vcc Gnd 60 40 Vil Vil 50 nor2
r5 50 Vtt 50
xreset Vcc Gnd Q1 50 Vil Vil 60 nor2
r6 60 Vtt 50

**Analysis Requests**
.tran 10ps 30000ps

**Output Request**
.probe
.end
```

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APPENDIX B. DATASHEETS

MAX9602 DATASHEET

This section of Appendix B consists of a datasheet for the MAX9602 PECL high-speed comparator used to model the comparator circuit.

19-2409; Rev 1; 9/02

MAXIM

Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

General Description

The MAX9600/MAX9601/MAX9602 ultra-high-speed comparators feature extremely low propagation delay (500ps). These dual and quad comparators minimize propagation delay skew (10ps) and are designed for low propagation delay dispersion (30ps). These features make them ideal for applications where high-fidelity tracking of narrow pulses and low timing dispersion is critical.

The differential input stage accepts a wide range of signals in the common-mode range from (V_{EE} + 3V) to (V_{CC} - 2V). The outputs are complementary digital signals, compatible with ECL and PECL systems, and provide sufficient current to directly drive transmission lines terminated in 50Ω.

The MAX9600/MAX9601 dual-channel ECL and dual-channel PECL output comparators incorporate latch enable (LE_, $\overline{LE\_}$), and hysteresis (HYS_). The complementary latch-enable control permits tracking, track-hold, or sample-hold mode of operations. The latch enables can be driven with standard ECL logic for MAX9600 and PECL logic for MAX9601. The MAX9602 quad-channel PECL output comparator is ideal for high-density packaging in limited board space.

The MAX9600/MAX9601 are available in 20-pin TSSOP packages, and the MAX9602 is offered in a 24-pin TSSOP package. The MAX9600/MAX9601/MAX9602 are specified for operation from -40°C to +85°C.

Applications

VLSI and High-Speed Memory ATE
High-Speed Instrumentation
Scope/Logic Analyzer Front Ends
High-Speed Triggering
Threshold and Peak Detection
Line Receiving/Signal Restoration

Features

- 500ps Propagation Delay
- 30ps Propagation Delay Dispersion
- 4Gbps Tracking Frequency
- -2.2V to +3V Input Range with +5V/-5.2V Supplies
- -1.2V to +4V Input Range with +6V/-4.2V Supplies
- Differential ECL Outputs (MAX9600)
- Differential PECL Outputs (MAX9601/MAX9602)
- Latch Enable (MAX9600/MAX9601)
- Adjustable Hysteresis (MAX9600/MAX9601)

Ordering Information

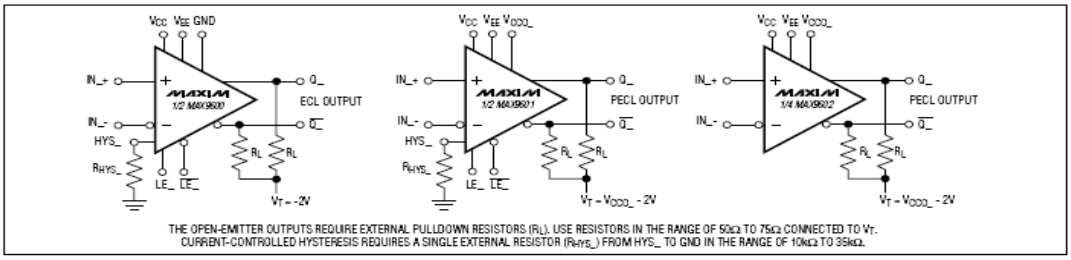
PART	TEMP RANGE	PIN-PACKAGE
MAX9600EUP	-40°C to +85°C	20 TSSOP
MAX9601EUP	-40°C to +85°C	20 TSSOP
MAX9602EUG	-40°C to +85°C	24 TSSOP

Selector Guide

PART	PIN-PACKAGE	SELECTION
MAX9600EUP	20 TSSOP	Dual ECL Output Comparator with Latch Enable and Hysteresis
MAX9601EUP	20 TSSOP	Dual PECL Output Comparator with Latch Enable and Hysteresis
MAX9602EUG	24 TSSOP	Quad PECL Output Comparator

Pin Configurations appear at end of data sheet.

Functional Diagrams



THE OPEN-EMITTER OUTPUTS REQUIRE EXTERNAL PULLDOWN RESISTORS (R_L). USE RESISTORS IN THE RANGE OF 50Ω TO 75Ω CONNECTED TO V_T.
CURRENT-CONTROLLED HYSTERESIS REQUIRES A SINGLE EXTERNAL RESISTOR ($R_{HYS\_}$) FROM HYS_ TO GND IN THE RANGE OF 10kΩ TO 35kΩ.

Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

ABSOLUTE MAXIMUM RATINGS

$V_S = V_{CC} - V_{EE}$ 12.0V
V_{CC} to GND (MAX9600) 6.8V
V_{EE} to GND (MAX9600) ..... -6.5V
Differential Input Voltage ..... ±6.5V
Latch Differential Voltage ..... ±4V
Common-Mode Input Voltage (V_{CM}) ..... V_{EE} to V_{CC}
$V_{CCO\_}$ to V_{EE}
(MAX9601/MAX9602) ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
LE_, $\overline{LE\_}$ to GND
MAX9600 ..... (V_{EE} - 0.3V) to 0.3V
MAX9601 ..... (V_{EE} - 0.3V) to ($V_{CCO\_}$ + 0.3V)
Input Current to Any Input Pin 10mA
HYS_ Current (MAX9600/MAX9601) ..... -1mA
Continuous Output Current 50mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 10.9mW/°C above +70°C) 879mW
24-Pin TSSOP (derate 12.2mW/°C above +70°C) 975mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS_ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE\_}$ = high (MAX9600/MAX9601), GND = 0V, R_L = 50Ω to -2V (MAX9600), $V_{CCO\_}$ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT (IN_+, IN_-)							
Input Differential Voltage Range	V_{ID}	Guaranteed by input bias current tests		-5.2		+5.2	V
Input Common-Mode Voltage	V_{CM}	Guaranteed by input bias current tests		V_{EE} + 3		V_{CC} - 2	V
Input Offset Voltage	V_{OS}	T_A = +25°C			±1	±5	mV
		$T_{MIN} \le T_A \le T_{MAX}$				±9	
Input Offset-Voltage Tempco	TCV_{OS}				8		µV/°C
Input Offset-Voltage Channel Matching					1		mV
Input Bias Current	I_B	V_{ID} = ±5.2V			6	20	µA
Input Bias-Current Tempco	TCI_B				10		nA/°C
Input Offset Current	I_{OS}				0.3	±5	µA
Input Resistance	R_{IN}	Differential mode ($V_{ID} \le$ 10mV)			10		kΩ
		Common mode (V_{EE} + 3V) ≤ V_{CM} ≤ (V_{CC} - 2V)			100		MΩ
LATCH INPUT (LE_, $\overline{LE\_}$)							
Latch Differential Input Voltage	V_{LD}	Guaranteed by latch input current	MAX9600	0.4		2.0	V
			MAX9601	0.25		3.50	
Latch Input Voltage Range	V_{LR}	MAX9600		-2		0	V
		MAX9601	$V_{CCO\_}$ ≥ 3.5V	$V_{CCO\_}$ - 3.5		$V_{CCO\_}$	
			$V_{CCO\_}$ < 3.5V	0		$V_{CCO\_}$	
Latch Input Current	I_{LE}, $I_{\overline{LE}}$	MAX9600			5	20	µA
		MAX9601			5	20	
HYSTERESIS INPUT (HYS_)							
Input-Referred Hysteresis		MAX9600/MAX9601	R_{HYS} = ∞		0		mV
			R_{HYS} = 16.4kΩ		30		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS_ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE\_}$ = high (MAX9600/MAX9601), GND = 0V, R_L = 50Ω to -2V (MAX9600), $V_{CCO\_}$ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT (Q_, $\overline{Q\_}$)							
Logic Output High Voltage	V_{OH}	T_A = +25°C	MAX9600	-1.10	-0.94	-0.75	V
			MAX9601/MAX9602	$V_{CCO\_}$ - 1.10	$V_{CCO\_}$ - 0.94	$V_{CCO\_}$ - 0.75	
		T_A = T_{MIN}	MAX9600	-1.2	-1.02	-0.8	
			MAX9601/MAX9602	$V_{CCO\_}$ - 1.2	$V_{CCO\_}$ - 1.02	$V_{CCO\_}$ - 0.8	
		T_A = T_{MAX}	MAX9600	-1.05	-0.87	-0.70	
			MAX9601/MAX9602	$V_{CCO\_}$ - 1.05	$V_{CCO\_}$ - 0.87	$V_{CCO\_}$ - 0.70	
Logic Output Low Voltage	V_{OL}	T_A = +25°C	MAX9600	-1.95	-1.72	-1.55	V
			MAX9601/MAX9602	$V_{CCO\_}$ - 1.95	$V_{CCO\_}$ - 1.72	$V_{CCO\_}$ - 1.55	
		T_A = T_{MIN}	MAX9600	-2.0	-1.78	-1.6	
			MAX9601/MAX9602	$V_{CCO\_}$ - 2.0	$V_{CCO\_}$ - 1.78	$V_{CCO\_}$ - 1.6	
		T_A = T_{MAX}	MAX9600	-1.9	-1.66	-1.50	
			MAX9601/MAX9602	$V_{CCO\_}$ - 1.9	$V_{CCO\_}$ - 1.66	$V_{CCO\_}$ - 1.5	
SUPPLY							
Positive Supply Voltage	V_{CC}	Guaranteed by output swing tests		4.3	5	6.3	V
Negative Supply Voltage	V_{EE}	Guaranteed by output swing tests		-6	-5.2	-4	V
Supply Voltage Difference	V_S	V_S = (V_{CC} - V_{EE}), guaranteed by output swing tests		9.5		11.5	V
Logic Supply Voltage	$V_{CCO\_}$	MAX9601/MAX9602		2.4		V_{CC}	V
Positive Supply Current	I_{CC}	(Note 2)	MAX9600		16	24	mA
			MAX9601		19	27	
			MAX9602		28	39	
Negative Supply Current	I_{EE}	(Note 2)	MAX9600		21	28	mA
			MAX9601		24	33	
			MAX9602		38	49	
Power-Supply Dissipation	P_{DISS}	(Note 2)	MAX9600		190	266	mW
			MAX9601		220	307	
			MAX9602		338	450	
Common-Mode Rejection Ratio	CMRR	(V_{EE} + 3V) ≤ V_{CM} ≤ (V_{CC} - 2V)			70		dB
Power-Supply Rejection Ratio	PSRR	4.3V ≤ V_{CC} ≤ 6.3V, -6V ≤ V_{EE} ≤ -4V, 9.5V ≤ V_S ≤ 11.5V			65		dB

Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS_ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE}$_ = high (MAX9600/MAX9601), C_L = 5pF, GND = 0V, R_L = 50Ω to -2V (MAX9600), V_{CCO}_ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Tracking Frequency Toggle Rate	f_{MAX}	V_{OUT} = 550mVP-P, input overdrive = 100mV			4		Gbps
Minimum Pulse Width	t_{PW}	V_{OUT} = 550mVP-P, input overdrive = 100mV			250		ps
Propagation Delay	t_{PD-}, t_{PD+}	Input overdrive = 100mV, Figure 1, (Note 3)			500	700	ps
Propagation Delay Tempco	TCt_{PD}				0.5		ps/°C
Propagation Delay Skew	t_{PDSKEW}	Input overdrive = 100mV (Note 4)			10		ps
Propagation Delay Match		Input overdrive = 100mV (Note 5)			40		ps
Propagation Delay Dispersion Overdrive		10mV to 100mV			15		ps
		100mV to 2V			40		
Propagation Delay Dispersion Common-Mode Voltage		V_{IN} = 1VP-P input overdrive = 100mV	(V_{EE} + 3V) ≤ V_{CM} ≤ (V_{CC} - 2V)		10		ps
Propagation Delay Dispersion Input Slew Rate			0.2V/ns to 10V/ns		40		
Propagation Delay Dispersion Duty Cycle			10% to 90% at 250MHz		30		
Propagation Delay Dispersion Pulse Width			350ps to 1ns		20		
Unit-to-Unit Propagation Delay Match		Input overdrive = 100mV			50		ps
Output Jitter		V_{IN} = 2VP-P; 50MHz			300		fs
Input Capacitance	C_{IN}	IN_+ or IN_-, with respect to GND			2		pF
Latch Setup Time	t_{LS}	Figure 1, (Notes 3, 6)		250	80		ps
Latch Hold Time	t_{LH}	Figure 1, (Notes 3, 6)		300	85		ps
Minimum Pulse Width	t_{LPW}	Figure 1			250		ps
Latch to Output Delay	t_{LPD}	Figure 1			200		ps
Rise Time and Fall Time	t_R, t_F	20% to 80%, Figure 1			200		ps

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: Does not include output state current in Q_, $\overline{Q}$_.

Note 3: Guaranteed by design.

Note 4: Propagation delay skew (t_{PDSKEW}) is for a single channel and is the difference between the propagation delay to the high-to-low output transition vs. the low-to-high output transition.

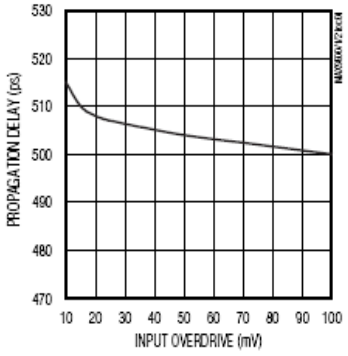
Note 5: Propagation delay match is the difference of t_{PD-} or t_{PD+} of one channel to the t_{PD-} or t_{PD+} of another channel of the same device.

Note 6: Latch setup and hold-timing specifications are for a differentially driven latch signal.

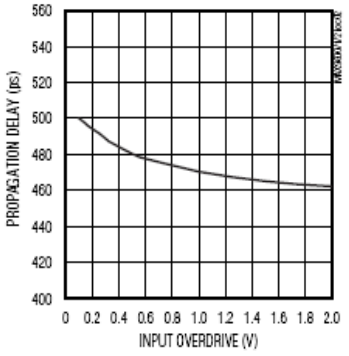
Typical Operating Characteristics

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS_ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE}$_ = high (MAX9600/MAX9601), C_L = 5pF, GND = 0V, R_L = 50Ω to -2V (MAX9600), V_{CCO}_ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), input slew rate = 2V/ns, duty cycle = 50%, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

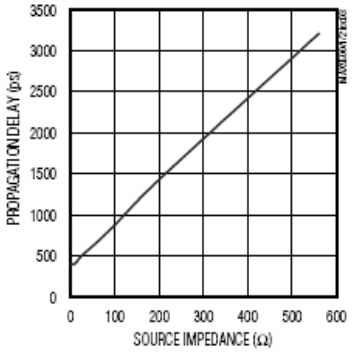
PROPAGATION DELAY vs. INPUT OVERDRIVE (V_{CC} = 10mV TO 100mV)



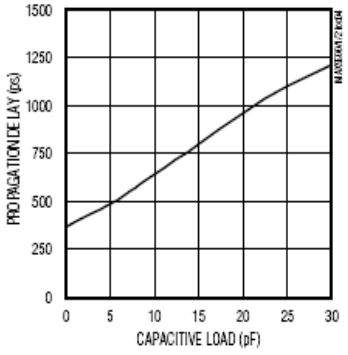
PROPAGATION DELAY vs. INPUT OVERDRIVE (V_{OD} = 0.1V TO 2V)



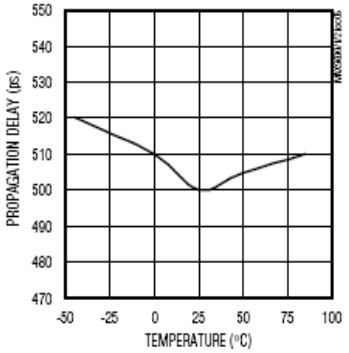
PROPAGATION DELAY vs. SOURCE IMPEDANCE



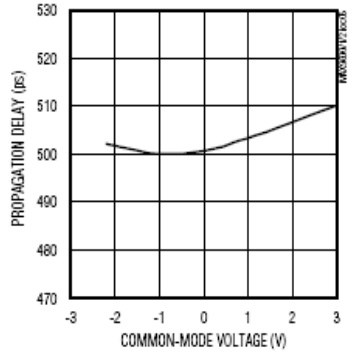
PROPAGATION DELAY vs. CAPACITIVE LOAD



PROPAGATION DELAY vs. TEMPERATURE



PROPAGATION DELAY vs. COMMON-MODE VOLTAGE

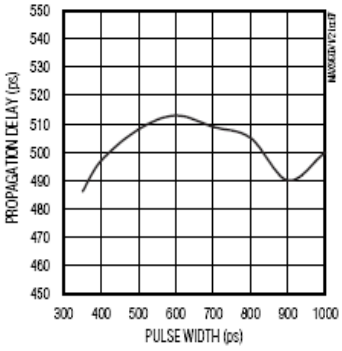


Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

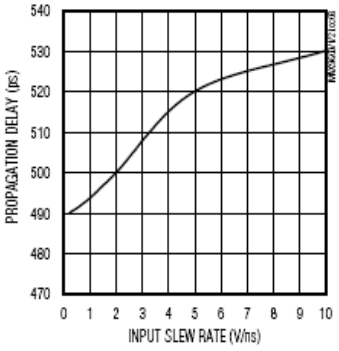
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS_ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE\_}$ = high (MAX9600/MAX9601), C_L = 5pF, GND = 0V, R_L = 50Ω to -2V (MAX9600), $V_{CCO\_}$ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), input slew rate = 2V/ns, duty cycle = 50%, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

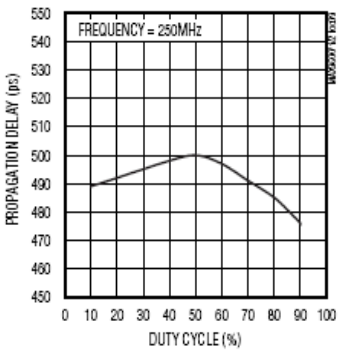
PROPAGATION DELAY vs. PULSE WIDTH



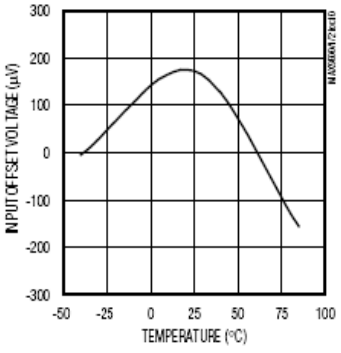
PROPAGATION DELAY vs. INPUT SLEW RATE



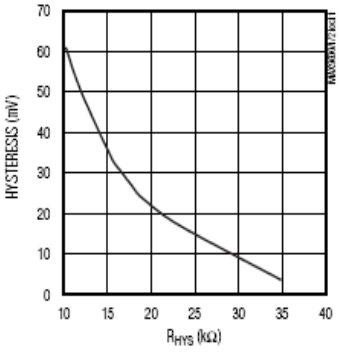
PROPAGATION DELAY vs. DUTY CYCLE



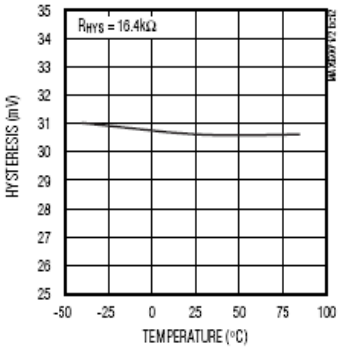
INPUT OFFSET VOLTAGE vs. TEMPERATURE



HYSTERESIS vs. R_{HYS} TO GND



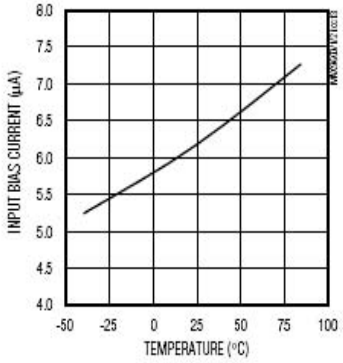
HYSTERESIS vs. TEMPERATURE



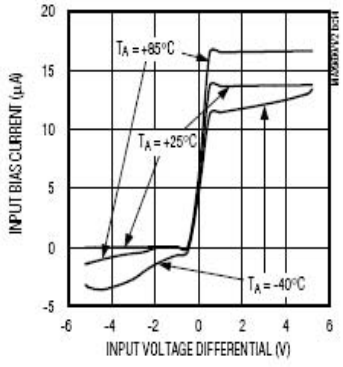
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = -5.2V, V_{CM} = 0V, HYS_ = open (MAX9600/MAX9601), LE_ = low, $\overline{LE}$_ = high (MAX9600/MAX9601), C_L = 5pF, GND = 0V, R_L = 50Ω to -2V (MAX9600), V_{CCO}_ = 5V, R_L = 50Ω to 3V (MAX9601/MAX9602), input slew rate = 2V/ns, duty cycle = 50%, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

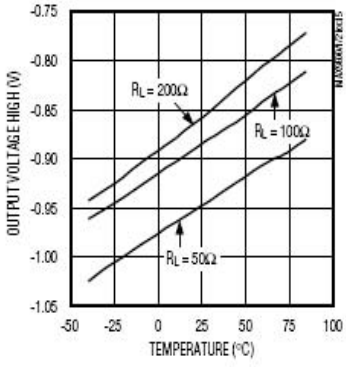
INPUT BIAS CURRENT vs. TEMPERATURE



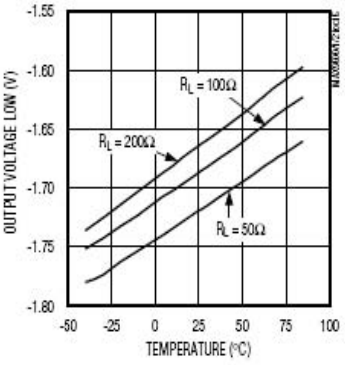
INPUT BIAS CURRENT vs. INPUT VOLTAGE DIFFERENTIAL



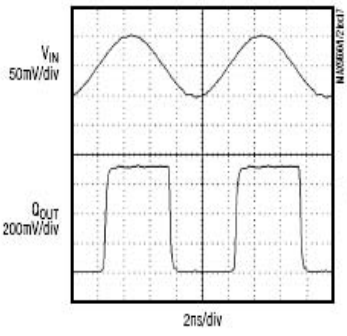
OUTPUT VOLTAGE HIGH vs. TEMPERATURE



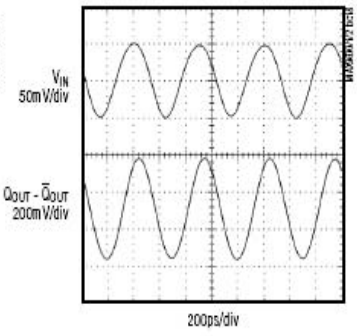
OUTPUT VOLTAGE LOW vs. TEMPERATURE



OUTPUT RESPONSE TO 100MHz INPUT



OUTPUT RESPONSE TO 4Gbps INPUT



Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

Timing Diagram

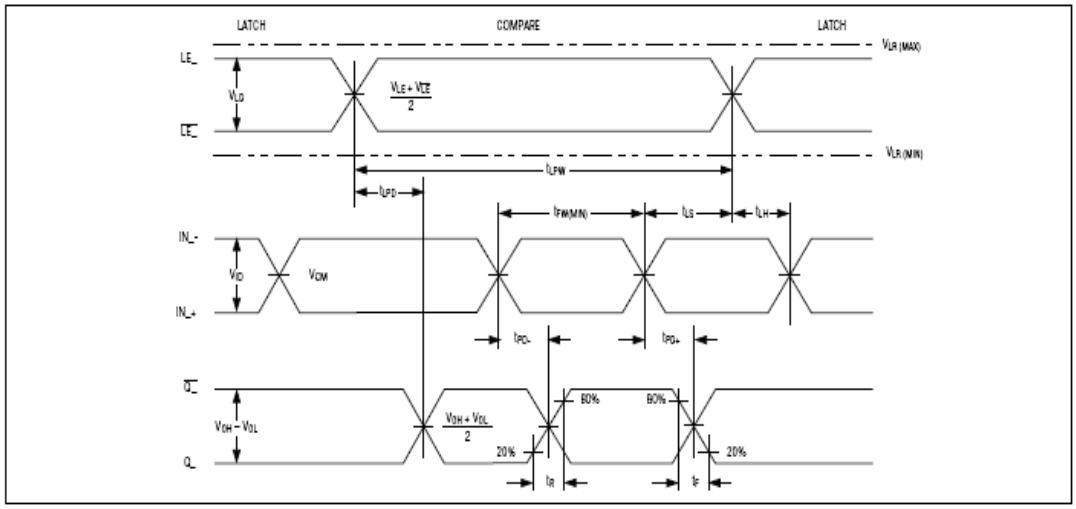


Figure 1. MAX9600/MAX9601/MAX9602 Timing Diagram

Pin Descriptions

MAX9600/MAX9601

PIN		NAME	FUNCTION
MAX9600	MAX9601		
1	1	QA	Channel A Output
2	2	$\overline{QA}$	Channel A Complementary Output
3	—	GND	Channel A Output Ground
—	3	V_{CCOA}	Channel A Output Driver Positive Supply
4	4	LEA	Channel A Latch-Enable Input
5	5	$\overline{LEA}$	Channel A Latch-Enable Complementary Input
6, 15	6, 15	V_{EE}	Negative Supply Voltage
7, 14	7, 14	V_{CC}	Positive Supply Voltage
8	8	HYSA	Channel A Hysteresis Input
9	9	INA-	Channel A Minus Input
10	10	INA+	Channel A Plus Input
11	11	INB+	Channel B Plus Input
12	12	INB-	Channel B Minus Input
13	13	HYSB	Channel B Hysteresis Input
16	16	$\overline{LEB}$	Channel B Latch-Enable Complementary Input
17	17	LEB	Channel B Latch-Enable Input
18	—	GND	Channel B Output Ground
—	18	V_{CCOB}	Channel B Output Driver Positive Supply
19	19	$\overline{QB}$	Channel B Complementary Output
20	20	QB	Channel B Output

Pin Descriptions (continued)

MAX9602

PIN	NAME	FUNCTION
1	INA+	Channel A Plus Input
2	INA-	Channel A Minus Input
3, 9	V_{EE}	Negative Supply Voltage
4	INB+	Channel B Plus Input
5	INB-	Channel B Minus Input
6, 12	V_{CC}	Positive Supply Voltage
7	INC+	Channel C Plus Input
8	INC-	Channel C Minus Input
10	IND+	Channel D Plus Input
11	IND-	Channel D Minus Input
13	$\overline{QD}$	Channel D Complementary Output
14	QD	Channel D Output
15	V_{CCOD}	Channel D Output Driver Positive Supply
16	$\overline{QC}$	Channel C Complementary Output
17	QC	Channel C Output
18	V_{CCOC}	Channel C Output Driver Positive Supply
19	$\overline{QB}$	Channel B Complementary Output
20	QB	Channel B Output
21	V_{CCOB}	Channel B Output Driver Positive Supply
22	$\overline{QA}$	Channel A Complementary Output
23	QA	Channel A Output
24	V_{CCOA}	Channel A Output Driver Positive Supply

Detailed Description

The MAX9600/MAX9601/MAX9602 ultra-high-speed comparators feature extremely low propagation delay (500ps). These dual and quad comparators minimize channel-to-channel skew (10ps) and are designed for low propagation delay dispersion. These features make them ideal for applications where high-fidelity tracking of narrow pulses and low timing dispersion is critical. The devices operate from either standard supply levels of -5.2V/+5V or shifted levels of -4.2V/+6V.

The differential input stage accepts a wide range of signals in the common-mode range from (V_{EE} + 3V) to (V_{CC} - 2V) with a CMRR of 70dB (typ). The outputs are complementary digital signals, compatible with ECL and PECL systems, and provide sufficient current to directly drive transmission lines terminated in 50Ω. The ultra-fast operation makes signal processing possible at a data rate up to 4Gbps. Figure 2 shows a 1Gbps (500MHz) example with an input-signal level of 100mV_{P-P}.

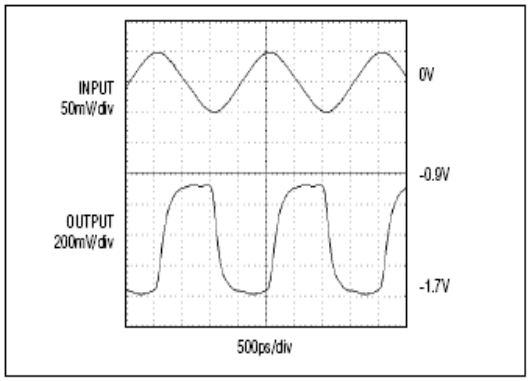


Figure 2. Signal Processed at 500MHz with Input-Signal Level of 100mV_{RMS}.

Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

The MAX9600/MAX9601 incorporate latch-enable and hysteresis control. Hysteresis rejects noise and prevents oscillations on low-slew input signals. The latch-enable control permits tracking or sampling mode of operations. Drive the complementary latch enable with standard ECL logic for MAX9600 and PECL logic for MAX9601. The MAX9602 quad-channel PECL output comparator does not include the latch-enable or hysteresis control functions.

Applications Information

Layout

Special layout precautions exist due to the large gain-bandwidth characteristic of the MAX9600/MAX9601/MAX9602. Use a printed circuit board with a good, low-inductance ground plane. Mount 0.01µF ceramic decoupling capacitors as close to the power-supply inputs as possible. Minimize lead lengths on the inputs and outputs to avoid unwanted parasitic feedback around the comparators. Use surface-mount chip components to minimize lead inductance. Pay close attention to the bandwidth of the decoupling and terminating components.

Use microstrip layout and terminations at the input and output. Avoid discontinuities in differential impedance. Maximize common-mode noise immunity by maintaining the distance between differential traces and avoid sharp corners. Minimize the number of vias to prevent impedance discontinuities. Match the electrical length of the traces to minimize skew.

Input Slew-Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of these devices can create oscillation problems when the input goes through the threshold region. This is typically due to parasitic paths, which cause positive feedback to occur. For clean switching without oscillation or steps in the output waveform for the MAX9600/MAX9601, use an input with a slew rate of 5V/µs or faster. For the MAX9602, use a slew rate of 25V/µs or faster. The tendency of the part to oscillate is a function of the layout and source impedance of the circuit employed. Poor layout and larger source impedance increases the minimum slew-rate requirement. Adding hysteresis accommodates slower inputs (see the *Hysteresis* section).

Hysteresis (MAX9600/MAX9601)

Hysteresis can be introduced to prevent oscillation or multiple transitions due to noise. The MAX9600/MAX9601 feature current-controlled hysteresis, which is set by placing a resistor between HYS_ and GND. The value of the current-setting resistor is determined by the output voltage of 2.5V at HYS_ divided by the desired hysteresis current level in the range of 0 to 200µA. R_{HYS} of 10kΩ to 35kΩ resistors provides hysteresis of 60mV to 5mV (see the Hysteresis vs. R_{HYS} to GND graph in the *Typical Operating Characteristics* section). For a zero hysteresis (0µA hysteresis current), leave HYS_ open or connect it to V_{CC}.

Propagation Delay Dispersion

Propagation delay dispersion is defined as a variation in propagation delay as a function of change in input conditions. In an automatic test system pin-driver electronics, for example, the dispersion determines the maximum edge resolution.

Many factors can affect the dispersion, such as common-mode voltage, overdrive, input slew rate, duty cycle, and pulse width. The typical propagation delay dispersions of the MAX9600/MAX9601/MAX9602 are less than 10ps to 40ps (see the *Typical Operating Characteristics* and *Electrical Characteristics* sections).

Comparators with Latch Enable (MAX9600/MAX9601)

The latch-enable function allows the comparator to be used in a sampling mode. When LE_ is low ($\overline{LE}$_ is high), the comparator tracks the input signal. When LE_ is driven high ($\overline{LE}$_ is low), the outputs are forced to an unambiguous logic state, dependent on the input conditions at the time of the latch input transition. If the latch-enable function is not used, connect the appropriate LE_ input to a low ECL/PECL logic, and its complementary $\overline{LE}$_ input to a high ECL/PECL logic level (see Table 1).

The input range of the MAX9600 differential latch-enable inputs is 400mV to 2V. The logic-input swing excursion must fall within an input-voltage range (V_{LR}) of -2V to 0 to work properly. The input range of the MAX9601 differential latch-enable inputs is 250mV to 3.5V. The logic-input swing excursion must fall within an input-voltage range (V_{LR}) of 0 to 3.5V for ($V_{CCO\_}$ < 3.5V) or V_{LR} of ($V_{CCO\_}$ - 3.5V) to $V_{CCO\_}$ for ($V_{CCO\_}$ ≥ 3.5V) to work properly.

Table 1. Latch-Enable Truth Table

LATCH-ENABLE INPUT		OPERATION
LE_	$\overline{LE}$_	
0	1	Compare Mode. Output follows input state.
1	0	Latch Mode. Output latches to last known output state.
0	0	Invalid condition, output is in unknown state.
1	1	

Timing Information (MAX9600/MAX9601)

The timing diagram (Figure 1) illustrates the operation of a comparator with latch enable. The top line of the diagram illustrates a latch-enable pulse. Initially, the latch-enable input (LE, $\overline{LE}$_) is differentially high, which places the comparator in latch mode. When the input signal (IN_+, IN_-) switches from low to high, the output (Q_, $\overline{Q}$_) remains latched to the previous low state. When the latch-enable input goes differentially low, starting the compare function, the output responds to the input and transitions to high after a time (t_{LPD}). The leading edges of the subsequent input signal switch the comparator after time interval t_{PD+} or t_{PD-} (depending on the direction of the input transitions) until a high latch-enable pulse places the device in latch mode again. The input signal must occur at minimum time (t_{LS}) before the latch rising edge, and must maintain its state for at least t_{LH} after the rising edge. A minimum latch-pulse width (t_{LPW}) of 250ps (typ) is needed for proper latch operation.

ECL/PCL

The MAX9600/MAX9601/MAX9602 outputs are emitter followers that require external resistive connections to a voltage source (V_T) more negative than the lowest V_{OL} for proper static and dynamic operation. When properly terminated, the outputs provide appropriate levels, V_{OL} or V_{OH}, for ECL (MAX9600) or PECL (MAX9601/MAX9602). Output-current polarity always sinks into the termination scheme during proper operation.

ECL-output signal levels are referenced to GND, and PECL-output signals are referenced to $V_{CCO\_}$.

Chip Information

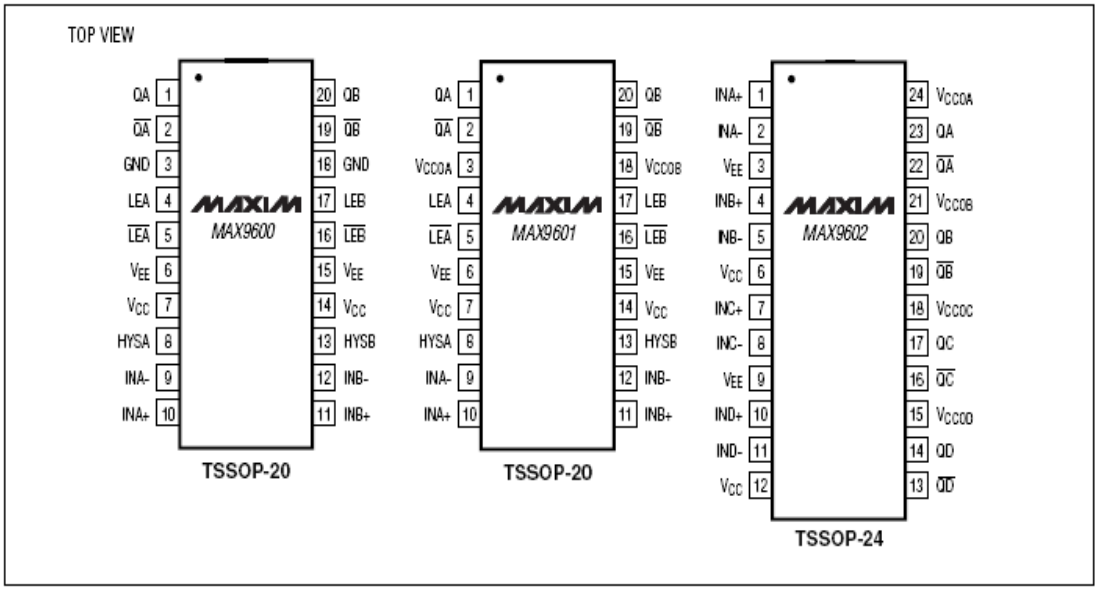
MAX9600 TRANSISTOR COUNT: 558

MAX9601 TRANSISTOR COUNT: 600

MAX9602 TRANSISTOR COUNT: 608

PROCESS: Bipolar

Pin Configurations

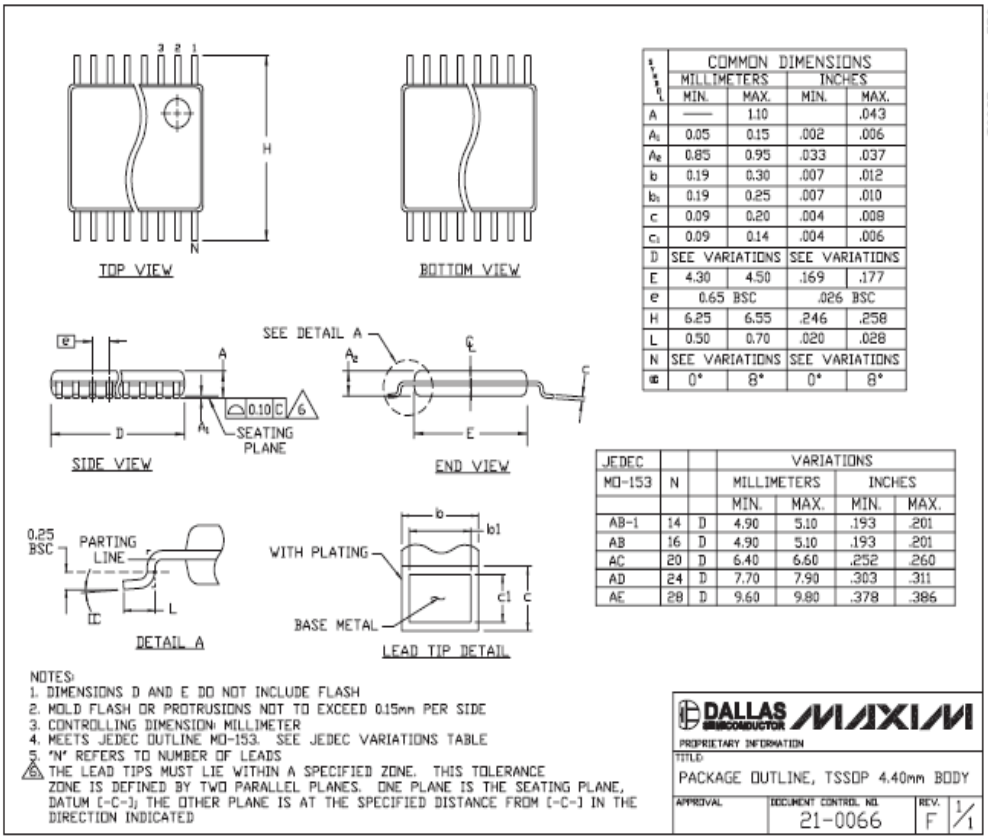


Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY
APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV. F | 1/1

EM4 DFB LASER DIODE DATASHEET

This section of Appendix B consists of the datasheet for the DFB laser diode.

EM4

High Power 14 Pin DFB Laser

Features

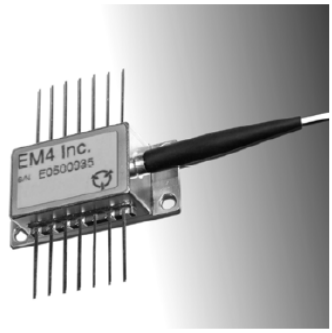
- ITU grid wavelengths
- Up to 80mW of output power
- Low RIN
- PM Fiber
- Laser welded, epoxy free and hermetically sealed
- Built in thermistor and monitor detector
- Telcordia GR-468 Core / MIL-Std 883 compliant

Applications

- Long haul WDM transmission
- RF Links
- Seeding
- CATV

General Description

The EM4 high power distributed feedback laser (DFB) is a CW InGaAsP/InP multi-quantum well (MQW) laser diode. The module is ideal in applications where high power, low RIN and stable PM properties are needed. The module contains a cooler, thermistor, monitor detector and bias-T for SBS prevention using low speed modulation techniques. The module is designed and built using EM4s high reliability platform for defense components.



Ordering Information

(See channel table on page 4 for wavelength information)

Part	Output Power [mW]	Wavelength [nm]
EM253-080-YYY	80	See channel table
EM253-063-YYY	63	See channel table
EM253-050-YYY	50	See channel table
EM253-040-YYY	40	See channel table

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or conditions beyond these are not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

Parameter	Sym	Condition	Min	Max	Unit
Storage Temperature	T_{STG}		-40	85	°C
Operating Case Temperature	T_{OP}		-20	70	°C
Laser Forward Current	I_F			600	mA
Laser Reverse Voltage	V_R			2	V
Photo Diode Forward Current	I_{PD}			10	mA
Photo diode Reverse Voltage	V_{PD}			20	V
TEC Current	I_{TEC}			3.0	A
TEC Voltage	V_{TEC}			6.0	V
Thermistor Current				2	mA
Thermistor Voltage				5	V
Lead Soldering Time				10	s
Lead Soldering temperature				250	°C
ESD		HBM		500	V

Optical And Electrical Characteristics

T_{OP}=25°C, continous wave and beginning of life unless otherwise specified.

Parameter	Sym.	Condition	Min	Typ.	Max	Unit
Operating Chip Temperature	T_{CHIP}		20		35	°C
Threshold Current	I_{TH}			50		mA
Laser Drive Current	I_{OP}			375	500	mA
Laser Forward Voltage	V_F	I= I_{MAX}			3	V
Output Power	P_{OP}	EM253-080-YYY, I=I_{OP}	80			mW
		EM253-063-YYY, I=I_{OP}	63			
		EM253-050-YYY, I=I_{OP}	50			
		EM253-040-YYY, I=I_{OP}	40			
Center Wavelength	λ	P=P_{OP}	See ordering information			nm
Linewidth	Δ υ			1		MHz
Relative Intensity Noise	RIN	P=P_{OP}, 0.2GHz→14GHz			-150	dB/Hz
Side Mode Suppression	SMSR	P=P_{OP}	30			dB
Optical Isolation	ISO		30	35		dB
Polarization Extinction Ratio	PER		17	21		dB
Monitor Photo Diode Current	I_{PD}		100			μA
Monitor Photo Diode Dark Current	I_D				100	nA
Tracking Error			-0.5		0.5	dB
Modulation Input Bandwidth	F			1		GHz
Modulation Input Reflection	S_{11}				-7	dB
Modulation Input Matching	Z_{IN}			25		Ω
TEC Current		T_{OP}=70°C, P=P_{OP}, T_{CHIP}=25°C			2.5	A
TEC Voltage		T_{OP}=70°C, P=P_{OP}, T_{CHIP}=25°C			4	V
Thermistor Resistance	R_{TH}	T=25°C	9500	10000	10500	Ω
Thermistor β coefficient	β	0 / 50°C		3892		

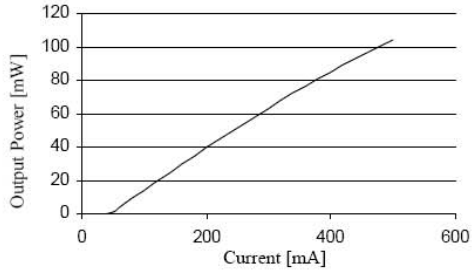
Fiber Specification

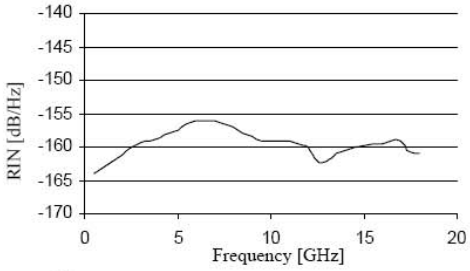
Parameter	Typ.	Unit
Fiber Type	PM	-
Connector Type	FC/APC	-
Core Diameter	8	μm
Outer Diameter	125	μm

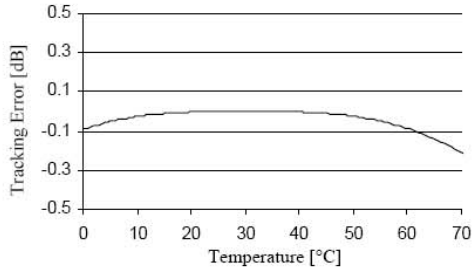
Parameter	Typ.	Unit
Buffer Diameter	250	μm
Buffer Material	Acrylate	-
Minimum Pigtail Length	1	m
Minimum Bend Radius	35	mm

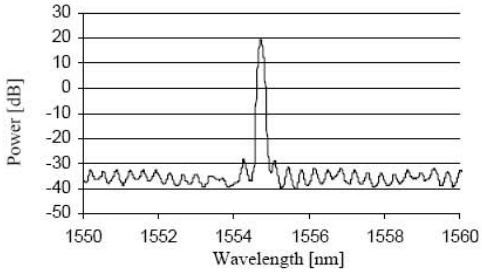
Typical Operating Characteristics

T_C=25°C



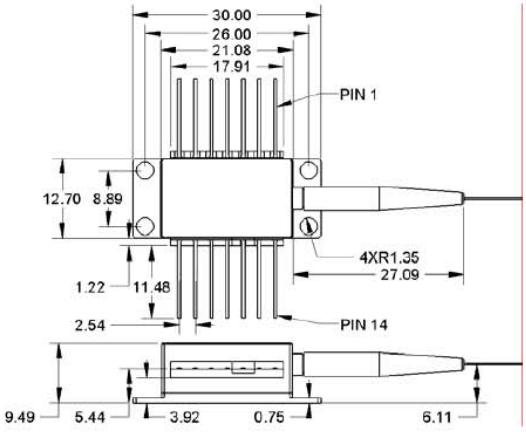






Mechanical Drawing

All units in mm



Pinning

Pin	Description
1	Thermistor
2	Thermistor
3	Laser Cathode (Bias)
4	Monitor PD Anode
5	Monitor PD Cathode
6	TEC +
7	TEC -
8	Case GND, Laser Anode
9	Case GND, Laser Anode
10	Case GND, Laser Anode
11	Case GND, Laser Anode
12	Laser Cathode (modulation)
13	Case GND, Laser Anode
14	Case GND, Laser Anode

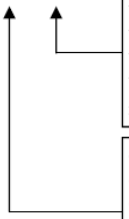
OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC DEVICES

EM4

High Power 14 Pin DFB Laser

Ordering Information

EM253-XXX-YYY



Wavelength channel
YYY: 1515-1600nm
YY1: 1515-1530nm
YY2: 1530-1545nm
YY3: 1545-1560nm
nnn: Channel number

Output Power
080: 80mW
063: 63mW
050: 50mW
040: 40mW

For pricing and delivery information, please contact EM4 inc. direct at +1 781 275 75 01, sales@em4inc.com or any of the representatives listed at www.em4inc.com.

The component complies with all applicable portions of 21 CFR 1040.10, 21 CFR 1010.2 and 21 CFR 1010.3. Since this is a component, it does not comply with all of the requirements contained in 21 CFR 1040.10 and 21 CFR 1040.11 for complete laser products.

Channel Table

Ch.	F [THz]	λ [nm]	Ch.	F [THz]	λ [nm]	Ch.	F [THz]	λ [nm]	Ch.	F [THz]	λ [nm]	Ch.	F [THz]	λ [nm]
001	196.00	1529.55	041	194.00	1545.32	081	192.00	1561.42	121	190.00	1577.86	161	188.00	1594.64
002	195.95	1529.94	042	193.95	1545.72	082	191.95	1561.83	122	189.95	1578.27	162	187.95	1595.06
003	195.90	1530.33	043	193.90	1546.12	083	191.90	1562.23	123	189.90	1578.69	163	187.90	1595.49
004	195.85	1530.72	044	193.85	1546.52	084	191.85	1562.64	124	189.85	1579.10	164	187.85	1595.91
005	195.80	1531.12	045	193.80	1546.92	085	191.80	1563.05	125	189.80	1579.52	165	187.80	1596.34
006	195.75	1531.51	046	193.75	1547.32	086	191.75	1563.45	126	189.75	1579.93	166	187.75	1596.76
007	195.70	1531.90	047	193.70	1547.72	087	191.70	1563.86	127	189.70	1580.35	167	187.70	1597.19
008	195.65	1532.29	048	193.65	1548.11	088	191.65	1564.27	128	189.65	1580.77	168	187.65	1597.62
009	195.60	1532.68	049	193.60	1548.51	089	191.60	1564.68	129	189.60	1581.18	169	187.60	1598.04
010	195.55	1533.07	050	193.55	1548.91	090	191.55	1565.09	130	189.55	1581.60	170	187.55	1598.47
011	195.50	1533.47	051	193.50	1549.32	091	191.50	1565.50	131	189.50	1582.02	171	187.50	1598.89
012	195.45	1533.86	052	193.45	1549.72	092	191.45	1565.90	132	189.45	1582.44	172	187.45	1599.32
013	195.40	1534.25	053	193.40	1550.12	093	191.40	1566.31	133	189.40	1582.85	173	187.40	1599.75
014	195.35	1534.64	054	193.35	1550.52	094	191.35	1566.72	134	189.35	1583.27	174	187.35	1600.17
015	195.30	1535.04	055	193.30	1550.92	095	191.30	1567.13	135	189.30	1583.69	175	187.30	1600.60
016	195.25	1535.43	056	193.25	1551.32	096	191.25	1567.54	136	189.25	1584.11	176	187.25	1601.03
017	195.20	1535.82	057	193.20	1551.72	097	191.20	1567.95	137	189.20	1584.53	177	187.20	1601.46
018	195.15	1536.22	058	193.15	1552.12	098	191.15	1568.36	138	189.15	1584.95	178	187.15	1601.88
019	195.10	1536.61	059	193.10	1552.52	099	191.10	1568.77	139	189.10	1585.36	179	187.10	1602.31
020	195.05	1537.00	060	193.05	1552.93	100	191.05	1569.18	140	189.05	1585.78	180	187.05	1602.74
021	195.00	1537.40	061	193.00	1553.33	101	191.00	1569.59	141	189.00	1586.20	181	187.00	1603.17
022	194.95	1537.79	062	192.95	1553.73	102	190.95	1570.01	142	188.95	1586.62	182	186.95	1603.60
023	194.90	1538.19	063	192.90	1554.13	103	190.90	1570.42	143	188.90	1587.04	183	186.90	1604.03
024	194.85	1538.58	064	192.85	1554.54	104	190.85	1570.83	144	188.85	1587.46	184	186.85	1604.46
025	194.80	1538.98	065	192.80	1554.94	105	190.80	1571.24	145	188.80	1587.88	185	186.80	1604.88
026	194.75	1539.37	066	192.75	1555.34	106	190.75	1571.65	146	188.75	1588.30	186	186.75	1605.31
027	194.70	1539.77	067	192.70	1555.75	107	190.70	1572.06	147	188.70	1588.73	187	186.70	1605.74
028	194.65	1540.16	068	192.65	1556.15	108	190.65	1572.48	148	188.65	1589.15	188	186.65	1606.17
029	194.60	1540.56	069	192.60	1556.55	109	190.60	1572.89	149	188.60	1589.57	189	186.60	1606.60
030	194.55	1540.95	070	192.55	1556.96	110	190.55	1573.30	150	188.55	1589.99	190	186.55	1607.04
031	194.50	1541.35	071	192.50	1557.36	111	190.50	1573.71	151	188.50	1590.41	191	186.50	1607.47
032	194.45	1541.75	072	192.45	1557.77	112	190.45	1574.13	152	188.45	1590.83	192	186.45	1607.90
033	194.40	1542.14	073	192.40	1558.17	113	190.40	1574.54	153	188.40	1591.26	193	186.40	1608.33
034	194.35	1542.54	074	192.35	1558.58	114	190.35	1574.95	154	188.35	1591.68	194	186.35	1608.76
035	194.30	1542.94	075	192.30	1558.98	115	190.30	1575.37	155	188.30	1592.10	195	186.30	1609.19
036	194.25	1543.33	076	192.25	1559.39	116	190.25	1575.78	156	188.25	1592.52	196	186.25	1609.62
037	194.20	1543.73	077	192.20	1559.79	117	190.20	1576.20	157	188.20	1592.95	197	186.20	1610.06
038	194.15	1544.13	078	192.15	1560.20	118	190.15	1576.61	158	188.15	1593.37	198	186.15	1610.49
039	194.10	1544.53	079	192.10	1560.61	119	190.10	1577.03	159	188.10	1593.79	199	186.10	1610.92
040	194.05	1544.92	080	192.05	1561.01	120	190.05	1577.44	160	188.05	1594.22	200	186.05	1611.35

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