SENSITIVITY ANALYSIS OF ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS TO PROCESS VARIATION

THESIS

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Abstract

A sensitivity analysis of AlGaN/GaN HEMT performance on material and process variations was performed. Aluminum mole fraction, barrier thickness, and gate length were varied ± 5% over nominal values to determine how sensitive simulated device performance was to changes in these 3 parameters. Simulated data was generated with the Synopsys TCAD software suite using a physics-based HEMT model. To validate model performance, simulated data was correlated with experimental data, which consisted of wafer epilayer characterization data as well as DC and small-signal RF device performance data from 1-26 GHz.

Trends were observed in the experimental data due to variations in the fabrication process. Epilayer data showed cross-wafer trends in sheet resistance, barrier thickness and aluminum mole fraction but did not show any discernable trends in mobility or sheet carrier concentration. Maximum output current was the only measured performance metric that showed a strong trend across the wafers. Data from two different device geometries on the same wafers were compared to determine whether performance variations across a wafer could be attributed to epilayer variation or device geometry. Variation in power and current gain cutoff frequencies was attributed to differences in the device geometry whereas variations in maximum output current was correlated to sheet resistance and barrier thickness variation.

Simulated device performance showed varying sensitivities when ± 5% changes in aluminum mole fraction, barrier thickness, and gate length were made. Aluminum

mole fraction and barrier thickness had a large effect on DC output up to 40%, while the gate length only moderately effected DC output by 2-3%. However, of all 3 parameters, changes in aluminum mole fraction and gate length had the greatest effect on the RF performance (1-6%) while RF performance was negligibly affected by changes in aluminum mole fraction and barrier thickness. Although varying these three parameters affects device performance, variation in these three parameters alone is insufficient to accurately account for variations in measured device performance.

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HIGH ELECTRON MOBILITY TRANSISTORS TO PROCESS VARIATION

Chapter 1. Introduction

1.1 Introduction

Although solid state electronics have largely replaced vacuum-tube driven electronics over the last quarter century there is one area where they still consistently fall short. High-power radio frequency (RF) devices for microwave and millimeter-wave applications in large-scale communications and radar systems are still in limited supply. Systems requiring high RF power levels at frequencies above 100 GHz along with the ability to operate at high temperatures (greater than 250 °C) are still overwhelmingly driven by microwave tubes [1]. Research into solid-state devices that can meet these harsh requirements, specifically transistors made using wide bandgap materials, is an important area of study right now.

Wide bandgap semiconductors have several distinct advantages over conventional silicon (Si) or gallium arsenide (GaAs) including higher electrical breakdown fields, and the ability to sustain stable DC and RF operation at very high temperatures. There are several wide bandgap material systems that are currently the focus of the majority of research including silicon carbide (SiC), aluminum nitride (AlN), indium nitride (InN) and gallium nitride (GaN).

The AlGaN/GaN HEMT (High Electron Mobility Transistor) is the most popular of the wide bandgap devices being studied right now for many reasons. The two-

dimensional electron gas (2DEG) that occurs at the AlGaN/GaN heterointerface has a high sheet carrier concentration ($n_s \sim 10^{13}$cm^{-2}) as well as high electron mobility ($\mu_n \sim$ 1500 cm^2/V-s) and high saturation velocity ($v_s \sim 2 \times 10^7$ cm/s) [1]. These characteristics allow the HEMT to produce high RF current, which, along with GaN's exceptional critical breakdown field (35 x 10^5 V/cm) for high voltage operation, results in high RF power operation [2].

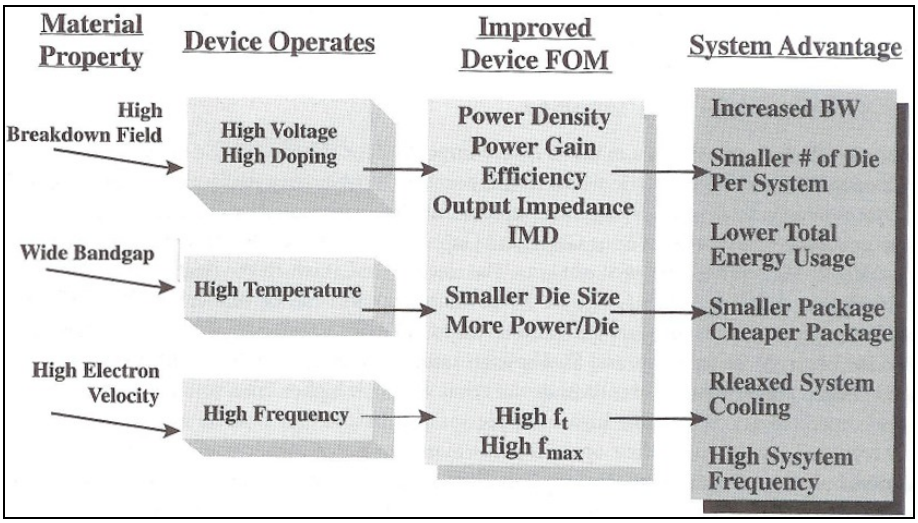

Figure 1: Relationship between material properties and device and system level performance for transistors and systems using GaN [2]

1.2 Motivation

GaN production is still in its infancy when compared to conventional semiconductors like Si and GaAs and is a much more complex process which can make repeatability between individual wafers, and even across the same wafer, more difficult than with Si. This often results in variation of key material parameters and geometry between devices of the same design. Variation in these parameters can lead to undesired

material properties and unexpected device topologies. Alloy mole fraction, layer thickness, and device geometry are just a few of the parameters that can vary when fabricating a device. What is unknown is how sensitive device performance is to variations in these parameters. Which parameters significantly affect simulated device performance? What trends exist in device performance relative to these interdependent material and process parameters? These are important questions to answer in order to determine both how much process variation is tolerable, and where to focus process improvement efforts.

1.3 Problem Statement

Process variations during wafer growth and device fabrication can result in non-uniformity of key device parameters. This non-uniformity results in non-optimal, inconsistent device performance. A comparison will be made between these parameters using both measured and simulated device output data to determine which has the greatest impact on device performance. An assessment will also be made as to whether or not variation in the studied parameters is adequate to explain the variation seen in the performance of measured devices.

1.4 Scope and Assumptions

Given a commercial device manufacturer's baseline structure, material and process variability will be mapped to device performance variability. Technology Computer Aided Design (TCAD) device performance data will be correlated to measured device performance data. This correlation will be used to map the variability of these

device parameters that can result from the fabrication processes to final measured device performance variations.

This thesis focused on variation of the following three parameters within a range of ± 5% from nominal values: 1) aluminum mole fraction (Al%), 2) AlGaN barrier thickness (d_{AlGaN}), and 3) gate length (L_g). These parameters were chosen based on several factors. The available measured data includes these parameters and they are also more readily implemented in the extremely complicated Synopsys TCAD simulation environment. Additionally, after discussions with local experts from both AFIT and the Air Force Research Laboratory it was decided that these are a good starting place, which will leave open possibilities for future researchers.

This thesis was written under the assumption that the reader has a basic understanding of semiconductor physics as well as a basic understanding of S-parameters and their meaning, along with how to interpret Smith charts.

1.5 Thesis Organization

The next chapter of this thesis covers the background information necessary to understand the results of this research. A discussion of heterostructures, HEMT structure, GaN properties, and fabrication processes are included. There is also a literature review included in chapter 2 that covers some of the current research that applies to this thesis. Chapter 3 covers the methodology used to complete the research as well as a detailed explanation of the TCAD code used. The analysis of the results, including comparison of measured to simulated data will be discussed in chapter 4. Finally, a conclusion and a look at future topics will be discussed in the last chapter.

1.6 Chapter Summary

The purpose of this thesis is to determine the sensitivity of AlGaN/GaN HEMTs to variations in the fabrication process. Specifically Al%, barrier thickness, gate and channel dimensions will be varied by ± 5% in a series of Synopsys TCAD simulations and the results will be compared to measured data that has been provided by a device manufacturer. Analysis of the data will result in a clearer picture regarding which process should undergo improvements as well as which parameters do not significantly affect final device performance.

Chapter 2. Background

2.1 Chapter Overview

The purpose of this chapter is to provide relevant background information regarding RF figures of merit, heterostructure and HEMT physics, AlGaN/GaN material characteristics, polarization induced sheet charge, as well as information on wafer and device processing techniques and difficulties.

2.2 RF Figures of Merit (FOMs)

A top level explanation of some key RF FOMs will be useful to understand the RF results of the research. These explanations do not go into great depth but are intended to give the reader a solid starting point. For detailed derivations of these FOMs consult the cited references as the derivations are beyond the scope of this thesis.

2.2.1 Transconductance (g_m)

Transconductance refers simply to the change in device drain output current for a given change in gate input voltage

$$g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{ds}=\text{constant}} \tag{1}$$

and is given in units of millisiemens (mS). Transconductance depends on the geometry of the device as well as the carrier mobility and threshold voltages [3]. Generally increased device width, shortened channel length and a thinner barrier layer will result in higher g_m with the opposite holding true for lower g_m.

2.2.2 Current Gain Cutoff Frequency (f_T)

The cutoff frequency is the frequency at which the small-signal current gain is unity, or the frequency at which the output current is equal to the input current. The cutoff frequency is highly dependent on g_m, gate to channel capacitance (C_i) and L_g as shown in [4]

$$f_T = \frac{g_m}{2\pi(\text{total gate capacitance})} = \frac{v_s}{2\pi(L_g + C_p / ZC_i)} \tag{2}$$

where v_s is the saturation velocity, Z is the gate width and C_p is the parasitic capacitance. Generally f_T can be improved by using a material with a high v_s (AlGaN/GaN), and minimizing L_g and the parasitic capacitances [4].

2.2.3 Power Gain Cutoff Frequency (f_{max})

Current gain cutoff frequency is mainly used as a measure of physical device performance but a more practical measurement of high-frequency performance is the power gain cutoff frequency because it is determined not only by the material system but also the process technology and device design parameters [2]. This is the frequency at which the power gain is unity and is defined as

$$f_{\max} = \frac{f_T}{\sqrt{4 g_{ds} R_{in}}} \tag{3}$$

where g_{ds} is the output conductance and R_{in} is the input resistance of the intrinsic device [2]. The key steps that increase f_{max} are to minimize g_{ds} and the source /gate parasitic resistances as well as the gate to drain capacitance (C_{gd}). Source and gate resistance depend on process technologies but it is common to decrease gate resistance by using mushroom or T gate designs. C_{gd} can be reduced by increasing the gate to drain spacing

(L_{gd}), which also reduces short channel effects, but unfortunately doing so increases the effective L_g of the device. The optimum value for L_{gd} is 2.3 times the value of L_g [2].

2.3 Heterostructures

A heterostructure consists of at least 2 layers of different semiconductor materials. The interface between the two layers is called a heterojunction. Each material has a different bandgap (E_g) which results in offsets at both the conduction (ΔE_C) and valence energy bands (ΔE_V) as shown in Figure 2.

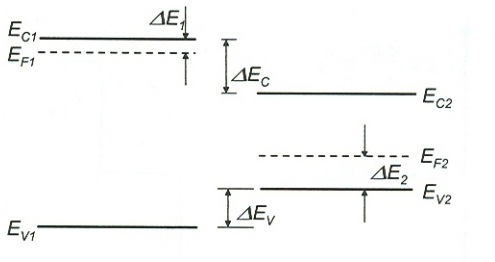

Figure 2: Band offsets between wide and narrow bandgap materials[5].

ΔE_C can also be calculated by

$$\Delta E_C = q(\chi_1 - \chi_2) \tag{4}$$

where χ is the electron affinity of each material. The offsets both contribute to the total bandgap difference (ΔE_g) by

$$\Delta E_g = \Delta E_C + \Delta \mathrm{E_V} \tag{5}$$

ΔE_g is a key factor in the performance of a heterostructure-based device such as a HEMT and generally the higher it is the better [5].

When the two materials are brought into contact the energy bands bend until the device reaches a state of equilibrium, which is indicated by a flat Fermi level (E_F) across

the device. The band bending results in discontinuities in both the conduction and valence bands as shown in the energy band diagram in Figure 3.

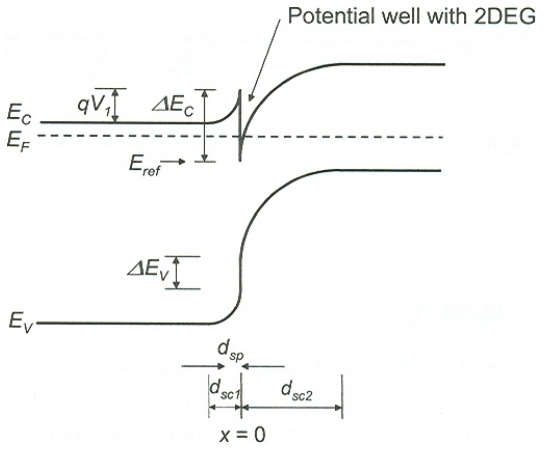

Figure 3: Energy band diagram illustrating the band bending that confines the 2DEG [5]

This discontinuity results in the formation of a two-dimensional electron gas (2DEG) in the conduction band or a two-dimensional hole gas in the valence band in the triangular potential well created on the narrow bandgap (NBG) side of the heterojunction. Due to the much higher mobility of electrons over holes, n-channel devices are almost universally preferred over p-channel and as such this research focuses on n-channel devices which operate using a 2DEG. The 2DEG is formed because electrons become trapped in the potential well which allows movement in only two dimensions parallel to the junction. The 2DEG is exploited in all HEMTs.

The 2DEG is characterized by its sheet carrier concentration (n_s) and the channel mobility. Typically the NBG material is undoped, which results in a much higher mobility at low temperatures in the 2DEG channel than in the bulk material due to

reduced ionized impurity scattering in the channel. Typically there is also a spacer layer placed between the doped wide bandgap (WBG), or barrier layer, and the undoped channel layer. The spacer is typically the same material as the barrier layer and is undoped. The spacer provides further isolation of the 2DEG carriers from their parent donor ions in the barrier layer which enhances channel mobility by reducing the coulomb effect (decreased mobility due to scattering in the material) [5].

2.4 HEMT Basics

HEMTs have a unique structure that exploits the high electron concentration and high mobility of the 2DEG. At its most basic, a HEMT consists one layer of (typically n^+ doped) WBG material on top of one layer of NBG material with a Schottky barrier gate contact as shown in Figure 4.

The Schottky barrier of the gate induces a space charge region (SCR) in the WBG material directly beneath the gate. The heterojunction between the WBG and NBG layers induces a second SCR in the WBG material. Ideally the two SCRs should overlap, fully depleting the WBG of all carriers for proper HEMT operation. All free electrons will be in the 2DEG in the undoped channel layer, exploiting the high mobility due to the absence of the ionized impurity scattering found in the doped WBG material. The majority of all HEMTs are depletion mode devices.

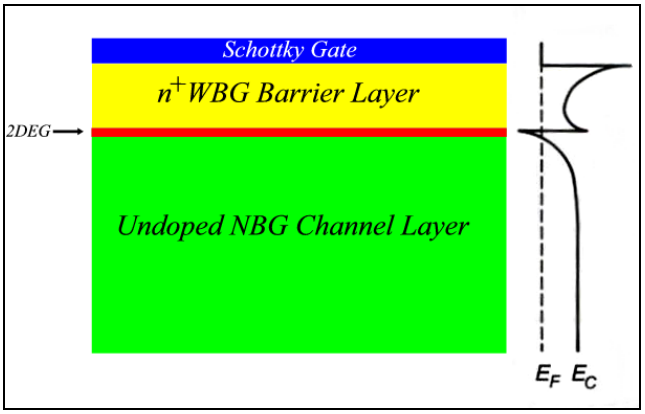

Figure 4: Layer structure and energy band diagram of the area directly underneath the gate of a HEMT (adapted from [5]).

In the event that the SCRs do not fully overlap there will be two conducting channels in the HEMT, one in the highly-doped barrier layer and the other in the undoped channel layer. Both of these channels will contribute to the drain-source current when a drain-source voltage (V_{ds}) is applied, which will affect HEMT turn-on operations. This is undesirable because the WBG layer has a much lower mobility due to ionized impurity scattering from the doping as well as the naturally lower mobility in the WBG layer.

Figure 5 illustrates the formation of a conducting channel in the barrier layer as a result of non-overlapping SCRs. This is overcome by applying a negative bias to the gate contact to the point that the undesired channel in the barrier is totally depleted of free carriers. As such, it is critical that both the barrier layer thickness and bias conditions are properly chosen to ensure complete depletion of the WBG material [5].

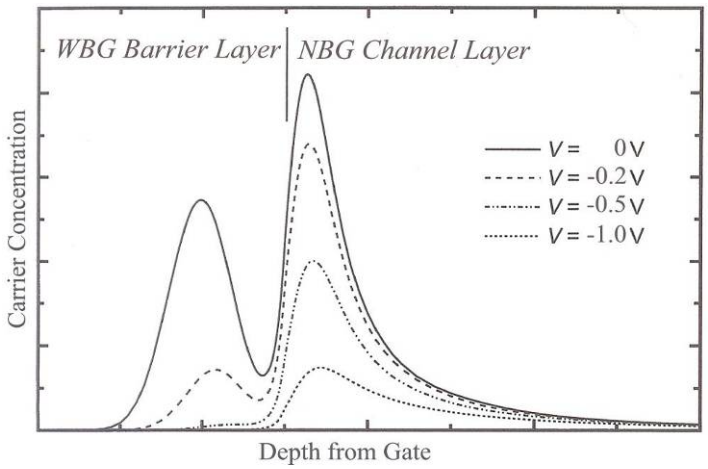

Figure 5: Sheet carrier concentration in both the WBG and NBG layers when the SCRs do not overlap. As a negative voltage is applied to the gate the carriers are pushed out of the barrier layer [5].

As the gate-source voltage (V_{gs}) becomes more negative, it depletes the 2DEG until it reaches a voltage at which point there are no free carriers in the channel and the device is pinched off. n_s is constant throughout the channel when $V_{ds} = 0$. When V_{ds} is applied, current flows through the channel, and the potential throughout the channel (V_x) varies as well. This causes n_s to vary linearly between the source and the drain as given by

$$qn_s(x) = \frac{\varepsilon_{AlGaN}}{d_{AlGaN}}\left[V_{gs} - V_{th} - V(x)\right] \tag{6}$$

with ε_{AlGaN} being the permittivity of the barrier layer and V_{th} is the threshold voltage. The smallest n_s is found at the drain end of the channel with maximum n_s found at the source end as shown in Figure 6 [5].

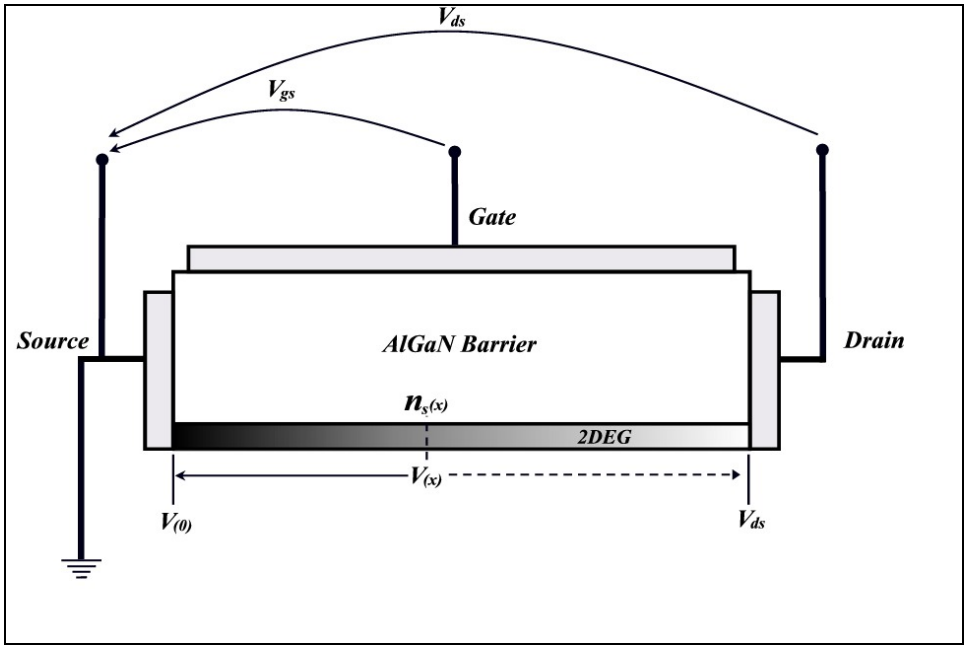

Figure 6: Simple model showing all relevant voltages and contacts, adapted from [5].

2.5 AlGaN/GaN HEMT Structure

Figure 7 shows a generic AlGaN/GaN HEMT structure. The intrinsic AlGaN cap layer is used to increase the distance between the surface and the channel which reduces the effect of surface potential fluctuations on device performance. AlGaN is used instead of GaN for its wider bandgap which can sustain a higher electric field and provides a larger Schottky barrier [6]. Typical Al% values for the cap and barrier layers are between 0.15 and 0.30 in most non-experimental devices. An aluminum nitride (AlN) nucleation layer is included to control the polarity of the GaN and AlGaN layers as well as to overcome the 3% lattice mismatch between the GaN and the SiC (or sapphire) substrate [7, 8].

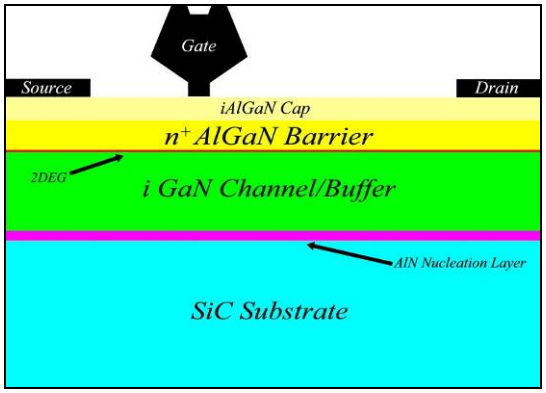

Figure 7: AlGaN/GaN HEMT structure

The gate-drain spacing is much larger than the gate-source spacing to increase the breakdown voltage between the gate and drain. This allows the device to operate at higher voltages [9]. A mushroom or T gate is normally used to improve the high frequency performance of the device. The shorter dimension of the bottom of the gate defines the channel length, which is ideally as short as possible and increases f_T and g_m of the transistor. Additionally, the larger top portion of the gate reduces the gate resistance which improves f_{max} [9].

2.6 GaN Material Characteristics

There are several key material properties that affect the performance of high-speed, high-power and RF devices. Critical field, bandgap, saturation velocity, electron/hole mobility, and thermal conductivity are a few of the properties of concern when choosing a material system for those applications [2].

2.6.1 Critical Field

GaN has a critical field ($\mathcal{E}_c$) of 3.5 MV/cm which is five times that of Si or GaAs and three times that of AlN[2, 10]. $\mathcal{E}_c$ determines breakdown voltage (BV) of the device

$$BV = \frac{\varepsilon \mathcal{E}_c^2}{2qN} \tag{7}$$

where N is the background (or unintentional) doping level on the semiconductor side of the Schottky gate contact near the drain region [2]. If the target BV, is known AlGaN/GaN allows for higher doping levels in the device than conventional semiconductors, as shown in Figure 8, which in turn allows tighter device dimensions. This leads to higher g_m, power gain, f_T, f_{max} and lower parasitic resistances. Lower resistance results in higher device efficiency which translates into lower total power usage per device [2].

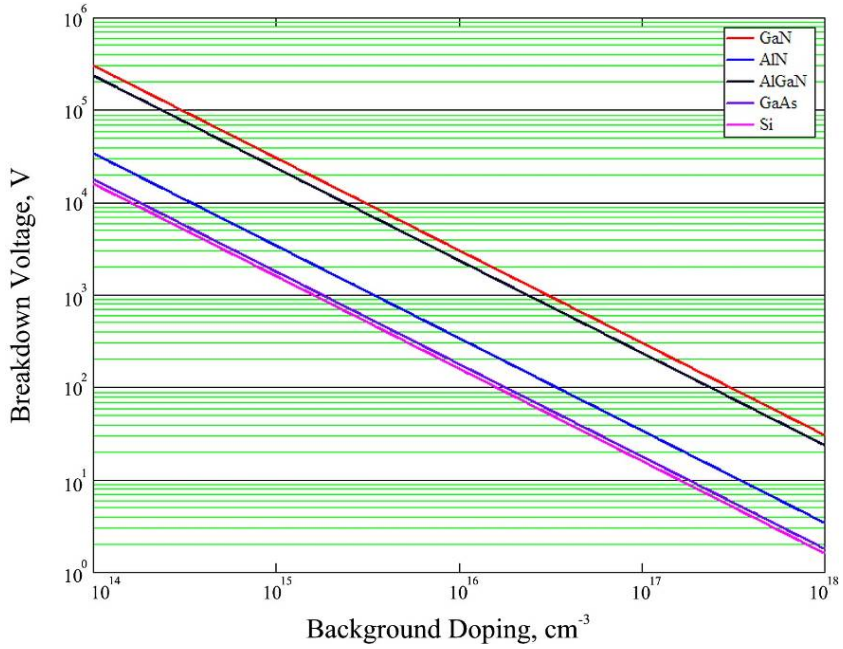

Figure 8: Breakdown voltages of various materials with varied doping levels based on equation 7. GaN allows the highest operating voltage of these materials. AlGaN is shown with an Al mole fraction of 0.25.

2.6.2 Bandgap

GaN has an E_g of 3.4 eV at 300K versus 1.12 and 1.42 for Si and GaAs, respectively. The size of E_g is a determining factor in the upper temperature limit of device operation. The wide E_g of GaN allows it to operate at high temperatures which makes it possible to design small, dense devices that can withstand the heat generated under bias better than conventional group IV materials [2]. AlGaN E_g varies with Al% (x) following [11]

$$E_g(x) = x6.13 + (1-x)3.42 - x(1-x) \text{ eV} . \quad (8)$$

The addition of Al increases E_g further as shown in Figure 9. The Al content is typically between 15-30% [5].

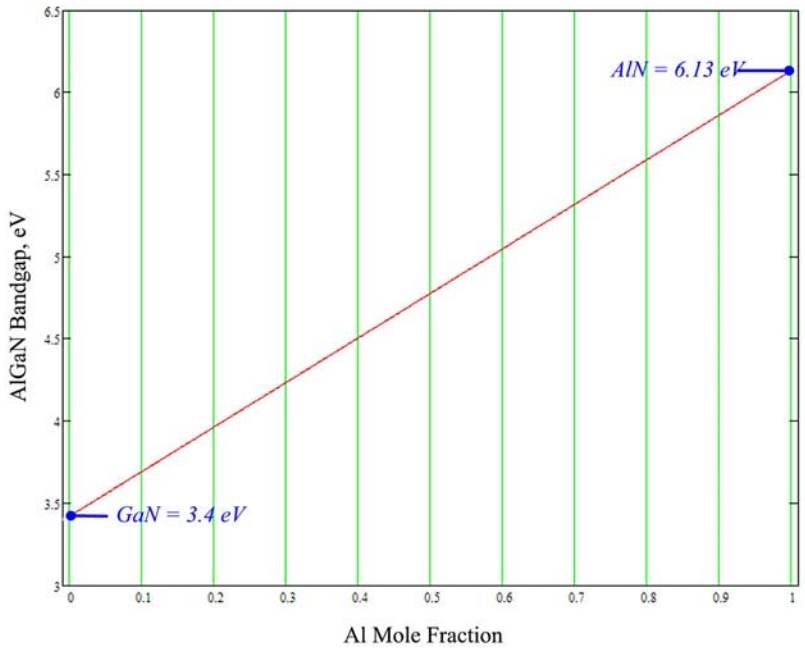

Figure 9: Chart showing how the bandgap changes as a function of Al mole fraction.

2.6.3 Saturation Velocity

Saturation velocity (v_{sat}) is important when working with sub-micron L_g devices because they typically operate at high electric fields. RF performance at very small L_g is largely determined by electron velocity [2]. GaN has a v_{sat} of 2 x 10^7 cm/s, 50% higher than that of Si or GaAs. An associated factor to consider is the electric field at which v_{sat} is reached. GaN saturates at 1.5 x 10^4 V/cm compared to 8 x 10^3 V/cm for silicon. The combination of low mobility and high saturation field for GaN will result in a higher saturation voltage requirement. Therefore wide bandgap devices such as GaN operate most efficiently (in saturation) at higher drain voltages than conventional semiconductors due to the resulting higher knee voltage requirement [2].

2.6.4 Electron Mobility

Electron and hole mobility at 300 K for intrinsic GaN are relatively low at 1000 and 200 cm^2/V-s compared to 1350/6000 and 450/330 cm^2/V-s for Si/GaAs, respectively, while intrinsic AlN has extremely low mobility at 300 and 14 cm^2/V-s [12]. As the Al mole-fraction increases in the AlGaN layer, its mobility rapidly drops. Low mobility results in higher parasitic resistances and losses, and lower gain. As temperature and/or doping level rises the mobility decreases even more. Degradation due to doping is overcome by the nature of the 2DEG formed by the AlGaN/GaN heterojunction. Since all of the free carriers are in the undoped GaN channel layer, they are not influenced by ionized impurity scattering, which keeps the mobility very close to 1000 cm^2/V-s at 300 K.

2.6.5 Thermal Conductivity

Thermal conductivity describes how well heat that is generated from device operation is removed from the material. Higher temperatures degrade device performance by lowering mobility and saturation velocity which causes efficiency to drop. GaN has a thermal conductivity comparable to Si at 1.7 W/cm-K but GaN is typically grown on sapphire substrates which have poor thermal conductivity (0.46 W/cm-K) which is a major limitation for GaN devices leading to intense research to find a bulk substrate with suitable thermal properties [2]. SiC has exceptional thermal conductivity (4.9 W/cm-K) and is commonly used as a substrate for GaN but it extremely expensive. This topic is covered more extensively in a later section.

2.7 Polarization Induced Sheet Charge in AlGaN/GaN 2DEG

Polarization induced charges are the major contributor to the carrier concentration in the 2DEG in GaN. The contribution is so strong in fact that it is common to find HEMTs using the AlGaN/GaN system without any barrier layer doping at all. The 2DEG of an undoped AlGaN/GaN HEMT typically has sheet carrier concentrations from 10^{12} to 3×10^{13} cm^{-2}. The derivations and equations in this section are from Ambacher *et al*'s 1999 and 2000 publications regarding 2DEG formation resulting at undoped AlGaN/GaN heterointerfaces [11, 13] unless otherwise noted. The reader is encouraged to review those papers for a more detailed explanation of this complex topic.

There are two types of polarization charges that contribute to the total polarization of the AlGaN/GaN system: spontaneous and piezoelectric. Spontaneous polarization

(P_{SP}) is the polarization of the material when it is at zero strain and is easily calculated using the linearly interpolated formula for $Al_xGa_{1-x}N$

$$P_{SP}(x) = (-0.052x - 0.029) \ \frac{\mathrm{C}}{\mathrm{m}^2}. \tag{9}$$

Piezoelectric polarization is caused by the tensile strain in the pseudomorphic $Al_xGa_{1-x}N$ layer grown on the relaxed GaN layer. When $Al_xGa_{1-x}N$ is grown on relaxed GaN there is a lattice mismatch. The degree of mismatch is determined by the mole fraction of Al found in the $Al_xGa_{1-x}N$ barrier layer using the formulas for the interpolated lattice constants of $Al_xGa_{1-x}N$ *a* and *c* given by

$$a(x) = (-0.077x + 3.189) \ \text{Å} \tag{10}$$

$$c(x) = (-0.203x + 5.189) \ \text{Å}. \tag{11}$$

To calculate the piezoelectric polarization, the interpolated formulas for the elastic and piezoelectric constants *C* and *e* are required and are given by

$$C_{13}(x) = (5x + 103) \ \text{GPa} \tag{12}$$

$$C_{33}(x) = (-32x + 405) \ \text{GPa} \tag{13}$$

$$e_{31}(x) = (-0.11x - 0.49) \ \frac{\mathrm{C}}{\mathrm{m}^2} \tag{14}$$

$$e_{33}(x) = (0.73x + 0.73) \ \frac{\mathrm{C}}{\mathrm{m}^2}. \tag{15}$$

The polarization due only to piezoelectric strain P_{PE} is then given by

$$P_{PE}(x) = 2\frac{a(x) + a(0)}{a(0)}\left(e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)} \right). \tag{16}$$

The total polarization induced sheet charge, shown in Figure 10, is simply the sum of the spontaneous and piezoelectric polarizations of the AlGaN layer minus the spontaneous polarization of the GaN layer

$$\sigma(x) = P_{SP}(x) + P_{PE}(x) - P_{SP}(0)\,. \tag{17}$$

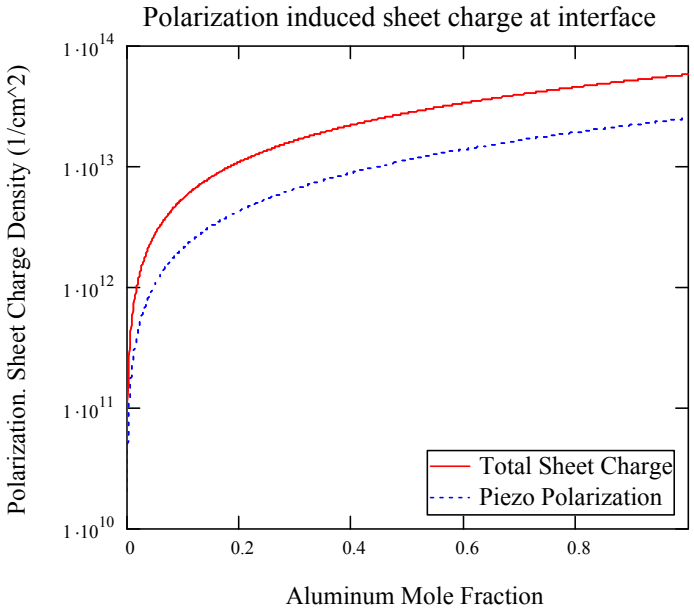

Figure 10: Piezoelectric and total polarization induced sheet charge of pseudomorphic AlGaN/GaN heterostructure vs. alloy composition

To find the polarization induced sheet carrier concentration, which is what we really care about, we need to calculate the bandgap (using equation (8)), dielectric constant (ε), the conduction band offset (ΔE_C) and the Fermi energy (E_F) with respect to the conduction band edge (E_C) of the $Al_xGa_{1-x}N$

$$\varepsilon(x) = -0.5x + 9.5 \tag{18}$$

$$\Delta E_C = 0.7\left(E_g(x) - E_g(0)\right)\ \text{eV} \tag{19}$$

$$E_F(x) = \left(\frac{9\pi\hbar q^2}{8\varepsilon_o\sqrt{8m_{eff}}} \right)^{2/3} + \frac{\pi\hbar^2}{m_{eff}} n_s(x) \text{ eV} \tag{20}$$

Where $m_{eff} \approx 0.22\ m_o$, $\hbar$ is a modified Planck's constant ($h/2\pi$), ε_o is the permittivity of free space and $n_s(x)$ is

$$n_s(x) = \frac{\sigma(x)}{q} - \left(\frac{\varepsilon_o \varepsilon(x)}{d_{AlGaN} q^2} \right) \left[q\phi_b(x) + E_F(x) - \Delta E_C(x) \right] \tag{21}$$

where $q\phi_b(x)$ is the Schottky barrier height for nickel given by

$$q\phi_b(x) = (1.3x + 0.84)\ eV\ . \tag{22}$$

The equations for $n_s(x)$ and $E_F(x)$ must be solved simultaneously to reach a solution as they are dependent on each other. Figure 11 shows the maximum n_s of the 2DEG located at the AlGaN/GaN interface. For a d_{AlGaN} of 30 nm, n_s is 0.92, 1.51, and 2.13×10^{13} cm^{-2} for mole fractions of 0.2, 0.3, and 0.4, respectively. If d_{AlGaN} is decreased from 30 to 10 nm at Al% 0.25, n_s is lowered from 1.21 to 0.86×10^{13} cm^{-2}.

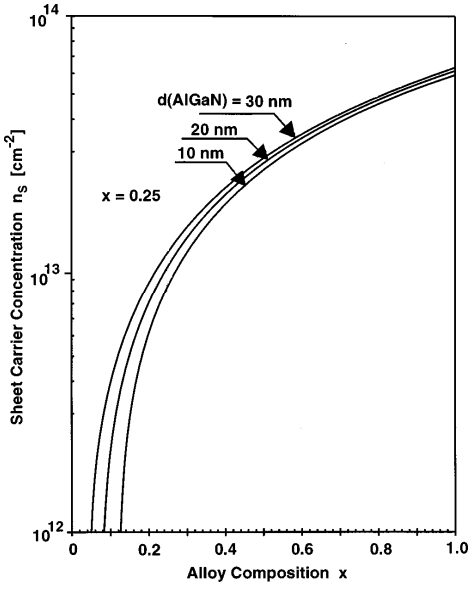

Figure 11: Sheet carrier concentration at the AlGaN/GaN interface for different barrier layer thicknesses along with varying Al% [11]

2.8 Metal Organic Chemical Vapor Deposition (MOCVD)

The two prevalent techniques for growing GaN epiwafers are molecular beam epitaxy (MBE) and MOCVD. Commercially, MOCVD has become the method of choice for large scale manufacturing of III-N wafers as it is much more suited to the task of large scale manufacturing than MBE [10]. The devices modeled and tested for this thesis were all grown using MOCVD. MOCVD reactors consist of three major components: the gas delivery system, reaction chamber, and reactor safety infrastructure (not covered in this paper). A GaN MOCVD reactor system is shown in Figure 12.

MOCVD is also known by several other names such as organometallic chemical vapor deposition (OMCVD), metalorganic vapor phase epitaxy (MOVPE) and organometallic vapor phase epitaxy. The technique originated in 1968 at North

American Rockwell and since then has dominated (along with MBE) the research, development, and manufacture of compound semiconductor devices. MOCVD is the crystal growth method of choice for a wide array of devices including light emitting diodes (LEDs), lasers, heterostructure bipolar transistors (HBTs), photodetectors and solar cells along with many other devices [14]. Most MOCVD growth of III-N semiconductors involves the use of hydride and alkyl sources.

Figure 12: GaN MOCVD Reactor System [15]

2.8.1 Reaction Equations

The growth of AlGaN and GaN is accomplished by mixing the vapors of the different constituents in the appropriate ratio to form the desired material composition. The basic reaction that results in the growth of GaN during the MOCVD process is

$$(CH_3)_3Ga + (NH_3) \rightarrow GaN + 3CH_4 \tag{23}$$

where $(CH_3)_3Ga$ is trimethylgallium (TMG), (NH_3) is ammonia and (CH_4) is methane [14]. Similarly the basic reaction that results in the creation of AlGaN during the MOCVD process is

$$x(CH_3)_3Al + (1-x)(CH_3)_3Ga + NH_3 \rightarrow AlGaN + 3CH_4 \quad (24)$$

where x is the mole fraction of aluminum and $(CH_3)_3Al$ is trimethylaluminum (TMA). Typically the organometallic constituents (TMG and TMA) are sent to the heated substrate in the reaction chamber by passing a carrier gas (usually H_2) over or through the constituents contained in a constant temperature bubbler [14].

2.8.2 Reactor Gas Delivery Systems

A basic schematic diagram of an MOCVD reactor delivery gas panel is shown in Figure 13. The reactor gas delivery system, or gas panel, consists of a network of stainless steel tubing, automatic valves and electronic mass flow controllers (MFC). There are separate control systems for each constituent source. The ammonia delivery system simply consists of a few valves and a MFC due to the fact that it is normally provided as dilute high-pressure gas in portable gas cylinders [14].

The Al and Ga delivery modules are more complicated and they consist of high vapor-pressure source materials contained in stainless steel bubblers which are held in a refrigerated bath that maintains a stable vapor pressure over the liquid or solid source. The carrier gas is pushed through the bubbler where it picks up the TMG/TMA and delivers the material to the reaction chamber for deposition. Small variations in the carrier gas flow can significantly change the source delivery rate (typically on the order of tens or hundreds of cm^3/min. Therefore the gas delivery systems must not succumb to transients that can arise from switching or dead space. As long as a fixed relationship is maintained between overall pressures throughout the system, transients will be minimized, allowing the source flow to be properly controlled [14].

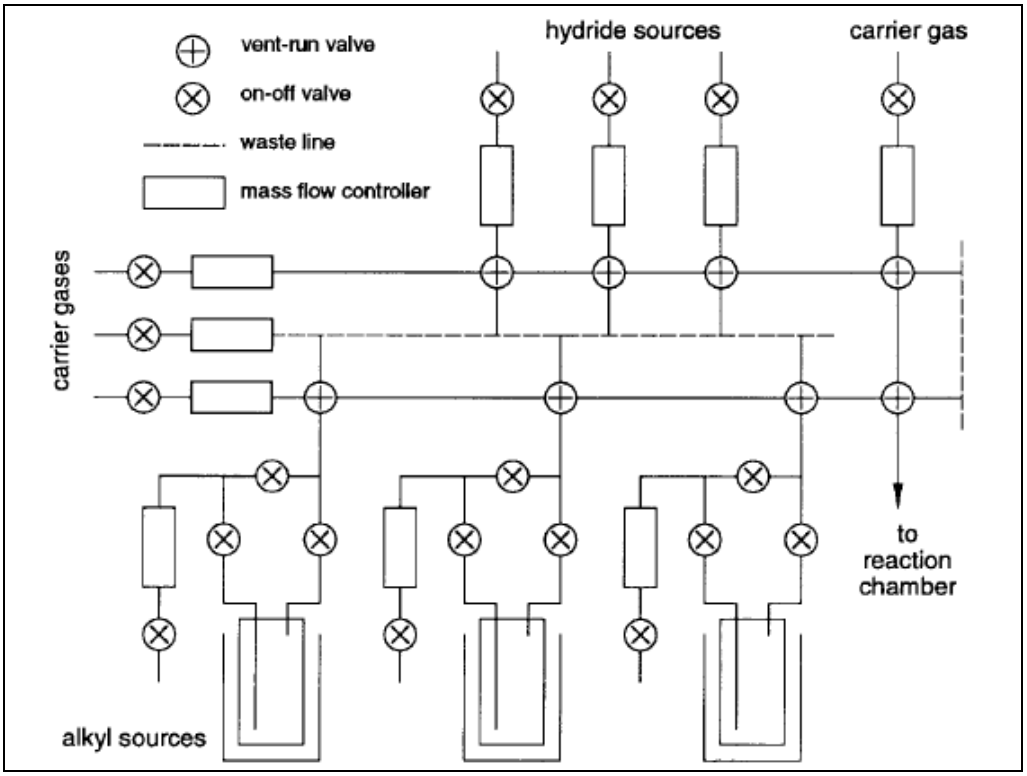

Figure 13: Schematic diagram of a typical MOCVD reactor delivery system gas panel including both hydride and alkyl delivery modules and the vent/valve configurations [14]

2.8.3 Reaction Chamber

The reaction chamber is where the source gases are combined as well as where the substrate wafers are found. The wafers are arranged on a showerhead susceptor, an example of which is shown in Figure 14. The susceptor heats the substrate to between 1000 – 1100 °C [16] which causes the constituents to undergo pyrolysis. Temperatures in excess of 800 °C are required in order to obtain single crystalline high-quality GaN films. GaN films with the best electrical and optical properties are grown at 1050 °C.

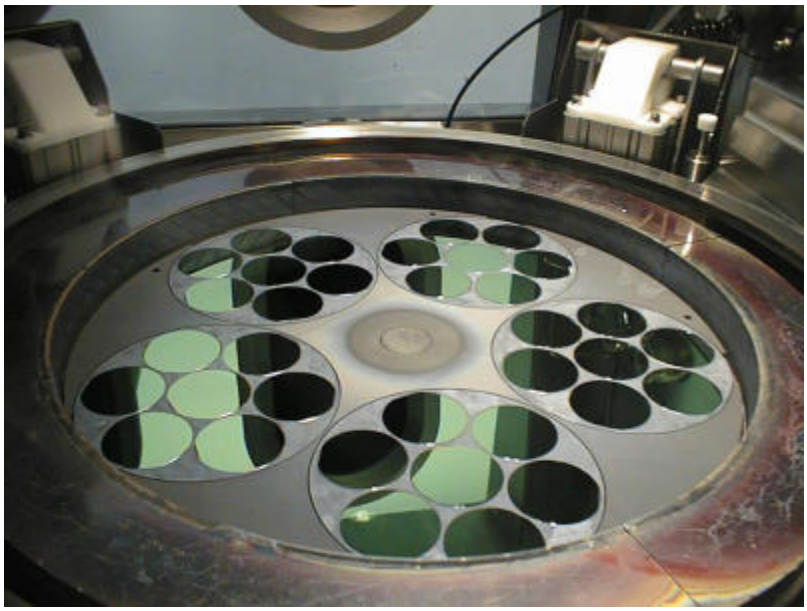

Figure 14: Planetary showerhead susceptor in an industrial reaction chamber [17]

Substrate temperatures over 1100 °C will begin to cause voids in the GaN layer so it is very important to perfectly control the temperature within this fairly tight range [18]. The high growth temperatures are one of the restricting factors when choosing a substrate. The high temperatures have both positive and negative effects on the resulting crystal quality. High temperatures result in higher surface mobility of atoms and higher quality film growth as well. Unfortunately, post growth cooling introduces more strain resulting in more structural defects [18].

A simplified schematic of a commercial vertical reaction chamber is shown in Figure 15. The constituents are brought into the reactor and combined in the mixing chamber. The gas is then sent through a diffuser to force a uniform gas flow against the susceptor. The susceptor's rotation (and in the case of the planetary susceptor each wafer rotates within the susceptor which is also rotating) together with the multi-stage heater

block allows the system to control the temperature gradient across the susceptor for improved uniformity.

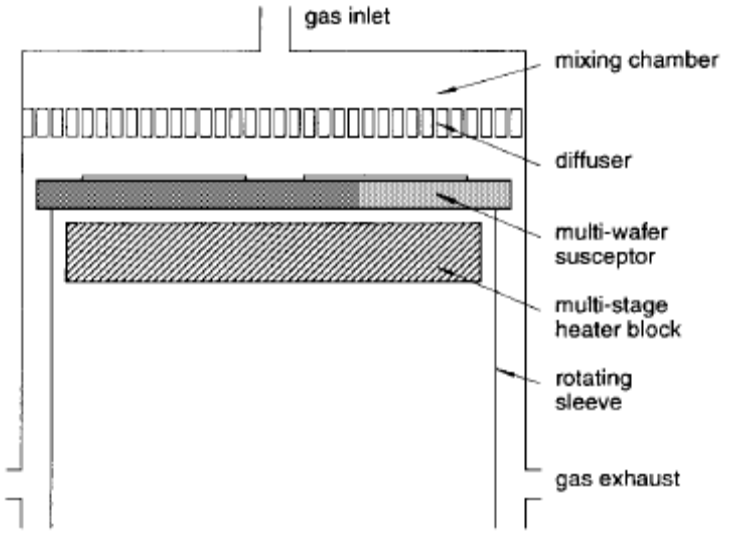

Figure 15: Simple schematic diagram of a commercial vertical reaction chamber [14]

2.9 GaN Growth Rate

The growth rate of III-N materials has 3 distinct temperature regimes as shown in Figure 16. The absolute growth rate depends on too many process specific variables and parameters to quantify so the scale used in Figure 16 is arbitrary and shows the three regimes relative to each other [14]. The reaction rate limited regime, found at the lower end of the temperature scale, is limited by the reaction rate of the constituents. Alkyl pyrolysis efficiency is fairly steep so the reaction rate limited regime should only cover a small temperature range [14].

Once the temperature reaches the third regime there are parasitic effects occurring in the reactor. Specifically the temperature of the gas above the substrate gets high

enough to cause gas pyrolysis of the constituents to occur [14]. This will result in undesired solid particulate "snowing" onto the substrate.

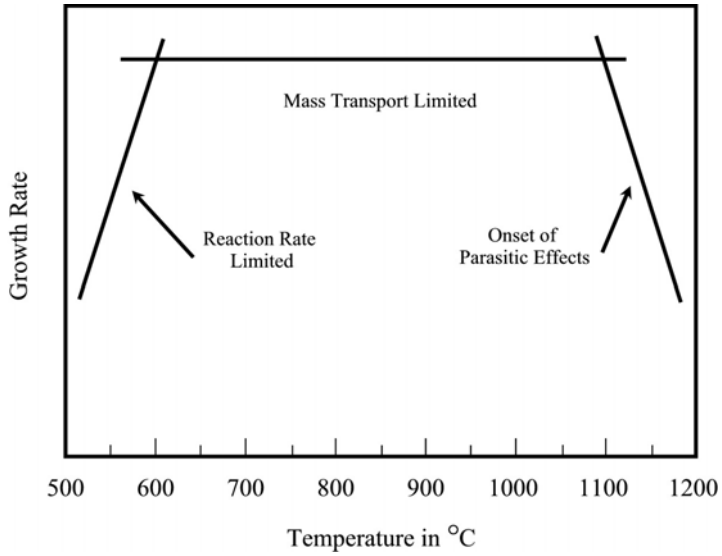

Figure 16: Growth rate as a function of temperature showing the three distinct regimes for GaN MOCVD growth [19]

The regime of primary interest though is the mass transport limited regime. This is the temperature range at which most MOCVD processes occur because the rate of growth is controlled by the input rate of the source gases, which can be controlled by the operating technician, rather than the substrate temperature.

Under mass transport limited conditions the following assumptions are made: Ga/Al incorporation is solely dependent on the amount of constituent fed into the reactor cell; Ga/Al precursor molecules are completely decomposed; and ammonia vapor is supplied in excess (ranging from 1300 to 6000 times the amount of Ga/Al constituent [19]) and does not impact the overall growth rate of the alloy. Ultimately, under these assumptions, AlGaN/GaN composition and growth rate depends, to a good first

approximation, on the amount of $(CH_3)_3Ga$ and $(CH_3)_3Al$ source vapor fed into the reactor [20].

2.10 Difficulties Working with GaN

When AlGaN/GaN HEMTs were introduced they attracted much attention because of the high performance possibilities of GaN such as high-bandgap, fairly high electron mobility and high saturation velocity. These properties fueled a research frenzy trying to exploit GaN to its fullest, specifically its use in high power amplifiers operating at GHz or higher frequencies. Unfortunately, there were, and still are, fabrication difficulties that need to be overcome to exploit this technology to its fullest on a mass-market scale.

2.10.1 Lack of Bulk Substrates

One of the primary shortcomings of GaN is its lack of a readily available, lattice matched, substrate [2]. When AlGaN/GaN HEMTs were first introduced, they were grown on sapphire substrates. The downsides to using sapphire are its very low thermal conductivity compared to GaN (0.46 W/K-cm to 1.7 W/K-cm respectively [2]) and its very large lattice mismatch (13 - 16%) to GaN [2, 21]. The poor thermal conductivity of sapphire makes it more difficult to take advantage of the high temperature operation under which GaN should excel. The large lattice mismatch results in a large number of dislocations in the bulk which limits the performance of the device. To overcome this large mismatch a nucleation layer (typically AlN or AlGaN) is grown first on the substrate. This controls the polarity of the GaN and AlGaN layers and allows a monocrystalline growth of the AlGaN/GaN layers in spite of the significant lattice

mismatch [7]. Ga-face polarity ensure that a 2DEG is formed at the AlGaN/GaN interface where as N-face polarity will result in a 2DHG in this configuration [11].

The substrate of choice today is SiC, but its disadvantages are that it's not readily available in mass quantities and is extremely expensive - up to $5K for a single 3" wafer according to one manufacturer. It is not lattice matched to GaN (3% mismatch [8]) so a nucleation layer is still required for the same reasons as for sapphire. In addition to SiC's better lattice match to GaN it also has a thermal conductivity over 10 times higher than sapphire [2]. As shown in Figure 17, SiC wafer diameters are increasing at a very fast rate which raises hopes that per device cost will be reduced as wafer sizes increase. Some believe that SiC wafer manufacturers are waiting for the market to develop before they push larger SiC wafers on to the industry due to the large amount of existing fabrication equipment that would need to be redeveloped to accommodate the larger sized wafers [22].

Figure 17: The increase in wafer diameter as a function of time, demonstrated for R&D GaAs, Si and SiC wafers. SiC wafers have gone from 25 to 100 mm in about half the time it took GaAs or Si to make the same increase [22]

Other technologies are being developed by researchers looking for affordable but effective substrate alternatives for GaN. Zinc oxide (ZnO) (Figure 18) is interesting for its low lattice mismatch to GaN of 2%. The downside is that current literature suggests that it is difficult or even impossible to grow high-quality GaN on ZnO [22].

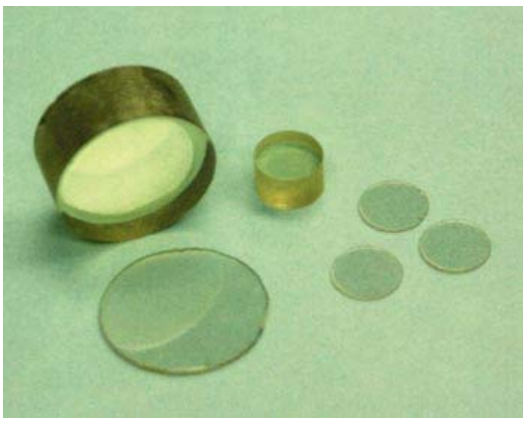

Figure 18: ZnO boules and wafers. ZnO is being developed as a material suitable for GaN epitaxy [22].

Silicon is also being investigated as a possible substrate material due to its low cost (10% the cost of sapphire), compatibility with current silicon processing tools and using silicon allows the possibility of monolithic integration with silicon electronics [23]. Silicon's properties make it much harder on which to grow GaN than on sapphire or SiC though. The lattice mismatch to GaN is 17% and thermal expansion coefficients are much different (100% difference [22]). These characteristics cause the GaN layers to crack when they are grown over 1μm in thickness.

2.10.2 Other GaN Growth Challenges

There are other challenges growing GaN besides the lack of a lattice-matched substrate to contend with. One of the main challenges is overcoming the high nitrogen

(N_2) vapor pressures required during growth. A certain minimum N_2 pressure must be maintained in the vapor in order to produce a GaN solid with no other condensed phases [16]. If the pressure is too low, a Ga-rich liquid is created along with the GaN solid.

Also, because of the high Ga-N bond strength very high temperatures are required to grow high-quality material. The need for the high growth temperatures required for quality crystal growth and the low growth temperatures needed to keep the N from leaving the solid is perhaps the top obstacle overcome in growing bulk GaN material [16]. The combination of high growth temperatures and high nitrogen volatility results in high concentrations of N vacancies in the GaN (as high as 10^{19} cm^{-3} [16]). These vacancies act as unwanted electron donor centers in the intrinsic GaN which must be considered when designing any device from that material.

2.11 Current Research

Sood *et al.* [24] understood the characterization of undoped AlGaN/GaN epitaxial layers grown by MOCVD on SiC substrates for RF applications. This paper is valuable because the majority of the research currently done on GaN devices is regarding electro-optical performance. In this paper they demonstrate that the key to high quality HEMT structures is the ability to grow uniform AlGaN layers. Two sets of samples were grown: one using standard MOCVD processing and one using optimized MOCVD processing techniques. The sheet resistance was mapped on representative wafers from each reactor run as shown in Figure 19.

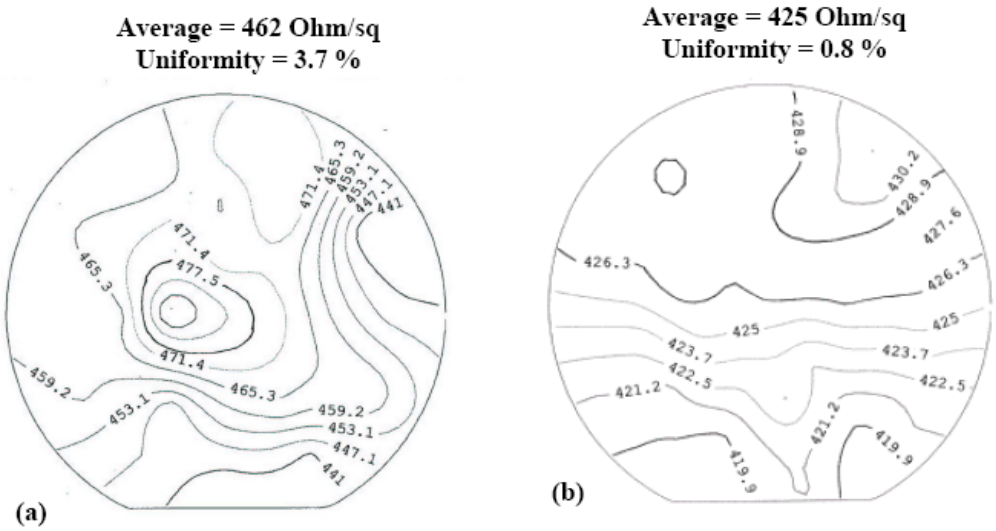

Figure 19: Sheet resistance maps of (a) the initial HEMT wafer and (b) optimized HEMT wafer. Both wafers have identical structures with 27% Al% [24]

The variation of Al% in the first wafer was over 2% and followed the variation of in sheet resistance. Sood found that the variation in Al% decreased by a large margin with increasing ammonia flow, from 2.3% at a flow rate of 2 slm to 0.9% at a flow rate of 10.5 slm as shown in Figure 20.

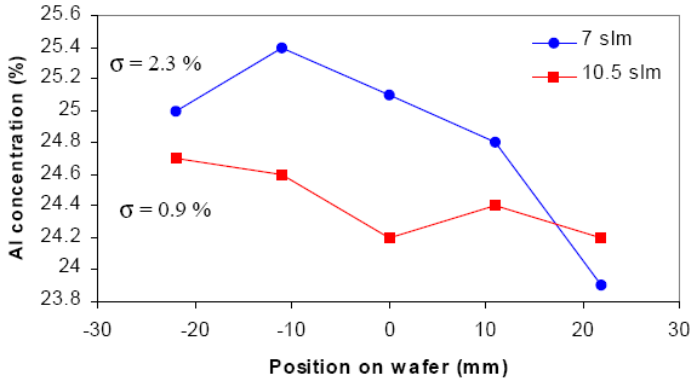

Figure 20: Al% at five points across a 2" wafer from two AlGaN samples grown with different ammonia flow rates [24]

Decreasing the growth temperature and increasing the AlGaN growth rate were found to improve compositional uniformity as well as shown in Figure 21 [24]. Increasing the growth rate is as simple as increasing the ammonia flow rate.

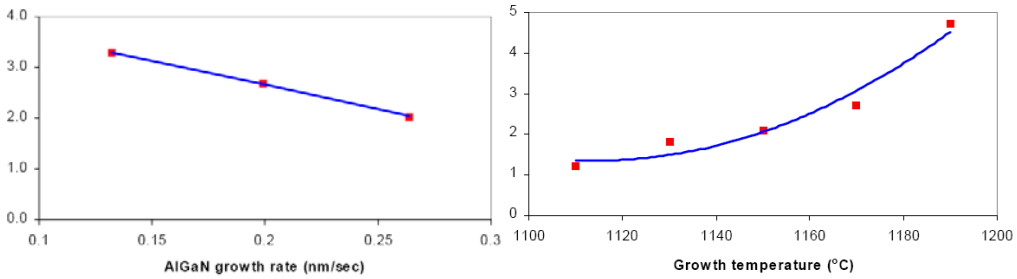

Figure 21: Standard deviation in AlGaN composition across a 2" wafer as a function of growth rate (left) and as a function of growth temperature (right) [24]

There is an engineering tradeoff to be made in deciding the growth temperature. Because the HEMT structures are undoped, the relationship between sheet resistance (R_s) and n_s is given by [24]

$$R_s = \frac{1}{q\mu n_s}. \tag{25}$$

For a fixed device structure Sood found that using higher growth temperatures resulted in lower sheet resistance, which is caused by higher n_s, but increasing growth temperatures also caused decreased wafer uniformity which results in devices with a wider variety of performance across a single wafer. The solution to this issue was to increase the ammonia flow rate. Figure 22 shows the effect increasing the ammonia flow rate has on the overall sheet resistance of the wafer.

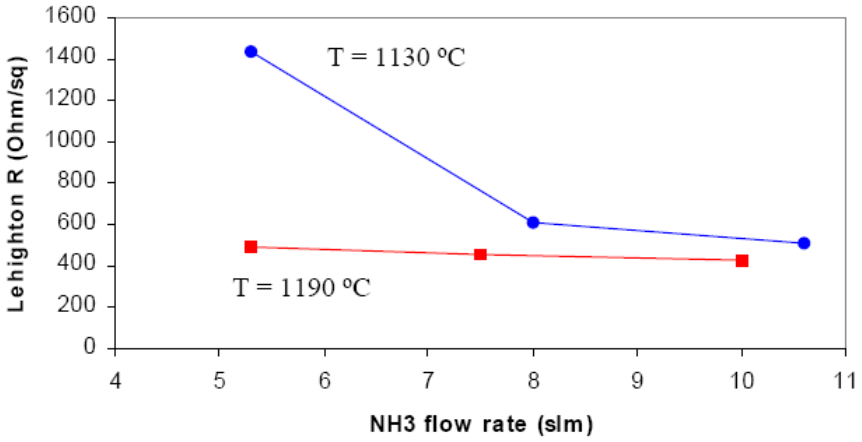

Figure 22: Overall sheet resistance of two sets of HEMT wafers as a function of NH3 flow. One set uses an AlGaN growth temperature of 1130° C, the other 1190° C [24].

Miyoshi *et al* [25] demonstrated that even though higher Al% can provide higher n_s values there is a tradeoff of decreased 2DEG mobility (Figure 23) due to degraded barrier/channel interface quality caused by dislocations from the increasing strain in the AlGaN.

Faraclas *et al* [26] completed a study in 2004 on the dependence of RF performance of AlGaN/GaN HEMTs on barrier layer thickness variation. Specifically he tracked the dependence of f_T and f_{max} on Al% and barrier thickness. The determination of the microwave parameters was accomplished by self-consistently solving Schrodinger's and Poisson's equations to calculate the dependence of the 2DEG on changes in the AlGaN barrier composition and thickness.

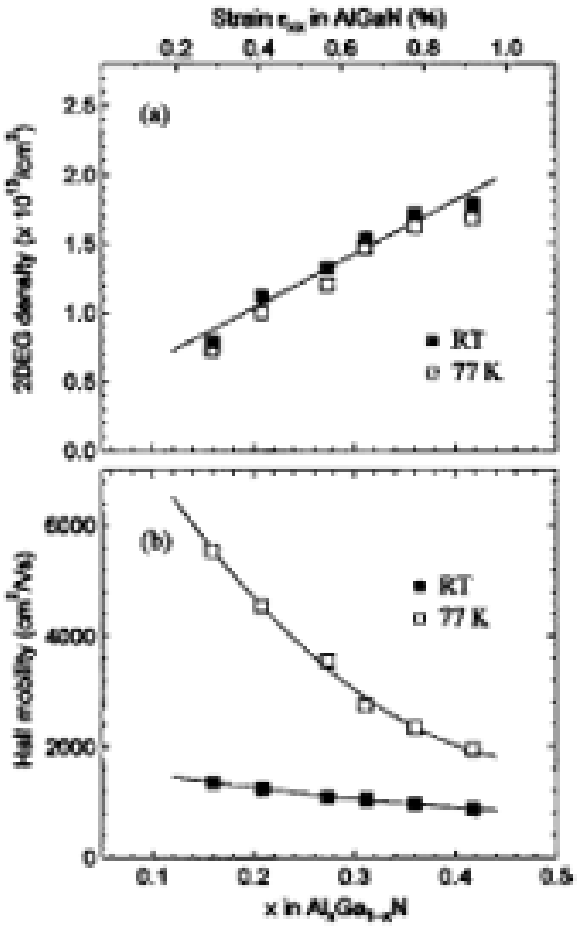

Figure 23: (a) 2DEG density and (b) mobility of different Al% AlGaN/GaN structures measured at room temperature and 77 K [25].

In Figure 24 Faraclas shows the effect that changing the barrier layer thickness has on the 2DEG concentration. It is shown that with increasing barrier thickness the slope of n_s as a function of the gate bias decreases. That slope is proportional to the device transconductance which decreases as barrier thickness increases[26].

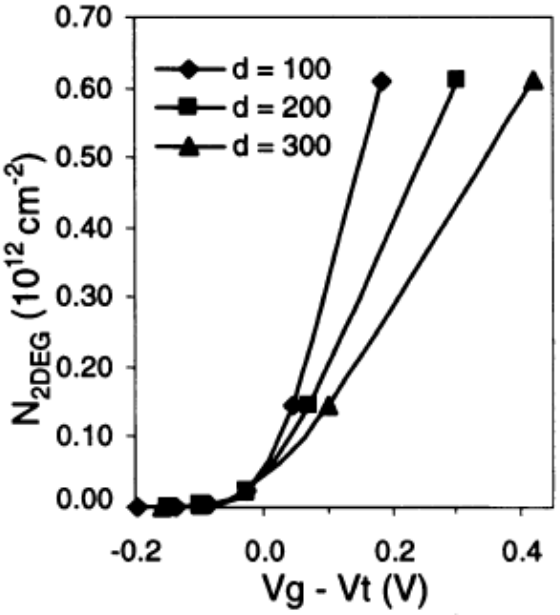

Figure 24: Variation of the 2DEG concentration as a function of normalized gate bias with barrier layer thickness (d) as a parameter and the Al% is 0.3 [26]

He shows the variation of f_T as a function of the thickness of the barrier layer in Figure 25 by implementing a physics-based model that uses both operating temperature and mole fraction as parameters. f_T is calculated using equation (2) . It is seen that for Al% of 0.2, f_T increases with barrier thickness and saturates around 250 Å. Al% of 0.3 causes f_T to reach a maximum around 200 Å. As mentioned earlier, for a given gate and drain bias, g_m decreases with increasing barrier thickness but at the same time the higher thickness creates a larger separation between the gate and the channel which decreases that gate to source capacitance (C_{gs}) resulting in an initially increasing f_T. This leaves the engineer the decision of which tradeoffs are acceptable since the barrier layer can't be thicker than the critical thickness for a given Al% without relaxing the AlGaN and destroying device performance. However, C_{gs} is also dependent on the average distance

to the 2DEG peak from the metallurgical junction which increases as n_s decreases as shown in Figure 26 [26]. As the peak moves closer to the gate, C_{gs} increases which increases the total gate capacitance causing f_T to decrease as per equation (2).

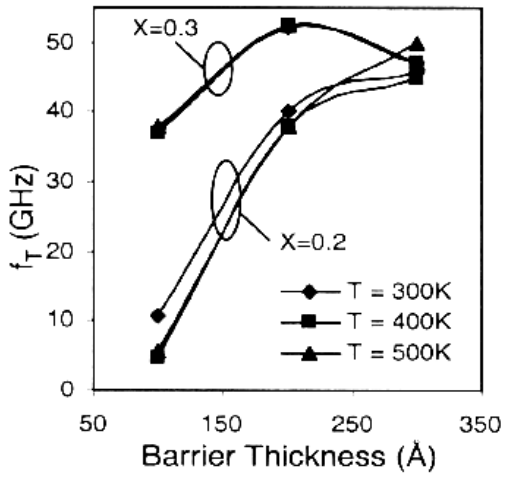

Figure 25: Cutoff frequency as a function of barrier thickness and temperature [26]

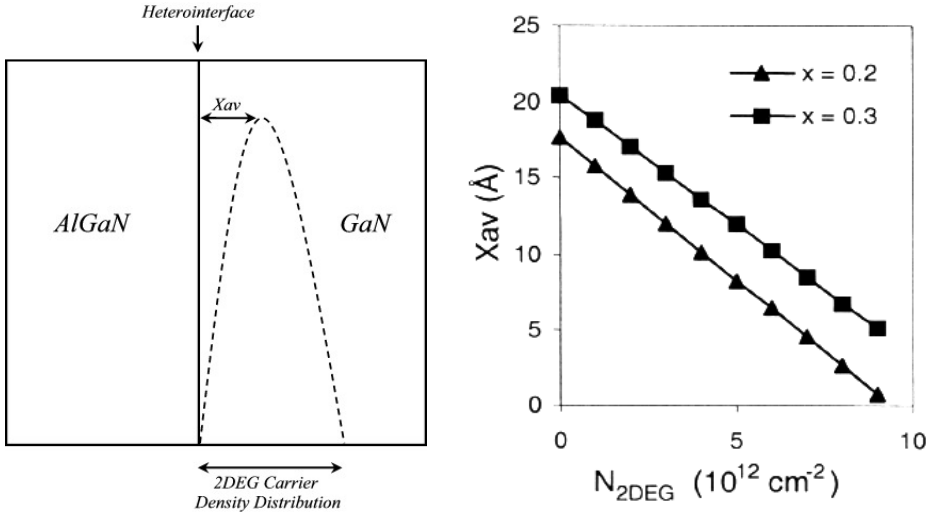

Figure 26: Average distance of the 2DEG peak from the heterointerface, Xav, as a function of n_s for Al mole fractions of 0.2 and 0.3 [26]

Faraclas' research demonstrated that there is a strong connection between AlGaN/GaN HEMT performance and the barrier thickness and Al% parameters. He showed that g_m decreases more rapidly for higher Al% while C_{gs} decreases more slowly resulting in a reduced f_T. Finally, he determined that f_T and, in turn, $f_{max,}$ are both weakly temperature dependent for this material system which is one reason that GaN is so useful for high temperature applications [26].

2.12 Chapter Summary

This chapter provided background information on the basics of heterostructures and, HEMT device operation. It also covered a basic AlGaN/GaN HEMT structure similar to the ones that were used as the basis for this thesis. Next, the basic properties of GaN, as well as what makes it a desirable material to work with were covered. The effects of both piezo and spontaneous polarizations were thoroughly covered because polarization provides the carriers in an undoped HEMT and the density of carriers is dependent on both Al% and barrier thickness. The MOCVD process was also explained due to the fact that that is where much of the process variation will occur when fabricating GaN devices. Finally some current, applicable research was discussed including the impact of mole fraction and barrier thickness variation on the values of f_T as well as f_{max} through its dependence on f_T.

Chapter 3. Methodology

3.1 Chapter Overview

This chapter discusses the methodology used for completion of this thesis. The different types of data used for the analysis as well as where it is acquired from and how it was obtained will be covered. Three sources of data were used in this research: 1) epilayer characterization data provided by AFRL, 2) DC and RF characterization data collected in the AFRL sensors clean room, and 3) TCAD simulation data generated at AFIT.

3.2 Nominal Wafer Description

Three 3" wafers were provided by AFRL for this research project. Each wafer was processed using the same growth and device fabrication techniques for the reasons explained in chapter 2. SiC was used as the substrate on which an AlN interfacial layer was grown in order to overcome the 3% lattice mismatch between the SiC and GaN layers. An undoped GaN buffer layer followed by a AlGaN barrier layer with 25% concentration of Al were grown on the Al nucleation layer with a GaN cap layer on top of the AlGaN barrier layer. There are several different options available when deciding on a cap layer. It is common to see doped or undoped AlGaN and doped or undoped GaN caps for various reasons. The manufacturer of these devices chose to use an undoped GaN cap layer for reasons that are proprietary. Finally, the nominal device has a 0.5μm L_g.

3.2.1 Epilayer Characterization Data

Information on the fabrication process and the characteristics of the epilayer structure of the HEMTs is essential in order to assess the sensitivity of device performance due to variation of material parameters. AFRL provided complete epilayer characteristics for each of the three wafers. Figures 28-30 show the device layout for each wafer. Empty sites do not have viable devices in them. The horizontal and vertical numbering on both sides of the wafer correspond to the coordinate system used to specify individual cells, with (0,0) being the cell at the center of the wafer, (-3,-3) being the lower left cell and (3,3) being the upper right cell. Each cell contains a large number of different experimental device layouts with only a single HEMT structure per cell considered in this thesis (shown in Figure 27).

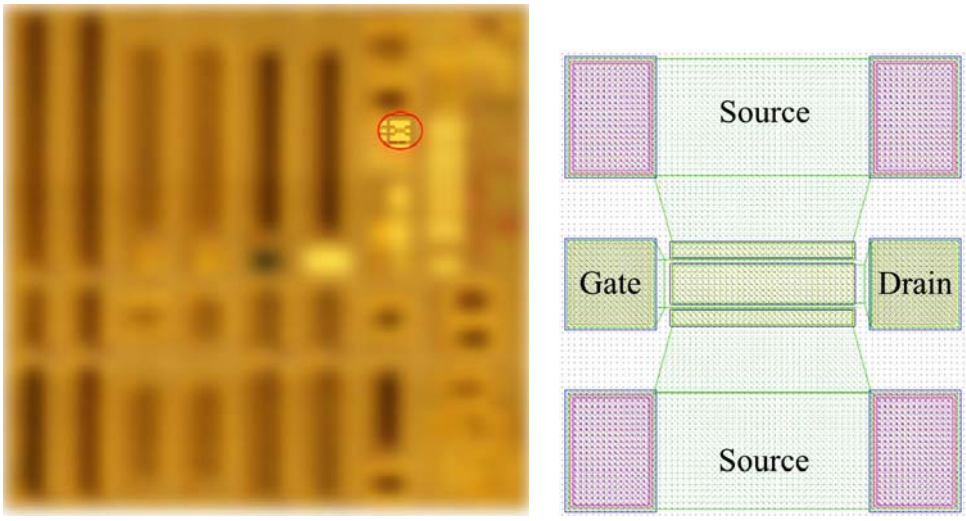

Figure 27: An image of a single cell with extraneous devices blurred out. The device of interest is circled in red with the co-planar pad layout shown on the right.

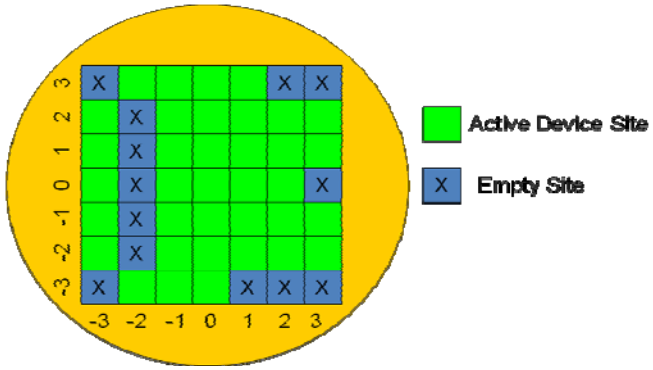

Figure 28: Wafer #1

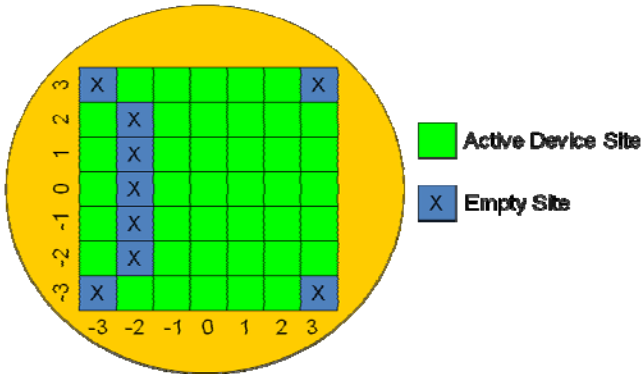

Figure 29: Wafer #2

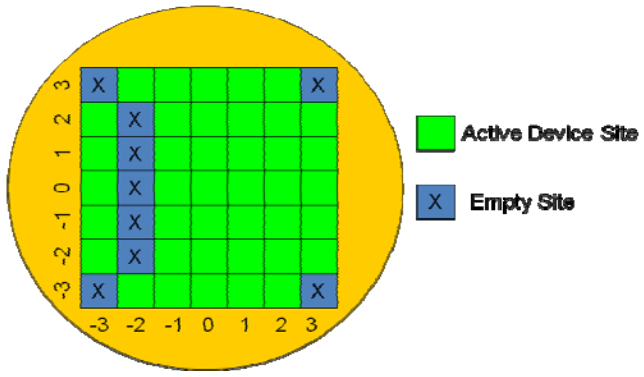

Figure 30: Wafer #3

The material and layer characteristics provided for each wafer were collected at AFRL. The details of the measurement and data collection processes were not available at the time of this writing but the key parameters pertaining to this research were provided for 3 device locations on each wafer. Specifically the Al% and the AlGaN barrier thickness were provided for devices at locations (0,-3), (0,0) and (0,3) on all three wafers. These values are summarized in Table 1.

Table 1: AFRL provided epilayer data

Wafer Number	Aluminum Mole Fraction (%)	AlGaN Barrier Thickness (Å)
Wafer 1		
Site: (0 , 3)	25.82	241.48
(0 , 0)	25.53	240.97
(0 ,-3)	25.99	236.11
Wafer 2		
Site: (0 , 3)	25.44	247.43
(0 , 0)	25.60	248.35
(0 ,-3)	26.54	240.70
Wafer 3		
Site: (0 , 3)	24.75	245.14
(0 , 0)	25.32	243.83
(0 ,-3)	25.32	239.23

3.2.2 DC and RF Characterization

DC and RF characterization was conducted in the AFRL sensors directorate (AFRL/RYDD) clean room. The cadre of experienced technicians and engineers who operate the characterization equipment handled the setup and execution of the characterization process with my limited involvement. The lead engineer during characterization was 1Lt Derrick Langley and the procedures detailed in chapter 4 of his thesis, titled "*AlGaN/GaN HEMT Topology Investigation Using Measured Data and*

Device Modeling" [27], were followed and this section draws heavily from that document.

The 3 wafers used for this research were tested at DC to collect families of I-V curves and g_m curves. They were also tested at RF to collect S-parameters S_{11}, S_{22}, S_{12} and S_{21}. Both the DC and RF testing were completed on a Cascade Microtech 12000 Characterization Probing system very similar to the one shown in Figure 31 along with an HP 8510C network analyzer and an HP 4142 DC parameter extraction system. The process of collecting data is entirely automated including reticle alignment and probe manipulation. Normal, AFRL developed, start-up and calibration procedures were followed for all tests.

DC and RF data was collected at each of the active device sites shown in Figures 23-25. I-V curves were collected from V_g = 1V to V_g = -5V in 1V intervals while sweeping V_{ds} between 0V and 28V, which are the designed operating range of these devices. g_m testing was accomplished by keeping V_{ds} at 28V and ramping V_g from -5V to 1V and back down to -5V. This generated I-V curves that were differentiated within the HP 4142 to create the g_m curve for each device. Finally, S-parameters were collected by first determining the V_g that produced the maximum transconductance for each device and then conducting small signal analysis using the HP 8510C over the frequency range of 1 to 26 GHz with V_{ds} at 10V. Data is output from the Cascade system in standard spreadsheet format for manipulation in any data analysis package.

Figure 31: Cascade Microtech characterization probe station.[28]

3.3 TCAD Simulations

3.3.1 TCAD Operation Overview

This section borrows liberally from the Synopsys TCAD user's guides. The reader can refer to the user's guides for more detailed explanations of the code contained herein.

TCAD uses computers for simulating semiconductor processing and device operation to solve fundamental, physical partial differential equations, such as diffusion and transport equations that model the charge carrier physics in the HEMT. This physics-based approach is what gives TCAD simulations their predictive accuracy. This accuracy allows us to substitute TCAD computer simulations for costly and time-

consuming test wafer runs when developing and characterizing novel devices or structures [29].

TCAD simulations can be thought of as virtual measurements of the electrical behavior of a semiconductor device, such as a transistor or diode. The device is represented as a meshed finite-element structure. Each node of the device has properties associated with it, such as material type and doping concentration. For each node, the carrier concentration, current densities, electric field, generation and recombination rates, and so on are computed [29].

Electrodes are represented as areas on which boundary conditions, such as applied voltages, are imposed. The device simulator solves the Poisson equation

$$\nabla \cdot \varepsilon \nabla \phi = -q(p - n + N_D - N_A) - \rho_{trap} \tag{26}$$

where p and n are the hole and electron densities respectively, N_D and N_A are the concentrations of ionized donors and acceptors respectively and ρ_{trap} is the charge density contributed by traps and fixed charges. TCAD also solves the electron and hole continuity equations

$$\nabla \cdot J_n = qR_{net} + q\frac{\delta n}{\delta t} \tag{27}$$

$$-\nabla \cdot J_p = qR_{net} + q\frac{\delta p}{\delta t} \tag{28}$$

where R_{net} is the net electron/hole recombination rate and J_n and J_p are the electron and hole current densities, respectively. All of the simulations for this research used the drift-diffusion model where the current densities are given by

$$J_n = -nq\mu_n \nabla \Phi_n \tag{29}$$

$$J_p = -pq\mu_p \nabla \Phi_p \tag{30}$$

where μ_n and μ_p are the electron and hole mobilities and Φ_n and Φ_p are the electron and hole quasi-Fermi levels respectively. After solving these equations, the resulting electrical currents and voltages at the contacts are extracted and used to generate the desired high frequency and DC operation data [29].

The software suite consists of many different modules that are used in different situations to simulate everything ranging from epilayer growth to radiation strikes on finished devices. For this thesis only 4 modules are used: 1) Sentaurus Workbench (SWB) 2) Sentaurus Structure Editor (SE) 3) Sentaurus Device (SDE) and 4) Inspect / Tecplot.

SWB is the primary graphical front end that integrates all TCAD tools into a single environment. The graphical user interface was used to design, organize, and run all of the simulations for this research. SWB automatically manages the information flow from one tool to another. This includes preprocessing of user input files, setting up and executing tool instances, and visualizing the results. The process flow used for the TCAD simulations in this thesis are shown in Figure 32.

Figure 32: TCAD process flow used for this thesis. SE and SDE files are compiled in SWB and the output data is extracted from Inspect and/or Tecplot.

3.3.2 HEMT Model

The device model was constructed in SE using code that was provided by AFRL [30]. The provided code was modified to allow for variation of the parameters of interest in this research: Al%, d_{AlGaN} and L_g via the SWB interface. The 2D-structural model is shown in Figure 33 The actual compiled TCAD model can't be shown here due to the structures proprietary nature.

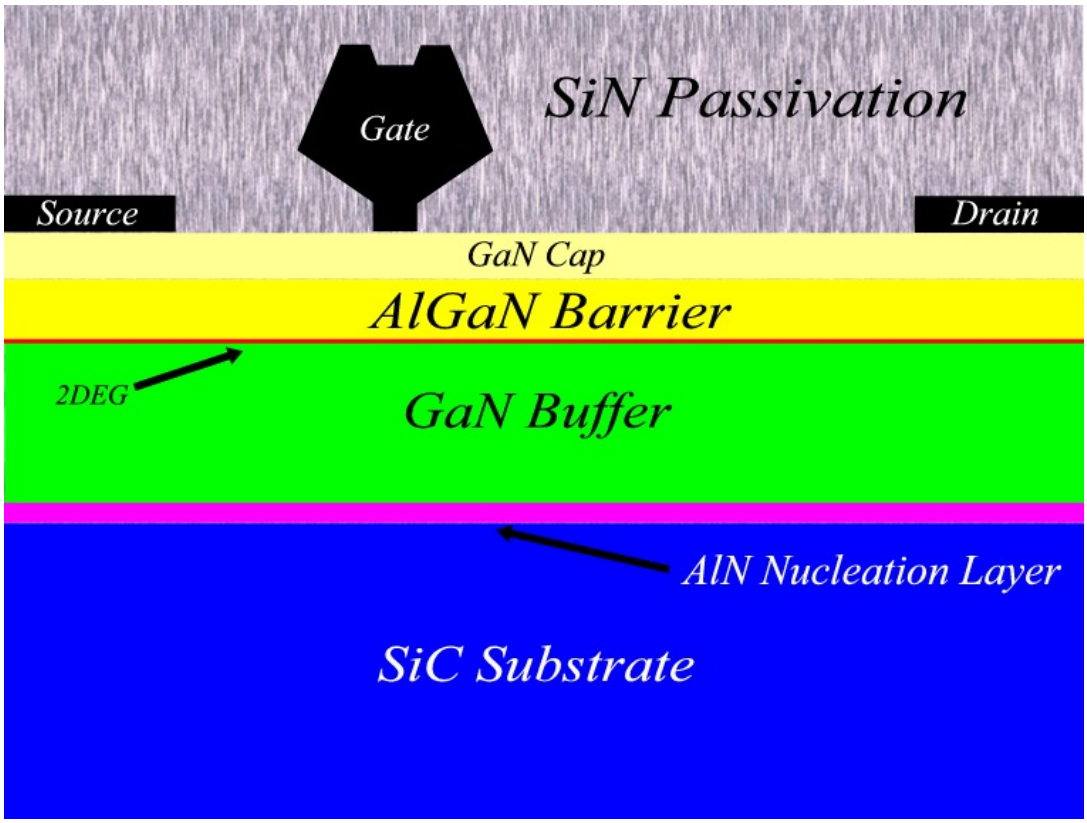

Figure 33: HEMT model used in TCAD simulations as displayed in Tecplot.

The AFRL code is proprietary and cannot be included in this paper in its entirety. The code is broken down into several smaller sections that describe the device as a whole. The SE code includes the interpolated equations for the elastic and piezo constants, equations (6) – (9). Strain is also calculated and integrated into the model here. There are small thermodes buried inside the model (not visible in Figure 33) to allow the simulation to properly implement temperature effects within the device.

TCAD functions much like any finite element analysis software in that it uses coarse meshes in the areas of least interest and fine meshes in areas of high interest within the device. For this device, the main areas of interest are in and near the channel between the source and the drain contacts; particularly beneath the gate. Figure 34 shows the meshing used for this device. The channel has a very fine refined mesh throughout because most of the device operation of interest occurs there. As you move away from the channel the mesh becomes coarse such as in the bulk GaN and in the SiN passivation layer. The targeted meshing allows the simulation to run much faster than if there were a uniform fine mesh across the entire structure. The layout of the mesh was developed by engineers within AFRL/RYDD and cannot be shown in its entirety here.

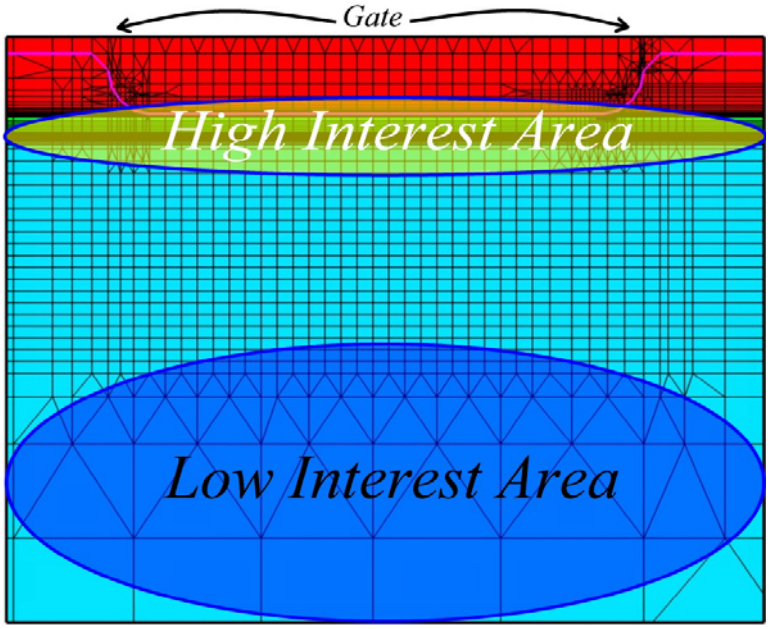

Figure 34: HEMT mesh plot as shown in Tecplot. The high interest area has a very tight mesh in the channel between the source and drain. The low interest area has a very coarse mesh. Targeted meshing greatly speeds up the simulation.

3.3.3 Sentaurus Device Simulation Files

Once the structure was defined in SE the next step was to develop the SDE code needed to simulate DC and RF simulations. Discussion with other experts in this field determined that 3 primary simulations would be required to determine the DC and RF performance of these devices: 1) DC I-V curves, 2) S-parameters and 3) transconductance curves.

A typical SDE script consists of the following sections: 1) file, 2) electrode/ thermode, 3) physics, 4) plot, 5) math and 6) solve. The file, electrode/ thermode, physics, and plot sections are the same for all 3 primary simulations. The file section is simply a book-keeping step that keeps track of all of the files during the simulation. The remaining 5 sections of the SDE script will now be discussed.

Electrode and Thermode Blocks

The electrode and thermode sections define all of the contacts for SDE to use in its simulation and are the same for all 3 simulation configurations as shown in Code Excerpt 1. They correspond to the contacts that were defined in the SE file described above. Each electrode has an initial condition set for the voltage, which is "0.0" in all cases as well as a series resistance of 800 Ω. The gate contact is defined differently than the source or drain contacts due to the fact that the gate is a Schottky contact.

```
Electrode {
      { Name="source" Voltage=0.0 Resistor = 800}
      { Name="Gate"   Voltage=0.0 Schottky Workfunction =
      @<3.94 +0.02725*MOLE_FRAC-0.75*MOLE_FRAC*MOLE_FRAC>@ }
      { Name="drain"  Voltage=0.0 Resistor = 800}
}
```

Code Excerpt 1: Electrode definitions.

Physics Block

The physics section is quite complicated and was entirely developed by AFRL. The decision to use certain settings over others was made long before this research topic was started. This section has two primary areas: 1) global physics and 2) region or interface physics. The global physics, as expected, are implemented device-wide, while the region and interface physics impact only those regions and interfaces for which they are specified. This will briefly explain how each line effects the overall simulation, though the physics section of the code is proprietary to AFRL and as such it cannot be included in its entirety in this document but several excerpts are included. Any requests for the complete TCAD code, parameter files, and structure files described herein should be directed to AFRL/RYDD.

The global and region specific physics sections are the same for all 3 key simulation configurations. The code is outlined as shown in Code Excerpt 2. There are two modes available when incorporating piezoelectric effects into the simulation: `stress` and `strain`. The `strain` mode captures the effect of the interface charge due to the strain in the vertical component of the polarization vector at material interfaces. The `stress` mode is more robust and computes the full polarization vector without simplifying assumptions and is used in this research [31]. The `Fermi` command overrides the default use of Boltzmann statistics for determining carrier densities and implements the use of Fermi-Dirac statistics to calculate carrier distributions.

Including the `Thermodynamic` and `Temperature` commands in this section is critical for accurate simulation of self-heating effects. `AnalyticTEP` uses analytical expressions (found on page 429 of [31]) to calculate the thermoelectric power (TEP) for electrons and holes instead of pulling from the default table of experimental values for TEP for silicon that is included with Synopsys TCAD. The `Effective-IntrinsicDensity` is determined without regard to bandgap narrowing due to doping, carrier concentration and temperature. `Highfieldsaturation` accounts for the carrier velocity saturation that occurs due to high electric fields, and `DopingDependence (Arora)` specifies the model used for doping dependent mobility calculations [31].

```
Physics {
      Piezoelectric_Polarization (stress)
      Fermi
      Thermodynamic
      AnalyticTEP
      EffectiveIntrinsicDensity ( Nobandgapnarrowing )
      Temperature
      Highfieldsaturation
      DopingDependence (Arora)}
```

Code Excerpt 2: Global physics block [30]

There are additional physics defined for several specific regions and their interfaces (shown in Code Excerpt 3). Particularly donor and acceptor traps at region interfaces and their associated energy levels are included. Also, Al%-dependent charge concentration expressions are defined in the physics section specific to the interface between the barrier/buffer and the cap/barrier layers. These expressions are proprietary and are not included in this document.

```
Physics (RegionInterface = "Nitride/GaN_Cap"){
      Traps (( Acceptor Level Conc = PROPRIETARY)
             ( Donor Level Conc = PROPRIETARY))}

Physics (RegionInterface = "GaN_Cap/intrinsic-AlGaN_Barrier"){
      Charge ( Uniform Conc = PROPRIETARY)}

Physics (Region = "intrinsic-GaN_Buffer"){
      Traps ( Acceptor Level Conc = PROPRIETARY)
            ( Donor Level Conc = PROPRIETARY)}

Physics (Region = "GaN_w_Charge_Model"){
      Traps ( Acceptor Level Conc = PROPRIETARY)}
            ( Donor Level Conc = PROPRIETARY)

Physics ( RegionInterface = "i-AlGaN_Barrier/AlGaN_w_Charge_Model " ) {
      Charge ( Uniform Conc = @<(PROPRIETARY)>@ )}

Physics ( RegionInterface = "AlGaN_w_Charge_Model/GaN_w_Charge_Model"){
      Charge ( Uniform Conc = @<0.93*(PROPRIETARY)>@ )}
```

Code Excerpt 3: Physics block with proprietary values removed from the code.

Math Block

SDE iteratively solves the partial differential device equations self-consistently at each point of the mesh that is formed in SE. During each iteration, the error is calculated while SDE tries to converge on a solution that reaches the lower threshold of error set by the user. The math block (shown in Code Excerpt 4) contains the mathematical constraints for the numeric solver [31].

`Extrapolate` obtains the initial guess for a given step by extrapolation from the solutions of the previous two steps if they exist. `Digits` specifies the relative error threshold between solutions such that error threshold = $10^{-Digits}$. `Notdamped` specifies the number of iterations over which the error is allowed to increase. `Iterations` sets the maximum number of iterations allowed for each bias step before a solution is reached. If the solver doesn't reach a solution within the error threshold it will automatically reduce the size of the bias step and begin a new iterative solution until it reaches the error threshold or the minimum bias step size defined in the Solve block. `Notdamped` is typically higher than `Iterations` so that the simulation can continue even though the error is increasing [31].

`RelErrControl` prevents error control from using internal error parameters instead of the more physically meaningful error parameters `ErrRef`. The error control parameters, `ErrRef`, are reduced from the default values of $10^{10}cm^{-3}$ to $10^{7}cm^{-3}$ for electrons and $10^{4}cm^{-3}$ for holes in order to accurately track electron and hole concentrations [32].

```
Math{
   Extrapolate
   Digits = 5
   Notdamped=50
   Iterations=15
   RelErrControl
   ErrRef(Electron) = 1e7
   ErrRef(Hole)     = 1e4
}
```

Code Excerpt 4: SDE Math Block [32]

Solve Block

The Solve block defines a sequence of solutions that will be obtained by the solver. The solver starts all contacts at zero bias and ramps them to the bias conditions specified in the code, obtaining solutions at many different points along the way with the step size between points in the code. Each solve block starts with an initial solution as shown in Code Excerpt 5 and builds from there. All configurations (DC I-V, RF and g_m) use the same initial solution.

`Poisson` specifies that the initial solution of the simulation is of the Poisson equation only. Next, `Coupled {Poisson Electron Hole}` introduces the continuity equations for electrons and holes and solves them fully coupled to the Poisson equation using the solution of the first line as the initial guess [31]. Finally, `Coupled {Poisson Electron Hole eTemperature}` solves the electron temperature equations fully coupled to the previously solved Poisson, electron and hole continuity equations. The result of this is the initial solution for each of the simulations.

```
Solve{
*- Initial Solution:
   Poisson
   Coupled{ Poisson Electron Hole }
   Coupled{ Poisson Electron Hole eTemperature }
```

Code Excerpt 5: SDE Initial Solution Block [32]

Before moving on to the actual sweeps it is important to understand how SDE handles ranged sweeps. Figure 35 shows an example of how SDE defines a voltage sweep between 0V and 5V. The start of the sweep is always 0.0 and the end of the sweep is always 1.0. So, for example, a step of 0.5 would be 2.5V and a step of 0.2 would be 1V.

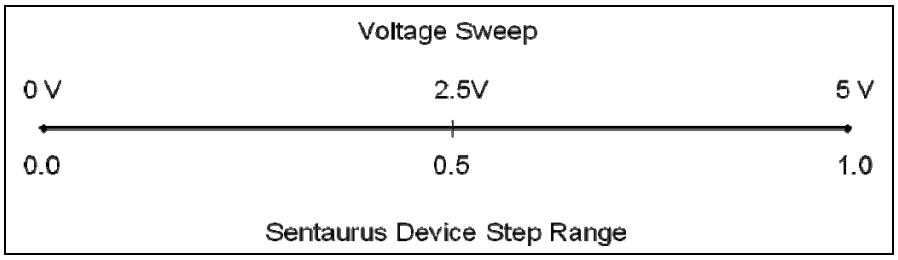

Figure 35: Voltage sweep vs. SDE step range example. As shown above, the entire voltage sweep range of 0V to 5V is described in SDE as a sweep from 0.0 to 1.0.

3.3.4 DC I-V Curve Specific Code

The I-V curve data is generated using two separate sections of code. In the first piece, shown in Code Excerpt 6, V_g is ramped down to `Vgmin` and then up to `Vgmax`. For this research `Vgmin` = -5V and `Vgmax` = 1V to match the gate voltage range measured at AFRL.

A fully coupled method for the self-consistent solution of Poisson, electron/hole continuity equations and electron temperature equations is completed at each step.

`Quasistationary` means that steady state or 'equilibrium' solutions will be calculated for each step of the simulation. The initial step size is specified as 10^{-2} and, assuming that the solution converges at that step size, the next step size will be 1.25×10^{-2}. If the solution does not converge at that step size then the simulation will automatically rerun again at 0.5×10^{-2} and if it still does not converge the step size will continue to decrease until either it does converge or it hits the `Minstep` size of 10^{-5}.

```
Quasistationary(
   InitialStep=1e-2 Increment=1.25
   Minstep=1e-5 MaxStep=0.2
   Goal{ Name="gate"  Voltage= @Vgmin@ }
){ Coupled{ Poisson Electron Hole eTemperature } }

Quasistationary(
   InitialStep=1e-3 Increment=1.2
   Minstep=1e-5 MaxStep=0.2
   Goal{ Name="gate"  Voltage= @Vgmax@ }
){ Coupled{ Poisson Electron Hole eTemperature }
```

Code Excerpt 6: Gate voltage sweep for I-V curves. First the gate voltage is ramped down to `Vgmin` *and then it is ramped up to* `Vgmax`*. Extraneous code such as file loads and saves are not shown [32].*

Once the V_g sweep is complete V_{ds} is swept for each gate voltage specified in SWB as shown in Code Excerpt 7. `i` is an index that is incremented from 0 to `IdVd`, which is the number of curves that are desired. In this case we want 7 curves, one at each gate voltage integer interval from 1V to -5V. V_{ds} is swept from 0V to 20V to match the range of the measured data. `CurrentPlot` tells SDE to break the sweep down into 2 sections: one from 0 to 0.25, which is where the rapidly changing linear region of the curve should be located, with 15 intervals, and the other from 0.25 to 1, also with 15

intervals, which needs less fidelity due to the slowly changing drain current in that region.

```
*- Vd sweeps
 (
  for { set i 0 } { $i < @IdVd@ } { incr i } {
      Quasistationary(
      InitialStep=1e-3 Increment=1.5
      MinStep=1e-5 MaxStep=0.05
      Goal \{ Name=\"drain\" Voltage= @Vd@ \}
    )\{ Coupled \{ Poisson Electron Hole eTemperature \}
        CurrentPlot( Time=(Range=(0 0.25) Intervals=15;
                           Range=(0.25 1) Intervals=15) )
   \}"
  }
)
```

Code Excerpt 7: Drain voltage sweeps for I-V curves. The sweep is run for each gate voltage that was used in the previous section. Extraneous code such as file loads and saves are not shown [32].

Transconductance (g_m) Specific Code

The transconductance simulation as shown in Code Excerpt 8 runs much like the DC I-V curve simulation. After the initial solutions are determined (Code Excerpt 5) V_g is ramped up to `Vgmax` and V_{ds} is ramped up to the desired drain voltage which in this case is 28V. Once V_g and V_{ds} have reached the target voltages V_g is ramped down to `Vgmin` while V_{ds} is kept at 28V. This results in data for an *Id*/*Vg* curve that is then differentiated to develop the g_m curve.

```
*- Gate/Drain ramping to IdVg starting point:
   Quasistationary(
      InitialStep=5e-2 Increment=1.25
      Minstep=1e-5 MaxStep=0.2
      Goal{ Name="drain" Voltage=  @Vd@ }
      Goal{ Name="gate"  Voltage=  @Vgmax@ }
   ){ Coupled{ Poisson Electron Hole eTemperature } }

*- IdVg sweep:
   Quasistationary(
      InitialStep=5e-3 Increment=1.25
      Minstep=1e-5 MaxStep=0.025
      Goal{ Name="gate" Voltage= @Vgmin@ }
      DoZero
   ){ Coupled{ Poisson Electron Hole eTemperature }

   }
```

Code Excerpt 8: Gate and drain voltage sweeps for finding transconductance. First V_g and V_{ds} are ramped up and then V_g is ramped down to `Vgmin` *while V_{ds} is held at 28V. Extraneous code such as file loads and saves are not shown [32].*

RF Simulation Specific Code

The RF simulation follows the same biasing and sweeping scheme of the transconductance simulation. At equidistant bias points a small signal analysis is performed over the frequency range 1 GHz to 26 GHz and all of the admittances and capacitances for all combinations of contacts are stored in the matrix of y-parameters.

In order to accomplish the RF simulation a mixed mode environment is necessary, meaning that instead of simulating the isolated device it is embedded in an external circuit [32]. A two port network is configured as shown in Figure 36 with voltage sources connected to the gate (port 1) and drain (port 2) contacts with the source grounded.

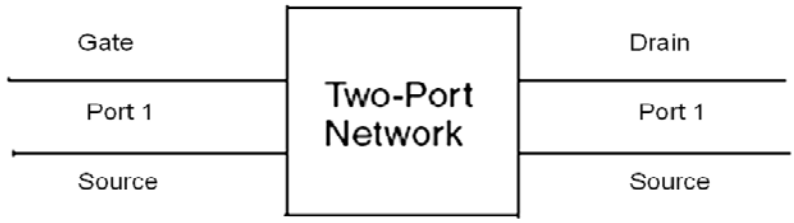

Figure 36: Two-port network configuration for RF simulation of the HEMT [32].

Code Excerpt 8 is similar to the other simulations. V_g is ramped down to `Vgmin` (-5V) and V_{ds} is ramped up to 10V once the initial solutions are determined (from Code Excerpt 4). Once the target voltages are reached V_g is ramped up to `Vgmax` (1V). `ACCoupled` sweeps the frequency from 1-26GHz in 1GHz increments at each V_g and creates the Y-Matrix based on the resulting data.

```
*- Ramping Gate to starting operating point:
   Quasistationary(
      InitialStep=0.01 Increment=1.4
      MinStep=1e-6 MaxStep=0.25
      Goal{ Parameter=vg.dc Voltage= @Vgmin@ }
      Goal{ Parameter=vd.dc Voltage= @Vd@ }
  ){ _Hydro3_ }

*- AC analysis
   Quasistationary(
      InitialStep=0.1 Increment=1.25
      MinStep=1e-6 MaxStep=0.5
      DoZero
      Goal{ Parameter=vg.dc Voltage=@Vgmax@ }
   ){ ACCoupled(
        StartFrequency= 1e9 EndFrequency= 2.6e10
        NumberOfPoints= 26 Linear
        Node(1 2) Exclude(vg vd)
        ACCompute( Time=(Range=(0 1) Intervals=20) )
      ){ Poisson Electron Hole }
```

Code Excerpt 9: Gate voltage is ramped down to Vgmin (-5V) and V_{ds} is ramped up to the required voltage, 10V in this case. Once they reach their target voltage V_g is ramped to Vgmax (1V) with an AC frequency sweep from 1-26GHz in 1GHz increments at each gate bias point. Extraneous code such as file loads and saves is not shown [32].

The resulting y-matrix is post-processed in Inspect®, which is the Synopsys 2-D data analysis package. Inspect® uses built-in routines to convert the y-matrix to the four desired S-parameters. The Inspect® routine uses standard Y-S conversion expressions to complete the transformation, which are readily available in any microwave engineering text book such as [5].

3.4 Modifications to the Model

This research started out using an existing AlGaN/GaN HEMT model that was developed by AFRL. Though it was extremely helpful to have an existing model which, saved an immeasurable amount of time, there were several modifications that were needed in order to make it more suitable for this task. Many hours were spent modifying the code to properly accept the required parameter variations but unfortunately without reprinting the structure file it's not possible to describe these changes clearly to the reader.

One area of significant modification deals with the interface charge. The output current of the device is strongly impacted by the carrier concentration at the AlGaN/GaN interface (the last entry in Code Excerpt 3), as that is where the 2DEG is located. When the device was first simulated it was found that I_{ds} was too high at all V_g values when compared to the family of measured curves as shown in Figure 37.

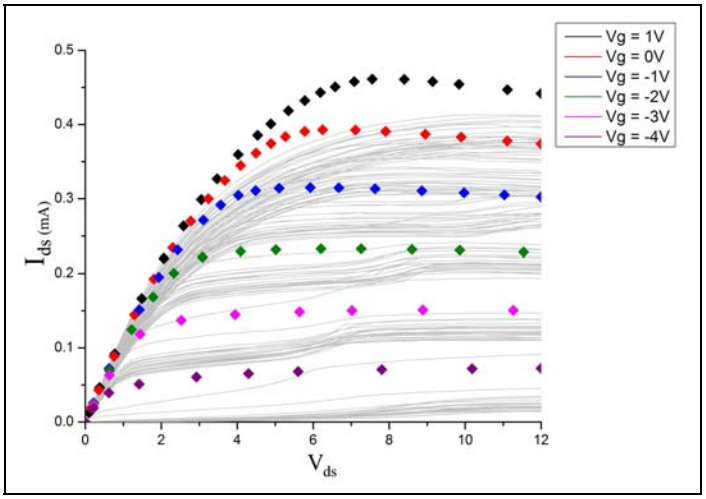

Figure 37: Nominal simulated I-V curves without the charge fitting factor included clearly showing that simulated I_{ds} is too high for all V_g.

A fitting factor (red text in Code Excerpt 3) was chosen using the plot generated in Figure 38. The light gray curves are the measured curves for V_g = 1V for a single wafer while the colored curves are simulation results for the nominal device with V_g = 1V for a charge fitting factor of 0.80 to 1.1. Using a visual assessment of which curve was the most "in family" it was determined that a 0.93 charge factor provided the best overall fit. Complete I-V curves with the charge fitting factor implemented can be seen in Figure 59. Though the curves for V_g = -1 to 1V are much closer than those seen in Figure 37, V_g = -4 to -2V are still not as accurate as hoped. This is due to the nature of the measured data where the I-V curves are not evenly spaced at higher V_g but the simulated curves are evenly spaced. The reason for this behavior in the measured data is not known and the discrepancy between the simulated and measured curves cannot be explained by this researcher. The simulated curves still suit their purpose in being able to demonstrate output changes based on parameter variance though.

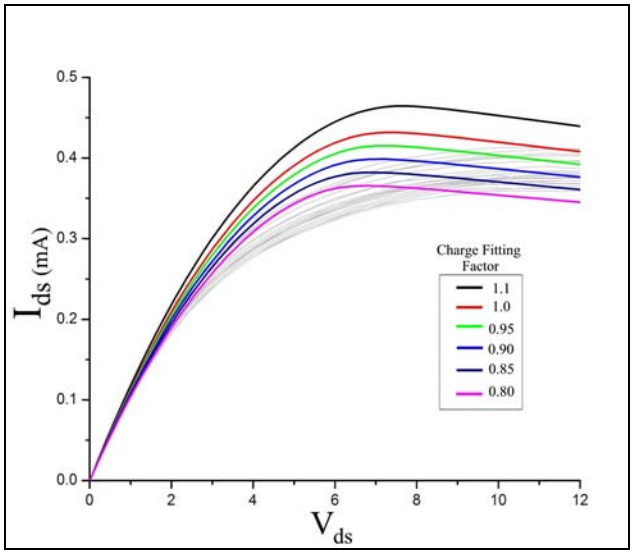

Figure 38: Simulated V_g = 1V I-V curves for varying charge fitting factors plotted over measured curves. A charge fitting factor of 0.93 was chosen visually as the best fit.

Another area where AFRL's code was modified was in the SDE file. The simulation settings used by AFRL were very "brute force" and didn't use some useful features of the TCAD software package. Synopsys published a DC and RF HEMT characterization template that used some of the more advanced features available in the software. Many hours were spent combining the AFRL structure and physics blocks with the Synopsys DC and RF solve blocks and Inspect scripts. This resulted in a far more robust simulation environment where key operating parameters such as $|h_{21}|, f_t, f_{max}, g_m$, and threshold voltage could be easily extracted. Due to the complexity of the software, this took much more time than originally estimated as significant time was spent to achieve successful simulations with the new combined code.

3.5 Chapter Summary

This chapter began with a description of the nominal wafer including general dimensions of some key parameters as well as a description of the epilayer characterization that was provided by AFRL/RYDD. The process of collecting the DC and RF measured data was described along with the equipment that was used to do so. A general overview of how TCAD operates was provided as well as the process flow used in the simulations that were run for this thesis. The 2-D model was described followed by a detailed breakdown of the SDE file and its associated physics (where not limited by proprietary prohibitions). The chapter closed with an explanation of several areas where the AFRL provided code was modified for this research.

Chapter 4. Analysis and Results

4.1 Chapter Overview

This chapter presents the experimental and simulated data that were collected during this research. First, wafer plots are presented that show actual epilayer characteristics and DC/RF performance trends across each wafer for a device designed with a nominal L_g of 0.5μm. Next, the TCAD model that was developed for this research is presented and explored to demonstrate that device physics are represented correctly. Then experimental data is used to validate the TCAD model and confirm that it behaves as expected followed by simulation results that show the direct effect of individually varying the three parameters of interest ± 5% from the nominal. Finally, the measured DC/RF data from the 0.5μm device is compared with data collected from 0.9μm L_g devices on the same wafers to attempt to attribute performance differences to geometry differences (such as variation of L_g, source/drain spacing, field plate design etc…) or epilayer variations (such as layer thicknesses, Al%, growth quality etc…).

4.2 Experimental Data

4.2.1 Wafer Epilayer Data

Wafer epilayer characterization was completed by AFRL with the results provided to me for this research in *.JMP file format which was processed and analyzed using JMP version 6.0 statistical software at AFIT. The provided data was collected at specific sites on each wafer and was then interpolated in JMP to produce the full wafer

contours. There are 5 pieces of the available epidata that are of interest: 1) Al%, 2) AlGaN thickness, 3) n_s, 4) sheet resistance (R_{sh}) and 5) electron mobility (μ).

1) Al%

Al% measurements were only taken at 3 sites on each wafer and show the trend from the bottom (yLoc = -3) to the top (yLoc = 3) in Figure 39. The variation across each of the wafers follows a slightly different trend but generally each wafer has a lower Al% at the top than at the bottom with the maximum across all wafers being 0.2654 and the lowest being 0.2475.

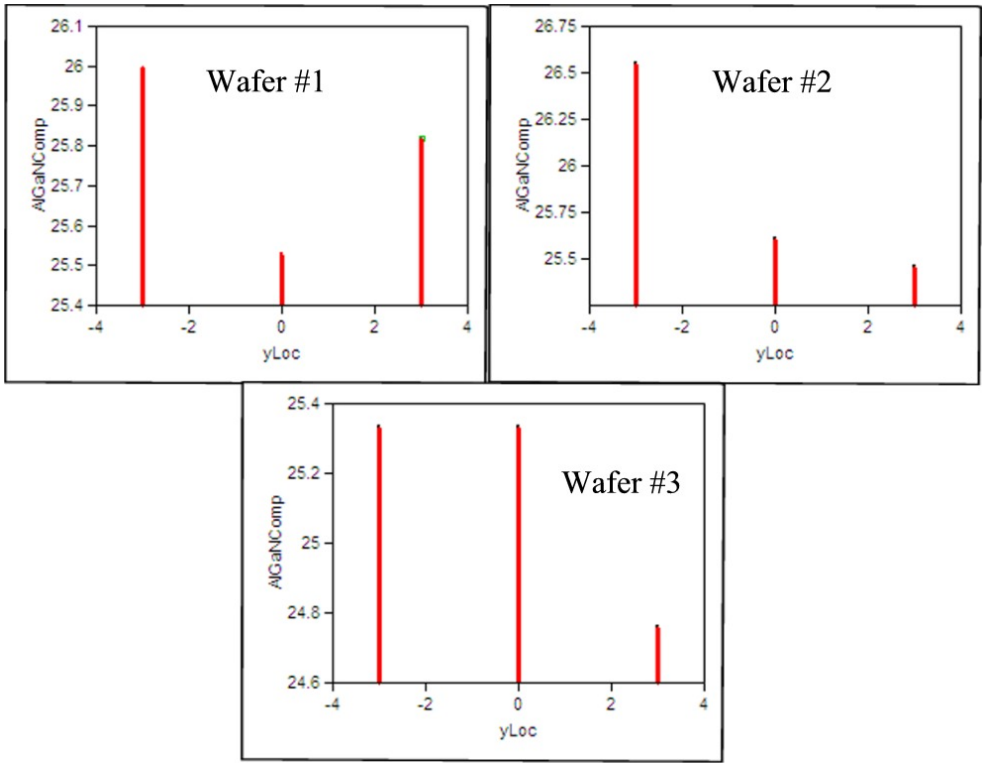

Figure 39: Al% as a function of yLoc with yLoc = -3 the bottom and yLoc = 3 the top of the wafer.

2) AlGaN Thickness

Figure 40 shows contour plots of the AlGaN layer thickness (including the thin GaN cap) across each wafer. Data was collected at 9 discrete sites across each wafer and then interpolated using JMP to create the contours in Figure 40. There is a clear trend across all three wafers where the AlGaN layer thickness decreases as you move from top to bottom, possibly due to thermal variation across the susceptor, with the minimum measured thickness being 235.3 Å and the maximum measured thickness being 248.4 Å.

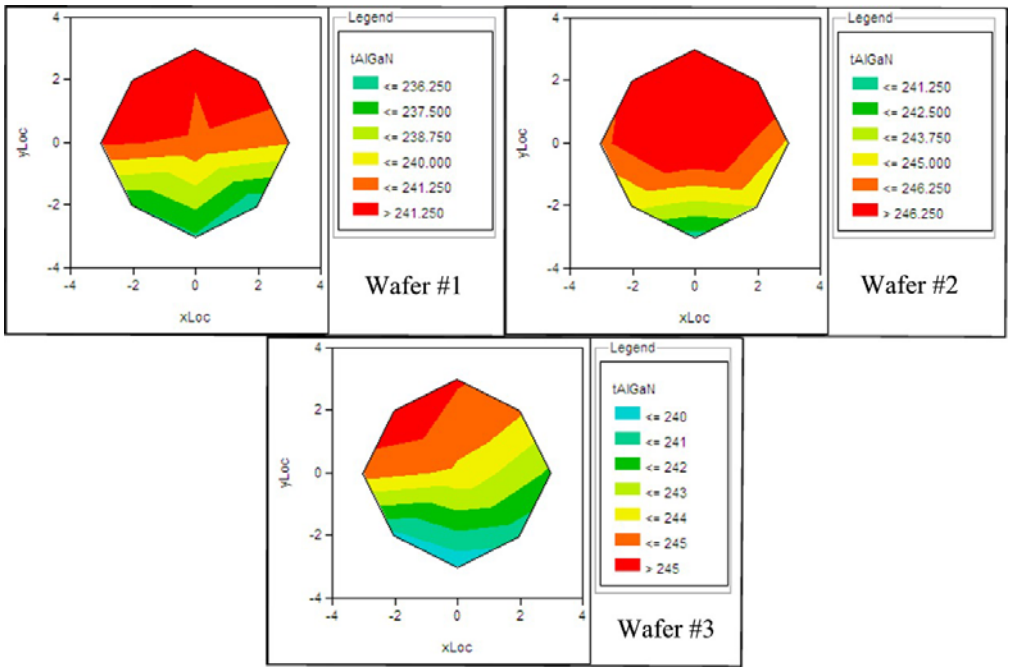

Figure 40: Contour plots of d_{AlGaN}, including the GaN cap, (in Å) across each of the 3 wafers. There is a trend of decreasing thickness across the wafers from top to bottom.

3) Sheet Carrier Concentration at the 2DEG (n_s)

Figure 41 shows contour plots of the sheet carrier concentration at the 2DEG across each wafer. Data was collected at 9 discrete sites across each wafer and then

interpolated using JMP to create the contours in Figure 41. There is no noticeable trend across any of the wafers. The minimum measured n_s being 8.3 x 10^{12} cm^{-2} and the maximum measured n_s being 1.06 x 10^{13} cm^{-2}.

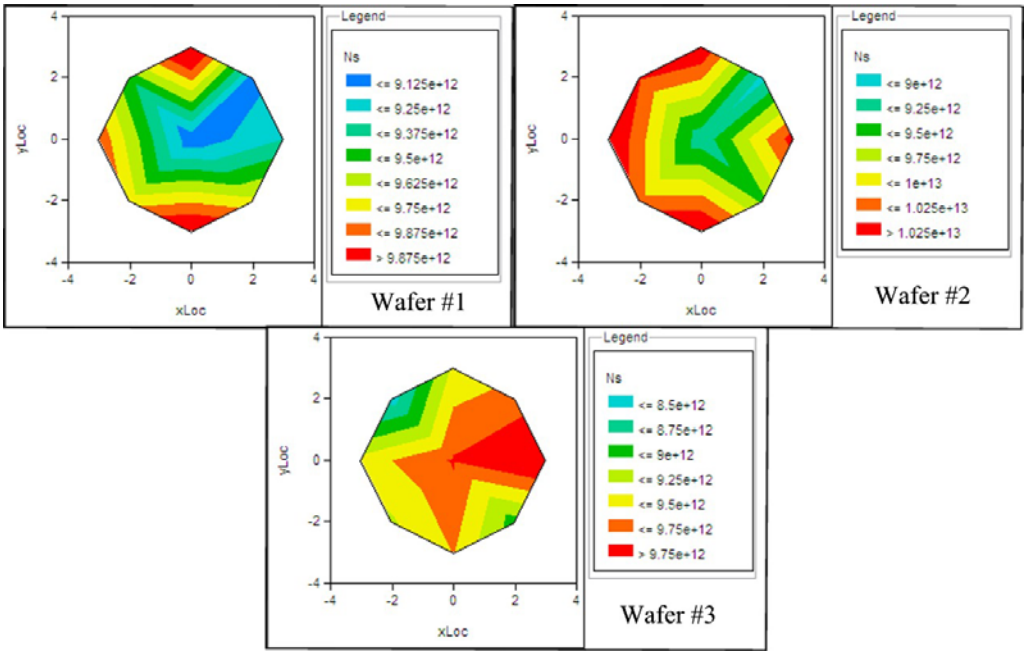

Figure 41: Sheet carrier concentration (cm^{-2}) across each wafer measured using the Hall effect at room temperature. There is no noticeable trend across the wafers for n_s.

4) Sheet Resistance (R_{sh})

Figure 42 shows contour plots of the sheet resistance across each wafer. Data was collected at 9 discrete sites across each wafer and then interpolated using JMP to create the contours in Figure 42. There is a noticeable trend across all three wafers showing R_{sh} decreasing from top to bottom. The minimum measured R_{sh} being 383.6 Ω/□ and the maximum measured R_{sh} being 416.4 Ω/□.

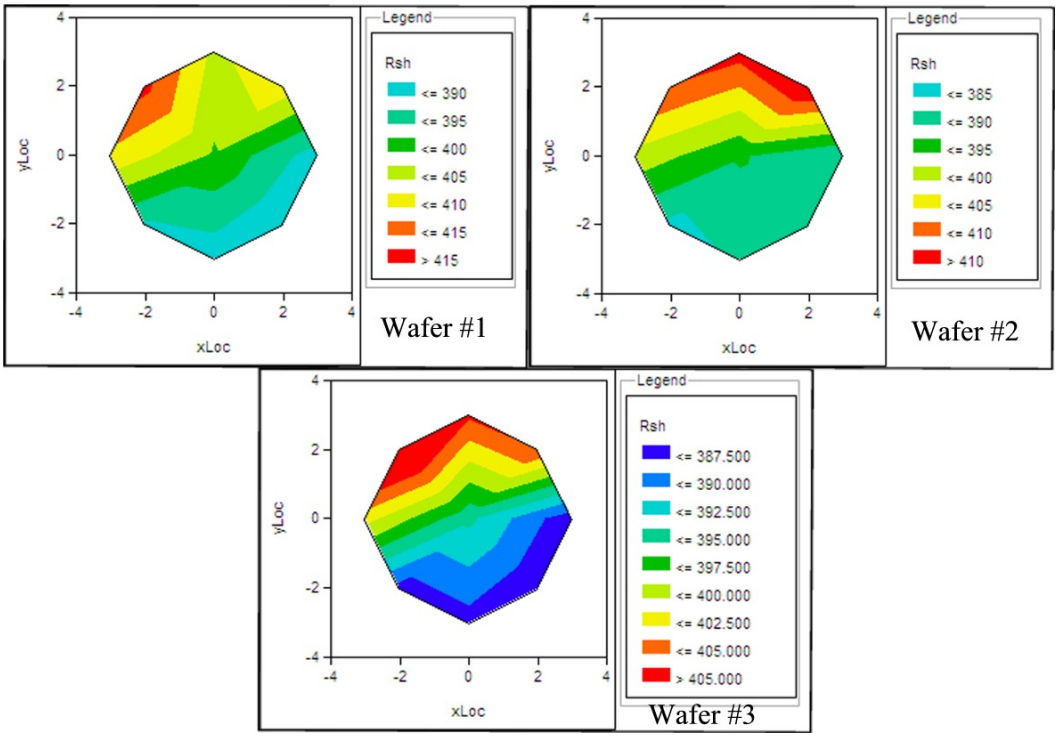

Figure 42: Sheet resistance (Ω/□) plotted across the three wafers. There is a clear trend showing R_{sh} changing from high to low from the top to bottom of the wafer.

5) Electron Mobility (μ)

Electron mobility was not measured directly but was calculated using

$$\mu = \frac{1}{qR_{sh}n_s}. \tag{31}$$

The trend across all three wafers is not the same. Wafers 1 and 2 display increasing mobility when moving from the top left to bottom right areas while wafer 3 shows increasing mobility from the top right to bottom left areas.

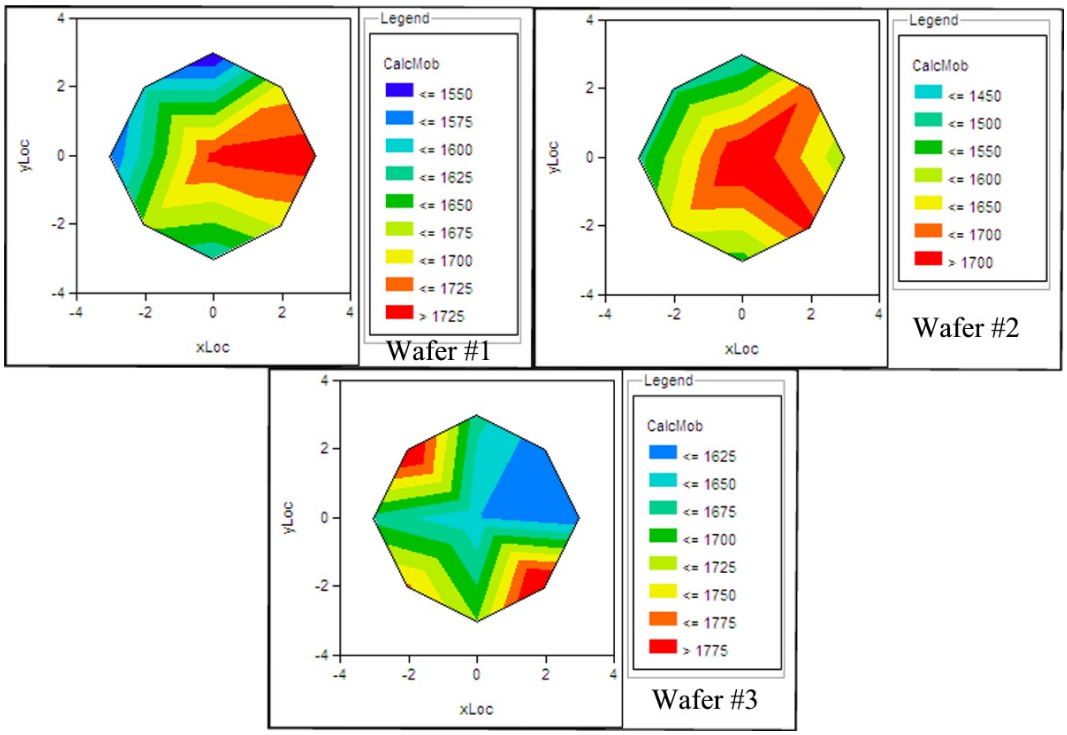

Figure 43: Electron mobility contour plots for all three wafers. Wafers 1 and 2 show the trend of increasing mobility from the top left to bottom right areas of the wafer while wafer 3 increases from the upper right to lower left areas.

4.2.2 Wafer DC/RF Performance Plots

These plots are generated in Matlab using the DC and RF data from the Cascade Microtech 12000 probe station. They allow us to quickly visualize performance trends across wafers, if there are any, by using a gradient and grid system to represent each measured device. The coordinate system used by the Cascade probe station is slightly different than the one used to collect the epidata. Figure 44 directly correlates the epidata coordinate system with the Cascade coordinate system. For example, device (-1,-2) in the epidata is device (3,2) in the Cascade data.

There are 5 performance trend plots presented here for wafers 1 and 3 (wafer #2 was returned to the manufacturer before data could be collected on the 0.5 µm devices): 1) I_{max}, 2) g_{mpeak} (maximum transconductance), 3) V_{gmp} (V_g at g_{mpeak}), 4) f_t at V_{gmp} and 5) f_{max} at V_{gmp}. A wafer plot legend is provided in Figure 45 which explains how to read the data collected by the Cascade probe station.

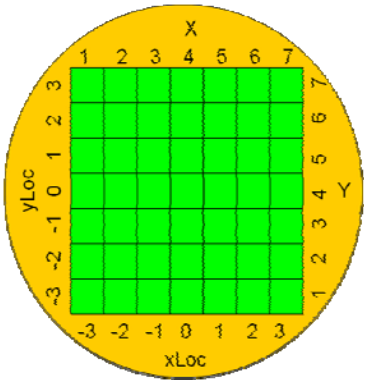

Figure 44: Plot showing how the epidata coordinate system (-3 to 3) correlates to the coordinate system used for the Cascade probe station (1 to 7)

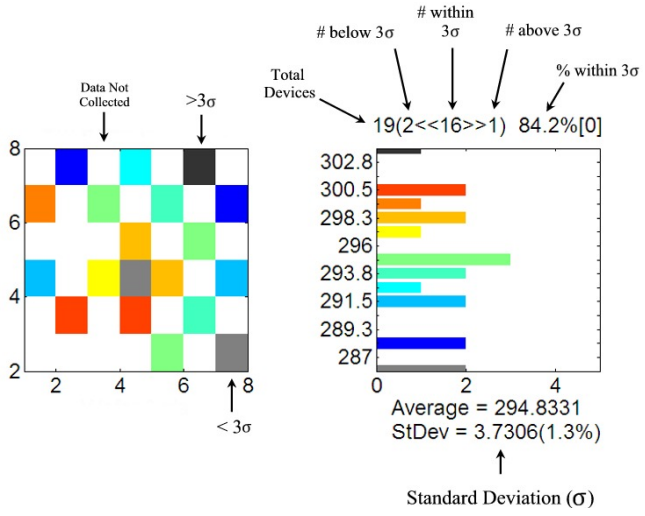

Figure 45: Wafer plot legend explaining how to read the data collect by the Cacscade probe station

1) I_{max}

Figure 46 shows the wafer plot of I_{max} for both wafers. There is a clear trend seen on both wafers with the lowest I_{max} being found in the upper left corner of the wafer and the highest I_{max} found in the lower left corner.

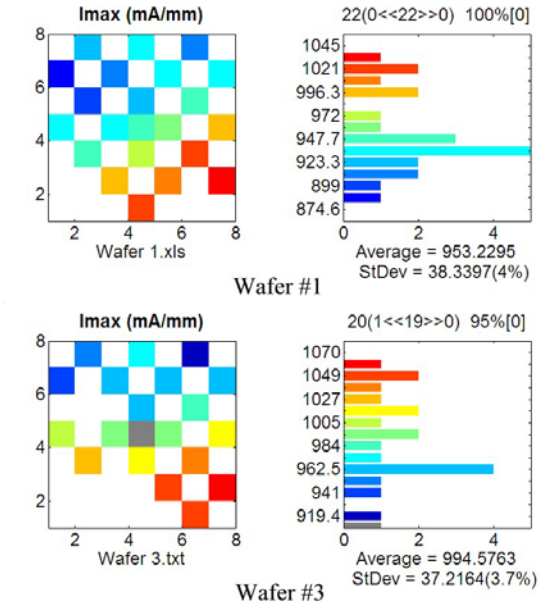

Figure 46: I_{max} wafer plots for wafers 1 and 3. There is a clear trend showing I_{max} increasing from the top left to bottom right corners on both wafers. Wafer 3 has a slightly higher average I_{max} than wafer 1.

2) g_{mpeak} (Maximum Transconductance)

Figure 47 shows the wafer plot of g_{mpeak} for both wafers. There isn't a strong trend shown but both wafers do show an increase in g_{mpeak} from right to left. Average g_{mpeak} is much higher on wafer 1 than on wafer 3.

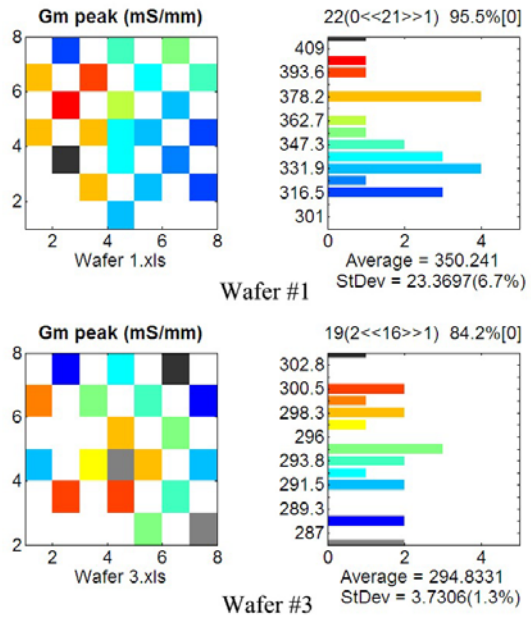

Figure 47: g_{mpeak} wafer plots for wafers 1 and 3. There is no strong trend here, though g_{mpeak} does seem to be higher on the left half than on the right.

3) V_{gmp}

Figure 48 shows the wafer plot of V_{gmp} (V_g at g_{mpeak}) for both wafers. Though wafer 1 shows a trend of increasing V_{gmp} from bottom right to upper left closer inspection reveals that both wafers have a very consistent average value near -3.5V for V_g at maximum transconductance.

4) f_T (Unity Current Gain)

Figure 49 shows the wafer plots of f_T for both wafers. f_T varies greatly across both wafers with wafer 1 showing cutoff frequencies ranging between 18 and 24 GHz and wafer 3 showing cutoff frequencies ranging between 20.5 and 23.5 GHz. There is no noticeable trend seen across wafer 3 and only a slight trend of f_T increasing from top to bottom on wafer 1.

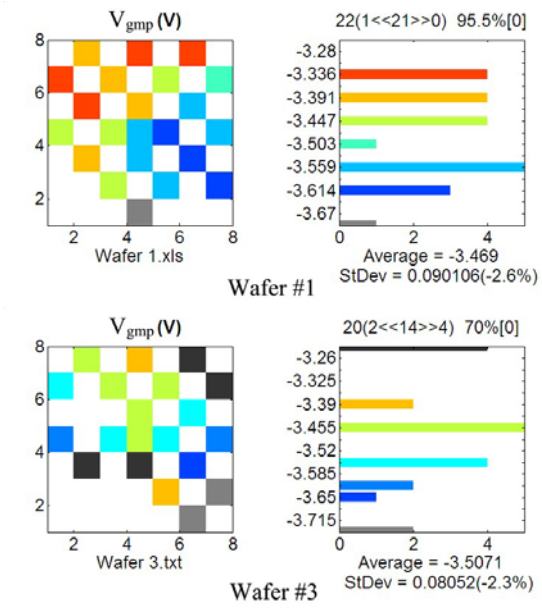

Figure 48: V_{gmp} wafer plots for wafers 1 and 3. V_{gmp} is fairly consistent across both wafers.

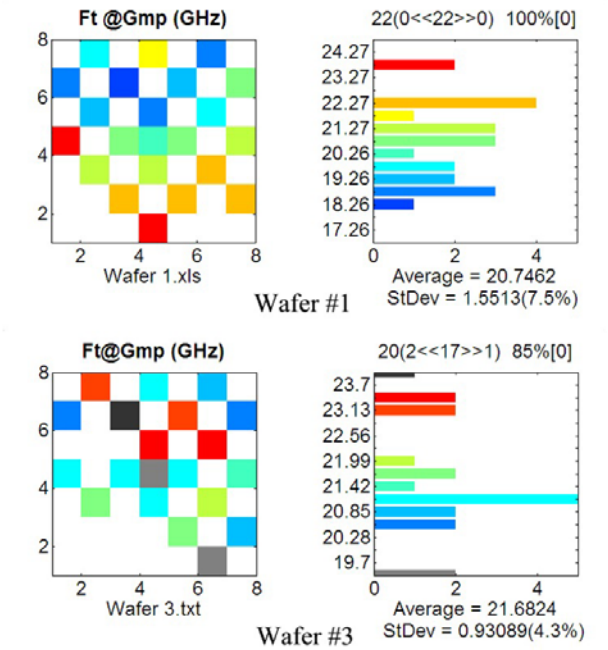

Figure 49: f_t wafer plot for wafers 1 and 3. f_t varies greatly across both wafers but there is no noticeable trend.

5) f_{max} (Unity Power Gain)

Figure 50 shows the wafer plots of f_{max} for both wafers. There is no noticeable trend seen across either wafer with average f_{max} for both wafers at 22 GHz. In typical applications f_{max} is considerably higher than f_t but in this case it is almost equal. This device is a power HEMT which utilizes a large field plate which causes the electric field to decrease and spread out between the gate and drain which in turn allows a higher breakdown voltage. The downside to this is that the gate to drain capacitance (C_{gd}) increases dramatically which causes f_{max} to decrease as explained in section 2.2.3.

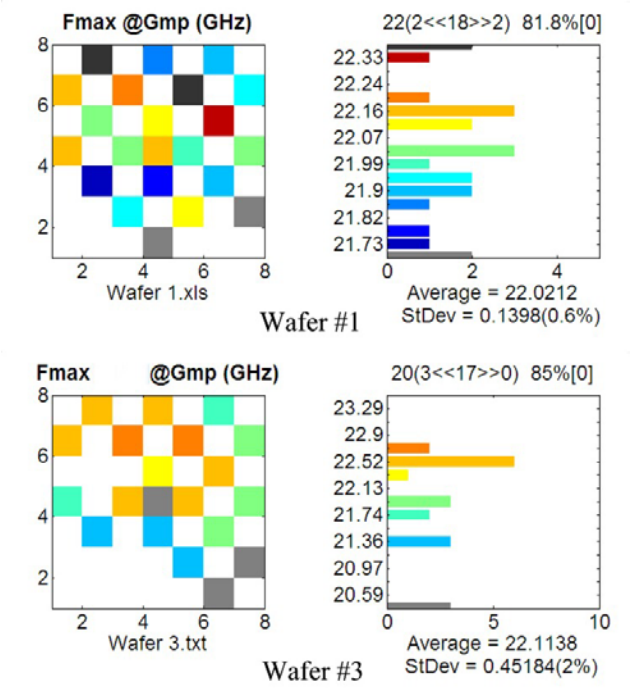

Figure 50: f_{max} wafer plots for wafers 1 and 3. f_{max} is fairly consistent across both wafers with no noticeable trends.

4.3 TCAD Model Behavior

Due to the proprietary nature of the investigated device, exact geometry and dimensions cannot be revealed in the graphical representations of the device generated from the output of TCAD. Images taken from the simulations are magnified to mask the exact dimensions of the device. Any requests for more detailed images of device geometry should be made directly to AFRL/RYDD management.

Figure 51 shows an SEM image of the region of interest in one of the devices while Figure 52 shows the same region in the modeled device. There are layers of silicon-nitride on top of the cap layer as well as an AlN layer on top of the SiC substrate as described earlier but they are not of interest for these simulations. The primary areas of interest are the GaN cap, AlGaN barrier and the top portion of the GaN buffer as that is where the conducting channel is located.

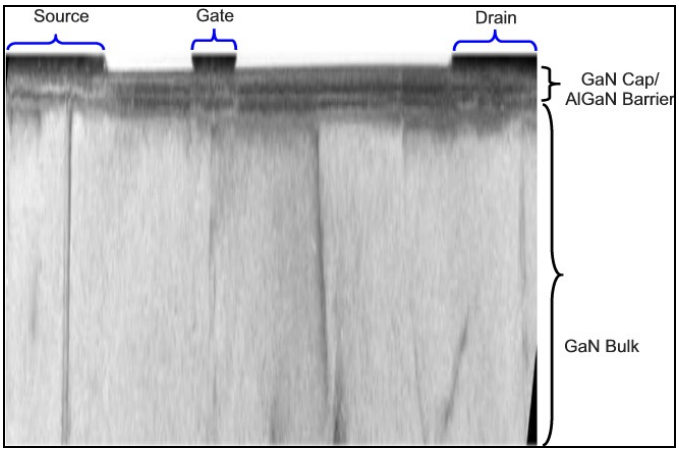

Figure 51: SEM image of the region of interest on a representative experimental device. Provided by AFRL/RYDD.

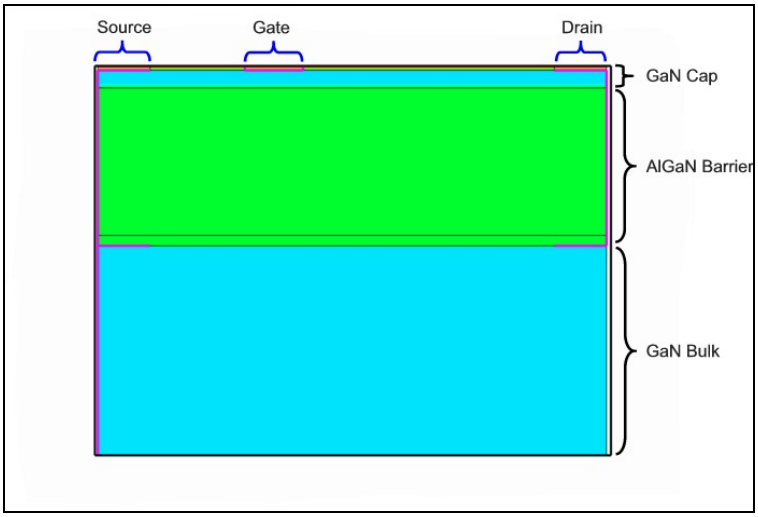

Figure 52: Structure as modeled in TCAD. Only regions of interest are shown. Device width to height aspect ratio in the image is not 1:1in order to mask the true structure of this proprietary device.

Once the nominal model was constructed in TCAD, a simulation was run to see how the modeled device behaved under the initial conditions of $V_g = 0\text{V}$ and $V_{ds} = 0\text{V}$. Pictured in Figure 53 is the energy band diagram through the device as calculated by TCAD. The band diagram is shown directly beneath the center of the gate contact. The bands appear as expected based on the device configuration and structure. Starting at the gate contact and moving into the wafer, the GaN cap/bulk layers show a band gap of 3.4 eV and the AlGaN barrier layer shows a band gap of 3.93 eV, which is accurate for an Al% of 0.25 based on Figure 9.

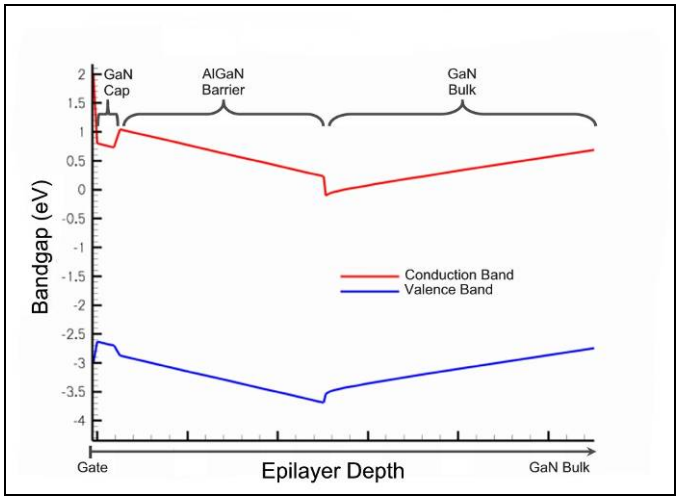

Figure 53: Energy band diagram at V_g and V_{ds} at 0V. Bandgap values are as expected and are supported by Figure 9. In this plot E_F is at the 0 reference.

Figure 54 and Figure 55 show the carrier distribution throughout the device. The channel is clearly visible in the GaN bulk at the heterointerface as expected. Carrier concentrations over 10^{21} cm^{-3} are found at the peak of the 2DEG but it quickly decreases to a negligible amount as we move away from the interface. There is a high density of carriers shown inside the source and drain contacts. These regions were n-type doped at 10^{17} cm^{-3} to ensure a good ohmic contact solely for the simulations and are not part of the actual device design. The classical model for carrier distribution was used for these simulations versus the more accurate quantum mechanical model for several reasons. The quantum mechanical model is much more computationally intensive than the classical model and also makes the simulations much more unstable which can cause significant convergence issues. The classical model, combined with the interface charge fitting factor discussed in chapter 3, provides sufficient accuracy for the purposes of this research.

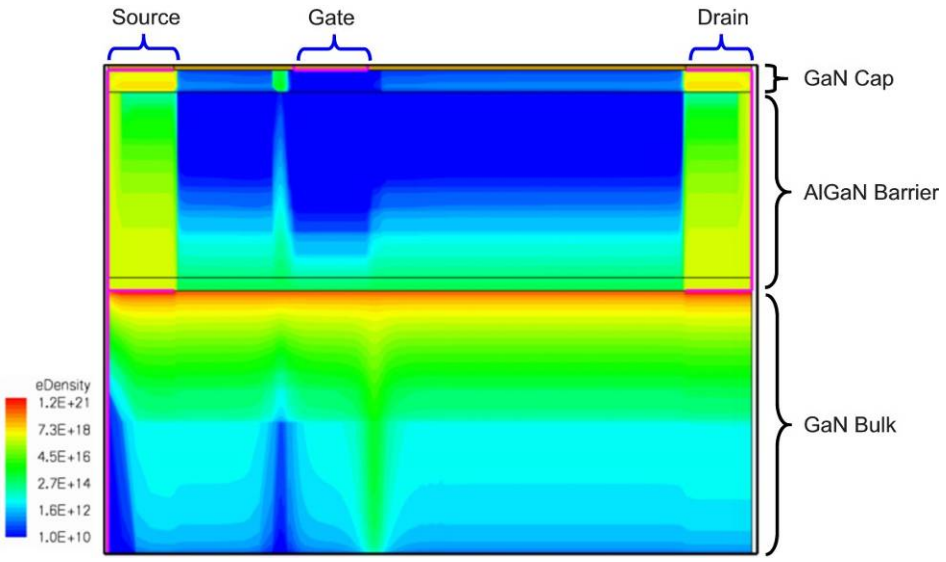

Figure 54: 2-D carrier density plot with V_g and V_{ds} at 0V on a logarithmic scale. The channel is clearly visible at the heterointerface as expected due to piezo-induced carriers from the AlGaN/GaN material system. The vertical spikes shown on either side of the gate are an artifact of finer mesh resolution at those locations.

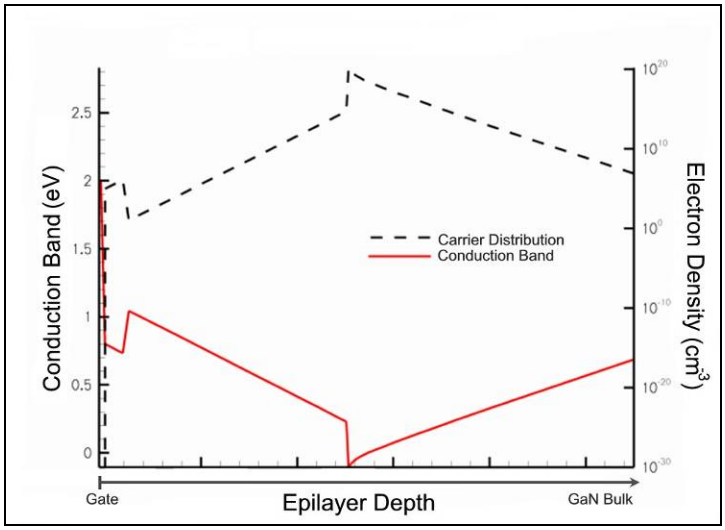

Figure 55: 1-D carrier density (calculated using the classical method) plot directly underneath the gate contact at zero-bias. The highest density of carriers is found in the 2DEG at the heterointerface as expected.

Model behavior was recorded while V_g was swept over the range 0 to -5V and V_{ds} stayed at 0V (shown in Figure 56 and Figure 57). Under these conditions as V_g becomes more negative E_c increases relative to E_F, the channel is depleted of carriers directly beneath the gate and the device is pinched-off when V_g = -5V.

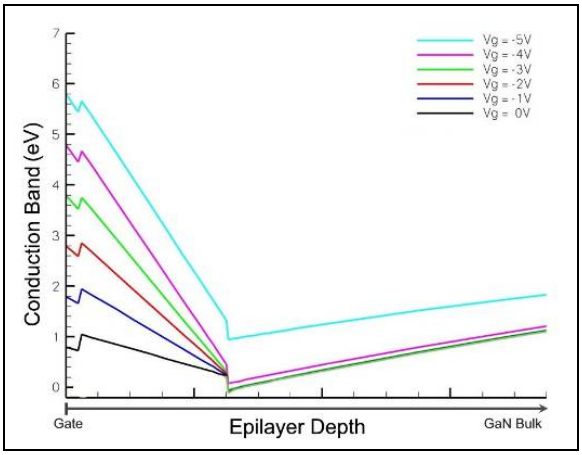

Figure 56: Conduction band energy (E_c) behavior over the range of V_g from 0V to -5V with E_F at the 0 reference.

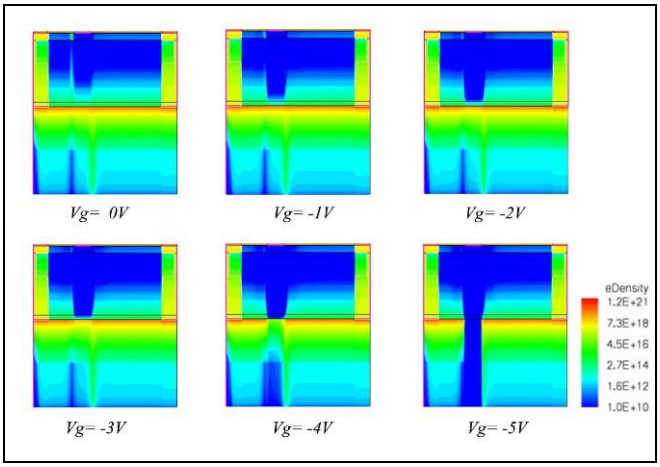

Figure 57: Channel depletion under the gate occurring over the range 0 to -5V V_g.

The results presented in Figures 52-58 demonstrate that the model behaves as expected. The energy band diagram is shaped correctly and the carriers are distributed appropriately throughout the material. The device is properly pinched off as V_g goes more negative. Next the simulated DC and RF data was compared to the measured data collected at AFRL/RYDD to validate that the device model accurately predicts "real life" device output.

4.4 Measured Data vs. Optimal Simulation Data

4.4.1 DC I-V Curves

I-V curve data was collected at AFRL for all devices on each wafer. Figure 58 shows all of the I-V curves for one wafer (36 devices) plotted together. Both wafers have similar I-V plots. These are plotted together to show the range over which the magnitude of I_{ds} can vary from device to device on the same wafer for the same V_{ds} and V_{gs} combination. Figure 59 shows the I-V curves collected from a simulation of a single device with nominal values of L_g = 0.5 μm, d_{AlGaN} = 225 Å and $Al_{\%}$ = 0.25 used. The simulated curves are generally within the family of the measured curves and as such they are suitable for determining the performance trends that result from variations in L_g, d_{AlGaN} and Al%.

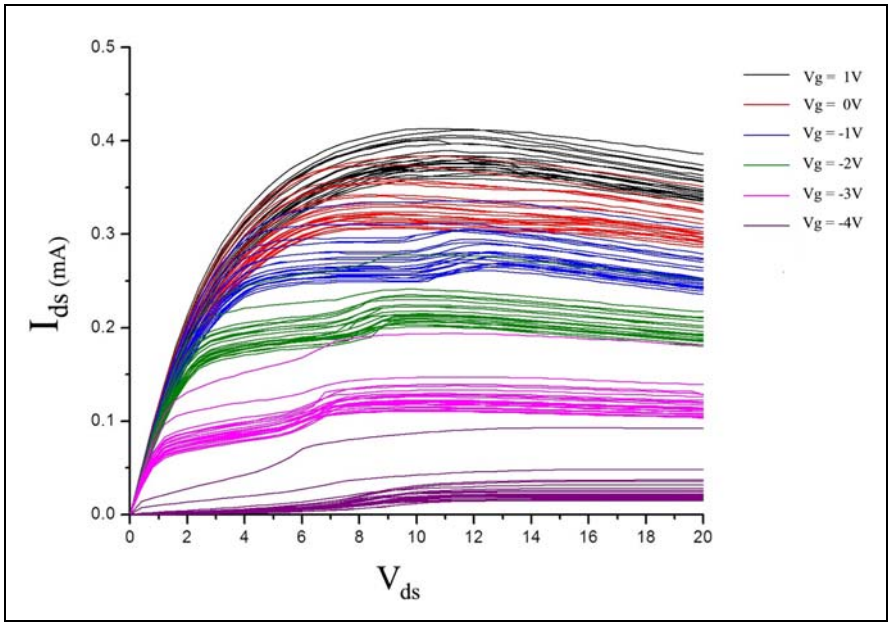

Figure 58: I-V curves from one wafer collected at AFRL (Wafer #1).

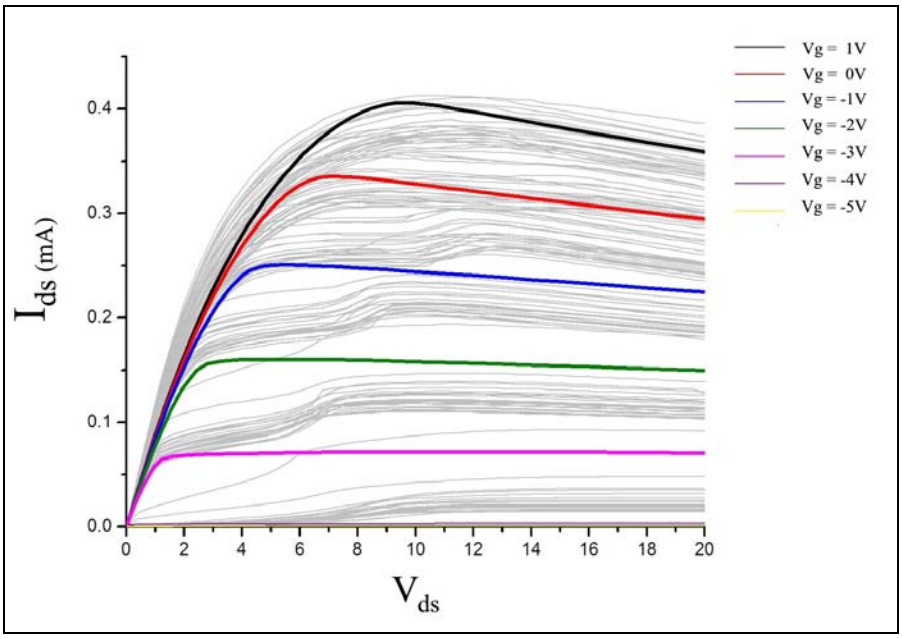

Figure 59: Nominal device model I-V simulation results overlaid on the Wafer #1 I-V plot. The simulated data matches the measured data closely enough to accurately determine the trends as key device parameters are varied.

4.4.2 Transconductance

Figure 60 shows the transconductance of all devices plotted together on a single plot to show the range over which g_m varies on a single wafer. Transconductance was measured at V_{ds} = 28V for these devices. Maximum g_m is found anywhere between -3.3 and -3.6V V_g (V_{max}) for all measured devices. Figure 61 shows the transconductance of the nominal device overlaid on the measured transconductance curves. The g_m measurements show an unexplained drop in g_m around -1V V_g on all three wafers. This drop is not found in the simulated data and since optimal operation is found at V_{max} the drop at -1V V_g is not explored in this research.

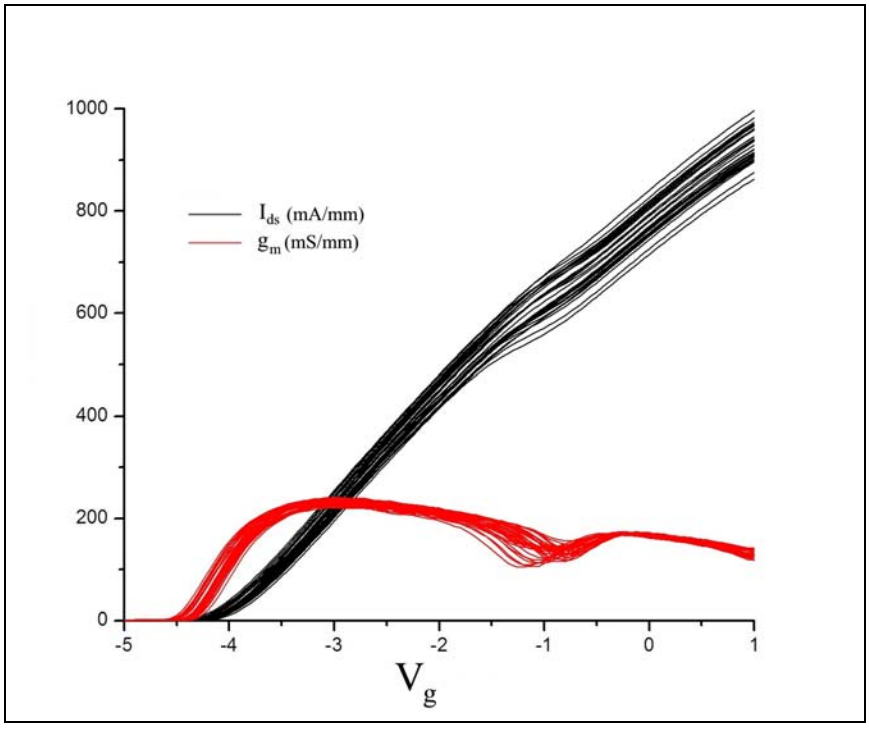

Figure 60: Transconductance vs Vg measured at V_{ds} = 28V plotted for all devices on Wafer #1.

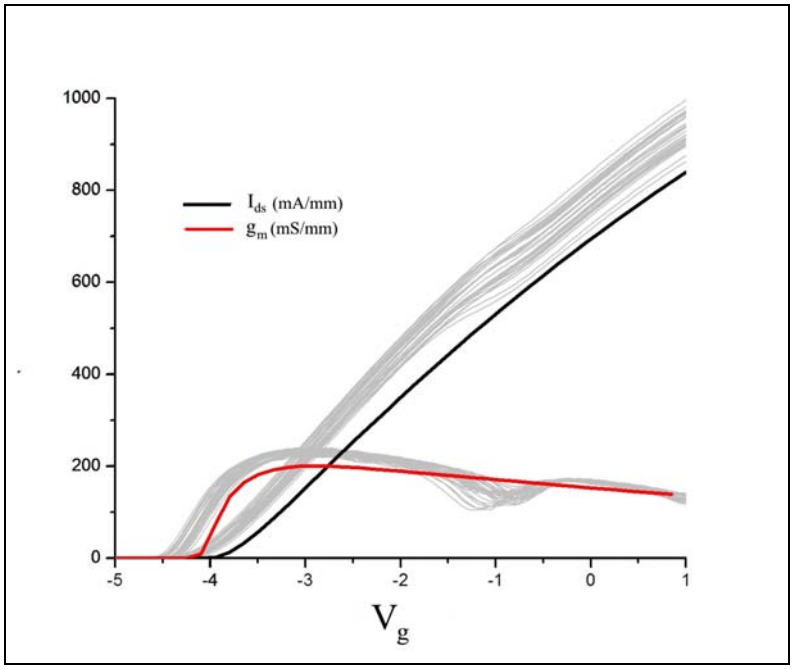

Figure 61: Nominal device model g_m and I_{ds} simulation results at V_{ds} = 28V overlaid on the Wafer #1 g_m and I_{ds} plots. The simulated data matches the measured data closely enough to accurately determine the trends as key device parameters are varied.

4.4.3 RF Data

RF data was measured at V_{gmp} for all devices. This voltage varies from device to device so V_g = -3.5V was chosen as the gate voltage at which to run the nominal model simulations and was chosen because it was the most commonly measured V_{gmp} for all devices, ± 0.05V.

Figure 62 is a plot of the magnitude of h_{21} from the nominal simulated device, which is the magnitude of the output current over the magnitude of the input current. When $|h_{21}|$ is equal to 1, the device has reached its current gain cutoff frequency, f_T. Comparing the cutoff frequency of 21 GHz to Figure 49 demonstrates that the modeled device has the same cutoff frequency as a measured device.

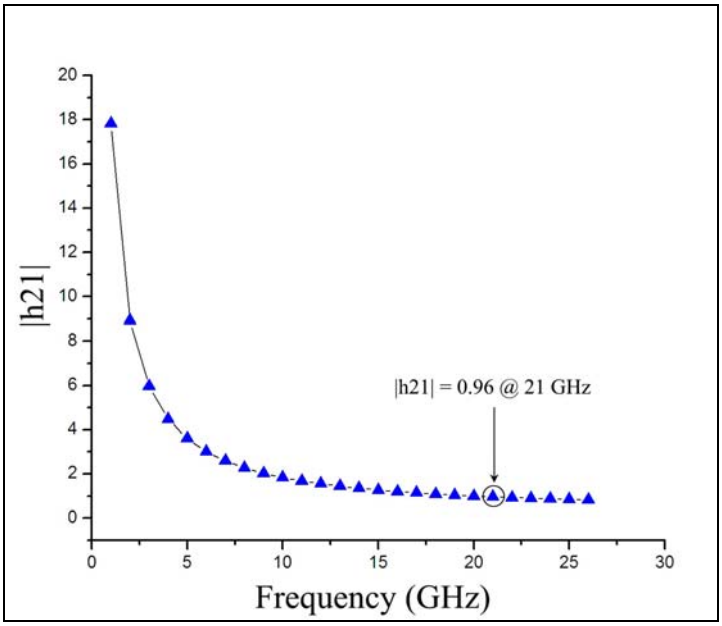

Figure 62: Modeled $|h_{21}|$ as a function of frequency. f_t is equal to the frequency at which the magnitude of h_{21} is equal to 1. The nominal model cuts off at 21 GHz which compares well to Figure 49.

Figure 63 shows a comparison between simulated and measured S_{21} data as frequency is swept starting from 1 to 26 GHz. Measured data for all 36 devices from wafer #1 are shown in the figure. The plots match very closely near 1GHz, but as the frequency increases the modeled behavior matches the measured data even more closely. Figure 64 shows the data points inside the 1.5 magnitude circle to facilitate data comparison at the higher frequencies. Overall, the nominal model very closely simulates the measured devices at high frequencies.

4.4.4 Overall Model Suitability

Based on the data presented in sections 4.1 through 4.3 this TCAD model is suitable for determining which single parameter variation has the greatest impact on device performance. Though the simulation does not produce results that are exactly the

same as the measured data, they are well within reasonable tolerances for determining device sensitivity to changes in the 3 key parameters that are studied in this research.

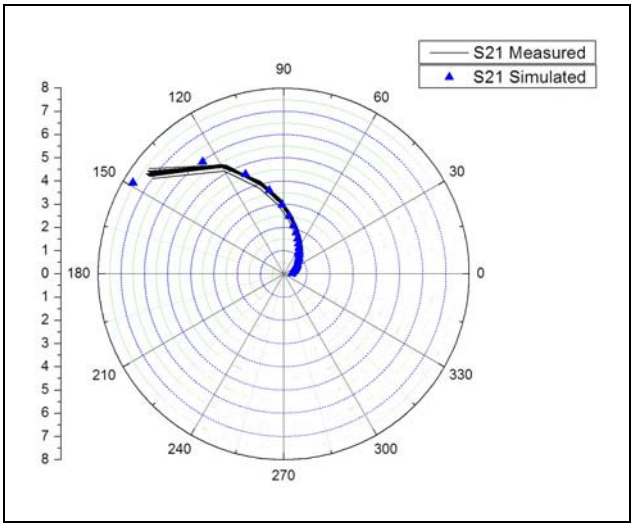

Figure 63: Measured S_{21} vs nominal simulated S_{21} across the full range of frequencies 1-26GHz with $V_g = V_{gmp.}$

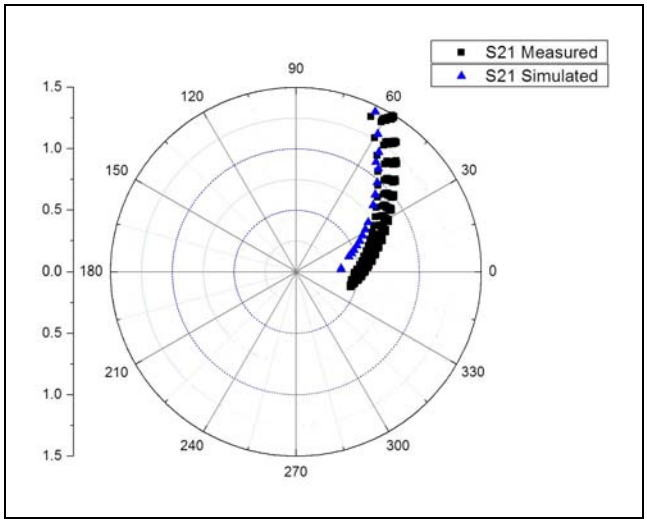

Figure 64: Measured S_{21} vs nominal simulated S_{21} showing the magnitude of S_{21} near unity. The high frequency performance of the model is very close to that of the measured devices.

4.5 Parameter Variations in TCAD

Originally the plan was to collect exact measurements for d_{AlGaN}, Al% and L_g and simulate the model using those values to show that the difference between the measured and simulated performance could be decreased by accounting for actual variations. However the measured epilayer data and device geometry varied by only 0-2% which rendered the planned simulations irrelevant. Throughout this section the percent change in the ±5% simulation results relative to the nominal simulation results is presented. The percent change is calculated by

$$\left(\frac{\pm 5\%\ \text{Sim Results - Nominal Sim Results}}{\text{Nominal Sim Results}}\right)*100\,. \tag{32}$$

This representation of the data was chosen due to the fact that the magnitude of the change in the output is quite small and as a result visualization is easier using percent change.

4.5.1 Barrier Thickness (d_{AlGaN})

Figure 65 is a comparison plot of the I-V curves of the nominal device, the device with +5% d_{AlGaN} and the device with -5% d_{AlGaN}. V_g was swept from -4V to 1V and V_{ds} was swept from 0V to 20V. Upon inspection, it is clear that increasing d_{AlGaN} increases the output current and conversely decreasing d_{AlGaN} decreases the output current. This makes sense due to the fact that when increasing d_{AlGaN} for a given gate bias the 2DEG concentration increases, which in turn increases I_{ds} [26].

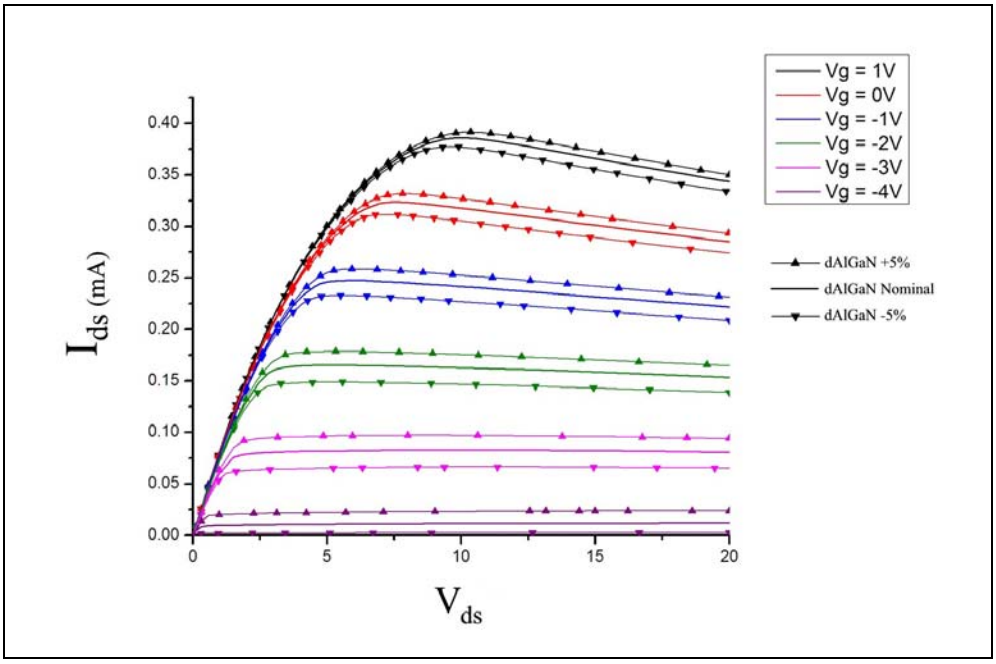

Figure 65: Simulated I-V curve comparison plots for d_{AlGaN} ± 5%. Increasing d_{AlGaN} results in an increase in I_{ds}.

Figure 66 shows the percent change in the output current at each combination of V_g and V_{ds} for the ±5% change in d_{AlGaN} (-4V V_g is not shown because it is so close to pinch-off that it's not interesting). Clearly the biggest impact is seen at ±3V V_g with a 17 percent increase/decrease seen in the output. This is because the device is nearing pinch-off, the channel is being depleted, and the 2DEG density is most sensitive to changes in V_g near this voltage.

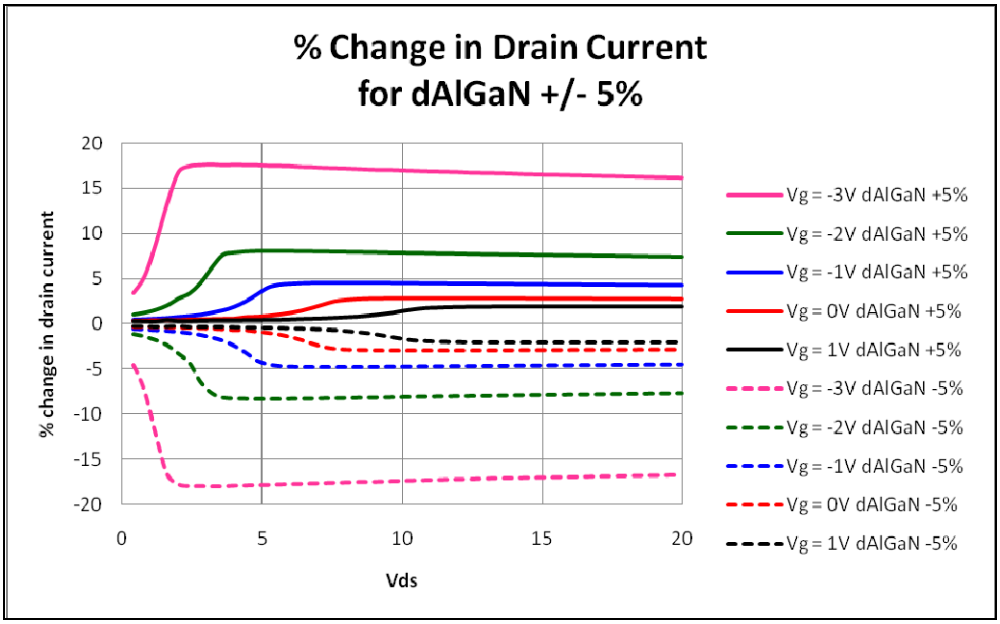

Figure 66: Percent change in simulated I-V data relative to the nominal case for varying d_{AlGaN} at as a function of V_g from -3 to 1V. For example, there is a 17% increase in I_d at V_g=-3V and V_{ds}= 5V.

Figure 67 is a comparison plot of simulated g_m versus V_g at V_{ds} = 28V for ±5% d_{AlGaN}. There is a moderate impact seen as a higher d_{AlGaN} results in a lower V_{gmp} due to the thicker barrier which requires an increased electric field, and more negative V_g, to reach v_{sat} which is where g_{mmax} is found [5, 26, 33]. Figure 68 is a plot of the percent change of $|S_{21}|$ relative to the nominal model over the frequency range of 1-26 GHz. This type of plot was chosen because the small variation in $|S_{21}|$ is not perceptible on a typical polar plot. Changing d_{AlGaN} changes results between a 0.5 and 2% change over the full frequency range. Thicker d_{AlGaN} creates a larger separation between the gate and the channel, resulting in a lower C_{gs} which translates into improved RF performance as shown in Figure 68. Thinner barriers are also associated with RF current slump as well which reduces output current gain at high frequencies [33]

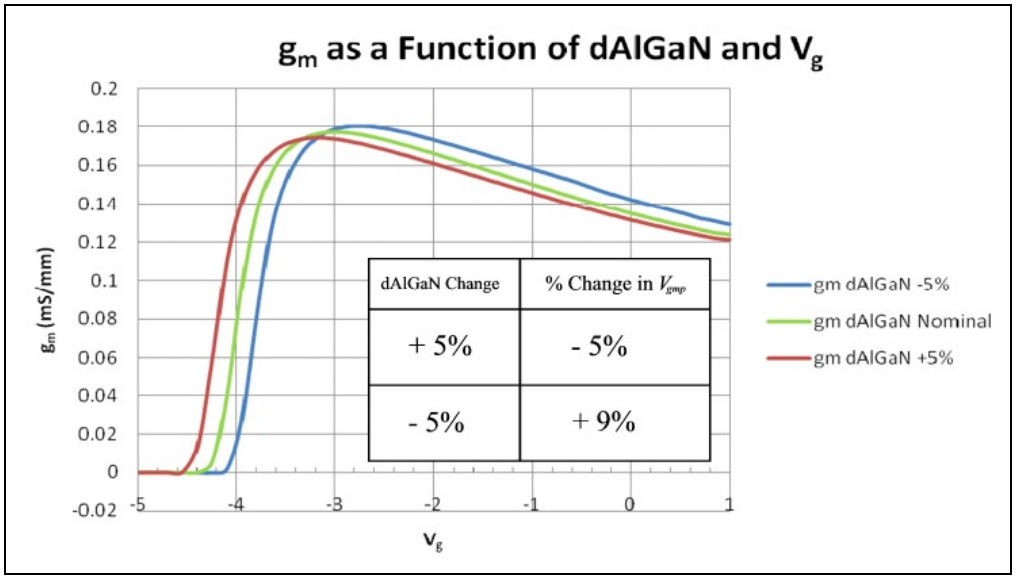

Figure 67: Simulated g_m plot for $d_{AlGaN} \pm 5\%$. As d_{AlGaN} decreases V_{gmp} increases moderately while higher d_{AlGaN} makes V_{gmp} moderately more negative.

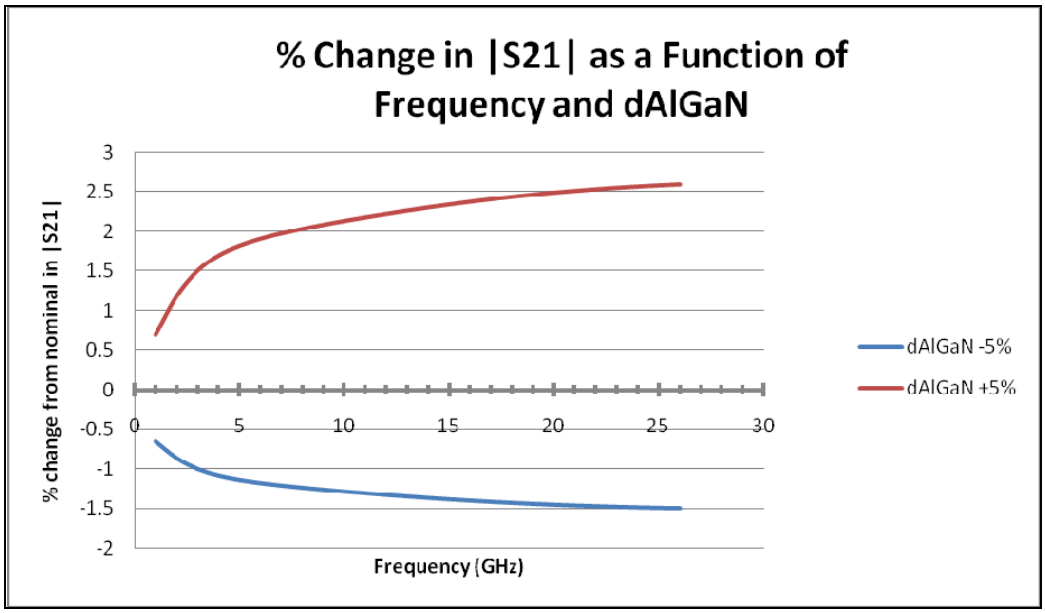

Figure 68: Percent change in $|S_{21}|$ as a function of frequency and d_{AlGaN} with $V_g = V_{gmp}$. The impact of the d_{AlGaN} variation is small overall but trends as expected due to the change in the gate to source capacitance resulting from the change in d_{AlGaN}.

Overall, changing the barrier thickness by ±5% only has a small effect on the RF performance of a device with this geometry. The greatest impact is seen in the DC performance near pinch-off.

4.5.2 Gate Length (L_g)

Figure 69 is a comparison plot of the I-V curves of the nominal device, the device with +5% L_g and the device with -5% L_g. V_g was swept from -4V to 1V and V_{ds} was swept from 0V to 20V. Changing L_g has a moderate effect on the DC output of this device. This makes sense because changing L_g has no effect on the number of carriers in the channel which has the most direct effect on I_{ds}.

Figure 70 shows the percent change in the output current at each combination of V_g and V_{ds} for the ±5% change in L_g (-4V V_g is not shown because it is so close to pinch-off that it's not interesting). This presents a clearer picture of the impact of L_g on I_{ds} than Figure 69. For smaller L_g, I_{ds} increases and, conversely for larger L_g, I_d decreases. This is because the resistance across the channel beneath the gate changes inversely to L_g but it is only a small change which is why the change in I_{ds} is equally small. The percent change flattens out at V_{dssat} due to the fact that I_{ds} is not dependent on L_g when in saturation [3].

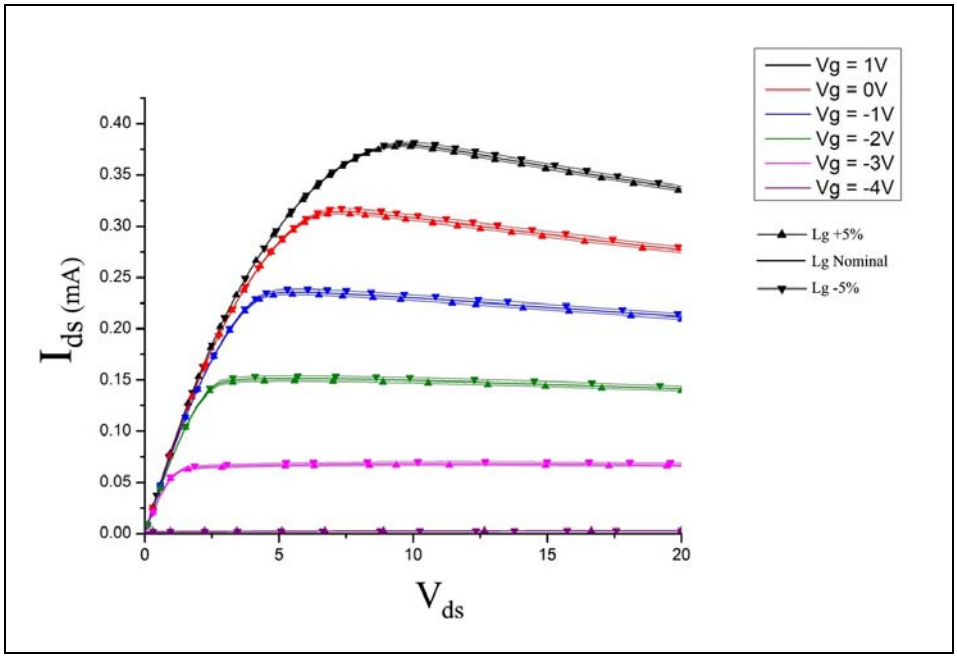

Figure 69: Simulated I-V curve comparison plots for $L_g \pm 5\%$. The change in I_d is small.

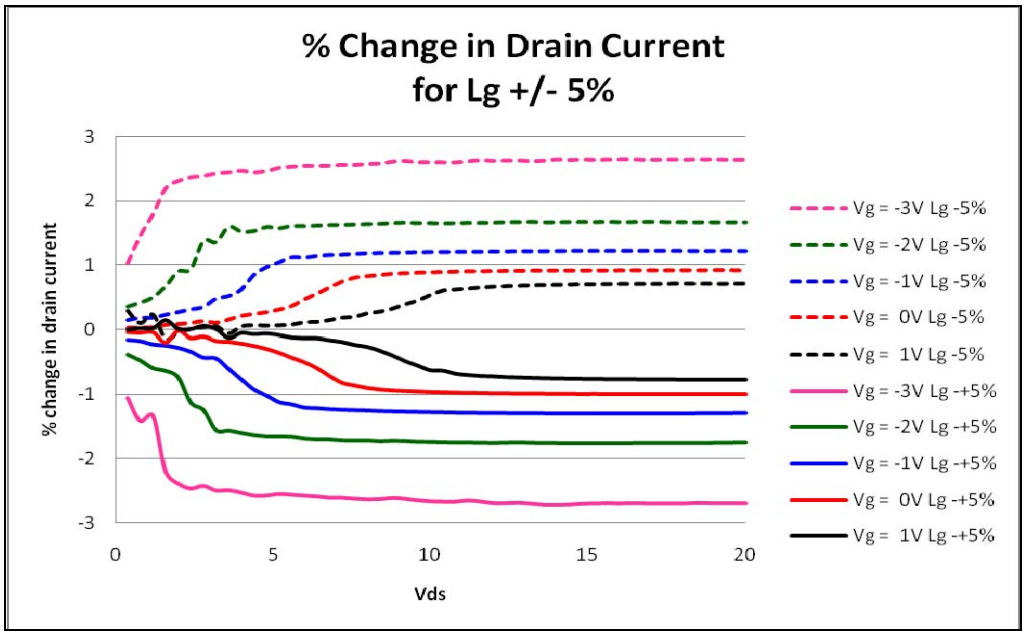

Figure 70: Percent change in I_d relative to nominal I_d for varying $L_g \pm 5\%$. at V_g=-3 to 1V. The change ranges from small to moderate but does behave as expected with I_d inversely proportional to L_g

Figure 71 is a comparison plot of g_m over V_g simulated at V_{ds} = 28V for ±5% variation in L_g. Though the impact is slight, g_{mmax} does trend as expected with a higher L_g, which increases channel length, resulting in a lower g_{mmax} due to its dependence on I_{ds}, which decreases with larger L_g [3]. V_{gmp} does not change for variance in L_g.

Finally, Figure 72 is a plot of the percent change of $|S_{21}|$ relative to the nominal model over the frequency range of 1-26 GHz. The effect of changing L_g is moderate for this device geometry, showing between a 1 and 2% change over the most of the frequency sweep. The trends behave as expected as $|S_{21}|$ is inversely proportional to L_g. The difference is greatest at the higher frequencies due to the increased/decreased carrier transit time across the channel.

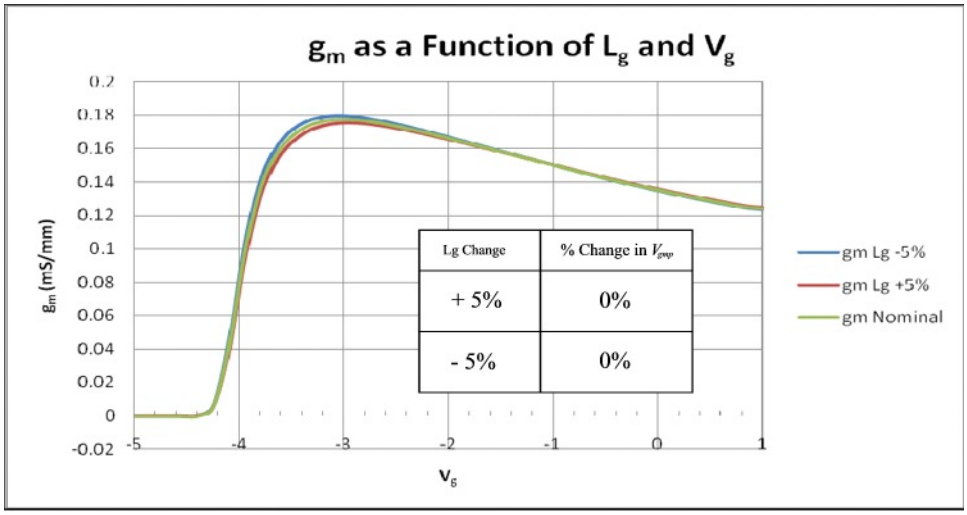

Figure 71: Simulated g_m plot for L_g ± 5%. There is negligible effect on V_{gmp} and very little effect on g_{mmax}.

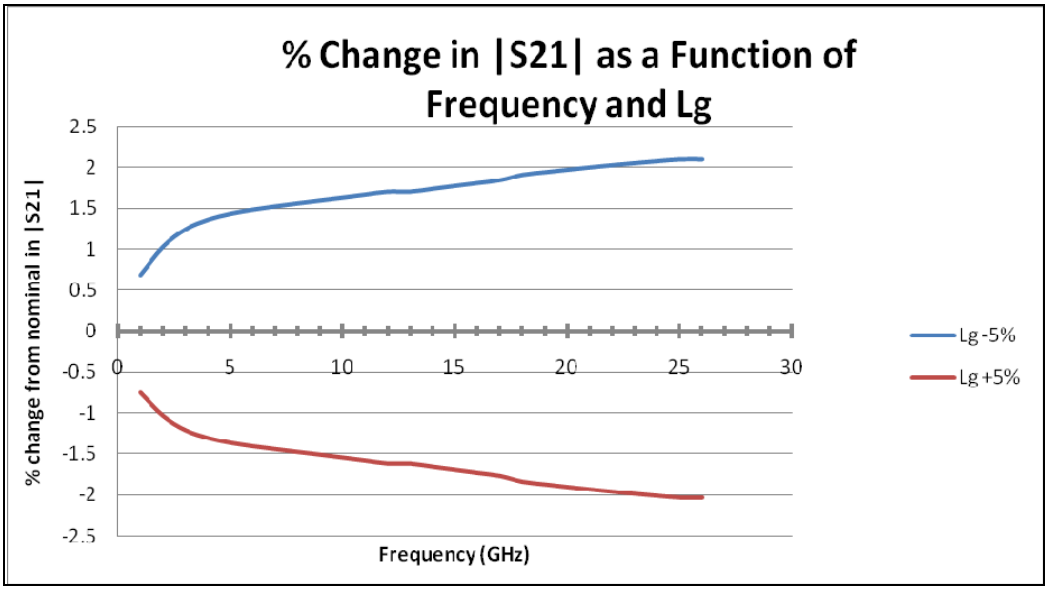

Figure 72: Percent change in $|S_{21}|$ as a function of frequency and L_g with $V_g = V_{gmp}$. The impact of the L_g variation is negligible but it does trend as expected with a shorter L_g resulting in a higher $|S_{21}|$

Overall changing L_g by 5% changes RF performance of the device by 2% or less depending on the operating frequency with this geometry while the DC performance swings by up to 40% at V_g = -3V with maximum variance seen once V_{sat} is reached.

4.5.3 Aluminum Mole Fraction (Al %)

Figure 73 is a comparison plot of the I-V curves of the nominal device, the device with +5% Al% and the device with -5% Al%. V_g was swept from -4V to 1V and V_{ds} was swept from 0V to 20V. Al% has a strong effect on the output current of this device. This makes sense due to the high dependence of n_s on Al% (refer to section 2.7 for details) which in turn creates the same dependence for I_{ds} because I_{ds} is proportional to n_s.

Figure 74 shows the percent change in the output current at each combination of V_g and V_{ds} for the ±5% change in Al% (-4V V_g is not shown because it is so close to

pinch-off that it's not interesting). There is a large impact at all V_g with varying Al% with the largest impact being at V_g = 3V.

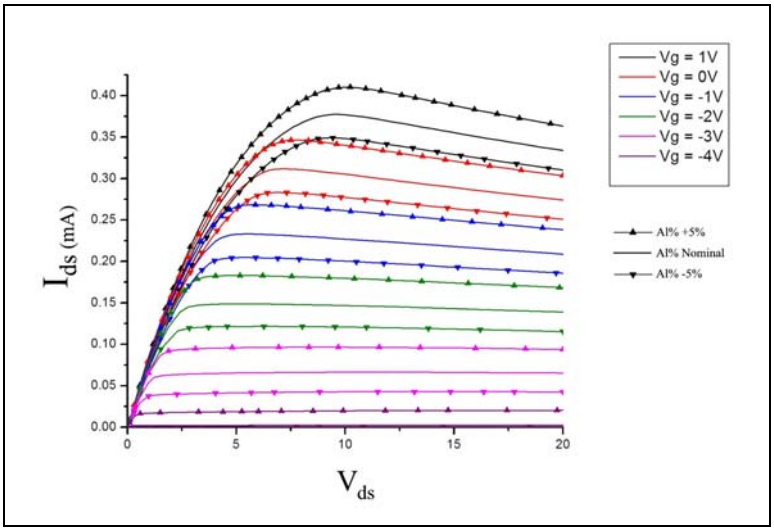

Figure 73: I-V curve comparison plots for Al% ± 5%. Increased Al% results in a large increase in the output current.

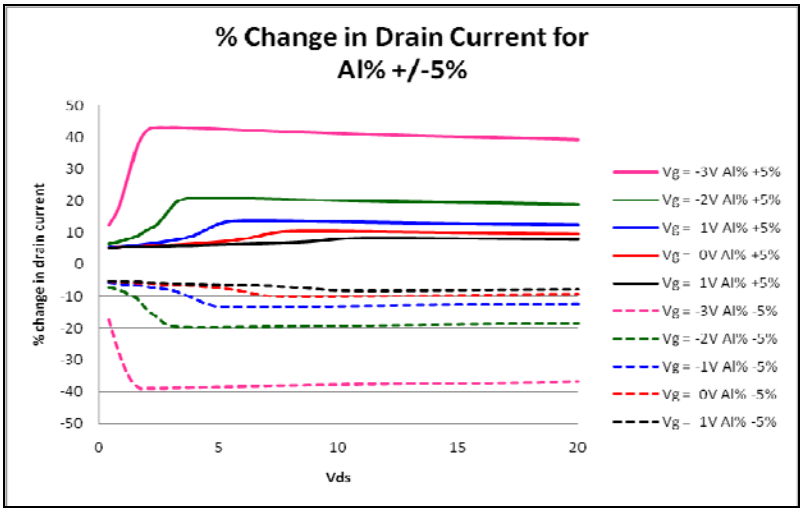

Figure 74: Percent change in I_d/V_{ds} relative to nominal for varying d_{AlGaN} at V_g=-3 to 1V. There is a substantial change in the output current at all V_g.

Figure 75 is a comparison plot of g_m over V_g simulated at V_{ds} = 28V for ±5% Al%. Al% has a larger impact on g_m than the other 2 parameters. V_{gmp} changes greatly for variance in Al% with higher Al% resulting in lower V_{gmp} and higher g_{mmax}.

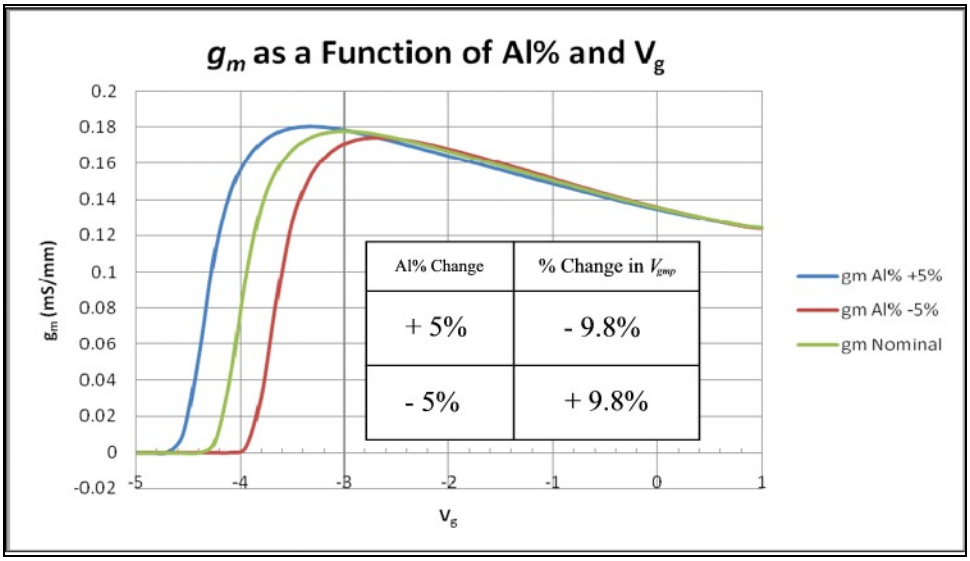

Figure 75: g_m comparison plot for Al% ± 5%. There is a large effect on g_m with g_{mmax} being proportional to Al%.

Finally, Figure 76 is a plot of the percent change of $|S_{21}|$ relative to the nominal model over the frequency range of 1-26 GHz. The effect of changing the Al% is moderate for this device geometry, showing between a 1 and 3% change over the full range of the frequency sweep. The data trends as expected, with an increase in Al% resulting in an increase in $|S_{21}|$ and a decrease in Al% resulting in a decrease in $|S_{21}|$ due to the impact of Al% on $n_{s,}$ explained in chapter 2, which greatly effects the output current of the device.

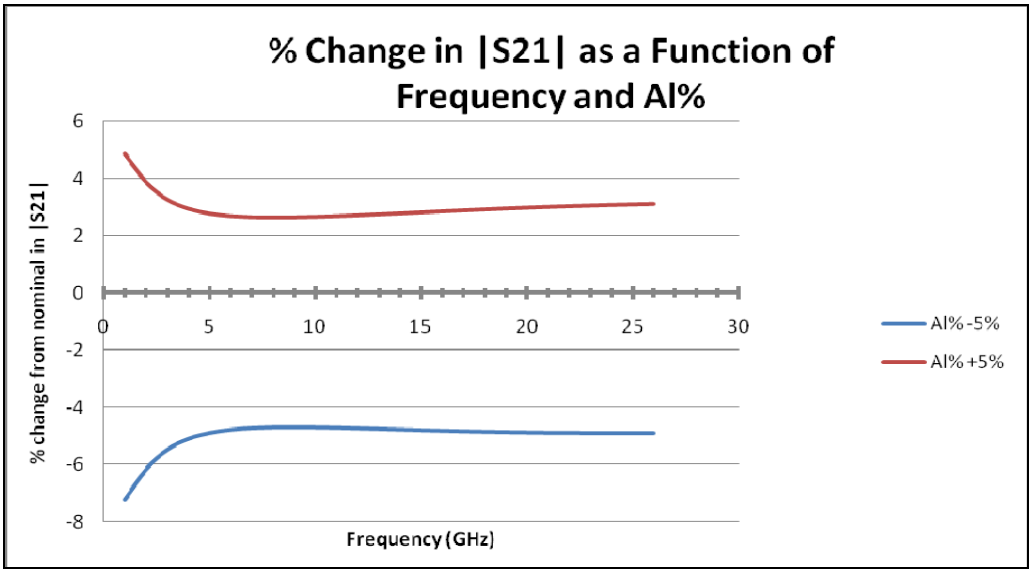

Figure 76: Percent change in $|S_{21}|$ as a function of frequency and Al% with $V_g = V_{gmp}$. Data trends as expected, with an increase in Al% resulting in an increase in $|S_{21}|$ and a decrease in Al% resulting in a decrease in $|S_{21}|$ due to the impact of Al% on n_s which greatly effects the output current of the device and therefore forward gain.

Overall changing the Al% by 5% has the greatest effect on the DC performance of all three parameters (d_{AlGaN}, Al%, and L_g). The impact on the RF performance is comparable to that of varying d_{AlGaN} and L_g though.

Table 2 summarizes the impacts on device performance due to variation of each parameter that were presented in section 4.5. A "Large" change is defined as an output change greater than 9% for a parameter change of 5% and a "Moderate" change is defined as an output change between 2 and 9% for a parameter change of 5%. A "Small" change is defined as an output change of between 0.5 and 2% for a parameter change of 5% while a "Negligible" change is less than 0.5%.

Table 2: Summary of Performance Impacts Due to Parameter Variations

Parameter	% Change	DC I-V	V_{gmp}	$\|S_{21}\|$ *1-13 GHz*	$\|S_{21}\|$ *14-26 GHz*
d_{AlGaN}	*+5%*	Large ↑	Moderate ↓	Small ↓	Small ↓
	-5%	Large ↓	Large ↑	Small ↑	Small ↑
L_g	*+5%*	Moderate ↓	Negligible	Small ↓	Moderate ↓
	-5%	Moderate ↑	Negligible	Small ↑	Moderate ↑
Al%	*+5%*	Large ↑	Large ↓	Moderate ↑	Moderate ↑
	-5%	Large ↓	Large ↑	Moderate ↓	Moderate ↓

4.6 Waferplot Comparisons

The final section of chapter 4 is a comparison of measured data collected on a different device on the same wafers with a nominal L_g of 0.98 µm. Comparing the wafer trend plots of the 0.5 µm L_g devices to those on the 0.98 µm L_g devices should offer insight into what is causing variations across the wafers. If the same trend is seen for both devices then it points to variation in the epilayers being the primary cause since epilayers are the same for both devices. If the same trend is not repeated then epilayer variation is likely not the primary cause and geometry variations should be explored.

Figure 77 compares wafer plots for I_{max} and V_{gmp}. There is strong agreement in the trends across the wafers for both devices for I_{max}. The trend loosely correlates to the trends shown for d_{AlGaN} and R_{sh} in Figure 40 and Figure 42. Where R_{sh} is at its highest, I_{max} is at its lowest which makes sense due to Ohm's law. There is no apparent correlation between variation in I_{max} and variation in n_s or μ. These trends support the conclusion that variation in I_{max} is dominated by variation in the epilayer parameters with no significant impact shown for the different geometry of the devices. There is a trend seen in V_{gmp} with the 0.9 µm devices that is not seen with the 0.5µm devices. This could

indicate the 0.5 µm device is more sensitive to variations in geometry than the 0.9 µm. Figure 78 is a comparison of the g_{mpeak} wafer plots which are inconclusive regarding the impact of geometry vs. epilayer variation.

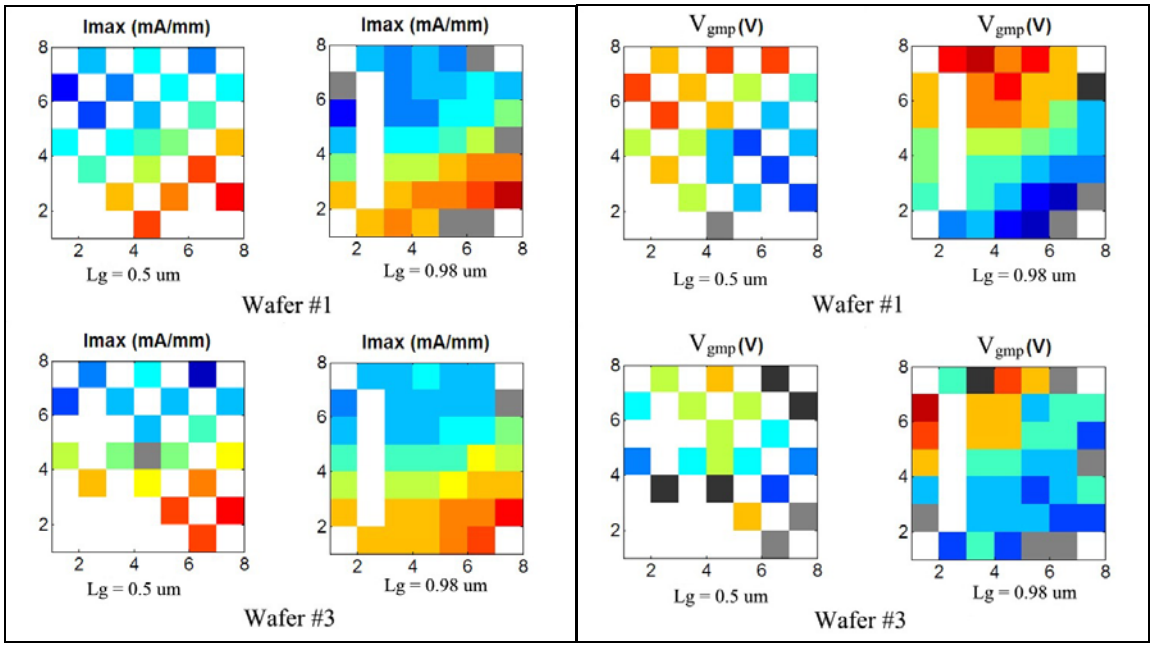

Figure 77: I_{max} wafer plots from the same wafer for L_g of 0.5 and 0.9 µm. I_{max} follows the same trends as R_{sh} and d_{AlGaN}. V_{gmp} shows a trend across the wafer 1 for both devices and the 0.9 µm on wafer 3 but not the 0.5 µm devices on wafer 3.

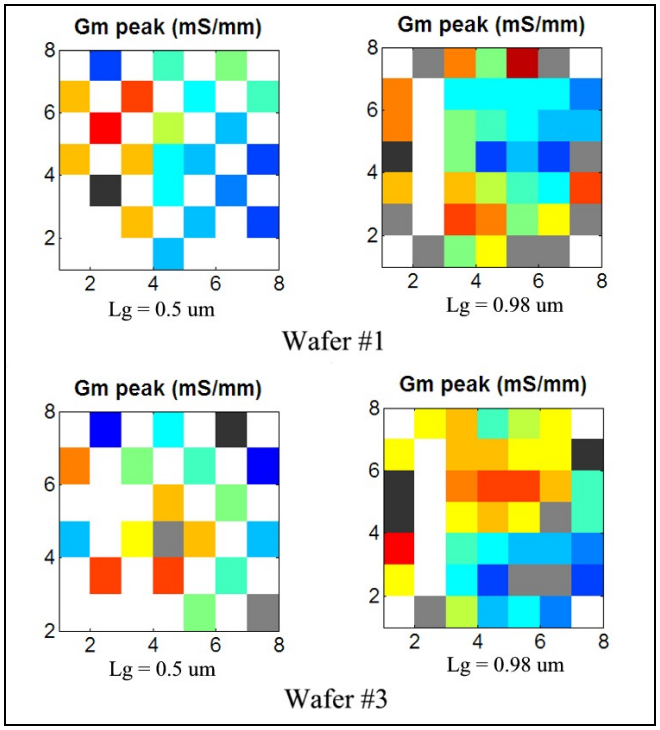

Figure 78: g_{mpeak} wafer plots from the same wafers for L_g of 0.5 and 0.9 µm. There are no significant trends and they don't track the measured variations in the epilayers from section 4.1.

Figure 79 shows the wafer plots for f_T and f_{max} for L_g = 0.5 µm and 0.9µm. f_T and f_{max} both show a strong trend for L_g of 0.9 µm that seem to correlate to the R_{sh} and d_{AlGaN} epilayer measurements. The thicker barrier and lower sheet resistance areas of the wafers correspond to the lower f_T and f_{max} regions on this device. The 0.5 µm device doesn't follow these trends at all, which can only be attributed to the differences in device geometry.

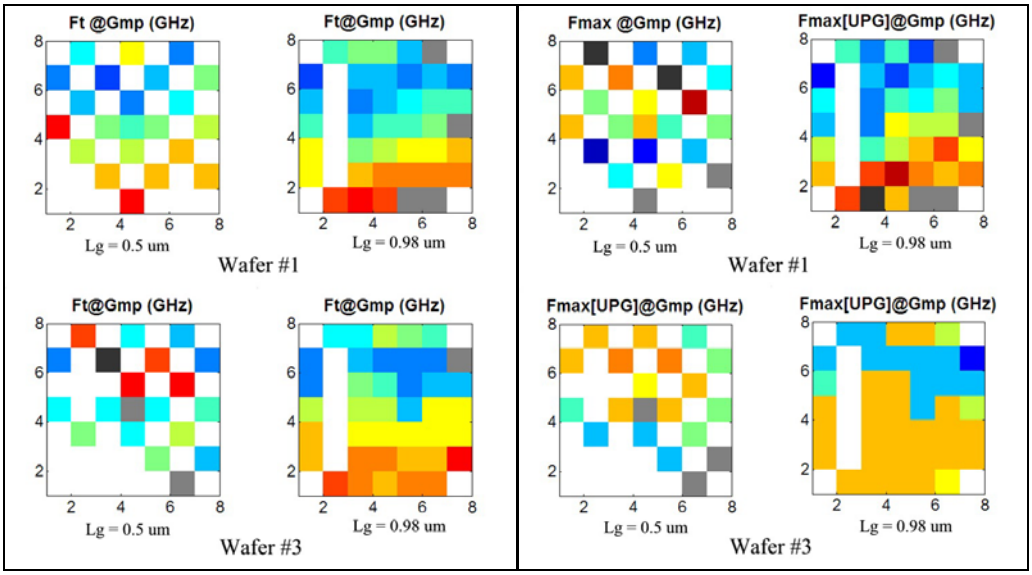

Figure 79: f_T and f_{max} wafer plots from the same wafer for L_g of 0.5 and 0.9 µm. The 0.9 µm devices show clear trends across the wafer for both f_T and f_{max} while the 0.5 µm device doesn't follow these trends. This can only be explained by the difference in device geometry.

Table 3 is a summary of the wafer plot performance data. The arrows represent the trend across the wafer in the direction of an increase in performance data. For example, ↘ indicates data that increases from the upper left to the lower right regions.

Table 3: Summary of Wafer Plot Performance Data Trends

Wafer #	Device	I_{max}	V_{gmp}	g_{mpeak}	f_T	f_{max}
Wafer 1	*Lg = 0.5µm*	↘	↖	No Trend	No Trend	No Trend
	Lg = 0.9 µm	↘	↖	No Trend	↘	↘
Wafer 3	*Lg = 0.5µm*	↘	No Trend	No Trend	No Trend	No Trend
	Lg = 0.9 µm	↘	↖	↖	↘	↘

4.7 Chapter Summary

This chapter presented all of the data collected over the course of the research for this thesis. First, cross-wafer epilayer variation and measured device performance was

shown. Next, the TCAD model that was used was presented and closely inspected to ensure that it behaved properly based on the physics of the device structure which was followed by validation of the performance of the simulated device through comparison to the measured data. Once performance was shown to be accurate, three device parameters, d_{AlGaN}, L_g and Al%, were varied individually by ±5% and the simulated data was presented and analyzed. Finally, wafer performance plots for a device with a nominal L_g of 0.9 μm were compared to the wafer plots for the 0.5 μm devices and epilayer contour plots to attribute performance trends to geometry or epilayer variation.

5. Conclusions and Recommendations

5.1 Research Summary

Key device performance parameters are susceptible to variation in the wafer growth and device fabrication processes. The goal of this thesis was to determine the impact of variations in 3 of the key parameters of an AlGaN/GaN HEMT: 1) d_{AlGaN}, 2) Al% and 3) L_g on final device performance.

Supporting concepts were discussed in chapter 2 starting with the RF figures of merit which are used to determine device performance at high frequencies followed by a discussion on the basics of heterostructure and HEMT device physics in which the key take-away from that section was that the sheet carrier density (n_s) and channel mobility (μ) are key device characteristics to consider when designing a HEMT. Next, the AlGaN/GaN HEMT structure was presented along with GaN material characteristics. GaN is proven to be well suited for high power / high frequency applications due to its high breakdown voltage and high saturation velocity. An analytical method was explored for determining polarization induced n_s as a function of Al% and d_{AlGaN} for an undoped AlGaN/GaN heterostructure. It was shown that an AlGaN/GaN heterojunction forms a 2DEG with an n_s upwards of 10^{12} cm^2 for undoped structures. Finally, the MOCVD growth process for AlGaN/GaN wafers were discussed in detail with the chapter closing out on the difficulties of working with GaN.

The thesis methodology was covered in chapter 3 beginning with descriptions of the wafers used for the experimental data followed by the performance data acquisition technique used at AFRL/RYDD to collect the DC and RF measurements. The TCAD

software package was described with a brief explanation of some of the key equations (Poissons, continuity equations etc…) that are solved by the simulator to determine device behavior. The device model was discussed including a detailed breakdown of key pieces of the Sentaurus Device simulation file. Finally, the method used to compare the simulated data across varied parameters was discussed.

Chapter 4 presented all of the data that was collected for this thesis. First, key pieces of wafer epilayer data was presented on all wafers with some parameters (d_{AlGaN} and R_{sh}) showing trends across the wafers while others (n_s and μ) did not. Wafer plots of the available DC and RF data were shown and correlated to the wafer epilayer data where possible. Next, the behavior of the TCAD model was explored in detail and validated using the measured data in order to prove that it is representative of the experimental device. DC and RF simulation results from the variation of the parameters of interest were compared and contrasted. It was found that a ± 5% variation in any of the 3 parameters individually did not significantly impact the RF performance of this particular device structure. Al% and d_{AlGaN} variance had a significant impact on the DC performance of the device though. Finally, a comparison was made between the cross wafer performance of the L_g = 0.5 μm nominal device and a device with a nominal L_g = 0.9 μm from the same wafers. This comparison allowed us to attribute performance variations across the wafer to epilayer variation or device geometry variation.

5.2 Conclusions of Research

The simulations showed the effects of varying the individual parameters for the L_g = 0.5 μm device. Varying the Al% had the most pronounced effect on the DC output

of the device with over a 40% variance in the output around V_{gmp} of -3V. Al% also had the largest effect on V_{gmp}. Varying d_{AlGaN} had a significant effect on the DC performance of the device near V_{gmp} as well, though the effect on g_m was not as pronounced. Finally, varying L_g had a moderate effect on both the DC performance and a negligible effect on g_m. Surprisingly, none of these parameters showed a large effect on the simulated $|S_{21}|$ of this device. This is supported by the measured data which shows very consistent S-parameters across each wafer.

There is a definite difference in the variance seen across the wafer plots for the 2 devices. The measured data showed more consistent trends in variation across the wafer for the nominal L_g = 0.9 µm device than the 0.5 µm L_g. This is likely attributed to more than just the change in nominal L_g *T*hese devices have other differences including larger source to drain spacing on the smaller 0.5 µm device as well as a much larger field plate to increase the breakdown voltage. This results in a very high gate capacitance that may over power the other reactances within the device causing the measured S-parameters to only show minimal variance across the wafer. Unfortunately, due to time constraints a TCAD model was not developed to simulate the L_g = 0.9 µm device to test this theory.

Based on the simulated and measured data, it was determined that the 3 key parameters studied in this research are insufficient on their own to explain the variance in performance across a single wafer. L_g varies negligibly across single wafers as measured by AFRL/RYDD so, at least for these devices, L_g can be ruled out as a significant contributing factor to performance variance. Although the Al% simulations showed significant impacts on the DC performance of the simulated device the provided epidata

only provides the Al% at 3 distinct points on each wafer which prevents me from attributing any cross wafer trends to variation in Al% with any certainty. Finally, variance in d_{AlGaN} epidata trends closely with several of the wafer plots for the 0.9 µm device, but unfortunately they do not trend close enough to the 0.5µm wafer plots to be able attribute measured variations in those devices directly to d_{AlGaN}.

5.3 Recommendations for Future Research

There are several areas for future research resulting from this study. The first area would be to develop a more robust TCAD model that could readily accept a wider range of parameter variations. The current model is very rigid and can only handle variations over limited ranges for the few parameters that were addressed in this research. A more robust model would readily allow variation of other layers and geometries and would be useful for investigating the effect of multiple parameter variations at the same time, which would be more true to life because an actual device has variations in many different parameters. Other parameters that may be of interest are variations in the SiN passivation layer, GaN cap layer, source/gate/drain spacing, and variations in the design of the field plate.

A more ambitious follow-on project would be to use Sentaurus Ligament and Sentaurus Process to model the actual fabrication process for this AlGaN/GaN HEMT. Ligament would be used for designing mask layouts and setting up the fabrication process while Process would be used for simulating the actual fabrication. This would require a complete rebuild of the device model because the current model is built using discrete points in Structure Editor, bypassing Sentaurus Process all together, thereby not

needing any sort of mask design or fabrication process definitions. With GaN still being a relatively new material this would require substantial work due to the fact that the built in process data in TCAD is mostly for Si and GaAs and would require the researcher to create process data from scratch or data from epilayer growers and in-house or industry fabrication processes.

In addition, a future researcher could take a complete AlGaN/GaN HEMT TCAD model and export the final device into a SPICE circuit simulation to investigate the system level impacts of variations in these devices. These simulation results could be compared to actual measured circuit performance when available.

Bibliography

1. Trew, R.J., et al., *Microwave AlGaN/GaN HFETs.* Microwave Magazine, IEEE. **6**(1): p. 56-66 2005

2. Golio, J.M., *RF and Microwave Semiconductor Device Handbook*, Boca Raton, Fla.: CRC Press 2003.

3. Neamen, D.A., *Semiconductor Physics and Devices : Basic Principles*, Boston: McGraw-Hill. 746 2003.

4. Sze, S.M., *Semiconductor Devices : Physics and Technology*, New York: Wiley. 564 2002.

5. Schwierz, F. and J.J. Liou, *Modern Microwave Transistors : Theory, Design, and Performance*, Hoboken, N.J.: Wiley-Interscience. 486 2003.

6. Shen, L., et al. *Improved High Power Thick-GaN-Capped AlGaN/GaN HEMTs without Surface Passivation*. in *Device Research Conference, 2004. 62nd DRC. Conference Digest*

7. Schwierz, F. and O. Ambacher. *Recent Advances in GaN HEMT Development*. in *IEEE Conference Proceedings*. 2003.

8. Trew, R.J. *Microwave Power Amplifiers Fabricated from Wide Bandgap Semiconductor Transistors*.

9. Sze, S.M. and K.K. Ng, *Physics of Semiconductor Devices*, Hoboken, NJ: Wiley-Interscience. 815 2007.

10. Office of Naval Research,. *NSR Naval Semiconductor Research Website* http://www.onr.navy.mil/sci_tech/31/312/ncsr/materials/ 8 Feb 2008

11. Ambacher, O., et al., *Two-Dimensional Electron Gases Induced by Spontaneous and Piezoelectric Polarization Charges in N- and Ga-face AlGaN/GaN Heterostructures*. AIP. p. 3222-3233 1999.

12. Levinshteĭn, M.E., S.L. Rumyantsev, and M. Shur, *Properties of Advanced Semiconductor Materials : GaN, AlN, InN, BN, SiC, SiGe*, New York: Wiley. 194 2001.

13. Ambacher, O., et al., *Two Dimensional Electron Gases Induced by Spontaneous and Piezoelectric Polarization in Undoped and Doped AlGaN/GaN Heterostructures.* Journal of Applied Physics. **87**(1): p. 334-344 2000

14. Coleman, J.J., *Metalorganic Chemical Vapor Deposition for Optoelectronic Devices.* Proceedings of the IEEE. **85**(11): p. 1715-1729 1997

15. *http://www.esa.int/techresources/* 8 Feb 2008

16. Stringfellow, G.B., *Organometallic Vapor-Phase Epitaxy : Theory and Practice*, San Diego: Academic Press. 572 1999.

17. *www.hlphys.jku.at/fkphys/epitaxy/mocvd_fig2.jpg* 8 Feb 2008

18. Pearton, S.J., *GaN and Related Materials II*. Optoelectronic Properties of Semiconductors and Superlattices., Australia: Gordon and Breach Science Publishers. 698 2000.

19. Edgar, J.H., *Properties, Processing and Applications of Gallium Nitride and Related Semiconductors*. EMIS datareviews series ; no.23, London: INSPEC. xxiii, 656 1999.

20. Gaffney, M.S., et al. *Improved Composition and Thickness Control of III-V Epitaxy in a Metalorganic Chemical Vapor Deposition Process*. in *Decision and Control, 1995., Proceedings of the 34th IEEE Conference on*. 1995.

21. Trew, R.J., *Wide Bandgap Semiconductor Transistors for Microwave Power Amplifiers.* Microwave Magazine, IEEE. **1**(1): p. 46-54 2000

22. Newey, J., *Perfect Substrate within Reach for Wide-Bandgap Materials*, in *Compound Semiconductor* 2002.

23. Shuo, J., et al., *AlGaN-GaN HEMTs on Patterned Silicon (111) Substrate.* Electron Device Letters, IEEE. **26**(3): p. 130-132 2005

24. Sood, A.K., et al. *Growth and Characterization of AlGaN/GaN Epitaxial Layers by MOCVD on SiC Substrates for RF Device Applications*. 2006. San Jose, CA, United States: International Society for Optical Engineering, Bellingham WA

25. Miyoshi, M., T. Egawa, and H. Ishikawa, *Structural Characterization of Strained AlGaN Layers in Different Al Content AlGaN/GaN Heterostructures and its Effect on Two-Dimensional Electron Transport Properties.* Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures. **23**(4): p. 1527-1531 2005

26. Faraclas, E., et al. *Dependence of RF performance of GaN/AlGaN HEMTs upon AlGaN Barrier Layer Variation*. 2004.

27. Langley, D., *AlGaN/GaN HEMT Topology Investigation Using Measured Data and Device Modeling*, Graduate Thesis, Wright State University, Dayton Ohio, 2007.

28. Cascade Microtech, *http://www.cascademicrotech.com/go/engineering-products-division/product-portfolio/probe-stations/* 8 Feb 2008

29. Synopsys. *Sentaurus TCAD Tutorial* August 2007.

30. Heller, Eric, *Sentaurus TCAD Code. AFRL/RYDD.* June 2007.

31. Synopsys. *Synopsys TCAD Sentaurus Device User's Manual* August 2007.

32. Synopsys. *Synopsys TCAD Technology Template: DC and RF Characterization of HEMTs* August 2007.

33. Tilak, V., et al., *Influence of barrier thickness on the high-power performance of AlGaN/GaN HEMTs.* Electron Device Letters, IEEE. **22**(11): p. 504-506 2001

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14. ABSTRACT A sensitivity analysis of AlGaN/GaN HEMT performance on material and process variations was performed. Aluminum mole fraction, barrier thickness, and gate length were varied ± 5% over nominal values to determine how sensitive simulated device performance was to changes in these 3 parameters. Simulated data was generated with the Synopsys TCAD software suite using a physics-based HEMT model. To validate model performance, simulated data was correlated with experimental data, which consisted of wafer epilayer characterization data as well as DC and small-signal RF device performance data from 1-26 GHz.Trends were observed in the experimental data due to variations in the fabrication process. Epilayer data showed cross-wafer trends in sheet resistance, barrier thickness and Al mole fraction but didn't show any discernable trends in mobility or sheet carrier concentration. Maximum output current was the only measured performance metric that showed a strong trend across the wafers. Data from two different device geometries on the same wafers were compared to determine whether performance variations across a wafer could be attributed to epilayer variation or device geometry. Variation in power and current gain cutoff frequencies was attributed to differences in the device geometry whereas variations in maximum output current was correlated to sheet resistance and barrier thickness variation.Simulated device performance showed varying sensitivities when ± 5% changes in aluminum mole fraction, barrier thickness, and gate length were made. Al mole fraction and barrier thickness had a large effect on DC output up to 40%, while the gate length only moderately effected DC output by 2-3%. However, of all 3 parameters, changes in gate length had the greatest effect on the RF performance (1-3%) while RF performance was negligibly affected by changes in Al mole fraction and barrier thickness. Although varying these three parameters affects device performance, variation in these three parameters alone is insufficient to accurately account for variations in measured device performance.

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