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Nonvolatile reprogrammable logic elements using hybrid resonant tunneling diode-giant magnetoresistance circuits

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We have combined resonant interband tunneling diodes (RITDs) with giant magnetoresistance (GMR) elements so that the GMR element controls the switching current and stable operating voltage points of the hybrid circuit. Parallel and series combinations demonstrate continuous or two-state tunability of the subsequent RITD-like current-voltage characteristic via the magnetic field response of the GMR element. Monostable-bistable transition logic element operation is demonstrated with a GMR/RITD circuit in both the dc limit and clocked operation. The output of such hybrid circuits is nonvolatile, reprogrammable, and multivalued. © 2001 American Institute of Physics. [DOI: 10.1063/1.1395523]

Logic devices and gate arrays that are both reprogrammable and tunable are becoming increasingly important in digital logic systems. Field programmable gate arrays (FPGAs) are now being produced in volume because they more easily handle changing design requirements and result in a faster time to market. The resonant tunneling diode (RTD) is an especially attractive device component for such applications because it offers high frequency, low power operation which is derived from its negative differential resistance (NDR) operating characteristic. Memory, multivalue logic and monostable—bistable logic elements (MOBILEs) can be constructed using relatively simple, low component count circuits which combine RTDs and field-effect transistors (FETs). However, these circuits do not retain their state indefinitely upon loss of power.

In contrast, magnetic devices based on giant magnetoresistance (GMR) or tunneling magnetoresistance (TMR) are inherently nonvolatile, since the state of the device is stored as the magnetic orientation of a particular layer which is retained upon power cycling. This characteristic makes such elements extremely attractive for computer random access memory applications, and provides fast, reliable data storage while simultaneously guarding against data loss. Successfully combining the high speed, low power operation of RTDs with GMR or TMR elements will enable hybrid device circuits that have the critical advantage of nonvolatile operation. Potential examples include reprogrammable logic cells and FPGAs for digital signal processing, and multiple-valued logic and memory cells in which the logic or memory levels can be tuned in a nonvolatile manner.

In this letter, we demonstrate the feasibility of this approach by showing that the critical parameters of RTDs can be adjusted over a useful range in simple GMR/RTD hybrid device circuits. The more complicated MOBILE structure⁴ is implemented in both the dc limit and with clocked operation. These prototype hybrid circuits prove the functionality and illustrate the utility of such devices.

A standard RTD is a two-terminal device based on a

double barrier quantum well heterostructure, whose *IV* characteristic is determined by resonant tunneling of conduction electrons through confined conduction band states in the well. A resonant interband tunneling diode (RITD) is a type of RTD that is distinguished by tunneling through valence band rather than conduction band well states. The RITD used in this study was grown by molecular beam epitaxy, and consisted of a pair of InAs electrodes, a pair of 15 Å thick AlSb barriers, and an 82 Å GaSb well. *IV* curves for typical devices are shown in Fig. 1(a). At low bias voltage, the device appears ohmic as electrons near the Fermi level in the InAs emitter tunnel through resonant states in the GaSb quantum well. With increasing bias, this resonant alignment

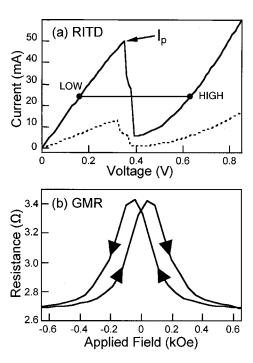


FIG. 1. (a) Typical IV data for the 10 (dotted line) and 20 μ m (solid line) diam RITDs used. The structure in the NDR regime is typical for this material system. A pair of high and low voltage, or logic, states, and the peak current, I_p , are indicated. (b) Resistance vs applied field for the Cu/Co GMR used. The offset of the curves is a manifestation of hysteresis in the system.

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is lost, and the current through the device actually decreases, producing a NDR regime. At higher voltages, the device again appears ohmic. When employed in circuits, the device is biased at either of two stable operating points on the ohmic portions of the curve, corresponding to the logic "low" and "high" voltages (see Fig. 1). The device switches rapidly across the NDR regime when a current greater than the critical peak current, I_p , is applied. The basic parameters that determine the operation of the device in a circuit are I_n , and the voltage values corresponding to the low and high logic levels. Photolithographically defined RITD mesas 5–50 μm in diameter exhibited switching currents of 10-100 mA, with peak current densities of 1.4×10^4 A/cm² and a peak-tovalley ratio of ~ 10 .

The GMR elements used here are 40-period Co/Cu multilayers sputter deposited onto silicon with layer thicknesses of 10 and 21 Å, respectively. The Cu layer thickness is chosen to correspond to the second peak in this antiferromagnetically exchange coupled system. 9 By applying current in plane (CIP) at 300 K, the resistance (R) can be varied smoothly with the magnetic field to a maximum $\Delta R/R$ =28% at 500 Oe, as shown in Fig. 1(b).

The processed RITD and GMR elements were independently mounted on a chip carrier and wire bonded to form a variety of test circuits. IV data were taken at 300 K by applying a fixed voltage and measuring the current of the system. Magnetic fields were applied perpendicular to the GMR film plane (easy axis) using either an air coil or an electromagnet.

Using a GMR element in series or parallel with a RITD results in a hybrid device circuit with a IV that is similar to that of a RITD, but one that can be tuned or programmed in a nonvolatile fashion. We first illustrate how the effective IV characteristics of the RITD-GMR devices can be tuned, and then demonstrate clocked operation of a magnetic MOBILE cell.

The IV characteristics for typical RITDs shown in Fig. 1(a) exhibit peak currents of 13 and 50 mA, respectively. Both RITDs "switch" from a high to low current state near 0.35 V. Figure 2(a) shows IV data for a hybrid circuit consisting of a 20 µm RITD in series with a GMR element [Fig. 2(a) inset], with the GMR in a high (17 Ω , solid line) and low (14 Ω , dashed line) resistance state. The voltage at which the RITD-GMR combination switches changes by up to 0.25 V. Note that the stable operating voltage points on the positive differential resistance portions of the curve are shifted by a similar amount, thereby defining a new pair of states with potential for multivalue logic or memory applications. In fact, this circuit provides the same functionality with a reduced component count as some proposed multiplestate static random access memory (SRAM) devices. 10 Because the resistance of the exchange-coupled GMR element employed here can be tuned continuously between its maximum and minimum, the peak switching value can be tuned continuously as well. Alternatively, the use of a spin-valve type element would provide two distinct, nonvolatile operating curves.

The utility of being able to tune the circuit IV characteristics becomes immediately obvious when the output voltage of the RITD-GMR series circuit is examined [Fig. 2(b)]. If Downloaded 31 Aug 2001 to 132.250.134.159. Redistribution subject to AIP license or copyright, see http://ojps.aip.org/aplo/aplcr.jsp

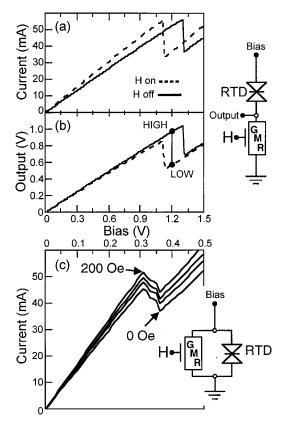


FIG. 2. (a) IV data for a RITD-GMR series circuit (schematic shown at right) with (dotted line) and without (solid line) applied magnetic field. (b) Output voltage vs applied voltage of the series combination shown in (a). High and low voltage state at a bias voltage of 1.2 V are indicated. (c) A series of IV data from a RITD-GMR parallel circuit (schematic inset) taken as a function of applied field.

the bias voltage is chosen correctly, there are two output voltages determined by the state of the GMR element. In this example the output voltage has two possible states at a bias of 1.2 V, depending on the state of the GMR: in one case (low), the RITD has "switched;" in the other case it has not. By varying the input, nonvolatile output voltages differing by 0.4 V are achieved.

In similar fashion, the current that is required before the RITD switches can also be tuned. A parallel RITD-GMR circuit [Fig. 2(c) inset] allows continuous control of the effective switching current by utilizing the GMR as a by-pass element. This is the basic function (normally provided by a pass transistor) necessary to implement the MOBILE cell discussed below. As more current is shunted through the GMR element, the net current going through the circuit required to switch the RITD increases monotonically by ~20% without changing the voltage of the NDR peak. The use of a spin-valve type element again would provide two stable, nonvolatile operating curves.

A recent proposal for a highly functional RTD-based logic cell utilizes two RTDs of different diameter connected in series, with a FET connected parallel to the smaller area one.⁵ This cell, called a MOBILE, is shown schematically in Fig. 3 (inset). In operation, the smaller RTD switches at a lower current because the size of the RTD determines the current at which it switches. The "input" for this circuit is the FET gate voltage. With the FET "OFF" (nonconducting), the lower (smaller) RTD determines the switching current

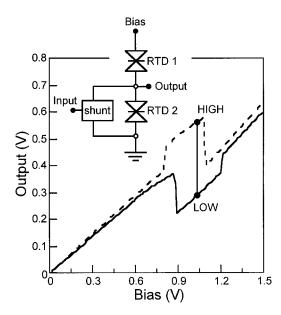


FIG. 3. Output voltage of hybrid MOBILE vs applied voltage. High and low voltage states are indicated for a bias voltage of 1.0 V. The inset shows a generic schematic of the MOBILE circuit. The current shunt can be either a FET or GMR element.

and output voltage of the MOBILE, while the larger RTD is effectively a resistor since it does not reach peak current. The output of the logic cell is changed by turning the FET "ON" (conducting), providing a current shunt around the smaller RTD. Now the upper (larger) RTD is able to reach its peak current first to switch, and thus controls the output of the cell. Note that this cell logic is *volatile* because the FET reverts to its "normally off" state upon loss of power.

A nonvolatile logic cell with the same cell functionality and component count is achieved by replacing the FET with a GMR element. A hybrid MOBILE cell was fabricated using two RITDs with diameters of 10 and 20 μ m, and a GMR element, also shown in Fig. 3 (inset). Now the "input" is an applied magnetic field. In its high resistance state, the GMR element is OFF and current flows through the lower RITD, which then controls the logic state of the cell. When the GMR element is switched with a magnetic field into its low resistance state (turned ON), it shunts current for the lower RITD so that the upper (larger) RITD can now reach its critical current, and thus controls the output of the cell. Figure 3 shows the output voltage of the magnetic MOBILE circuit, with (dashed line) and without (solid line) applied field, as a function of applied bias. In this example, the voltage difference between the high and low levels is 0.3 V. The output state is dependent on which RITD has switched, an event that can be controlled in a nonvolatile way by the GMR element through the application of a magnetic field.

Such MOBILE elements are normally intended to operate in a clocked circuit⁵ in which an ac bias voltage synchronizes the response of an array of such elements. Clocked operation of our hybrid MOBILE circuit is shown in Fig. 4 using 20 and 25 μ m diam RITDs and a GMR element with a resistance that is switched between 4 and 5 Ω . The circuit was run with a 1.2 V, 1 kHz clock signal, and the magnetic

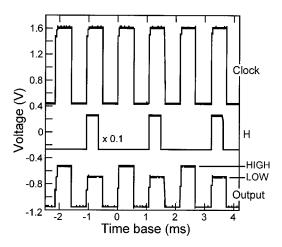


FIG. 4. (b) Clocked operation of MOBILE, showing clock, magnetic field input, and output voltage traces. The traces are offset for clarity.

field was pulsed to 230 Oe using an air coil. The top trace in Fig. 4 is the clock voltage and the bottom trace is the output voltage of the cell. The middle trace is the voltage driving the air coil power supply at half the frequency of the clock signal, i.e., an input is applied at alternate clock pulses. With no input, the smaller (lower) RITD switches and determines the output, which tracks the clock signal. When an input pulse is applied to decrease the GMR resistance, the upper RITD is allowed to switch, and the output of the cell toggles to a lower voltage corresponding to the logic low, inverting the clock signal. Thus the output of the cell is controlled by the magnetic field input, and exhibits well-defined high and low voltage (logic) levels. Note further that the input pulse is shorter than the output, i.e., the output "latches," a valuable characteristic of the MOBILE design.⁴ Although we have used an exchange coupled GMR element here to illustrate the principles of operation, it is clear that a spin-valve type structure would provide a true nonvolatile input.

In summary, GMR elements can be used to control and tune the critical parameters of the RTD operating characteristic and associated voltage (logic) levels in both steady state and clocked operation. While the components used here were not optimized for speed or power, these prototypes show that such hybrid device circuits provide nonvolatile operation to the existing attributes of RTD-based circuits.

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¹T. Whitaker, Compound. Semicond. 1, 36 (1998).

²C. Ajluni, Electron. Design **48**, (2000).

³P. Mazumder, S. Kulkarni, M. Bhattacharya, J. P. Sun, and G. I. Haddad, Proc. IEEE **86**, 664 (1998), and references therein.

⁴K. Maezawa and T. Mizutani, Jpn. J. Appl. Phys., Part 2 32, L42 (1993).

⁵ K. J. Chen, T. Akeyoshi, and K. Maezawa, Jpn. J. Appl. Phys., Part 1 **34**, 1199 (1995).

⁶J. M. Daughton, J. Magn. Magn. Mater. **192**, 334 (1999).

⁷L. L. Chang, L. Esaki, and R. Tsu, Appl. Phys. Lett. **24**, 593 (1974).

⁸J. R. Söderström, E. R. Brown, C. D. Parker, L. J. Mahoney, J. Y. Yao, T. G. Andersson, and T. C. McGill, Appl. Phys. Lett. 58, 275 (1991).

⁹S. S. P. Parkin, R. Bhadra, and K. P. Roche, Phys. Rev. Lett. **66**, 2152 (1991).

¹⁰M.-H. Shieh and H. C. Lin, IEEE J. Solid-State Circuits **29**, 623 (1994).