Q2 Known Good Substrates Technical Report
CONTRACT/PR NO. N00014-07-C-0918 Dow Corning Corporation
Quarterly Technical Report
Reporting Period: 1 Dec 2007 – 29 Feb 2008

Executive Summary

At the end of this quarter the majority of epiwafer deliveries scheduled for the program were completed. The delay in these deliveries leaves the program about 10 weeks behind schedule. Epiwafer defects where significantly reduced with new process alterations, bringing the epitaxy added defect density near the end of program objective. Reduction of MPD in n+ 4H-SiC continues on track, but there is difficulty to reduce resistivity to the range of program goals, primarily due to ingot cracks. LLS testing continues to develop and now offers what may be the first fully automated full quality area wafer inspection test that covers the entire wafer area.

Technical Progress

The following table documents the key program end metric goals.

Metric	50th Percentile	20th Percentile
MPD distribution 4H n+ 76 mm diameter (cm^{-2})	10	5
MPD distribution 4H n+ 100 mm diameter (cm^{-2})	20	10
Net scratch length by LLS relative to wafer diameter (%)	40	20
Equivalent Epitaxy Defect Density 76 mm diameter (cm^{-2})	<10	<5
Epitaxy Doping Target Accuracy	+/- 25%	+/-10%
Epitaxy Doping Variation within wafer (Max-Min/Min, %)	35%	10%
Substrate Resistivity Maximum 4H n+ 76mm	0.025	0.020

Progress Against Metrics

The following charts show early progress against the program metrics. Due to extended processing cycles, data tends to become available 4-6 weeks in the rears.

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14. ABSTRACT
The Known Good Substrates (KGS) Phase II program was initiated 29 August 2007. Wafer, epitaxy, modeling and metrology work has been the main focus of efforts in Q2. This technical report summarizes the progress by all team members against the tasks and milestones.

15. SUBJECT TERMS
SiC wafer, SiC epitaxy, SiC material metrology

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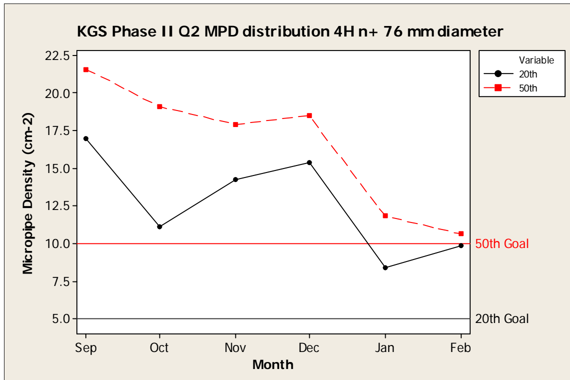
KGS Phase II Q2 MPD distribution 4H n+ 76 mm diameter
Micropipe Density (cm-2)
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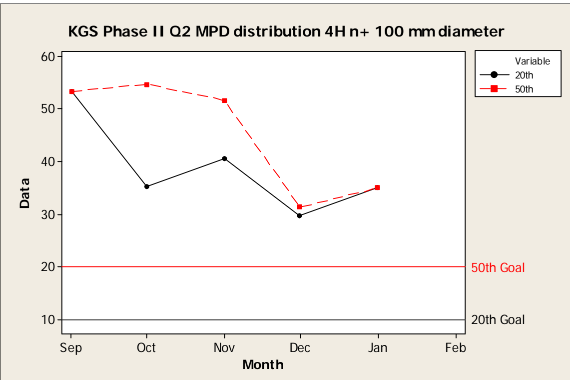
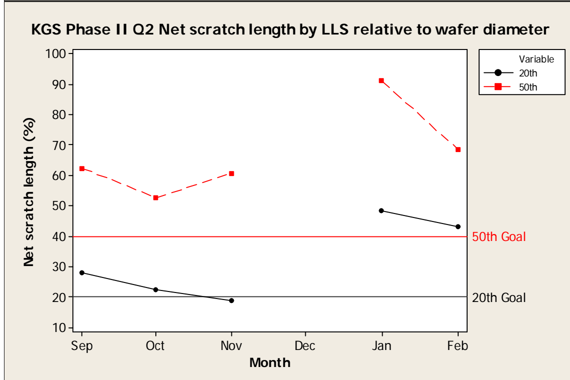
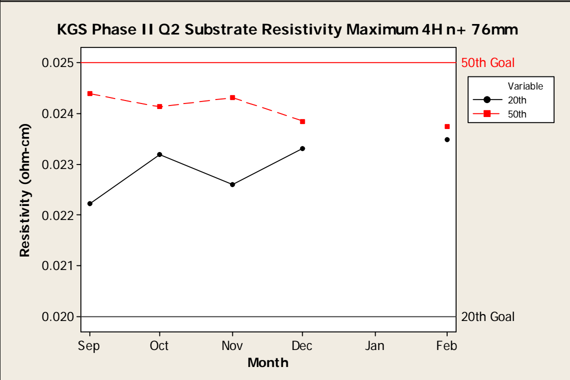

KGS Phase II Q2 MPD distribution 4H n+ 100 mm diameter
Data
Variable
20th
50th
50th Goal
20th Goal
Sep
Oct
Nov
Dec
Jan
Feb
Month


KGS Phase II Q2 Net scratch length by LLS relative to wafer diameter
Net scratch length (%)
Variable
20th
50th
50th Goal
20th Goal
Sep
Oct
Nov
Dec
Jan
Feb
Month


KGS Phase II Q2 Substrate Resistivity Maximum 4H n+ 76mm
Resistivity (ohm-cm)
50th Goal
Variable
20th
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20th Goal
Sep
Oct
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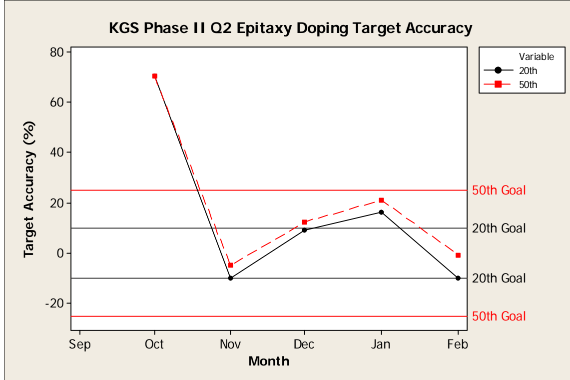
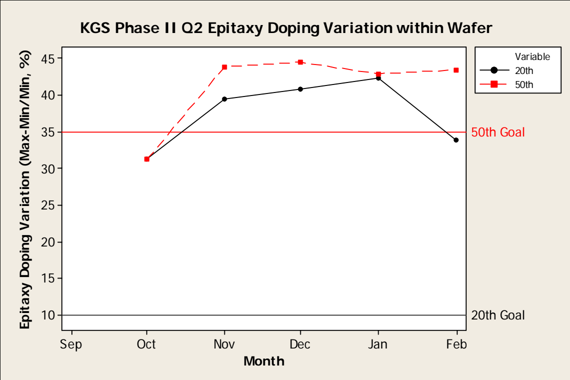
Month


KGS Phase II Q2 Epitaxy Doping Target Accuracy
Target Accuracy (%)
Variable
20th
50th
50th Goal
20th Goal
20th Goal
50th Goal
Sep
Oct
Nov
Dec
Jan
Feb
Month


KGS Phase II Q2 Epitaxy Doping Variation within Wafer
Epitaxy Doping Variation (Max-Min/Min, %)
Variable
20th
50th
50th Goal
20th Goal
Sep
Oct
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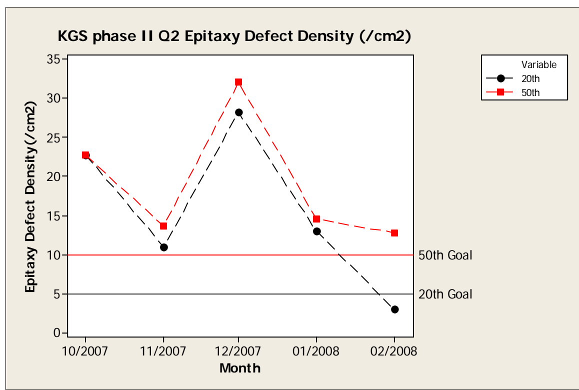
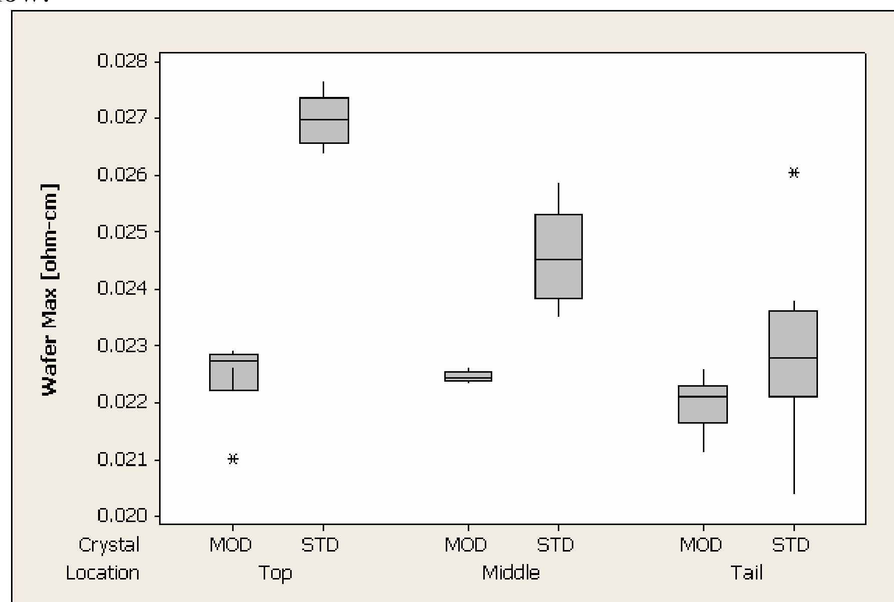

KGS phase II Q2 Epitaxy Defect Density (/cm2)
Epitaxy Defect Density(/cm2)
Variable
20th
50th
50th Goal
20th Goal
10/2007
11/2007
12/2007
01/2008
02/2008
Month

Details by task follow:

Task 1: SiC Wafers Products

Highlights:

- Advancements in PVT growth methodology based on improvements developed in Q1 continues to deliver reduction in MPD for 76mm n+ 4H materials month by month; MPD value tracking close to the 50th percentile goal value, with a tight distribution around 11/cm2. These improvements are generally realized through tight control of seed quality and tight control of reaction cell insulation.
- Improvements in control of thermal gradients, thermal budget, and annealing appear to continue to reduce crystal stress. Breakage of 100mm crystals is reduced and subsequently crystal yields in 100 mm 4Hn+ materials are improving. Wafer slices are now accumulating for the first batch polishing trials which should begin in May 2008.
- In-wafer maximum resistivity has been very stable and tracking within the 50th percentile goal. Experiments this quarter, focused on alteration of the source chemistry, via adjustment of the source morphology, prove to be a route to reduce the resistivity towards the 20th percentile goal. This is illustrated in the figure below:



The figure displays the resistivity ranges obtained for the top, middle, and seed end (tail) thirds of two 4H n+ SiC boules. The crystals were grown under identical conditions with exception of the source. The crystal grown with the modified source (MOD) shows consistently lower resistivity and lower within crystal variation.

- Epitaxial wafers have been manufactured to specification and shipped to contract partners, including GeneSiC, MicroSemi, NRL, and ASU, for device fabrication and testing. Shipments were completed in early March, data will be included in the next report.

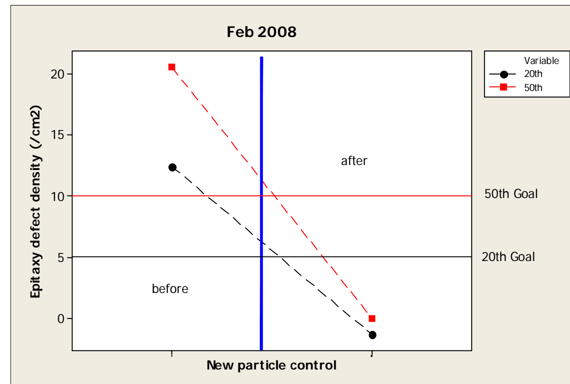
Roadblocks: (Red text are roadblocks from previous report)

- Pinhole problems in crystal growths during Sept limited material available for use in program. Supply of wafers into epitaxy for KGS projects is about 6-8 weeks behind schedule. Wafers stock is now replenishing and epitaxy growths for delivery of wafers to subs will begin in late December. *In Q2 of the program the process line produced the epitaxy wafers needed for subcontractor projects. These wafers show improvements in MPD and epitaxy defects compared to Phase I KGS deliverables. The epiwafers were shipped in late Q2-early Q3 as noted above. But due to these delays the program remains near 10 weeks behind schedule. Discussions with Microsemi indicate that they should be able to complete their work by year end; NGES hopefully by end of February 2008. NRL and university projects should be completed by end of 2008. These delays will be reviewed with the program manager, and may require an extension of the program completion date*.
- Highly N_2 doped 4H SiC materials manufactured to meet the 20th percentile resistivity goal continue to have low crystal yields due to cracking during ingot fabrication.
- Scratch defects are above goal. Rework of polished parts from Q1 has successfully reduced scratches (new Q1 values are below what was presented in the last report).
- Excessive epitaxial related defects in the first part of Q2 limited the ability to produce epitaxial wafers for subcontractors. However improvements in Q2 have greatly reduced this problem.

Task 2: Continuous Improvements in SiC Substrates

Highlights

- Improvements in the epitaxial growth process have resulted in lower particle formation which has significantly reduced defects in the epitaxy layer. This has allowed for epitaxial wafer with high predicted device yields to be produced and delivered to contractors. The figure below shows the distinct change obtained via SiC epitaxy process alterations. The equivalent Poisson-type defect density associated with defects added to the substrate during epitaxy was significantly reduced with the process alterations.



- A new induction heating source arrangement for PVT crystal growth furnaces has been designed and modeled electrically and by crystal growth simulation. The prototype is being fabricated to confirm electrical model results. The PVT simulation model results show the new heating arrangement is much less sensitive to reaction cell effects compared to the existing heater.
- UID 4H-SiC material have shown >1e6 ohm-cm resistivity at T=250 C by I-V measurements, along with consistent purity analysis by SIMS and LTPL spectra obtained from NRL.

Roadblocks

- While consistently low N and B levels are found in DCCSS 4H undoped SiC, levels consistent with semi-insulating SiC, material yields to electrical specifications vary significantly. Support from partners will be used to see if the variations can be traced to inconsistent concentrations of deep level impurities. Additional testing shows that the temperature dependent resistivity measured by I-V testing shows semi-insulating character (T>1E6 ohm-cm at 250 C and activation energy ~0.6 eV for the resistivity vs. temperature curve 50-250 C), LTPL shows semi-insulating character, yet microwave loss and COREMA have indicate low resistivity results. Samples have been sent out for additional testing using Hall Effect and DLTS.

Task 3: Metrology for Wafer Specifications.

Highlights

- LLS device yield prediction has been applied to bare and epitaxy wafers grown in 2007 and 2008 to gain a large statistical dataset of defect performance. The test detects micropipes, polishing defects, and defects resulting from epitaxial growth. It offers better screening of incoming bare wafers and is a simple test to identify additional defects added during epitaxy. By separating the wafer into sites of size common to SiC devices, the LLS test can be used to get the first true full quality area test for SiC substrates where >95% of the wafer area is inspected.

- Dominant range of epitaxy defect size has been identified through LLS and microscopic images confirm that small embedded particles are dominant epitaxy defect. Typical size range of defects detected by LLS is 10 um and greater.

Task 4: Device Technology Maturation

Highlights

- Two possible hypotheses, stacking fault (SF) formation and field enhanced generation, have been suggested to explain large generation lifetime variation in MOS structure. CL and EBIC tests have been performed to understand influence of SF on generation lifetime variation and no correlation between generation lifetime and SF has been observed. DLTS and various field analyses, however, support field enhanced generation for large generation lifetime variation.
- Oxidation impact on Schottky surface has been investigated. Oxidized surface show lower SBH and higher ideality factor than fresh Schottky surface. Oxidation induced defect generation and carbon rich layer formation are possible origins of the observations.

Roadblocks

- Majority of wafer shipments to major device contractors (Microsemi, GeneSiC, NGES) were completed in late Q2/Early Q3. The delays in shipping wafers have put the program about 10 weeks behind schedule.
-

Progress toward Milestones for End of Program (Sub-bullets are progress this quarter)

- Correlation Maps of PiN forward IV characteristics and recombination lifetime
- Correlation of PiN forward IV characteristics and n+ epitaxial buffer layer/MP blocking
- Primary SiC material defect limiting PiN performance (Roadmap input - GeneSiC)
    - Epiwafers in device fabrication are complete to ohmic contact formation
- SiC materials parameter assessed as most important for SIT performance improvements based on wafer probe data (Roadmap input - NGES)
    - Wafers shipped early March – more data next report.
- SiC materials parameter assessed as most important for SBD performance improvements based on wafer probe data (Roadmap input - Microsemi)
    - 14 pieces shipped to Microsemi in early March.
- Generational improvement of 4H SiC wafer crystal quality summarized by XRT and MPD analysis
    - Growths in progress
- Assessment of oxide quality for 76mm/100mm 4H epiwafers and link to generation lifetime
    - Epiwafers shipped to NRL and ASU in Late Q2.

Schedule

Program device fabrication work is at 8 weeks behind schedule.

Program Management

All subcontractors were under contact by end of January 2008.

Appendix 1: KGS Subcontractors and Quarterly Progress Points

Subcontractor	Area of Focus	Progress This Quarter
Northrup Grumman Electronics Systems	J-SIT fabrication and testing	Epiwafers delivered in early March
Microsemi	SBD fabrication and testing	Epiwafers delivered in early March
GeneSiC Semiconductors	PiN diode fabrication and testing	First two lots of PiN diode wafers have been fabricated through topside ohmic contact step. Next 3 lots have entered device fab.
SUNY – Stoney Brook	Crystal Structure of SiC	See progress below
Arizona State University	SiC Oxides, carrier lifetime and device failure analysis	Completing generation lifetime and SBD tests on delivered samples. (Dr. Schroder) 1 SBD epi wafer delivered. (Dr. Skromme)
Fluxtrol	Modeling and design of high uniformity induction heating systems	New coil design has been modeled and prototype is fabricated. Now testing prototype to confirm model results. PVT growth simulations using power density model results from new coil show reduced.
NRL	SiC Oxides, Epitaxy, Lifetime testing, materials testing, device testing	LT-IR-PL shows deep centers like UD1,2 and 3 on 4H UID samples. CL, EBIC and DLTS have been employed to understand lifetime. 1 SBD and 2 MOS epi wafers delivered.
STR	Modeling of CVD and PVT SiC Growth Processes	Simulations of induction coil skew effect show that this property can lead to

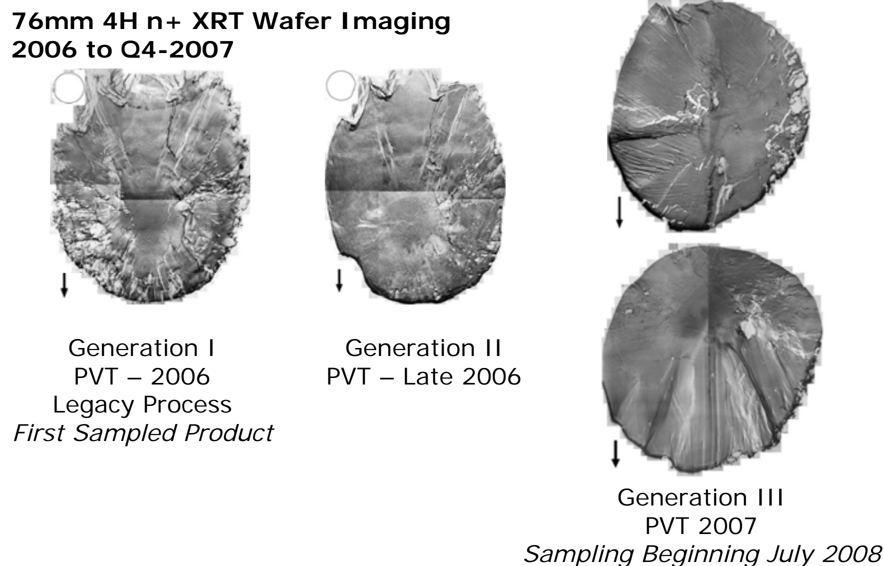
		significant local spatial variations in growth environment, and furnace to furnace variations due to small coil mount differences.

Progress in XRT testing at SUNY (Prof. M. Dudley)

Evaluation of DCCSS Advanced PVT SiC Crystal Growth Process

Dow Corning CSS has been working to develop an advanced PVT SiC growth method in order to reduce crystal defects to the level of its primary competitors. In Q1 this process was able to produce several crystals with MPD<10/cm2. Wafers from these crystals were delivered with epitaxy to Microsemi in early March 2008, where they will be compared to legacy DCCSS wafers from 2007 in an SBD process flow.

In Q1 and Q2 of the KGS program wafers of several iterations of the PVT process were sampled to SUNY for XRT imaging and the results are shown in the figure below. The "advanced process" is defined in the figure as Generation-III.



There are several striking differences. In the Gen III growth the crystal deformation is reduced considerably, evidenced by the more circular/rounder form compared to the Gen I and Gen II crystals. The Gen-III image is smoother to the eye as well. In this Si-face scan the white clumps that dominate half of the Gen I boule are not visible at all in the Gen III process. These white clumps are micropipe clusters. The Gen III process of reducing micropipes has significantly improved the crystal quality. The final difference is in the number of grain boundaries. White and dark radial lines are the trade mark of grain boundaries. There are fewer of these in the Gen III process. As the Gen-III crystals are grown using seeds from the Gen I type method, it is apparent from the XRT data that

this advanced PVT process can help to close the gap in materials performance between DCCSS and the established suppliers of SiC.

Publications

Comparison of 4H-SiC MOS capacitors and Schottky diodes
- M.J. Marinella, D.K. Schroder, G.Y. Chung, M.J. Loboda, T. Isaacs-Smith, and J.R. Williams – ONR Approval 43-065-08
  - Submitted to Electronic Material Conference at Santa Barbara, 2008