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**SCALABLE SiC POWER SWITCHES  
FOR APPLICATIONS IN MORE  
ELECTRIC VEHICLES (PREPRINT)**



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<b>14. ABSTRACT</b> SiC JFETs can be manufactured in three different conduction types; fully normally off (capable of blocking BVDS(max) at VGS = 0V), quasi-off (previously referred to as bias-enhanced capable of blocking half BVDS(max) at VGS = 0V), and 'hard' normally on (unable to block any amount of voltage at VGS = 0V). There exists trade-offs between each of the three conduction types mostly evident in the forward current ratings and specific on resistance. Due to the structure of the device the normally on device yields the greatest forward current ratings and lowest on resistance. The quasi-off device that is design to block up to half of the maximum blocking capabilities at VGS = 0, typically results in 1.5x reduction in forward current with the normally off device demonstrating greater than 2x reduction in forward current ratings. Because of the large reduction in conduction current capabilities of the normally off device, the normally on and quasi-off devices are more strongly promoted.					
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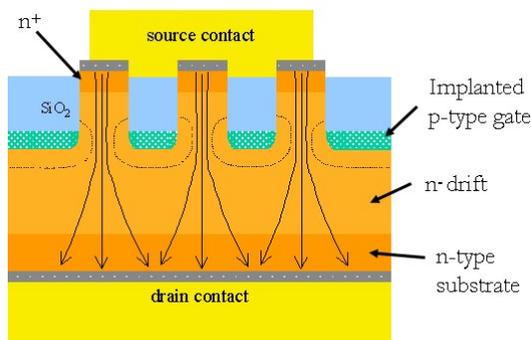
# Scalable SiC Power Switches for Applications in More Electric Vehicles

## Abstract

Silicon carbide power vertical junction field effect transistors (VJFET) are ideal candidates for next generation vehicle power conditioning systems. They combine the switching speed of MOSFETs with the voltage and current handling properties of IGBTs, and the excellent thermal properties derived from the SiC material. As a unipolar device they can be easily paralleled over the entire operating temperature range of the device. Characterization of five paralleled 3-mm<sup>2</sup> (active area) SiC VJFETs has shown excellent dc and switching performance at DC currents up to 171 A and pulsed currents up to 152 A with total switching cycle time (sum of rise and fall times) less than 150 ns. Current sharing is facilitated by a positive temperature coefficient for the on-resistance of 0.87 %/°C. These results indicate that additional paralleling of SiC VJFETs will lead to IGBT-like current handling with MOSFET-like switching performance, but with vastly improved thermal properties highly desirable for future hybrid-electric vehicles.

## I. Introduction

Perhaps the most advanced, technically ready silicon-carbide power switch is the vertical junction field effect transistor (VJFET). A substantial literature indicates that the devices are rugged,<sup>1,2</sup> capable of high-voltage operation in excess of 1.5 kV,<sup>3</sup> and do not have the gate oxide problems of other devices. This device has low specific on-resistance at 600 V and above where the best silicon MOSFETs are still five to twenty times higher. Acceptable yields occur with effective die areas similar to SiC Schottky barrier diodes (i.e., in the few mm<sup>2</sup>).



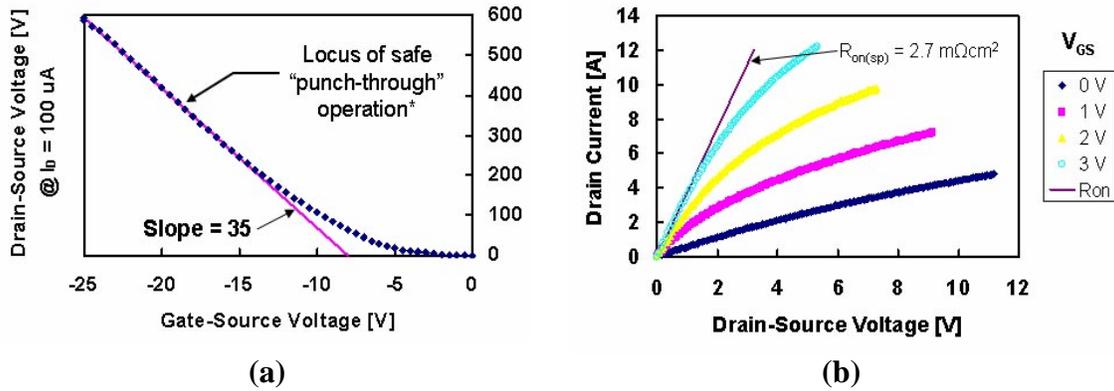
**Figure 1.** Cross section of a SemiSouth implanted-gate trench VJFET.

Individual devices can be applied to kilowatt-class single-switch power supplies requiring 5- to 10-A devices with 600-V or 1200-V ratings. But because the 4H-SiC VJFETs reported here are 100% unipolar, they can also be easily paralleled to form equivalent switches of much greater current, meaning hundreds of amperes. This means that switches with current and voltage ratings commonly used in electric vehicles are possible with currently available SiC VJFET technology. The possibility is to develop IGBT replacements that have average and surge current ratings like silicon IGBTs, switching properties like silicon MOSFETs, but lower thermal resistance and higher rated

junction temperature than available in silicon because of the thermal properties of silicon carbide. Substantial system benefits can be captured by such a development. This paper demonstrates the feasibility of massively paralleling SiC power VJFETs to develop Si IGBT replacements for use in electric vehicles.

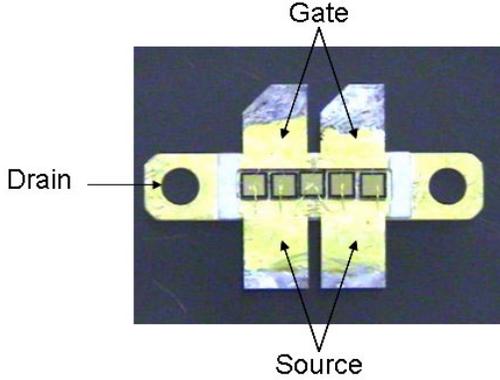
## II. Experiment

The VJFET technology is based on the implanted-gate trench VJFET illustrated in cross section in Fig. 1. Different device areas have been fabricated ranging from  $0.5 \text{ mm}^2$  to more than  $3 \text{ mm}^2$ . Two device sizes are considered in this work. One has an effective conduction area of  $1 \text{ mm}^2$  and the other has a  $3 \text{ mm}^2$  area. Figure 2 illustrates typical performance data of the  $1 \text{ mm}^2$  devices.



**Figure 2.** (a) Blocking gain of a typical normally on 4H-SiC VJFET with  $1 \text{ mm}^2$  effective area. The punch-through voltage is defined by the  $V_{DS}$  at which the drain leakage current reaches  $100 \text{ } \mu\text{A}$  at a given  $V_{GS}$ . (b) Forward characteristics of a  $1 \text{ mm}^2$  VJFET.

To examine the use of SiC devices in hybrid electric vehicle (HEV) class motor drive applications, a high current 600 V device was fabricated by bonding multiple die in parallel until a desired current rating was achieved. For this purpose, the larger  $3 \text{ mm}^2$  die were used even though they tend to exhibit slightly higher specific on resistance. Five die that individual testing showed to have similar (but not matched) properties were bonded to a standard three-terminal microwave package designed for vertical devices. The base of the package serves as the drain contact. The source and gate contacts are made by short wire bonds, thus minimizing both the total lead inductance and the asymmetry in lead inductance and resistance between the five die. The devices were wire bonded one at a time. The process began by wire bonding the first device to the package source and gate external terminals. It was then tested for quasi DC characteristics at room temperature, switching characteristics at room temperature, and finally quasi DC characteristics at  $175^\circ\text{C}$ . After all three tests were completed, the second device was added in parallel by completing the source and gate wire bonds and the measurements on the parallel combination were repeated. The process was continued until all five devices were fully wire bonded into the package and parallel connected. Figure 3 is an image of the packaged parts after completion of the testing.



**Figure 3.** Image of five 3 mm<sup>2</sup> 4H-SiC power VJFETs packaged in parallel.

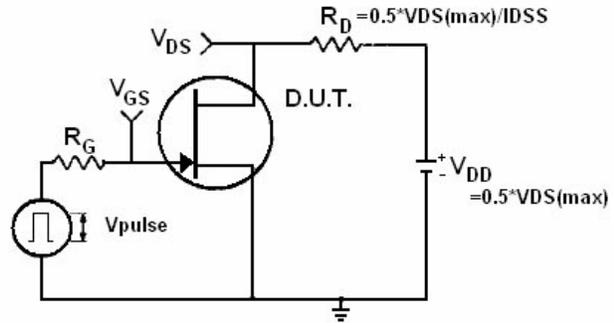
The “quasi” DC characteristics were measured with a Tektronix Model 370 curve tracer. Because of the high currents required to measure the forward characteristics, the curve tracer operated in pulsed mode. Pulsed mode uses a 100- $\mu$ s pulsewidth which, at the higher currents and drain-source voltages ( $V_{DS} > 2$  V), produces junction heating and thus a distortion in the curve. Because these unipolar devices exhibit negative temperature coefficient with respect to the current (or positive temperature coefficient with respect to the resistance) the distortion tends to underestimate the current available

at the specified temperature.

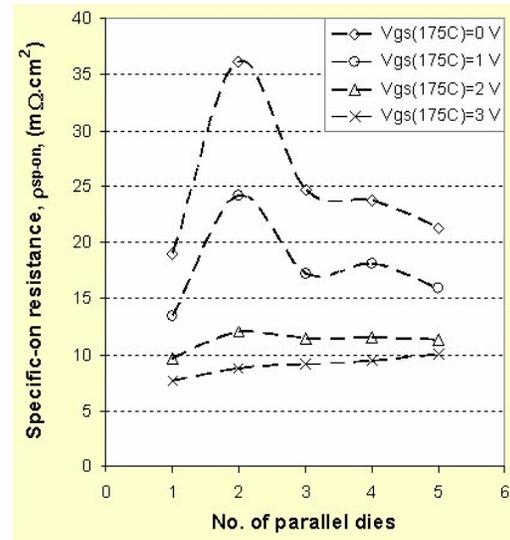
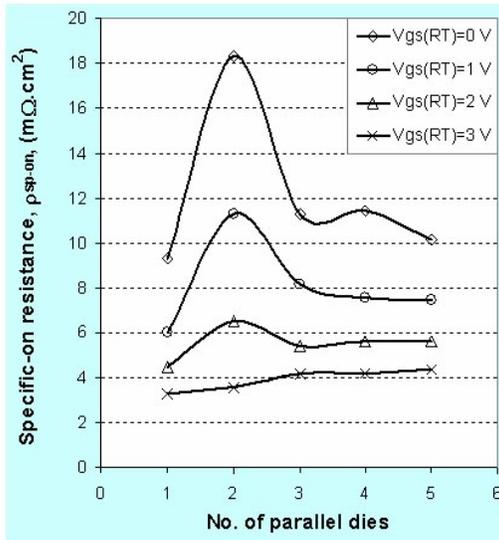
The switching characteristics were conducted according to the JEDEC standard documented in JESD24<sup>4</sup> using the circuit illustrated in Fig. 4. This standard requires that the device be tested in a low-inductance resistively loaded test circuit. The open-circuit voltage is set to 50% of the device rated blocking voltage and the short-circuit current is set to 100% of the device rated current. For all devices tested in the sequential process of paralleling described above,  $V_{oc} = 300$  V = 0.5  $V_{DS(max)}$ , where  $V_{DS(max)} = 600$  V at  $V_{GS} = -30$ V. The short-circuit current was increased when each device was added to the parallel combination by decreasing the load resistance proportionally. While all of the devices are “normally on” the minimum on resistance occurs when the gate is positively biased to the verge of gate-source diode cut on (i.e.,  $V_{GS} = 3$  V). Current was measured with a Tektronix Model current probe with waveforms displayed on a Tektronix TDS digital oscilloscope. An effort was made to reduce parasitic loop inductance so as to minimize voltage overshoot in the drain-source voltage while the VJFETs were interrupting the load current. This was largely successful, although the remaining  $Ldi/dt$  voltage spike was managed by slowing the trailing edge of the gate-source voltage pulse which had the effect of acting like a lossless snubber.

### III. Results

Figure 5 shows plots of specific on-resistance  $\rho_{sp(on)}$  extracted from the forward characteristics measured from the devices as the number of parallel die was successively increased from one through five die. Curves are given for four different values of  $V_{GS} = 0, 1, 2,$  and 3 V for room-temperature junction temperature ( $\cong 25$  °C) and  $T_j \cong 175$  °C. As expected, the  $V_{GS} = 3$  V curves uniformly produce the lowest specific on resistance. A moderate increase is observed as the number of devices in parallel increase. The curves at lower gate-source



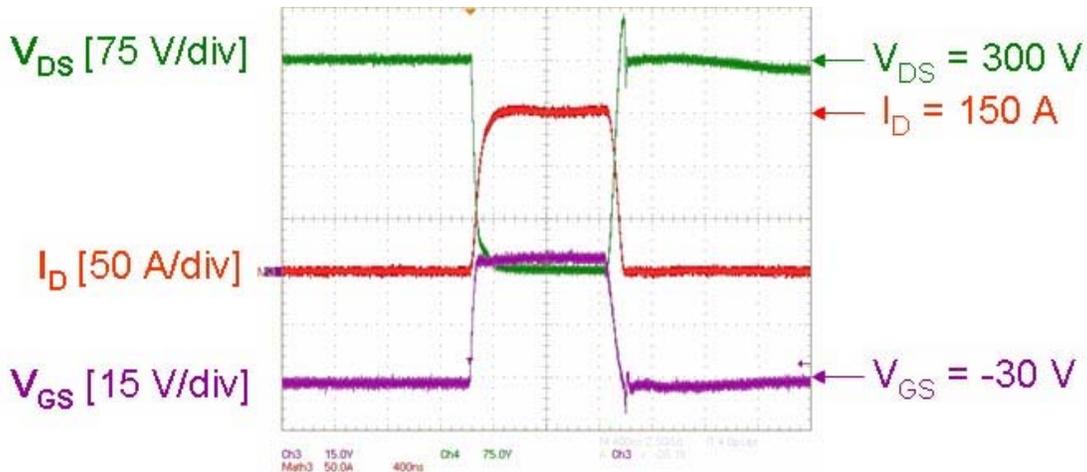
**Figure 4.** Equivalent circuit for JESD24 switching characterization of field effect transistors.



**Figure 5.** (a) Specific-on resistance vs. no. of parallel die at room temperature (25 °C). (b) Specific-on resistance vs. no. of parallel die at  $T_j \approx 175$  °C.

voltage are not as smooth, but this represents the differences in pinch-off voltage between the various devices. Under conditions other than minimum depletion that exist for  $V_{GS} < 3$  V the specific on resistance shows variations consistent with the fact that the devices are not matched. At  $T_j \approx 175$  °C the curves have similar shapes to those observed at room temperature, but the absolute value increases by more than a factor of two. This represents the reduction in mobility of the majority carriers (electrons) with temperature.<sup>5</sup> At  $V_{GS} = 3$  V, the average change in specific-on resistance,  $\Delta\rho_{sp(on)}$ , is 0.87 %/°C.

Figure 6 contains an image of oscilloscope traces recorded when all five devices



**Figure 6.** Oscilloscope traces of the drain-source voltage, drain current, and gate-source voltage during switching of the five-device parallel combination.

in parallel were tested in the circuit of Fig. 4. The drain-source voltage is 300 V until the gate-source voltage increases from -30 V to +3 V, which causes the drain-source voltage to collapse while the drain current rises. After a fall time of the  $V_{DS}$  waveform of 77 ns (the leading-edge of  $V_{GS}$  rises in 42 ns), the drain current settles to 152 A at an estimated  $V_{DS(on)} = 2.6$  V. The falling edge of  $V_{GS}$  initiates the turn-off of the paralleled VJFETs. The slopes of the trailing edges of  $I_D$  and  $V_{GS}$  are similar, but the rising edge of  $V_{DS}$  is noticeably faster (by about 30%) which suggests the influence of parasitic inductance. The 70-V overshoot in  $V_{DS}$  is further evidence of a  $L di_D/dt$  voltage induced by the fast turn-off of the transistors. The overshoot is accentuated if the trailing edge of  $V_{GS}$  is accelerated by adjustment of the gate driver. Thus the actual fall time of the current as might have been limited by the device rather than the gate driver during the transition to the blocking state is between the 65 ns measured from  $V_{DS}$  and the 93 ns measured from  $V_{GS}$ . Table I documents the results obtained as the number of parallel devices increased from one to five.

**Table I.** Summary of switching results.  $t_r$  = rise time,  $t_f$  = fall time,  $t_{d(on)}$  = turn-on delay,  $t_{d(off)}$  = turn-off delay. See Ref. 4 for complete definitions.

No. of Parallel Die	$V_{GS}$ [V]	$I_D$ [A]	$V_{DS}$ [V]	$V_{DS}$ tr [ns]	$V_{DS}$ tf [ns]	$t_{d(on)}$ [ns]	$t_{d(off)}$ [ns]	$V_{(on)}$ [V]
1	3/-30	36	300	42.0	20.0	12.8	9.6	5.0
2	3/-30	48	300	66.0	40.0	16.0	10.0	4.2
3	3/-30	88	300	96.0	40.0	10.4	12.8	3.0
4	3/-30	130	300	84.8	51.2	11.2	12.0	5.0
5	3/-30	152	300	77.6	65.6	9.6	19.2	2.6

#### IV. Scaling Analysis

The results with five die in parallel suggest that scaling the current of a potential IGBT replacement to, for example, 600 A is straightforward. Assuming a composite equivalent VJFET switch composed of 1-mm<sup>2</sup> 4H-SiC VJFETs with the properties recorded in Fig. 2 and a  $\Delta\rho_{sp(on)} = 0.87$  %/°C, a point design for the composite switch can be computed. Table II contains the key results from that point design. The Powerex PM600DVA060 “intellimod” two-pack IGBT half-bridge module (600 V, 600 A average, 1200 A peak) is used as a benchmark for the composite VJFET switch because it is known to be used in motor drives installed in series HEVs.

From Table II, a conservative estimate of the size of the equivalent switch (including co-packed SBDs) indicates that about 13 cm<sup>2</sup> (2 in.<sup>2</sup>) are required for an equivalent two-pack, which would easily fit in the existing package. Such a replacement, while meeting the same voltage and current ratings (including surge) of the IGBT, would offer the following advantages:

- 50 °C increase in junction temperature.
- 10× reduction in the recommended shoot-through dead time.
- Decreased switching losses.
- Potential for smaller package foot print.
- Copack with SiC Schottky barrier diodes to eliminate reverse recovery losses.

**Table II.** Point design for a composite VJFET device containing  $n$  devices.

$\rho_{sp(on)} @ 25^\circ\text{C}$ [m $\Omega\text{cm}^2$ ]	$\rho_{sp(on)} @ 175^\circ\text{C}$ [m $\Omega\text{cm}^2$ ]	J [A/cm $^2$ ]	I <sub>D</sub> [A]	Area [cm $^2$ ]	$n$
2.7*	6.2	323 <sup>†</sup> 646	600 1200	1.86	186*

\* Assuming 1 mm $^2$  die with characteristics shown in Fig. 2(b).

<sup>†</sup> Calculated at  $V_{DS} = 2$  V and  $T_j = 175^\circ\text{C}$ .

The first advantage, a significant increase in rated junction temperature, can be used by the HEV power train designer to increase the motor-drive base plate temperature from 80 °C to 105 °C, which could eliminate a redundant low-temperature cooling loop. Increasing the switching frequency in permanent magnet motor drives beyond that possible with high-current Si IGBTs will facilitate closer integration of the motor and the drive, which will further compact the HEV power train.

The issue of using normally off devices has not been addressed. However, it is noted that the reliable use of high-current Si IGBTs is facilitated by gate driver circuitry that is now built into IGBT modules such as the “intellimod” product. A VJFET equivalent “drop-in” replacement would include a similar feature to ensure correct drive of the SiC VJFETs during start-up and fault conditions.

#### IV. Conclusions

In this paper we have demonstrated the straightforward paralleling of five 3-mm $^2$  600-V 4H-SiC VJFETs. DC and switching results were presented that indicated approximately equal current sharing even though the devices were not selected to be matched die. The successful switching of a 152-A current pulse in a resistively loaded circuit with an open-circuit voltage of 300 V and an inductive spike of 70 V was demonstrated. The total switching time was shown to be less than 0.15  $\mu\text{s}$ , which indicates that a shoot-through dead time of 0.3  $\mu\text{s}$  would be adequate for a half-bridge leg used in a typical three-phase motor drive. A positive on-resistance temperature coefficient  $\Delta R_{(on)} = 0.87\ \%/^\circ\text{C}$  facilitates this reliable paralleling. The demonstration of a “drop-in” replacement for a commercially available Si IGBT module currently used in hybrid-electric vehicle conversions appears feasible.

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