10x Improvement of Power Transmission over Free Space Using Integrated Antennas on Silicon Substrates*

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Abstract

This paper reports the techniques for improving the characteristics of integrated antennas fabricated on silicon substrates for communications over air. Using these, the pair gain (G_a) of antennas on 20-Ω-cm substrates has been improved by ~10x over the previously reported result. Lastly, the possibility of realizing single chip radios with integrated antennas for communication over air is suggested by picking up, amplifying, and frequency dividing a 15-GHz sine wave transmitted from a 2-mm long on-chip antenna located 40 cm away using a packaged clock receiver with a 2-mm long on-chip zigzag antenna.

Introduction

A monolithically integrated true single chip radio (μNode), which incorporates a transceiver, a digital processor, a sensor and a power source has been proposed [1],[2]. The goal is to make this radio sufficiently small so that it can be used like the Smart Dusts [3]. Currently, a version with working frequency of ~24 GHz and range of 1-5 m is being developed. Since μNodes use on-chip antennas for transmission and reception, integration of antennas on to a silicon substrate is a critical requirement. μNodes can be distributed in large numbers to sense environments, and groups of μNodes can form a self-organizing wireless communication network for collecting and transmitting data (Fig. 1) much like the Smart Dusts [3].

Previous works have established that waves can be transmitted through silicon substrates and they can picked up using integrated antennas for communication within a silicon integrate circuit [1],[4]-[7]. For μNode applications, the waves must be transmitted outside of the chip and propagated over free space. In fact, to improve antenna efficiency, it is desirable to reduce propagation loss in the lossy substrate. To study this, measurement set-ups have been proposed and the basic feasibility of using integrated antennas for communication over 5-m has been established [2]. In order to improve the robustness of communication, to reduce power consumption of radios, and to increase the range, the antenna performance must be improved. To accomplish this, the dependences of integrated antenna characteristics for communication over air on silicon resistivity, substrate thickness, the separation between an antenna and silicon chip edge, and the thickness of oxide layer between an antenna and silicon substrate have been investigated and the results are presented in this paper. This paper demonstrates that the power transmission over 5 m can be improved by ~10x over the previously published result [2].

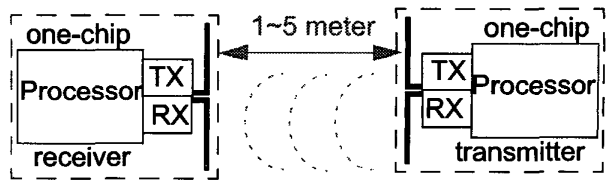

Fig. 1, μNode: a true single chip radio. The working range can be up to 5 m.

Test Chip and Measurement Setup

A testchip (Fig. 2) for integrated antennas is fabricated. The chip is similar to that used to study antenna characteristics for intra-chip communication [4]-[7]. All antennas are fabricated using a single Aluminum layer on an oxide layer on silicon substrates with no passivation. The metal thickness of all antennas is 1.5 μm and the metal width is 30 μm. Three different spacings between antennas and chip edge of ~50 μm, 0.5 cm and 1.0 cm were obtained by dicing a chip using on-chip separation markers. The testchip area is ~6 x 3 cm^2.

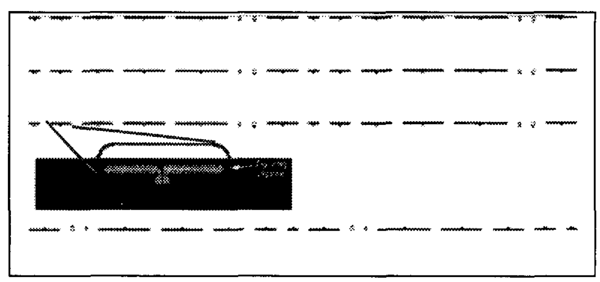

Fig. 2. An antenna test chip.

To evaluate integrated antenna characteristics as a function of the separation, two mobile wafer probe stands shown in Fig. 3 have been constructed using Derlin which is a type of plastic with ε_r of ~3.7 [2]. Each stand is equipped with a probe holder and a cable connection to test instruments (Fig. 3). These stands are used in two test configurations. The first test configuration (Fig. 4) utilizes a network analyzer for measuring antenna S-parameters [4]. The second configura-

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tion (Fig. 5) utilizes a signal generator and a spectrum analyzer. This second configuration enables measurements of power transmission gains of antenna pairs (G_a, equation (1)) [4] as a function of antenna separations in realistic operating environments. G_a includes the terms for gains of transmitter and receiver antennas and propagation loss.

$$G_a = \frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2 \qquad (1)$$

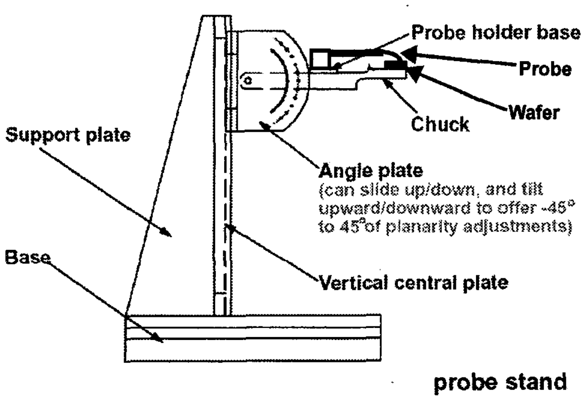

Fig. 3. Probe stand

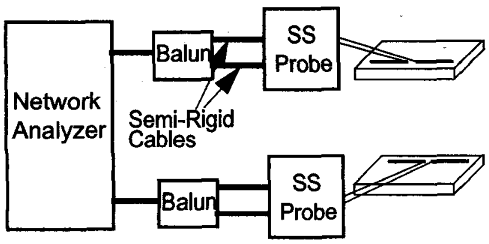

Fig. 4. Antenna measurement setup with a network analyzer.

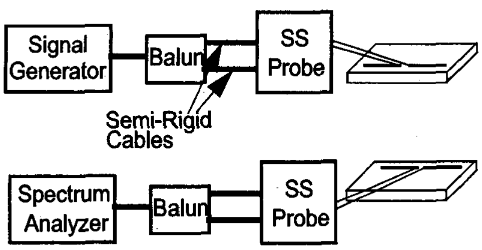

Fig. 5 Antenna measurement setup with a spectrum analyzer and a signal generator.

Measurement Results

The power transmission gains (G_a's) of pairs of 3-mm zigzag dipole antennas fabricated on 20-Ω-cm silicon substrates with a 3-μm oxide layer are characterized at 24 GHz. The silicon substrate thickness otherwise specified is 670 μm. In this study, because of higher G_a, 3-mm long antennas are used instead of 2-mm long antennas [2]. Fig. 6 shows plots of G_a versus antenna separations up to 10 m for two different substrate thicknesses. The distance (x-axis) is in a logarithm scale. The theoretical points are calculated for a pair of 3-mm linear dipole antennas transmitting and receiving in free space. The 3-mm on-chip antenna pairs with a 670-μm substrate thickness have ~20 dB more loss compared to the ideal 3-mm dipole pairs, and ~45 dB lower loss than that for a pair of probes. This loss is included in the antenna efficiency term of individual antenna gain (G_t and G_r) in Eq. (1). Clearly, this indicates that integrated antennas are critical to power transmission. G_a approximately obeys the inverse square law up to 10 m. Fig. 6 also shows the plot for a pair of antennas fabricated on a 20-Ω-cm substrate with thickness of 100 μm. This lower thickness was obtained by backlapping the substrate. G_a's can be improved by ~10 dB by this simple step due to reduction in substrate loss. It should be possible to improve G_a even more by further thinning the substrate.

Fig. 7 shows G_a versus antenna separation plots for the antennas located at three different spacings from a 20-Ω-cm wafer edge. The transmitting antenna has a 50-μm spacing to the edge, and the spacing to the edge is varied for the receiving antennas. The measurements were made in a lobby of a building which is close to the free space case (Fig. 8). Changing the separation from 50 μm and 0.5 cm has relatively small effect while increasing the separation to 1.0 cm decreases G_a by ~10 dB. This indicates that for antennas fabricated on 20-Ω-cm substrates, as long as the spacing is kept below ~0.5 cm, significant loss due to silicon substrate can be avoided.

Fig. 9 shows the input impedances for the antennas with varying spacings to the chip edge. The input impedances of 0.5-cm and 1-cm spacing cases are similar, but the 50-μm case is much different. When the separation is decreased to 50 μm, the real part of the impedance decreases because the antenna radiates almost directly to air with lower dielectric constant than that for silicon substrates. The data in Figs. 7 and 9 suggest that by adjusting the spacing, it should be pos-

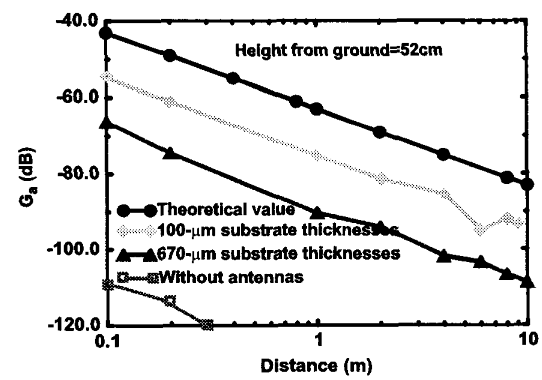

Fig. 6. Antenna gain vs distance in the outdoor dirt environment for 3-mm zigzag antennas on a 20-Ω-cm substrate with a 3-μm oxide layer with 670 and 100-μm substrate thickness at 52 cm height. The measurement frequency is 24 GHz.

sible to control antenna input impedance while not significantly degrading G_a's.

Fig 10 shows G_a's for antennas fabricated on substrates with varying resistivity and oxide thickness. Once again, a 3-mm antenna fabricated on a 20-Ω-cm substrate with a 50-μm separation to the wafer edge and a 3-μm oxide layer is used as the transmitting antenna. The receiving antennas were fabricated on a 10-mΩ-cm with a 3-μm oxide layer, 20-Ω-cm wafers with 1, 3 and 9-μm oxide layers, and on a sapphire substrate. The separation between antenna pairs is 1 m. The sapphire case has the highest G_a, and the 10m-Ω-cm case has the lowest G_a. For the antennas on 20-Ω-cm substrates, the

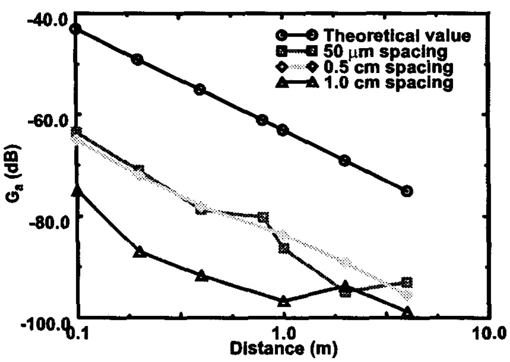

Fig. 7. Antenna gain at 24 GHz vs. distance for different spacings to the chip edge on a 20-Ω-cm substrate with a 3-μm oxide layer.

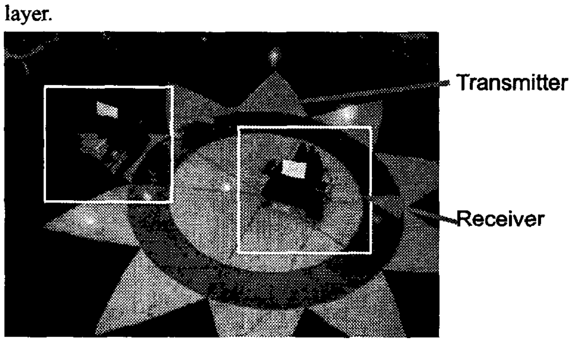

Fig. 8. Antenna radiation pattern measurement set-up.

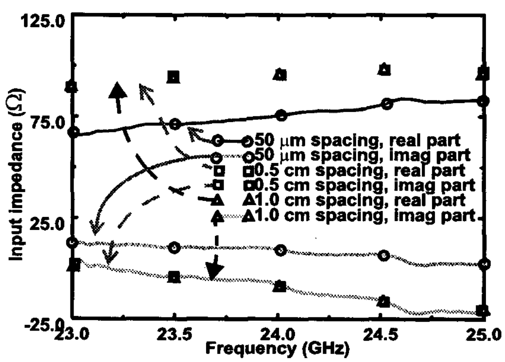

Fig. 9. Input impedance for different spacings to the chip edge on a 20-Ω-cm substrate with a 3-μm oxide layer.

G_a's of antennas on the 1-μm oxide layer is higher than those on 3 and 9-μm ones. The 1-μm oxide layer case has ~ 1.5 dB/side higher G_a than the 3-μm oxide layer case. The penalty associated with using a 20-Ω-cm substrate is ~10 dB/side compared to using a sapphire substrate which is essentially a loss less dielectric. The difference for a pair should be ~20 dB.

Fig. 11 shows the radiation pattern for a 3-mm zigzag antenna, which was fabricated on a 20-Ω-cm substrate with a 3-μm oxide layer. A 3-mm zigzag antenna is used as the transmitting antenna. Both antennas have the 50-μm spacing to the chip edge. The pair separation is 1.7 m. The pattern is similar to that for a pair of 2-mm long antennas on 1-μm thick oxide layer [2] and that for a pair of ideal short dipoles [2]. The set-up shown in Fig. 8 is also used for this measurement. G_a varies around ±2 dB over ~120 degrees.

The dipole has large energy storage close to the antenna. The region close to the dipole antenna maybe liken to a spherical resonator within which pulsating energy is trapped [6], so the performance of on-chip dipole antenna on a silicon substrate significantly suffers from the loss. Because of this, as the data indicated, the power transmission gain of antenna pairs can be improved by thinning silicon substrates, increasing the substrate resistivity, and decreasing the spacing between the antenna and chip edge.

Table 1 summarizes the numbers used in the link margin analysis for μNodes. For data rate of 100 kBits/sec, the expected sensitivity or the minimum signal the radio can detect is -95.8 dBm. Using the measured propagation and antenna loss, the received power is estimated to be -78 dBm

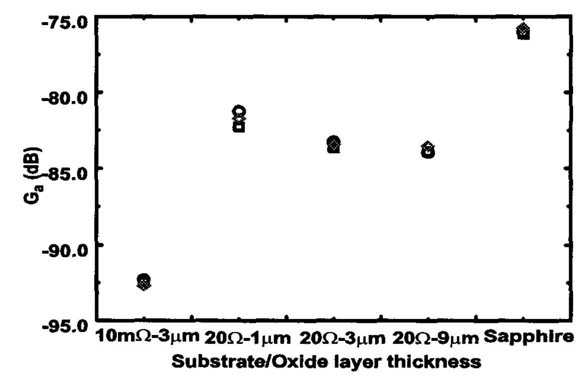

Fig. 10. Antenna gain at 24 GHz vs. substrate resistivity and oxide thickness for 3-mm zigzag antenna pairs. The antenna pair separation is 1 m. It shows three sets of data.

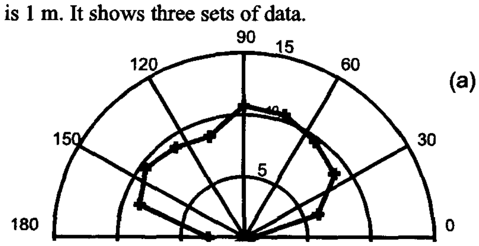

Fig 11. 3-mm zigzag antenna radiation pattern.

with transmitted power of 10 dBm. The difference between this and sensitivity or link margin of 17.8 dB is acceptable. This link margin is 12 dB larger compared to the previously reported result [2] due to the more than 10x improvement in power transmission.

Range	**5 m**
TX Power	**10 dBm**
Measured Propagation and Antenna Loss @ 24 GHz	**84 dB (100 μm thickness on 1μm oxide layer)**
Margin for radiation pattern (120° coverage)	**4 dB**
Received Power	**-78 dBm**
Thermal Noise	**-173.8 dBm/Hz**
Bandwidth (100 kBits/sec)	**50 dB**
E_b/N_o	**18 dB**
RX noise figure	**10 dB**
Sensitivity	**-95.8 dBm**
Link Margin	**17.8 dB**

Table 1. Link margin for μNode at 5-m separations

Figure 12 shows a clock receiver circuit [9] which has been packaged in a ball grid array package and mounted on a printed circuit (PC) board. The circuit is fabricated in a 0.18-μm CMOS technology. This has been utilized to receive a 14.8 GHz clock signal which was transmitted using a 2-mm long zigzag dipole antenna fabricated on a 20-Ω-cm substrate. The signal is picked up by the receiver which is 40 cm away (Fig. 12), amplified and frequency divided by eight to generate the ~1.79 GHz local clock signal. The spectrum of the 1.79 GHz signal in Fig. 13 is clean and well defined indicating that the receiver has locked on to the transmitted signal. The range was limited, because the sensitivity of the clock receiver is ~-40 dBm [9] instead of ~-96 dBm. This modest demonstration indicates that it is indeed possible to communicate over free space using CMOS radios with integrated antennas.

Conclusions

This paper has shown that there is a variety of ways to improve characteristics of integrated antennas fabricated on silicon substrates for communication over air. Using these, the pair gain of antennas on 20-Ω-cm silicon substrates has been improved by ~10x over the previously reported result [2]. The measurements indicate that for antennas fabricated on 20-Ω-cm substrates, as long as the antenna separation to the chip edge is kept below ~0.5 cm, large loss due to silicon substrate can be avoided. Reducing the substrate thickness from 670 to 100 μm, improves antenna pair gain by ~10 dB. Increasing the substrate resistivity also improves antenna pair gain.

References

[1] K. K. O et al., "Wireless Communication Using Integrated Antennas," 2003 IITC, pp. 111-113, San Francisco, CA, June 2003.

[2] J.-J. Lin et al., "Integrated Antennas on Silicon Substrates for Communication Over Free Space," Elec. Dev. Letts, IEEE, Volume: 25, NO. 4, pp. 196-198, April 2004.

[3]B. Warneke, M. Last, B. Liebowitz, K. S. J. Pister, "Smart Dust: communicating with a cubic-millimeter computer," Computer, vol. 34, no. 1, pp. 44-51, Jan 2001.

[4] K. Kim and K. K. O, "Characteristics of Integrated Dipole Antennas on Bulk, SOI, and SOS Substrates for Wireless Communication," 1998 IITC, pp 21-23, San Francisco, CA, June 1998.

[5] K. Kim, H. Yoon, and K. K. O, "On-Chip Wireless Interconnection with Integrated Antennas," Technical Digest of IEDM, pp. 485-448, San Francisco, CA, 2000.

[6] A.B.M.H. Rashid, S. Watanabe, T. Kikkawa, "High transmission gain integrated antenna on extremely high resistivity Si for ULSI wireless interconnect", Elec. Dev. Letts, IEEE, Volume: 23, Issue: 12, pp. 731 -733, 2002.

[7] K.T. Chan et al., "Integrated antennas on Si, proton-implanted Si and Si-on-quartz", IEDM Tech. Digest, pp. 40.6.1 -40.6.4, 2-5 Dec. 2001.

[8] J. D. Kraus and R. J. Marhefka, "Antennas: for all applications", McGraw-Hill, 3rd edition, 2003.

[9] B.-A. Floyd, C.-M. Hung, and K. K. O, "A 15-GHz Wireless Interconnect Implemented in a 0.18-μm CMOS Technology Using Integrated Transmitters, Receivers, and Antennas," IEEE J. of Solid-State Circuits, vol. 37, no. 5, pp. 543-552, May 2002.

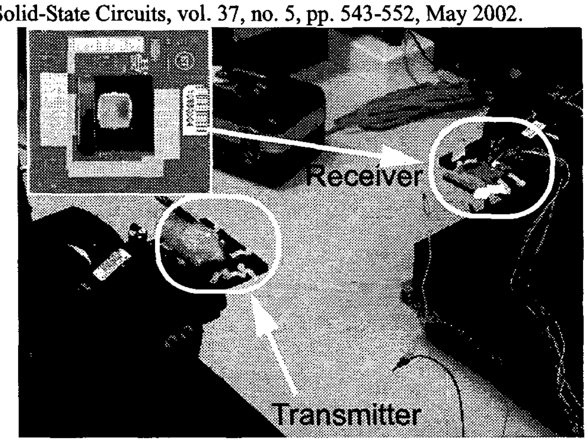

Fig. 12. The setup for wireless interconnect system demo.

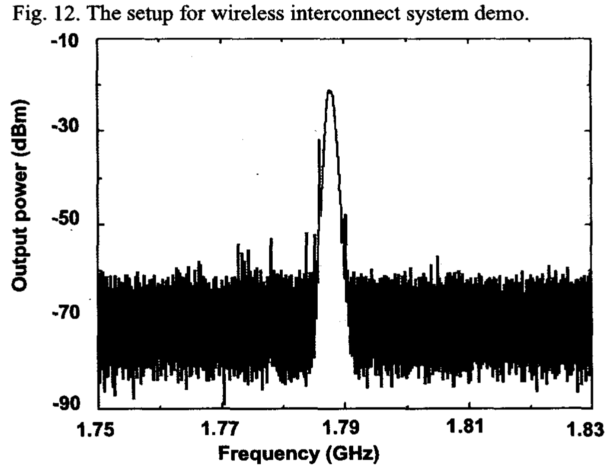

Fig. 13. Wireless interconnect system demonstration. The receiver locked onto a signal transmitted 40 cm away