Millimeter-Wave Voltage-Controlled Oscillators in 0.13-μm CMOS Technology

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***Abstract*—This paper describes the design of CMOS millimeter-wave voltage controlled oscillators. Varactor, transistor, and inductor designs are optimized to reduce the parasitic capacitances. An investigation of tradeoff between quality factor and tuning range for MOS varactors at 24 GHz has shown that the polysilicon gate lengths between 0.18 and 0.24 μm result both good quality factor (>12) and $C_{\max}/C_{\min}$ ratio (~3) in the 0.13-μm CMOS process used for the study. The components were utilized to realize a VCO operating around 60 GHz with a tuning range of 5.8 GHz. A 99-GHz VCO with a tuning range of 2.5 GHz, phase noise of −102.7 dBc/Hz at 10-MHz offset and power consumption of 7–15 mW from a 1.5-V supply and a 105-GHz VCO are also demonstrated. This is the CMOS circuit with the highest fundamental operating frequency. The lumped element approach can be used even for VCOs operating near 100-GHz and it results a smaller circuit area.**

***Index Terms*—CMOS, lumped model, millimeter wave, MOS varactor, quality factor, transmission line, voltage-controlled oscillator (VCO).**

I. Introduction

With the rapid advance of high-frequency capability for SiGe BiCMOS and CMOS technology, it is becoming possible to make circuits operating in millimeter-wave frequencies using silicon technology [1]–[16]. Monolithic microwave integrated circuits (MMICs) could be used to help satisfy the ever-increasing demand for bandwidth communication (broadband WLAN at 59–64 GHz ISM band) as well as the emerging needs for RF sensor systems such as automatic cruise control at 76–77 GHz and imagers at 94 GHz. The use of silicon technology will lead to lower cost and a higher integration level, and should turn the presently modest volume applications mentioned above, as well as others, into mainstream high-volume consumer applications.

Over the past five years, the maximum operating frequency of voltage-controlled oscillators (VCOs) fabricated in silicon technology has almost quadrupled from 25.9 to 117.2 GHz [1]–[6], [9]–[13], [15]. Push-push VCOs using the second harmonic operating at 63–131 GHz [8], [14], [16] have also been demonstrated in silicon technology. However, among these, the bulk CMOS fundamental VCOs operating around or above 50 GHz usually show poor phase noise, limited frequency range, or large power consumption. In this paper, the design tradeoffs and optimization techniques for high-frequency *LC*-resonator VCOs are described. These techniques are utilized to realize a lower phase noise or a wider tuning VCO operating around 60 GHz in the UMC 0.13-μm 1P8M CMOS technology. The low phase noise VCO achieves −109 to −102 dBc/Hz at 10-MHz offset over the tuning range of 3.8 GHz, while the other one achieves a wider tuning range of 5.8 GHz, but the phase noise varies between −108 and −99 dBc/Hz at the same frequency offset over the operating frequency range. Both VCOs consume 6.5 mA from a 1.5-V supply excluding that for output buffers. In addition, a 99-GHz VCO with a tuning range of 2.5 GHz, phase noise of −102.7 dBc/Hz at 10-MHz offset, and power consumption of 7–15 mW (not including buffers) from 1.5-V supply voltage, as well as a 105-GHz VCO with a tuning range of 200 MHz, phase noise of −97.5 dBc/Hz at 10-MHz offset, and power consumption of 7.2 mW (not including buffers) were demonstrated. This paper also shows that even at 100 GHz, the lumped element approach can be used to implement VCOs. Also, the circuit sizes can be reduced using the lumped elements instead of those based on transmission lines.

Section II describes the VCO circuit used in this work. This is followed by a discussion of the design of low parasitic varactor and inductor in Section III. Section IV proposes a low parasitic cross-coupled transistors layout. The experiment results are discussed in Section V. Conclusions and summary are presented in Section VI.

II. Circuit Architecture

The VCO employs the nMOS cross-coupled topology similar to [17] and is shown in Fig. 1. The resonator consists of a single-loop circular inductor and an accumulation mode MOS capacitor. The bias current is injected in the middle of the inductor by a pMOS transistor, M7. This enables the modulation of the $V_{\rm drain}$ node by changing the $V_{\rm bias}$ voltage [18]. As will be discussed, unlike other VCOs using the topology depicted in Fig. 1, this is the main mechanism used to tune the VCO frequency around 100 GHz. The use of pMOS current source allows utilization of the full range of the varactor without requiring tuning voltages above $V_{\rm dd}$ or below zero (Section III). In addition, the buffer for driving the 50-Ω load utilizes two tapered stages to lower the capacitance added to the *LC* tanks.

A key to achieving oscillation in an *LC* oscillator is providing sufficient negative resistance to cancel the losses in the resonant *LC* tank. This is particularly difficult at high frequencies, because the core transistors cannot be large due to the capacitances they add to the tank. To accommodate core transistors with a sufficient width, the parasitic capacitances connected to

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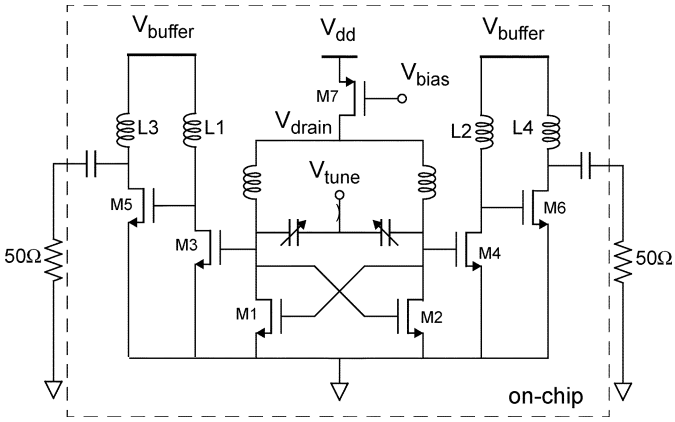

Fig. 1. Schematic of VCOs used in this study.

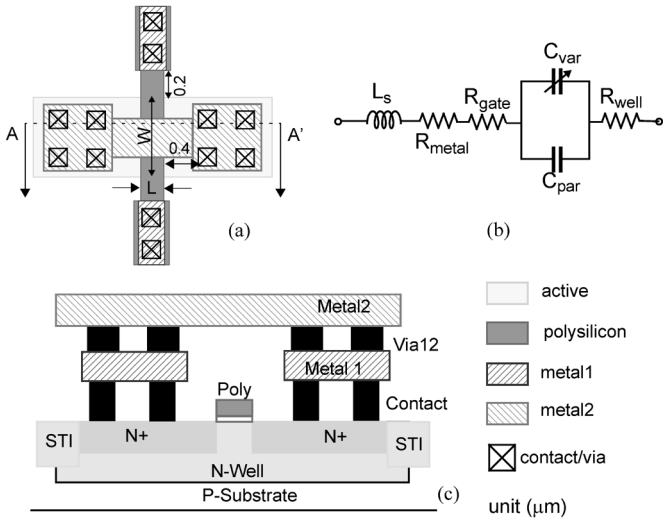

Fig. 2. (a) Top view, (b) cross section, and (c) equivalent circuit of MOS varactor.

the tank must be minimized. At a given operating frequency, the reduced parasitic capacitances also allow inclusion of larger varactors for a wider tuning range. The transistor size limitation can also be alleviated by increasing the quality factor (Q) of tank to lower the loss. Therefore, low parasitic and high-Q resonator network, as well as low parasitic and high gain transistor design is needed to increase the maximum VCO operating frequency.

III. Varactor and Inductor Design

A. MOS Varactor Design

Usually, at frequencies lower than 10 GHz, the Q of *LC* resonators is limited by the inductor. This is no longer the case at millimeter-wave frequencies. Because the Q of capacitors ($Q_C \sim 1/\omega R_s C$) decreases with frequency, while that of inductors ($Q_L \sim \omega L_s/R_s$) increases with frequency, the tank Q is limited by the Q's of capacitors at millimeter-wave frequencies and the optimized layout and accurate model for the MOS capacitor/varactor becomes more critical.

Fig. 2 shows the top-view, cross section of a MOS varactor and a simplified series $L_s - R_s - C$ model [19]. More dedicated varactor models, including n-well to substrate capacitance, substrate loss, and other effects, are discussed in [20] and [21]. The top and bottom plates are formed by silicided n^+ polysilicon and n-well, which are separated by a gate-oxide layer. The thickness of the gate oxide is only about 3 nm, which leads to a high capacitance density of 11 fF/μm^2 in the accumulation region. The poly gate is connected at two ends to reduce the resistance. To increase the tuning range, the parasitic capacitance must be minimized. This is especially important in advanced CMOS technologies, where the minimum metal-to-metal and contact-to-polysilicon spacing can be around 0.1 μm and the parasitic capacitance can be large [Fig. 2(a)]. To decrease the parasitic capacitance, the metal contacts for the n-well are placed 0.4 μm from the polysilicon gate. Since the n-well is usually AC-grounded, the increased n-well to substrate junction capacitance can be tolerated. The metal interconnection of the n-well is formed by only metal1 and metal2 layers, and the gates of each finger are connected together using the metal7 and metal8 layers. For comparison, a varactor structure using the minimum spacing and minimum poly gate length was fabricated. The metal connection for the n-well was formed by stacking metal1 through metal6. The measured capacitance is about 4 times that expected for the gate-oxide capacitance. The parasitic capacitance mainly due to the poly and metal interconnects is estimated to be about 3 times the gate-oxide capacitance.

As described in [19], if only the capacitance from gate oxide and resistance from poly gate and channel are considered, the Q of this simplified model is

$$Q \cong \frac{1}{\omega R_s C} = \frac{12}{\omega C_{\rm ox}(R_{\square,\rm nw} L^2 + R_{\square,\rm poly} W^2)} \qquad (1)$$

where W and L are the width and length of each finger, $R_{\square,\rm nw}$ and $R_{\square,\rm poly}$ are the sheet resistances of the n-well and poly gate, respectively, ω is the frequency, and $C_{\rm ox}$ is the gate-oxide capacitance per area. The factor of 12 in the numerator accounts for reduced series resistance from the double-sided n-well and poly gate contacts. To increase Q, smaller W and L should be used. However, the penalty is larger parasitic capacitance due to more metal interconnects and larger total metal width, which decreases the tuning range. Since $R_{\square,\rm nw}$ is more than 50 times $R_{\square,\rm poly}$, L should be made smaller, while the W of a finger can be made larger to reduce the parasitic capacitances. With the continuing scaling in CMOS technology, the Q of varactors should increase with smaller gate lengths and lower n-well sheet resistance. However, this increase will be tempered by the increases of $C_{\rm ox}$ as well as the contact and via resistances.

To experimentally examine these tradeoffs in varactors designed for operation above 20 GHz, structures with varying gate lengths were fabricated in the UMC process. The average capacitances of structures are kept approximately the same. The effects of pads are de-embedded using the open structure form by disconnecting the gate connection from the pad as discussed in [19]. One-port S-parameters of the test and open structures were measured using an HP8510C 26.5-GHz network analyzer. Using the simplified model in Fig. 2(b), the Q is calculated from $|\mathrm{Im(Y)/Re(Y)}|$ and the equivalent capacitance is calculated from $-1/(\omega \bullet \mathrm{Im(Z)})$. Fig. 3(a) shows the *C–V* and *Q-V* curves measured at 24 GHz for three varactors with different

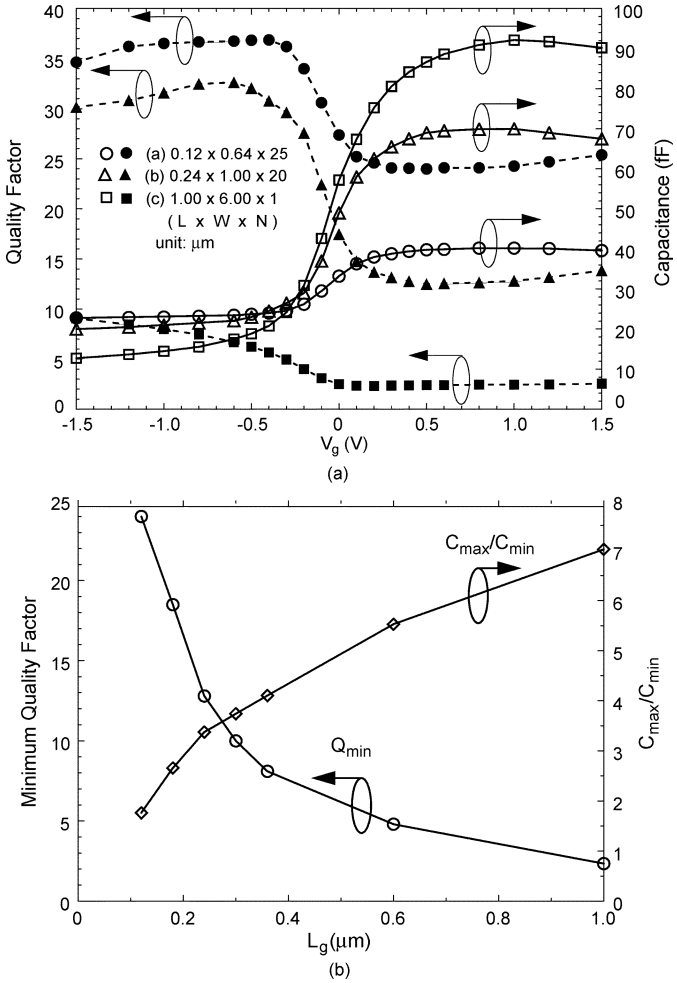

Fig. 3. (a) *C–V* and Q-V characteristics of the MOS varactors with different dimensions. (b) Minimum varactor Q and $C_{\max}/C_{\min}$ ratio as a function of gate length measured at 24 GHz.

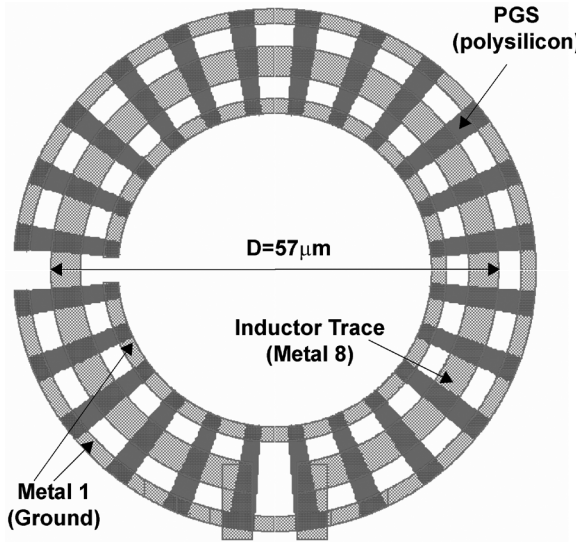

Fig. 4. Inductor layout.

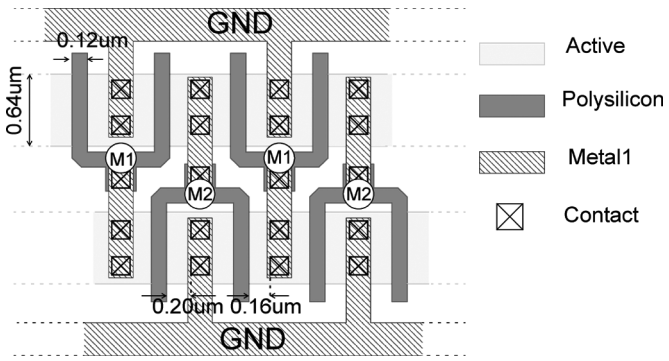

Fig. 5. Cross-coupled transistor layout.

dimensions. The minimum gate length of 0.12 μm is used for structure (a), thus, it gives nearly the highest Q available. A minimum Q of 24 is achieved at 24 GHz, which is close to the Q reported in [1]. When extrapolated using $Q = 1/(\omega R_s C)$, Q is about 9 and 6 at 60 and 100 GHz, respectively. In reality, the series resistance increases with frequency due to the skin effect, so the Q's at 60 and 100 GHz will be lower. For this minimum gate varactor, the tuning range is limited $(C_{\max}/C_{\min} = 1.75)$, though larger than 1.2 in [1]. In structure (c) with a gate length of 1 μm, the tuning range $(C_{\max}/C_{\min})$ is $\sim$7. As expected, the penalty is lower Q of $\sim$2.5 in the accumulation region. A medium gate length of 0.24 μm is used in structure (b), which has moderate Q at 24 GHz of 12.5 and an acceptable $C_{\max}/C_{\min}$ ratio of 3.5. Fig. 3(b) shows the measured minimum Q and $C_{\max}/C_{\min}$ ratio of varactors with varying gate lengths. The minimum Q decreases with an increase in the gate length, while the tuning ratio increases. Depending on the operating frequency, phase noise, power consumption and tuning range requirements for the VCO, a suitable varactor structure can be chosen using a plot like this. For the 0.13-μm CMOS process, the gate lengths between 0.18 to 0.24 μm result in good tuning and Q.

The varactor shows the best tuning around zero gate bias. For the VCO in Fig. 1, the top plate (gate) voltage of varactor is set to $\sim V_{\rm DD}/2$ by using the pMOS current source on the top. When the bias voltage on the bottom plate of varactor is varied between 0 and $V_{\rm DD}$, the voltage across the varactor varies from $-V_{\rm DD}/2$ to $V_{\rm DD}/2$. This enables utilization of essentially the full range of varactor capacitance without the need for tuning voltages below zero or above $V_{\rm DD}$. Fig. 3(a) also shows that the *C–V* curve is not monotonic due to the poly depletion when the gate bias is higher than 1 V. This may lead to a locking problem in the phase-locked loop [1]. Since $V_{\rm DD}$ is usually 1.2–1.5 V for the circuits built using this process, limiting the gate to bulk voltage from $-V_{\rm DD}/2$ to $V_{\rm DD}/2$ helps to avoid the bias range affected by the poly depletion effect.

B. Inductor Design

Fig. 4 shows the layout of the differential circular inductor used in the 105-GHz VCO. To reduce the capacitance to the substrate, only the top metal8 layer is used. The metal8 layer is 0.8 μm thick and $\sim$ 5 μm above the silicon substrate. The metal width is 3.6 μm. Since the skin depth of copper at 105 GHz is $\sim$ 0.2 μm, the metal width of inductor can be narrowed to $\sim 6 \times 0.2 = \sim 1.2$ μm. The patterned ground shield is formed using the polysilicon layer and each finger is perpendicular to

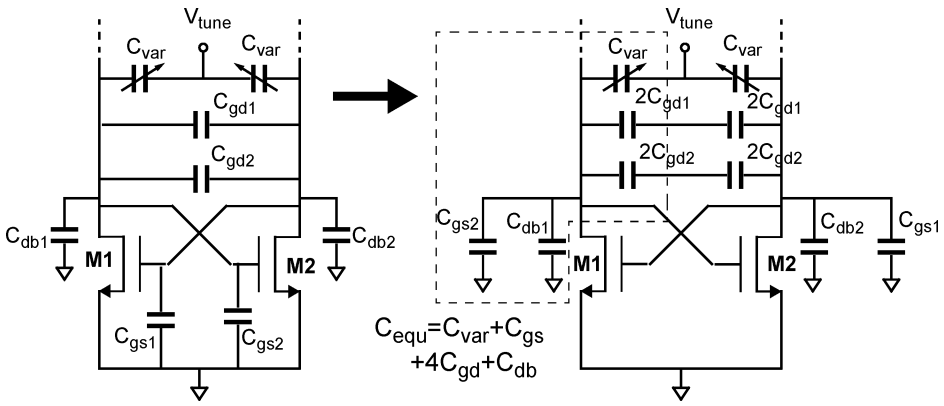

Fig. 6. Equivalent capacitor model.

the metal trace. The spacing between polysilicon shield is set to $\sim$ 4 μm to reduce the parasitic capacitance without degrading the quality factor [22]. A lumped inductor model [23], [24], including a series resistor, shunt capacitors, and substrate loss, is used for the design. The model parameters are extracted using Agilent Momentum, a 2.5-D EM field simulator. The simulations show the inductance of loop with a diameter of 57 μm is $\sim$90 pH and $Q_{\rm bw}$ [25] is $\sim$50 at 105 GHz. For the 59-GHz VCO, the inductor diameter is 89.6 μm and the trace width is 4.8 μm. The inductance is $\sim$200 pH and $Q_{\rm bw}$ is $\sim$35 at 60 GHz. Finally, the interconnections carrying signals at the millimeter-wave frequencies have also been modeled using the lumped inductor model.

IV. Transistor Design

As mentioned, to increase the oscillation frequency, the parasitic capacitance connected to the tank must be minimized. For the VCOs operating near 60–100 GHz, the capacitance of transistors in the 0.13-μm technology can be comparable to or larger than that from the varactors. Therefore, the parasitic capacitance of the transistor must also be minimized. Fig. 5 shows the top view of cross-coupled transistors, which is similar to that used in [26]. It consists of a top part (M1) and a bottom part (M2) that are directly cross connected from the drain to gate. This makes the metal interconnection between the two transistors shorter, which lowers the loss and parasitic capacitance of the interconnection. The drains of the fingers are connected together by metal6 lines. The finger width of transistors needs to be kept small to lower the gate resistance. This, however, increases gate-to-body/substrate capacitance. Because of these two competing effects, there should be an optimal finger width [26]. The final finger width of 0.64 μm is chosen. From the measured results in [7], $f_{\rm max}$ is expected to be $\sim$120 GHz.

As was done for the varactor, the metal spacing is intentionally increased. The spacing of source contact to gate is made 0.20 μm, so that the parasitic gate and drain-to-source capacitances are reduced at the expense of slightly larger source series resistance. The increased source-to-body capacitance has negligible impact on VCO operation since the source nodes are virtual grounds. The drain is usually made as small as allowed by design rules to reduce $C_{\rm db}$. However, in the VCO, the gate-to-drain capacitors $(C_{\rm gd})$ of two core transistors are connected to the anti-phase nodes. As shown in Fig. 6, due to the Miller effect, the gate-to-drain overlap capacitance contribution to the tank is $2(C_{\rm gd1}+C_{\rm gd2})$. Thus, the effective transistor capacitance at the drain node is actually $C_{\rm db}+4C_{\rm gd}$. Increasing the spacing between drain contact and gate decreases $C_{\rm gd}$ and increases $C_{\rm db}$. Simulations show that the drain contact to gate spacing of $\sim$ 0.16 μm minimizes the effective capacitance added to the tanks. As mentioned before, the capacitance of transistors can be comparable or larger than that from the varactor. Because of this, the Q of the *LC*-tank strongly depends on the transistor. For the 100-GHz VCOs, since the capacitance of the transistor is much larger than that of the varactor, the transistor capacitance is expected to determine the Q of the *LC*-tank.

V. Experiment Results

Fig. 7 shows the chip micrograph of the 59-GHz and 105-GHz VCOs. Each VCO occupies 500×480 μm^2 including bond pads. The VCOs were measured on-wafer with an Agilent E4448A 50-GHz spectrum analyzer and either an Agilent 11970U 40–60 GHz or 11970 W 75–110 GHz harmonic mixer. The harmonic mixer down-converts the output to $\sim$320 MHz [27]. A 75–120 GHz wave-guide probe is used to measure the VCOs operating near 100 GHz.

A. 59-GHz VCOs With Wide Tuning Range

The 60-GHz WLAN band spans the frequencies between 59 and 64 GHz. The VCO for this application must have a tuning range greater than 5 GHz. However, the recently published CMOS VCOs operating near 40–60 GHz have tuning ranges significantly less than 5 GHz [2], [3], [11], except those fabricated using SOI processes [4], [9] due to lower parasitic capacitances in the SOI processes. A wider tuning range in bulk CMOS is also possible when the parasitic capacitances from the varactor, transistor, and inductor are minimized as discussed in Sections III and IV. The varactor value should be maximized and varactors with a larger tuning ratio should be used. This, however, can degrade phase noise because of an increase of VCO gain and a decrease of varactor Q. To evaluate this tradeoff for VCOs operating in the millimeter-wave frequency range, two VCOs with different varactor structures are fabricated. In the first VCO, varactors with twenty 0.12 μm $(L)\times$ 0.64 μm (W) fingers are used. In the second one,

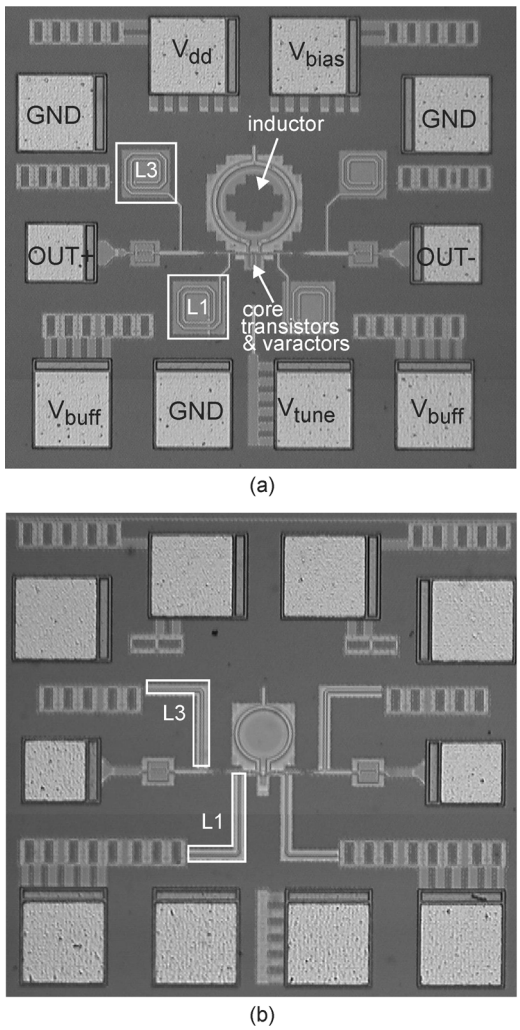

Fig. 7. Micrograph of (a) the 59-GHz VCO and (b) 105-GHz VCO.

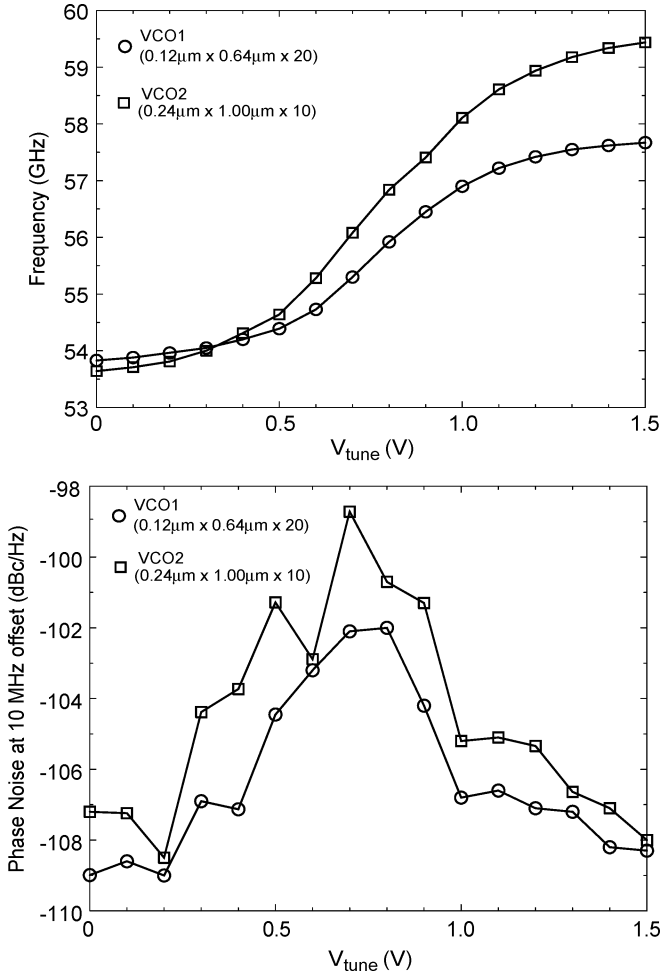

Fig. 8. Frequency tuning range and phase noise versus tuning voltage of two VCOs with different varactor gate lengths.

varactors with ten 0.24 μm $(L) \times 1$ μm (W) fingers are used. The two varactor structures have nearly the same capacitance value in the accumulation region. The core transistor width is chosen to be 14.72 μm. It is more than twice the minimum size required to sustain oscillation in simulation.

When the varactors are biased in the depletion region $(V_{\rm tune} = 1.5$ V), both VCOs start to oscillate with about 3.5-mA current from a 0.9-V supply. To achieve good phase noise performance and output power greater than -10 dBm, the measurements are made at 6.5-mA bias current and 1.5-V $V_{\rm DD}$. The output buffer consumes about 10 mA from a 0.8-V supply. Fig. 8 shows the measured carrier frequency and phase noise at 10-MHz offset versus the tuning voltage for these two VCOs. The phase noise peaks around 0.5$\sim$1.0-V tuning voltage due to larger VCO gain resulting from a higher rate of change of varactor capacitance. For the VCO using 0.12-μm gate-length varactors, the tuning range is 3.8 GHz, while for the second VCO using the varactors with 0.24-μm gate length, the tuning range is 5.8 GHz. This difference is due to the larger tuning from the varactors with a longer channel length. When the varactors are biased in the depletion region $(V_{\rm tune} = 1.5$ V), the two VCOs show similar phase noise of -89 dBc/Hz (not shown) and -108 dBc/Hz at 1-MHz and 10-MHz offset from carrier, respectively. This is because Q-factors of both varactors are similar in the depletion region. When the varactors are biased in the accumulation region $(V_{\rm tune} = 0$ V), the VCO using the shorter gates shows $\sim$1 dB better phase noise and when the varactors are biased in the transition region, the VCO using the shorter gates shows 2–3 dB better phase noise. The differences are attributed to the 50% lower Q of the longer channel varactor as well as the larger VCO gain in the transition region resulting from the larger tuning range.

B. VCOs Near 100 GHz

Since the $f_{\rm max}$ of nMOS transistors in the 0.13-μm CMOS process is higher than 100 GHz, so it should be possible to implement a VCO operating near 100 GHz. By applying the low-parasitic low-loss design approaches discussed in Sections III and IV, VCOs operating between 90–105 GHz were implemented. To explore the frequency limit of this process, varying transistor sizes from 12.16 to 8.32 μm are used to vary the center frequencies of VCOs. The varactor and inductor values are fixed. For the varactors, the minimum gate length is not used. Instead, one 0.24 μm $\times$ 0.9 μm finger with a larger tuning ratio is used. The inductor is already described in Section III. For the cross-coupled transistors, the finger width is 0.64 μm, while the

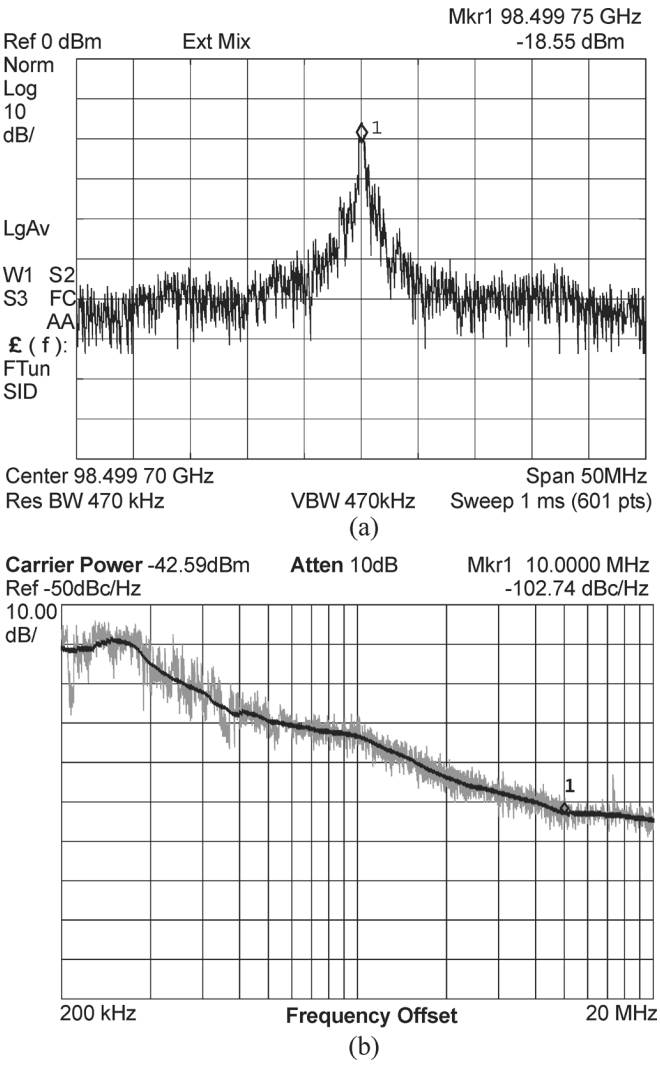

Fig. 9. Measured output spectrum and phase noise of the 99-GHz VCO.

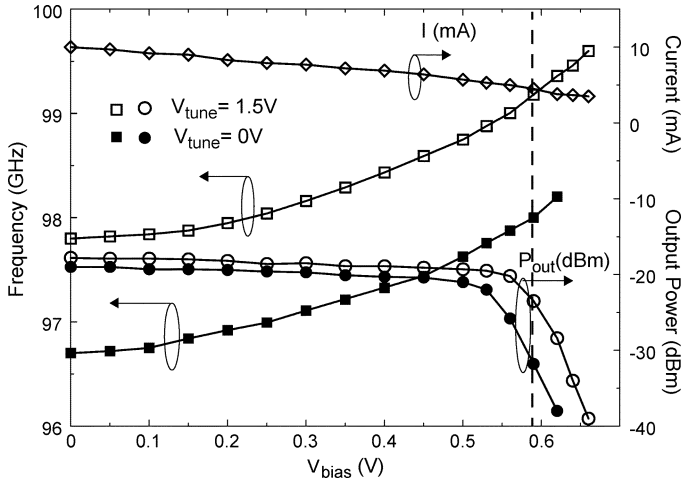

Fig. 10. Frequency tuning, current consumption and output power of the 99-GHz VCO at $V_{\rm DD} = 1.5$ V.

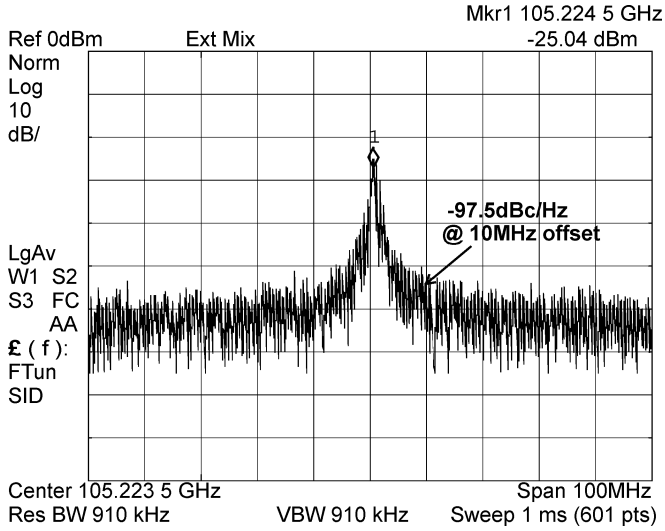

Fig. 11. Output spectrum of the 105 GHz VCO.

number of fingers is changed from 19 to 13. The maximum measured oscillation frequency for VCOs with the core transistor width of 12.16, 10.88, 9.6, and 8.32 μm is 93.5, 96, 99.2, and 105.3 GHz, respectively.

Transmission lines have been used for matching and tuning in the circuits operating at frequencies from 60 to 100 GHz [5]–[7]. However, a quarter-wavelength of typical dielectric layers used in silicon process technologies is still about 600 and 375 μm at 60 and 100 GHz, respectively. Because of this, the lengths of transmission lines used to implement inductors for the 100-GHz VCO in [5] are more than 300 μm. The dimensions of the components in the 105 GHz VCO are less than 90 μm or $\sim$6% of a wavelength. This makes the lumped element analysis still applicable for these components even at 105 GHz. Furthermore, it should be possible to reduce the size and loss using lumped elements even at 100 GHz. The lumped model of varactor was extracted from the measurements at 24 GHz and the inductor model was constructed using Agilent Momentum. The simulated carrier frequencies and tuning range are within 5% of the measurements.

The 99-GHz VCO using 9.6-μm-wide cross-coupled transistors starts to oscillate at the bias current and supply voltage of 3.4 mA and 1.0 V. Once again, for more stable oscillation and larger output power, the measurements are made at higher bias current of 6 mA and $V_{\rm DD}$ of 1.5 V. An amplifier with 20-dB gain and 4.5-dB noise figure is added between the mixer output and spectrum analyzer to reduce the impact of background noise from the analyzer. The measured output spectrum is shown in Fig. 9(a). The external amplifier gain, $\sim$40-dB conversion loss of mixer and $\sim$3-dB loss from probe and cable were de-embedded. The measured phase noise is about -103 dBc/Hz at 10-MHz offset from the carrier.

Since the transistor capacitance is the dominant contributor to the LC-tank capacitance and the transistor capacitance depends on the bias conditions, the transistor capacitance can be tuned to increase the tuning range. In fact, several authors have suggested changing supply voltage to increase the tuning range of VCOs [3], [5]. However, varying supply voltage is not practical. A simpler way to vary the DC bias of transistors is to change the gate bias of the tail transistor (M7 in Fig. 1) [18]. By limiting the current range, it is possible to limit the variations of output power and phase noise over the tuning range. In this implementation, the $V_{\rm bias}$ is used for fine tuning and the

TABLE I
COMPARISON WITH RECENTLY PUBLISHED HIGH-FREQUENCY VCOS IN SILICON TECHNOLOGIES

Ref	Frequency (GHz)	Phase Noise (dBc/Hz)	V_{dd} (V)	P_{dc} (mW)	Tuning (GHz)	Technology
This work	59	-89@1MHz	1.5	9.8	5.8	0.13-μm CMOS
	98.5	-102.7@10MHz	1.5	7–15	2.5[a]	
	105.2	-97.5@10MHz	1.2	7.2	0.2	
[2]	50	-100@1MHz	1.3	13	1.0	0.25-μm CMOS
[3]	51	-85@1MHz	1.0	1	1.0[a,b]	0.12-μm CMOS
[4]	40.7	-89@1MHz	1.8	11.3	6.0	0.13-μm SOI CMOS
[5]	103.9	<-94@10MHz	1.5	180	N/A	90-nm CMOS
[9]	60.6	-90@1MHz	1.5	21	8.3[b]	90-nm SOI CMOS
[10]	85.8	-97.5@1MHz	3	25.8	2.3	0.12-μm SiGe
[11]	43	-91@1MHz	1.0	7	1.7	0.13-μm CMOS
[12]	80.6	-97@1MHz	N/A	1200[c]	6.7	0.35-μm SiGe
	100.2	-90@1MHz	N/A	N/A	6.2	
[13]	117.2	N/A	2.5	25–70	3.7[a]	0.25-μm SiGe
	114.5	N/A	2.5	N/A	8.7	

[a]The bias conditions of the transistors are changed to increase tuning range.
[b]The tuning voltage is higher than supply voltage.
[c]Higher power consumption is due to the powerful output buffer and large output power level.

varactors are used for coarse tuning. Since the varactors are biased in either strong accumulation or depletion, where the VCO gain due to the varactors is smaller, this helps to keep the phase noise low. Fig. 10 shows the tuning characteristics of VCO. By varying $V_{\rm bias}$ from 0 to 0.59 V when $V_{\rm tune}$ is 1.5 V, the bias current can be changed from 4.5 to 10 mA and the VCO can be tuned between 97.8 and 99.2 GHz. By biasing the MOS varactor in the accumulation region ($V_{\rm tune} = 0$ V), the output frequency can be varied between 96.7 to 98 GHz. Over the tuning range, the phase noise at 10-MHz offset varies from -99.5 to -102.7 dBc/Hz and output power varies from -22 to -18 dBm. The total tuning range is 2.5 GHz or $\sim$2.5%. The best phase noise is measured at 6-mA bias current instead of the largest current. If larger output power level variations and higher phase noise can be tolerated, the tuning range can be increased to $\sim$3 GHz.

By reducing the core transistor width to 8.32 μm, a VCO operating from 105.1 to 105.3 GHz is demonstrated. The VCO consumes 6 mA from a 1.2-V supply. Fig. 11 shows the measured output spectrum. The VCO achieves phase noise of -97.5 dBc/Hz at 10-MHz offset. This is the highest fundamental frequency CMOS circuit reported to date. The tuning range is only 200 MHz. The circuit stops oscillation when the varactors are biased in the accumulation region or the bias current is reduced below 5 mA. This also suggests the oscillation frequency of 105 GHz is very close to the limit of 0.13-μm CMOS process. By using these VCOs in a push-push configuration [8], [14], [16], it should be possible to generate a signal at $\sim$200 GHz. Furthermore, if more scaled transistors are used, then it should be possible to generate signals with frequencies in the sub-millimeter wave frequency or even THz using bulk CMOS.

VI. CONCLUSION

Millimeter-wave VCOs operating near 60 and 100 GHz are presented. Reducing the metal parasitic capacitances of varactors, inductor and transistors is the key for achieving the wide tuning range ($\sim$6 GHz) at 60 GHz and operation near 100 GHz using a bulk CMOS process. Table I compares the characteristics of recently published millimeter-wave fundamental VCOs implemented using silicon technologies. The 59-GHz VCO has almost comparable phase noise and tuning range as that implemented in a 90-nm SOI CMOS process [9]. This work also shows that with optimized design, a much higher VCO operating frequency can be attained. As a matter of fact, the 105-GHz VCO has higher operating frequencies than the ones fabricated in a 90-nm technology [5]. This work has also shown that even at 100 GHz, lumped elements which should occupy a smaller area than the components based on transmission lines can be used. This should also reduce the simulation complexity.

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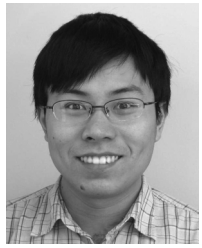

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