CMOS Readout System for a Double-sided Germanium Strip Detector[1]

R.A. Kroeger, W.N. Johnson, J.D. Kurfess
Naval Research Laboratory, Washington, DC 20375
W.G. Schwarz, M.E. Read
Physical Sciences Incorporated, Alexandria, VA 22312
M.D. Allen, G.T. Alley, C.L. Britton, L.C. Clonts, M.N. Ericson, and M.L. Simpson
Oak Ridge National Laboratory, Oak Ridge, TN 37831

Abstract – A wide variety of applications require a hard X-ray or gamma ray detector which combine both good spatial resolution and energy resolution. Double-sided solid-state strip detectors provide this capability. We report on the development of CMOS electronics designed for photon detection with strip detectors. These electronics include a low noise preamplifier, semi-gaussian shaping amplifier, discriminator, and peak detection circuitry. All circuits are designed to operate at low power. Circuits have been duplicated in both NMOS and PMOS to provide both polarities of signals. We have constructed an 8×8 channel system to test these prototype chips. Power consumption for the preamplifier through peak-detector circuit is 4 mW/channel. The test system has a conversion gain of ~35 mV/fC, system noise (equivalent noise charge) of ENC<220 e rms (0 pF), and a dynamic range of >100:1 in both NMOS and PMOS circuits.

I. Introduction

Double-sided solid-state strip detectors are important in a wide variety of photon detection applications that require both good spatial resolution and energy resolution. Germanium strip detectors are currently available which provide 2 mm spatial resolution combined with excellent energy resolution over a wide energy range extending to ~1 MeV [1]. CdZnTe and silicon strip detectors are finding applications as hard and soft X-ray detectors [2,3]. All of these detectors require compact, low-noise electronics with on the order of 10 to 1000's of channels. Both polarities of signals must be measured. Applications such as space-based detector systems also require that these electronics are low power. Most photon counting applications require that the electronics be self-triggering over a wide dynamic range. Very few end-to-end systems with all of these properties have been developed. Examples of chips developed originally for silicon strip detectors are the XA-1 (commercial device from IDE AS), and the ACE chip (NASA/Caltech). We present here results from an ASIC chip set developed at Oak Ridge National Laboratory (ORNL) specifically for the germanium strip detector.

II. Electronics

Four ASICs have been developed using the ORBIT FORESIGHT 1.2 micron n-well process. These chips are referred to collectively as NRL-4, and represent the fourth step in a series of prototype chips developed specifically for the germanium strip detector. One chip set is PMOS and the other NMOS for positive and negative input signals respectively. A standard die size of 2.4 × 2.4 mm (TINY chip) was selected for circuit development. The front-end chip is a two channel preamplifier and shaping amplifier similar to the chip described in reference [4]. The preamplifier has a conversion gain of ~35 mV/fC and an RC recovery time ~1 msec. The design is descended from the preamplifier developed by ORNL for silicon track detectors in the PHENIX and PHOBOS projects for the Relativistic Heavy Ion Collider [5]. The peaking time of the output pulse is ~6–9 μs which is optimizes the energy resolution achieved for a germanium detector with low current leakage. Pulse shaping is CR-RC^2 with poles provided by n-well or p-well resistors respectively. The second chip is a two channel Peak Detect and Hold (PDH) circuit with a discriminator for self-triggering. The peak detection circuit is based on a design by Kruiskamp and Leenarts [6] and uses a MOS current mirror instead of a rectifying diode, thereby minimizing the effect of charge injection into the hold capacitor when a peak is detected [7].

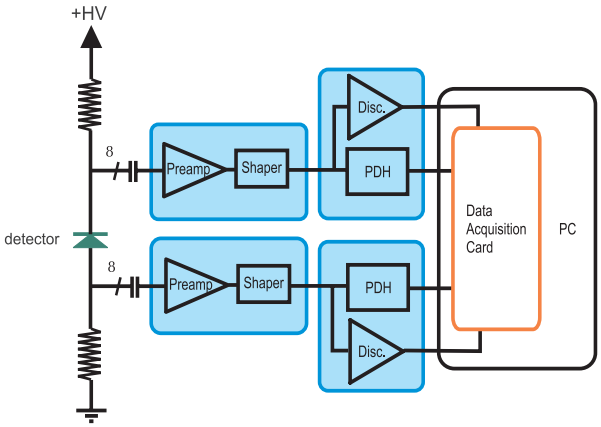

Fig. 1. Block diagram of the 8×8 channel demonstration system.

A simplified block diagram of the readout system is shown in Figure 1. The four varieties of ASICs are indicated by the shaded boxes. The demonstration system provides 8 p-channel and 8 n-channel readouts. Four copies of each ASIC are required in the full 8-channel system since the prototype ASICs are 2 channel devices (detail not shown in the Figure). In the 8×8 system, the PDH signals are digitized using a standard data acquisition card with 16 channels multiplexed

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into a 12-bit ADC. The data acquisition card is plugged into a personal computer (PC). Differential line drivers, optical isolators, and a ferrite loop were added between the PC and the demonstration board in order to minimize noise pick-up from the PC. Discriminator signals on the PDH circuits are combined to provide a trigger for the data acquisition cycle. All 16 signals are digitized. Data is stored in list mode for subsequent processing and analysis.

Several biasing adjustments are made external to the ASICs in the prototype chip set. Key adjustments are the DC level of the amplifier chip baseline, gate voltage of the feedback MOSFET (feedback resistance), discriminator voltage, and linear gate reference voltage. For this work, the NMOS devices were all operated with a baseline of 1.5 V and the PMOS devices with a baseline of 3.5 V. A large pulse will drive the NMOS shaping amplifier to near 5 V and the PMOS shaping amplifier to near 0 V from the baseline.

The ASICs are powered by a single 5 V power supply. Power consumption for the preamplifier through peak-detector is ~4 mW/channel. Most of the power is consumed in the front-end MOSFET in the preamplifier. The PDH accounts for only 0.5 mW/channel.

III. RESULTS

The output of the shaping amplifier and the PDH ASICs are shown in Figure 2 for an input pulse about 70% of full scale. The shaping amplifier produces a semi-gaussian peak with a peaking time ~6 μs with an input capacitance C_{in}=6 pF. Peaking time increases slightly with higher input capacitance. The PDH trace is superimposed showing the circuit following the rise in the shaper output, then holding the peak voltage. The PDH is observed to have a slight overshoot, typically on the order of 10-20 mV from channel to channel. The overshoot is constant and does not vary from pulse to pulse at a measurable level. The PDH is reset after its output voltage has been digitized and the is ready for the next pulse.

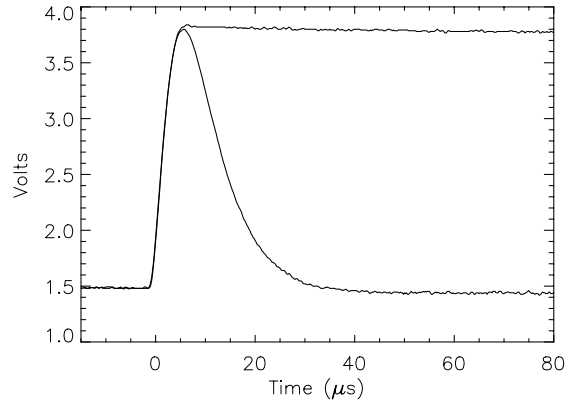

Fig. 2. Oscilloscope trace of the shaping amplifier output peak hold circuits.

Integral linearity of the ASICs is particularly important where good energy resolution is required and in systems with large numbers of channels that need to be to adjusted and calibrated similarly. Linearity of the NRL-4 chip set was measured over a dynamic range of >100:1, from <30 mV output above/below the baseline to >3000 mV for the NMOS/PMOS chip sets respectively. A charge input was generated using a voltage step into a 1.2 pF test capacitor connected to the preamplifier input. Results of this test are shown in Figure 3. Both the PMOS and NMOS chip sets performed within ±0.2% of linear over the full useful signal range. Linearity was excellent even when the chips are driven to well within 0.5 V of ground or +5V respectively, providing a useful range of signals spanning nearly ~3.5 V above/below the baseline voltage.

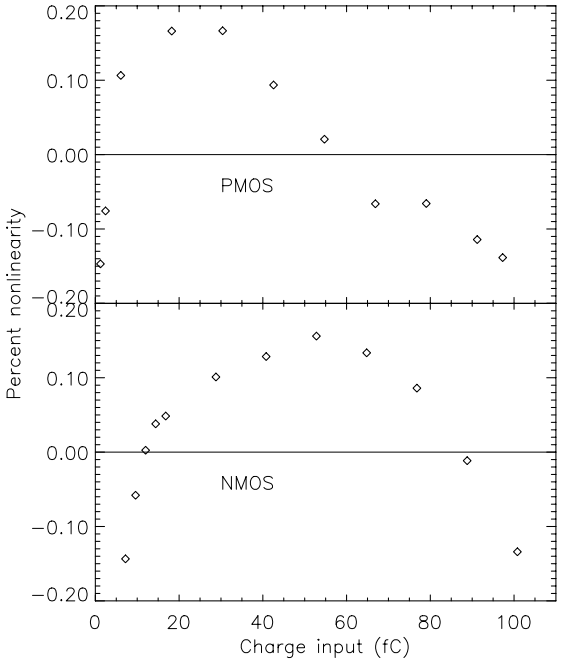

Fig. 3. Integral linearity of the NRL-4 PMOS and NMOS chip sets. The measurement includes the preamplifier/shaping amplifier chip and the PDH chip.

The isolation board was effective at reducing noise from the PC to low levels but not eliminating it entirely. Digital oscilloscope measurements of the shaping amplifier output show 2.2 mV rms with the PC on, and 1.8 mV rms with the PC off (C_{in}=6 pF). Expressed as equivalent noise charge, the PC is estimated to contribute ~210 e rms to the measurements. The validity this noise estimate is confirmed by comparing rms noise measured by the oscilloscope with the peak width measured in a pulse-height histogram obtained using the PC. The two methods estimate the noise to <10% of each other, indicating that the oscilloscope is an accurate measure of the noise out of the shaping amplifier.

The spectrum of a pulser is shown in Figure 4. The x-axis is scaled to units of input charge (electrons) using a calibration of 38 mV/fC. The peak is well fit to a gaussian function with a width of 869 electrons Full Width Half Maximum (FWHM). Corrected for noise pick-up from the PC, the true noise is reduced to 716 e FWHM. This is

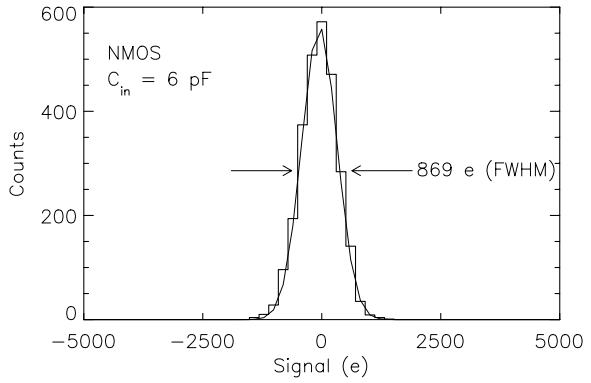

Fig. 4. Pulse-height histogram of an NMOS channel with a 36 fC input pulse. The histogram is plotted relative to the peak position on an x-axis scale in units of input charge.

equivalent to 2.1 keV FWHM using a germanium detector as a signal source, 2.6 keV FWHM in Silicon, or 3.6 keV FWHM in CdZnTe.

The noise slope of the NMOS and PMOS channels were measured by adding capacitance to ground to the front end of the preamplifier. A parasitic capacitance of 6 pF from the test board was measured and is included in the analysis. The measured noise is corrected for the estimated noise contribution from the PC. Results are summarized in Table 1 and plotted in Figure 5. These results are in general agreement with previously published results on the NRL-1 series of chips [4]. The noise slope of the NRL-4 series is slightly larger than for NRL-1. This may be attributed to minor changes in biasing of the front-end MOSFET.

TABLE 1
Noise slope measurements

	Noise (0 pF) e rms	Slope (e/pF)
PMOS	190	38.6
NMOS	205	14.6

III. CONCLUSIONS

The dynamic range of the NRL-4 chip set corresponds to an energy range in germanium of roughly 12 keV–1.2 MeV with an over-all linearity is better than ±0.2%. The low end of the dynamic range is limited by noise and some small head-room necessary for the PDH to function. Energy resolution of 2.1 keV FWHM should be possible using a germanium strip detector with a good design to minimize parasitic capacitance (assumed to be ~6 pF). This energy range and performance should already be adequate in a number of applications such as large area coded-aperture or Compton imaging systems built around an array of strip detectors.

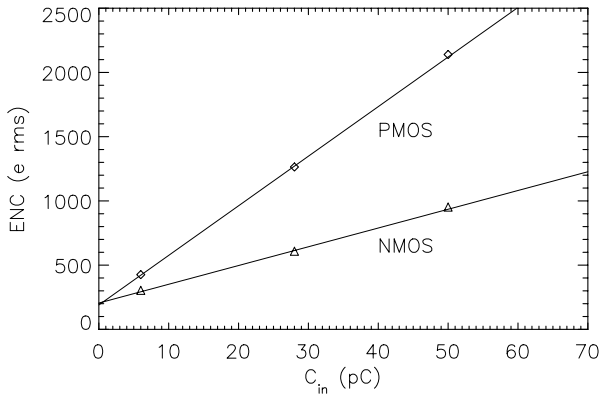

Fig. 5. System noise as a function of input capacitance (noise slope) measured for both the PMOS and NMOS channels.

Although this performance is already good enough for many applications, better energy resolution is still useful for measuring narrow lines, Doppler broadening and background rejection. The potential of germanium detectors to deliver sub-keV resolution demands lower noise electronics. Energy resolution can be improved by averaging signals from both detector faces [1]. With the NRL-4 electronics, energy resolution obtained using signals from both sides of the detector should be ~1.6 keV FWHM. Cooling the CMOS chips has also been demonstrated to reduce noise in previous work [4]. Another approach is to increase the preamplifier power consumption, thus increasing the transconductance of the front end MOSFET.

The next generation chip set is planned to combine both polarity inputs in a single front-end, and to include both the amplifier stages and the PDH circuit on a single multi-channel chip with a multiplexed output.

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