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HIGH DIELECTRIC CONSTANT OXIDES FOR ADVANCED MICRO-ELECTRONIC APPLICATIONS

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14. ABSTRACT

A series of mixed oxide compounds have been manufactured and studied with a view to assessing their suitability for applications in advanced microelectronics: ZrO_2, Ta_2O_5, $LaAlO_3$, Sm_2O_3, Pr_2O_3, Nd_2O_3, TiO_2, $Ti_xSi_{1-x}O_2$. Although each material has distinct advantages, particularly in terms of the magnitude of the dielectric constant, none of those studied can satisfy all of the requirements for thin films on Si. Consideration of the situation likely to arise under real technological conditions leads us to conclude that there are major issues still to be resolved, if indeed they can, if the goals outlined in the semiconductor roadmap for 2016 and beyond are to be attained.

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high dielectric constant, high-k, ZrO_2, Ta_2O_5, $LaAlO_3$, Sm_2O_3, Pr_2O_3, Nd_2O_3, TiO_2, $Ti_xSi_{1-x}O_2$, semiconductor technology

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Introduction

The International Technology Roadmap for Semiconductors[1] (ITRS) has clearly outlined the evolution of micro-electronics technology out to the time scale of ~ 2018. However, improvement in device performance and density of packing will clearly be achieved at the expense of some serious physical difficulties. One specific area relates to the dielectrics used in both the gates of metal oxide silicon field effect transistors (MOSFETs) and in the capacitors of memory cells of dynamic random access memories (DRAMs) and is the primary subject of this contract. To situate the problem we examine the evolution of the gate oxide thickness of MOSFETs as a function of time (often referred to as technology "node"). This data is summarized in Table I and is extracted directly from the ITRS.

Year	2007	2010	2013	2016
Technology Node	65	45	32	22
Printed Gate Length	35	25	18	13
Gate oxide Thickness	1.2	0.9	0.8	0.7

Table I. ITRS requirements for MOSFET gate length and oxide thickness for appropriate scaling with technology generation. Units are nm.

Note that the gate oxide is, for convenience, assumed to be SiO_2. If one bears in mind that in SiO_2, the Si-Si physical distance is ~ 0.3 nm then one concludes that ultimately, a dielectric film approximately 2 monolayers thick is anticipated. In such thin layers direct charged carrier tunneling is possible[2] leading to unacceptable levels of "gate leakage

current" which appear as a parasitic off current so that the device on/off ratio is severely impacted (essentially represented by I_{on}/I_{gate})

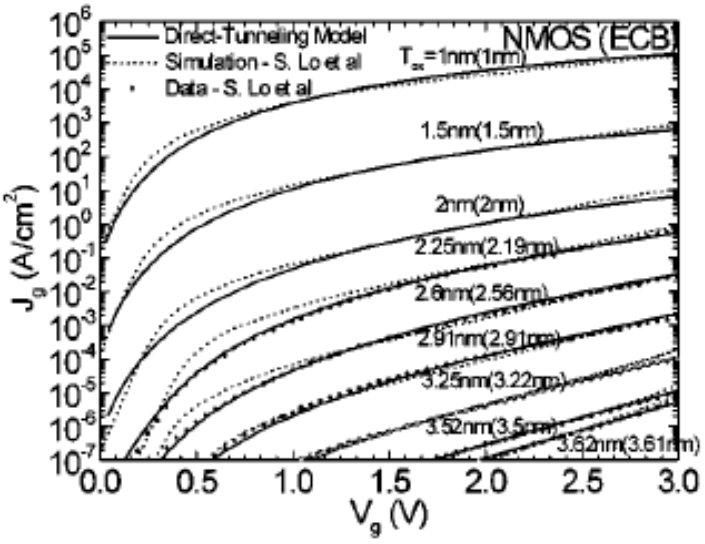

Figure 1. Calculated and measured variation of the leakage current density in thin SiO_2 films

Figure 1. shows the results of calculation and measurement of the direct tunneling leakage current as a function of gate voltage in thin SiO_2 films taken from reference 2. It should be noted that the anticipated operating voltages described by the ITRS are 0.8-1.1V (2007), 0.7-1 V (2010) and 0.5-0.8 V (2016). Using the 2010 data as an example, in 2010 the oxide thickness will be slightly less than 1 nm (Table 1.) so that even for the lowest operating voltage (0.7 V), the leakage current due to direct tunneling is ~ 10^3 A cm^{-2}. The consequences of this leakage are twofold. High leakage currents give rise to circuit heating and loss of reliability and they impact the effective device on current to off current ratio. The latter effect is demonstrated in Figure 2.

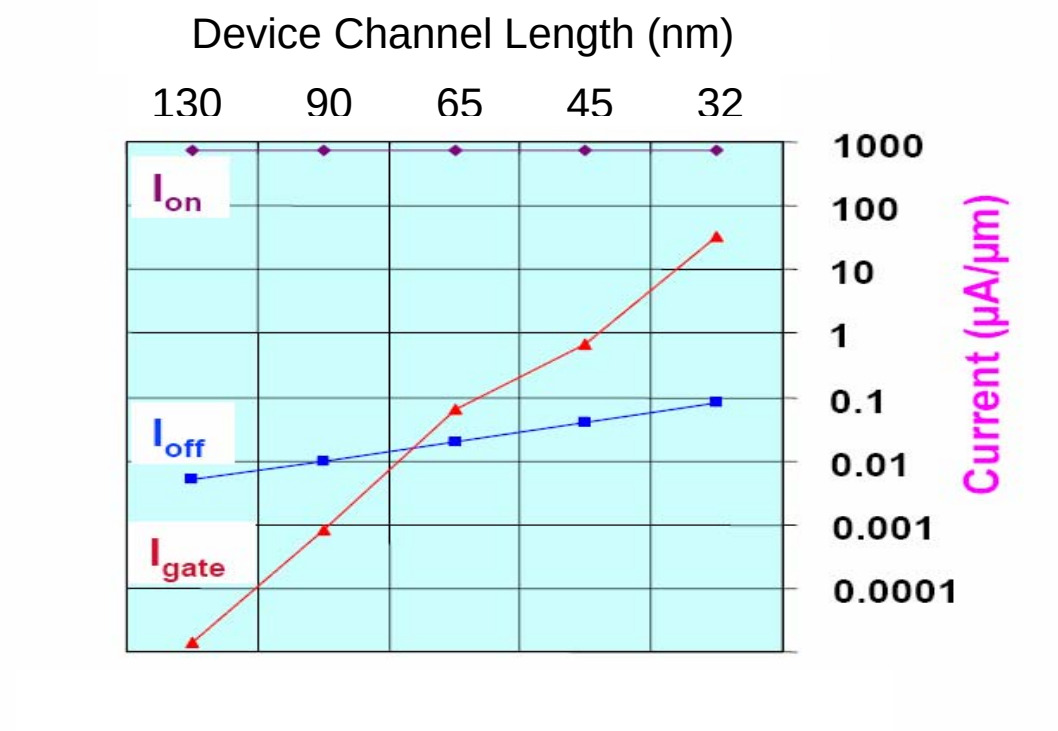

Figure 2. Anticipated variation of the various MOSFET currents as a function of device channel length. Note that the gate leakage current dominates the off current for device channel lengths shorter than ~ 65 nm.

The increase in leakage current resulting from the gate oxide thickness reduction leads, then, to unacceptable on/off ratios and power dissipation in the circuit even in the so called "off mode". The ITRS anticipates combating these undesirable effects by using alternative dielectrics to replace SiO_2 in the gate capacitance, C, and the simple philosophy applied is:

$$C_{SiO2}/C_{alternative} = (\varepsilon_{SiO2}/d_{SiO2})/(\varepsilon_{alternative}/d_{alternative}) \quad (1)$$

Where the d's are the dielectric thicknesses and the ε's are the relative dielectric constants. In other words, the same gate dielectric capacitance values can be obtained by maintaining the same ε/d ratio. Since the leakage current can be assumed to decrease exponentially with the thickness of the dielectric, a dramatic reduction in

leakage current can be obtained. However, this requires a commensurate increase in dielectric constant as shown in Equation 1. and therein lies the difficulty. It must be further stressed that it is not sufficient to simply replace the SiO_2 dielectric film by a thicker one of a material having an appropriately larger dielectric constant, other physical considerations come into play:

a) the material must be thermodynamically stable when in contact with Si and this throughout all the processing steps involving relatively high temperatures (say up to 1050 °C).
b) the optical bandgap and band offsets much be such as to minimize the possibility of charged carrier injection into the conduction band/valence band of the dielectric either from the gate electrode material or from the Si substrate.
c) the inherent carrier conduction through the dielectric film (typically Poole-Frenkel conduction) must be low enough so as to not introduce high levels of electrical leakage.
d) if the dielectric is polycrystalline, electrical leakage along grain boundaries must be insignificant
e) the interface between the Si substrate and the dielectric much be such as to result in a very low density of interface states (say $< 2 \times 10^{10}$ states cm^{-2} eV^{-1})
f) the process used to deposit the dielectric must be compatible with industrially based technological “practices”

and other parameters may need to be addressed. The choice of a material is clearly non-trivial and one rapidly concludes that the periodic table of the elements, at least for binary oxides, is severely limited.

The purpose of the present contract was therefore to try to address some of the aforementioned issues. Furthermore, when reflecting upon potential military usage, the question must be asked “how would the materials chosen behave when subjected to the very special requirements such as radiation hardness for space based operation ?.”

Experiment

One of the criteria elaborated above concerned “compatibility with industrial processes”. Though this may at first sight appear trivial, it is important when developing “new” materials to bear in mind that the material must be able to be manufactured using industrially acceptable methods. For a dielectric film these methods could include a) simple oxidation of a metal/semiconductor, b) deposition by chemical vapor based methods (cvd, plasma enhanced cvd), c) physical vapor deposition (pvd) d) sputtering, e) pulsed laser deposition (pld), etc. It must be further born in mind that industrial choice will also favor a batch processing technique as opposed to a wafer by wafer method. In consequence, technologies typically developed in an academic environment where throughput and complexity are not necessarily considerations may not be deemed industrially acceptable. In the work performed in the context of the present contract, we concentrated on developing commercially viable deposition methods using two principal techniques, low pressure plasma assisted chemical vapor deposition and sputtering. For the purposes of comparison of our experimental results with those of other researchers we also employed electron beam evaporation and pulsed laser deposition methods though for a very limited range of materials.

The plasma enhanced chemical vapor technology (industry compatible) adopted in this contract had the specific novelty of being operational at relatively low pressures. Typically the reactor operated with a plasma at a pressure of a few millitorr unlike common cvd/plasma enhanced cvd reactors which generally operate in the tens to

hundreds of millitorr pressure range. There are clear advantages to using such a low pressure reactor where source gases are concerned. Relatively few useful gaseous sources for metallic atoms (such as WF_6 or SiH_4 for example) exist which could be used to produce dielectrics of interest and one is therefore lead to metal organic materials. Examples of these are tantalum ethoxide ($Ta(C_2H_5O)_5$) for Ta_2O_5 and zirconium or hafnium tetra-butoxide ($Zr/Hf(C_4H_9O_4)$) for HfO_2 or ZrO_2. Given the relatively low vapor pressure at modest temperatures (0.1 torr for tantalum ethoxide at 120 C for example), higher pressure reactors typically require both heating of the evaporative source and of the delivery lines channeling the evaporated gas to the reactor body to avoid recondensation. However, for our reactor operating in the low millitorr regime, such metalorganic sources had an adequate vapor pressure even at room temperature or at slightly higher temperature (< 100 C). Furthermore, where concerns about potential carbon pollution from the source gas were considered, the possibility to use alternative non-carbon containing sources (TaF_5 for Ta_2O_5 or $TiCl_4$ for TiO_2) was exploited.

The unique reactor used in the present study was comprised of a cylindrical chamber into which 6 uniformly distributed microwave antennas were introduced via a top plate. Each antenna contained an $SmCo_6$ based permanent magnet at its end which provided a continuous magnetic field such that an electron cyclotron resonance condition was established along the antenna thereby enabling a plasma to be excited in the few millitorr pressure regime. The antennas were fed from a 2.45 GHz magnetron source with typical operating powers of 600 W (100 W per antenna). The substrate holder, placed ~ 12 ” below the top plate, could be excited with a 13.6 MHz radio frequency source so as to provide a potential bias to assist deposition by ion bombardment. The top plate also housed a commercial magnetron sputtering source (TORUS 2) which could be used to simply sputter targets placed within it. This source was also fed from an RF generator but one independent of that used for substrate bias.

The primary activity outside the domain of deposition involved extensive characterization of the physical and electrical properties of the films obtained. A large variety of methods was employed including infrared absorption spectroscopy, Rutherford backscattering, energy dispersive X ray scattering, single wavelength ellipsometry, atomic force microscopy, glancing incidence X ray scattering and capacitance versus voltage and current versus voltage. The latter measurements give us direct access to the parameter of prime interest, the dielectric constant of the thin film.

Results

Over the duration of this contract a very significant number of materials has been investigated and the results obtained have been the subject of both numerous publications in the public domain and frequent progress reports. We will not, therefore, discuss detailed individual results but present them in a tabular form followed by a short commentary on each system. For more detailed information the reader's attention is drawn to the extensive publications list presented at the end of this report and to the extensive series of progress reports submitted during the tenure of this contract.

The philosophy used in studying these materials was to reconcile our results obtained frequently by plasma assisted deposition techniques with those obtained by other authors frequently using such deposition methods as electron beam evaporation, a technique not considered viable for technological purposes since it frequently results in films containing large numbers of point defects resulting from slight substoichiometry. For example, e-beam evaporation of using a Ta_2O_5 source target usually results in films of stoichiometry Ta_2O_y where $y < 5$ indicating some oxygen loss.

Material	Deposition Method	Structure	Dielectric Constant	Comments
ZrO_2	PECVD	Amorphous	19	Reacts with Si at low T Defect charging
Ta_2O_5	PECVD	Amorphous Crystallized	25 53	Small band gap Large leakage currents
$LaAlO_3$	Sputtering Plasma ass. Oxidation	Amorphous Amorphous	15 13	 Oxidation of sputtered LaAl
	Electron beam	Amorphous	13	Single crystal as source
Sm_2O_3	Pulsed Laser	Amorphous	15	Sm_2O_3 target
Pr_2O_3	Electron beam	Amorphous Crystalline	15 27	Pr_6O_{11} source recrystallized e-beam evap
Nd_2O_3	Electron beam	Amorphous Crystalline (cubic) Crystalline (hex.)	11-12 13-15 27	 recrystallized e-beam evap
TiO_2	PECVD	Amorphous Crystalline Crystalline	30 80 117	Small bandgap Anatase phase Rutile phase
$Ti_xSi_yO_2$	PECVD	Amorphous	3.9-30	

All of these materials are suspected to react with Si at moderate temperatures and their use, therefore, is questionable.

Table II Synopsis of principal dielectric constant results for materials studied throughout this contract.

. The following is a sequence of comments relating to the quality of the films obtained and their applicability to technological applications.

ZrO_2 isomorphic with HfO_2, has $\varepsilon < 20$ in the amorphous phase and 26 in the crystalline. Contains high density of negative and positive charge traps. Recrystallizes

at low temperatures (< 600 C) but interacts then with Si. Large leakage currents due to grain boundary effects.

Ta_2O_5 good ε in the amorphous phase but low barrier (< 1 eV) to charge injection from Si. Interacts with Si when recrystallizing to form silicide and SiO_2.

$LaAlO_3$ expected ε ~ 29 in crystalline phase but much lower in amorphous phase. In order to achieve crystalline phase film must be deposited at T > 850 C – not practical technologically. If recrystallized whilst on Si surface it interacts with the Si.

Sm_2O_3 amorphous phase has low ε, tendency to be hygroscopic. Unable to obtain the hexagonal phase which should have a significant dielectric constant (~ 25). As with all rare-earth sesquioxides, tendency to be hygroscopic.

Pr_2O_3 amorphous phase ε too small, crystalline value ~ 27. Interacts with Si and is also hygroscopic.

Nd_2O_3 amorphous phase has low ε, difficult to stabilize crystalline phase, exists as both cubic and hexagonal, hygroscopic

TiO_2 amorphous phase ε ~ 30 and much higher if crystallized but band offset and band gap too small to be useful. Reacts with Si to form silicide and oxide.

$Ti_xSi_yO_2$ ε can be "tuned" by varying Ti concentration. To attain a satisfactory value for ε requires ~ 50%Ti, 50% Si. Suspect this Ti concentration is too high and will react with the Si substrate.

Conclusions and suggestions

None of the materials studied during the course of this contract emerge as clear solutions for the dilemma of finding a direct replacement for SiO_2 with a dielectric

constant > 20. However, by studying the variation of the dielectric constant as a function of the crystalline or amorphous phase structure we have found very clear evidence for the extremely important role played by network density. It is clear that large ε values can only be obtained from crystallized, dense phases of materials. This requirement poses significant difficulties since crystallization generally occurs at high temperatures where interaction of the film material with the underlying Si may occur. Furthermore, crystallized films are composed of nano or microcrystalline particles which lead to electrical leakage current paths along the grain boundaries and potentially hazardous surface roughness.

Intermediate solutions proposed by industry which address many of the issues mentioned in the introduction- for example ($Hf_xSi_yO_2$), have ε values ~ 10 – 11 and it is relatively simple to demonstrate that these materials will not respond to long term issues. Of primary concern is the problem of avoiding the formation of an interfacial SiO_2 layer during the process of manufacture of the high ε dielectric. Almost all conventional deposition methods will lead to the formation of some interfacial oxide and the capacitor formed by this oxide in series with the high ε material will lower the effective, average dielectric constant. Figure 3 is instructive in demonstrating this effect.

In Figure 3. each line corresponds to a different interfacial SiO_2 thickness: red – 0.3 nm, green – 0.2 nm, blue – 0.1 nm and black – 0 nm. The two sets of lines are for ε = 12 (highest slope set) and ε = 25 (the lowest slope set). To understand this figure one realizes that for any chosen thickness of high ε dielectric, as the SiO_2 thickness increases, the effective oxide thickness (EOT) increases since:

$$EOT = t_{SiO2} + t_{dielectric} \times 3.9/ \varepsilon. \qquad (2)$$

Note that in Table I. We quote “gate oxide thickness” in terms of the required thickness assuming it to be SiO_2. This is, of course, physically unreasonable for the reasons shown in Figures 1 and 2. and because the required thickness becomes of the scale of mono layers. We thus talk about the effective oxide thickness as defined in Equation 2.

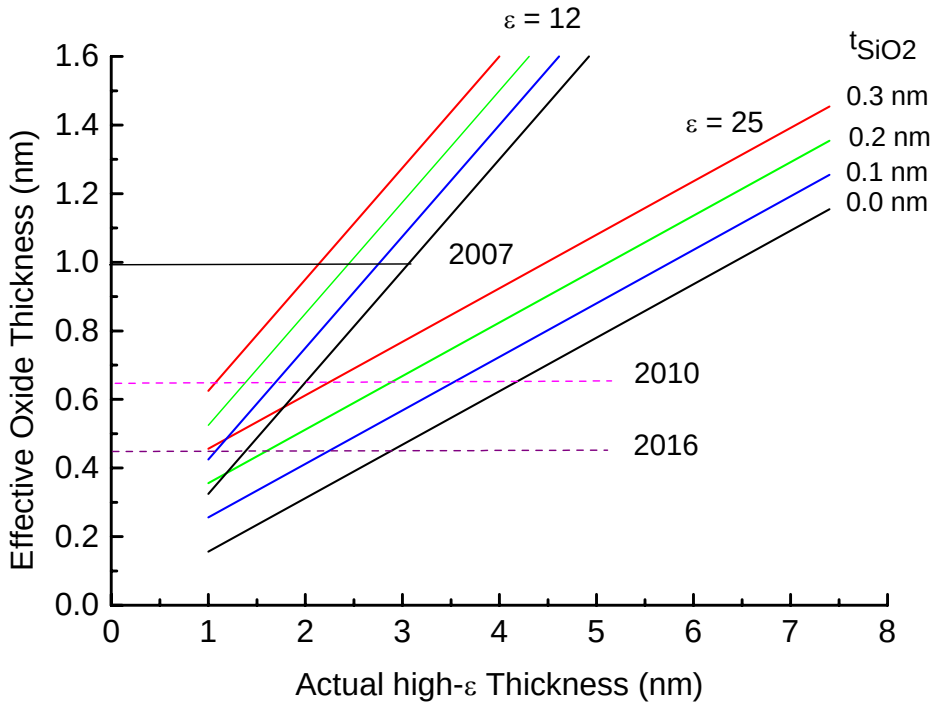

Figure 3. The influence of a thin SiO_2 linterfacial layer on the effective oxide thickness of the composite high ε dielectric /SiO_2 sandwich. The lines corresponding to 1, 0.65 and 0.45 nm are the industrial target values for the years 2007, 2010 and 2016 respectively.

Therefore, if we require an EOT ~ 1 nm (see Table 1) in 2007, this can be achieved by using a material with ε = 12 and $t_{dielectric}$ ~ 3 nm assuming there is no interfacial SiO_2 layer. If there were one monolayer (~ 0.3 nm) of SiO_2, then the high ε film would need to be ~ 2 nm. One must furthermore bear in mind that there is a

technological limit in manufacturing ultra thin high ε films which is probably ~ 1.5 nm and it is likely that leakage current in such thin, deposited films (Poole Frenkel mediated) will become excessive.

Examination of Figure 3. for the case of the 2016 industrial target indicates an EOT of 0.45 nm and clearly shows that if there is **any** interfacial SiO_2, the required EOT will not be attainable with ε = 12 material. For this reason, $Hf_xSi_yO_2$ is **not** a medium to long term solution. Even if we consider the data in Figure 2. for ε = 25, and we set the minimum manufacturable high ε film thickness to be 1.5 nm, we still cannot meet industrial requirements if the interfacial SiO_2 layer thickness > 0.2 nm, i.e. less than a monolayer !

The challenges in high ε materials remain clear. Above we listed 6 requirements which need to be met by the "ultimate" high ε dielectric, we can now add 3 more: a) one must be able to deposit low leakage films ≥ 1.5 nm thick, b) the interfacial SiO_2 film thickness must be essentially inexistent or of the order of a monolayer and c) the ε value must be > 25. We have successfully added to the complexity of the problem but failed, as others, to find an appropriate high ε solution. Furthermore we have still not addressed the very pertinent issues of long term electrical reliability of the films and their radiation hardness. These issues will need to be addressed when a clear candidate high ε dielectric becomes available.

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