P-type SiGe/Si Superlattice Cooler

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ABSTRACT

The fabrication and characterization of single element p-type SiGe/Si superlattice coolers are described. Superlattice structures were used to enhance the device performance by reducing the thermal conductivity between the hot and the cold junctions, and by providing selective emission of hot carriers through thermionic emission. The structure of the samples consisted of a 3 μm thick symmetrically strained $Si_{0.7}Ge_{0.3}$/Si superlattice grown on a buffer layer designed so that the in-plane lattice constant is approximately that of relaxed $Si_{0.9}Ge_{0.1}$. Cooling up to 2.7 K at 25 °C and 7.2 K at 150 °C were measured. These p-type coolers can be combined with n-type devices that were demonstrated in our previous work. This is similar to conventional multi element thermoelectric devices, and it will enable us to achieve large cooling capacities with relatively small currents.

INTRODUCTION

Effective cooling is essential for many high power or low noise electronic and optoelectronic devices. Thermoelectric (TE) refrigeration is a solid-state active cooling method with high reliability. Unlike conventional air-cooling, it can spot cool discrete or localized devices and reduce the temperature of the device below ambient. For a material to be a good thermoelectric cooler, it must have a high value of the dimensionless figure of merit ZT [1] which is given by $ZT=S^2\sigma T/\kappa$, where S is the Seebeck coefficient, σ is the electrical conductivity, T is the temperature, and κ is the thermal conductivity. The use of quantum-well structures to increase ZT was proposed by Hicks and Dresselhaus [2]. Since then much work has been done in the study of superlattice thermoelectric properties, mostly for the in-plane direction [3-6]. The physical origin of the increase in ZT comes mainly from the enhanced density of electron states due to the reduced dimensionality. Recent study shows that superlattice thermal conductivity of cross-plane direction is even lower than that of in-plane direction [7], which can further increase ZT. In addition, Shakouri and Bowers proposed that heterostructure could be used for thermionic emission to enhance the cooling [8]. Large ZT improvement is possible for the cross-plane transport [9, 10].

SiGe is a good thermoelectric material especially for high temperature applications [11]. Superlattice structures can enhance the cooler performance by reducing the thermal conductivity between the hot and the cold junctions [7, 12], and by selective emission of hot carriers above the barrier layers in the thermionic emission process [8, 9]. N-type SiGe/Si cooler was reported in our previous work [13]. In this paper, single element p-type SiGe/Si superlattice coolers with

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electrical transport in the cross-plane direction is demonstrated. This paves the road to make n-type and p-type superlattice coolers electrically in series and thermally in parallel, similar to conventional TE coolers, and thus achieve large cooling capacities with relatively small currents.

MATERIAL AND DEVICE FABRICATION

The p-type SiGe/Si superlattice cooler sample was grown with molecular beam epitaxy (MBE) on a five-inch diameter (001)-oriented Boron doped Si substrate with resistivity less than 0.006 Ω-cm. The cooler's main part is a 3 μm thick $200\times$ (5 nm $Si_{0.7}Ge_{0.3}$/10 nm Si) superlattice grown symmetrically strained on a buffer layer designed so that the in-plane lattice constant was approximately that of relaxed $Si_{0.9}Ge_{0.1}$. The buffer layer consisted of 1 μm $5\times$ (150 nm $Si_{0.9}Ge_{0.1}$/50 nm $Si_{0.845}Ge_{0.150}C_{0.005}$) and 1 μm $Si_{0.9}Ge_{0.1}$. Both the superlattice and the buffer layer are doped to 5×10^{19} cm^{-3} with Boron. 0.5 μm thick $Si_{0.9}Ge_{0.1}$ cap layer was grown on the superlattice with the top 0.25 μm doped to 2×10^{20} cm^{-3} to achieve good ohmic contact. The $Si_{0.7}Ge_{0.3}$/Si superlattice has a valence band offset of about 0.2 eV [14], and hot holes over this barrier produce thermionic cooling. In addition, superlattice structure has many interfaces that increase phonon scattering, and therefore gets lower thermal conductivity. The material growth procedure is similar to that of n-type SiGe/Si superlattice, described in reference [13]. A transmission electron microscopy (TEM) image of the grown p-type SiGe/Si superlattice cooler sample is shown in figure 1.

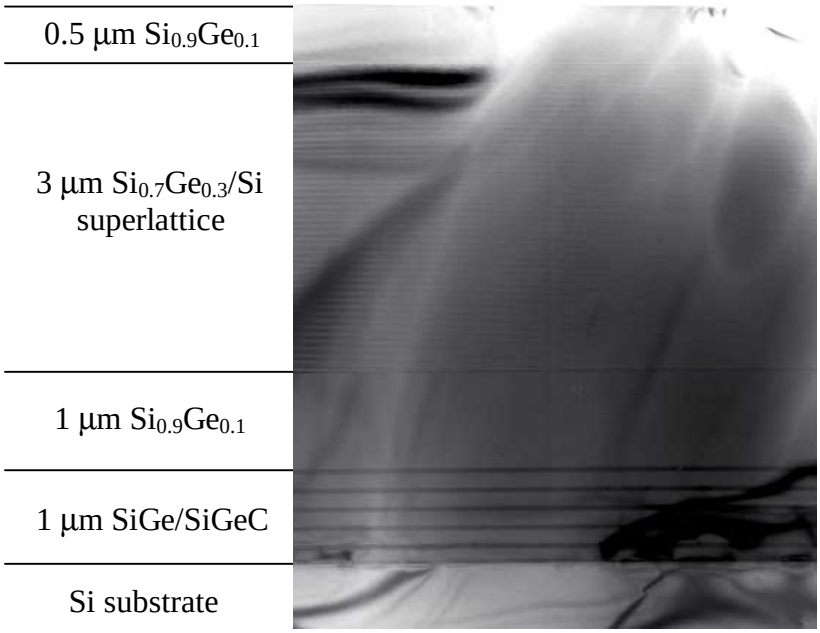

Figure 1*. TEM image of the p-type SiGe/Si superlattice cooler sample*

For the cooler device fabrication, mesas with an area of 50×50 μm^2 were etched down to the $Si_{0.9}Ge_{0.1}$ buffer layer using reactive ion etching. Metallization was made on the mesa and

$Si_{0.9}Ge_{0.1}$ buffer layer for top and bottom contact respectively. Electrical current goes from the top contact to bottom contact for cooling. This is a cross-plane transport in the superlattice. To reduce contact resistance and facilitate wire bonding, Ti/Al/Ti/Au was used for contact metallization. Annealing was accomplished at 450 °C, and specific contact resistance of 3.6×10^{-7} Ω-cm^2 was measured.

TEST RESULTS AND DISCUSSIONS

The p-type SiGe/Si superlattice coolers were tested on a temperature controlled copper plate that worked as the heat sink. The cooling area of the single element device is 50×50 μm^2. The device cooling temperatures were measured with micro thermocouples, and they are relative to the device temperature at zero current. Figure 2 shows the measured cooling temperature versus current with the heat sink at 25 °C. Cooling up to 2.7 K with respect to the heat sink was obtained, corresponding to cooling power densities on the order of 100 W/cm^2 at zero delta T.

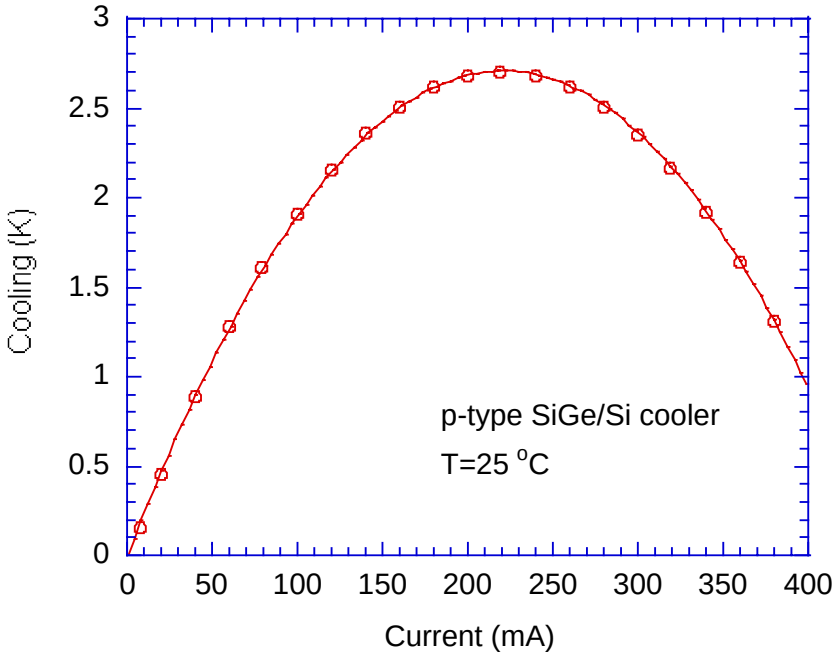

***Figure 2**. Measured cooling of p-type SiGe/Si superlattice cooler at 25 °C (heat sink). The dots are measured data and the line is their quadratic fitting curve.*

The device cools better at higher temperatures. The measured cooling of the 50×50 μm^2 p-type SiGe/Si device at 150 °C (heat sink temperature) is shown in figure 3. The maximum cooling increased from 2.7 K at 25 °C to 7.2 K at 150 °C. The reason for the improved performance with the increase in temperature is two fold. First, in the temperature range of our measurements, the figure of merit ZT of SiGe alloy increases with temperature due to smaller thermal conductivity and larger Seebeck coefficient [15], and second, the thermionic emission cooling power increases due to the larger thermal spread of carriers near the Fermi energy.

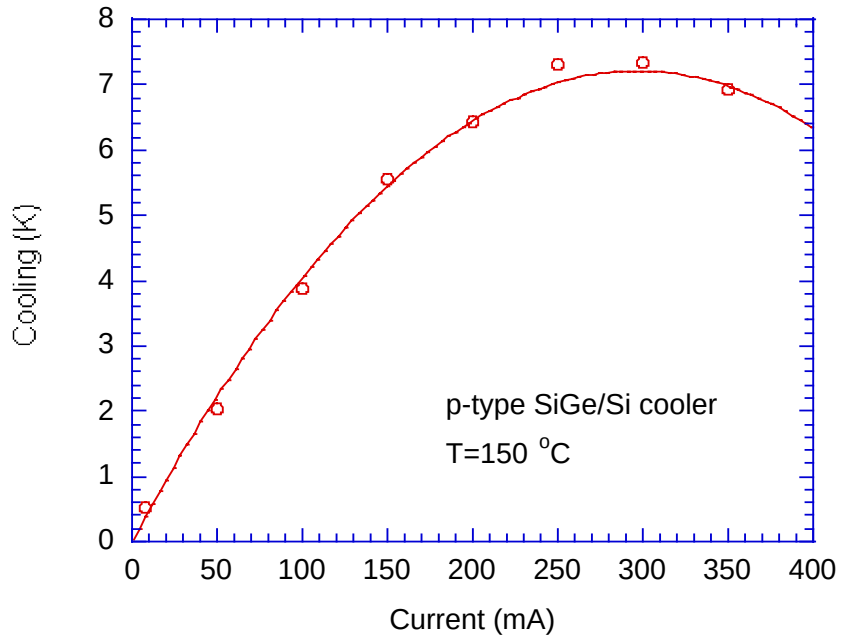

Figure 3*. Measured cooling of p-type SiGe/Si superlattice cooler at 150 ℃ (heat sink). The dots are measured data and the line is their quadratic fitting curve.*

Since the devices here are single element superlattice coolers, heat conduction to the cooling side from the bonding wires or probes are unavoidable. This reduces the maximum cooling. To solve this problem, n-type and p-type SiGe/Si superlattice coolers can be made in an array format electrically in series and thermally in parallel, similar to conventional thermoelectric coolers. In this way, both electrical terminals can be made at the heat sink side, and large cooling capacities can be achieved with relatively small currents. With optimized superlattice material and device design and packaging, cooling up to tens of degrees is possible. More important, the processing of SiGe/Si superlattice coolers is compatible with that of very-large-scale-integration (VLSI) technology, thus it is possible to integrate these coolers monolithically with Si and SiGe devices to achieve compact and efficient cooling.

CONCLUSIONS

P-type SiGe/Si superlattice cooler was demonstrated. Cooling up to 2.7 K at 25 °C and 7.2 K at 150 °C was obtained, corresponding to cooling power densities of hundreds of watts per square centimeter at zero delta T.

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REFERENCES

1. H. J. Goldsmid, *Thermoelectric Refrigeration* (Plenum, New York, 1964).
2. L. K. Hicks and M.S. Dresselhaus, *Phys. Rev. B*, **47**, 12727 (1993).
3. P. J. Lin_Chung and T. L. Reinecke, *Phys. Rev. B*, **51**, 13244 (1995).
4. R. Venkatasubramanian, E. Siivola, and T. S. Colpitts, *Proceedings of the 17th International Conference on Thermoelectrics*, 191 (1998).
5. T. Koga, T. C. Harman, S. B. Cornin and M. S. Dresselhaus, *Phys. Rev. B*, **60**, 14286 (1999).
6. T. Koga, X. Sun, S. B. Cronin and M. S. Dresselhaus, *Appl. Phys. Lett.*, **75**, 2438 (1999).
7. G. Chen, S. Q. Zhou, D.-Y. Yao, C. J. Kim, X. Y. Zheng, Z. L. Liu and K. L. Wang, *Proceedings of the 17th International Conference on Thermoelectrics*, 202 (1998).
8. A. Shakouri and J. E. Bowers, *Appl. Phys. Lett*., **71**, 1234 (1997).
9. A. Shakouri, C. Labounty, P. Abraham, J. Piprek, and J. E. Bowers, *Material Research Society Symposium Proceedings*, **545**, 449 (1999).
10. L. W. Whitlow and T. Hirano, *J. Appl. Phys*., **78**, 5460 (1995).
11. C. B. Vining, *J. Appl. Phys.*, **69**, 331 (1991).
12. S.-M Lee, D. G. Cahill and R. Venkatasubramanian, *Appl. Phys. Lett.*, **70**, 2957 (1997).
13. G. Zeng, A. Shakouri, C. LaBounty, G. Robinson, E. Croke, P. Abraham, X. Fan, H. Reese and J. E. Bowers, *Electronics Letters*, **35**, 2146 (1999).
14. R. People and J. C. Bean, *Appl. Phys. Lett*., **48**, 538 (1986).
15. J. P. Dismukes, L. Ekstrom, E. F. Steigmeier, I. Kudman and D. S. Beers, *J. Appl. Phys.*, **35**, 2899 (1964).