Experimental Investigation of Thin Film InGaAsP Coolers

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ABSTRACT

Most optoelectronic devices for long haul optical communications are based on the InP/InGaAsP family of materials. Thin film coolers based on the same material system can be monolithically integrated with optoelectronic devices such as lasers, switches, and photodetectors to control precisely the device characteristics such as wavelength and optical power. Superlattice structures of InGaAs/InP and InGaAs/InGaAsP are used to optimize the thermionic emission resulting in a cooling behavior beyond what is possible with only the Peltier effect. A careful experimental study of these coolers is undertaken. Mesa sizes, superlattice thickness, and ambient temperature are all varied to determine their effect on cooling performance. A three-dimensional, self-consistent thermal-electric simulation and an effective one-dimensional model are used to understand the experimental observations and to predict what will occur for other untested parameters. The packaging of the coolers is also determined to have consequences in the overall device performance. Cooling on the order of 1 to 2.3 degrees over 1-micron thick barriers is reported.

INTRODUCTION

Thermoelectric (TE) coolers have encountered widespread use in the temperature stabilization of optoelectronic components (lasers, switches, detectors, etc.) in high speed and wavelength division multiplexed (WDM) fiber optic communication systems. This is even more so in dense WDM systems where the spacing between adjacent wavelengths can be from 0.8nm (100GHz) to as small as 0.2nm (25GHz) [1]. Since typical InGaAsP-based DFB lasers operating around 1.55 μm have a wavelength drift of approximately 0.1 nm/°C, the temperature must be controlled to less than a degree of variance to prevent excessive loss in multiplexers / demultiplexers or crosstalk interference. While TE coolers have successfully met this requirement, they have added greatly to the total cost of components since they are not easily integrated with devices [2].

Another disadvantage to the use of TE coolers is the large mismatch in thermal mass between that of the cooler and the device. The smallest TE coolers are a couple of millimeters squared, whereas a typical optoelectronic device is an order of magnitude smaller.
Much work is currently underway in thin film thermoelectric refrigeration for other applications, however the same problems of integration with optoelectronics still exist. The InGaAsP/InP family of materials has poor thermoelectric properties due to the inherently small Seebeck coefficient [3]. However, the use of thermionic emission in heterostructures was recently proposed and has been demonstrated in the InGaAsP system to increase the cooling power [4,5]

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by selectively emitting only the hot electrons over a heterobarrier. An order of magnitude improvement beyond the bulk Peltier properties is possible [6].

In the following we investigate the behavior of several InGaAsP-based thin film thermionic coolers. A qualitative picture of device operation is constructed, and an effort is made to understand the current device limitations by comparing measurements for various device sizes, thickness, and operating temperatures.

MATERIAL STRUCTURE

The material structures investigated were all n-type. Each was grown by metal organic chemical vapor deposition (MOCVD) on n+ InP substrates and was composed of a superlattice barrier layer surrounded by anode and cathode layers of InGaAs. The anode and cathode layers were 0.5μm and 0.3μm thick respectively. Most of the results presented in this work are for a 25 period superlattice of 10nm InGaAs and 30nm InGaAsP (λ_{gap}=1.3μm). All compositions were grown lattice matched to the InP growth substrate.

FABRICATION & MEASUREMENT

Reactive Ion Etching was used to form mesas ranging in area from 3200 μm^2 to 20,000μm^2. In each case the etching depth was through the top cathode and superlattice layers, stopping in the lower anode region. Ohmic metal contacts were formed by electron-beam deposition of 50Å-Ni / 100Å-AuGe / 1000Å-Ni/ 10,000Å-Au. The contacts were then alloyed by rapid thermal annealing at a temperature of 450°C. The specific contact resistivity was measured on separate characterization samples with the transmission line model [7] and determined to be approximately $5x10^{-7}$ Ω/cm^2. The InP substrate was mechanically lapped to a thickness of 125μm in order to reduce the thermal resistance between the hot side of the cooler and the heat sink. The samples were then cleaved, mounted in packages, and wire bonded for testing.

Micro-thermocouples were used to monitor the temperature of the devices while the current bias was varied. A differential measurement with two thermocouples was used where one is placed on the device and the other on the reference stage. The stage was thermoelectrically controlled to maintain a set heat sink temperature.

EXPERIMENTAL RESULTS & DISCUSSION

It would be useful to begin by discussing qualitatively the device operation. The device can be broken into three regions as shown in figure 1, where the electrical conductivity (σ), thermal conductivity (κ), and area (A) are defined for each region. The equivalent circuit model is shown on the right with the arrows indicating sources or sinks of heat flux. Q_{TI} refers to thermionic heating/cooling, Q_{TE} to thermoelectric cooling (metal-semiconductor interface), and Q_C to heat generation by contact resistance. From circuit analysis, an expression can be found for the temperature at the cold side of the device (between regions 1 & 2). Since the thermal resistance of the wire (R_w) is usually at least an order of magnitude larger than the sum of the cooler and substrate, it is assumed to be zero to simplify the analysis. The resulting expression is,

$$\Delta T = \{(Q_{TI} + Q_{TE})(R_d^{th} + R_{sub}^{th}) - Q_{TI} R_{sub}^{th}\} - \{(\frac{1}{2} R_{Au} + R_C)(R_d^{th} + R_{sub}^{th})\} I^2 \qquad (1)$$

where $R_d{}^{th}$ and $R_{sub}{}^{th}$ are the barrier and substrate thermal resistances, and R_{Au} and R_C are the gold wire and contact electrical resistances respectively. Q_{TE} and Q_{TI} are both linearly proportional to current [4], hence the first term in equation 1 is linearly proportional to current representing the cooling effects, and the second term is proportional to the square of current representing the heating effects. This equation includes all of the important non-ideal parameters such as contact resistance, wire bond heat load, and substrate thermal resistance.

Cooling Vs. Size

Most of the terms in equation 1 are area dependent, and so studying the cooling dependence on device size provides much information about the behavior of the device. Figure 2(a) shows the measured cooling versus current density for several device areas. At low current densities, all the devices operate nearly identically as expected. As the current is increased, the area dependent non-ideal heating becomes apparent. The smallest size device ($5000\mu m^2$) cools best since it requires less current to reach a given current density. Referencing equation 1, the curves in figure 2(a) can be fitted with a second order polynomial and the corresponding linear and quadratic coefficients extracted. Figure 2(b) plots these coefficients versus area. Using equation 1 and the known material properties, the area dependence can be modeled and the device operation understood. In order to develop a more accurate model, the three-dimensional electrical and thermal spreading resistance was simulated for the given geometry. These effective values are used when applying equation one to fit experimental data. In order to replicate the area dependence in figure 2(b), it was necessary to include all of the non-ideal terms

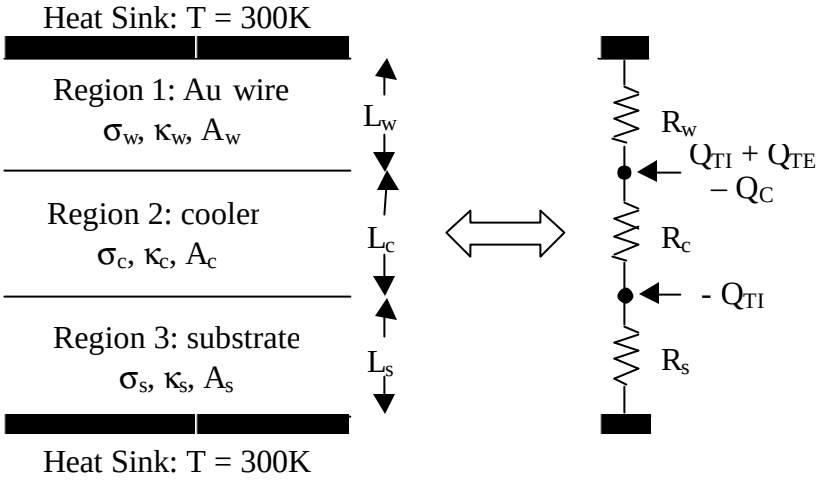
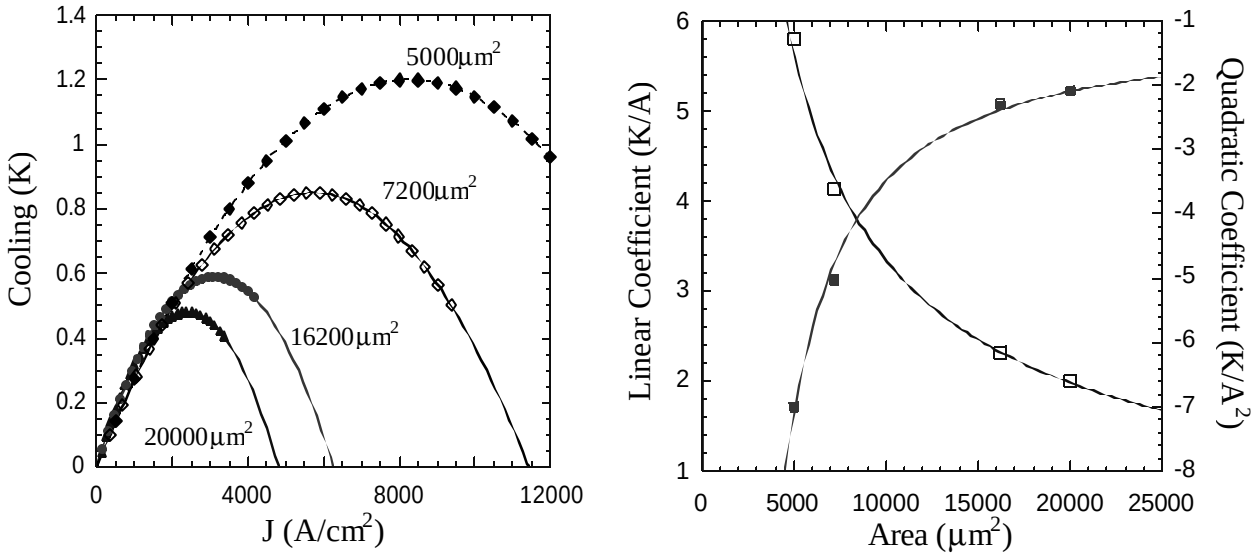


Figure 1. *One-dimensional model and boundary conditions. Electrical conductivity (s), thermal conductivity (k), and area (A), are defined in each region. The equivalent circuit model is shown on the right with the arrows indicating sources or sinks of heat flux.* Q_{TI} *refers to thermionic heating/cooling,* Q_{TE} *to thermoelectric cooling, and* Q_C *to heat generation by contact resistance.*



(a) (b)

Figure 2. ***(a)****Cooling versus current density for several sizes and* ***(b)*** *the corresponding linear (cooling) and quadratic (heating) coefficients from a second order polynomial fit as in equation 1. The points are the experimental values, and the curves are simulated from equation 1. Measurements were performed at 300K.*

from equation 1 indicating that all three (contact resistance, wire bond heat load, substrate thermal resistance) have room for improvement.

There does exist a discrepancy between the model and experimental results. With all the non-ideal parameters included, the simulations predict a performance increase for thicker superlattice barriers. Experimentally, little or no improvement has been observed with thicker devices, however the superlattice barriers differed in each case. A more thorough investigation of cooling for thicker identical superlattice barriers is currently underway.

Cooling Versus Temperature

Ideally the height of the heterobarrier and the Fermi level are engineered to be optimum for a given operating range. All of the devices examined were designed for room temperature operation. The cooling behavior was examined for various heat sink temperatures to determine the effects. Figure 3 shows the cooling versus current bias at different temperatures for a 5000 μm^2 cooler. The observed trend is increased cooling at higher operating temperatures. The origin of the temperature dependence stems from the change in material properties (thermal and electrical conductivity) and in the thermionic and thermoelectric cooling mechanisms. Borrowing from the analogous case of conventional thermoelectrics, the maximum cooling and optimum current can be expressed as [8],

$$\Delta T_{\max} = \frac{1}{2}\frac{(\Phi_B + 2k_B T/e)^2 s}{k} \qquad (2a) \qquad\qquad I_{opt} = \frac{\Phi_B + 2k_B T/e}{R} \qquad (2b)$$

where $(F_B + 2k_BT/e)$ is the effective cooling for the thermionic effect in the limit of Boltzmann statistics [4], s and k are the electrical and thermal conductivity respectively, and R is the electrical resistance. Over the temperature range of interest, the effective cooling is thus approximately $\propto T$ and thermal conductivity $\propto T^{-1.4}$ [9]. The temperature dependence of electrical conductivity is determined by the mobility which is approximately constant over these temperature values since it is mostly dominated by impurity scattering. From equations 2a & 2b the maximum cooling and optimum current are hence roughly proportional to $T^{2.4} + T^{3.4}$ and T respectively. The data points in Figure 3(b) fit very well to these corresponding powers, however we are only looking at a small temperature window and a larger spectrum is needed to confirm the validity of these derivations. For an analysis over a wider temperature range, the dependence of the electrical conductivity will have to be estimated, as well as a more accurate model of the effective cooling using Fermi-Dirac statistics.

Cooling Versus Packaging

The packaging has proven to be an important factor to optimize [10]. The addition of a package between the substrate and heat sink adds another thermal barrier for heat to pass through. Improvements in reducing this added thermal resistance by using silicon or copper packages and by optimizing the length of the wire bond have resulted in a maximum cooling increase greater than 100%. It is believed that the package no longer limits device performance.

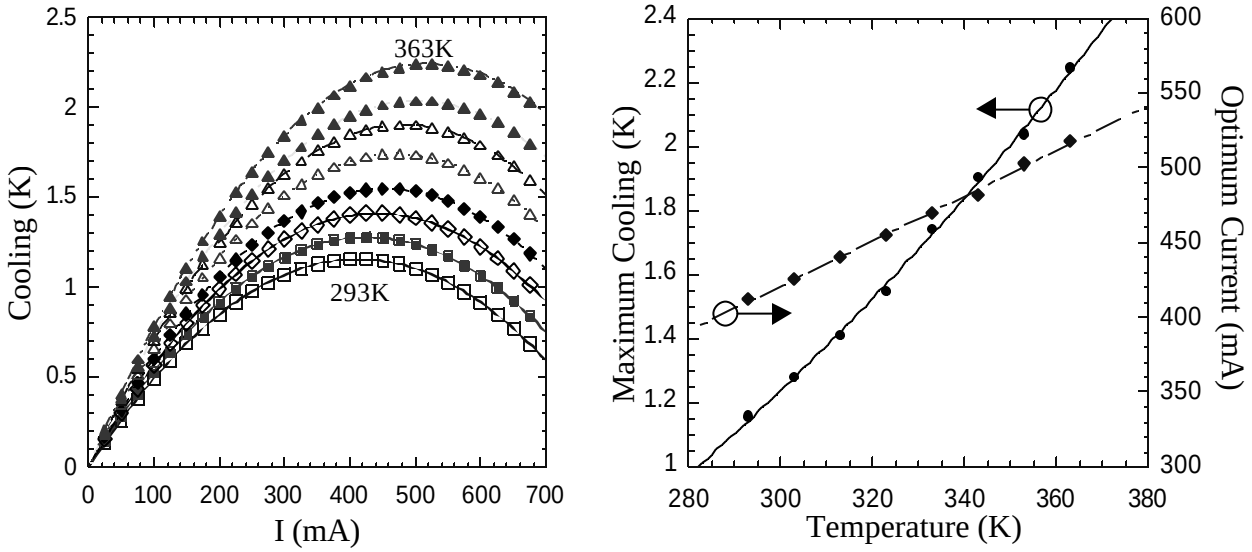


Figure 3. ***(a)****Cooling versus current bias for heat sink temperatures of 293-363K in 10K increments.* ***(b)*** *Corresponding maximum cooling (solid) and optimum current (dashed) versus heat sink temperature. The points are the experimental values and the curves are the theoretical curve fits,* $DT_{max} \mu\ T^{2.4}+T^{3.4}$, $I_{opt} \mu\ T$. *Cooling is measured with respect to the heat sink temperature.*

CONCLUSIONS

A thorough experimental investigation of InGaAsP-based thin film thermionic coolers has been presented. Through modeling of the geometry and temperature dependent cooling, an understanding of device performance has been achieved. It was found that smaller area coolers at higher temperatures performed the best, and 2.3K of cooling was demonstrated at 363K for a 5000 μm^2 size device. This amount of cooling over a 1 μm thick barrier corresponds to cooling power densities of several hundred watts per square centimeter. With further improvements in contact resistance, wire bond heat load, and substrate thermal resistance, maximum achievable cooling is expected to reach tens of degrees for single stage devices. These types of thin film coolers should prove to have far reaching applications in optoelectronic devices where a large cooling power, small thermal time constant, and a low cost alternative to thermoelectric coolers are necessary.

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