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14. ABSTRACT: The Known Good Substrates (KGS) program is on track technically and financially with program tasks. Q4 wafer fabrication will be completed on time, Q4 metrology and characterization was completed, and Q3 wafers were distributed to partners early in Q4. Many subcontractors are ramping down activities as their work nears completion. A full program review meeting was held in December 2006.			
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Q2 Known Good Substrates Technical Report
CONTRACT/PR NO. N00014-05-C-0324 Dow Corning Corporation
Quarterly Technical Report
Reporting Period: 1 September 2006 – 30 November 2006

Executive Summary

The following tables summarize progress against key milestones and metric goals after 9 months of work. The color coding shows red as incomplete milestone or below metric target, yellow as behind schedule or close to metric and green as a completed milestone or achieved metric.

Thrust	Quarter	Milestone
Task 1: SiC Wafer Products	1	50% sliced wafer increase for 76 mm diameter crystals
	2	Complete model of 100 mm PVT growth*
	3	80% sliced wafer increase for 76 mm diameter crystals
	4	Deliver first generation 4H n+ 100mm wafers - DELAYED
Task 2: Materials Applied Research	1	Complete model of Generation1 bulk gas growth
	1	Qualify Batch Epitaxy processes for program
	2	Demonstration of CVT growth*
	4	Deliver first 76mm CVT wafers
Task 3: Metrology for Wafer Specifications	2	Implement LLS inspection with particles, pits, and scratches delineated.
	3	Start routine microwave loss inspection of 4H SI wafers
	2	u-PCD tool installed and lifetime measurements implemented for epitaxy layers and SI wafers
Task 4: Device Technology Maturation	1	Publish Rev-0 roadmap for wafer and epi goals
	2	Complete disposition strategy for n+ epiwafers
	4	Publish revised roadmap to reflect power and RF device progress

Executive Summary

As the end of the calendar year approaches most of the tasks have been completed on schedule. All team members gathered for a progress review in Chicago on December 14, 2006. Data on all tasks were presented except RF device fabrication. Highlights of key learning include micropipe levels for 76 mm 4H n+ wafers dropping to a median of ~25/cm2, beyond the main milestone; PL data showing that the trend of reduction of nitrogen concentration during PVT is within 3x of the level needed for growth SI-4H-SiC wafers; mechanisms for crystal defect propagation and suppression in crystal growth and epitaxy were extracted from x-ray diffraction and topography. Key to the roadmap for 2007 is to eliminate grain boundaries in PVT crystal growth, as these tend to be the defect exacerbating micropipes. A new PVT approach at DCCSS was presented which shows possible capability to eliminate grain boundaries.

While 100mm work was delayed, two boules of sufficient quality to produce wafers were processed and three wafers will be delivered with the third quarter group along with UID

and n+ 76mm 4H wafers. Fourth quarter deliverables have been adjusted per conversations with ONR and will now be almost entirely on axis 76mm 4H n+ SiC wafers.

CVT work progresses and the first 5 mm thick 4H crystal was deposited. This was done in incremental growths to circumvent issues with injector clogs and downstream reactant concentration. Modification of the system to circumvent these problems is underway, but progress is not such to insure delivery of wafers in the first year of the program, hence the condition yellow in the table.

Device wafers sent to NGES for SIT fabrication should be exiting fab and moving to test, with results expected in mid-January. With these results the device roadmap can be completed, and until available this task is listed as condition yellow.

The following table presents the technical progress in the program relative to the metrics projected at the program start:

KGS Program Goal Metrics	**Q3 2006 Status (Program Month 8)**	**Top 30% Goal**	**Top 50% Goal**
Timing for 76 mm diameter	Pilot Production	Q1/06	
Timing for 100 mm diameter	100 mm wafers produced, grain boundary count unsatisfactory level – 6 months behind schedule. Examples provided to ONR.	Q1/07	
MPD and inclusions (cm^{-2})	**MPD Top 50% is <30 cm^{-2}** **MPD Top 30% is <25 cm^{-2}** **Inclusions Top 50% is <40 cm^{-2}**	<10	<30
Scratches (total length), visual inspection	Met Program goal based on Q2 final results	<50% diameter	<75% diameter
Areal density surface particles and pits in epiwafers, diameter >0.5 um	**LLS Pits <10 cm^{-2}** **at diameter >25um** **(test method not mature for <25um)**	<5 cm^{-2}	<10 cm^{-2}
Bulk Metals Contamination B, Al, Ti, V, Fe (atoms/cm^3)	100% is between 1E15 and 5E15	<1E15	<5E15
Stable Epi drift layer carrier concentration (atoms/cm^3)	100% is less than 5E14 (process development)	<1E14	<5E14
Epi thickness uniformity	100% is less than 8%	<8%	<10%
Epi Doping Uniformity (10^{15}-$10^{19}/cm^3$ layers)	Top 60% is <15%; 20% is <10%	<10%	<15%

Most all metrics have been achieved in the program. Current data in Q4 shows that by the end of 2006 the MPD median will emerge below 25/cm2, which should put the overall distribution near the program goal. Improvements in Q3 and Q4 wafers should bring inclusions and pits also very near or at the program objective.

Technical Progress

The following table documents the key program thrusts, milestones by quarter and progress for the activity in the quarter documented by this report. New text, associated with Q4 progress is shown in black.

Thrust	Complete by Quarter	Milestone	Progress
Task 1: SiC Wafer Products	**1**	50% sliced wafer increase for 76 mm diameter crystals	Since Jan 2005 (the anticipated start of the KGS program, about which the goal was projected) the slice wafer yield has increased by 2x.
	2	Complete model of 100 mm PVT growth	Thorough modeling of 76mm was extended one month to insure agreement with all experimental results. 100 mm modeling is underway at both subcontractor and in house. Initial modeling of the heat losses has helped to drive PVT process alterations which resulted in a 3x reduction of growth rate variability in 100 mm PVT processes.
	3	80% sliced wafer increase for 76 mm diameter crystals	Since Jan 2005 (the anticipated start of the KGS program, about which the goal was projected) the slice wafer yield has increased by 2x.
	4	Deliver first generation 4H n+ 100mm wafers	Work on 100mm crystal growth has succeeded to produce crystals of diameter 100mm and length exceeding 25 mm, but crystal stress grain boundary density is undesirable. Recent PVT process development for 76mm diameter crystal growth has yielded new methods to reduce stress and micropipes. DCCSS feels that to achieve the desired quality for 100mm diameter crystals, it is pertinent to go stall the 100mm effort and repeat the crystal expansion work using these new techniques. Three polished wafers will be delivered to ONR to baseline the progress so far in the program.
Task 2: Materials Applied Research	**1**	Complete model of Generation 1 bulk gas growth	Due to delay in release of funds for KGS, Dow Corning funds were used to initiate the modeling project in the second half of 2005. A Gen-1 model has been completed based on one chlorosilane precursor and one set of process conditions. The results show that growth rate and deposition uniformity comparable to PVT processes can be expected over the temperature range 1900-2100 C. At this point it is believed largest source of error in the model is the formation of deposits on ancillary surfaces of the crucible. Additional modeling work was performed to better understand the mechanism for observed ancillary

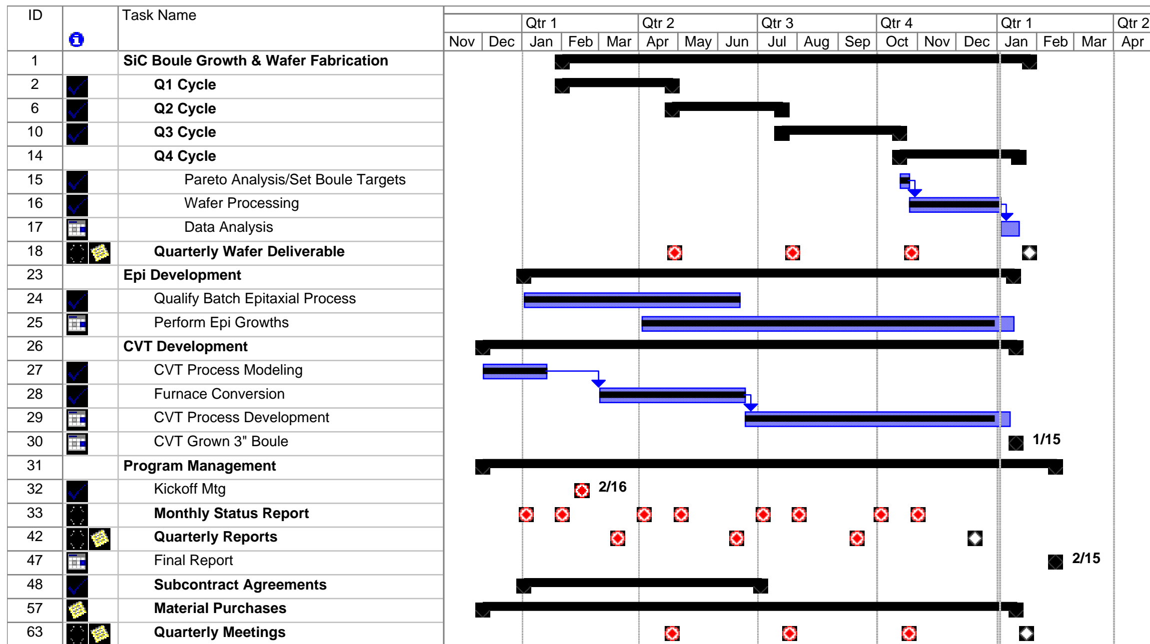
			deposition of silicon in the gas injector. The temperature distribution near the region of deposit is the critical issue. A new injector design is being developed.
	1	Qualify Batch Epitaxy processes for program	Recent epitaxy work focused to develop processes for the Northrup Grumman device subcontract. Developmental work in the multiwafer reactor produced mid doped (1E15-1E16/cm3) epi layers with thickness uniformity (standard deviation/mean) of less than 4 % and doping uniformity of less than 8%. By the end of Q2 24 epiwafers will be processed and delivered to Northrup for device fabrication. Limited work was performed to assess low doped drift layer epitaxy. In these cases it was demonstrated that levels of 5E14/cm3 could be produced in the multiwafer reactor. Epiwafer deliverables were shipped to NRL with full characterization data. Samples exhibit carrier lifetimes in the 5-10 usec range. For the remainder of the first year of the KGS program, the minimum doping target for drift layer epitaxy will stay in the 1-3E15/cm3 range to afford better assessment of carrier lifetime by microwave photoconductive decay measurement.
	2	Demonstration of CVT growth	CVT (gas phase) depositions start week of 6/12/06. System is in house and facilitized.
	4	Deliver first 76mm CVT wafers	After several developmental growth experiments a major issue evolved with silicon deposition upstream of the seed in the injector. Modeling has been used to define the effect very accurately. New injector designs are being developed. A 5 mm thick crystal was grown in the CVT system in 5 successive growth experiments. The injector was changed each time. The growth rate was very consistent throughout the crystal growth at nominally 250 um/hr. Step formation was apparent over the majority of the crystal. The resulting crystal was primarily 4H, with some sections of 6H polytype. Small (<1 mm) inclusions of 3C-SiC were clustered in the center, and this is likely the result of gas induced cooling of the growth front. The system will now be rebuilt with a different crucible design and modified

			exhaust system to suppress downstream reactant condensation.
Task 3: Metrology for Wafer Specifications	**2**	Implement LLS inspection with particles, pits, and scratches delineated.	Wafers were shipped to ONR and NRL with LLS topography maps. First generation work to segregate defect types is nearly complete and data will be provided in June. Algorithms and mapping used for pit detection and fine scratch identification are in use. The results show a clear reduction of pits and scratches has been achieved between Q1 and Q2. Pit and scratch levels on polished wafers are now at program goal.
	3	Start routine microwave loss inspection of 4H SI wafers	Loss measurement calibration and test is progressing well. Full wafer global loss testing in cavities has been performed at 4 GHz and compared to SI GaAs as a benchmark-Several 6H SI wafers with resistivity 1E5-1E7 ohm cm show microwave loss equal to SI GaAs. There is no obvious correlation between loss and resistivity, as expected in these materials. Mapping tests show many regions with loss less than SI GaAs. Next focus is on extending the measurements to X-band. In Q3 a method for measurements of microwave loss on SiC wafers has been developed. Trends closely mimic the observations at L-Band. In general, the results show that SiC is a lower loss material than both GaAs and alumina. In Q4 additional capability was developed to make measurements to 13 GHz. Similar trends between SiC, GaAs and sapphire were observed from 2-13 GHz. A capability to perform loss maps on wafers over this frequency range is now established.
	2	u-PCD tool installed and lifetime measurements implemented for epitaxy layers and SI wafers	u-PCD testing of carrier lifetime is fully operational. Key results show that chlorosilane-based SiC epi has very high lifetime. Samples were delivered to NRL for conformational analysis. Photoluminescence decay tests at NRL confirm long recombination lifetime values in chlorosilane-based epitaxial layers grown and tested at Dow Corning. The samples generated to date in the KGS program represent the longest lifetime values reported in the literature. Efforts at ASU to measure generation lifetime in

			MOS structures grown on chlorosilane-based epitaxial layers also show large values consistent with PL and u-PCD testing. A provisional patent has been filed by Dow Corning regarding gas phase processes to produce long lifetimes in SiC semiconductors. u-PCD testing on PiN structures was peformed. It was found the presence of the p+ layer does not inhibit the measurement of the carrier lifetime, but it does result in a lower measured lifetime compared to the same structure with the p+ layer removed. This could be the result of interfacial or surface recombination effects. The u-PCD maps will be compared to PiN device yields when the devices complete fabrication in year two of the program.
Task 4: Device Technology Maturation	**1**	Publish Rev-0 roadmap for wafer and epi goals	See Appendix 2
	2	Complete disposition strategy for n+ epiwafers	See Appendix 3.
	4	Publish revised roadmap to reflect power and RF device progress	

Schedule

A detailed description of achievements and progress against milestones and deliverables was provided in the table above. The project schedule is provided below as an overview of the progress against the high level tasks on the program. Progress is on track with exception of the gas phase (CVT) task, which is 1.5 months behind due to delays in receiving the tool from the vendor (the schedule has been update accordingly) and the 100mm wafer task (described in the technical section above).



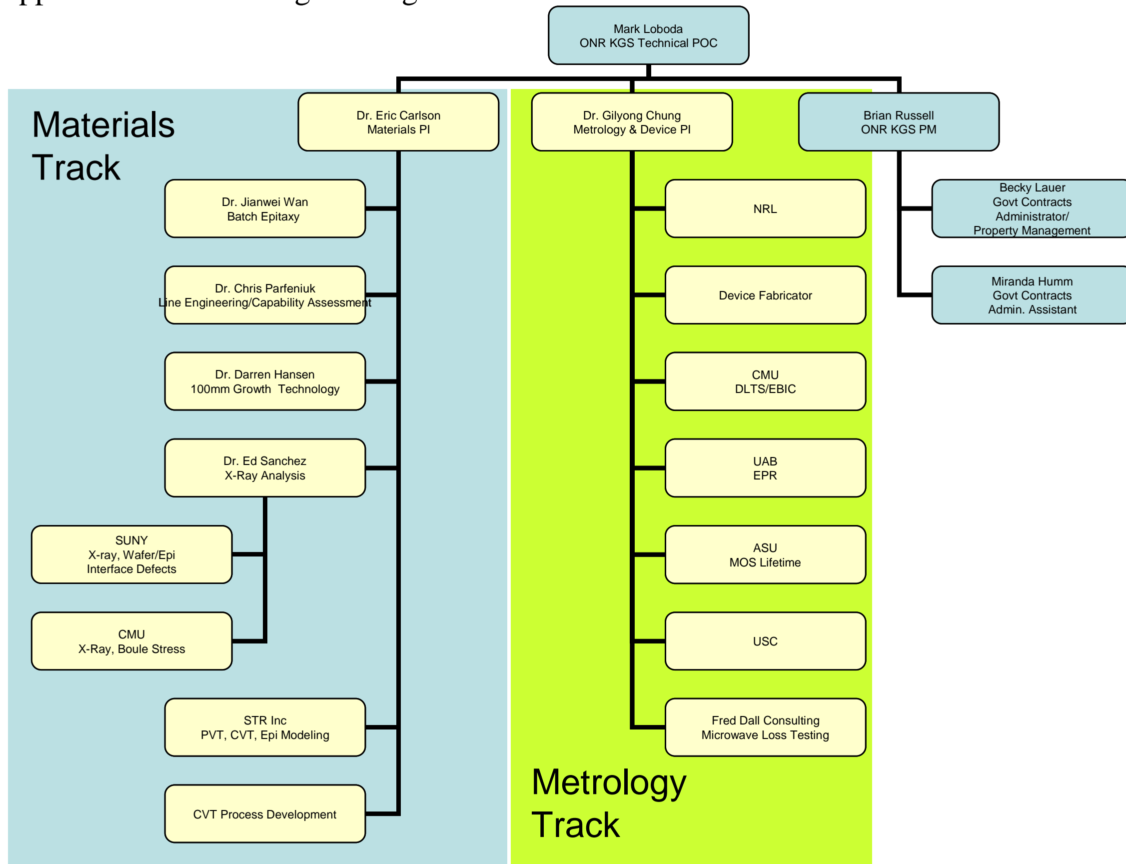
Program Management

Monthly e-mail status updates were submitted to the Program Officer, Dr. Colin Wood. The face to face (all participants) program review meeting that was planned for October was actually held on December 14th in Chicago due to scheduling conflicts for a majority of the attendees in the months of October and November. Appendix 3 contains the updated distribution of program wafers. It is important to note that the original plan had to be modified to meet various needs and opportunities for the work on the program – see Appendix 3 for details.

Cost Status

Cost status updates are provided to Dr. Colin Wood in the monthly e-mail updates.

Appendix 1 – KGS Program Organization



Appendix 2 – KGS Rev-0 Roadmap for Wafer and Epi Goals

Proposed Goals:	Top 30%	Top 50%
Timing for 76 mm diameter	Q1/06	
Timing for 100 mm diameter	Q1/07	
MPD and inclusions (cm^{-2})	<10	<30
Scratches (total length)	<50% diameter	<75% diameter
Areal density surface particles and pits in epiwafers, diameter >0.5 um	<5 cm^{-2}	<10 cm^{-2}
Bulk Metals Contamination B, Al, Ti, V, Fe (atoms/cm^3)	<1E15	<5E15
Stable Epi drift layer carrier concentration (atoms/cm^3)	<1E14	<5E14
Epi thickness uniformity	<8%	<10%
Epi Doping Uniformity	<10%	<15%

Appendix 3 – KGS Wafer Disposition Plan

Wafers Produced for Program	Q1	Q2	Q3	Q4	Total Wafers
75mm n+	0	43	21	56	120
75mm SI	0	0	6	0	6
100mm n+	0	0	3	0	3
100mm SI	0	0	0	0	0
Total	0	43	30	56	**129**

Distribution	Q1 Epi	Q1 No Epi	Q2 Epi	Q2 No Epi	Q3 Epi	Q3 No Epi	Q4 Epi	Q4 No Epi	
NRL (Lifetime Measurements)			5		2	2	4	0	13
CMU (Deep Level, XRT)					2	2	2	0	6
Alabama (Deep Level Measurements)						2		0	2
ASU (Lifetime Measurements)					2		2		4
USC (Diodes)			2		1		1		4
NGES			28		14		14		56
ONR			2	6		3	0	33	44
									129

Mixed Lots
n+
SI

The plan has been altered again as compared to the original proposal and the Q3 modification. No cost changes result. The number of wafers increases. Changes are primarily a result of the Northrup Grumman subcontract which required more n+ wafers than originally proposed and new direction from the ONR program manager requiring substrates for ONR use (see details below). To accommodate these changes, less semi-insulating material and less 100mm material will be produced. DCCS has already started to send in deliverables shown for Q3 with some Q4 deliverables planned for early January delivery. Additional wafers were sent to University of Alabama, Arizona State and CMU at no cost to the program.

November 2006 – per request of ONR, Q4 deliverables will be adjusted. 35 pcs. 4H n+ 76 mm on axis polished wafers will be delivered.