**Naval Research Laboratory**

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# Delta-Sigma UHF Digital Waveform Generator

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The Naval Research Laboratory (NRL) has developed and built a prototype UHF Digital Waveform Generator (DWG) based on the Delta-Sigma ($\Delta$-$\Sigma$) algorithm, which allows arbitrary waveform generation. It provides predicted low phase and spurious noise. Much of the design uses field programmable gate arrays (FPGAs) for single-bit digital waveform generation. Four filter topologies were initially considered, including cascade, hybrid, parallel, and transposed. The cascade and parallel forms were eliminated because they imposed a heavy computational burden on the system. After analyzing the transposed topology, quantization error in higher-order filters led to the selection of the hybrid form of the digital filter because it performed well. A 12th order hybrid filter was selected and implemented using FPGAs. The NRL development demonstrates that a simple-to-code single-bit $\Delta$-$\Sigma$ DWG can cost-effectively provide the same resolution as a 16-bit or greater digital-to-analog converter (DAC) DWG. These results provide the promise of low-cost diverse waveform generation capability in future high-performance Navy radar systems.

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# DELTA-SIGMA UHF DIGITAL WAVEFORM GENERATOR

## 1. INTRODUCTION

The Naval Research Laboratory (NRL) has developed and built a prototype Digital Waveform Generator (DWG) in the ultra-high-frequency (UHF) range. The objective of this project was to develop, test, document, and deliver a preproduction-ready high-performance prototype DWG. This prototype uses Delta-Sigma (Δ-Σ) modulation techniques, which permit arbitrary and accurate waveform generation, to meet the demanding and diverse waveform requirements of future radar applications, including linear-FM (LFM) and continuous wave (CW) signals. This DWG also allows for the generation of waveforms at other frequencies by upconversion or downconversion. The work described here is based on some of the earlier work of Scholnik [1] on Δ-Σ topology and Harrell [2] on single-bit digital signal synthesizers. Some of the efforts on this project were previously reported in Reference 3.

The development of this DWG concept was relatively simple and required only minimal computing effort. It provides predicted low phase and spurious noise. Much of the design uses field programmable gate arrays (FPGAs) for single-bit digital waveform generation. Four filter topologies were initially considered, including cascade, hybrid, parallel, and transposed. However, the cascade and parallel forms were eliminated because they imposed a heavy computational burden on the system. Following analysis of the transposed topology, quantization error in higher-order filters lead to the selection of the hybrid form because it provides the best performance. A 12th order hybrid filter was selected and implemented using FPGAs. FPGAs are rapidly improving with embedded multipliers, more memory availability within the chip architecture, and greater ease of use. Utilizing this advancing technology, NRL coded a FPGA to generate a single-bit Δ-Σ waveform.

The NRL development demonstrates that a simple-to-code single-bit Δ-Σ DWG can provide the same resolution as a 16-bit or greater digital-to-analog converter (DAC) DWG. Based on the results of the effort described here, this technology shows the promise of providing the diverse waveform and improved accuracy requirements of future high-performance Navy radar applications with reduced complexity at relatively low cost.

## 2. DELTA-SIGMA ALGORITHM

The Δ-Σ filter algorithm or Δ-Σ modulator is used to generate a single-bit waveform from the digital input data with a CW center frequency between 406 and 450 MHz, both with and without a 4-MHz bandwidth LFM, with a nominal pulsewidth of 10 μs and an available filter bandwidth of 50 MHz. Initially, four different Δ-Σ digital filter topologies were considered: (1) cascade; (2) hybrid; (3) parallel; and (4) transposed. The *order* M of a Δ-Σ modulator is indicated by the number of feedback loops. The cascade and parallel forms allow for a growing critical path in proportion to increasing filter order. They are thus computationally more intensive and challenging for the FPGA hardware and were therefore eliminated from further consideration. Only the transposed and hybrid forms were considered here in order to achieve the intended ≥ 90 dB dynamic range for CW signals.

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The basic operation of the Δ-Σ modulator in encoding waveforms can be understood more intuitively by demonstration [4]. A simple, first-order modulator is shown in Fig. 1. The output of the comparator, V(z), is also the output of the loop, which is full-scale ±1 V. At the summation, either +1 V or −1 V is added to the input voltage. The result is the input to the Δ-Σ digital filter. The digital filter can implement the filter equation using the two fundamental arithmetic operations, multiplication and addition (or accumulation). If the output of the digital filter, Y(z), is greater than 0 V, V(z) becomes +1 V; if it is less than 0 V, V(z) becomes −1 V. A no-change condition, however, causes the modulated signal to remain at the same ±1 V state of the previous sample. Each operation occurs once during each clock cycle. The output of the loop, either +1 V or −1 V, will be saved in a single-bit data file as either a 1 or 0, respectively. Then the digital single-bit data series is converted to an analog signal by using a high-speed single-bit DAC. In general, first- and second-order modulators are stable, but stability must be considered in higher-order units.

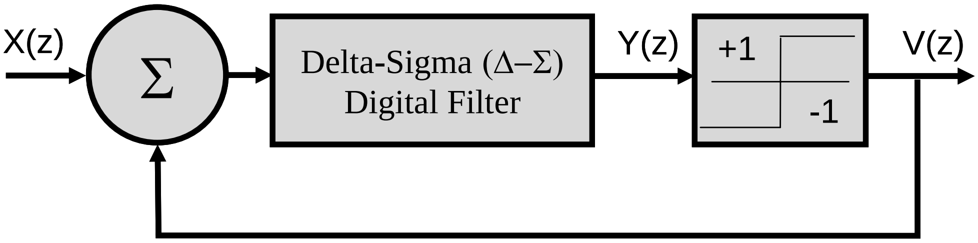


Fig. 1 — A typical Δ-Σ modulator to encode digital waveforms

## 2.1 Delta-Sigma Filter Topologies

Both transposed and hybrid Δ-Σ approaches were considered as described in the next two sections of this report. The approaches included a comparison of transposed filters of various orders. The transposed filter quantization error in higher-order (e.g., M = 8) filters was considered and hybrid filters of various orders were compared.

### *2.1.1 Transposed Form*

The transposed filter has a short critical path of two full additions and one multiply. It thus has the advantage of a short critical path and an efficient finite-impulse response (FIR) implementation. It is, however, extremely sensitive to coefficient quantization accuracy. Transposed filters were analyzed for three orders (M = 2, 4, 8). In particular, the sensitivity of quantization error vs signal-to-noise ratio (SNR) was investigated and is addressed below.

Transposed filters of order M are implemented with an efficient FIR filter, where two full adders and one multiplier are used in each stage. For an N-length discretization $[X(1), X(2), \ldots, X(N)]^T$ of the input signal X(z), the N equations for the $M^{th}$ order transposed Δ-Σ filter are given by

$$Y(n) = \sum_{m=1}^{M} \{a_m Y(n-m) + b_m[X(n-m) + V(n-m)]\}, \quad \text{for } n > m,$$

where $a_m$ and $b_m$ are the $m^{th}$ coefficients of the filter, X(n) is the input signal at the $n^{th}$ discrete value of z for n = 1,…,N, and V(n) is the output of the Δ-Σ filter at the $n^{th}$ discrete value of z. In particular,

$$V(n) = \begin{cases} +1, \text{if } Y(n) > 0 \\ -1, \text{if } Y(n) < 0. \end{cases}$$

A typical transposed Δ-Σ digital filter for M = 4 is shown in Fig. 2. The associated transposed-filter coefficients for M = 2, 4, 8, as shown in Table 1, were computed using the MatLab Δ-Σ coefficient-generator subroutine. The Δ-Σ digital filter provides noise shaping within the filter bandwidth. The CW spectra of the transposed filter outputs are shown in Fig. 3 for (a) M = 2, (b) M = 4, and (c) M = 8. On observing Fig. 3, it can be seen that as the filter order increases the SNR increases within the filter bandwidth, which is 50 MHz in this example. However, with higher-order filters such as M = 8, coefficient quantization decreases the SNR within the filter bandwidth.

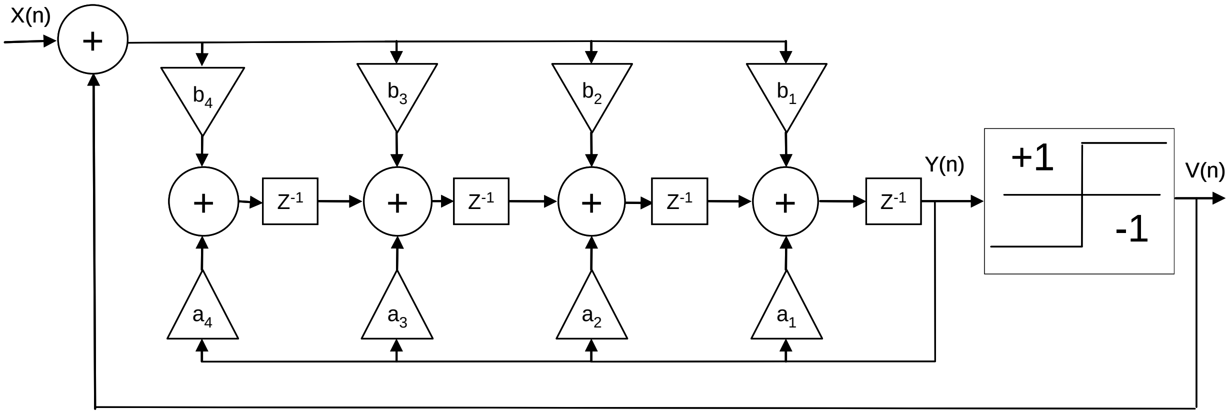


Fig. 2 — A typical transposed Δ-Σ digital filter for M = 4

Table 1 — Transposed Filter Coefficients for M = 2, 4, 8

| Filter Order M | Coefficients $a_1, \ldots, a_M$ | Coefficients $b_1, \ldots, b_M$ |
|---|---|---|
| 2 | $a_1$ = 0.3956<br>$a_2$ = 0.5878 | $b_1$ = 0.9503<br>$b_2$ = -1 |
| 4 | $a_1$ = 0.3988<br>$a_2$ = -1.0661<br>$a_3$ = 0.8812<br>$a_4$ = -0.5567 | $b_1$ = 1.8988<br>$b_2$ = -2.8973<br>$b_3$ = 1.8988<br>$b_4$ = -1 |
| 8 | $a_1$ = 0.3851<br>$a_2$ = -1.8220<br>$a_3$ = 4.0464<br>$a_4$ = -6.0648<br>$a_5$ = 6.0185<br>$a_6$ = -4.3489<br>$a_7$ = 1.9440<br>$a_8$ = -0.5576 | $b_1$ = 3.7978<br>$b_2$ = -9.3983<br>$b_3$ = 14.7971<br>$b_4$ = -17.5997<br>$b_5$ = 14.7971<br>$b_6$ = -9.3983<br>$b_7$ = 3.7978<br>$b_8$ = -1 |

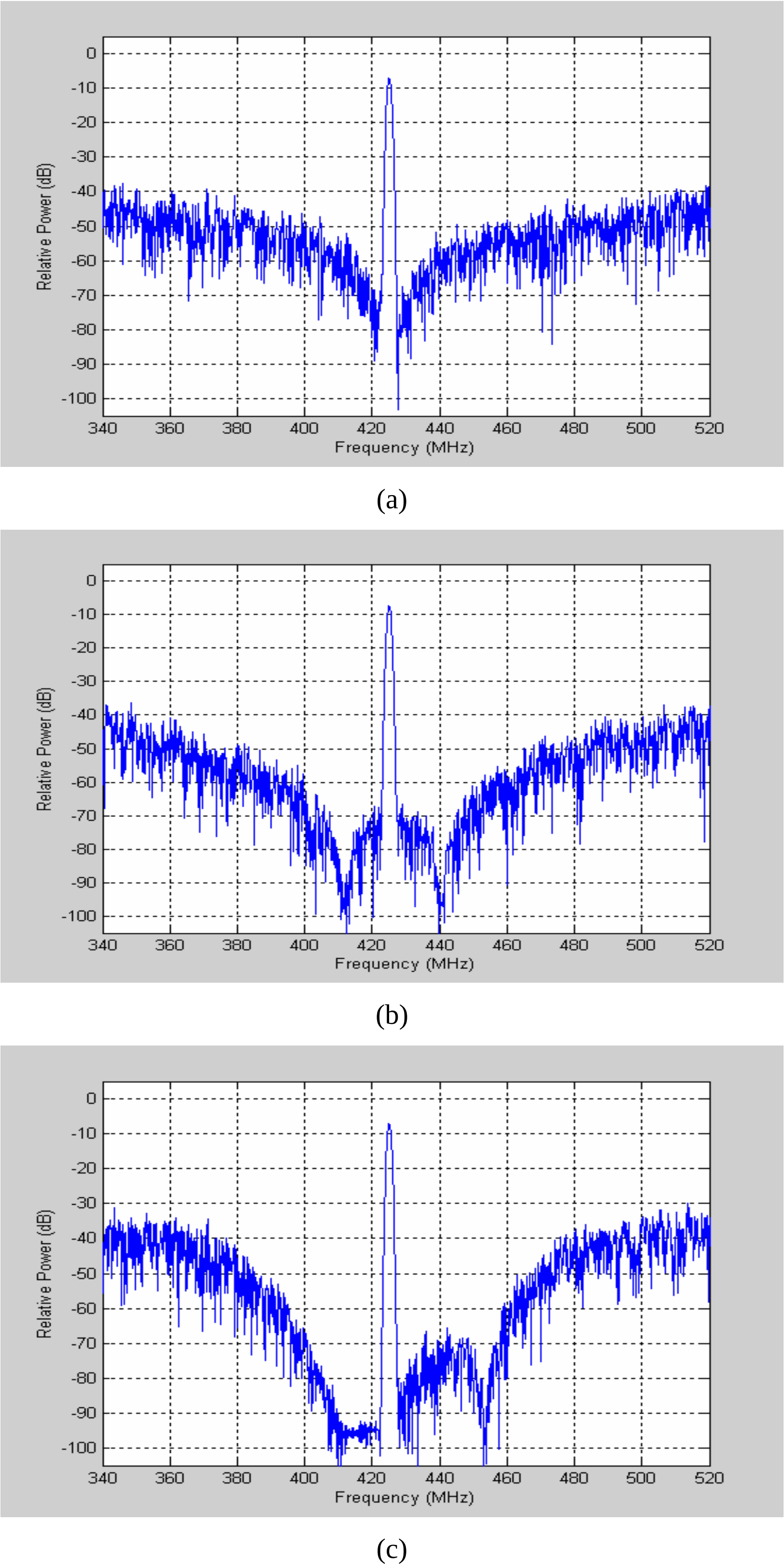
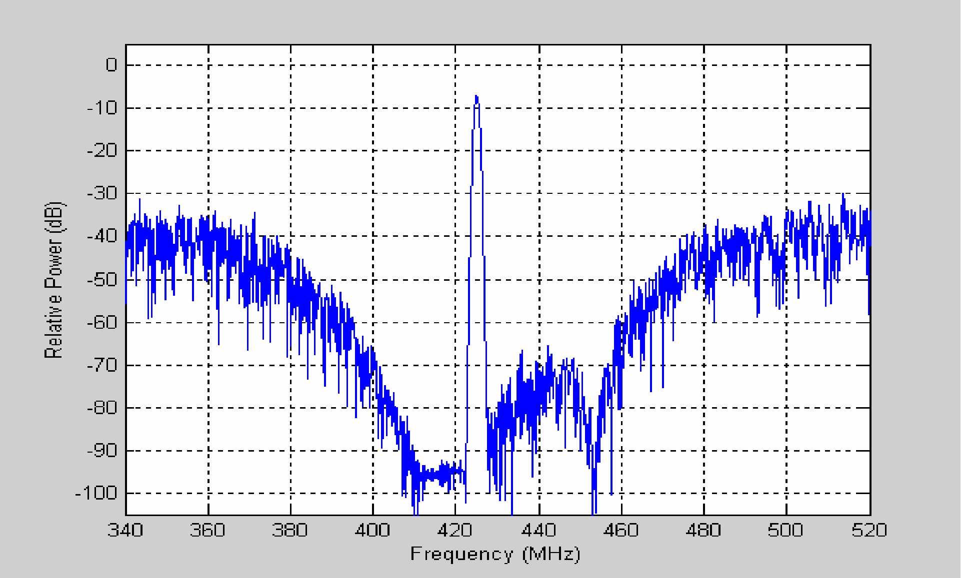
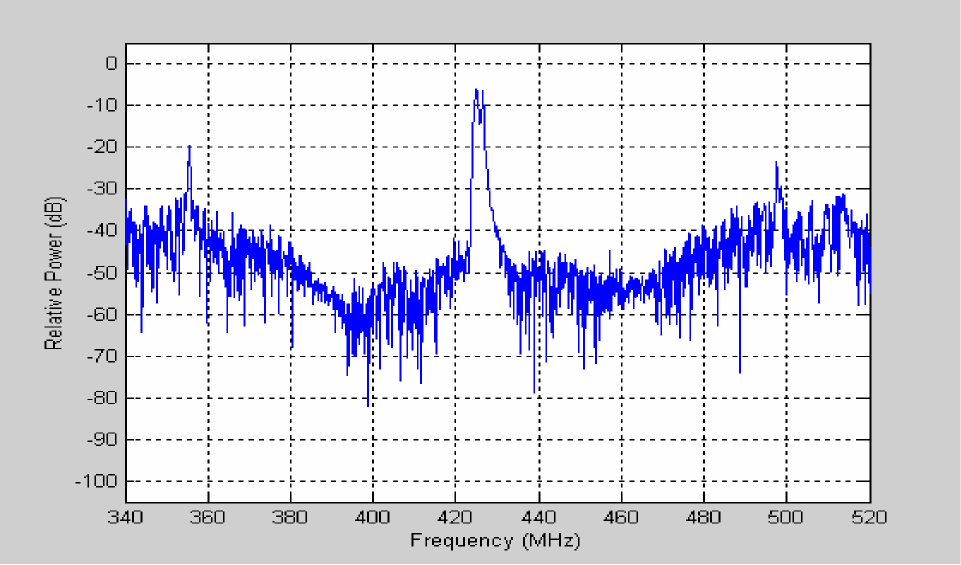


Fig. 3 — CW spectra using Δ-Σ transposed filters: (a) M = 2, (b) M = 4, and (c) M = 8.

To show that SNR reduction in a higher-order filter is sensitive to coefficient quantization, $b_1 = 3.7978$ for the filter spectra of Fig. 3(c) for M = 8, as shown again for comparison in Fig. 4(a), is changed to $b_1 = 3.7976$ with the resulting spectra shown in Fig. 4(b). On comparing Figs. 4(a) and 4(b), it can be observed that this filter is extremely sensitive to coefficient quantization for higher-order filters. In this example, the sidelobe levels increase by at least 20 dB. The Δ-Σ hybrid filter, which has the same critical path as the transposed filter, is considered in the following section.



(a)



(b)

Fig. 4 — CW spectra using a Δ-Σ transposed filter for M = 8 with (a) $b_1 = 3.7978$ and (b) $b_1 = 3.7976$

### *2.1.2 Hybrid Form*

The hybrid filter has the same short critical path as the transposed filter with two full additions and one multiply. It thus also has the advantage of a short critical path, but poles on the unit circle reduce the multiply count. However, the zeros may be sensitive to coefficient quantization accuracy. The impact of hybrid filters is determined and analyzed for M = 2, 4, 8, 12, 16. The equations for the M$^{th}$ order hybrid Δ-Σ filter are given by

$$Y_M(n) = a_M\,[Y_{M-1}(n-1)] + b_M\,[X(n-1) + V(n-1)];$$

$$Y_{M-k}\,(n) = a_{M-k}[Y_{M-k}(n-1)] + b_{M-k}\,[X(n-1) + V(n-1)] + Y_{M-k+1}(n-1);\ \text{for } k = 1,3,...,M-1$$

$$Y_{M-k}\,(n) = a_{M-k}[Y_{M-k-1}(n-1)] + b_{M-k}\,[X(n-1) + V(n-1)] + Y_{M-k+1}(n-1);\ \text{for } k = 2,4,...,M-2$$

where $a_M$ and $b_M$ are the M$^{th}$ coefficients of the filter, X(n) is the input signal at the n$^{th}$ discrete value of z for n = 1,…,N, and V(n) is the output of the Δ-Σ filter at the n$^{th}$ discrete value of z. In particular,

$$V(n) = \begin{cases} +1, \text{ if } Y(n) > 0 \\ -1, \text{ if } Y(n) < 0. \end{cases}$$

A typical hybrid Δ-Σ digital filter for M = 4 is shown in Fig. 5. The associated hybrid filter coefficients for M = 2, 8, 12, 16, as shown in Table 2, were computed using the MatLab Δ-Σ coefficient-generator subroutine. The CW spectra of the hybrid Δ-Σ filter outputs are shown in Fig. 6 for (a) M = 2, (b) M = 8, (c) M = 12, and (d) M = 16 Δ-Σ hybrid filters. The corresponding equations for the 4$^{th}$ order hybrid filter can be easily written as

$$Y_4(n) = a_4\,[Y_3(n-1)] + b_4\,[X(n-1) + V(n-1)];$$

$$Y_3(n) = a_3\,[Y_3(n-1)] + b_3\,[X(n-1) + V(n-1)] + Y_4(n-1);$$

$$Y_2(n) = a_2\,[Y_1(n-1)] + b_2\,[X(n-1) + V(n-1)] + Y_3(n-1);$$

$$Y_1(n) = a_1\,[Y_1(n-1)] + b_1\,[X(n-1) + V(n-1)] + Y_2(n-1).$$

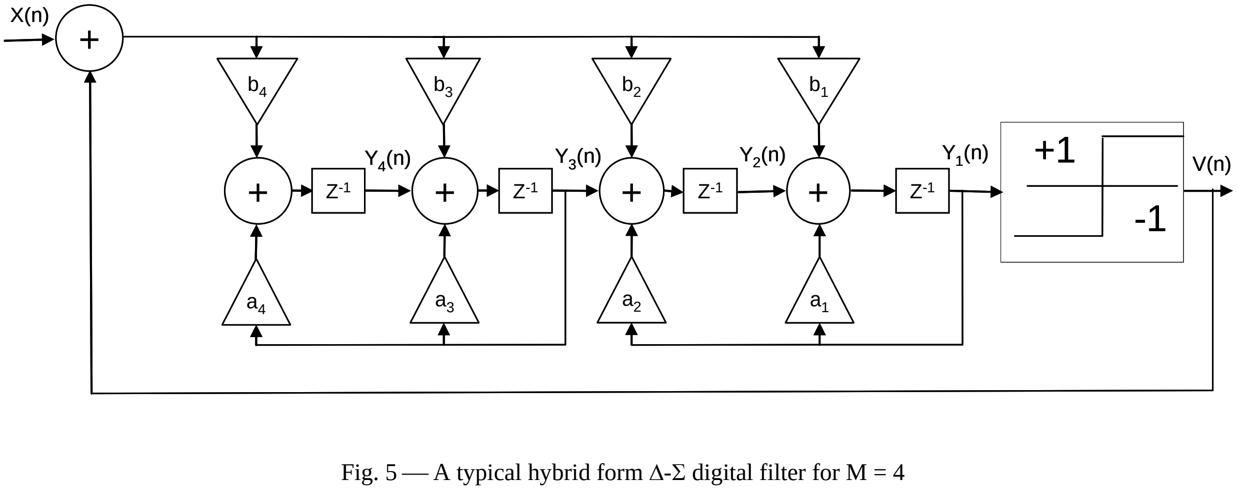
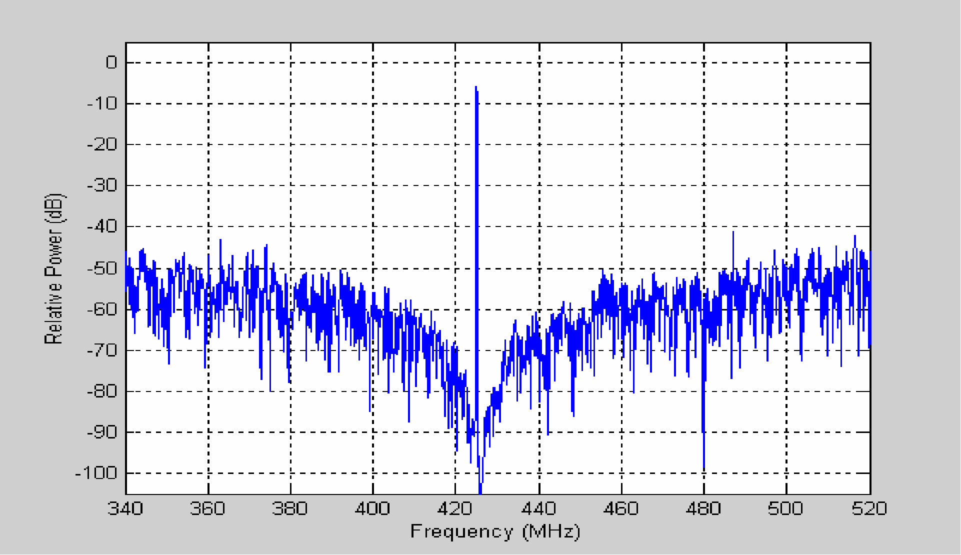


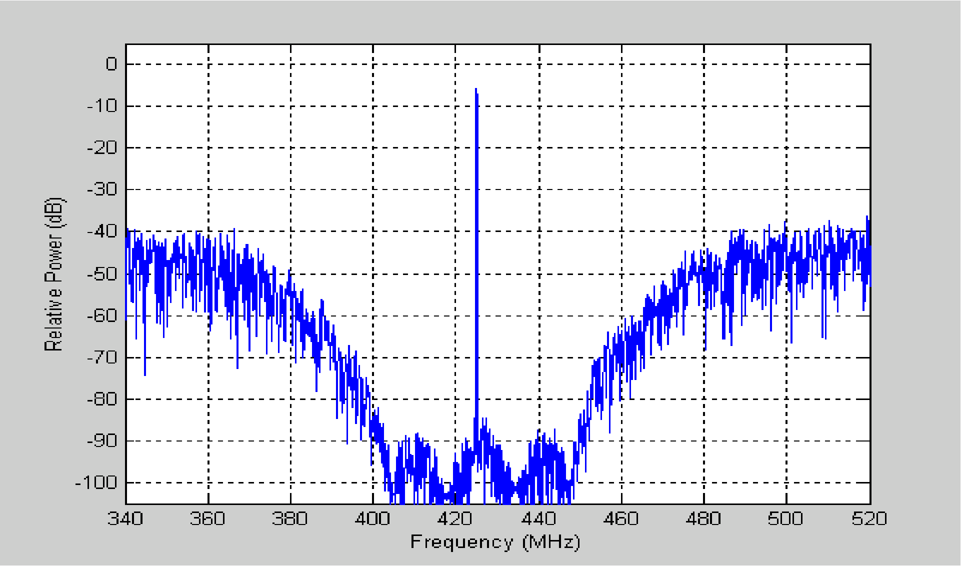
Fig. 5 — A typical hybrid form Δ-Σ digital filter for M = 4

Table 2 — Hybrid Filter Coefficients for M = 2, 8, 12, 16

| Filter Order (M) | Coefficients $a_1$,…., $a_M$ | Coefficients $b_1$, …, $b_M$ |
|---|---|---|
| 2 | $a_1 = 0.9503$ | $b_1 = 0.3956$ |
| | $a_2 = -1$ | $b_2 = -0.5878$ |
| 8 | $a_1 = 1.0440$ | $b_1 = 0.3856$ |
| | $a_2 = -1$ | $b_2 = -0.7613$ |
| | $a_3 = 0.9876$ | $b_3 = -0.1778$ |
| | $a_4 = -1$ | $b_4 = 0.2445$ |
| | $a_5 = 0.9125$ | $b_5 = 0.0375$ |
| | $a_6 = -1$ | $b_6 = -0.0442$ |
| | $a_7 = 0.8537$ | $b_7 = -0.0035$ |
| | $a_8 = -1$ | $b_8 = 0.0034$ |
| 12 | $a_1 = 1.0517$ | $b_1 = 0.3856$ |
| | $a_2 = -1$ | $b_2 = -0.7686$ |
| | $a_3 = 1.0225$ | $b_3 = -0.1749$ |
| | $a_4 = -1$ | $b_4 = 0.2583$ |
| | $a_5 = 0.9765$ | $b_5 = 0.0389$ |
| | $a_6 = -1$ | $b_6 = -0.0588$ |
| | $a_7 = 0.9238$ | $b_7 = -0.0051$ |
| | $a_8 = -1$ | $b_8 = 0.0090$ |
| | $a_9 = 0.8764$ | $b_9 = 0.0004$ |
| | $a_{10} = -1$ | $b_{10} = -0.0008$ |
| | $a_{11} = 0.8456$ | $b_{11} = 0.0000$ |
| | $a_{12} = -1$ | $b_{12} = 0.0000$ |
| 16 | $a_1 = 1.0547$ | $b_1 = 0.3369$ |
| | $a_2 = -1$ | $b_2 = -0.6781$ |
| | $a_3 = 1.0371$ | $b_3 = -0.1191$ |
| | $a_4 = -1$ | $b_4 = 0.1997$ |
| | $a_5 = 1.0078$ | $b_5 = 0.0182$ |
| | $a_6 = -1$ | $b_6 = -0.0421$ |
| | $a_7 = 0.9705$ | $b_7 = -0.0006$ |
| | $a_8 = -1$ | $b_8 = 0.0062$ |
| | $a_9 = 0.9299$ | $b_9 = -0.0003$ |
| | $a_{10} = -1$ | $b_{10} = -0.0005$ |
| | $a_{11} = 0.8916$ | $b_{11} = 0.0000$ |
| | $a_{12} = -1$ | $b_{12} = 0.0000$ |
| | $a_{13} = 0.8610$ | $b_{13} = 0.0000$ |
| | $a_{14} = -1$ | $b_{14} = 0.0000$ |
| | $a_{15} = 0.8424$ | $b_{15} = 0.0000$ |
| | $a_{16} = -1$ | $b_{16} = 0.0000$ |

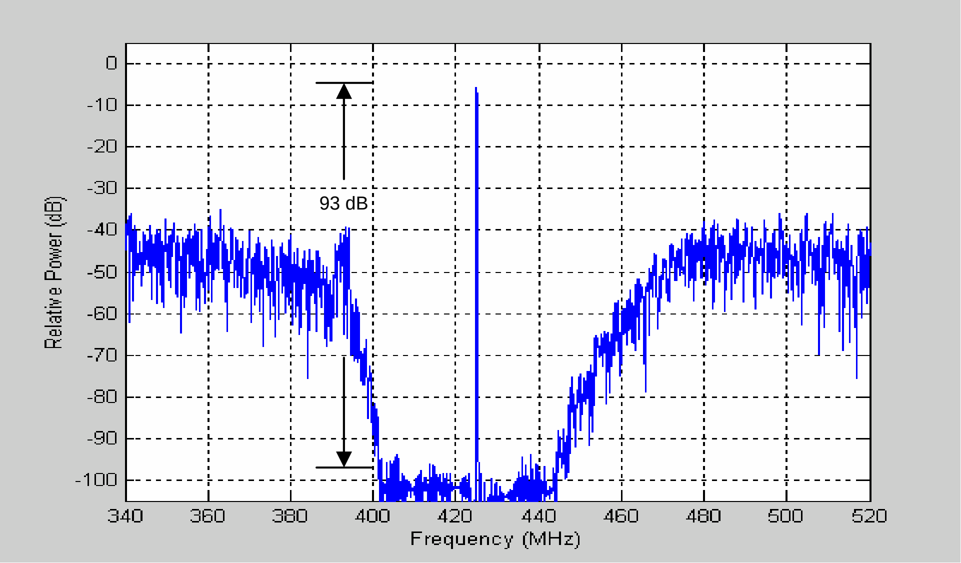


(a)

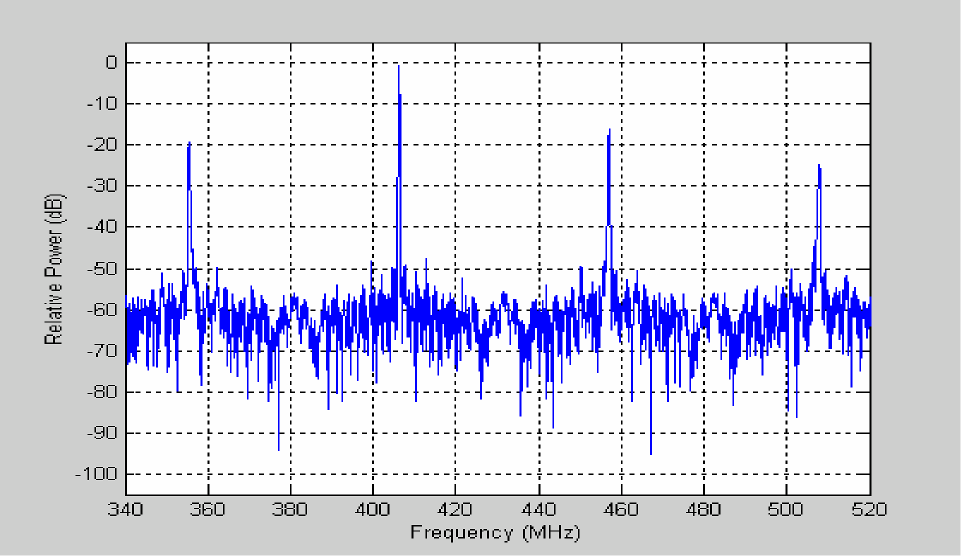


(b)

Fig. 6 — CW spectra using Δ-Σ hybrid filters: (a) M = 2, (b) M = 8, (c) M = 12, and (d) M = 16 (see next page for (c) and (d))



(c)



(d)

Fig. 6 — (continued) CW spectra using Δ-Σ hybrid filters: (a) M = 2, (b) M = 8, (c) M = 12, and (d) M = 16

Figure 6 indicates that the dynamic range of the signal increases with filter order. However, with the use of higher-order filters such as with M = 16, coefficient quantization reduces the SNR to an unacceptable level. It should be noted that the 93 dB SNR shown in Fig. 6(c) is comparable to a 16-bit or greater conventional DAC DWG. These figures also show the spectrum of a CW signal at 425 MHz with more than 90 dB desirable dynamic range using a Δ-Σ hybrid filter for M = 12. Based on these simulated filter outputs, the hybrid digital filter with M = 12 is chosen to generate UHF waveforms in the range of 406 to 450 MHz.

## 3. SYSTEM HARDWARE DESCRIPTION

The DWG is designed to take advantage of current technology advances in digital circuitry including the use of FPGAs. An FPGA system provides a flexible programmable computer-logic environment in which to generate waveforms using Δ-Σ modulation techniques. The general system diagram is shown in Fig. 7. This section describes the high-level functionality of the UHF DWG in implementing Δ-Σ techniques.

A MatLab code was used to generate the digital waveform at the UHF frequency range of 406 to 450 MHz with an oversampling frequency of 2488 MHz. Typical waveform parameters include: (1) a UHF frequency of 425 MHz; (2) a bandwidth of 4 MHz; (3) a pulsewidth of 10 µs; and (4) a pulse repetition interval (PRI) of 0.1 to 10 kHz. This digital waveform code is loaded onto BlockRAM memory contained in the FPGA chip. The waveform is then filtered using a Δ-Σ algorithm. The output of this filter is a single-bit Δ-Σ waveform. The serial output of the single-bit waveform is converted from a single-bit to a 20-bit parallel format and is loaded in a selected BlockRAM memory location to be read out to the synchronizer. The functionality of these FPGAs is shown in Fig. 8.

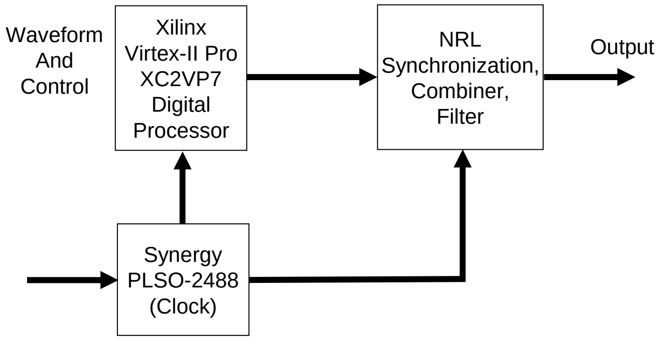


Fig. 7 — DWG board

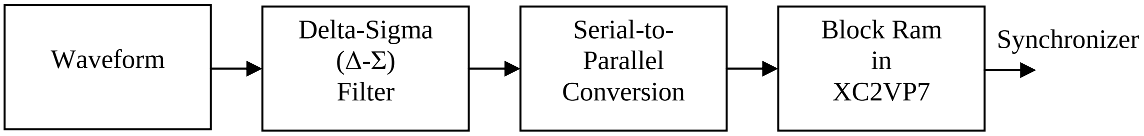


Fig. 8 — FPGA functionality

## 4. SIMULATION

Initial simulation of the Δ-Σ algorithm is conducted in a MatLab environment. Following successive MatLab runs, the desired filter characteristics are programmed into the FPGA environment.

### 4.1 MatLab Simulation

The procedure for accomplishing the MatLab simulation is: (1) generate the coefficients for the chosen filter using the MatLab Δ-Σ coefficient-generator subroutine; (2) write the mathematical code for the selected Δ-Σ digital filter; (3) generate digital data representative of a signal with a center frequency from 406 to 450 MHz supporting a 4 MHz bandwidth LFM modulation format with a nominal pulsewidth of 10 μs; and (4) output a single-bit Δ-Σ waveform from the Δ-Σ filter. For a Δ-Σ hybrid filter of M = 12, the time-domain modular outputs and the resulting spectra from a CW signal and a 4-MHz bandwidth LFM, both with nominal pulsewidth of 10 μs, are shown in Figs. 9 and 10. The spectra are generated as 20 $\log_{10}$ of the fast Fourier transform (FFT) of the time-domain outputs. After analyzing these figures, one can conclude that the CW signal at the filter frequency range of 406 to 450 MHz could produce an output with more than a 90 dB dynamic range. In the case of LFM, about a 46 dB dynamic range is expected because of the accumulation of energy loss due to the 4-MHz bandwidth of the signal. As expected, the spectrum is not well constrained in frequency beyond the 50-MHz band-limited bandwidth.

### 4.2 FPGA Simulation

A similar procedure provides a simulation in the FPGA environment. The spectra resulting from a CW signal and a 4 MHz bandwidth LFM using a Δ-Σ hybrid filter for M = 12, both with nominal pulsewidth of 10 μs, are shown in Fig. 11. On comparing Figs. 9, 10, and 11, it can be concluded that similar filter output dynamic ranges are attainable in the FPGA environment.

## 5. HARDWARE IMPLEMENTATION

Data generated using the Δ-Σ algorithm were loaded into the NRL UHF Δ-Σ waveform generator via an Agilent pattern generator as well as by means of a Virtex-II Pro-P7 FPGA development board. Waveforms produced by the hardware implementation were nearly as high in quality as the spectra of the waveforms shown in Fig. 11. In the FPGA environment, the Xilinx Rocket I/O architecture technology was chosen to sample a single-bit Δ-Σ output at a data rate of 2.5 Gbps.

## 6. SUMMARY AND CONCLUSIONS

The Naval Research Laboratory has developed and built a prototype UHF Digital Waveform Generator based on the Delta-Sigma algorithm, which allows arbitrary waveform generation. The development of this DWG concept was relatively simple and required only minimal computing effort. It provides predicted low phase and spurious noise. Much of the design uses field programmable gate arrays for single-bit digital waveform generation. Four filter topologies were initially considered, including cascade, hybrid, parallel, and transposed. However, the cascade and parallel forms were eliminated because they imposed a heavy computational burden on the system. After analyzing the transposed topology, quantization error in higher-order filters led to the selection of the hybrid form of the digital filter because it performed well. A 12th-order hybrid filter was selected and implemented using FPGAs. The NRL development demonstrates that a simple-to-code single-bit Δ-Σ DWG can provide the same resolution as a 16-bit or greater digital-to-analog converter DWG. Based on the results of the efforts described here, this technology shows the promise of providing the diverse waveform requirements of future high-performance Navy radar applications at relatively low cost.

## 7. ACKNOWLEDGMENTS

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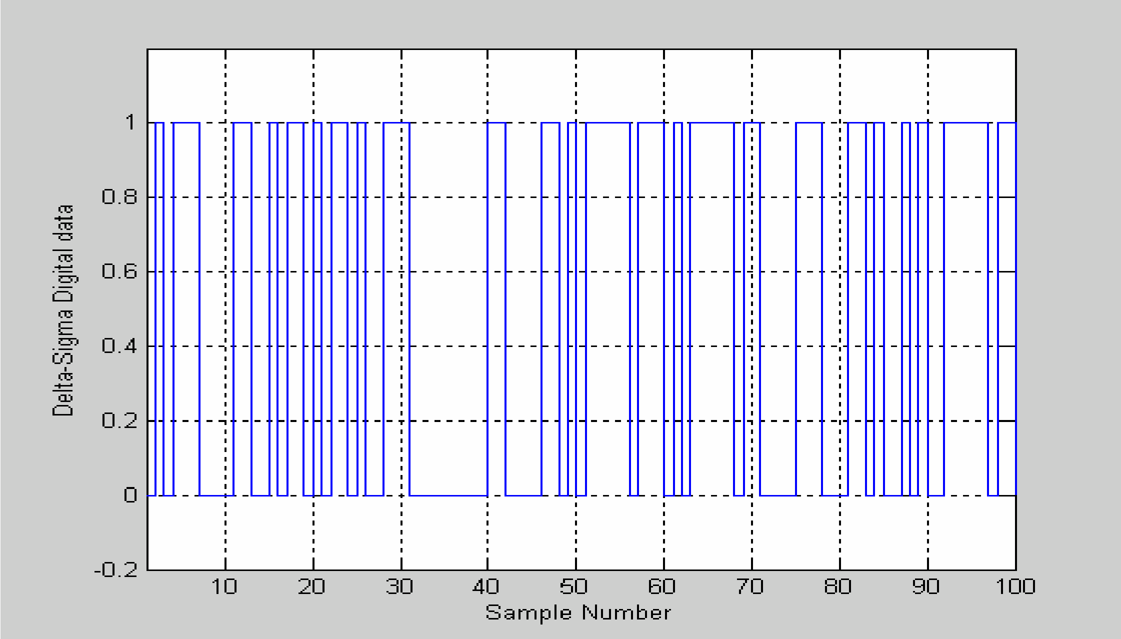
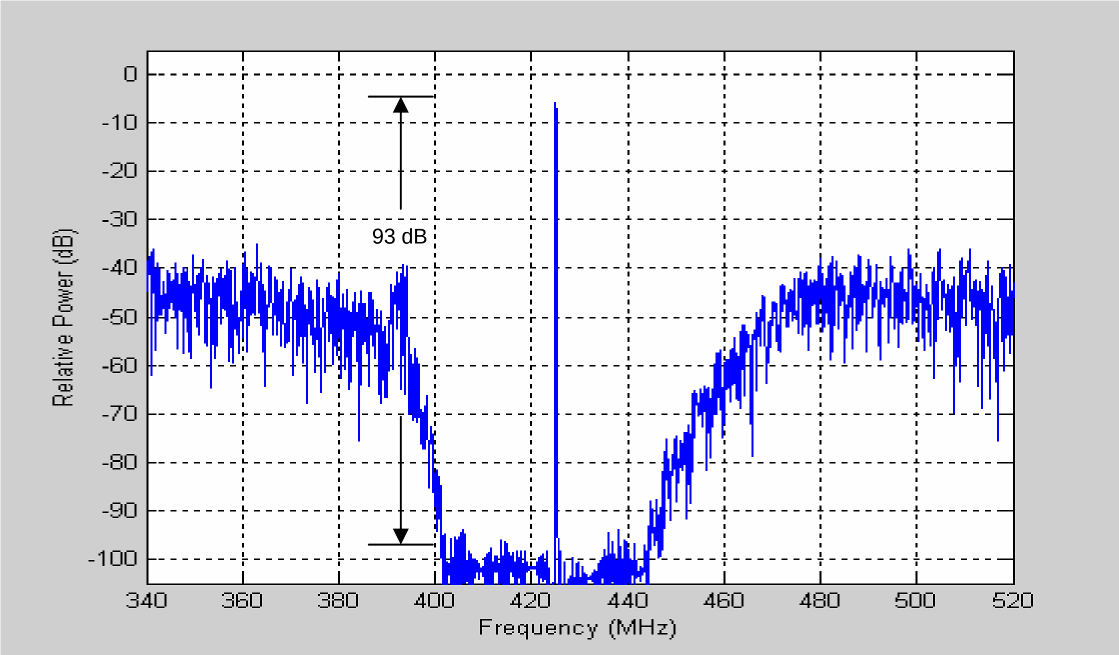
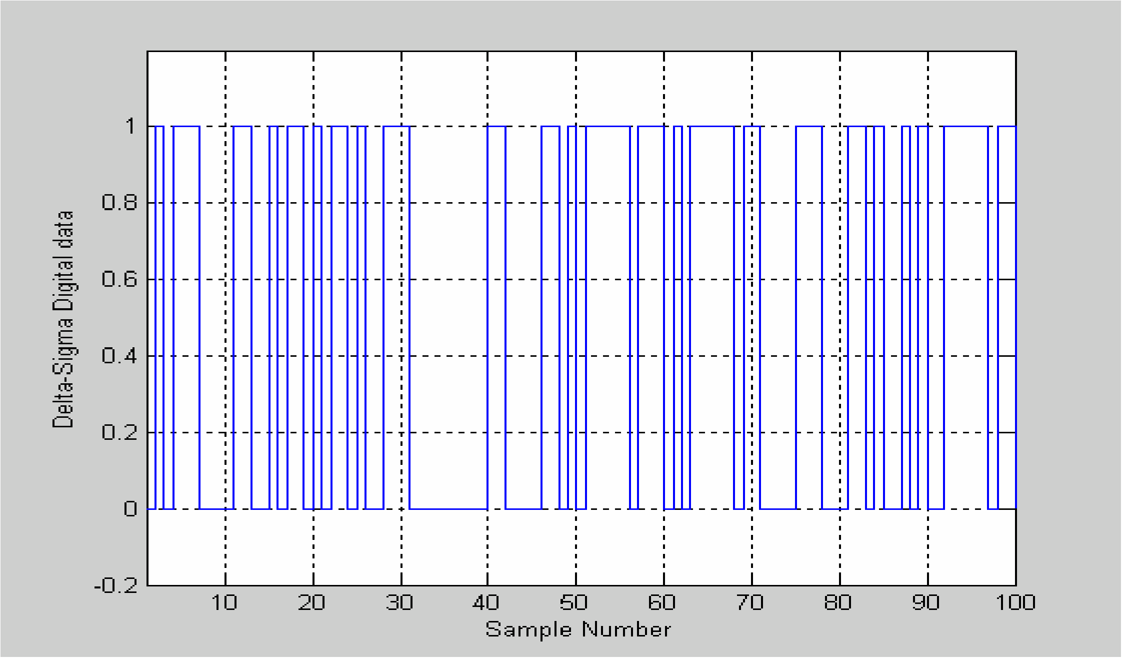


(a)

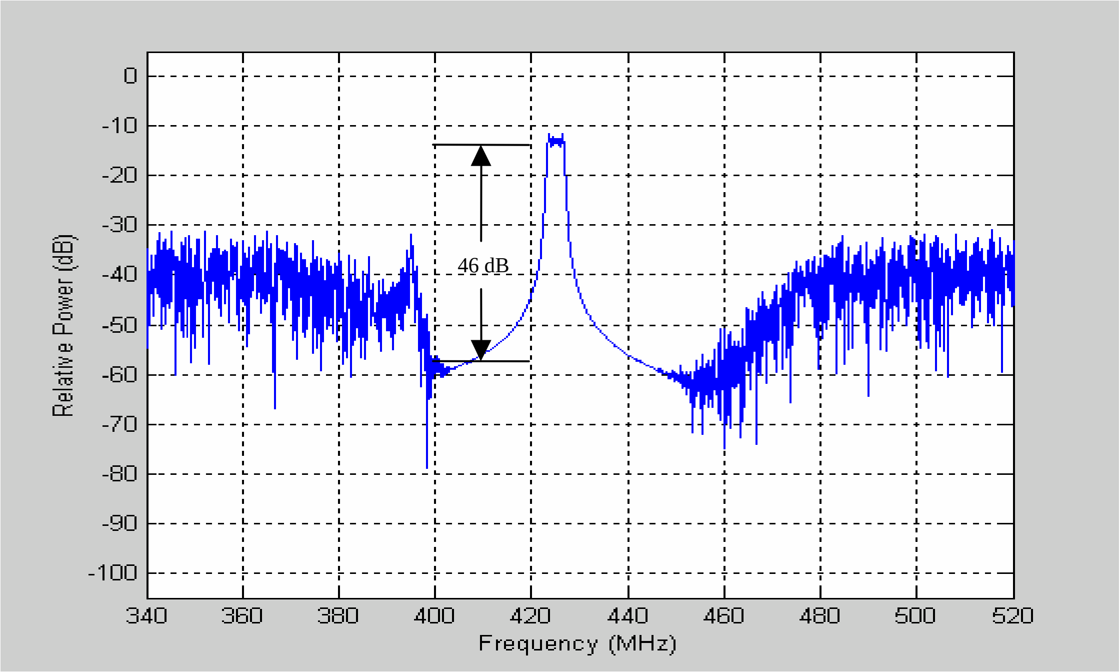


(b)

Fig. 9 — CW time-domain output (a) and spectrum (b) at 425 MHz using a MatLab Δ-Σ hybrid filter for M = 12

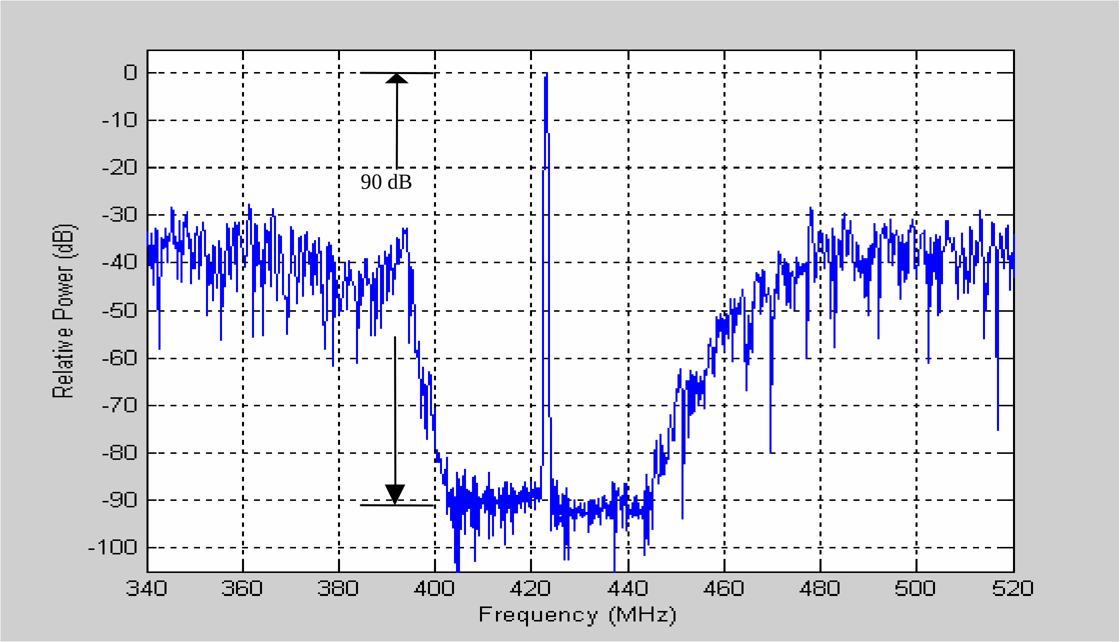


(a)

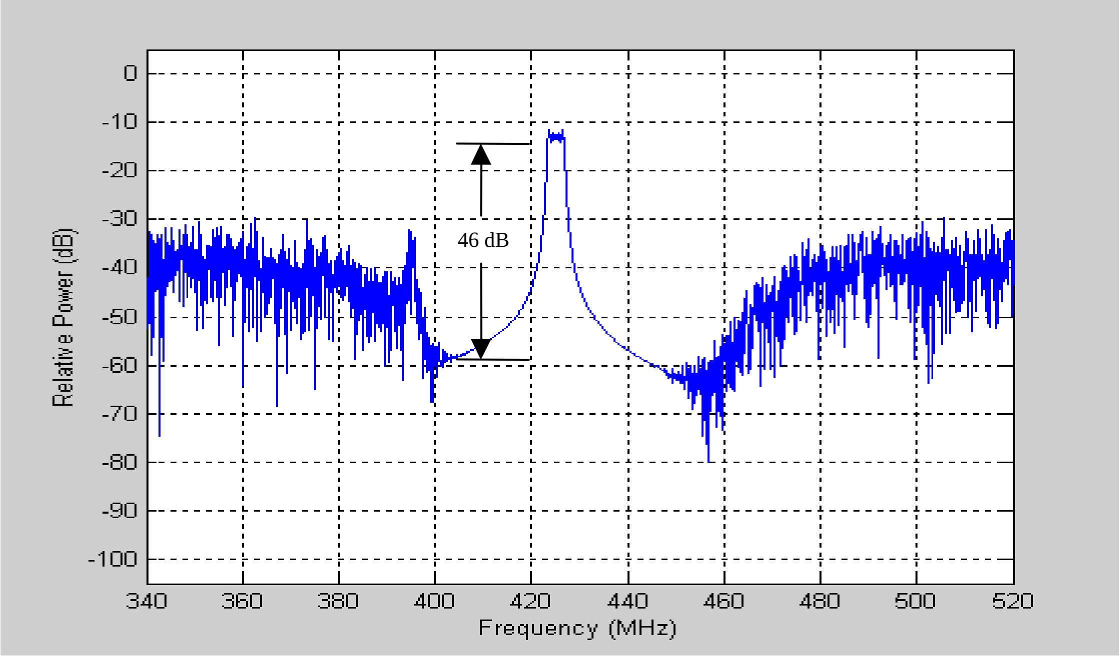


(b)

Fig. 10 — LFM time-domain output (a) and spectrum (b) at 425 MHz using a MatLab Δ-Σ hybrid filter for M = 12



(a)



(b)

Fig. 11 — Spectra of (a) CW and (b) LFM signals at 425 MHz using an FPGA Δ-Σ hybrid filter for M = 12

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