Measurementof Seebeck coefficient perpendicular to SiGe superlattice

Yan Zhang[1], Gehang Zeng[2], Rajeev Singh [1],James Christofferson[1], Edward Croke[3], John E. Bowers[2] and Ali Shakouri[1],

[1]Electrical Engineering Dept. of University of California, Santa Cruz, CA 94056,
[2]Electrical and Computer Engineering Dept. of University of California, Santa Barbara, CA 93106;
[3]HRL laboratories, LLC Malibu, California 90265

Abstract

Seebeck coefficient is one of the key parameters to evaluate the performance of thermoelectric coolers. However, it is very difficult to directly measure Seebeck coefficient perpendicular to thin film devices because of the difficulty of creating a temperature gradient and measuring localized temperature and voltage change simultaneously. In this paper, a novel method is described and it is used to measure the Seebeck coefficient of SiGe superlattice material perpendicular to the layers[1]. Successful measurement was achieved by integrating a thin film metal wire as a temperature sensor and heat source on top of the SiGe superlattice micro coolers. Extensive thermoreflectance imaging characterization was performed to ensure uniform temperature distribution on top of the thin film device. Details of the experimental set-up and measurement technique are discussed. By analyzing the measured thermoelectric voltage for various device sizes and superlattice thickness, Seebeck coefficient of the superlattice material perpendicular to the layers is deduced.

Introduction

In VLSI circuits, high heating power density is one of the bottlenecks that limits the reliability and performance of the chip in high-speed, high-density applications. Conventional bulk Bi_2Te_3 coolers[2] have limited applications in microelectronic circuits due to low cooling power density and difficulty of integration and packaging[3]. Conventional Si or III-V based semiconductor materials have a low thermoelectric figure-of-merit and they are not suited for cooling application. There have been several excellent recent studies on BiTe-based thin film coolers with high thermoelectric figure-of-merit[2]. We are concentrating on SiGe-based coolers for the possibility of direct integration with silicon circuits. Use of thermionic emission in heterostructure superlattices can improve the figure-of-merit by selective emission of hot electrons above potential barriers and by reducing the phonon heat conduction in multiplayer materials. SiGe and SiGeC-based coolers have already demonstrated a cooling power density exceeding $500 W/cm^2$ and a maximum cooling of 4^0C at room temperature. [4]

In this paper, we focus our study on the Seebeck coefficient perpendicular to SiGe superlattice layers. Although there are some papers on the cross-plan thermal conductivity, electrical conductivity of SiGe superlattice[5,6,7,8]. There are still very few papers on the experimental measurements of the Seebeck coefficient perpendicular to the thin film because of its difficulty to measure the voltage and temperature change simultaneously.[9,10] We used an integrated thin film resistor both as a heater and a sensor on top of the SiGe superlattice microcooler. The processing was done using the standard semiconductor fabrication process [11].

In a linear transport regime, the Seebeck coefficient is defined as the voltage produced across two points on a material divided by the temperature difference between them. This has an expression of $S = \frac{\Delta V}{\Delta T}$ [12]. Seebeck coefficient is the main parameter to evaluate performance of thermocouples. It is also the key parameter to calculate the ZT, the thermoelectric figure of merit, which has the expression of:

$$ZT = S^2 T / rK_T \qquad \text{(Eqn.1)}$$

Where S: Seebeck coefficient; T: temperature; ρ: electrical resistivity; K_T: Thermal conductivity[12].

Experiments

The micro-cooler structure is based on cross-plane electrical transport theory. The main part of the cooler is a superlattice structure of 80Å Si/40 Å $Si_{0.7}Ge_{0.3}$ grown at 500^0C, doped with boron to about $5x10^{19}$ cm^{-3}. The buffer layer was grown on top of the silicon with the structure of 1um $SiGe_{0.1}$ doped to $5x10^{19}$ cm^{-3} and 1μm $SiGe_{0.1}/SiGe_{0.15}C_{0.005}$. Finally, the sample was capped with 250nm $SiGe_{0.1}$, doped to approximately $2x10^{20}$ cm^{-3}. The SiGe/Si micro-coolers are fabricated with standard silicon integrated circuit technology. The cooler device areas were defined by etching mesas down to the SiGe buffer layer. Ti/Al/Ti/Au metallisation was made on top of the mesa and on the SiGe buffer layer next to the mesa for top and bottom contacts respectively. The size of the sample is ranging from 50x50μm to 100x100μm. Figure. 1 shows a scanning electron micrograph picture of this device.

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
2006		**00-00-2006 to 00-00-2006**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Measurement of Seeback coefficient perpendicular to SiGe superlattice	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Department of Electrical and Computer Engineering,University of California,Santa Barbara,CA,93106**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES
The original document contains color images.

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**		**4**	

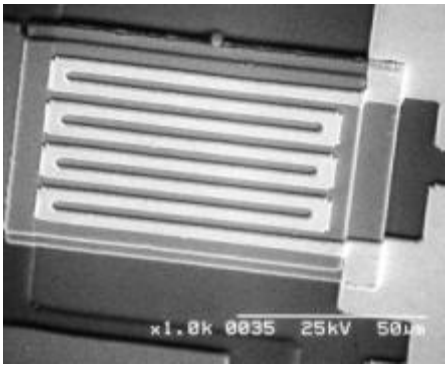

Figure 1 The SEM picture of SiGe superlattice microcooler integrated with heater sensor

First resistance versus temperature of the heater sensor was calibrated. Four-wire measurement was used to reduce the effect of contact wires and pads. Then at a given heater power (fixed top layer temperature, T_h), the voltage difference across the device ΔV was measured. The bottom of the silicon substrate was maintained at the heat sink temperature (T_s). It is important to note that the measured thermoelectric voltage ΔV has a contribution from both the superlattice Seebeck coefficient and also the Si substrate Seebeck coefficient.

$$\Delta V = S1 \times (T_s' - T_s) + S2 \times (T_h - T_s') \qquad \text{(Eqn. 2)}$$

S1 is the Seebeck coefficient of bulk Silicon; T_s' is the temperature at the interface between the superlattice layer and substrate. If the temperature T_s' is equal to T_s, then the effective Seebeck coefficient equals to that of superlattice. However, this is not the case for our devices. We will see that the superlattice Seebeck coefficient S2 could be easily derived by analyzing experimental results for different thin film layer thicknesses and device sizes. Bao Yang et al have used AC method to measure Seebeck coefficient of thin films[13], the signal of our samples are large enough for an accurate DC measurements.

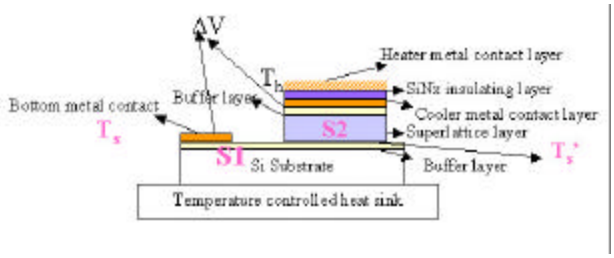

Figure 2 Cross-section schematic of superlattice device (not to scale)

Results and Discussion

The heater resistance changes linearly with temperature near 300K, so it was used as a temperature sensor on top of the superlattice device. The temperature sensor was calibrated by measuring the resistance with very low excitation currents at different ambient temperatures. Variations of the resistance with temperature could be fitted well with a line, with an error less than 0.02%. The heater samples used in this experiments have an average of 4×10^{-3} /°C in a unit resistance ($\frac{dR/dT}{R}$). Subsequently thermoreflectance imaging was used to measure the temperature distribution on top of the device when the heater was on. As it can be seen from Fig. 3, the heating was localized on top of the thin film device.

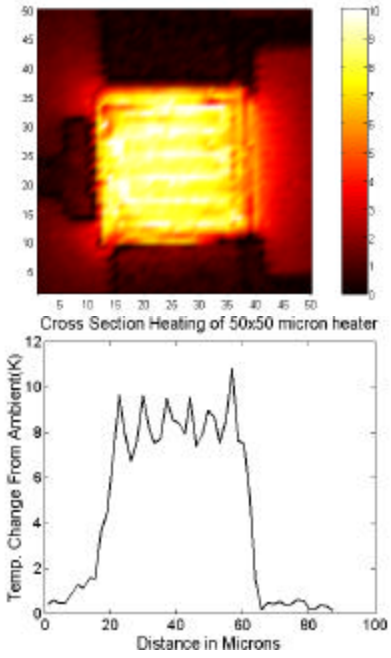

Figure 3 Demonstration of localized heating of SiGe superlattice micro coolers

Figure 4 displays the voltage change across the sample as a function of the temperature gradient for all different size samples, ranging from 50x50µm to 100x100µm. The slope of the curve is the average Seebeck coefficient with contribution from superlattice and silicon substrate It is known that seebeck coefficient is geometry independent thermodynamic property. This corresponds with the results in Figure 4, which shows size independent of effective seebeck coefficient. Table 1 summarizes the thermoelectric voltage measured in the experiments. It shows the sample $SiGe_{0.2}$:B with 3um superlattice thickness and doping concentration of $5\text{-}7 \times 10^{19}$ cm^{-3} has an average Seebeck coefficient of 135.4µV/°C.

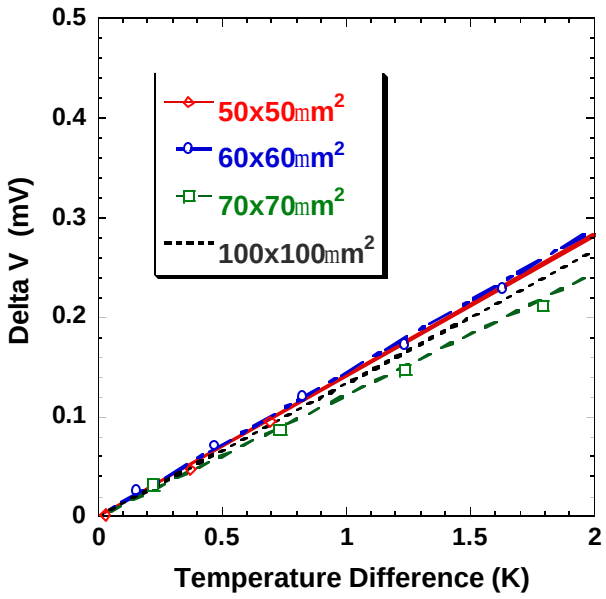

Figure 4 Thermoelectric voltage versus temperature difference between top of the device and bottom contact

Sample size (μmxμm)	Effective Seebeck coefficient (μV/^{0}C)
50x50	138±0.1
60x60	140.0±1.0
70x70	131.0±0.6
100x100	132.4±1.0
Average	135.4

Table 1 $Si_{0.7}Ge_{03}$ superlattice microcooler Seebeck coefficient data for different size samples

Venkatasubramanian's recent paper in Nature[2] reported the cooling performance is related to the thickness of the superlattice layer. To further investigate the influence of different superlattice thickness on the device property. We also measured the thermoelectric voltage for different superlattice thickness, 1um, 3um, and 6um. The results were illustrated in . It can be seen that thicker the superlattice thickness, higher the measured thermoelectric voltage 135μV/^{0}C, 154μV/^{0}C and 174μV/^{0}C for 1μm, 3μm and 6μm superlattice respectively. The increase of the thermoelectric voltage is due to the increase in the thermal resistance of the thin film device with respect to the substrate as superlattice becomes thicker. As illustrated in Figure 6 simplified thermal model of superlattice micro-cooler device, from the equation of

$$R_{th} = \frac{1}{b_{th}} * \frac{d}{A} \qquad \text{(Eqn.3)}$$

it is obvious to see R_{th}(SL): thermal resistance superlattice is proportional to the uperlattice thickness d_{sl}. The change of R_{th}(SL) directly influences T_s':

$$Ts' = Ts + \frac{R_{th}(Si)}{R_{th}(Si)+R_{th}(SL)} * \Delta T \qquad \text{(Eqn. 4)}$$

And it causes the change of effective seebeck coefficient:
S= [S2*(Th-T_s')+S1*(T_s'-T_s)]/DT (Eqn.5)

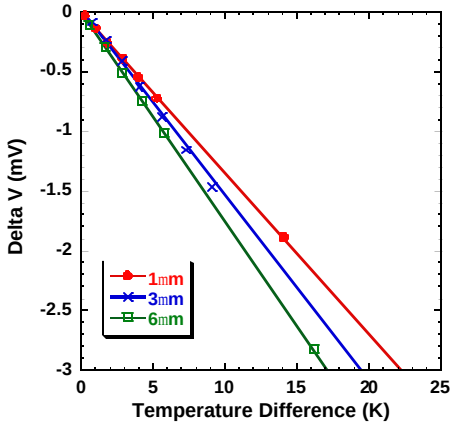

Figure 5 Comparison of seebeck coefficient with different superlattice thickness (fitted)

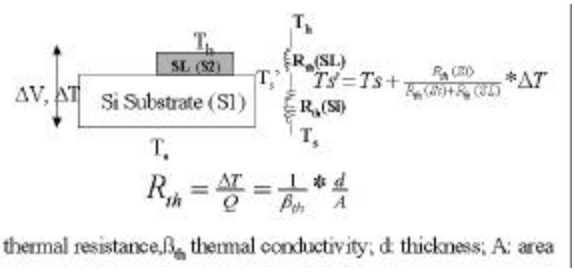

Figure 6 Simplified thermal model of superlattice micro-cooler (This model assumes the thermal resistance of the SiN_x and buffer layer is much smaller than the thermal resistance of the superlattice layer)

To calculate the actual Seebeck coefficient of superlattice, we need to know the T_s', which is related with the thermal resistance of the device. In this calculation, thermal resistance was obtained experimentally by using equation: $R_{th} = \frac{\Delta T}{Q}$ (Eqn. 6), ΔT is the temperature difference created, Q is the heat load on top of the device. The thermal resistance for a 100x100um^2 device based on bulk silicon R_{th}(Si) was 157.0 K/W, the measured thermal resistance of the device with different superlattice thickness were listed in Table 2. From the known of thermal resistance of bulk Silicon and that of the overall device (superlattice+substrate), the T_s' - T_s could be calculated by Eqn.4 assuming a temperature change of 10K. The ΔV of the device could be obtained by its effective Seebeck

cofficient. Then a pure superlattice of this structure S2 could be calculated by Eqn.2 with all the known data.
Table 2 lists all the calculation results and it showed an average seebeck coefficient of this structure superlattice is around 217.6 $\mu V/^0C$.

SL thickness	R_{th} (Device) (K/W)	ΔV (mV)	$T_s'-T_s$ (K)	S (SL) ($\mu V/^0C$)
1um	215.1	1.28	7.30	229.6±10.0
3um	322.3	1.54	4.87	205.3±10.5
6um	422	1.68	3.72	217.8±8.2
Ave. SL seebeck coefficient	217.6 $\mu V/^0C$			

Table 2 Calculation of superlattice thickness
(Sample size 100x100μm)

Conclusions

We showed that the integrated heater sensor on top of the thin films provides a convenient method to characterize the Seebeck of SiGe superlattice material. This will help further development and improvement of the performance of SiGe superlattice coolers.

Seebeck coefficient of ~217μV/K was measured for Si/SiGe superlattice p-doped to $5x10^{19}cm^{-3}$. The experimental results were verified by obtaining consistent results with various superlattice thickness (1-6um) and device sizes (2,500-10,000 μm^2).

Acknowledgements

This work was supported by the DARPA HERETIC program and the Army Research Office.

Reference

[1] Xiaofeng Fan etc. Applied Physics Letters, Vol. 78, No.11, 12 March 2001.
[2] Rama Venkatasubramanian et. al. "Thin-film thermoelectric devices with high room-termperature figures of merit", P597 Vo. 413, October 11th, 2001, Nature
[3] Xiaofeng Fan et. al. "Integrated Cooling for Si-based Microelectronics", International conference on Thermoelectrics, June 2001
[4] Xiaofeng Fan et. al. "High cooling power density SiGe/Si micro coolers" Elec. Lett., Vol. 37, No. 2, 18 January 2001
[5] T. Borca-Tasciuc et.al. Superlattices and Microstructure 28, 199 (2000)
[6] R. Venkatasubramanian, Phys. Rev. B 61, 3091 (2000)
[7] H. Beyer, et al Proc. 18th Int. Conf. Thermoelectrics, ICT'99, 687 (1999)
[8] R. Venkatasubramanian, Recent Trends in Thermoelectric Materials Research III, T. M. Tritt, Ed., Academic Press 71, 196 (2001)
[9] W. L. Liu et. al. J. Nanosci. And Nanotech. 1, 37 (2001)
[10] T. Yao, Appl. Phys. Lett. 51, 1798 (1987).
[11] Xiaofeng Fan etc. Applied Physics Letters, Vol. 78, No.11, 12 March 2001.
[12] CRC Handbook of Thermoelectrics, ed. by D.M. Rowe (CRC Press, Boca Raton, FL, 1995)
[13] Bao Yang et. al. "Characterization of cross-plane thermoelectric properties of Si/Ge Superlattices" Proceeding of 20th International Conference on Thermoelectrics (2001)