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LINEAR MODELS FOR LARGE SIGNAL CONTROL OF HIGH POWER FACTOR AC-DC CONVERTERS[1]

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Abstract

This paper shows that the *large* signal behavior of high power factor ac to dc power conditioners can be analyzed via *linear* models, by using *squared* output voltage as the state variable. The state equation for general loads (e.g. constant power plus resistive) is obtained by a simple dynamic power balance. Time invariant or periodically varying controllers, acting at the time scales of the line or switching periods respectively, are then easy to design from the resulting averaged or sampled data models.

Catagory: Modeling and Control

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LINEAR MODELS FOR LARGE SIGNAL CONTROL OF HIGH POWER FACTOR AC-DC CONVERTERS

1 INTRODUCTION

Recently, there has been much work on designing control schemes for high power factor ac to dc converters. Schlecht [1] introduces techniques for controlling the pole-zero locations of the time varying system, based on a quasi-static argument. Subsequent work has largely focused on the scheme shown in Fig.1, using a boost converter whose input voltage, $v_{in}(t)$, is the rectified ac waveform. The inner current loop specifies the switching sequence for the transistor in such a manner that the input current, $i_{in}(t)$, is regulated around a reference, $i_{cmd}(t)$, that is proportional to the input voltage. The outer voltage loop varies the proportionality constant, k, from cycle to cycle, to regulate the output voltage, $v_o(t)$, about the desired level, V_d. Several recent papers discuss different approaches to designing the inner and outer loops. Henze and Mohan [2] use a hysteretic current control loop, and implement the voltage control loop digitally using a simple PI controller, but some modeling aspects are left unclear. Williams [3] designs a controller using the small signal 'transfer function' between commanded input current and output voltage. While his analysis contains insight into the operation of the circuit, it is mathematically incorrect since it is based on Laplace transform operations on equations with time varying coefficients even though the conditions for quasistatic analysis do not hold. A correct small signal model and associated control design are provided by Ridley [4].

The present paper designs and simulates a high power factor control scheme for the boost converter shown in Fig. 1. Unlike previous papers, however, *large* signal *linear* models are developed for the voltage loop. This allows the simple design of control schemes that permit recovery from large perturbations away from the operating point. The modeling and control design are developed for the general case of a constant power load in parallel with a resistive load. The simulations presented in this paper illustrate the response using the constant power load only, since this is more relevant when the load itself consists of regulated converters. The simulations use the following component values:

$$L = 600\mu H \qquad C = 940\mu F \qquad P = 1100W$$
$$R = \infty \qquad v_{in}(t) = V|sin(120\pi t)| \qquad V = 200volts$$

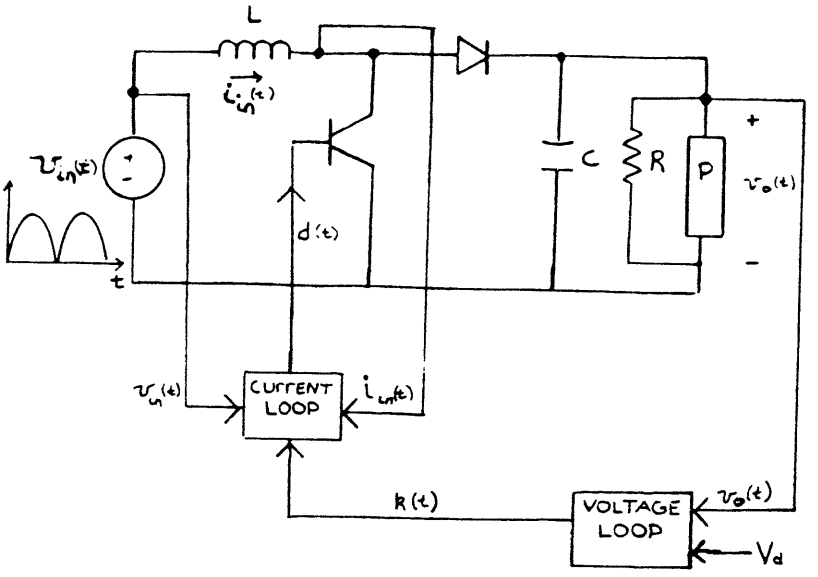

Figure 1: Boost Converter with Current and Voltage Control Loops

Section 2 describes the operation of the inner current loop shown in Fig. 1. Section 3 presents models for the dynamics of the outer voltage control loop. Finally Section 4 discusses the design of the outer control loop, including PI control, and presents simulation results for the behavior of the full closed loop system. Experimental verification is being planned, and results will be included in the final paper.

2 CURRENT LOOP DYNAMICS

The current loop is responsible for obtaining the high power factor by drawing a resistive current from the ac line. Its operation is illustrated in Fig. 2. At the beginning of every switching period, every T_s seconds, a decision is made to have the transistor on or off, as required to force the inductor current towards the switching boundary, $i_{cmd}(t)$. This is a compromise between usual fixed frequency operation and hysteresis band control. It provides a natural control implementation, given that the control is exercised periodically, and was shown in [5] to be effective in digital sliding mode control of the buck-boost converter.

The commanded input current, $i_{cmd}(t)$, is set according to:

$$i_{cmd}(t) = k(t)v_{in}(t) \tag{1}$$

where $k(t)$ is provided by the voltage control loop. In usual practice, $k(t)$ is held constant for the duration of the input period, T_L. Its value in Fig. 2 equals 0.055. The power factor during

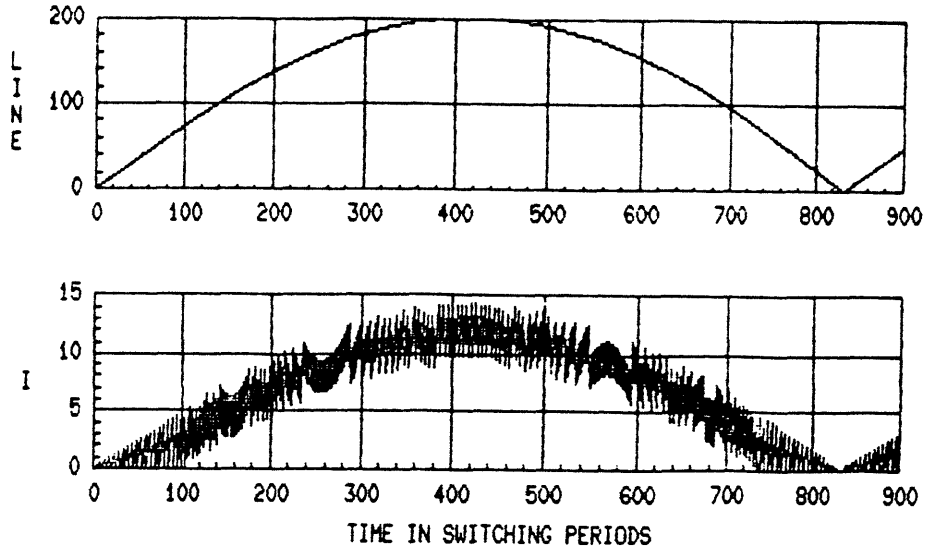

Figure 2: Current Loop

this line cycle is calculated to be 0.977. We shall also explore changing $k(t)$ within a cycle during transients, even as fast as every switching period; results on this will be presented in the full paper.

The running average, $i(t)$, of the input current over an interval T_S is defined by $i(t) = \frac{1}{T_S}\int_{t-T_S}^{t} i_{in}(\sigma)d\sigma$. It is reasonable to assume, when the current loop is working well, that $i(t) = i_{cmd}(t) = k(t)v_{in}(t)$.

3 VOLTAGE LOOP DYNAMICS

In this section, dynamic models for the outer control loop are obtained. Ignoring switching frequency ripple in the output voltage, $v_o(t)$, and assuming that the inner current loop maintains $i(t) = k(t)v_{in}(t)$, conservation of power for the boost converter is written:

$$\frac{1}{2}Cd[v_o^2(t)]/dt = k(t)v_{in}^2(t) - \frac{1}{2}Ld[k^2(t)v_{in}^2(t)]/dt - P - v_o^2(t)/R \qquad (2)$$

This already shows that the use of $v_o^2(t)$ as the state variable, instead of the more common $v_o(t)$, leads to an essentially *linear* model for *large* signal behavior. This observation has also been made by Sanders [6]. A variety of sampled data models (SDM) and averaged models that are more suited to control design can be obtained from (2). If $v_o(t)$ is taken as the state variable, (2) is a nonlinear description; linearization yields a small signal periodically varying model, which is the starting point for Williams' discussion of control possibilities [3].

To obtain an exact SDM on the level of the line frequency, (2) is integrated over the input period, $T_L = 1/120$ sec, assuming that $k(t)$ is constant over T_L. The resulting model, called the "T_L-exact SDM" is shown below, with $k(t)$ in the n^{th} cycle denoted by $k[n]$ and $v_o^2(t)$ at the beginning of the n^{th} cycle by $v_o^2[n]$:

$$v_o^2[n+1] = \exp(-2T_L/RC)v_o^2[n] + (V^2k[n] - 2P)T_L/C \tag{3}$$

Since the regulation of v_o about its desired level V_d can be accomplished by regulating v_o^2 about V_d^2, an alternative state variable $x[n]$ is defined as:

$$x[n] = v_o^2[n] - V_d^2 \tag{4}$$

$$x[n+1] = \exp(-2T_L/RC)x[n] + (V^2k[n] - 2P)T_L/C \tag{5}$$

Note that $x[n]$ is *not* restricted to be small. When $R \to \infty$ we obtain the result for a constant power load and when $P = 0$ we obtain the result for a purely resistive load. Hence, assuming that the inner control loop successfully maintains $i(t)$ at its commanded value $i_{cmd}(t)$, the dynamics of the boost converter are completely described by the single linear, time invariant difference equation (5), with state $x[n]$ and control $k[n]$. If $v_o[n]$, rather than $v_o^2[n]$, is taken as the variable of interest, (3) is nonlinear; linearization yields a small signal time invariant model that turns out to be the same as what Williams [3] obtains through heuristic and not very satisfying arguments.

The exact SDM on the level of the switching frequency is derived in a similar manner, by integrating (2) over the switching period T_S. Assuming that $k(t)$ is constant over T_S, the resulting model, called the "T_S-exact SDM", can be derived, and will be given in the full paper.

To obtain an *averaged* model on the level of the line frequency, (2) is averaged over T_L using the fixed lag average defined by $\bar{w}(t) = \frac{1}{T_L}\int_{t-T_L}^{t} w(\sigma)d\sigma$. Denote $\bar{v_o^2}$ by $y(t)$. (If the line frequency ripple is small, then $y(t) \approx \bar{v_o}^2$.) Assuming that $k(t)$ varies slowly enough to be considered constant over any interval of length T_L, the averaged model is given by:

$$dy(t)/dt = -2y(t)/RC + (V^2k(t) - 2P)/C \tag{6}$$

This form already suffices to design controllers (e.g. PI controllers) for *large* deviations in $y(t)$. In contrast to this, Ridley [4] and Williams [3] work with linearized models, and therefore only guarantee good control for small perturbations. We will explore sampled data control as an alternative, since it is less familiar, and to take better account of the fact that $k(t)$ in present practice is set only once per input cycle. Integrating (6) over T_L results in the following model,

called the "T_L-averaged SDM":

$$y[n+1] = \exp(-2T_L/RC)y[n] + [V^2k[n] - 2P]T_L/C \tag{7}$$

The T_L-exact SDM (3) and the T_L-averaged SDM (7) are the same because the differential equation (2) is periodic in T_L, so integrating over T_L to obtain a sampled data model has the same effect as first averaging and then integrating.

4 CONTROL DESIGN

For purposes of illustration, the control design and analysis will proceed with the T_L-exact SDM with the constant power load. In steady state, $x[n+1] = x[n] = 0$, so the constant control $k[n] = K$ required to maintain equilibrium in steady state is seen from (5) to be:

$$K = 2P/V^2 \tag{8}$$

which varies as $1/V^2$. Rewriting the control as $k[n] = K + u[n]$ reduces the state equation (5) to:

$$x[n+1] \;=\; x[n] + V^2T_Lu[n]/C \tag{9}$$

Specifying the control to be in state feedback form,

$$u[n] = -Cbx[n]/(V^2T_L) \tag{10}$$

yields the closed loop model

$$x[n+1] = (1-b)x[n] \tag{11}$$

The constant b is chosen to place the pole $z_p = 1 - b$ at a desired location. (A similar choice of control is made in [6].)

Placing the pole at $z_p = 1/2$ and initiating the output voltage with a 50% initial perturbation away from equilibrium results in the output voltage transient shown in Fig. 3 for the model (10), (11). The output voltage starts at $v_o = 173$ volts and requires approximately 8 input periods to attain the desired level $V_d = 346$ volts.

Before connecting the voltage loop to the current loop, the range of values of $k[n]$ specified by the voltage loop must be checked for consistency with the range allowed by the current loop.

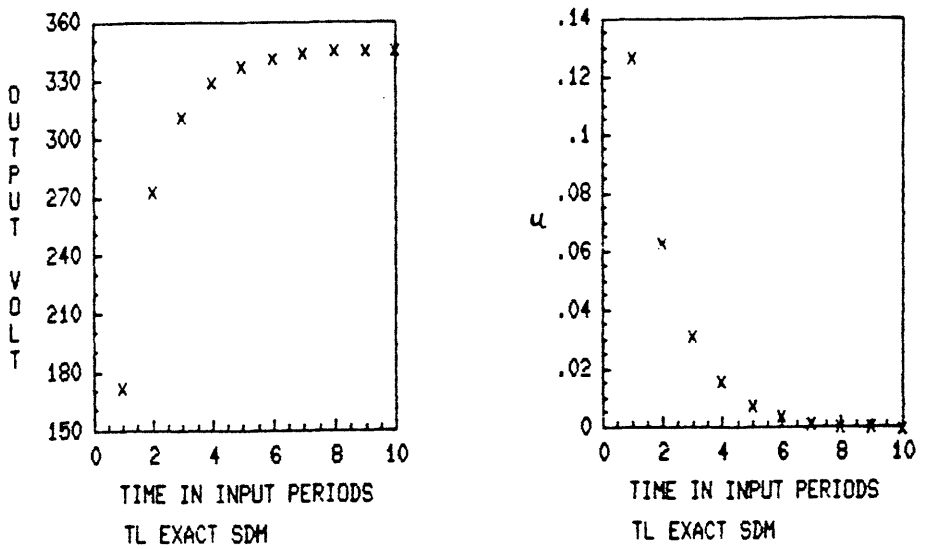

Figure 3: Voltage Loop with Initial Perturbation

For instance, if $k[n]$ is too large, then the inductor current will be unable to rise fast enough to follow the commanded current $i_{cmd}(t) = k(t)v_{in}(t)$. In this example $k[n] = K = .055$ results in the current response shown in Fig. 2. Further simulations demonstrate that for $k[n] < .5$, the input current is able to follow its commanded value $i_{cmd}(t)$. Consequently, for $k[n]$ in the vicinity of K the full closed loop system will perform as expected. In particular, for the transient in Fig. 3, the current loop will perform as desired.

Results

Figure 4 shows the response of the full closed loop system to an initial 50% perturbation away from the desired output voltage level, $V_d = 346$ volts. As predicted by the voltage loop simulation in Fig. 3, the transient has decayed in about 8 input periods. In Fig. 4, each input period T_L is approximately equal to 830 switching periods T_S. The power factor corresponding to each cycle of the current response in Fig. 4 is shown in Fig. 5. The power factor in steady state is close to the power factor of the open loop response in Fig. 2.

Figure 6 illustrates the response of the full closed loop system to an unanticipated step change in output power at $t = 2000$. At that time, the power in the load is stepped by 50% from 1100 watts to 1650 watts. The output voltage attains a new cyclic steady state, but exhibits a dc offset of approximately 30 volts, or 9%. In order to correct for the effect of such uncertainties in the load power, integral control must be incorporated into the voltage loop

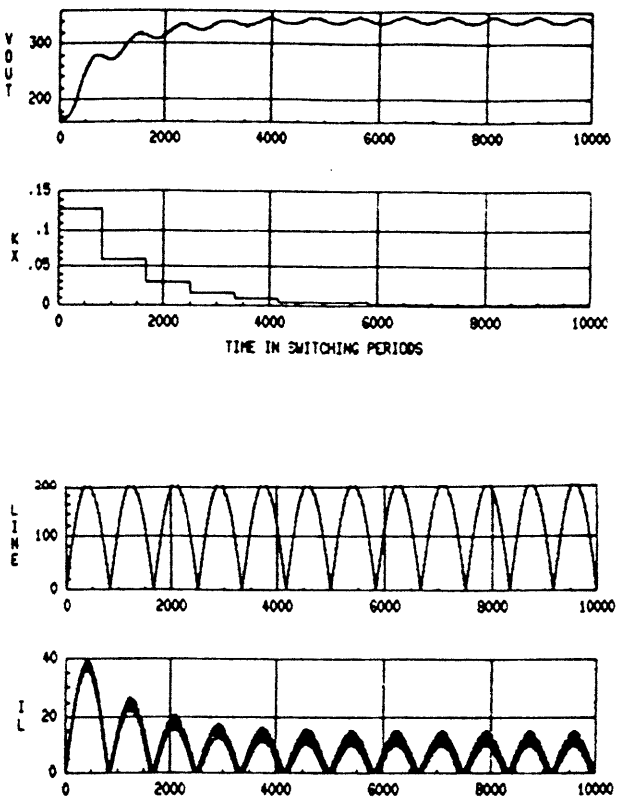

Figure 4: Closed Loop System with Initial Perturbation

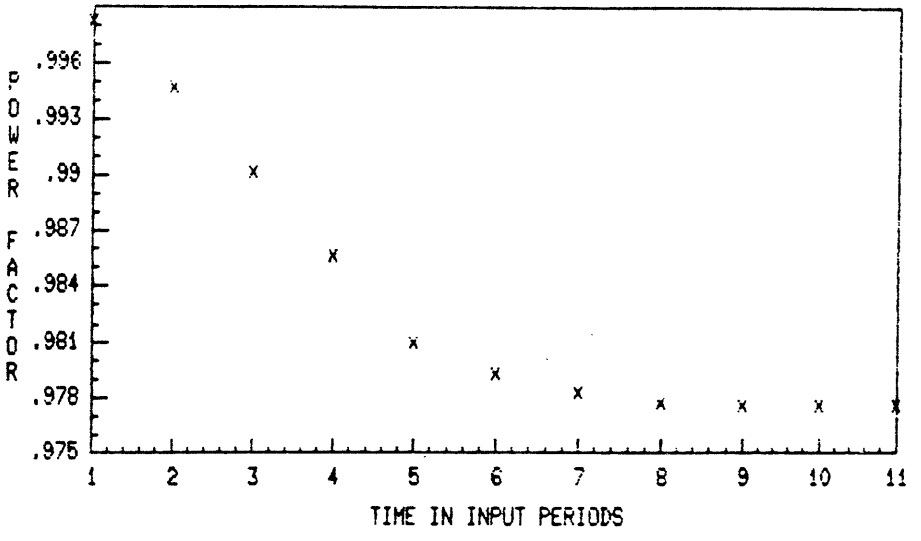

Figure 5: Power Factor

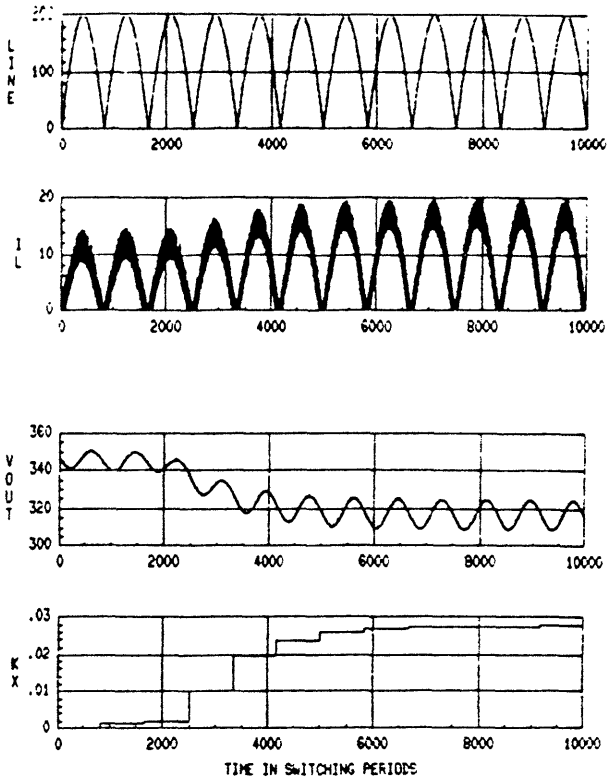

Figure 6: Closed Loop System with Step Change in Constant Power Load

control scheme, as shown in Fig. 7. The state equations for the outer loop are given by:

$$q[n+1] = q[n] + x[n] \tag{12}$$

$$x[n+1] = -b_I q[n] + (1 - b_P)x[n] \tag{13}$$

The design and simulation using integral control will appear in the full paper.

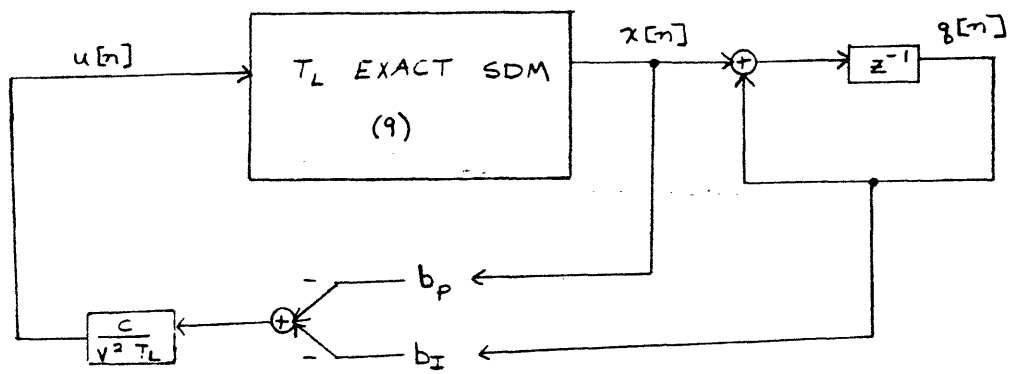

Figure 7: Voltage Loop with Integral Control

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