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14. ABSTRACT
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Silicon ... Beyond Silicon: Beginning of the End or End of the Beginning?

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1. Introduction

In the early 1960's, at the beginning of the electronics revolution, silicon integrated circuits built their current dominance fundamentally and pervasively on tailor-made materials, starting at the atomic level. Early development in thin-film deposition techniques, particularly chemical vapor deposition (CVD) and molecular beam epitaxy, led the way to accurate control over material constituents in "atomic amounts," in order to form the active part of high-performance devices.

In the early 1970's, our team at Space and Naval Warfare Systems Center, San Diego, focused its vision to achieve a structure based on CMOS, an unknown and unproven technology at that time. One important attribute of that vision was the affordable implementation using devices with ever-increasing speed, wider bandwidth and lower power dissipation. During the eighties and nineties, CMOS became the mainstay technology and workhorse of the electronics revolution. It remains the dominant circuit configuration in today's systems because it offers low power, the largest signal-to-noise ratio, process simplicity, and flexibility in design. In this context,

- while new materials and highly engineered novel structures, such as silicon-germanium (SiGe) and silicon-on-insulator (SOI) for computing devices and processors, have demonstrated an incremental improvement in performance,
- our pursuit of the integration of SiGe on sapphire substrates has led to truly outstanding device performances that could not otherwise be obtained. The SiGe-on-sapphire configuration has helped integrate for the first time, without loss of performance, both analog and digital functions.

We have, therefore, projected increased levels of integration, increased performance, and lower cost for future integrated systems-on-a-chip. These systems will continue to fuel the exponential improvements predicted by Moore's Law, *e.g.* sub-50-nm devices, many tens of GHz speeds (f_T, f_{max} in excess of 200 GHz for both carriers) and billions of transistors per chip by the year 2010. These systems also will enable new applications to be realized at the high end of the performance spectrum. The driving force for the continuing explosive growth of

the semiconductor industry, which doubles in size every 3.5 years (a corollary of Moore's Law) is continued process improvement. That was also demonstrated; CMOS on SOS reduces process complexity, as well as parasitic capacitance loading. Moreover, the introduction of Ge into the silicon wafer offers novel structures in strained material (tensile Si or compressive SiGe layers, 3–10 monolayers thick), fixes some existing device problems, and enhances performance without major complexity or cost penalties.

The advances resulting from the developments carried out in the context of our first visionary technological push have led to the investigation of SiGe on sapphire, a new vision for the next decade. Therefore, we will discuss the "past" results, as a prelude to the "present," with compelling reasons to pursue our new vision of CMOS on SiGe on sapphire.

2. The past

Silicon-on-sapphire (SOS) has all the advantages of other SOI technologies as well as many others specifically relevant to microwave circuits. These advantages include reduced self-heating effects (due to sapphire's higher thermal conductivity, 0.46 W/cm·K, compared to 0.014 W/cm·K in SiO_2), reduced device parasitic capacitances, radiation hardness, reduction of latch-up in CMOS structures, higher packing density, and improved isolation. SOS also has lower minority carrier lifetimes (~1 ns) that result in a higher source-drain breakdown voltage and a reduced parasitic bipolar gain. Another SOS characteristic to note is that the silicon film is under compressive stress. This stress splits the light and heavy hole valence bands leading to increased hole mobilities over that of bulk silicon. At the same time, this stress also causes lower electron mobilities as compared to bulk, similar to the effects seen in SiGe on Si. In SOS, *p*-MOS and *n*-MOS devices are more closely matched than in other CMOS variants.

Sapphire, and more generally polycrystalline sapphire (alumina), is known to have excellent dielectric properties. The dielectric constant, dielectric loss tangent, and resistivity of sapphire are $\varepsilon_r = 9.39$, $\tan\delta < 0.0001$ at 3 GHz, $\rho = 10^{14}$ Ω·cm. Hence, in addition to the desirable traits of other SOI technologies, sapphire wafers make excellent microwave substrates for passive elements such as transmission lines and inductors, allowing on-chip integration with active devices.

The development of SOS started with Manasevit *et al.*,[1] who described a technology to achieve single-crystal silicon on a sapphire substrate in 1964. Since then, as evidenced from several well documented reviews,[2,3] the technological advances achieved for SOS can be traced, in parallel, with the evolutionary establishment of the silicon VLSI industrial infrastructure from *p*-MOS to *n*-MOS to *n*-MOS E/D and to the current workhorse CMOS. In the late 1970's, Lau *et al.*[4] demonstrated that the crystalline quality of SOS films could be improved by utilizing a silicon implant to create a buried amorphous layer followed by a thermal anneal, which causes regrowth of an improved film from the surface downward. This process is labeled "solid phase epitaxy" (SPE).

The application of the technique has caused a resurgence in the interest in SOS technology for its use in high-speed low-power CMOS circuitry implemented with sub-micrometer minimum device feature size. Almost concurrently, two research teams[5,6] applied the SPE (or double-SPE, DSPE) process to achieve device-quality crystal in 200-nm thin-film silicon on sapphire. G. Garcia and R. Reedy[7,8] extended their work to 20-nm thin films, commensurate with a 80–100 nm minimum device feature size. Three main observations were made. First, no aluminum out-diffusion from the substrate was observed, as shown from the SIMS profiling (Fig. 1). The SIMS data give a uniform background concentration for ^{27}Al of approximately $1–3\times10^{15}$ cm^{-3}, within the minimum detection margin of error for both the bulk Si and the DSPE-improved SOS samples.[6] Secondly, higher carrier mobilities (μ_e = 500, μ_p = 200 $cm^2/V{\cdot}s$) were noted, along with a drastic reduction (albeit not elimination) of deep traps ($<10^{11}$ cm^{-2}) associated with the Si/sapphire interfacial region. The essential steps of the DSPE technique are deep amorphization by a 170 keV ^{28}Si implant at a dose of 1×10^{15} cm^{-2} followed by a thermal anneal of 550 °C for 2 hours, then 1050 °C for 1 hour. The top surface of the Si film is then rendered amorphous by a 100 keV Si implant at a similar dose of 1×10^{15} cm^{-2} followed by the same anneal cycle. Thinning the film is accomplished by growth of an oxide at 875 °C in steam. The film thickness is measured by interferometry and spreading resistance.

The 2.2 MeV $^4He^+$ channeled RBS data and the high resolution TEMs of both "as-received" (non-implanted or non-improved) SOS and DSPE-improved SOS samples are shown in Fig. 2. The virtual elimination of "twin" defects and the $^4He^+$ de-channeling in the DSPE-improved SOS wafers coming very close to that obtained for the bulk silicon demonstrate the substantial improvement achieved.

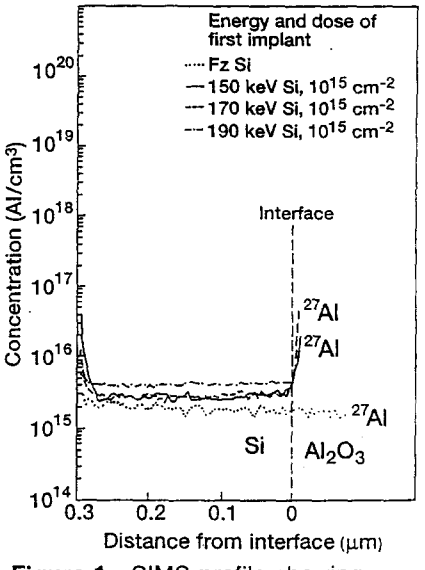

Figure 1. SIMS profile showing absence of Al in Si layer.

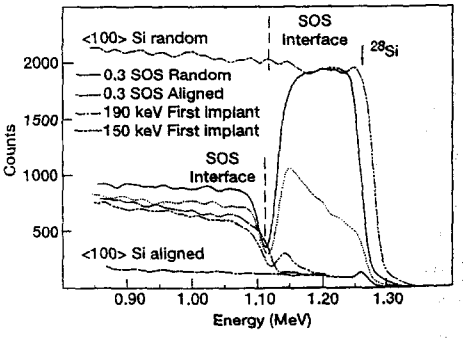

Figure 2. Channeled RBS data of as-received and DSPE-improved SOS samples for two different implant energies (150 and 190 keV).

3. The present

The measured characteristics of a front-end receiver at 2.4 GHz[9] and frequency dividers[10] at >20 GHz illustrate a real technological renaissance for silicon-on-sapphire. The demonstrated performance, unachievable in bulk silicon technologies, of a transmit/receive switch, mixer, and low noise amplifier[9] make possible the integration of an rf front end and VLSI digital circuits on the same substrate. The resulting system-on-a-chip implementation can reduce cost and increase overall performance for functions targeted at wireless/satellite communications, radar, image processing and others in the military, industrial, scientific, and commercial sectors.

A specific requirement for the function of the transmit/receive (TR) switch, needed to connect the antenna to the receiver chain (receive mode) or the transmitter chain (transmit mode), is that of very low insertion loss. It is important not to degrade the signal-to-noise ratio prior to the low-noise amplifier on the receive side, or reduce the efficiency on the transmit side. In addition, nonlinearity must be small to accommodate large output power and isolation from one side to the other must be high. The measured data demonstrates the excellent suitability to this combination of requirements of the switch implemented in DSPE-improved SOS. The insertion loss is around 1.7 dB and the isolation is greater than 30 dB at 2.4 GHz. At 5 GHz, the insertion loss increased from 1.7 dB to only 2.0 dB and the isolation remained greater than 25 dB; while the isolation is the same, the insertion loss for SOS is three times lower than for SIMOX. The switch also displays excellent linearity and power handling capability. The two-tone measurements (f_1 = 2.4 GHz, f_2 = 2.425 GHz) show an input-referred third order intercept point (IP3) of 18 dBm.

The mixer, used in up- and/or down-conversion of the carrier frequency (rf or 2.4 GHz) to the intermediate frequency (IF or 250 MHz) has good isolation of rf and the local oscillator (LO at 2.15 GHz, 0.7 dBm power), as well as high IP3 (5 dBm) and low noise figure. Unlike III-V HBTs, the selected SOS design targets high IP3 (18 dBm) with little gain (the SOS mixer has 5 dB conversion loss), as it is easier to increase the gain in the receiver chain than to increase IP3.

The one-stage low-noise amplifier (LNA), a critical element of the receive path, has very low noise as well as high gain and output IP3 (OIP3) compared to a 2-stage HEMT LNA. Spiral inductors and MIM capacitors were used to match the FETs to the minimum noise figure at Γ_{opt}. The LNA was operated at V_{DS} = 1.5 V and V_{GS} = 0.7 V. The dc current consumption at low input power levels is 8.8 mA (while it rises to 9.9 mA for an input power corresponding to the 1 dB compression point). This corresponds to an average power dissipation of 14 mW. Using the spiral inductors, the LNA is well matched for gain (10 dB) and noise figure (2.8 dB) at 2.4 GHz. Two-tone (f_1 = 2.4 GHz, f_2 = 2.425 GHz) linearity measurements of the LNA were performed. The output referred 1-dB compression point and third order intercept (OIP3) are 4 dBm and 14 dBm, respectively.

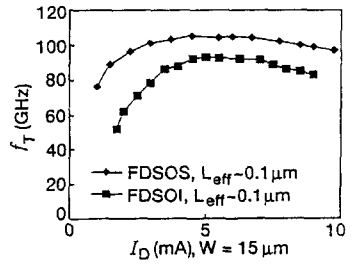

Figure 3. Transition frequency f_T *vs.* I_D for fully-depleted SOS and SOI.

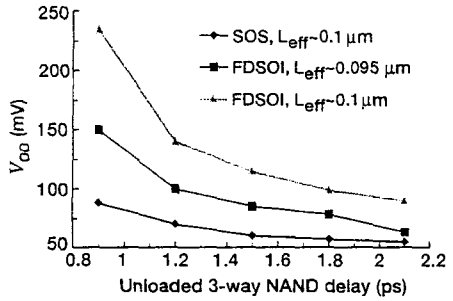

Figure 4. Unloaded 3-way NAND delay (ps) for SOS and fully-depleted SOI.

These results represent the highest-frequency CMOS low-noise amplifier reported to date.[11,12] The noise characteristics of this LNA are similar to Si bipolar circuits and satisfy wireless requirements. On the basis of simulation, even lower noise figure would be possible if the metal thickness used to realize the on-chip inductors were greater. The excellent linearity observed may be attributed to the good turn-off and low output conductance of the SOS FETs, together with the absence of the body effect. The combination of low noise figure, high OIP3, and low power consumption is desirable for wireless receiver circuits.

With further scaling, fully depleted devices with 100-nm gate length on 30–40 nm thin DSPE-improved SOS were characterized and were compared to similar devices implemented on SOI and bulk Si substrates. The 100-GHz f_T data for SOS are shown in Fig. 3; the heating effect in SIMOX devices is responsible for the lower value of f_T.

Very fast unloaded CMOS switching speeds have been observed (<10 ps delay). For three-way NAND ring oscillators, SOS devices are faster than SIMOX

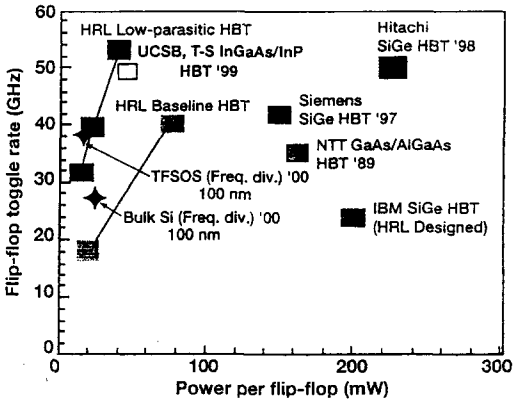

Figure 5. Flip-flop toggle rate *vs.* power per flip-flop in different technologies.

ones because of the higher hole mobility and lower threshold voltage (Fig. 4). Circuit functions such as a frequency divider[10] at 26 GHz have the highest frequency of operation for similar Si functions. Figure 5 compares several material implementations of the frequency divider.

4. The future

Recent advances in SiGe epitaxial growth indicate that SiGe-based strained-layer MODFETs may be promising alternatives to III-V MESFETs and HEMTs for future high-speed analog communications applications. Electron and hole mobilities well in excess of bulk Si mobilities can be realized in tensile-strained Si quantum wells (QWs)[13] and compressive-strained SiGe[14] or pure Ge QWs,[15] respectively. These improvements have led to *n*-MODFETs with f_T = 62 GHz[16] and f_{max} = 120 GHz[17] and *p*-MODFETs with f_T = 70 GHz and f_{max} = 85 GHz.

Höck[18] and Hammond *et al.*[19] have both investigated a Ge QW grown on a $Si_{0.4}Ge_{0.6}$ relaxed buffer layer and showed the impressive performance of the Ge-channel MODFETs. However, a significant drawback of these devices is the high Ge content (60%) of the relaxed buffer layer which leads to increased surface roughness and defect density. In addition, 60%-Ge-content relaxed buffer layers are not well suited for integration with strained Si channel *n*-MODFETs.

We have observed that the *p*-MODFETs dc and rf performance figures are comparable to those of *n*-MODFETs suggesting the possibility of very high-speed complementary operation,[20] a capability not available in current III-V technology. Furthermore, *p*-MODFETs may actually be preferable to *n*-MODFETs for unipolar applications due to their comparable performance and the fact that they

tend to be simpler to fabricate, particularly for self-aligned T-gated devices. Channels grown on buffer layers with $x < 40\%$ are much more attractive from a technological point of view, because they have better surface quality and are compatible with *n*-MODFETs. In order to address this issue, a new "composite-channel" layer structure design that utilizes a 30–35%-Ge-content buffer layer was developed. This heterostructure is still capable of producing hole mobilities as high as 1300 cm^2/Vs. In our work, we have applied the knowledge of material properties to the growth of strained layers of $Si_{0.2}Ge_{0.8}$ on relaxed $Si_{0.7}Ge_{0.3}$ layers on thin-film SOS for the fabrication of SiGe *p*-MODFETs.

Losses due to the conductivity of the Si substrate used in standard SiGe MODFET designs is another serious obstacle for applications in the microwave frequency regime. Insulating substrates, such as sapphire, provide an optimum solution. We have demonstrated the epitaxial growth of high-mobility modulation-doped composite-channel heterostructures on SOS substrates, and described the resultant outstanding rf characteristics of ≤100 nm T-gate *p*-MODFETs fabricated on these layers.

The composite-channel heterostructure device[21] on SOS has the following basic structure. A $Si_{1-x}Ge_x$ graded layer is first grown where the Ge alloy composition is increased from $x = 0$ to 30%. This layer is followed by a constant-alloy-composition $Si_{0.7}Ge_{0.3}$ layer, a 3.5-nm $Si_{0.7}Ge_{0.3}$ boron-doped supply layer, a 5-nm $Si_{0.7}Ge_{0.3}$ offset layer, an 8.5-nm $Si_{0.2}Ge_{0.8}$ QW, and finally a 9-nm $Si_{0.7}Ge_{0.3}$ capping layer. The quantum well is grown by nucleating a thin (<1 nm) Ge seed layer, followed by the 80% channel, thereby creating a "composite-channel" layer structure. This layer structure was grown on an SOS substrate as well as on a bulk Si control wafer. The devices had a gate length of 100 nm.

The room-temperature Hall mobility and sheet carrier density[21] of this composite-channel layer structure grown on an SOS wafer were 800–1200 $cm^2/V{\cdot}s$ and $3.1–2.5\times10^{12}$ cm^{-2} at room temperature, respectively. The room-temperature output (transfer) characteristic for devices with 100-nm gate length showed practically no difference between SOS and Si. Experimental data has also shown that the best SOS transistor has a maximum extrinsic transconductance of 377 mS/mm which is, to the authors' knowledge, the highest ever reported for alloy-channel *p*-MODFETs. The device has a corresponding output conductance of 25 mS/mm leading to a maximum dc voltage gain of 15. The only apparent degradation of the device performance due to the SOS substrate is a roughly one-order-of-magnitude higher gate leakage current compared to the Si monitor, a result that we again attribute to the increased defect density of the SOS wafers.

Figure 6 shows frequency-dependent plots[22] of the forward current gain ($|h_{21}|^2$) and the maximum unilateral gain (MUG) for a 0.1×50 μm^2 *p*-MODFET on SOS. Values of $f_T = 49$ GHz and $f_{max} = 116$ GHz, were obtained after de-embedding the contact pads; the latter value being the highest f_{max} ever reported for a SiGe *p*-MODFET. Figure 7 illustrates the fact that f_T and f_{max} saturate at a very low bias voltage; f_{max} reaches 100 GHz at $V_{DS} \sim -0.6$ V and is sustained over a wide bias range. Figure 8 further indicates low noise at high frequencies. This performance level should enable an entirely new technology. One of the characteristics of SOS

technology is the higher hole mobility, as the transport of carriers is through "light" holes. Therefore, a primary driving factor in pursuing SOS investigation has been to increase the performance of the *p*-channel FET through higher hole mobility, to enhance CMOS circuitry performance. In this context, our objective is to increase *p*-channel mobility to a level close or equal to *n*-channel mobility in CMOS circuitry by use of a SiGe heterostructure MODFET.[23–25] By confining the holes to an undoped channel away from the Si/SiO_2 interface in a strained layer where the hole mobility is enhanced, a significant improvement in hole transport can be realized. More recently, 3–4× increases in both hole mobility and electron mobility using SiGe films with high levels of germanium (>70%) have been

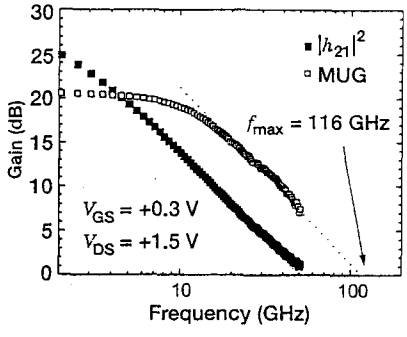

Figure 6. Highest reported f_{max} = 116 GHz for a *p*-FET in any material system (0.1 × 50 μm² composite-channel SiGe *p*-MODFET on SOS).

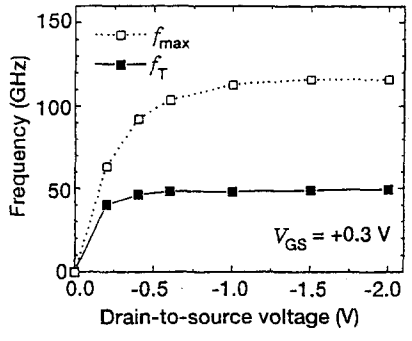

Figure 7. The f_T and f_{max} saturate at a very low bias voltage; f_{max} reaches 100 GHz at V_{DS} ~ –0.6 V.

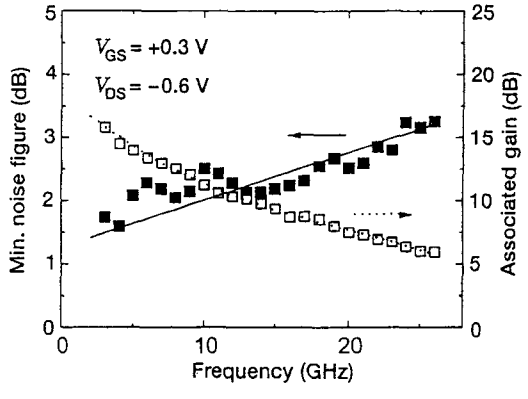

Figure 8. Minimum noise figure and the associated gain *vs.* frequency for a 0.1×90 μm² *p*-MODFET on SOS.

reported.[26] Performance of both polarity devices can be enhanced in the same set of layers using tensile strained Si on relaxed SiGe for the *n*-channel devices and compressively strained high-germanium-content SiGe layers for the *p*-channel devices. This structure requires, however, thick SiGe graded buffer layers, which are incompatible with ultrathin silicon-on-insulator technology. Epitaxially grown silicon-on-sapphire (SOS) has micro-twin densities (after improvement) in the 10^4 cm^{-2} range, resulting in an equal density of large faceted pits on ultra-high vacuum chemical vapor deposition (UHV-CVD) grown SiGe *p*-MODFET wafers. We should expect similar issues with deposited SiGe layers on sapphire, as discussed above. Although individual devices have been fabricated and tested on such wafers, the high density of pits makes these substrates unsuitable for ICs. Additionally, it is necessary first to grow a strain-relieved (600–800 nm thick) SiGe buffer layer[27,28] underneath the active layers, reducing the advantages of using a sapphire substrate.

However, the technique of bonding a thin (<100 nm) relaxed layer of $Si_{1-x}Ge_x$ (x < 35%) provides a greater potential for an affordable reliable substrate, compatible with the deposition of strained $Si_{1-x}Ge_x$ (x > 70–75%) on the defect-free relaxed $Si_{1-x}Ge_x$ (x < 35%) layer. It is well known that wafer-bonding methods rely on van der Waals attractive forces between the mirror-polished surfaces. The use of an interfacial medium between them, subsequent high temperature annealing, and a complete understanding of the underlying physical, chemical and electrical bonding processes are a prerequisite to achieve a permanently reliable bond of a very thin crystalline semiconductor to a supporting, preferably insulating, substrate.

A case in point is the successful "Smart-Cut" approach from SOITEC[29] which is, incidentally, not suitable for rf mixed-signal functions (integrated on a single chip) due to the high conductivity of the Si substrate. Other attempts to bond a thin Si layer on sapphire,[30–32] with and without an intermediary compliant SiO_2 medium, have met with various degrees of success. The presence of a thin oxide layer (>20 nm) prevents the void formation that is induced by poor water absorption by the native oxide. Due to the ready availability of sapphire substrates with a "bonding" finish, development focuses on materials integration alternatives and issues in order to achieve a stable interface at high temperatures (>550–850 °C). The next two figures[33] illustrate the evolution of this approach, from direct bonding of Si or SiGe on sapphire, to the use of SiO_2 as an integration medium that functions as a "sponge" for bond reaction products (H_2O, OH, H_2) to avoid the formation of bubbles at the interface during annealing.

Figure 9[33] illustrates the direct room-temperature bonding of a 92.5-nm thin silicon layer to sapphire, resulting from thinning the original bulk Si wafer. The bonding area is close to 75% of the 100-mm diameter of the substrate. Subsequent to the thinning, the annealing at 550 °C for 15 minutes results in a blistered film delaminated due to the expansion of trapped vapor at the interface. Also, the (004) high-resolution x-ray diffraction (HRXD) rocking curve data are compared to the theoretical calculation of the rocking curve from a defect-free Si layer. There is

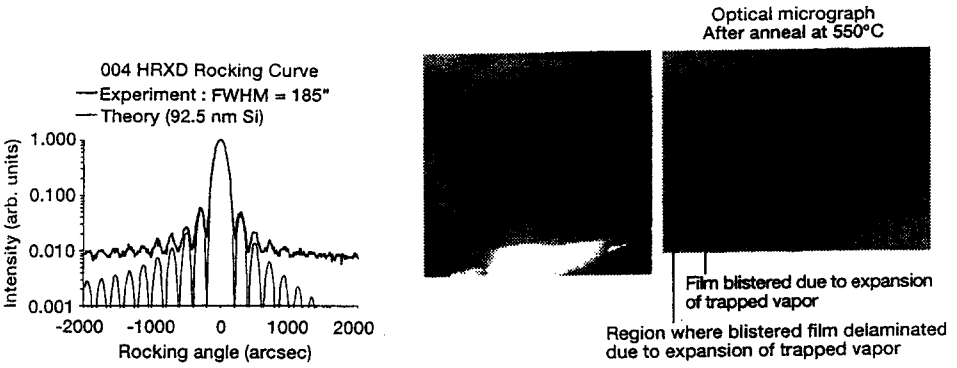

Figure 9. High-resolution x-ray (004) rocking curve data recorded from a 92.5-nm Si layer directly bonded to a sapphire wafer at room temperature, compared to the theoretical calculation of a rocking curve from a defect-free Si layer (a). There is good agreement between experiment and calculation. The result of thermally cycling the directly-bonded SOS structure to 550 °C (b).[33]

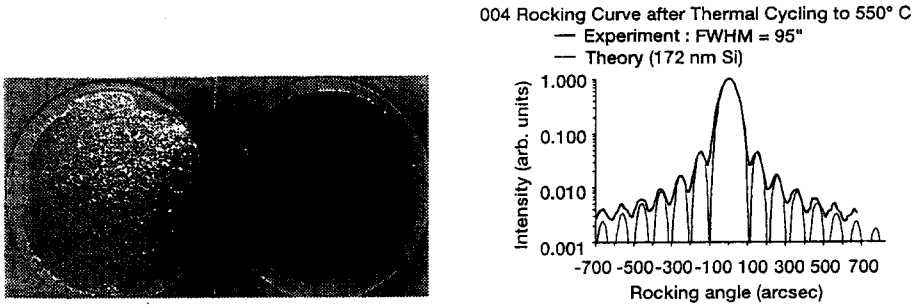

Figure 10. Photographs comparing the results of thermally cycling two SOS structures to 550 °C (the left wafer has no intermediary dry oxide at the bonded interface, whereas the right wafer has a 350-nm dry oxide). An x-ray diffraction (004) rocking curve from a bonded structure with an intermediate dry oxide after thermal cycling to increasingly higher temperatures (right). The rocking curve is compared to a theoretical calculation corresponding to a defect-free Si layer.[33]

agreement between experiment and calculation. The bonded silicon layer is relaxed.

Figure 10[33] demonstrates the results of thermally cycling two SOS structures to 550 °C. The structure on the left has no intermediary dry oxide, whereas the one on the right has a 350-nm dry oxide at the bonded interface. No additional blisters are observed if the sample on the right is subsequently cycled up to 850 °C. The dry oxide absorbs the interfacial OH groups that would otherwise form blisters. The experimental (004) rocking curve is shown for the wafer structure on

the right, after thermally cycling the bonded structure to increasingly higher temperatures. The data is compared to a theoretical calculation of the rocking curve from a defect-free Si layer. The bonded structure can be thermally cycled to 550 °C without the introduction of enough structural defects to broaden the rocking curve. Also, as was observed in Fig. 9, the bonded structure with the intermediate dry oxide is relaxed.

5. Conclusions

The incorporation of thin-film SiGe or Si on sapphire (either through SPE or bonding) leading to strained SiGe heterostructure *n*- and *p*-FETs characterized by superior transport carrier properties, high dynamic performance ($f_T, f_{max} > 200$ GHz), and low noise (~1–1.5 dB at 20 GHz) at high frequencies will enable an entirely new technology. This technology combines low-power high-speed analog and digital CMOS functions capable of very large scale integration, comparable to (if not higher performance than) III-V MESFETs and HEMTs, and at a greatly reduced cost due to compatibility with the Si CMOS IC manufacturing infrastructure. This enhanced silicon technology will enable the implementation of truly single-chip systems. These highly integrated systems will cost less to produce, occupy less volume, and draw less power than the same system realized with several chips. The incorporation of sapphire, an optimum rf substrate, will provide the required isolation between the front end and the noisy digital back-end functions, thus eliminating the need for III-V low-noise amplifiers. The resulting impact of the combined thin-film SOS and SiGe technology on the marketplace, both nationally and internationally will be quite revolutionary, as no other material can provide a complementary technology as efficiently, both technically and economically.

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