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1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
30-06-2006	Final Technical	01-07-2005 - 31-03-2006

4. TITLE AND SUBTITLE
Assembly of Ultra-Dense Nanowire-Based Computing Systems

5a. CONTRACT NUMBER

5b. GRANT NUMBER
FA9550-05-1-0444

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
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5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Air Force Office for Scientific Research
875 North Randolph St.
Suite 325, Room 3112
Arlington, VA 22203
Dr Anne Matsuura/NE

10. SPONSOR/MONITOR'S ACRONYM(S)

AFRL-SR-AR-TR-06-0390

12. DISTRIBUTION/AVAILABILITY STATEMENT
Distribution Statement A: unlimited

13. SUPPLEMENTARY NOTES

20061102537

14. ABSTRACT

Effective ultra-dense integrated digital information processing strains the leading edge of current chemistry and materials science, and requires hybrid top-down and bottom-up assembly techniques, with highly reliable defect- and fault-tolerant architecture. We have fabricated and assembled molecular-scale logic elements based on overlapping semiconducting nanowire arrays using novel wafer-scale assembly techniques. Based on breakthrough addressing techniques, we have connected these logic blocks to ultra-dense memory blocks, and to external CMOS-process lithographic interfaces for testing as well as test applications. Our architecture to construct highly reliable components out of high-defect-density logic and memory, using new sublithographic scale PLA array architectures include novel reliable circuit techniques and higher-level redundancy mechanisms. Using state-of-the-art modeling and simulation platforms, we have optimized test designs, developed defect-tolerance approaches, and are continuing to develop and optimize larger systems.

15. SUBJECT TERMS
nanowire;core/shell nanowire heterostructures; nonvolatile diode switch; nanowire/ferroelectric heterostructures; nonvolatile nanowire transistor; nanofabrication; hierarchical assembly, hybrid fabrication; logic arrays, nanoPLAs; fault tolerance; ECC

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE		32	Webb Brightwell
					19b. TELEPHONE NUMBER *(Include area code)* 617-384-7673

Final Technical Report for
GRANT NUMBER FA9550-05-1-0444
1 July 2005 – 31 March 2006

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II TECHNICAL REPORT

A. Executive Summary

Effective ultra-dense integrated digital information processing strains the leading edge of current chemistry and materials science, and requires hybrid top-down and bottom-up assembly techniques, with highly reliable defect- and fault-tolerant architecture. The challenges inherent in building nanoscale electronic devices are daunting, but recent in semiconducting nanowire growth, assembly, and architectural design have begun to show that the very aggressive MoleComputing program goals can be met or exceeded with our nanowire-based approach.

We have and continue to fabricate and assemble arbitrary molecular logic elements based on overlapping semiconducting nanowire arrays using novel wafer-scale assembly techniques. Based on breakthrough addressing techniques, we can connect these logic blocks to ultra-dense memory blocks, and to external CMOS-process lithographic interfaces for testing as well as test applications. Our architecture to construct highly reliable components out of high-defect-density logic and memory, using new sublithographic scale PLA array architectures include novel reliable circuit techniques and higher-level redundancy mechanisms. Using state-of-the-art modeling and simulation platforms, we have optimized test designs, developed defect-tolerance approaches, and are continuing to develop and optimize larger systems. During the base period of the MoleComputing program we have met the Program milestones and demonstrated the great potential of our approach. A summary of results achieved directly relevant to the program milestones are as follows:

- **Demonstrated basic logic structures without feedback for 2 bit word size**
  - demonstrated 2-bit adder consisting of AND1/Inverter/AND2 stages designed and simulated
  - demonstrated 2-bit adder structures consistently fabricated by our hybrid assembly and lithography approach
  - characterized basic device element properties and statistics
  - demonstrated product of sums (POS) validating assembled 2-bit adder structures
- **Demonstrated local device pitch of ca. 100 nm**
  - demonstrated that assembly and lithography can fabricate reliably crossed arrays for logic circuits with local device pitches of $\leq$100 nm
- **Demonstrated 2 to 5 logic tiles on one die**
  - demonstrated hybrid assembly and lithography for fabrication of $\geq$2 logic tiles per standard die/chip using scalable process that is readily extended to more complex logic and computation.
- **Demonstrated novel state-of-art nanowire devices**
  - demonstrated a new core/shell germanium/silicon nanowire heterostructure transistor with device properties exceeding the best in CMOS by factor of four.
  - demonstrated a novel core/shell silicon/barium titanate structure that functions as the first nonvolatile and reversibly-switchable transistor.

Continuation of this MoleComputing effort promises to lead to unprecedented levels of processing and memory power that will enable applications of immediate national need such as extremely cheap highly-dispersed sensor-processor-memory-communications platforms, as well as longer-term high-impact examples such as massive direct digital electronic interfaces to nerves, scalable emulation engines, and applications yet to be imagined.

B. Scientific Results

A summary of the results and achievements of our effort during the first base period of the program, which address successfully the program milestones, are described below.

1. High-performance nanowire transistors. Silicon and germanium nanowires (NWs) have been the focus of much recent effort on field-effect transistors (FETs), however, metal contacts to single component nanowires generally produce Schottky barriers that limit device performance and scattering from charged dopants can also reduce the intrinsic mobility of these NW devices. In contrast, we recently demonstrated transparent contacts and low bias ballistic transport in undoped Ge/Si core/shell NW heterostructures (Figs. 1a,b), with an estimated scattering mean free path of ~500 nm. The 1D subband spacing in the typical 15 nm core Ge/Si nanowires determined through both experimental measurements and theoretical calculations is ~25 meV, and thus at room temperature several subbands may participate in NWFET transport. While the Ge/Si NW devices will not be strictly 1D, the limited number of conduction channels and clean material structure can benefit performance through, for example, a reduction in scattering. To define the potential of Ge/Si NW heterostructures as high-performance FETs we have fabricated devices using thin HfO_2 and ZrO_2 high-κ gate dielectrics and metal top gate electrodes (Figs. 1c,d). Cross-sectional transmission electron microscopy (TEM) images (Fig. 1e) show that both the high-κ and metal top gate conform to the approximately circular cross-section of the NW, and also verify the Ge/Si core/shell structure.

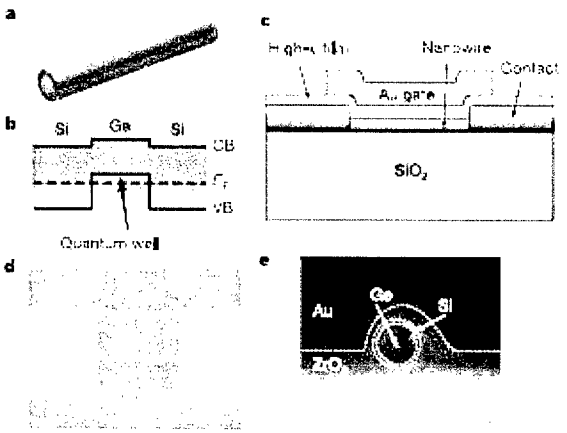


Figure. 1. a, Schematic of a Ge/Si core/shell nanowire. **b**, Cross-sectional diagram showing the formation of hole gas in the Ge quantum well confined by the epitaxial Si shell, where CB is the conduction band and VB is the valence band. The dashed line indicates the Fermi level, E_F. The valence band offset of ~500 meV between Ge and Si serves as a confinement potential to the hole gas as discussed previously[7]. **c**, Schematic of the NWFET device with high-κ dielectric layer and Au top gate. **d**, Top-view SEM image of a typical device. The Au top gate overlaps with the Ni source/drain electrodes to ensure full coverage of the channel. Scale bar, 500 nm. **e**, Cross-sectional TEM image of a device prepared using 7 nm ZrO_2 dielectric. Dotted lines are guides to the eye showing boundaries between different materials denoted in the image. The nanowire is tilted off the imaging axis. Scale bar, 10 nm.

Typical output and transfer characteristics recorded from a Ge/Si device fabricated in this way with a channel length, L = 1 μm and a total diameter of 18 nm (device A) are shown in Figs. 2b. The I_d–V_g transfer curve recorded for V_{ds} = -1 V (Fig. 2b) demonstrates that the NWFET has a peak transconductance, $g_m = dI_d/dV_g$, of 26 μS. In addition, the device exhibits a maximum drain current I_{dmax} of 35 μA at V_g = -2 V. We note these values of g_m and I_{dmax} exceed substantially the best performance reported to date in single semiconductor NWFETs. The on current I_{on} for a FET device is usually determined at V_g=V_{ds}=V_{dd}, where V_{dd} is the power supply voltage and equals 1V in our case. Following conventions in planar devices, we define on and off currents as the values measured at $V_{g(on)} = V_T - 0.7V_{dd}$ and $V_{g(off)} = V_T + 0.3V_{dd}$, so that 30% of the V_g swing above the threshold voltage V_T is applied to turn the device off, while the remaining 70% sets the operation range of the on state (Fig. 2b). Similar methods have been proposed in benchmarking carbon nanotube FET devices. From Fig. 2b, we can obtain I_{on} = 14 μA for this 1 μm long device. Significantly, the scaled values of g_m and I_{on}, 1.4 mS/μm and 0.78 mA/μm, using the total NW diameter as the device width, already exceeds the values of 0.8 mS/μm and 0.71 mA/μm recently reported in much shorter, sub-100 nm silicon p-MOSFETs employing high-κ dielectrics.

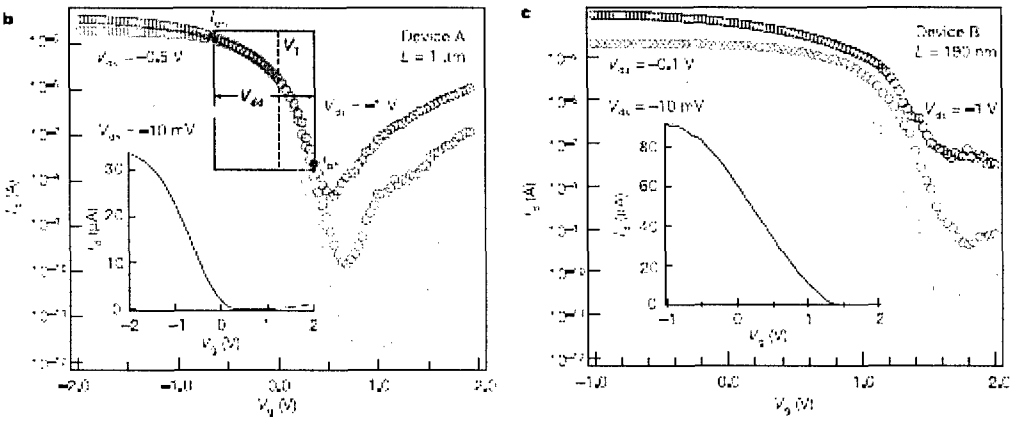


Figure 2. b, I_d–V_g for device A with blue, red, and green data points corresponding to V_{ds} values of −1, −0.5 and −0.01 V, respectively. Inset, linear scale plot of I_d versus V_g measured at V_{ds}=−1 V. The blue-shaded area defines the 1 V gate voltage window, where V_T was determined from the intercept of the tangent of maximum slope (linear transconductance) region of the I_d–V_g curve. **c**, I_d–V_g data for device B (L=190 nm, 4 nm HfO_2 dielectric) with blue, red and green data points corresponding to V_{ds} values of −1, −0.1 and −0.01 V, respectively. Inset, linear scale plot of I_d versus V_g measured at V_{ds}=−1 V.

In addition, we have prepared and studied a large number of Ge/Si NWFET devices with L varying from 1 μm to 190 nm; essentially all of these devices exhibited high performance behaviour and testify to the reproducibility of both the Ge/Si NWs and contacts to this material. Representative data obtained from a L = 190 nm device (device B), which should exhibit larger g_m and I_d values due to reduced channel resistance, are shown in Fig. 2c. These data yield g_m = 60 μS, I_{on}=37 μA (V_{dd} = 1V), and I_{dmax} = 91 μA, and correspond to scaled values of g_m and I_{on} of 3.3 mS/μm and 2.1 mA/μm, respectively. Notably, these values are more than twice that achieved in the longer channel device and are 3-4 times greater than state-of-the-art Si p-MOSFETs. Moreover, the hole mobility for this Ge/Si NWFET, 730 cm^2/V-s, extracted at the linear region (V_{ds}= 10 mV) from the peak g_m = 3 μS at $|V_g - V_T|$= 0.13 V using the charge control model, represents more than a factor of 10 improvement over that of the Si pMOSFET with HfO_2 gate dielectric (50~60 cm^2/V-s), and also is more than twice the reported low-field mobility of Ge and strained SiGe heterostructure PMOS devices. These

improvements over planar device structures thus verify the performance benefit due to the quasi-1D transport in clean Ge/Si heterostructure NWs.

An important benchmark of transistor performance is the intrinsic delay, $\tau = CV/I$, where C is the gate capacitance, $V = V_{dd}$, and I is on current I_{on}. As defined, τ represents the fundamental RC delay of the device and provides a frequency limit for transistor operation that is relatively insensitive to gate dielectrics and device width, and thus represents a good parameter for comparing different types of devices. The calculated intrinsic delays are 57 and 4 ps for devices A and B in Fig. 2, respectively, where C was determined by numerical simulation (Methods). A summary of the results from 7 Ge/Si NWFETs versus L and the corresponding scaling for Si MOSFETs (Fig. 3a) highlights several key points. First, the data show clear speed advantage at a given L for the Ge/Si NWFETs versus Si p-MOSFETs. For example, the intrinsic delay for 190 nm Si planar device is larger than 10 ps, about three times longer than our device B. Second, the delay time for the 190 nm Ge/Si device is about the same as that of similar length CNTFET devices. Last, length scaling of τ is more favourable for our Ge/Si NWFETs than Si MOSFETs (i.e., slope of ~1.5 vs. ~1.1). We attribute this important difference to a suppression of scattering in the quasi-1D quantum confined Ge/Si NWs versus MOSFETs, although additional studies will be needed to support this idea.

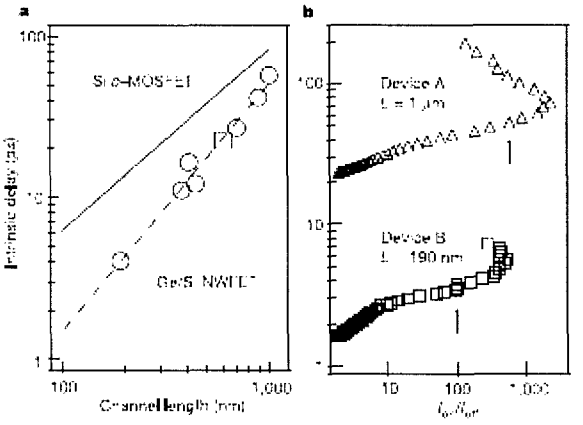


Figure 3. a, Intrinsic delay τ versus channel length for seven different Ge/Si nanowire devices with HfO_2 dielectric (open circle) and ZrO_2 dielectrics (open square). The dashed line is a fit to the data points while solid line is the Intel Si p-MOSFET results. **b**, Intrinsic delay versus on/off ratio for the two devices in Fig. 2 Arrows indicate the values of intrinsic delay used in **a**.

In summary, we have demonstrated top-gated Ge/Si NWFET heterostructures with high-κ dielectrics that exhibit scaled transconductance and on-current values of 3.3 mS/μm and 2.1 mA/μm, respectively, which are three to four times greater than those for state-of-the-art MOSFETs. In addition, the Ge/Si NWFET hole mobility, 730 cm^2/V-s, is more than a factor of 10 greater than Si pMOSFET with HfO_2 gate dielectric and more than twice that of Ge and strained SiGe heterostructure PMOS devices. These values together with the demonstrated control over threshold voltage and ambipolar behaviour suggest substantial promise of Ge/Si NWFETs.

2. Design and implementation of nanowire nonvolatile diode switches. Through synthesis of core-shell engineered inorganic nanowires, we have developed a unique way of building crossbar switches by utilizing the doped NW core as one electrode contact and treating the shell which can be controlled synthetically as the storage medium. Here the electrode and the storage medium, can be seamlessly integrated in a core-shell manner, thus ensuring reliable device behaviour. As shown in Figure 4a, the crossbar structure is formed by crossing a lithographically defined metal line with a heterostructure NW, which consists of a heavily doped p-type crystalline silicon (c-Si) core and an amorphous silicon (a-Si) shell. Figure 1a inset shows one typical such device with metal line width of around 150 nm. The

core-shell nanowires used in this structure were synthesized by chemical vapor deposition. High resolution transmission electron microscopy (HRTEM) image of the as-grown nanowire (Fig. 1b) shows the existence of ca. 5 nm uniform amorphous silicon shell outside the c-Si core and confirms the seamless a-Si/c-Si interface. Device fabrication was then carried out at room temperature by assembling these nanowires onto different substrates with our solution based strategy, and then defining different metal contacts to the c-Si core and the a-Si shell in a stepwise manner.

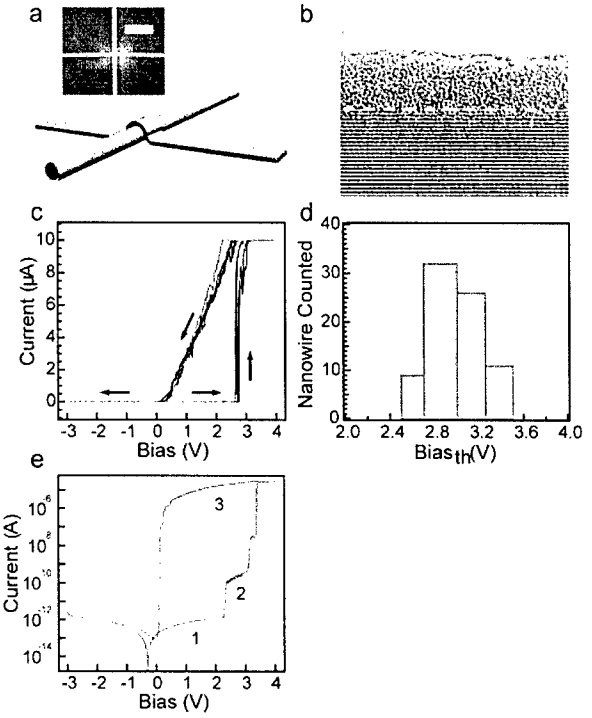


Figure 4. a, A single memory bit is formed at the crosspoint of a metal line (gray) and a c-Si (blue) /a-Si (cyan) core-shell nanowire. Inset, Scanning electron micrograph (SEM) image of a typical crossbar device. Scale bar is 1 μm. **b**, HRTEM image of a c-Si/a-Si core/shell nanowire. Dashed line indicates the interface between the c-Si and a-Si. Scale bar is 5 nm. **c**, DC I-V curves. The arrows indicate the voltage-scanning direction. The initial cycle is in red and subsequent cycles are in black. **d**, Histogram of the threshold voltage distribution from over 80 NW crossbar switch devices showing high reproducibility and a tight distribution. **e**, A typical switching cycle in log scale showing experimental data (Red) and corresponding fitting with the tunnelling model. The numbers indicate different steps during OFF to ON switching.

The behaviour of a single memory bit showed that when the voltage is increased from 0 to 4 V, the current abruptly increases at ~3 V and switches the Ag/a-Si/c-Si junction to the low resistance ON state (denoted as '1'), Fig. 4c. Subsequent sweeping of the voltage back to a negative value (-3 V in this case) switches the device back to the high resistance OFF state (denoted as '0'). The I-V curve between two Ni contacts shows linear behaviour, demonstrating good Ni/c-Si ohmic contact and that the switching can only be attributed to the Ag/a-Si/c-Si junction. Detailed studies on the switching behaviour show several interesting features. First, our devices show intrinsic rectification, that is, the devices show low conductance when negative bias is applied (Fig. 4c). This rectification simplifies high density array design since it eliminates cross talk between memory bits. Secondly, the switching is highly repeatable, as evidenced by tests on over 80 devices (Fig. 4d), which show a narrow threshold voltage distribution (mean of 3V and a standard deviation of 0.5 V). Thirdly, data recorded on a log scale (Fig. 4e) shows that the ON/OFF ratio is higher than 10^6.

To address the origin of these switching features, especially the unique rectification behaviour, we carried out scaling, temperature dependent and metal dependent studies on devices. First, the intrinsic junction resistance variation was characterized when the metal line width was scaled from 1 μm to 30 nm (Fig. 5a), and these results demonstrated the ON state resistances is approximately independent of width. This result suggests that a local nanoscale filament conduction accounts for the ON state. In addition, temperature dependent switching results clearly show that the rectification is strongly temperature related (Fig. 5d). At 250 K

or above devices exhibit rectification, but at 200 K or lower devices lose the rectification characteristic. This observation can be understood within a tunneling model, where the switch conductance depends strongly on whether the last few traps closest to c-Si NW core are filled with metal ions or not. Thus the energy barrier height ϕ and the mobility of the metal ion in these traps will play a central role on the conductance. Since hopping of the metal ions is a thermally activated process, at room temperature or higher, the trap energy barrier is low and the metal ion mobility is high, and the ions have a non-negligible probability to hop back, away from c-Si, as illustrated in Figure 5e. As a result, the traps closest to c-Si can be thermally emptied, turning the device into the high resistance state. At low temperatures, the ions have a higher probability of staying in the traps (Fig. 5f), and can only be emptied at higher negative biases.

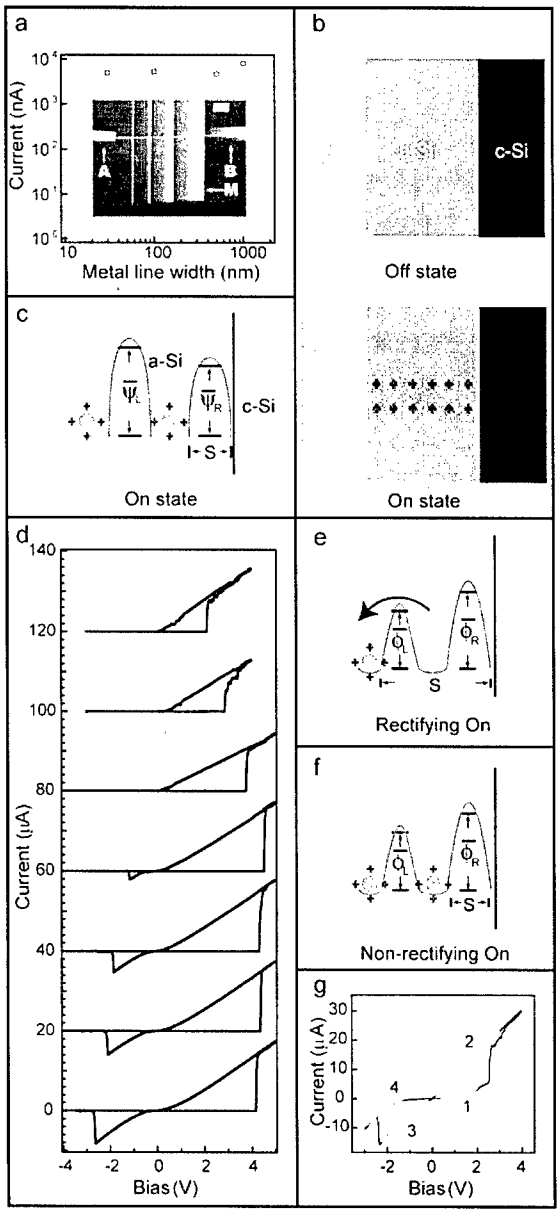


Fig. 5. a, metal line width scaling measured with three terminal setup[22]. ON state resistances for devices fabricated with different metal line widths (30 nm, 200 nm, 500 nm and 1 μm) on one single core/shell nanowire. Inset, SEM image of the devices. Scale bar is 1 μm. **b**, Schematic diagram of the OFF (up) and ON (bottom) states of metal ion filament conduction in a-Si matrix. **c**, Energy diagram for deriving I-V equation. s indicates the distance between the last metal island and the c-Si core. Ψ indicates barrier height for electron tunneling. L and R represent left and right respectively. **d**, I-V curves obtained on one switching device at different temperatures. The curves are offset vertically for clarity. The temperatures from top to bottom are 350, 300, 250, 200, 150, 100 and 50 K respectively. **e**, Energy diagram for rectifying ON state and **f**, non-rectifying ON state. ϕ indicates barrier height for metal ion hopping. The arrow shows ion hopping direction. **g**, I-V curve (black) obtained on Au/Cr/a-Si/c-Si switches at room temperature. The green curves show results from the tunneling model. The numbers indicate different stages during switching.

Important parameters of our metal/a-Si/c-Si nonvolatile switches, including cycling stability, switching speed and data retention time, have been characterized (Fig. 6). For

endurance cycles test, the device was repeatedly written, read and erased. First, devices can be reliably switched ON/OFF for at least 10^4 cycles without obvious change (Fig. 6a). Second switching speed tests (Fig. 6b) showed that devices can be switched on microsecond time-scale with write pulses of of 4 V, and significantly, can be switched on 100 ns time scale using larger 6.5 V write pulses, where in this latter case the time scale limited by our experimental set-up. Third, studies of the retention time (Fig. 6c) show that after 2 weeks, the readout current for ON state decays less than 20%, while the OFF state current shows almost no change, confirming the nonvolatile nature of the memory effect.

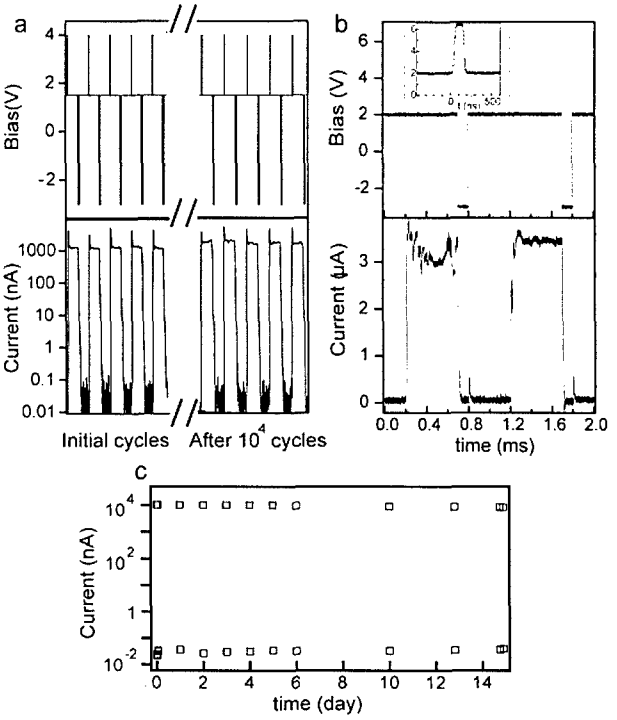


Fig. 6. **a**, Write-Read-Erase-Read cycles. The top curve shows the applied bias sequence and the bottom curve shows corresponding current response. The measured OFF state current is limited by the dynamic range of the current amplifier used. **b**, Switching speed test (analogous to **a**). Inset, zoom in of the 100 ns write pulse. **c**, Retention time test results for both ON and OFF states after writing or erasing the switch at 4 V and – 3 V respectively. Current is read at 2 V.

We have also studied scalability of the a-Si crossbar switches in one dimensional (1D) and two dimensional (2D) arrays. Dense 1D memory array were fabricated by crossing one nanowire with several (n) metal lines (denoted as 1 X n). Figure 7a shows one 1 X 6 array with metal line width of 30 nm and 150 nm spacing. We can write or erase the six memory bits (crosspoints) to arbitrary combination (e.g. 000000, 111111, 101010, 010101 (Fig. 7b) and then read out the information by sequentially scanning every point at small bias. The results show that every crosspoint can be individually addressed without crosstalk during writing, reading or erasing. A memory based on this current device structure can in principle have a storage capacity already over (4.4 Gbit/cm^2 or 28 Gbit/inch^2). Two dimensional memory arrays were also demonstrated. In a 2 X 2 array, all combinations (e.g. 1111, 1010, 0101) can be written into the array and read out without crosstalk (Figs. 7c,d). The success of these arrays arises from the intrinsic rectification property of our designed devices. In summary, we have demonstrated a simple approach towards fast, reliable and flexible crossbar non-volatile memories with uniform switching, high ON/OFF ratio, long retention time and intrinsic rectification.

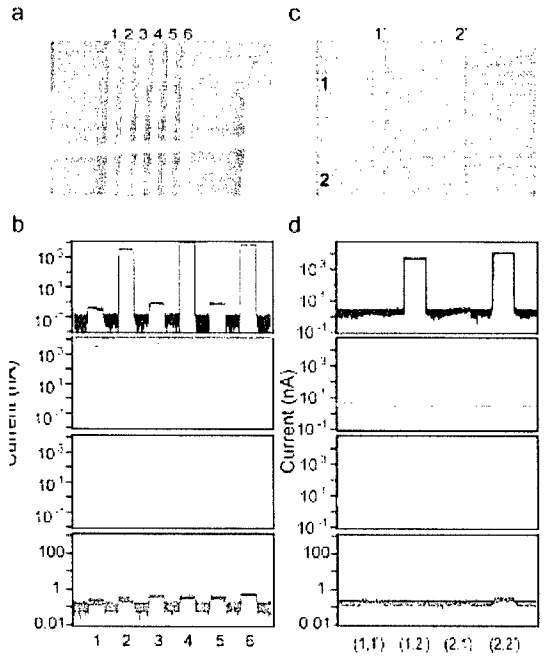


Fig. 7. **a**, SEM image of one nanowire crossing six metal lines (1X6) array. Metal line width: 30 nm, pitch: 150 nm, Scale bar is 500 nm. **b**, The states of the cross point 1-6 of the memory array are read out by a 2 V bias after writing or erasing them to arbitrary combination with a 4 V pulse or a -3 V pulse respectively. (Blue: 010101, Green: 101010, Yellow: 111111, Red: 000000). **c**, SEM image of a two nanowires/two metal lines (2X2) array. Scale bar is 1μm. **d**, The four bits are individually written or erased to arbitrary combination (Blue: 0101, Green: 1010, Yellow: 1111, Red: 0000) and then sequentially read out.

3. Nanowire nonvolatile diode and transistor element arrays for logic. The nonvolatile diode devices are a key component together with nanowire FETs for our 2-bit adder design, which is illustrated in Fig. 8.

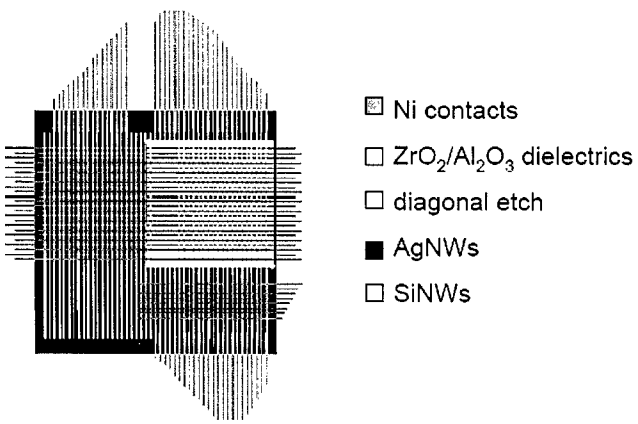


Fig. 8. Schematic illustrating structure and key materials for nanowire-based 2-bit adder.

The 2-bit adder was designed to exploit hybrid fabrication approach combining high-density assembly of the functional nanowires together with lithography to define metal nanowires and interconnects. The first step in the process involves nanowire assembly by Langmuir-Blodgett (LB) technique, which enables control of orientation and density of the nanowires, followed by several lithography/deposition steps as indicated by the distinct materials in Fig. 8.

Significantly, we have successfully implemented this multi-step approach on a wafer scale level to enable definition of 2-bit adder structures as tiles across the wafer as shown in Fig. 9. We designed lithography masks to enable fabrication of 3x3 die pattern on standard 75mm silicon wafer, where in each die region there are 20 2-bit adder structures.

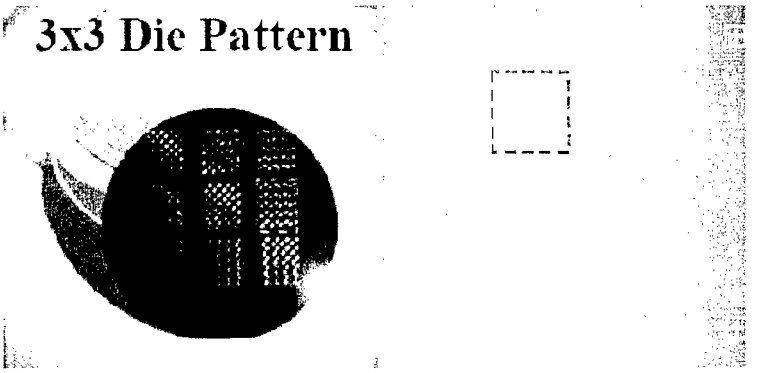


Fig. 9. (left) 3x3 die pattern of adder structures fabricated on a 3-inch wafer. (right) a zoom image of one of the illustrating 20-independent 2-bit adder structures.

The basic fabrication involves initial assembly of nanowires by the LB technique on wafer on die-sized chips, followed by photolithographic patterning of the larger scale metal interconnect visible clearly in Fig. 9. Subsequently, we have exploited high-resolution electron beam lithography to define metal lines and interconnects to the nanowires at 100 nm or higher resolution needed to meet the program milestones as shown in Fig. 10. These results demonstrate clearly that (i) functional nanowires can be assembled at sub-100nm spacing required for program goals, (ii) that multiple functionalities – 2 AND stages and 1-FET inversion stage – can be integrated using our hybrid approach, and (iii) that this can be carried out for multiple tiles with consistent output for testing.

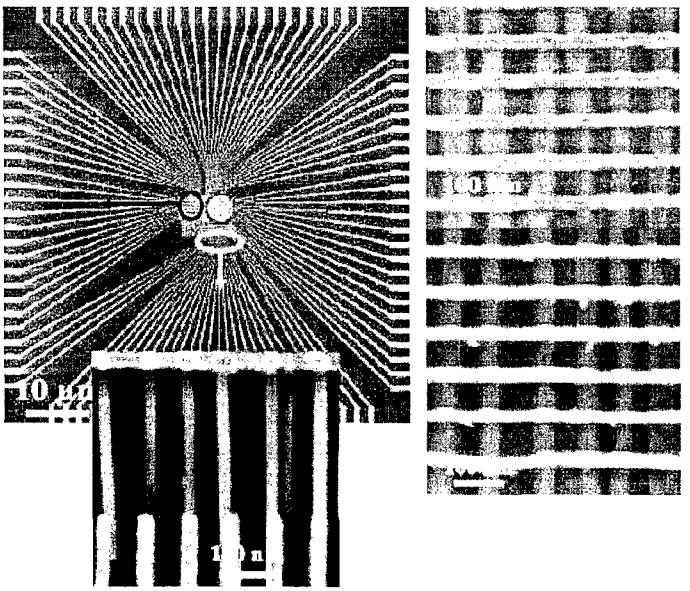


Fig. 10. Scanning electron microscopy images of the interconnect and device regions of the 2-bit adder structure. Upper left shows lines from photolithography defined features (periphery of image) to the dense nanowire device region at the center. The right and lower left images show crossed nanowire device in the FET inversion stage and interconnects to the nanowires in AND2 stage of the adder.

In parallel with our demonstration of fabrication of the 2-bit adder structure, we have fabricated and verified the electrical properties of each of the key circuit components required for successful adder function. First, we have demonstrated that using a single core/shell nanowire developed for the critical nonvolatile diode switches that it is also possible to simultaneous introduce FET function by local deposition of a high-k dielectric at the desired positions for FET device cross-points (Fig. 11). Electrical transport measurements demonstrate that in single nanowires with two distinct cross-points exhibit both functions, and significantly, these functions can be combined to yield inverter behavior as required.

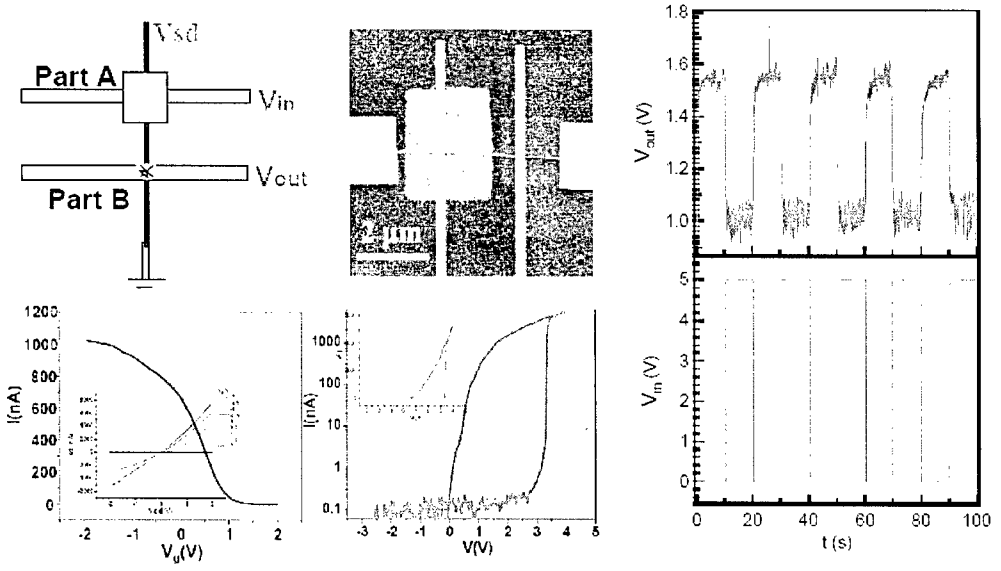
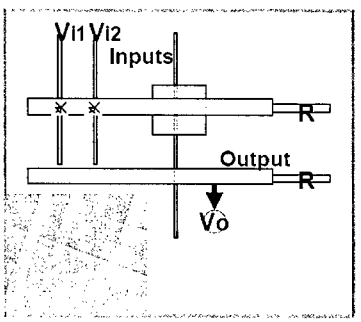


Fig. 11. Combined FET (part A) and nonvolatile diode (part B) integrated on single function nanowire unit. Lower left illustrates electrical device data demonstrating FET (left) and nonvolatile diode (right) functions. Right demonstrates inverter function from combined two-device circuit.

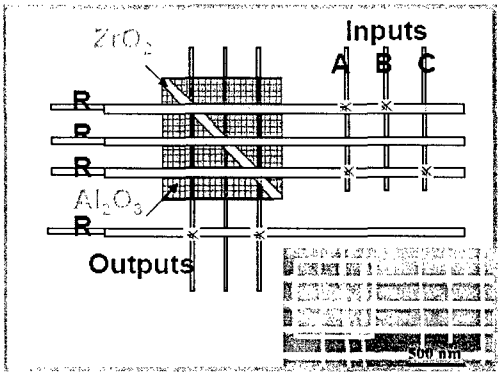
The basic 1-FET/1-diode structure was then further elaborated to two separate diode stages, which is required to demonstrate AND logic and inversion using the basic structure illustrated in Fig. 12. This structure incorporates 4-independent cross-point junctions, where two nonvolatile diode junctions on NW1 & NW2 make up the AND1 stage, the FET on NW3 enables inversion, and the diode on NW3 serves as output. Significantly, transport measurements demsontrate that this substantially more complex circuit behave as required.



V_{i1} (V)	V_{i2} (V)	V_o (V)
0.0(0)	0.0(0)	1.73(1)
2.0(1)	0.0(0)	1.54(1)
0.0(0)	2.0(1)	1.46(1)
2.0(1)	2.0(1)	0.75(0)

Fig. 12. Schematic, device and input/output table for AND-INV circuit comprising four independent cross-points (3-diode; 1-FET).

Last, we have increased circuit complexity one further level to include all basic functions required for the 2-bit adder and demonstrated critical product of sums function as shown in Fig. 13. These results represent key proof-of-concept for our approach and meet basic milestones of program.

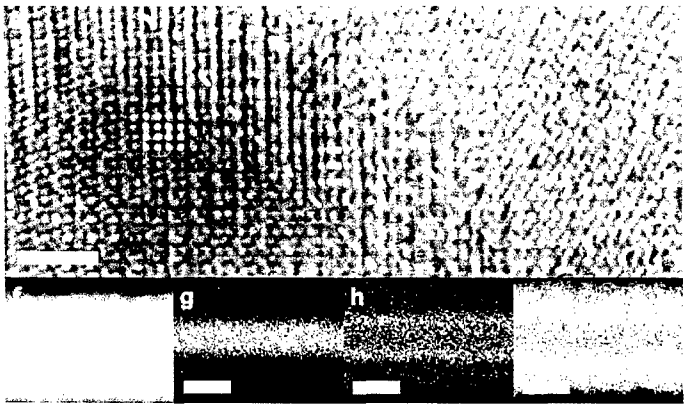


A	B	C	(A+B)·(A+C) =(A+B)·(A+C)
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Fig. 13. Basic elements required for adder design, and used to demonstrate key function as product of sums (POS).

4. Ferroelectric nanowire elements and arrays for memory and logic. Functional oxide nanostructures can introduce unique properties but have thus far received much less consideration for integration into nanoscale semiconductor devicesTo explore exciting opportunities with such materials, we have developed and implemented a rational strategy of coupling functional oxides with semiconductor nanostructures with precise control down to atomic level. We have used atomic layer deposition to integrate barium titanate, a ferroelectric oxide, onto our well-studied semiconductor silicon nanowires. Specifically, we synthesized silicon (Si) - zirconium oxide (ZrO_2) – barium titanate (BaTiO3) semiconductor-dielectric oxide-ferroelectric oxide core-shell-shell nanowire heterostructures as shown in Fig. 14. Transmission electron microscopy (TEM) studies show clearly the core-shell structure, energy dispersive X-ray spectroscopy confirms the elemental spatial distribution, showing that Si is localized at the core, Zr at the inner shell, and Ba and Ti at the outer shell.

Fig. 14. d-f, h, HRTEM image of the $BaTiO_3$ (left), ZrO_2 (middle) and Si (right) regions. Insets, crystal structures simulations of the $BaTiO_3$ (pink), ZrO_2 (green) and Si (blue). The scale bar is 2 nm. E\lemental mapping images showing that Si is localized at the core (g), Zr at the inner shell (h), and Ba and Ti at the outer shell (i). The scale bars are 50 nm.



To demonstrate unique electrical properties of these new structures, we prepared field-effect transistor (FET) devices (Fig. 15). Transport data show that the current (I_{ds}) versus source–drain voltage (V_{ds}) data (Fig. 15a) at different gate voltages (V_{gs}) exhibit the behaviour expected of a depletion mode p-FET. Further measurements of source-drain conductance versus gate voltage show a hysteresis loop in the gate sweep (Fig. 15b). In the hysteresis loop, two bi-stable states have been observed around 0 V gate voltages: one higher conductive "on" state and one at lower conductive "off" state. Switching from "on" to "off" occurs at ca. +5 V, whereas the reverse process occurs at ca. -3 V.

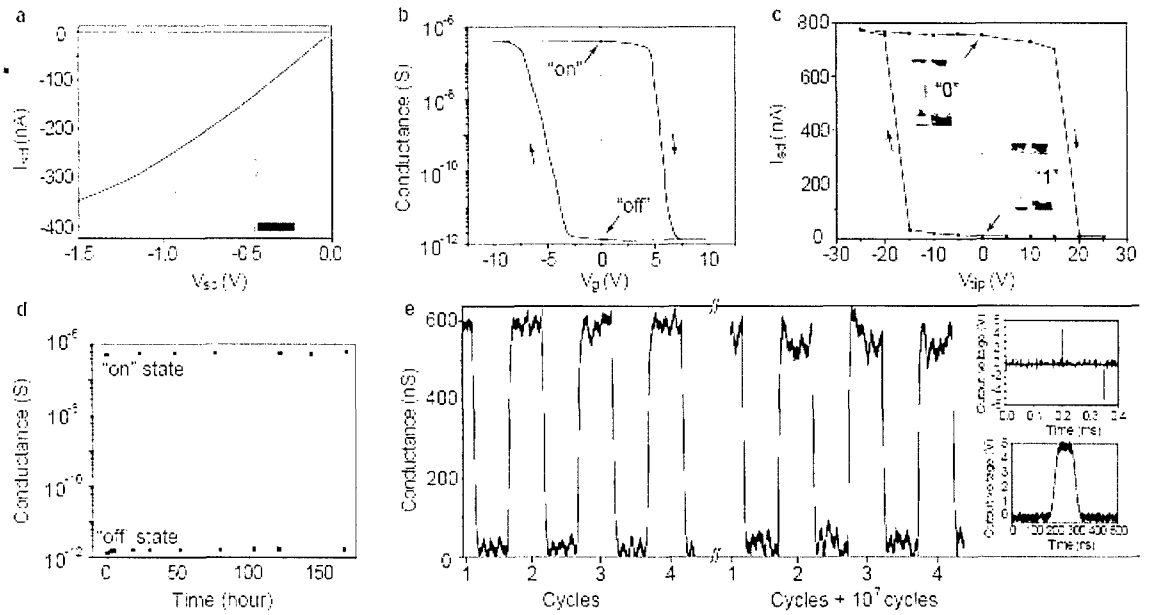


Fig. 15. a, Current vs. source-drain voltage. Inset, SEM image showing the device. The scale bar is 2 μm. **b,** Gate sweep obtained from the same device at a bias voltage of -1.5 V. **c**, EFM measurement performed on a FET device without top gate showing that a ferroelectric polarization has been generated on the $BaTiO_3$ shell by gate voltage applied on the conductive AFM tip. The scale bars are 2 μm. **d**, Conductance change of a FET device over weeks showing no obvious degradation of the "on" state conductance (upper spots). Similarly, the device turned "off" by the ferroelectric polarization generated by positive gate voltage shows no obvious increase in conductance over weeks (lower spots) even after the removal of the external gate voltage. **e**, The device can be switched "on" and "off" continuously for one hour with fixed -1 V source-drain bias without obvious fatigue, showing the endurance can be at least 10^7 cycles

Electrostatic force microscopy (EFM) confirmed that the origin of the hysteresis loop is polarization switching in ferroelectric $BaTiO_3$ (Fig. 15c). In addition, the core-shell nanowire heterostructure FET, once turned "off" by the ferroelectric polarization generated by positive gate voltage, retains the "off" state for weeks without obvious degradation even after the removal of the external positive gate voltage (Fig. 15d), clearly demonstrating device non-volatility. We have also characterized the switching speed and endurance of the core-shell nanowire heterostructure FET device (Fig. 2e). For example, the nanowire heterostructure can be switched with pulses of 100 ns (insets, Fig. 15e). Faster switching speeds of 50 ns have also been seen, but this is near the limit of our instrument. This switching behaviour is maintained without obvious fatigue degradation for at least 10^7 cycles of writing and erasing (Fig. 15e).

Significantly, we have fabricated multiple gates crossing one FET devices (Fig. 16a) to store multiple bits of information per transistor, which expands on the conventional configuration in which only one bit can be stored per transistor. Our results show that one can randomly write different combinations of polarization using a positive gate voltage applied on the metal gate; for example, applying +8V on all three gates on the FET (Fig. 16a) will write polarizations in the separate BaTiO3 domains beneath the gates, which will turn off the device and allow for multiple bits of information ("111") to be stored (Fig. 16b, black line, write ABC). To read the information, a small negative gate voltage (usually -1 V), which is large enough to screen part of the electric field caused by the ferroelectric polarization and increase the conductance but small enough not to reverse the ferroelectric polarization direction, is applied to all three gates.

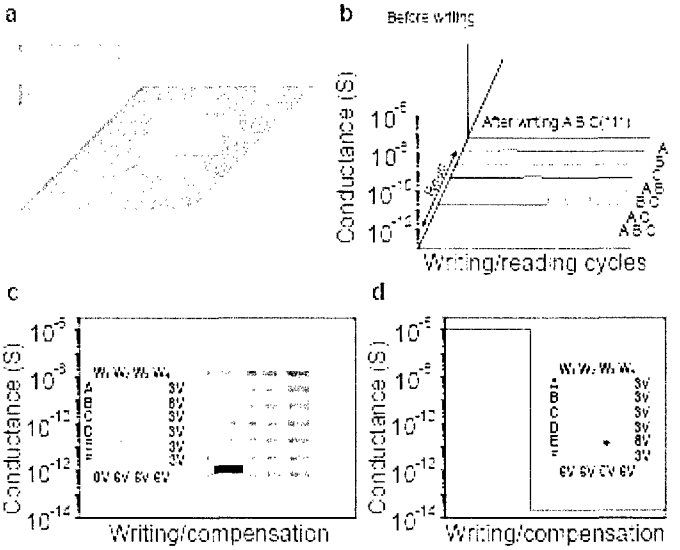


Fig. 16. One (a,b) and two (c,d) -dimensional arrays of nanowire/ ferroelectric core/shell nonvolatile transistors.

Lastly, we have addressed the issue of integration of these core-shell nanowire heterostructures into large scale memory arrays and NOR logic device arrays by fabricating multiple gates crossing multiple well-aligned nanowires (Fig. 16c,d). For example, in a prototype memory array (right inset, Fig. 16c) composed of 4 nanowires (W_1, W_2, W_3, W_4) crossing six gates (A, B, C, D, E, F) (left inset, Fig. 16c), applying +8 V gate voltage on gate B and ground on nanowire W_1 can efficiently write a polarization at the cross point between nanowire W_1 and gate B, which will turn "off" the nanowire W_1 FET device. However, +6 V on nanowires W_2, W_3, W_4 and +3 V on gates A, C, D, E, F must be applied to avoid writing extra polarization at the cross points among gate B and nanowires W_2, W_3, W_4. The -3 V potential difference between the gates A, C, D, E, F (+3 V) and nanowires W_2, W_3, W_4 (+6 V) will not wipe the possible existence of polarizations at cross points among them. A similar strategy was also adopted during the following writing of the cross point between nanowire W_3 and gate E (red point in the inset, Fig. 16d). After the writing, nanowire W_3 FET device is turned "off" (red line, Fig. 16d) while no disturbance has been observed on the nanowire W_1 FET device (green line, Fig. 16d). These results show that such strategy of applying writing and compensation voltage is efficient and will enable us to individually address all the cross points in the array.

5. Thermal transport and dissipation in nanowire elements. Energy dissipation and thermal transport are very important issues for nanoscale device applications. One of the fundamental properties that are also important for the device operation is how electrons transport is related with the thermal transport in nanoiwres. We have characterized thermoelectric transport phenomena in Si nanowires (SiNW) using novel mesoscopic thermoelectric measurement scheme. Fig. 18 shows a typical microfabricated SiNW hybrid device for simultaneous conductance (G) and thermopower (TEP) at different temperatures as a function of gate voltage (V_g). Cross correlation study between electrical conductance and thermoelectric power in the SiNW shed light on the transport mechanism in the wire. Specifically, these studies reveal the dopant density in SiNWs directly and allows to estimate the upper bound of Schottky barriers between electrodes and SiNWs. Expending these successes, we are now investigating the nature of energy dissipation in SiNW, employing TEP as an additional experimental method to explore the interplay between electrical and

thermal transport phenomena. Understanding such interaction will be critical in designing minimal energy dissipative devices based on SiNWs.

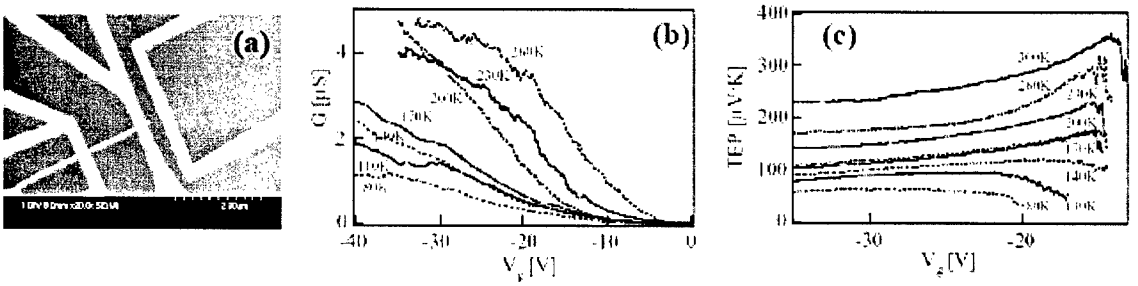


Fig. 17. (a) Scanning electron microscope (SEM) image of a device for mesoscopic TEP measurements on isolated silicon nanowire. (b) Conductance of silicon nanowire at different gate voltages and temperatures. (c) The corresponding TEP of the nanotube device in (b).

6. Shift-register design and test. The basic nanoPLA cycle supports clocked logic, and hence registers, using the pre-charge clocking scheme [2]. Simply cascading buffered logic in this style gives us shift registers. We can build loadable shift registers by designing multiplexer logic and feedback along with the clocked buffers. Using these registers, we can build Linear Feedback Shift Registers (LFSR) to evaluate reliable operation over long time periods at high clock frequencies. The basic nanoPLA cycle is shown in Figure 18. Focusing initially on the top-left wired-OR plane. Here, the vertical (red) wires are inputs with the horizontal (green) wires being outputs. This will charge up the top row of horizontal wires to the programmed set of ORs of the identified inputs. Assume we start with the restoration columns to the right (vertical, red wires) disabled using the /evalA and /prechargeA controls. Now, once the row wires have settled to their appropriate value, we use the /evalB and /prechargeB controls to isolate this wired-OR stage. The output values will stay precharged at their resolved logic values. We then use /prechargeA and prechargeA (further to the right) to discharge both the restoration columns (red, vertical nanowire groups on right) and the following OR outputs (bottom row of horizontal, green wires). Once these have been charged low, we release the precharge and enable evaluation of the restoration using /evalA. This allows the stored logic values on the top set of OR terms to gate the restoration columns (top-right restoration plane). The restoration wires which see a low input across their lightly-doped control region will allow conduction and be pulled high, while those with high inputs will remain in their low precharged state. The high-driven lines will couple through the OR plane (lower-right OR plane) and pull up the appropriate wired-OR wires in the lower row. Once this evaluation is completed, we can turn off the /evalA control, thus isolating this stage just as we initially isolated the previous stage. Holding /prechargeA and /evalA into the disconnected state, we can evaluate the following stage using /prechargeB and /evalB in a similar manner. The result is a two-phase logic evaluation similar to two-phase clocked logic in CMOS.

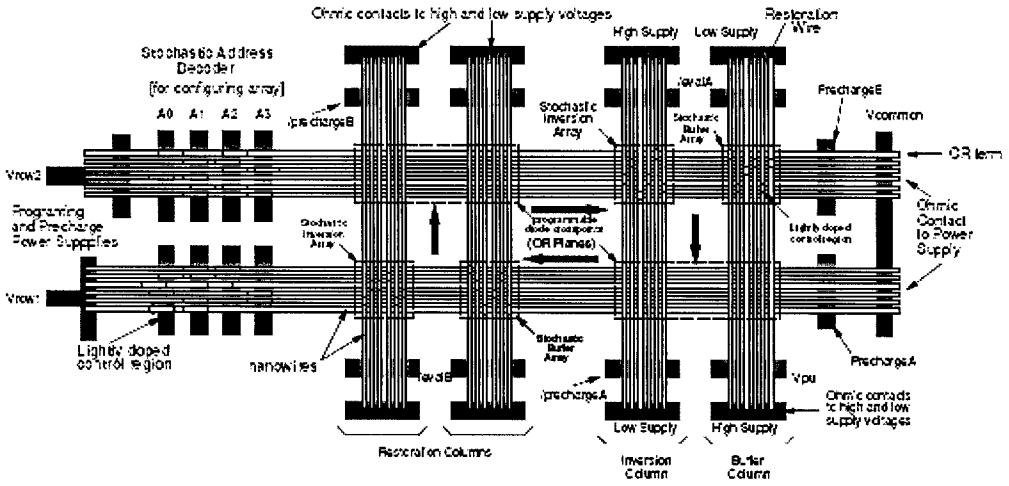
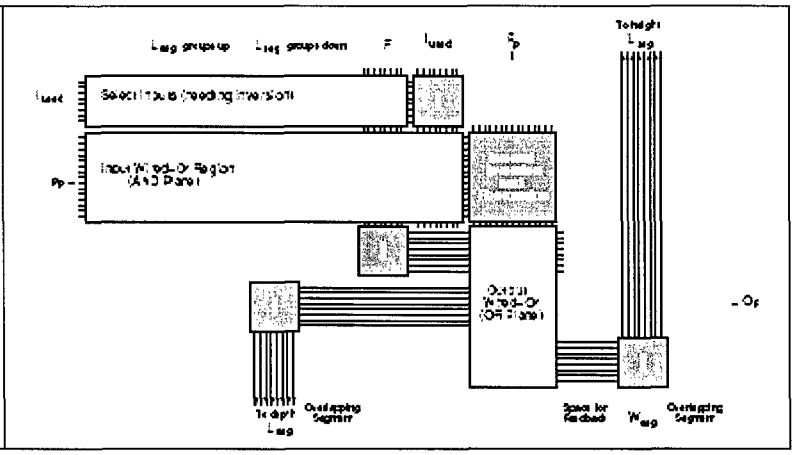


Fig. 18. The basic nanoPLA architecture.

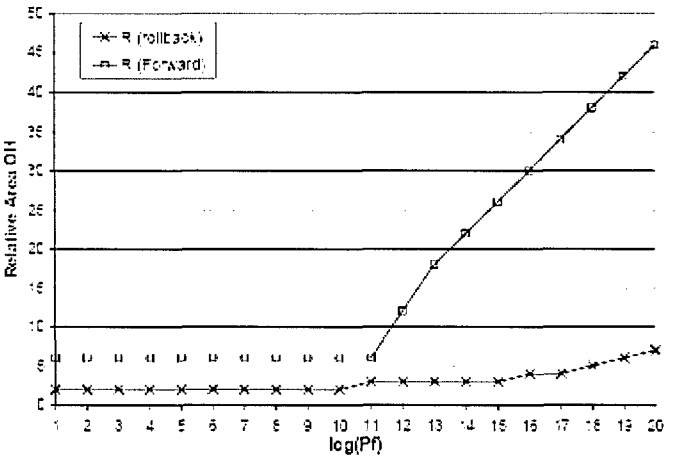
7. Inversion schemes. The pre-charge logic scheme reviewed above works as long as all the signals are inverted in the restoration stage. Unfortunately, typical PLA logic requires both polarities of each signal, not just the inverted sense. The original scheme built the non-inverting buffer in the same way, but relied on ratioed logic for the non-inverted signal. Unfortunately, this dissipates static power and significantly slows evaluation. We previously noted that we could compute both the true and complement sense of all signals (*i.e.* compute the logic "dual rail") as a way to get around this. However, we had not previously evaluated the cost of such a scheme. A third solution is to modify the nanoPLA topology so that we can pass signals which we want in the non-inverted sense through an extra inversion stage in order to get back to the true logic sense. Figure 19 shows a suitably modified topology for this local-inversion scheme. Evaluation now occurs in three phases rather than two. In the third phase, we locally invert inputs that arrive at a nanoPLA block in the wrong phase. Note that the original inputs are also available, so the nanoPLA block has both phases available for use by its PTERMs. To fully understand these cases, we developed mapping tools to map the dual-rail logic and area models for the three schemes. We mapped the Toronto 20 benchmarks for all designs and compared their final areas. The dual-rail scheme required twice the area of the original scheme, while the local-inversion scheme required only 77% of the area. This suggests the local-inversion scheme is a good alternative that allows us to save additional area while avoiding the static power dissipation and slow evaluation of the original, ratioed-logic buffering scheme. This study is documented in a recent paper (currently under review). A preprint is included with this report.

Fig. 19. Local-inversion nanoPLA block. The nanoPLA topology passes signals in the non-inverted sense through an extra inversion stage in order to get back to the true logic sense.



8. NanoPLA fault tolerance. Individual nanowires switch with roughly 1000 electrons. With state represented by such small charges, nanowire state can easily be disrupted by ionizing particles or thermal fluctuation. Further, when working with such small charges, it is statistically possible that logic transitions may not occur. Consequently, in addition to fabrication defects, we must ultimately guard against dynamic logic upsets during operation. Von Neumann introduced schemes to cope with unreliable logic roughly 50 years ago; while little practical work has derived from Von Neumann's scheme, much theoretical work has built upon it establishing the achievable asymptotes. Von Neumann's scheme is basically to replicate and vote computations at the gate level (*e.g.* like Triple Modular Redundancy (TMR) conventionally used at the processor level in ultra-high reliability scenarios, Von Neumann replicates gate-level computation and uses majority gates to vote for the correct answer). More recent efforts concentrating on faulty nanotechnology have explored versions of Von Neumann's feed-forward scheme. Unfortunately, the feed-forward schemes have very high overhead, requiring large replication factors. As an alternative, we are exploring rollback schemes. In these rollback schemes, we simply need to detect that an error has occurred and signal the event. The logic can then be recomputed until it produced a correct answer. As a result, rollback schemes require significantly lower redundancy than feed-forward schemes. As a simple example, we can detect a single error with only one copy of the logic (duplication), whereas feed-forward correction requires at least three copies of the logic to produce the correct result when one gate is in error. The gap widens as the fault rate and system size increases, demanding that we operate correctly in the presence of even more errors. Fig. 20 compares the redundancy required in a gate-level feed-forward scheme based on to a replication-based detection and rollback scheme. We see here that detection can= significantly lower the redundancy required for reliable operation. To complete the rollback scheme, we must also be able to store intermediate data reliably so we can recompute with it when errors are detected. This demands area for buffers to store the data; we use buffers based on the shift register designs described above. Further, the data stored in those buffers must actually be protected in a feed-forward manner. Together, this could mean a large area cost in addition to the replicated logic. As a result, the net area benefit may be less than the redundancy factors shown in Fig. 20. This leads us to ongoing work to develop area efficient buffers and buffer correction so we can keep the area-overhead required for the rollback scheme close to the redundancy factor shown in Fig. 20. Initial designs do require less net area than the feed-forward schemes, and we anticipate we can increase the savings further with more highly optimized designs.

Fig. 20. The replication factor of rollback and forward recovery. The system reliability goal is 90%.



9. Error-correcting codes (ECCs) in nanoscale memory. Current-day micro-scale devices (e.g., gates, PLAs, memories, etc.) constructed using top-down lithographic techniques yield error rates less than 1%. But with feature sizes being scaled down to the nano-scale, future computing and storage components created from nano-scale elements (e.g., bistable and switchable organic molecules, carbon nanotubes, and single-crystal semiconductor nanowires) using bottom-up synthesis techniques will have orders of magnitude higher rates of faults (up to 10-15%). So, error-correcting codes (ECC), which are already used to ensure reliable computation in micro-scale devices, especially embedded memory devices, will become much more relevant in nanoscale computing, and hybrid computing that uses both nano and micro components. In this project, we have initially focused on error-correcting codes for nanoscale memory, built from nano-scale PLA and gate elements.

In microscale memory with ECC capabilities, different codes, e.g., Hamming codes, Hsiao codes, etc. have been used. The encoders/decoders for these codes are simple to implement in hardware and have low encoding/decoding complexity. However, they have relatively low error-correcting capacity (e.g., Hamming is single error-correcting, double error-detecting). In order to have higher error correcting capability, one has to use better codes like Reed-Solomon codes. These codes, however require more sophisticated decoding algorithms, which would need either (1) complex algebraic decoders that can decode in fixed-time, or (2) simpler graphical decoders, that use iterative algorithms (e.g., belief propagation) and hence need more computation time.

Implementing these decoders in nanoscale may be difficult for a couple of reasons. First, designing complex encoder/decoder hardware using nanoscale components would incur significant overhead if the encoder/decoder has to be made totally self-checking (which may be necessary if the encoder/decoder hardware components themselves are synthesized from faulty nano-components), since then the corresponding parity-predicting hardware in the self-checker could be quite complex. Second, Since ECC would need to be used in many core components for nanoscale computing applications (e.g., ALU, memory, etc.), iterative encoders/decoders (which are generally easier to implement in hardware) may not be fast enough for at-speed error-correcting operations. To solve these problems, one should use nanoscale error correcting codes that have: (1) high error correcting/decoding capacity, (2) relatively simple encoding/decoding circuits so that the operations can be performed fast, (3)

variable error-correcting capability, to give optimal ECC-power tradeoff along the bath-tub curve: as the lifetime of the part increases, the faults decrease during the normal operation of the circuit as compared to the infant mortality rate, and later increases again as the part ages. One would typically want the ECC circuit for the nano-memory to have higher error correcting capacity during the initial and final stages, but disable unused parts of the ECC encoder/decoder circuit while operating at a lower error-correcting rate during normal operation, thereby saving power.

We have focused on a prototype problem – ECC for nanoscale memory, using nano-PLA blocks and simple nano-gates (majority gate, nand/nor gates, etc.) as design components. We are using Gallager's Low Density Parity Codes (LDPC) for this application. LDPC codes have several advantages, which have made them popular in many communication applications: (1) low density of the encoding matrix, (2) easy iterative decoding, (3) generating large code-words that can approach Shannon's limit of coding. For the nano-computing application, we are using a particular type of LDPC code – the Gallager code, which is the original LDPC code proposed by Gallager. The advantage of this code is that the decoding H-matrix of this code can be expressed in a special form, $H^T = (H_1^T\ H_2^T\ H_3^T \ldots\ldots\ldots)$, H_1 is a matrix in the standard form [I : P], and H_2, H_3, . . . are permutations of H_1. Note that since LDPC is a linear code and H_1 is in the standard form, the generator matrix G can also be expressed in a similar form. One more useful result, which we are using in our work, is that the regular Gallager code can correct upto /2 errors. This form has two advantages that we will exploit. First, the hardware design for the encoder/decoder can be modular. We can use the same decoder (encoder) component for each H (G) matrix block along with a permuting array – this will make the design modular, and hence easy to implement (even with parity prediction for self-checking) using nano-PLA components.

Second, since the H (G) matrix is modular, we can use the LDPC with different error-correcting capability at different time of operation of the computing element. According to the bath-tub curve of failures [6], most components have a high failure rate in the initial phases of operation, which plateaus out in the middle range of the product's lifetime, and again increases towards the end. Since we can selectively enable modules of the ECC circuit at different times of the operation, so that is higher during the initial and end phases and low during the middle time of operation, we have the capability of changing the error correcting capacity of the encoder and decoder. This will give us high error correcting capacity when needed, but at the same time the modular enabling/disabling of the decoder/encoder blocks could enable significant power savings during normal operations. In his initial work, Gallager showed the existence of a LDPC code with H-matrix, but did not give a constructive proof. Recently, researchers in coding theory used different heuristic search algorithms (e.g., simulated annealing) to search through the space of all possible permutations of blocks to get H matrices with the particular properties outlined by Gallager. In recent work, Euclidean Geometry (EG) constructions over GF(2s) have been used to construct H-matrices for Gallager LDPC codes. Using EG(m, 2s), where each point in the geometrical space can be represented by a m-tuple over GF(2s), the H-matrix can be interpreted as an incidence matrix – every column of the matrix represent a point in this space, every row represents a line, and every entry of 1 in the matrix represents that the corresponding row line is incident on the column point. This connection has a lot of advantages for our application. Using the structure of EG(m, 2s), the Gallager H-matrix can be constructed quite efficiently, since this matrix has some useful properties, e.g., every Hi component in the matrix represents a set of parallel lines (a bundle), which can be easily enumerated using Galois Field operations. This obviates the necessity of a search algorithm for designing the H-matrix. Instead, for any size of the memory, we design the corresponding H-matrix efficiently using GF operations. The

geometric structure also makes the corresponding Gallager code de- code-able using a multi-step majority decoder, thus making it unnecessary to have iterative decoders.

C. PUBLICATIONS STEMMING FROM RESEARCH EFFORT

C. M. Lieber, Harvard University

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16. C. Yang, Z. Zhong and C.M. Lieber, "Encoding Electronic Properties by Synthesis of Axial Modulation Doped Silicon Nanowires," *Science* **310**, 1304-1307 (2005).

17. J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan and C.M. Lieber, "Ge/Si nanowire heterostructures as high-performance field-effect transistors," *Nature* **441**, 489-493 (2006).

18. Y. Li, J. Xiang, F. Qian, S. Gradecak, Y. Wu, H. Yan, D.A. Blom and C.M. Lieber, "Dopant-Free GaN/AlN/AlGaN Radial Nanowire Heterostructures as High Electron Mobility Transistors," *Nano Lett.* **6**, 1468-1473 (2006).

Papers Accepted for Publication

1. J.E. Savage, E. Rachlin, A. DeHon, C.M. Lieber and Y. Wu, "Radial Addressing of Nanowires," *J. Emerg. Technol. Comput. Syst.*

A. DeHon, California Institute of Technology

1. A. DeHon, "Design of Programmable Interconnect for Sublithographic Programmable Logic Arrays," *In Proceedings of the International Symposium on Field-Programmable Gate Arrays*, 127–137 (2005).

2. A. DeHon, "Nanowire-Based Programmable Architectures," *ACM Journal on Emerging Technologies in Computing Systems*, 1(2):109–162 (2005).

3. A. DeHon, and H. Naeimi., "Seven Strategies for Tolerating Highly Defective Fabrication," *IEEE Design and Test of Computers*, 22(4):306–315 (2005).

4. H. Naeimi, and A. DeHon, "A Greedy Algorithm for Tolerating Defective Crosspoints in NanoPLA Design," In *Proceedings of the International Conference on Field-Programmable Technology, IEEE*, 49–56 (2004).

5. H. Naeimi, and A. DeHon, "Fault Tolerant Architecture using Streaming and Rollback Recovery for Sublithographic Designs." In *Proceedings of the Workshop on the System Effects of Logic Soft Errors* (2005).

P. Kim, Columbia University

1. B. H. Hong, J. P. Small, M. S. Purewal, A. Mullokandov, M. Y. Sfeir, F. Wang, J. Y. Lee, T. F. Heinz, L. E. Brus, P. Kim, and K. S. Kim, "Extracting subnanometer single shells from ultra long multiwalled carbon nanotubes," *Proc. Nat. Acad. Sci. USA* 102, 14155-14158 (2005).

2. L. Venkataraman, Y. S. Hong, and P. Kim, "Electron Transport in a Multi-Channel One-Dimensional Conductor: Molybdenum Selenide Nanowires," *Phys. Rev. Lett.* 96, 076601 (2006).

3. J. P. Small and P. Kim, "Modulation of Thermoelectric Power in Individual Silicon Nanowires," Submitted (2006).

D. Presentations of Research **STEMMING FROM RESEARCH EFFORT**

C. M. Lieber, Harvard University, Invited Talks

1. August 13, 2004 – 2004 US-Korea Conference on Science, Technology and Entrepreneurship, Durham NC
   Plenary: "Nanoscience: Building a Big Future from Small Things"

2. September 14, 2004 - 131st Meeting of the National Cancer Advisory Board: Nanotechnology Seminar, Bethesda, MD
   "Nanoscience for Cancer Biology, Diagnosis & Treatment"

3. November 18, 2004 – Princeton Physics Colloquium Series, Princeton NJ
   "Nanoscience: Physics, Chemistry and Much More"

4. December 2, 2004 – 24th Army Science Conference, Orlando FL
   "Nanowire Nanosensors"

5. December 7, 2004 – 30th Anniversary of Samsung Electronics Semiconductor Business, Seoul Korea
   Keynote: "Nanotechnology: Emerging Opportunities in Electronics and Much More!"

6. December 14, 2004 – 2004 IEEE International Electron Devices Meeting, San Francisco CA
   "Nanowires: Building Blocks for the Assembly of Integrated Nanosystems"

7. 10 February 2005 – 27th Annual Alexander Graham Bell Lecture, McMaster University, Canada
   "Nanotechnology: From Biological Sensing to Electronics and Much More!"

8. 22 March 2005 – Second International Workshop on Nano and Bio-Electronics Packaging, Georgia Institute of Technology
   Keynote: "Nanowires: From Biological Sensing to Computing and Much More!"

9. 7 April 2005 – 2005 Fritz London Memorial Lecture, Duke University, Durham NC
   "Nanotechnology: Emerging Opportunities in Electronics, Biology and Much More!"

10. 5 May 2005 - Samuel McElvain Seminar Series (Materials Chemistry Division) University of Wiconsin-Madison
    "Nanoscience and the Pathway to Nanotechnologies"

11. 16 May 2005 – Gerhard Schmidt Memorial Lecture, Weizmann Institute of Science, Israel
    "Nanoscience & Nanotechnology: Emerging Opportunities in Electronics, Biology and Much More!"

12. 7 June 2005 – International Symposium on "Chemistry in the Emerging Fields of Nanotechnology and Biotechnology," Seoul National University, South Korea
"Nanotechnology: From Fundamental Science to Emerging Opportunities in Electronics, Biology and Much More!"

13. 8 June 2005 – Samsung SAIT, South Korea
"Nanotechnology: From Fundamental Science to Emerging Opportunities in Electronics, Biology and Much More!"

14. 9 June 2005 – China NANO 2005, Beijing China
Plenary: "Nanotechnology: Emerging Opportunities in Electronics, Biology and Much More!"

15. 9 June 2005 – Molecular Science Forum, Chinese Academy of Sciences, China
"Nanowires for Nanoscience and Nanotechnology"

16. 21 June 2005 – 65th Annual Physical Electronics Conference, University of Wisconsin-Madison
Keynote: "Nanoscience and the Pathway to Nanotechnologies"

17. 29 September 2005 – MESA+ Day Annual Meeting 2005, University of Twente, The Netherlands
Plenary: "Nanowires for Nanoscience and Nanotechnology"

18. 6 October 2005 – Symposium on Semiconductor Nanowires, Lund University, Sweden
Keynote: "Nanowires, Nanoscience and Emerging Nanotechnologies"

19. 24 October 2005 – Optics East 2005, Boston MA
Keynote: "Nanowire based electrical sensors for multiplexed detection of biological/chemical species down to single particle level, and new advances in nanophotonic sources/detectors for integrated optical-based sensing and/or photon detection"

20. 7 November 2005 – Fifth Annual Richard M. and Patricia H. Noyes Lectureship, University of Oregon
"Science and Technology at the Nanoscale"

21. 8 December 2005 – International Semiconductor Device Research Symposium 2005, Bethesda MD
Plenary: "Nanowires for Nanoscience and Nanotechnology"

22. 28 February 2006 – Gordon Research Conference on Bioanalytical Sensors, Ventura CA
"Nanowire Nanosensors"

23. 1 March 2006 – DARPA/MTO Workshop: Nanowires and Nanotubes for Defense Applications, Napa CA
"Nanowires and the Pathway to Multi-Functional Integrated Systems"

24. 4 April 2006 – MITRE Workshop on Nanosensors for Nose-Like Sensing, McLean VA
Keynote: "Toward Nanowire Bio-sensing Systems"

25. 25 April 2006 – Samsung Semiconductor Technology Advisory Committee Forum 2006, Seoul Korea
"Nanowires and the Pathway to Multi-Functional Integrated Systems"
Panel Discussion
Technical Seminar

26. 26 April 2006 – Peking University College of Engineering Distinguished Lecture, Beijing China
"Nanowires and Pathways to Nanotechnologies"

C. M. Lieber Group, Harvard University

1. July 19, 2004 – Gordon Research Conference on Nanostructure Fabrication, Tilton, NH
"Synthesis, Properties and Applications of Modulation Doped Silicon Nanowires"
(Chen Yang – Poster Presentation)

2. November 30, 2004 – Materials Research Society 2004 Fall Meeting, Boston, MA

"Branched and Hyper-branched Nanowire Structures as Building Blocks for Nanoelectronics and Nanophotonics "
(Fang Qian – Contributed Talk)

3. December 1, 2004 – Materials Research Society 2004 Fall Meeting, Boston, MA
"Synthesis, Properties, and Applications of Modulation-Doped Silicon Nanowires"
(Chen Yang – Contributed Talk)

4. December 1, 2004 – Materials Research Society 2004 Fall Meeting, Boston, MA
"Coherent Single Charge Transport in Molecular-Scale Silicon Nanowire Transistors "
(Zhaohui Zhong – Contributed Talk)

5. 13 March 2005 – 229th ACS National Meeting, San Diego, CA
"Single Charge Transport Studies in Silicon Nanowires"
(Zhaohui Zhong – Invited Talk on behalf of C. Lieber)

6. 16 March 2005 – 229th ACS National Meeting, San Diego, CA
"Fully Integrated High Frequency Nanowire Ring Oscillators"
(Michael McAlpine – Contributed Talk)

7. 21 March 2005 – 2005 APS March Meeting, Los Angeles, CA
"High Performance Ge/Si Core/Shell Nanowire Transistors with High-k Dielectrics"
(Jie Xiang – Contributed Talk)

8. 22 March 2005 – 2005 APS March Meeting, Los Angeles, CA
"Manipulation and Assembly of Semiconductor Nanowires with Holograhic Optical Traps"
(Ritesh Agarwal – Contributed Talk)

9. 23 March 2005 – 2005 APS March Meeting, Los Angeles, CA
"One-dimensional Hole Gas in Ge/Si Nanowire Heterostructures"
(Wei Lu – Contributed Talk)

10. 31 March 2005 – 2005 MRS Spring Meeting, San Francisco, CA
"Integration of Multiple Functions into Nanoscale Building Blocks"
(Yue Wu – Contributed Talk)

11. 31 March 2005 – 2005 MRS Spring Meeting, San Francisco, CA
"Fully Integrated High Frequency Nanowire Ring Oscillators"
(Robin Friedman – Contributed Talk)

12. 19 July 2005 – Gordon Research Conference: Chemistry of Electronic Materials, Connecticut College, New London, CT
"Nanowire Photonic Circuit Elements"
(Carl Barrelet – Poster Presentation)

13. 20 July 2005 – Gordon Research Conference: Chemistry of Electronic Materials, Connecticut College, New London, CT
"Integration of Multiple Functions into Nanoscale Building Blocks"
(Yue Wu – Poster Presentation)

14. 1 August 2005 – Gordon Research Conference: Clusters, Nanocrystals, and Nanostructures, Connecticut College, New London, CT
"Waveguiding and modulation of light in semiconductor nanowires"
(Andrew Greytak – Poster Presentation)

15. 2 August 2005 – Gordon Research Conference: Clusters, Nanocrystals, and Nanostructures, Connecticut College, New London, CT
"Fabrication of Semiconductor Core/Shell Nanowire Heterostructures by Atomic Layer Deposition"
(Yue Wu – Invited Talk)

16. 3 August 2005 – Gordon Research Conference: Clusters, Nanocrystals, and Nanostructures, Connecticut College, New London, CT
"Semiconductor Nanowire Heterostructure"
(Yue Wu – Poster Presentation)

17. 28 August 2005 – ACS Fall 2005 Meeting, Washington DC
"General synthesis and properties of manganese-doped II-VI and III-V diluted magnetic semiconductor nanowires"
(Pavle Radovanovic – Contributed Talk)

18. 29 August 2005 – ACS Fall 2005 Meeting, Washington DC
"General synthesis and properties of manganese-doped II-VI and III-V diluted magnetic semiconductor nanowires"
(Pavle Radovanovic – Poster Presentation)

19. 29 November 2005 – MRS Fall 2005 Meeting, Boston, MA
"Metal-Semiconductor Nanowire Heterostructures"
(Yue Wu – Contributed Talk)

20. 30 November 2005 – MRS Fall 2005 Meeting, Boston, MA
"Modulation-Doped Nanowires for Nanoelectronics and Nanophotonics"
(Chen Yang – Contributed Talk)

21. 13 March 2006 – 2006 APS March Meeting, Baltimore, MD
"Physics and Applications of GE/Si Core/Shell Nanowires"
(Jie Xiang – Contributed Talk)

22. 17 March 2006 – 2006 APS March Meeting, Baltimore, MD
"Challenges and Issues in Nanowire Nanodevices"
(Robin Friedman – Invited Talk)

23. 30 March 2006 – 231st ACS National Meeting, Atlanta, GA
"Nanowire Radial Heterostructures as High Electron Mobility Transistors"
(Yat Li – Contributed Talk)

24. 19 April 2006 – 2006 MRS Spring Meeting, San Francisco, CA
"1D Hole Gas in Ge/Si Nanowire Heterostructures and Demonstration of High Performance Field Effect Transistors"
(Jie Xiang – Contributed Talk)

25. 19 April 2006 – 2006 MRS Spring Meeting, San Francisco, CA
"Nanowire Radial Heterostructures as High Electron Mobility Transistors"
(Yat Li – Contributed Talk)

26. 19 April 2006 – 2006 MRS Spring Meeting, San Francisco, CA
"Integrated Silicon Nanowire Logic and Memory Arrays for Nanocomputing"
(Guihua Yu – Poster Presentation)

A. DeHon, California Institute of Technology

1. 10 July 2004 – International Technology Roadmap for Semiconductors' Emerging Research Architecture Workshop, San Francisco, CA
"Computing with Sublithographic Nanowire Building Blocks"

2. 22 September 2004 – IBM's Post-CMOS Deep Dive Workshop, Yorktown Heights, NY
"Nanowire-Based Sublithographic Programmable Logic Arrays"

3. 13 October 2004 – Altera Corporation, San Jose, CA
"Sublithographic Semiconductor Computing Systems"

4. 20 October 2004 – University of Texas Computer Engineering VLSI Seminar, Austin, TX
"Sublithographic Semiconductor Computing Systems"

5. 26 October 2004 – University of Illinois at Urbana-Champaign CompE Seminar, Urbana, IL
"Sublithographic Semiconductor Computing Systems"

6. 29 October 2004 – University of California Davis, Electrical & Computer Engineering EEC290 Seminar, Davis, CA
"Sublithographic Semiconductor Computing Systems"

7. 15 November 2004 – IBM Workshop: Science and Technology of Semiconducting Nanowires, IBM Research Laboratory, Zurich, Switzerland
"Nanowire-Based Sublithographic Programmable Logic Arrays"

8. 17 November 2004 – Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland
"Sublithographic Semiconductor Computing Systems"

9. 22 November 2004 – University of Wisconsin-Madison Electrical & Computer Engineering, Madison, WI
"Sublithographic Semiconductor Computing Systems"

10. 03 February 2005 – University of California of Los Angeles Electrical Engineering Seminar, Los Angeles, CA
"Sublithographic Semiconductor Computing Systems"

11. 14 April 2005 – University of Pennsylvania Electrical and Systems Engineering Seminar, Philadelphia, PA
"Sublithographic Semiconductor Computing Systems"

12. 26 April 2005 – Stanford University Electrical Engineering, Palo Alto, CA
"Nanowire-based Computing Systems"

13. 14 July 2005 – 5th International Forum on Application-Specific Multi-Processor on a Chip, Relais de Margaux, France
"Sublithographic Semiconductor Computing Systems"

14. 16 August 2005 – Advanced Research and Development Agency (ARDA) CMOS Nanotechnology Workshop, Park City, UT
"Nanowire-Based Programmable Logic Arrays"

15. 30 August 2005 – 6th International Workshop on Future Information Processing Technologies, Asheville, NC
"Atomic-Scale Computing"

16. 13 September 2005 – National Science Foundation Workshop: Architectures for Silicon Nanoelectronics and Beyond, Portland, OR
"Strategies for Tolerating Highly Defective Fabrication and Faulty Operation"

17. 15 September 2005 – Defense Advance Research Projects Agency's M2 Workshop: Math and Molecules, Evanston, IL
"Challenges and Opportunities"

18. 25 October 2005 – Frontiers of Extreme Computing Workshop: Transitioning Moore's Law to the Next Generation, Santa Cruz, CA
"Nanowire-based Computing Systems"

19. 8 November 2005 – The International Conference on Computer-Aided Design, San Jose, CA
"Hybrid CMOS/Nanoelectronic Digital Circuits: Devices, Architectures, and Design Automation"

20. 29 November 2005 – Brown University Electrical Engineering Talk, Providence, RI
"Nanowire-based Computing Systems"

21. 09 March 2006 – HRL Laboratories Talk, Malibu, CA
"Nanowire-based Computing Systems"

22. 27 March 2006 – The 7th International Symposium on Quality Electronic Design, San Jose, CA Tutorial: Emerging Technologies for VLSI Design

P. Kim, Columbia University

1. 6 Jul. 2003 - International conference on the science and application of nanotubes, Seoul, Korea,
"Mesoscopic Thermopower Measurement in Single Walled Nanotubes"

2. 7 Jul. 2003 - Special Departmental Seminar, Dept of Material Science, POSTECH, Pohang, Korea
"Electric and Thermal Transport Phenomena in Nanoscale Materials"

3. 4 Aug. 2003 - Stig Lundqvist Conference on Advancing Frontiers of Condensed Matter Physics, Trieste, Italy
"Mesoscopic Thermal Transport in Nanoscale Systems"

4. 10 Sep. 2003 - Physics Colloquium, Hunter College, New York, New York
"Mesoscopic Thermal Transport in Nanoscale Materials"

5. 21 Oct. 2003 - International Thermal Conductivity Conferences Knoxville, Tennessee
"Unusual High Thermal Conductivity in Carbon Nanotubes"

6. 9 Dec. 2003 - International Conference on Advanced Materials and Devices Jeju, Korea
"Electric and Thermal Transport Phenomena in Nanoscale Materials"

7. 22 Mar. 2004 - American Physical Society March Meeting Montreal, Canada
"Mesoscopic Thermal Transport Measurement in Nanotubes"

8. 12 May 2004 - American Electro Chemical Society Meeting, San Antonio, Texas
"Mesoscopic Thermal and Electrical Transport in Nanotubes"

9. 25 Oct. 2004- Optics East 2004, Philadelphia, Pennsylvania
"Carbon Nanotube Chemical Sensors"

10. 8 Dec. 2004 - 2nd International Symposium on Nanostructured Materials, Seoul, Korea "Electric and Thermal Transport in Nanoscale Materials"

11. 23 Jan. 2005 - Lecture in Nanotechnology, University of Washington, Seattle, WA "Electric and Thermal Transport in Nanoscale Materials"

12. 28 Jan. 2005 - Workshop on Strongly Correlated Electronic Materials, Princeton, NJ "Transport in Graphene and Other Layered Materials"

13. 1 Feb. 2005 - Materials Science Division Seminar, Brookhaven National Laboratory, Brookhaven, NY
"Electric and Thermal Transport in Nanoscale Materials"

14. 10 Feb. 2005 - Materials Science Department Seminar, Rensselaer Polytechnic Institute, Troy, NY
"Electric and Thermal Transport in Nanoscale Materials"

15. 22 Apr. 2005 - Korean Physical Society Meeting Seoul, Korea
"Electric Transport Spectroscopy in Nanoscale Materials"

16. 23 May. 2005 - Device Research Conference, Santa Barbara, CA
"Transport in Graphene and Other Layered Materials"

17. 20 Jul. 2005 - Summer School on Condensed Matter Physics, Center for Complex Materials, Princeton, NJ
"Electric and Thermal Transport in Nanotubes and other 1D Materials"

18. 28 Jul. 2005 - Molecular Conduction and Sensor Workshop, Purdue University, Lafayette, Indiana
"Electric Conductance in Nanotubes and Graphene"

19. 28 Sep. 2005 - Condensed Matter Physics Seminar, University of Pennsylvania. Philadelphia, PA
"Low Dimensional Transport Phenomena in Nanoscale Materials"

20. 5 Oct. 2005 - Graduate Seminar, University of Pittsburgh, Pittsburgh, PA
"Low Dimensional Transport Phenomena in Nanoscale Materials"

21. 12 Oct. 2005 - Physics Department Seminar, Yale University, New Haven, CN
"Low Dimensional Transport Phenomena in Nanoscale Systems"

22. 24 Oct. 2005 - Chez Pierre Seminar, MIT, Cambridge, MA
"Low Dimensional Transport Phenomena in Nanoscale Materials"

23. 7 Nov. 2005 - Condensed Matter Physics Seminar, Case Western Reserve University, Cleveland, OH
"Low Dimensional Transport Phenomena in Nanotubes and Other Low Dimensional Systems"

24. 17 Nov. 2005 - Department Colloquium, Princeton University, Princeton, NJ
"Quantum Physics at Your Pencil Tips: Dirac Fermions in Graphene"

25. 18 Nov. 2005 - Condensed Matter Physics Seminar, SUNY Stony Brook, Stony Brook, NY
"Low Dimensional Transport Phenomena in Nanoscale Materials"

26. 7 Jan. 2006 - Interaction and Dynamics in Low Dimensional Quantum Systems Conference, Weizmann Institute Rehovot, Israel
"Experimental Observation of Quantum Hall Effect in Graphene"

27. 12 Jan. 2006 - Nanoelectronics 2006, Lancaster University, Lancaster, United Kingdom, "Unusual Transport in Graphitic Nanoscaled Materials: Nanotubes and Graphene"

28. 17 Jan. 2006 - New York Nanoscience Discussion Group, New York University, New York, NY
"Novel Transport Phenomena Carbon Based Nanoscaled Materials"

29. 2 Feb. 2006 - Condensed Matter Physics Seminar, Rutgers University, New Brunswick, NJ
"Unusual Transport in Graphitic Nanoscaled Materials: Nanotubes and Graphene"

30. 15 Feb. 2006 - Condensed Matter Physics Seminar, Pennsylvania State University, College Park, PA
"Low Dimensional Transport Phenomena in Nanoscale Materials"

31. 20 Feb. 2006 - Department Colloquium, Cornell University, Ithaca, NY,
"Quantum Electrodynamics at Your Pencil Tips: Dirac Fermions in Graphene"

32. 6 Mar. 2006 - International Winter School of Electronic Properties of Novel Materials, Kirchberg, Austria
"Unusual Transport in Graphitic Nanoscaled Materials: Nanotubes and Graphene"

33. 13 Mar. 2006 - American Physical Society March Meeting, Baltimore, MD
"Experimental Observation of Quantum Hall Effect in Graphene"