High Efficiency Class-F MMIC Power Amplifiers at Ku-Band

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Abstract

Two high efficiency Ku-band pHEMT power amplifier MMICs are presented in this paper. A single stage, high efficiency amplifier provides a peak power added efficiency of 57.6% with 10.5 dB associated gain and 26.5 dBm output power into a 50Ω load at 14 GHz. Additionally, a dual stage, high gain amplifier provides a peak power added efficiency of 50.4% with 19.7 dB associated gain and 27.5 dBm output power into a 50Ω load at 14.3 GHz. State-of-the-art efficiency performance at these frequencies is achieved through Class-F transistor operation. Process selection, circuit design, and measured results are described.

1. Introduction

Current wideband transmit apertures for airborne platforms are generally based on single beam, mechanically steered reflector antennas and traveling wave tube amplifiers (TWTAs). Installation of these large apertures on airframes is complex and costly. The challenges associated with installation include limited real estate, airframe structural integrity, airstream projection and drag, co-site interference, link coverage, thermal dissipation, and thermal signature. These problems have led to the development of one-of-a-kind solutions for each type of airborne platform, increasing the cost of realizing required communications capabilities and limiting the installation of high data rate terminals on airframes.

Phased arrays have the potential to mitigate many of the challenges involved in placing apertures on airframes, while providing multiple simultaneous beams and enhanced beam control capabilities. The distributed solid state power amplifiers (SSPAs) or receivers in an array also provide graceful degradation. Integration of radio frequency (RF) transmit and beamforming elements into an array structure eliminates the power losses associated with the RF transmission line between the antenna and power amplifier. One problem that has hindered the development of arrays suitable for mobile
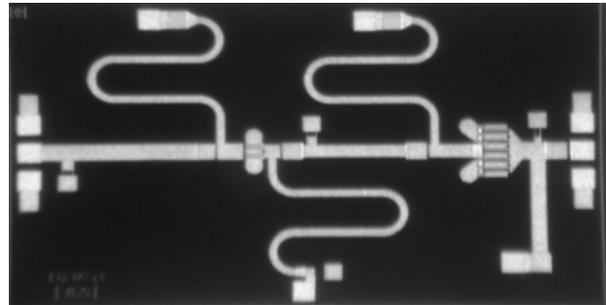
Figure 1. Photograph of the dual-stage Ku-band high efficiency power amplifier MMIC. Chip size is 4 mm X 1.8 mm.

communications is the significant thermal load that is generated by the solid state power amplifiers in the array, due in part to poor conversion efficiency at microwave and millimeter wave frequencies. Decreasing the thermal load in the array can be accomplished by increasing the amplifier DC to RF conversion efficiency. High efficiency power amplifiers at high microwave or millimeter-wave frequencies are a key enabling technology for the realization of transmit arrays for high data rate airborne communications.

Significant work has been done on high efficiency modes of operation at UHF through L-band frequencies, motivated by the extension of battery life in consumer products for wireless mobile applications. Traditionally, solid state power amplifier efficiency at higher microwave frequencies has been improved through semiconductor device enhancement [1-2]. By increasing the gain or decreasing the internal loss of a device, a designer can consequently improve the power added efficiency (PAE) of an amplifier because the conduction angle of the current waveform can be reduced without compromising power gain. However, the maximum attainable PAE for these designs is fundamentally limited to between 60% (for Class AB) and 78.5% (for Class B). High efficiency modes of operation offer significant improvements in PAE. The theoretical maximum PAE for Class E and F modes of operation is near 100%. Until recently, work on these high efficiency modes of operation has been limited at higher frequencies, in part

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1. REPORT DATE **2005**	2. REPORT TYPE	3. DATES COVERED **00-00-2005 to 00-00-2005**

4. TITLE AND SUBTITLE **High Efficiency Class-F MMIC Power Amplifiers at Ku-Band**	5a. CONTRACT NUMBER
	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **MITRE Corporation,202 Burlington Road,Bedford,MA,01730-1420**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT **unclassified**	b. ABSTRACT **unclassified**	c. THIS PAGE **unclassified**		**4**	

due to modeling and linearity issues. The transistor models needed for high efficiency modes of operation have not been well developed. Additionally, high efficiency modes of operation result in degradation of some aspects of amplifier performance, especially linearity. Non-linearity in an amplifier can result in unacceptable levels of distortion for the modulation waveforms and access methods used in certain communication systems. Extensive research is currently underway to develop methods which mitigate linearity issues, including pre-distortion and new modulation waveforms [3-4].

This paper describes a high efficiency Class F power amplifier design at Ku-Band to be used in a phased array application. The circuit and results presented in this paper pertain to a first pass design. A single-stage high efficiency amplifier and a dual-stage high gain amplifier (shown in Figure 1) were fabricated using a commercially available 0.25 um pseudomorphic HEMT process. Measurements of the DC-to-RF conversion efficiency of these new monolithic microwave integrated circuit (MMIC) amplifiers represent a significant advance in the state-of-the-art at this frequency.

2. PHEMT Process

Performance, process maturity, device models, and risk were evaluated for a number of semiconductor processes and devices, including GaAs MESFET, GaAs HBT, SiGe HBT, GaAs pHEMT, InP HEMT, and GaN HEMT. A 0.25 um T-gate GaAs pHEMT process from TriQuint was selected for this effort. These pHEMT devices have good performance at Ku-band, and transistor models are available for linear classes of operation. This process has an Idss of 285 mA/mm, an Imax of 510 mA/mm, a peak transconductance of 375 mS/mm, and an Ft of 60 GHz [5]. Load pull data for output power and PAE was not provided by the foundry at currents near pinchoff.

3. Design

Traditionally, the goal of power amplifier design is to present the optimal value of impedance, Γopt, to the drain of the transistor so that maximum power transfer to the load is achieved. The value of Γopt can be found through load pull measurements or by implementing a loadline match with careful attention paid to device parasitics. The objective of Class F power amplifier design, in addition to the previously stated goal, is to control the harmonic impedances at the current source of the transistor so that the normally sinusoidal voltage waveform becomes a square wave [6]. This is achieved by providing a short circuit to the even harmonics and an

open circuit to the odd harmonics. Class F waveforms have higher efficiency then corresponding sinusoidal waveforms because the squared voltage is at zero for a longer period of time while the current is on. At low frequencies, this functionality can be achieved by using a simple short-circuit quarter wave stub. However, at microwave frequencies, the parasitic components of the device tend to distort the quarter wave stub functionality relative to the current source and so a different approach
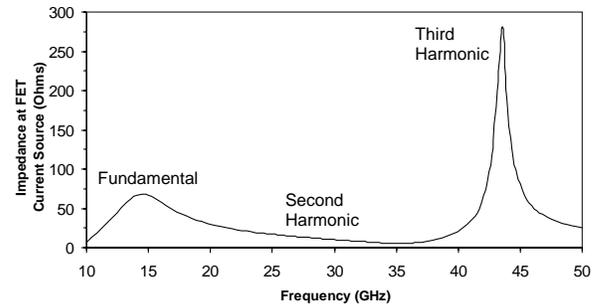

Figure 2. Input impedance as a function of frequency across the current source of the 1 mm transistor

must be used. A third harmonic peaking circuit at X-Band was developed by Kopp and Pritchett [7], which includes the parasitic drain-source capacitance, Cds, as part of the design. This technique uses an LC network attached in shunt to the drain of the device to invoke a short circuit resonance at the second harmonic. Additionally, the parallel combination of the internal capacitance and the LC network presents a high impedance to the third harmonic. Values for the LC network were calculated through this approach and were then optimized using the Agilent ADS harmonic balance simulator [8]. Initial simulations indicated that it was also necessary to include the gate-drain capacitance Cgd when calculating circuit values. Due to practical constraints, higher order harmonics were not targeted for this design. The impedance presented to the current source of the transistor is shown in Figure 2, and corresponding Class F waveforms and loadlines are shown in Figure 3.

A 1 mm device was chosen for the design. Nonlinear simulations showed that this device size offered the best tradeoff between PAE and power gain. It was necessary to scale the model provided by the foundry to operate under Class F bias conditions due to the highly nonlinear nature of the parasitic components in pHEMT devices [9]. Since this model was originally intended for use in a linear amplifier design, it was unknown how accurately the scaled version would predict large signal operation under reduced bias currents. Transmission lines, capacitors and substrate vias were analyzed using formula-based distributed models. A number of iterations

were performed to realize a physical layout. Once a layout was generated, EM simulations using Agilent's Momentum 2.5D simulator [10] were used to more accurately characterize the matching networks. This amplifier was implemented on the chip as a stand-alone module.
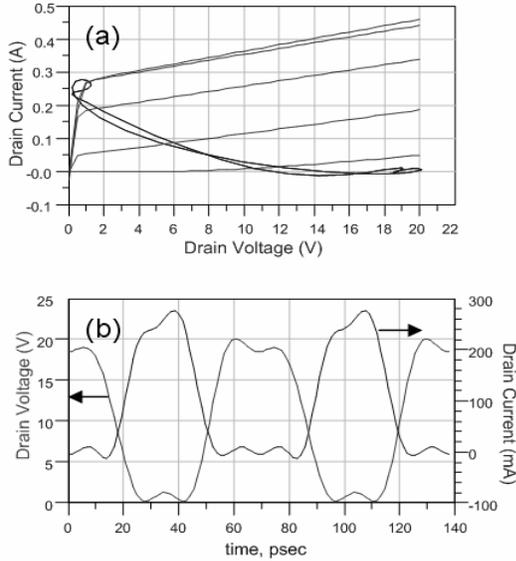

Figure 3. (a) Dynamic loadline and (b) voltage and current waveforms at the ideal current source of the transistor

In addition to efficiency, high gain was also desired for the array application. A driver stage was added to the existing Class F amplifier topology to increase the power gain. The driver was implemented using a smaller 300 um FET operating under suboptimal drain bias conditions to provide a minimal impact on power added efficiency. The low-pass interstage matching network between the transistors provides a loadline power match to the output of the driver stage and a conjugate match to the input of the power stage. A schematic of this circuit is shown in Figure 4 and a photograph of the chip is shown in Figure 1.

4. Results

The two power amplifier modules were diced and packaged separately in a StratEdge 50GHz package [11]. The package was used to house the external bypassing components while microwave GSG probes were used to bring the RF signals to and from the chip. The RF probe losses were removed from the measurements to provide de-embedded results at the chip level. DC probes were used to deliver the bias voltages to the package. This strategy allowed for circuit stabilization with no impact

on the in-band performance of the amplifier. After the initial testing, the package was mounted in a microstrip test fixture for further characterization.
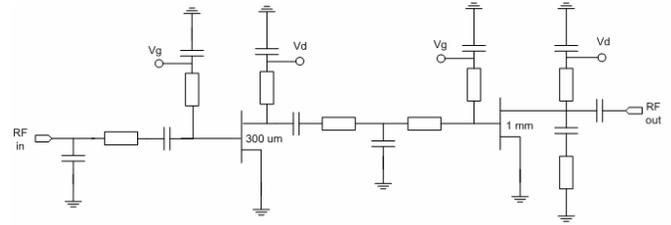

Figure 4. Schematic of dual stage amplifier

Performance for both the single stage and dual stage amplifiers is summarized in Table 1. The peak efficiency of 57.6% for the single stage amplifier is state-of-the-art at this frequency. Greater than 50% PAE was measured over a 400 MHz bandwidth for the single stage amplifier. From the simulations, an output network loss of 0.5 dB was calculated, resulting in a peak device efficiency of 64.4%. Measured compression curves for the single stage amplifier are shown in Figure 5 at 13.95 GHz, with the transistor biased at Vd=9V, Id=9 mA (~3% Idss).

Parameter	High Gain Amp	High Efficiency Amp
Maximum PAE	50.4% @ 14.3 GHz	57.6% @ 13.95 GHz
Power Gain @ Max PAE	19.7 dB	10.5 dB
Output Power @ Max PAE	27.5 dBm (.56 W)	26.5 dBm (.45 W)
3 dB Gain Bandwidth	14.0-15.0 GHz	12.9-14.7 GHz
1 dB Gain Bandwidth	14.1-14.75 GHz	13.2-14.3 GHz

**Table 1. Power amplifier performance summary**

Maximum efficiency of 50.4% for the dual stage amplifier occurs at 14.3 GHz, however, the amplifier achieves better gain and power performance at 14.5 GHz while still maintaining 50.2% PAE. Compression curves are shown in Figure 6 at 14.5 GHz, with the driver transistor biased at Vd=5.6V, Id=14 mA (~16% Idss) and the output transistor biased at Vd=10.5V, Id=7 mA (~2.5% Idss). The dual stage amplifier maintained greater than 50% PAE over a 300 MHz bandwidth. As these results indicate, the best efficiency performance for both circuits was attained with the transistors biased well below pinchoff. Swept frequency performance is plotted in Figure 7 for the dual stage amplifier at the previously stated bias point with an input power of approximately 8 dBm. Large signal simulated output power and PAE are also shown as dashed lines on this plot. Although these models were not intended to be used at low bias currents, the large signal simulations did predict the center frequency and general shapes of the output power and PAE curves.
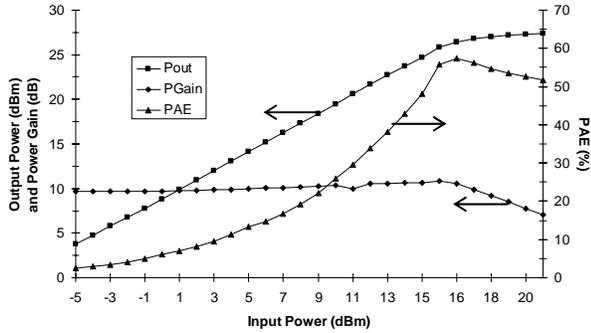
Figure 5. Measured output power, gain and PAE as a function of input power at 13.95 GHz for the single-stage, high efficiency power amplifier.
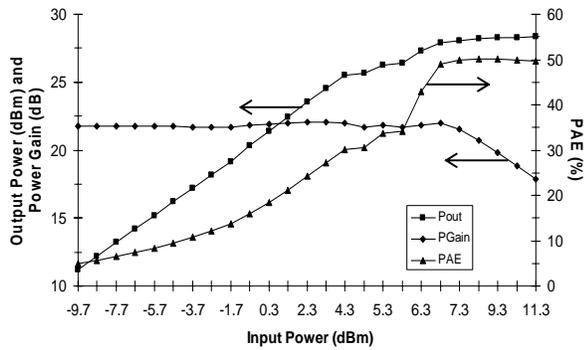
Figure 6. Measured output power, gain and PAE as a function of input power at 14.5 GHz for the dual-stage, high gain power amplifier
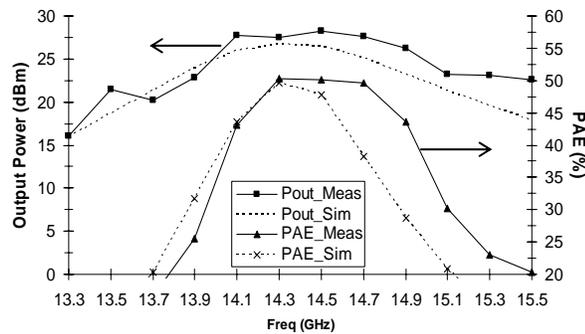
Figure 7. Measured and Simulated output power and PAE for the dual-stage, high gain power amplifier as a function of frequency. Pin=8 dBm.

5. Conclusion

Two high efficiency MMIC power amplifier modules have been demonstrated. A peak power added efficiency of 57.6% at 14 GHz was obtained using a single stage Class F topology. In a second design, a driver stage was added to the previously designed amplifier to increase the power gain by 9.2 dB while providing a minimal degradation in PAE. High efficiency power amplifiers have the potential to significantly reduce the thermal load in a phased array. In the future, improved device technology coupled with high efficiency power amplifier circuit topologies will help to enable the realization of transmit arrays for high data rate airborne communications.

6. Acknowledgements

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