Development of Heterostructure Materials for Thermoelectric Device Applications

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1. Abstract

A seed program was performed to establish directions for materials research in lead salt quantum dot superlattices. The objective is to define a program that could increase the ZT of quantum dot superlattices in the lead salt system, as well as move in a direction compatible with future DOD commercial access. This final report for the seed contract also acts as the main input into a proposal for future work, submitted in parallel. We propose that the future program will first concentrate on connecting microstructure to ZT performance, elucidating the structure-property relations for this system and leading to further optimization of the structure. The lead salt superlattices will be investigated in collaboration with MIT Lincoln Laboratories, where all film deposition will take place. As ZT is improved for thin film thermoelectrics, we will investigate depositing these structures on alternative substrates that will facilitate economic device fabrication. Of particular interest is the deposition of quantum dot superlattices on stainless steel, aluminum, and silicon substrates. Another issue in the anticipated scaling of thin film thermoelectrics is long term reliability. We will employ characterization techniques to study the stability of thin film thermoelectrics, including the potential use of in-situ TEM observations. Device work using new structures and substrates will be accomplished through collaboration with the Harman-Turner ONR project at Lincoln Laboratories. A successful research program will elucidate future paths for thermoelectric commercialization.

2. Significance of Opportunity and Background

Thermoelectric materials have been researched extensively over several decades for power generation and refrigeration applications. The key materials properties that determine a material's suitability for thermoelectric applications are its Seebeck coefficient, S, its electrical conductivity, σ, and its thermal conductivity, κ. These three materials properties can be combined, along with the absolute temperature of operation, to create the dimensionless figure of merit

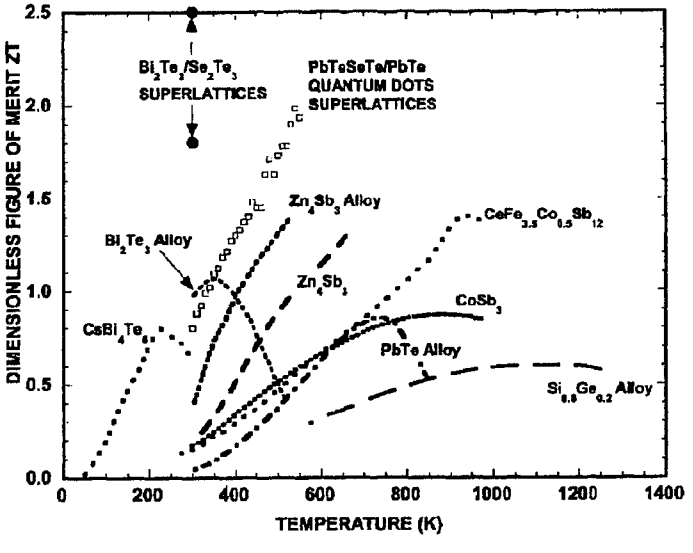

Figure 1: ZT for Various Materials Systems over a Wide Range of Operating Temperature. [1]

$$ZT = \frac{S^2 \sigma T}{\kappa} \qquad (1)$$

Materials with $ZT>>1$ are of great interest for thermoelectric applications. However, such a figure of merit has been difficult to achieve and this has limited the use of thermoelectrics to applications that require much greater reliability (*e.g.*, space power applications) than traditional power generation or refrigeration methods, or applications that require the compactness (*e.g.*, cooling of microelectronics) that thermoelectric materials can provide. There is a pressing need for materials

engineering efforts to fabricate high *ZT* materials that will enable new thermoelectric cooling and power generation applications.

In general, there is a strong emphasis on engineering materials with higher ZT, however, it should be noted that this task is further complicated when considering the operating temperature for the thermoelectric application in question. Figure 1, taken from Chen, *et al.*, shows state-of the-art results for thermo-electric materials over a wide range of operating temperatures. Examining the bulk configurations (*i.e.*, no superlattice or quantum dot configurations) in the diagram, one can see why Bi_2Te_3 alloys are commonly used for room temperature (300 K) applications and Ge_xSi_{1-x} alloys are preferred at extremely high temperatures (>900 K). There are a wide variety of materials systems in the regime between these limits that exhibit very interesting thermoelectric properties. For the very important applications of waste heat energy conversion from automotive engines and nuclear reactors the temperature range of interest is from 450 to 650 K. One of the key opportunities for commercial and military applications is the development of high *ZT* materials in this temperature range. Thin film, not bulk, thermoelectric materials have shown the most promise for enabling the highest performance thermoelectric devices.

Since the advent of epitaxy techniques that allow for materials engineering of a suite of materials at the nanometer scale, two-dimensional quantum wells, one-dimensional quantum wires, and zero-dimensional quantum dots have attracted the interest of researchers attempting to create superior thermoelectric materials. The combination of quantum wells into superlattice structures, with the incorporation of quantum dots, has been of special interest. Figure 1 shows that PbTeSe/PbTe quantum dot superlattices have demonstrated to exhibit excellent *ZT* characteristics, especially in the temperature range of interest for energy conversion from waste heat from automotive and nuclear vessels. However, the study of these materials is very much at the nascent stage, where the effects of microstructure, defect morphology, and process conditions on device performance and reliability are not completely understood, and as such, have not been optimized. In addition, the current fabrication methodologies are very time consuming and unlikely to be economical in wide-scale applications. There is a significant opportunity to advance the state-of-the-art in PbTe-based thin film thermoelectric materials for application in power generation for commercial and military application.

The deliverables from the proposed program will center on fundamental understanding and optimization of the thermoelectric properties PbTeSe/PbTe quantum dot superlattice (QDSL) materials system, going further to establish the feasibility of alternative substrates and growth techniques to enable more cost effective solutions for wide-scale implementation of high *ZT* PbTe-based thermoelectrics.

2.1 Overview of Bulk Thermoelectric Devices

The emphasis of the proposed research program is on connecting detailed structure to thermoelectric properties in nanoscale thermoelectric materials. This research program can influence both thin film devices (*i.e.*, superlattice-based) thermoelectric devices and bulk thermoelectric materials. We briefly review previous work below.

Bi_2Te_3 alloyed with Sb_2Te_3 and/or Bi_2Se_3 is commonly used at room temperature However, Bi_2Te_3 alloys can only achieve a *ZT* of about 1 at room temperature, although there have been reports of enhanced *ZT* up to about 1.4 at 300K with post processing of the as-grown crystals. [2] Even with enhanced *ZT* at 300K, the thermoelectric properties of bulk Bi_2Te_3 decay with increasing temperature and are not suitable for operating temperatures greater than 400K.

Bulk, polycrystalline Ge_xSi_{1-x} alloys prepared by powder metallurgical methods have been shown to have excellent applicability to thermoelectric power conversion at high temperatures and have been implemented for spaced-based power applications. The primary advantage of the alloying Si with Ge (and vice versa) is the potential six-fold reduction in the thermal conductivity of the material.[3] With optimized doping, Ge_xSi_{1-x} can display ZT values for n-type and p-type alloys of 0.9 and 0.5, respectively, at temperatures above 1000K.[4]

The Bi_2Te_3 and Ge_xSi_{1-x} alloy systems have been extensively studied, so there is little investigation into improving their bulk properties. Much of the present work on optimization of bulk thermoelectric properties has focused on the fabrication of phonon-glass-electron crystals, which are targeted at having high electrical conductivity (large electron [hole] mean free paths) while having poor thermal conductivity (small phonon mean free paths). Materials based upon the skutterudite, $CoAs_3$, structure have been at the forefront of this approach. Skutterudites have large unit cells with the atoms having low coordination numbers, leading to large voids in the crystal structure. The strategy with skutterudites has been to fill the voids with elements that disrupt phonon propagation, while maintaining desirable electrical properties.[5] The choice of the element placed in the voids and the fraction of the voids filled play a significantly effect the thermal conductivity.[6] Investigators have shown that skutterudites have the potential for ZTs greater than 1.[7]

Despite the advances in bulk thermoelectric materials, the ZT values are still fall far short of the values required for substantial efficiency improvements for power generation applications. For example, a ZT of 1 corresponds to only an energy conversion efficiency that is approximately 30% of the ideal Carnot efficiency, whereas a ZT of 4, allows for a conversion efficiency that is 55% of that is allowable by thermodynamic constraints.[8] Quantum-well/superlattice-based thermoelectrics have shown the promise to achieve highly efficient energy conversion efficiencies.

2.2. Overview of Quantum-Well/Superlattice Thermoelectric Devices

There are several advantages of reduced dimensionality in superlattice structures, which affect every term in equation 1. Although there are tradeoffs depending on which term one wishes to optimize, superlattice structures provide additional degrees of freedom to tailor better thermoelectric properties. First, the Seebeck coefficient, S, is heavily dependent on the band structure, specifically the number of sub-bands that contribute to the Seebeck coefficient and the density of states in each band. The reduced dimensionality in quantum wells decreases the number of bands that contribute to the Seebeck coefficient and creates a more discrete (*i.e.*, less continuous) distribution of density of states in-plane, enhancing the thermoelectric properties of the system.[9] Modeling has shown that the greater the potential well for the quantum well layers and the smaller the superlattice period, the better the figure of merit.[10] In addition to the tailoring of the band structure, superlattice structures can take advantage of the density of states mass, m, and carrier mobility, μ, anisotropies in many materials. The density of states mass affects both S and σ in equation 1. Interestingly, it is the product, $\mu m^{3/2}$, that should be maximized for optimal thermoelectric properties. Thus, increasing mobility via reducing the density of states mass does not provide the best benefits. Nevertheless, for the case of Bi_2Te_3 quantum wells with a_0-c_0 crystallographic plane orientation and current flow in the high mobility a_0 direction, theory has shown that quantum well structures have the potential to improve ZT over the bulk value by a factor of 13.[11] Lastly, it is well known that interfaces and local variations in microstructure reduce the thermal conductivity of materials. Superlattices with their many interfaces of

dissimilar materials reduce the thermal conductivity, as long at the characteristic lengths of the films in the superlattice are less than the phonon mean free path in the bulk materials. In general, this corresponds to a decreasing thermal conductivity with decreasing film period. Superlattices with alternating Si and Ge layers <70 Å in period have thermal conductivities that are much less than pure Si, pure Ge, or Ge_xSi_{1-x} alloys.[12]

In practice, since the wells and the barriers in superlattices are dissimilar materials, strains are inherent in these structures and as such, the choice of materials for the wells and barrier layers has limitations. Some of the common materials systems fabricated into thermoelectric superlattice structures have been Ge_xSi_{1-x}/Si superlattices[13], $Ge_xSi_{1-x}/Ge_ySi_{1-y}$ superlattices on relaxed Ge_zSi_{1-z} buffers[14], Bi_2Te_3/Sb_2Te_3 superlattices[15], and $PbTe/PbSe_xTe_{1-x}$ superlattices[16]. As mentioned earlier, quantum dots can be embedded into superlattices to form what are called quantum dot superlattices (QDSLs). QDSLs have also been fabricated with the $PbTe/PbSe_xTe_{1-x}$ materials system via the incorporation of PbSe island formation during epitaxy.[17]

Table 1 lists the results of three important attempts to use superlattice (SL) structures for enhanced *ZT*. For reference, a typical *ZT* value for bulk $(Bi,Sb)_2(SeTe)_3$ alloys[18] and a modeled optimum *ZT* for a $Ge_{0.30}Si_{0.70}$ alloy[16] are also tabulated. It is important to note that SL structures have been able to achieve *ZT* values far exceeding traditional bulk materials. Bulk materials have recently made progress, achieving *ZT* values greater than 2 as well.[19] However, the values are still not high enough to be competitive with traditional methods of refrigeration and power generation. In the case of Ge/Si SL structures, the *ZT* is not competitive enough to displace bulk Ge_xSi_{1-x} alloys. However, theory predicts that Ge/Si superlattices could achieve *ZT* as high as 1.25 at 300K and 1.5 at 600K.[20]

Much work needs to done to establish not only better *ZT* values with SL structures, but also much further understanding of the relationships between the exhibited thermoelectric properties and the microstructures. Since PbTe-SL-based materials system has exhibited excellent potential for thermoelectric power generation applications in the much desired temperature range between 450-650K, it will be the focus for the proposed research program.

Although not the focus of the proposed work plan, quantum well structures can also exhibit thermionic effects, where hot carriers are selectively emitted over a barrier between the cathode and the anode leading to cooling effects and what may appear to be enhanced thermoelectric properties.[23] To our knowledge, these effects have not been investigated in PbTe-based SL structures and any observations to this effect would be novel scientific work.

Table 1: Reported ZT values for several materials systems

Material	Carrier Type	ZT at 300K	Reference
$(Bi,Sb)_2(Si,Te)_3$ bulk alloys	N/P	1.0	G.D. Mahan[18]
$Ge_{0.70}Si_{0.30}$ bulk alloys	N	0.17	C. B. Vining [21]
Si/Ge SL on $Ge_{0.5}Si_{0.5}$	N	0.10	Koga [20]
Bi_2Te_3 SL	P	2.4	Venkatasubramanian [15]
PbTe QDSL	N	1.6	Harman [22]

2.2.1. Lead-salt Superlattice Structures

Lead-salt superlattice structures comprising of PbEuTe/PbTe[23] planar and PbTeSe/PbTe[24] quantum dot superlattice (QDSL) heterostructures have recently been used to demonstrate high ZT performance in the 300-650K temperature range. Based on theoretical models, the enhanced ZT of quantum well superlattices over conventional bulk materials is due to a combination of factors including electron confinement and phonon-filtering effects.[1]

Ted Harman *et al.* have recently demonstrated high ZT in QDSL structures utilizing the PbTeSe/PbTe material system. The 5.2% lattice mismatch between PbTe (a_o=6.462Å) and PbSe (a_o=6.126Å) causes the $PbSe_{1-x}Te_x$ layers to grow via the Stranski-Krastanov mechanism, leading to $PbSe_{1-x}Te_x$ quantum dots embedded within a PbTe matrix. These structures are grown by molecular beam epitaxy (MBE) on BaF_2 substrates which are chosen for their lattice constant and coefficient of thermal expansion, both of which are closely matched to PbTe. The QDSL device layer requires growth of a ~100 μm thick heterostructure which is subsequently removed from the substrate for fabrication of the TE test element. Therefore, the BaF_2 substrate is also a convenient choice for selective removal relative to PbTe by chemical etching.

In a recent publication[22], Harman *et al.* have reported a ZT of 1.6 and 3 at temperatures of 300 and 550K, respectively, in Bi-doped n-type PbSeTe/PbTe QDSL samples. Complementary p-type TE elements also show high ZT (1.1 at 300K) in early experiments. Even more notably, these results were obtained from structures which have been neither characterized, nor optimized for material quality or film morphology. Larger values of ZT are quite likely upon closer examination of the effects of growth parameters on the evolution of microstructure in these QDSL heterostructures.

3. Technical Focus

As previously mentioned, the underlying factors that yield large ZT in current lead-salt QDSL structures are poorly understood in that the effect of film microstructure on thermoelectric performance has not been closely correlated. While there are opportunities in materials research for further improvement of QDSL structures, the full potential of high ZT thermoelectrics can only be realized if the issues of device fabrication are also addressed. Among these are the formation of low resistance contacts, fabrication of TE arrays and development of alternate substrate and deposition methods for increasing the throughput of QDSL material growth. The issues of contact resistance and TE array fabrication are addressed in Ted Harmon's proposal to ONR dated 2/7/2005. Here we focus on the research opportunities pertaining to QDSL material growth and microstructure optimization.

3.1. Optimization of QDSL Microstructure and Growth

The large figure of merit measured by Harman *et al.* was obtained from a QDSL structure in which the microstructure has not been microstructurally characterized with TEM. It is quite likely that even larger values of ZT can be obtained after a thorough examination of the effect of growth parameters on material quality and quantum dot microstructure. The islanded film morphology of the PbTeSe/PbTe QDSL structure arises as a result of the lattice mismatch between PbTe and PbTeSe. The quantum dot morphology (size, density, etc.) can be tailored by altering the strain of the $Pb_xSe_{1-x}Te$ layer and growth parameters. The substrate also has an effect on quantum dot morphology. It was previously shown that self assembled growth of highly uniform PbSe/PbTe quantum dots is possible on a Si(111) surface.[43] This effect was

attributed to heterogeneous nucleation on the surface steps generated by a high density of misfit dislocations at the highly mismatched PbTe/Si interface. This is yet another benefit of growing these structures on Si substrates as a high density of highly-ordered, uniformly-sized quantum dots is expected to provide high values of ZT.[25] Additional adjustment of the lattice constant mismatch will also be possible with PbTe/$Pb_{1-x}Sn_xSeTe$ structures which are also expected to yield higher power factors owing to increased carrier confinement. Much of the mechanistic theories of material structure in the thin film QDSLs are largely speculative, and therefore a ripe area for investigation.

Previous work exploring the evolution of quantum dot microstructure includes the effect of layer thickness and growth temperature on the ordering of PbSe/PbEuTe quantum dots by Kang, *et al.*.[44] The authors have shown that microstructures ranging from self-assembled to disordered dots can be grown by altering the thickness of the PbEuTe spacer layer as illustrated by the series of TEM micrographs in Figure 4. In this unusual case, the microstructure is investigated, but no correlation to TE measurements and devices is done. Furthermore, the largest thickness of the QDSL structures studied by Kang, *et al.* consisted of only 30 periods. Very thick (50-100 μm, corresponding to ~10,000 periods) PbTeSe/PbTe structures have not yet been studied. The evolution of microstructure in these thick QDSL structures will be affected if strain accumulates during film growth. Harman has indicated that indeed there are surface morphology changes as thick QDSLs are grown. Therefore, a correlation of strain and film morphology by x-ray and TEM analysis will be important for development of TE devices based on these structures.

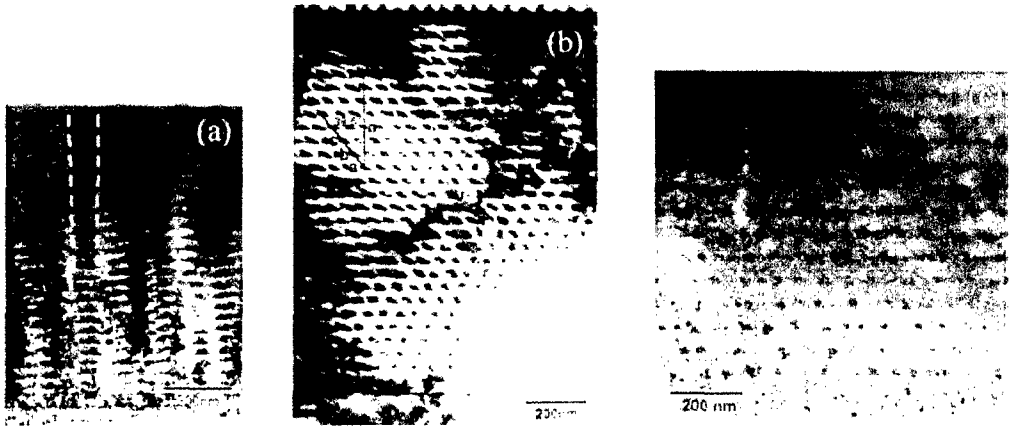

Figure 4: Cross-sectional TEM micrographs of PbSe/PbEuTe QDSL morphology as a function of PbEuTe spacer thickness adapted from H. Kang, *et al.*[44] (a.) PbSe quantum dots with linear stacking, (b.) PbSe quantum dots with FCC-like stacking, (c.) PbSe quantum dots with disordered stacking. The thermoelectric properties as a function of these morphologies have not been characterized.

3.2. Alternative Substrates for Epitaxial QDSL Structures

Theoretical calculations[32] and experimental data[24,33] show that the thermoelectric figure of merit in lead-salt multiple-quantum-well (MQW) structures is highest along the <111>

direction. Consequently, PbTeSe/PbTe QDSLs are grown on (111)-oriented BaF_2 substrates to maximize their thermoelectric figure of merit. BaF_2 also has a coefficient of thermal expansion which is matched to that of PbTe ($\alpha_{PbTe} \approx \alpha_{BaF2} = 19.8 \times 10^{-6}\ K^{-1}$) allowing growth of thick films at elevated temperature with minimal thermal stress. Furthermore, a BaF_2 substrate allows the QDSL structure to be removed from the substrate for TE device fabrication by selective chemical etching. Unfortunately however, BaF_2 is an unconventional substrate material which obstructs the scalability and commercialization of TE devices based on the QDSL structure.

Despite the ~19% lattice constant mismatch between PbTe and Si, (111)-oriented epitaxial layers of PbTe have been demonstrated on Si substrates by means of IIa-fluoride buffer layers including BaF_2 [34], CaF_2 [35], stacked CaF_2/BaF_2 [36] and compositionally graded $Ca_xBa_{1-x}F_2$ layers[37]. The strains arising from both lattice and thermal mismatch of the PbTe/(IIa)-fluoride/Si system are relaxed by dislocation glide. The principal slip system in IIa-fluorite and IV-VI Pb-salt crystals is <110>{100}. Consequently, strain relaxation is easy in (111)-oriented films since the inclination of {100} glide planes to the surface yields large Schmid factors. Conversely, (001)-oriented films have a tendency to crack from thermal stress as a result of their zero Schmid factor. The orientation of the PbTe slip system is therefore fortuitous since (111) films are also favorable for their thermoelectric properties. Thus, (111)-oriented lead salt layers appear to be the desired orientation for both QDSLs as well as favorable for slip. The effect of dislocation glide during growth, processing, and device operation is currently unknown.

Dislocation glide in PbTe crystals is observed[38] at temperatures as low as 77K, yielding significant relaxation of the thermal stress in films as they are cooled to room temperature.[39] The high dislocation mobility in Pb-salt crystals and their large CTE mismatch with Si has enabled $\sim 10^6\ cm^{-2}$ dislocation density in PbTe films grown on Si mesas by thermal cycling. [39] Since thermoelectric devices consist of discrete p and n elements, etching mesas in the PbTeSe/PbTe film stack could be naturally incorporated in the device fabrication process to reduce the dislocation density in QDSL devices.

3.3. Alternative Substrates for Polycrystalline QDSL Structures

While thermal cycling can be used to reduce the defect densities in QDSL structures, the presence of dislocations is not necessarily deleterious to TE device performance. A high density of defects such as dislocations and grain boundaries may in fact improve ZT by providing scattering centers for phonons, thereby reducing the thermal conductivity of the material. However, the correlation between defect structure and TE performance has not been studied, and is one of the objectives of the proposed work. While epitaxial heterostructures have demonstrated large figures of merit, textured polycrystalline films are also expected to perform well.

Direct growth (without a fluoride buffer layer) of Pb-salts on Si results in polycrystalline film growth. [40] Furthermore, textured polycrystalline PbTe films can be grown on a variety of substrates including Si[31], SiO_2[31] and stainless steel[41] using a variety of growth techniques including sputtering and evaporation.

IV-VI semiconductors have a natural tendency to nucleate with a (001) orientation[42], therefore polycrystalline films on amorphous substrates tend to grow with a (001) texture unless a IIa-fluoride buffer layer, which nucleates with a preferential (111) orientation, is used.[34] At first, one may preclude many alternative substrates from study, since (111) is the preferred orientation for QDSLs to date. However, most of the published data for PbTe grown without a

fluoride buffer layer are for films <1μm in thickness. The work published by Boichot shows an evolution of texture with film thickness.[41] This work indicates that PbTe films evaporated onto stainless steel grow with a (001) texture for thin layers, but eventually develop a (111) preferred orientation for layers >1 μm thick, depending on deposition rate and residual background pressure. To our knowledge, the evolution of texture in polycrystalline PbTe films on Si or SiO_2 substrates has not been studied. Such films may also develop a (111) texture if grown to a large enough thickness.

The availability of large, inexpensive substrates will enable the commercialization of a scalable TE device process. Polycrystalline films on metal substrates also offer the additional benefit of providing a back contact to the TE element, simplifying device fabrication and improving reliability. Also, many metals are thermally matched to PbTe as indicated in Table 2. Of particular interest are stainless steel and aluminum substrates due to their thermal expansion-matching to lead salt materials. Si is also of interest due to its large wafer size and compatibility with production thin film process tools. Aluminum substrates may be particularly useful since CMP technologies for obtaining extremely smooth surfaces have already been developed for the hard disk industry. The same substrate technology can be used for growing polycrystalline PbTeSe/PbTe QDSL structures.

Table 2: Material parameters pertinent to PbTe/PbSeTe QDSL film growth.

Material	Crystal Structure	a_0 (Å)	α ($\times 10^{-6}$ K^{-1})
PbTe	Rock salt	6.462	19.8
BaF_2	Fluorite	6.20	19.8
CaF_2	Fluorite	5.46	19.1
Si	Diamond cubic	5.431	2.6
Stainless steel	N/A-polycrystalline	-	11-19
Aluminum and alloys	N/A-polycrystalline	-	21-25
Tin and alloys	N/A-polycrystalline	-	23
Cr-Ni-Fe superalloys	N/A-polycrystalline	-	17-19

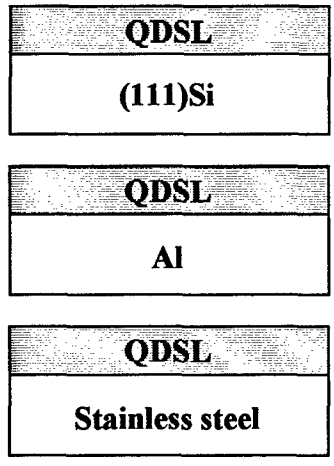

Figure 2 Alternative substrates for PbTe/PbSeTe QDSL growth.

The growth of PbTe/PbSeTe QDSL structures on alternate substrates will greatly improve the commercialization potential of thermoelectric devices based on these novel materials. We summarize the most promising substrate materials in Figure 2. Growth of PbTe on Al and stainless steel metal substrates will yield polycrystalline films which are expected to develop texture with film thickness. Metal substrates are electrically conductive, providing an electrical contact for TE devices. Perhaps most importantly however, stainless steel and

aluminum substrates are thermally matched to PbTe, potentially improving the reliability of TE devices which currently suffer from mechanical failure due to stress arising from thermal mismatch.

Si substrates can yield epitaxial or polycrystalline films depending on whether a fluoride buffer layer is used, as illustrated in Figure 3. Consequently, Si can be used as a vehicle for exploring both epitaxial and polycrystalline QDSL structures for their thermoelectric properties.

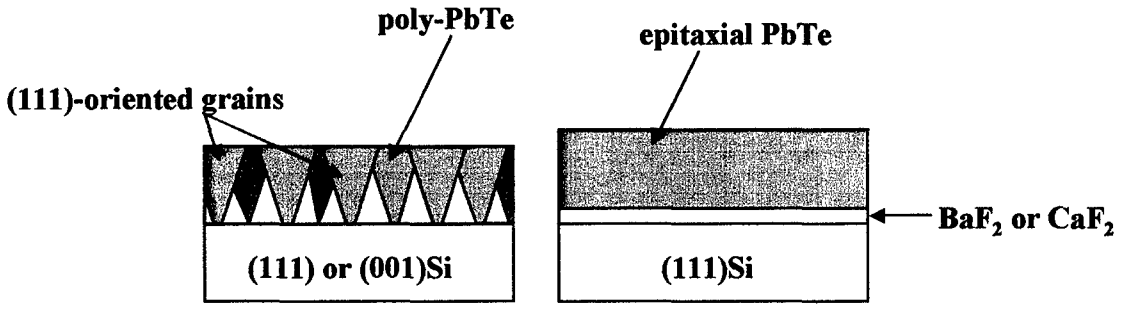

Figure 3: (a.) Epitaxial or (b.) polycrystalline PbTe film growth on Si. A fluoride buffer layer is used to initiate (111) PbTe epitaxial growth. However, since polycrystalline films may in fact improve the TE figure of merit by reduction of thermal conductivity through grain boundary scattering, direct poly-PbTe growth may be advantageous. Literature data indicates that (111) texture develops with PbTe film thickness as detailed in the text.

3.4. Thermoelectric Device Reliability

Thermoelectric devices are generally considered highly reliable since they contain no moving parts. The primary degradation mechanism for these devices is failure of their contacts as a result of thermal expansion mismatch. [45] As already mentioned, growth of QDSL device structures on thermally matched metal substrates may provide improved reliability by minimizing thermal stress and eliminating the need for a back metallization, thus reducing processing complexity. Indeed, the thermal expansion and geometry of the packaging material must also be engineered to minimize mechanical stresses during high temperature device operation.

In the case of nanostructured thermoelectrics, a second possible degradation mechanism is interdiffusion of the structure during high temperature operation. The anticipated operating temperature of devices based on the PbTeSe/PbTe QDSL structure will range between 450 and 650K. The maximum operating temperature corresponds to 55% of the melting point of PbTe (T_m=1197 K). However, high ZT structures based on nanostructured thermoelectrics will need to be studied for morphological stability within the TE element as well as within the contact areas.

3.5. Alternative QDSL Growth Techniques

Lead salt films are traditionally prepared by molecular beam epitaxy (MBE), an inherently low throughput process as compared to other techniques such as chemical vapor deposition (CVD). Currently, the growth procedure in Ted Harman's group requires ~50 hrs of film growth to yield the ~100 μm thick structure required for a thermoelectric device. While this is a reasonable method for growing test structures for material development, the scalability of

QDSL devices will require alternate techniques for deposition of thick film stacks at high growth rate and increased wafer capacity.

An alternative technique for growth of epitaxial PbTe is metal organic chemical vapor deposition (MOCVD). Surprisingly, MOCVD has been largely neglected for growth of PbTe as indicated by the lack of publications in the literature. Despite this, extremely high growth rates (>1 μm/min) of PbTe on BaF_2 substrates utilizing tetramethyllead (TMPb) and dimethyltellerium (DMTe) metalorganic sources have been achieved, yielding unintentionally doped p-type films with a hole concentration of 9×10^{18} cm^{-3} and room temperature mobilities of 480 $cm^2/V\cdot s$.[25] Earlier reports have also shown that the doping of the film can be adjusted by varying the TMPb/DMTe ratio. Using this approach, a 16 μm thick PbTe film on BaF_2 was grown at >0.5 μm/min yielding an n-type layer with a carrier concentration of 4.3×10^{16} cm^{-2} and mobility of 22,460 $cm^2/V\cdot s$ at 77K.[27] The growth rates of these high-quality films represent a ~15× improvement over the currently employed MBE technique.

Other high growth rate techniques such as plasma-enhanced chemical vapor deposition (PECVD) or sputtering also provoke the question of whether polycrystalline or amorphous films can be beneficial for high ZT structures. Theoretical calculations indicate that the figure of merit of a material can be improved if the mean free path of a phonon is greater than that of the majority charge carrier.[28] The thermal conductivity of such materials can be engineered by incorporating phonon scattering centers in the form of grain boundaries. This effect has already been demonstrated in bulk polycrystalline Ge_xSi_{1-x} alloys where the figure of merit increases markedly with decreasing grain size.[29] Hydrogenated polymorphous films, consisting of microcrystalline particles embedded in an amorphous matrix are also expected to perform well as thermoelectrics as these materials exhibit improved electronic transport compared to amorphous films while providing phonon scattering centers owing to the heterogeneity of the structure.[30]

Magnetron sputtering can be used to create textured polycrystalline films of PbTe on Si and SiO_2 substrates.[31] Polycrystalline films may provide improved ZT performance, particularly if they are textured with a preferred (111) orientation. Film texture is dependent on the substrate and growth initiation technique as are discussed in the following two sections.

4. Statement of Work

A successful program will lead to paths that allow commercial quantities of thin film thermoelectric materials to be fabricated for Navy applications. Energy harvesting using thermoelectrics in submarines, for example, could simultaneously absorb heat and produce additional power for submarine systems. Below, we outline the first steps we will take in this program to accomplish that goal.

Development of high performance lead-salt QDSL TE devices requires an analysis of the evolution of microstructure as a function of growth parameters and a correlation of the material characteristics with the thermoelectric figure of merit. Our goal is to develop a QDSL structure with a figure of merit of ≥4 at 550 K, allowing for a maximum power conversion efficiency of 55%. Furthermore, feasible TE devices will make use of alternative substrates using growth techniques that enable high throughput growth of material while preserving the microstructure yielding optimal TE device performance. TE elements will need to be characterized for potential reliability issues.

With these goals in mind, we propose a fundamental study to determine the processing-structure-performance relationship of lead-salt QDSL structures. Initial growth experiments, including work with alternative substrates will be carried out at Lincoln Laboratory using Ted

Harmon's MBE reactor. Material characterization including TEM, triple axis x-ray analysis and atomic force microscopy (AFM) will be carried out at MIT while thermoelectric measurements will be carried out at Lincoln Laboratory. Initial experiments may be carried out on easily accessible BaF_2 substrates with the goal of optimizing the baseline QDSL process. By correlating microstructure to TE performance, the aim of this part of the program will be to maximize ZT, with a goal of increasing ZT beyond 4. Once the structure-properties relationship of the QDSL structure is understood and a baseline growth process has been established, alternate substrate materials will be explored.

For the case of Si substrates, we propose that PbTe growth initiation will be performed initially without a fluoride initiation layer for study of epitaxial polycrystalline QDSL structures. If (111) texture does develop, the formation of high ZT QDSL on (111) texture polycrystals would be a scientific and practical breakthrough. The relief of multi-layer thermal stress will be studied, although thermal mismatch stress between PbTe and (111)Si are not anticipated owing to the high room temperature dislocation mobility and high Schmid factors of <111>-oriented PbTe films.

Concurrently, polycrystalline QDSL structures will also be grown on stainless steel and aluminum hard-disk substrates. We will undertake a fundamental study detailing the evolution of texture of these films and characterize their thermoelectric properties using Ted Harmon's test setup at Lincoln Laboratory. These experiments will allow us to develop a processing-structure-performance relationship for polycrystalline QDSL structures and ascertain their applicability for high performance TE devices.

Thermoelectric devices will be fabricated at Lincoln Laboratory with regular communication with the Fitzgerald group at MIT. As device-related problems are identified, appropriate activities can be transferred to MIT campus as expertise and facilities-related needs arise. A priority to device development efforts will be to identify and mitigate device-related parasitics such as contact resistance which reduce the figure of merit of the thermoelectric device. Reliability of optimized lead salt TE devices will be tested by thermal cycling and structural assessment. TEM will be the primary tool in correlating thermal cycling with structural changes, and hot-stage TEM analysis of nanostructure stability may be employed if ex-situ analysis is not sufficient to determine cause-and-effect in a reliability problem.

Another important aspect of QDSL thermoelectric device development is the assessment of alternative deposition techniques for high throughput growth of lead-salt films. One highly promising approach is MOCVD which is capable of increasing the growth rate of PbTe and PbSe films by an order of magnitude relative to the currently employed MBE technique. The MOCVD reactor in Eugene Fitzgerald's research group is a potential candidate for exploring growth of lead-salt films; however the system is currently configured for growth of III-V semiconductor and will require reconfiguration to include lead-salt MO sources. Exploration of MOCVD as an alternate growth technique is possible in the future after the device performance of the optimized QDSL structures has been characterized.

5. Preliminary Experimental Research Results

Our research group at MIT campus began a collaborative effort with MIT LL in this seed program. Our objective was to learn about the materials systems, devices, and determine future directions with an emphasis on scalability. However, the start of the collaboration also allowed us to begin testing some of the future directions we recommend in this final report and in the proposal. Specifically, one of our conclusions was the need for close correlation between QDSL

structure and thermoelectric properties. To that end, establishing structural techniques like TEM as a potential technique for investigating the superlattices was of prime importance. Although limited TEM data of lead salt structures has been reported (and quoted in this final report), the lack of TEM data in this field combined with the relative soft nature of the lead salt materials cast doubt as to whether good information could be gleaned from ground and milled TEM samples.

To initially test the usefulness of the technique, we acquired lead salt superlattices from the MIT LL group. These samples were archival samples, as our intent was to observe what microstructure the materials possessed in general, and to see if we could notice the coarsest differences in structures that had very different thermoelectric properties. The details of the acquired samples are listed below:

Sample 310

Epitaxial Layer Structure

2.28 nm	PbSe0.98Te0.02:Bi2Te3	1.00E+19	452 period	Total thickness
15.3 nm	PbTe:Bi2Te3	1.00E+19	QDSL	7960 nm
250 nm	PbTe:Bi2Te3	1.00E+19	Buffer #2	
0.8 to 1.5 nm	Te	undoped	Buffer #1	
1 mm	BaF2	Insulating	Substrate	

Sample 313

Epitaxial Layer Structure

2.1 nm	PbSe0.98Te0.02:Bi2Te3	3.07E+19	periods = 408	Total thickness
14.3 nm	PbTe:Bi2Te3	3.07E+19	QDSL	6950 nm
250 nm	PbTe:Bi2Te3	3.07E+19	Buffer #2	
0.8 to 1.5 nm	Te	undoped	Buffer #1	
1 mm	BaF2	Insulating	Substrate	

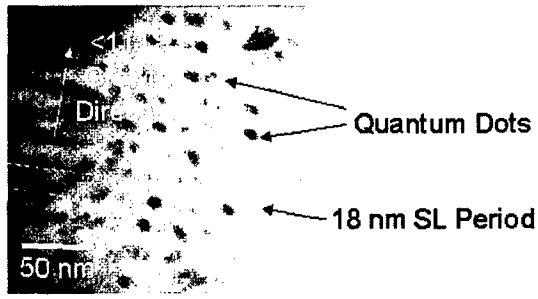

Figure 4: TEM cross-section of sample 310 (ZT=1.5). Quantum dots are seen, and the period agrees with the intended growth targets

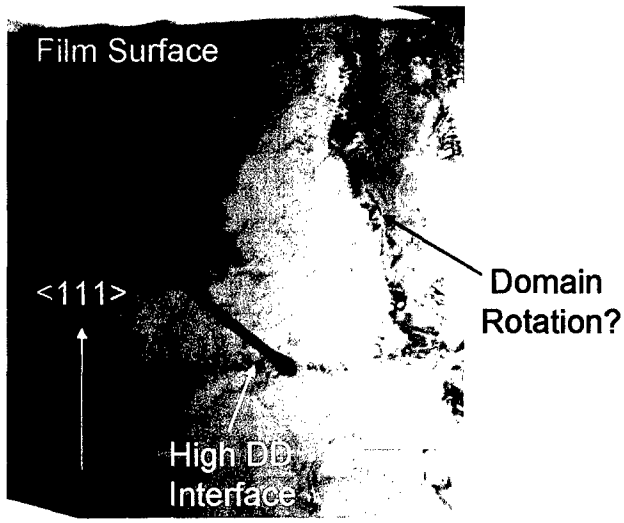

Figure 5: TEM cross-section of sample 310 at lower magnification, imaging crystalline defects in the superlattice structure

Sample 313 shows a relatively low ZT (0.54 and 0.39, respectively), and thus the sample set is a good comparison for sample 310, which showed a relatively high ZT of 1.5. Samples were prepared and milled in a somewhat standard fashion, except the milling times were increased and damage was minimized. Fig.4 is a TEM cross-section of sample 310. Note the approximately 18nm period as indicated on the figure, which is approximately equal to the intended period in the structure. Also note that the diffraction condition used in this micrograph enhances the observation of the quantum dots and minimizes the contributions from other crystallographic changes like defects. Fig. 5 is a cross-section of the same sample imaged at a lower magnification and also set to image crystalline defects. One observation is that all superlattice structures have a plethora of threading dislocations, and therefore these defects do not preclude the material from possessing a ZT>1. We also observe boundaries which define contrast between two regions in the sample, suggesting that the boundary is a low-angle grain boundary. In terms of unintended defects in Fig. 5, there appears to me a misfitted layer in the middle of the structure. This layer created a high density of dislocations in a plane parallel to the growth plane. The features suggest an unintended jump in composition at that particular place in the growth. The implications for such a single jump in lattice mismatch are currently unknown. However, we can correlate that Fig. 6, a cross-section of sample 313 at lower magnification, and many more misfitted planes are observed in this cross-section as there are many more planes of highly concentrated misfit dislocations. Higher magnification of this structure has yet to reveal the intended quantum dot superlattice in this structure. A preliminary conclusion is that the quantum dot structure unintentionally led to highly mismatched layers in this structure. Either the quantum dots were too large, resulting in coalescence and massive dislocation nucleation, or only planar layers were achieved instead of dots, leading to layers with high mismatched interfaces but no quantum dot formation.

We conclude that TEM is now a critical tool for correlating structure and thermoelectric properties in QDSL materials, confirming one of our main directions proposed for the new program. We have shown that TEM sample preparation can lead to data extraction without the introduction of confusing artifacts. This preliminary work reveals that quantum dot formation as a function of growth parameters must be studied in detail, followed by the effects of other aspects of the microstructure, like dislocations and low-angle grain boundaries. The current structures increase our optimism of depositing high ZT material on alternative substrates, and also suggest that further materials engineering of these heterostructures can be expected to increase ZT values.

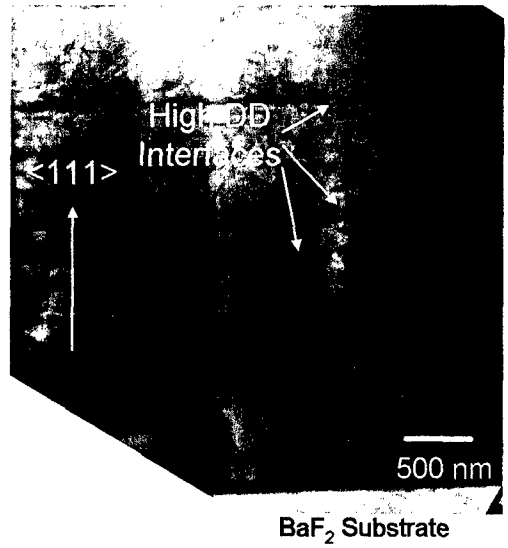

Figure 6: TEM cross-section of sample 313, revealing lack of quantum dots and a plethora of high-mismatched layers throughout the structure

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