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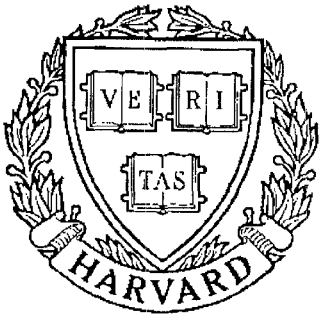


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# Analog VLSI Implementations of Auditory Wavelet Transforms Using Switched-Capacitor Circuits

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# Analog VLSI Implementations of Auditory Wavelet Transforms Using Switched-Capacitor Circuits

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**Abstract**

A general scheme for the VLSI implementation of auditory wavelet transforms is proposed using switched-capacitor (SC) circuits. SC circuits are well suited for this application since the dilation constant across different scales of the transform can be precisely implemented and controlled by both capacitor ratios and the clock frequency. The hardware implementations are made possible by several new circuit designs. Specifically, extremely area-efficient designs are presented to implement very large time-constant filters such as those used to process speech and other acoustic signals. The designs employ a new charge differencing technique to reduce significantly the capacitance spread ratios needed in the filter banks. Also, a new sum-gain amplifier (SGA-SI) is designed which permits several inputs to be sampled with the same phase. The proposed circuits have been fabricated using a $2\mu m$ CMOS double-poly process. Preliminary data and performance measures of the circuits are very encouraging and are presented. Two possible architectures for implementing the wavelet transform are discussed and compared: parallel and cascade filter banks. Responses of both filter banks are simulated using SWITCAP-II. Finally, we shall also briefly discuss the utility, from an implementation point of view, of decomposing the transfer functions of the filter banks into rational form using a recently-developed *wavelet system* (WS) technique.

## 1 Introduction

Wavelet transformations have found a wide range of applications in the processing of signals such as speech and images [1]. In biological systems such as the auditory and visual nervous systems,

affine wavelet transforms serve as excellent models of the operations leading to the generation of robust and perceptually accurate representations of the input signals[2]. However, a principal obstacle to the wider utilization of these and other nonorthogonal wavelet based algorithms is the heavy computational cost of the wavelet transform stage. Consequently, hardware implementations have been an attractive option to achieve real-time performance. For instance, a number of attempts at hardware implementations of the cochlear filter bank have employed analog designs using subthreshold operational transconductance amplifiers to construct a cascade of second-order filter stages [3, 4, 5]. Although successful in many respects, these designs suffer from the effects of parasitic capacitances and nonuniformity of the fabrication process, and thus require post-fabrication tuning to compensate for these effects. To alleviate some of the difficulties associated with such analog designs, we consider a different approach which employs a bank of switched-capacitor filters (SCF's) [6, 7]. SCF's in general have extremely precise and reliable response characteristics that would obviate the need for any post-fabrication tuning.

A key feature of using SC circuits for implementing wavelet transforms is that dilations of a given filter may be easily and very precisely controlled. Two distinct mechanisms exist for implementing dilations via SC circuits. Given a filter $G(s)$, and its dilated version $G(as)$, the direct approach of SC circuit implementation permits control of the dilation constant $a$, to within 0.1% error, since $a$ depends only on the ratios of certain capacitors and not their absolute values. A second, and perhaps more interesting method of controlling $a$, in a SC circuit implementation involves controlling the various clock frequencies of the circuits. This second approach implementing dilations is discussed further in Section 5. Such accuracy is in general unachievable using conventional analog designs. The circuits described here are very area-efficient, compensated for non-ideal effects, and are free from the effects of parasitic capacitances.

Several difficulties arise in designing switched-capacitor filters to implement wavelet transforms of acoustic signals. The most serious is the need for a frequency range which is broad and stretches to relatively low frequencies. Conventional switched-capacitor circuit designs[8, 9] require a capacitance spread ratio of approximately $1/(\Omega_0 T)$, where $\Omega_0$ is the pole frequency of the linear section or the second order filter (also known as a biquad), and $T$ is the sampling period. Thus, for a filter processing low acoustic frequencies, this ratio becomes very large, hence requiring a large silicon area. Another problem with existing SCF's is that area efficient designs are achieved by signal

attenuation, rendering them vulnerable to op-amp's non-ideal effects such as input offset voltage and finite DC gain[10].

In order to overcome these difficulties, new system architectures and SC circuit designs are presented that would facilitate the VLSI implementation of arbitrary wavelet transforms as parallel or cascade filter banks. In order to illustrate the design concepts, a specific implementation of a 32-channel wavelet transform is carried out. The filter bank mimics the transformations observed in the cochlea of the inner ear which are discussed in detail in [11]. In the following section, we discuss two overall system design considerations: (1) the specification of the filter shapes, and (2) the architecture of the system, specifically, the advantages and disadvantages of parallel *versus* cascade implementations of the filter bank. In Section 3, we discuss in detail the design of the new SC circuits needed to implement the parallel filter bank. Examples of such circuits are a new very large time-constant (VLT) switched-capacitor circuit employing gain and offset compensation (GOC) and charge differencing (CD) techniques [12], and a sum-gain amplifier (SGA-SI) which permits inputs to be sampled with the same phase to eliminate the need for sample-and-hold circuitry at the output of each individual filter (or filter section). The performance of IC fabricated versions of these circuits is also discussed briefly. In Section 4, the cascade filter bank option is considered. Finally, simulation results of the two filter bank architectures are also compared.

# 2 Overall System Design Considerations

## 2.1 Design of Filter Transfer Functions

In the design of a wavelet transform, the first issue to be tackled is that the exact shape and number of filters to be used. This in general involves application dependent considerations. For example, the desired frequency response of a single channel of the cochlear filter bank may be empirically obtained, analytically derived from mathematical models of the basilar membrane, or manually designed to suit a particular application. Often the desired frequency responses take the form of unparameterized models (e.g. empirically obtained responses) or nonrational transfer function models (e.g. responses derived from continuum mechanical models of the basilar membrane). For the purpose of circuit implementations, it is often convenient (as in the case of the parallel filter bank) to look for finite-dimensional linear filters to approximate the desired responses of the cochlear

filters. It is well-known that a linear filter has a finite-dimensional state space realization if and only if the corresponding transfer function is rational. Hence the problem is one of constructing rational approximants to the desired cochlear filter transfer functions.

Systematic methods of rational approximation have received considerable attention in the control theory and system identification literature. In Appendix A we discuss the use of the recently-proposed *wavelet system* (WS) [13, 14] technique for constructing rational approximants to the cochlear filter transfer functions. Our use of this technique in the present paper is motivated by the fact that the WS approximation method is particularly well-suited to approximate systems with transfer functions which are well-localized in time-frequency. Secondly, approximants generated by the WS methodology are suitable for hardware implementation via the SC circuits discussed in Section 3. The basic idea behind WS approximations is the decomposition of a class of transfer functions via dilations and complex translations of a single real-rational function. Specific truncations of such decompositions are then used as rational approximants. We include a brief description of the WS methodology in Appendix A. For a detailed treatment and comparison with methods based on the classical Laguerre filters, we refer to [14].

We should emphasize that while the WS formalism provides a systematic methodology for rational approximation of fairly complicated filter shapes, its use is strictly limited to the parallel filter implementations. This is because the cascade implementation of a filter bank imposes implicit restrictions on the form of the filter transfer functions which are not easily derived from their rational form. In the parallel filter bank, each channel can in principle be implemented independently of all others, and hence a rational form is immediately useful. However, in an especially efficient form of the parallel bank in which filter elements are shared across channels (see Section 3), we shall see that in general the rational form acts merely as a guide for the design process.

## 2.2 Parallel versus Cascade Architectures

In general, there are two possible architectures for implementing the wavelet transform: as a parallel or as a cascade filter bank. Each of these approaches has its advantages and disadvantages, somewhat depending on the specific application at hand. The primary advantages of the cascade filter bank is the ability to obtain high frequency resolution in the low frequency ranges with lower Q circuits. This, combined with the fact that no sum-gain amplifiers are required makes

this architecture more silicon area efficient than a comparable parallel bank. However, a host of potential disadvantages may balance out these benefits. To start with, from a circuit design viewpoint, a cascade implementation requires more robust designs since an accurate DC unity gain and low offset voltages are needed at each stage of the filter bank so as to maintain an adequate system dynamic range. The other obviously undesirable feature of the cascade filter bank is that the failure of one filter stage will affect all succeeding filter stages. From a theoretical point of view, the cascade filters are interdependent, and hence one may not be able to design one filter without affecting many others. As such, the ability to find a rational form for the filter transfer function in a given tap is of no direct consequence, but rather is only useful indirectly, e.g., as an indicator of the needed Q's. More problematic is the fact that in implementing a wavelet transform, the dilation relationship among the different channels is difficult to maintain, resulting in inevitable implementation errors that may be significant in some applications.

The parallel filter bank offers significantly greater flexibility since its filters in general are implemented independently of each other. Thus, a rational form of the transfer function of a seed filter can be implemented directly as SCF circuits, with other filters being simple dilations of it (e.g., through SCF clock frequency shifts). It is, however, also possible to implement more efficient designs by, for instance, sharing biquad elements between adjacent channels. In this case, the biquad elements themselves need to be dilations of each other, i.e., it is essential that each filter be implemented with constant Q biquad circuits. As in the cascade case, sharing the filter elements creates inter-filter dependencies that render the rational forms of the filter transfer functions only indirectly useful as a guide for more general curve fitting procedures. We shall discuss in detail an example of such an architecture in Section 3.

# 3 Parallel Filter Bank Implementations

We focus in this section on the design of a 32-channel parallel filter bank *with shared elements*. This is a special case of the general parallel architecture which has particularly efficient silicon area utilization. Generalizing the design to the simpler, but less efficient, non-shared filter bank is straightforward. All SCF's designed to implement the filter biquads are illustrated in detail, together with simulations of their response characteristics. The circuits are generic in nature, and

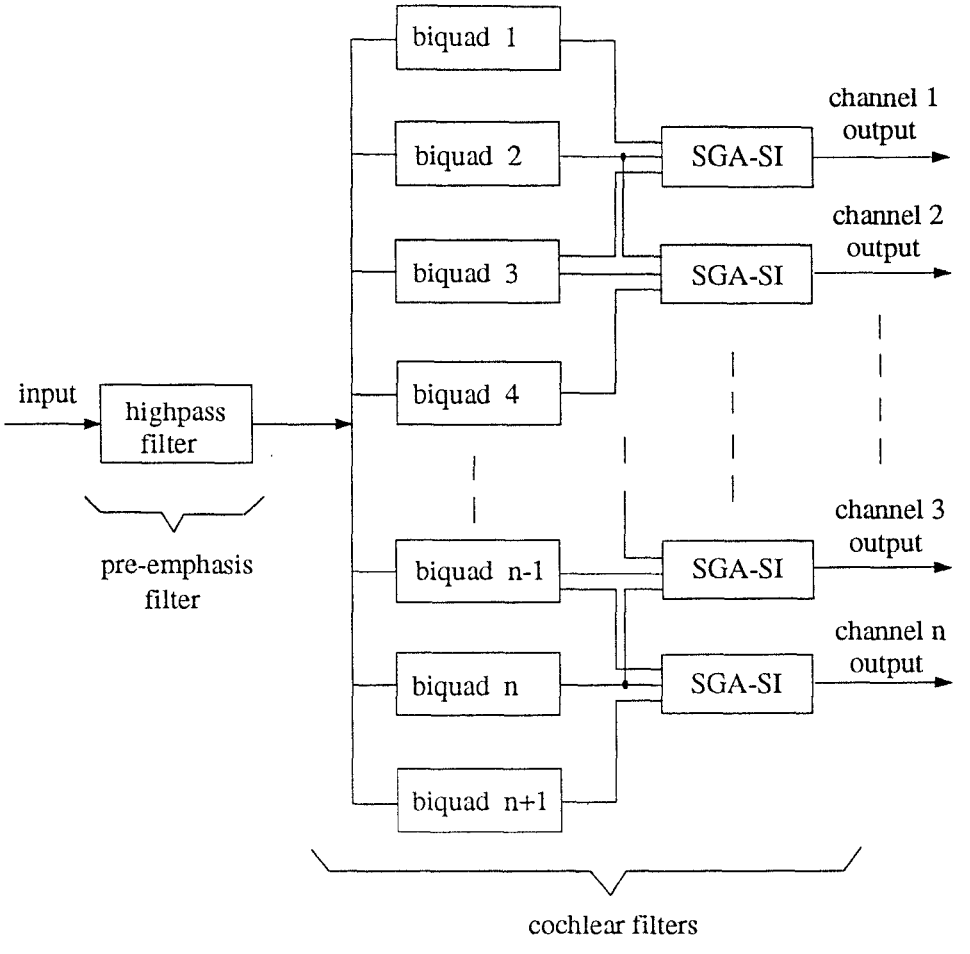


Figure 1: System topology of a wavelet transform using a shared-component parallel filter bank.

can be readily used in any arbitrary wavelet transformation.

### 3.1 System Design: Dilating-functions Filter Bank

The system topology of the shared parallel filter bank implementation is shown in Fig. 1. In this specific design example, each channel is implemented by connecting 3 adjacent lowpass biquads in parallel. The output signals from these circuits are amplified and summed together through the sum-gain amplifier (SGA) to approximate the desired filter transfer function. Note in general, the number of biquads used in each filter is purely dependent on the order of the filters desired. The biquads are designed with progressively dilated impulse responses which permits sharing them

among channels[1]. In the specific example of Fig. 1, a n-channel filter bank only requires n+2 biquads and n sum-gain amplifiers. The transfer function of the n-th biquad is chosen as

$$H_n(s) = H(a^{n-1}s) \tag{1}$$

where, $H(s)$ is a 2nd order lowpass filter in the s-domain, $a$ is a dilation constant, and $n = 1, \cdots, 34$ in this design example. Using these biquads, the transfer function of the m-th channel in the z-domain is approximated by

$$G_m(z) = \sum_{i=1}^{i=3} k_i H_{i+m-1}(z) \tag{2}$$

where, $k_i$'s are gain factors. Since the same set of $k_i$'s is used in every channel, only one sum-gain amplifier has to be designed. The rest will just be its duplicates. The output signals from biquads are available simultaneously in this system topology. Therefore, a new sum-gain amplifier (SGA-SI) which permits the inputs to be sampled in the same phase is proposed here. The new design requires no sample-and-hold circuitry to connect the outputs of a parallel bank of biquads to the input of a SGA-SI, thereby saving considerable silicon area. The pre-emphasis highpass filter is often useful in the processing of acoustic signals such as speech [15]. Since the filter is shared among many channels, the driving capability of its op-amp has to be considered carefully.

In the following subsections, we shall discuss in detail the SCF circuits that we designed in order to implement the filter bank. In the Section 3.2, we focus on the SCF's needed in the low acoustic frequency ranges, the so-called VLT integrators and biquads. New designs are formulated here in order to produce area-efficient and robust filters. For the midfrequency ranges, conventional biquads can be used as in Section 3.3. The highpass pre-emphasis filter design and the sum-gain amplifiers are presented in Sections 3.4 and 3.5, respectively. Finally, simulations of the filter bank operation using all these SCF circuits are shown in Section 3.6.

## 3.2 Circuit Design I: Area-Efficient GOC VLT Biquad

It is known that the performance of switched-capacitor circuits can be degraded by the non-ideal effects of op-amps such as offset voltages and finite DC gains. Since these effects can usually be improved simultaneously, the circuits with gain- and offset-compensation are called GOC

[1]Note that sharing of biquads need not be restricted to adjacent channels, and that more general shared-component topologies are also possible.

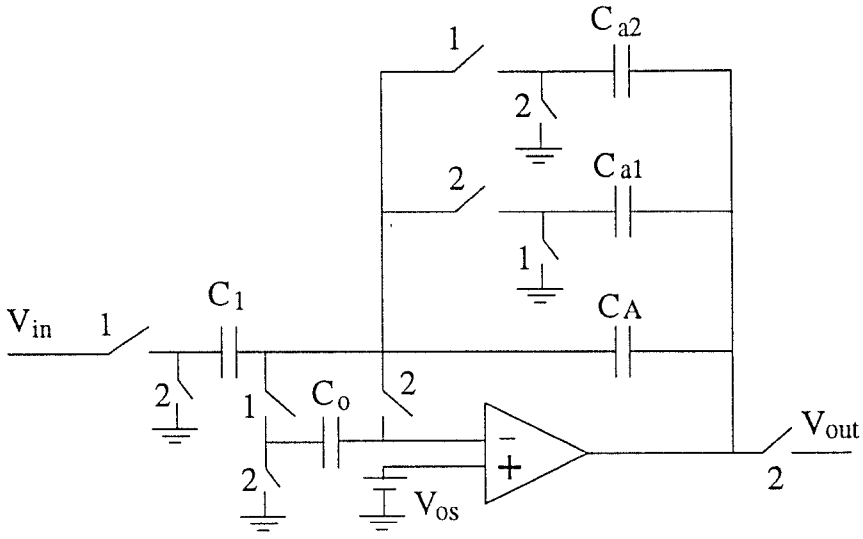


Figure 2: GOC charge differencing inverting integrator.

circuits[16, 17]. In this section, we describe new GOC area-efficient biquads which employ a technique called charge differencing[12]. These circuits are specifically designed for use in the low frequency channels where very large time-constants (VLT), and hence large capacitances and silicon areas, are typically needed in conventional designs. First, we shall describe a VLT integrator circuit, and then use it to design the larger $2^{nd}$ order (biquad) circuits.

### 3.2.1 Gain and Offset Compensated (GOC) VLT Integrator

The GOC inverting integrator, where $C_{a1} > C_{a2}$, is shown in Fig. 2. Its operational principle can be stated as follows (assume op-amp is ideal first). When switches 1 are closed, the charge $V_{in}(n)C_1$ is accumulated in the capacitors $C_A$ and $C_{a2}$. The output voltage is sampled by $C_{a1}$ simultaneously, i.e., the charge $[V_{in}(n)C_{a1}C_1]/(C_A+C_{a2})$ is transferred into $C_{a1}$. When the switches 2 are closed, a charge $V_{in}(n)C_1$ is effectively pulled back to ground from capacitors $C_A$ and $C_{a1}$. Since $C_A$ received the charge $[V_{in}(n)C_AC_1]/(C_A+C_{a2})$ in the previous phase, $C_{a1}$ has to compensate the net difference charge $[V_{in}(n)C_{a2}C_1]/(C_A+C_{a2})$ before it redistributes the charge received in the previous phase with $C_A$. The transfer function

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1(C_{a1}-C_{a2})z^{-1/2}}{(C_A+C_{a1})(C_A+C_{a2})(1-z^{-1})} \tag{3}$$

can be obtained.

The charge differencing technique is based on both the difference of capacitors and ratio of capacitors, thus the capacitance spread ratio can be made very small. Note that the difference between the capacitors $C_{a1}$ and $C_{a2}$ should not be made arbitrarily small because of sensitivity problems[12]. This integrator is stray-insensitive, glitch-free, and only one medium capacitor is needed.

Now, let the offset voltage be $V_{os}$. During the phase 2, the LHS plate of capacitor $C_o$ is connected to ground, thus the voltage $-V_{os}$ is stored in $C_o$. During the phase 1, only the RHS plate of $C_o$ is only connected to the inverting terminal of the op-amp, therefore the charge held in $C_o$ is preserved. Consequently, the LHS plate of $C_o$ acts like the virtual ground, and this can be used to improve the non-ideal effects of the op-amp. The arrangement of switching phases surrounding the capacitor $C_o$ is very important. In the above case, the virtual ground exists in the phase 1. If the switching phases surrounding the capacitor $C_o$ are interchanged, the virtual ground will appear in the phase 2 and this alters dramatically the degree of compensation. Using time domain analysis, the GOC integrator output is given by

$$\begin{aligned} V_{out}(n+\frac{1}{2}) &= -\frac{C_1(C_{a1}-C_{a2})}{(C_A+C_{a1})(C_A+C_{a2})}V_{in}(n) + V_{out}(n-\frac{1}{2}) \\ &+ [\frac{C_{a2}}{C_A+C_{a2}} + \frac{C_1(C_{a2}-C_{a1})}{(C_A+C_{a1})(C_A+C_{a2})}]V_{os}. \end{aligned} \tag{4}$$

For the non-GOC case (the junction of $C_1$ and $C_A$ is connected to the inverting terminal of the op-amp directly, and omit the capacitor $C_o$ and its associated switches), it can also be shown that the effective offset voltage is

$$(\frac{C_{a1}}{C_A+C_{a1}} + \frac{C_{a2}}{C_A+C_{a2}})V_{os}. \tag{5}$$

Comparing eqns. 4 and 5, the effective offset voltage is reduced by at least a factor of 2 in the GOC design. In the special case of $C_{a2} = 0$, the output offset voltage of the GOC VLT integrator is approximately inversely proportional to ${C_A}^2$. That is, the effective offset voltage is further reduced, and with lower circuit sensitivity[12, 18, 7, 19].

### 3.2.2 Gain and Offset Compensated VLT Biquads

With the above GOC charge differencing integrator, two types of biquads can be built (Figs. 3 and 4). Type-I biquad has a somewhat simpler design equations and is suitable in high Q applications,

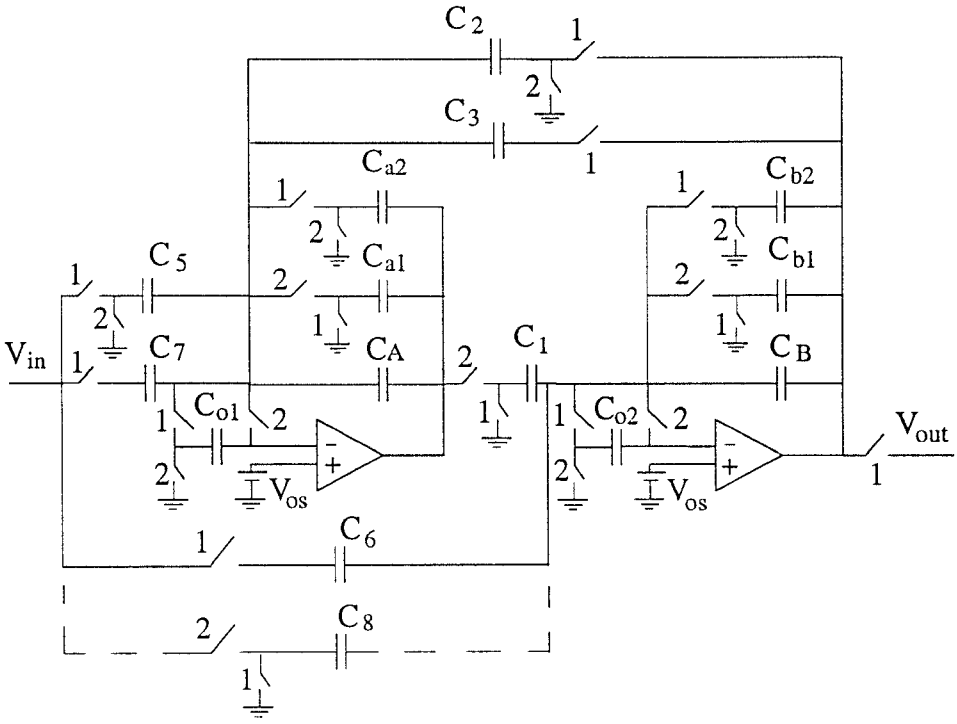


Figure 3: Type-I GOC charge differencing biquad.

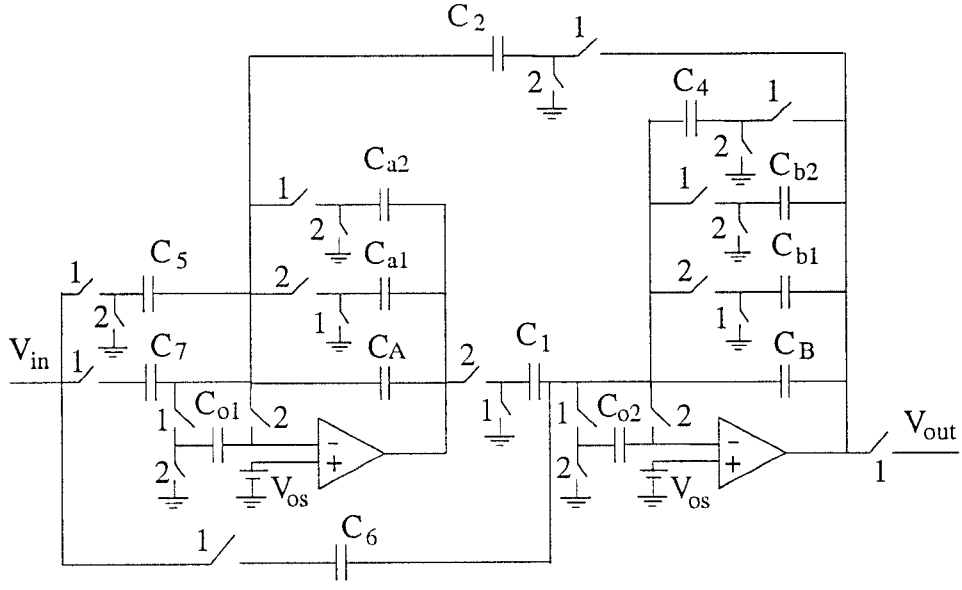


Figure 4: Type-II GOC charge differencing biquad.

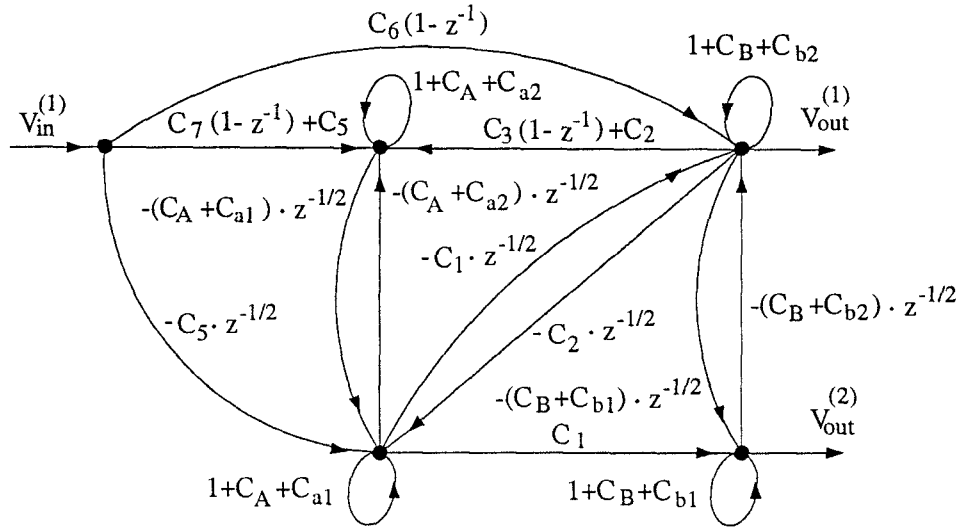


Figure 5: Signal flow graph of Type-I GOC charge differencing biquad.

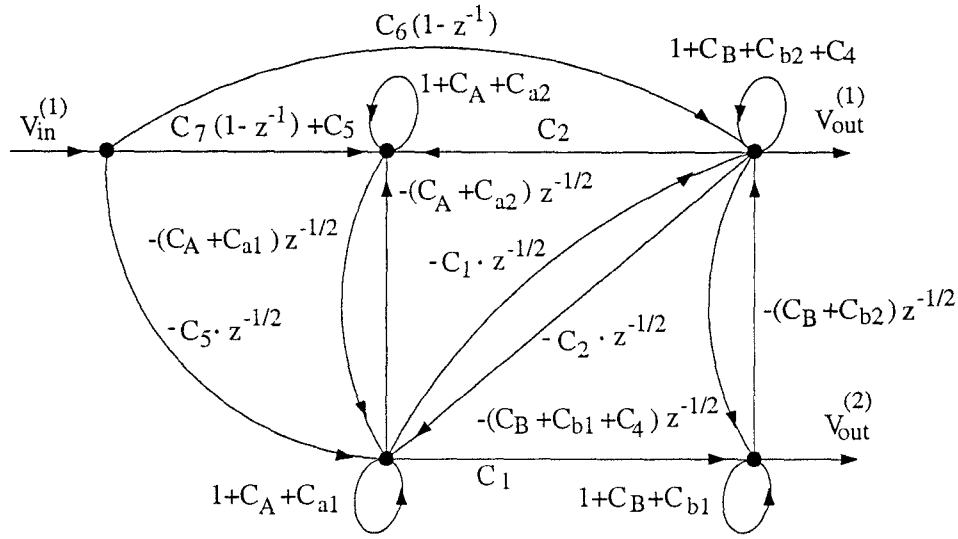


Figure 6: Signal flow graph of Type-II GOC charge differencing biquad.

while Type-II is more appropriate for low Q filters. From the signal flow graphs shown in Figs. 5 and 6 (assuming ideal op-amps and no offset voltages), and apply Mason's rule, the transfer function of biquads is given by

$$H(z) = -\frac{C_5}{C_2}\frac{\alpha_c}{\gamma_c}\frac{1-(2-\gamma_c-\eta_c)z^{-1}+(1-\eta_c)z^{-2}}{1-(2-\alpha_c-\beta_c)z^{-1}+(1-\beta_c)z^{-2}}, \tag{6}$$

where,

$$\gamma_c = \frac{C_1C_5(C_{a1}-C_{a2})(C_{b1}-C_{b2})}{C_6(C_A+C_{a1})(C_A+C_{a2})(C_B+C_{b1})} \tag{7}$$

$$\eta_c = \frac{C_1C_7(C_{b1}-C_{b2})}{C_6(C_A+C_{a2})(C_B+C_{b1})}. \tag{8}$$

For the Type-I biquad,

$$\alpha_c = \frac{C_1C_2(C_{a1}-C_{a2})(C_{b1}-C_{b2})}{(C_A+C_{a1})(C_A+C_{a2})(C_B+C_{b1})(C_B+C_{b2}+C_4)} \tag{9}$$

$$\beta_c = \frac{C_4(C_{b1}-C_{b2})}{(C_B+C_{b1})(C_B+C_{b2}+C_4)}. \tag{10}$$

For the Type-II biquad,

$$\alpha_c = \frac{C_1C_2(C_{a1}-C_{a2})(C_{b1}-C_{b2})}{(C_A+C_{a1})(C_A+C_{a2})(C_B+C_{b1})(C_B+C_{b2})} \tag{11}$$

$$\beta_c = \frac{C_1C_3(C_{b1}-C_{b2})}{(C_A+C_{a2})(C_B+C_{b1})(C_B+C_{b2})}. \tag{12}$$

Consider the following transfer function in the s-domain,

$$H_a(s) = -k\frac{1+s/(Q_1\Omega_1)+s^2/\Omega_1^2}{1+s/(Q_0\Omega_0)+s^2/\Omega_0^2}. \tag{13}$$

Defining $x_i = 2/\Omega_i T$ and performing the bilinear transformation (if necessary, the prewarp has to be done before taking the transformation), the z-domain transfer function is given by

$$H(z) = -k\frac{(x_1^2+x_1/Q_1+1)-(2x_1^2-2)z^{-1}+(x_1^2-x_1/Q_1+1)z^{-2}}{(x_0^2+x_0/Q_0+1)-(2x_0^2-2)z^{-1}+(x_0^2-x_0/Q_0+1)z^{-2}}. \tag{14}$$

Let

$$\alpha = \frac{4}{x_0^2+(x_0/Q_0)+1} \tag{15}$$

$$\beta = \frac{2x_0/Q_0}{x_0^2+(x_0/Q_0)+1} \tag{16}$$

$$\gamma = \frac{4}{x_1^2+(x_1/Q_1)+1} \tag{17}$$

$$\eta = \frac{2x_1/Q_1}{x_1^2+(x_1/Q_1)+1}, \tag{18}$$

then the transfer function becomes

$$H(z) = -k\frac{\alpha}{\gamma}\frac{1-(2-\gamma-\eta)z^{-1}+(1-\eta)z^{-2}}{1-(2-\alpha-\beta)z^{-1}+(1-\beta)z^{-2}}. \tag{19}$$

Let the capacitor values be assigned as:

$$C_1 = C_2 = C_{o1} = C_{o2} = 1 \tag{20}$$

$$C_{a2} = C_{b2} = y \geq 0 \tag{21}$$

$$C_{a1} = C_{b1} = y + \delta > 0 \tag{22}$$

$$C_A = C_B = K > 0 \tag{23}$$

where y is chosen to be smaller than 1 in the VLT applications. Comparing the coefficients of eqns. 6 and 19, the $K$ for the Type-I biquad becomes the solution of

$$K^2 + (2y+\delta)K + (y^2 + y\delta - \frac{\delta}{\sqrt{\alpha}}) = 0. \tag{24}$$

For $\Omega_0 T \ll 1$, and after some simplifications,

$$K \approx \sqrt{\delta/(\Omega_0 T)} - 1 \tag{25}$$

$$C_3 = (\beta/\alpha)[\delta/(K+1+\delta)] \approx \frac{1}{Q_0}\frac{1}{\Omega_0 T}. \tag{26}$$

If the Type-II biquad is used, $K$ satisfies the following equation

$$K^4 + (4y+2\delta)K^3 + (6y^2+6y\delta+\delta^2)K^2 + (4y^3+6y^2\delta+2y\delta^2+\frac{\beta\delta}{\alpha})K$$
$$+(y^4+2y^3\delta+y^2\delta^2+\frac{y\beta\delta+\beta\delta^2-\delta^2}{\alpha}) = 0. \tag{27}$$

In the same way, it can be seen that

$$K \approx \sqrt{\delta/(\Omega_0 T)} - 1 \tag{28}$$

$$C_4 = (\beta\delta)/[\alpha(K+1+\delta)(K+1)] \approx \frac{1}{Q_0}. \tag{29}$$

The other capacitor values can now be computed as

$$C_5 = k \tag{30}$$

$$C_6 = \frac{C_5\delta^2}{\gamma(K+y+\delta)^2(K+y)} \tag{31}$$

$$C_7 = \frac{\eta C_6(K+y)(K+y+\delta)}{\delta}. \tag{32}$$

Note that if a zero outside the unit circle is required, then one more capacitor $C_8$ can be added as shown in the Fig. 3, and the design equations can also be obtained in the same way. It is apparent from the above analysis that the use of the charge differencing technique can reduce the required capacitor spread ratios to approximately $\sqrt{\delta/(\Omega_0 T)}$. This means that a comparable saving in the silicon areas can be achieved with these VLT circuits. For instance, in a lowpass filter design (later used in the implementation of the parallel filter bank with $Q_0 = 0.707$, $\Omega_0 = 2\pi \cdot 200Hz$, and $f_s = 125kHz$, and assume unity DC gain, $y = 1$, $\delta = 0.5$), the capacitor values which Type-II biquad needed are

$$C_A = C_B = 5.444 \tag{33}$$

$$C_4 = 1.572 \tag{34}$$

$$C_5 = 1. \tag{35}$$

In the other word, the total capacitance is 22.46 in such an implementation. If compared with the Type-II GOC conventional biquad shown in Fig. 11 which requires the total capacitance of 204.66, only about 11% of capacitance area is needed. Even compared to the most area-efficient biquads so far, more than 25% capacitance area can be saved easily[12]. SWITCAP-II[2] simulations of both the ideal case (op-amp's gain=$\infty$) and the non-ideal case (op-amp's gain=1000) are shown in Fig. 7. The results illustrate the robustness of these area-efficient VLT biquads, in that minimal changes in the transfer functions occur that are due to the non-ideal effects of the op-amps.

A LPN filter has also been fabricated and tested. Both the frequency and time responses are shown in the Figs. 8 and 9 respectively. The notch frequency deviation from its designed value is less than 1% without any post-fabrication tuning. This can be improved further if larger unit capacitor is used instead of the $0.2pF$ used here. A single tone with swept frequency was used to measure the entire frequency responses of the fabricated-IC chip. The responses match very closely with designs already discussed. Furthermore, the DC unity gain error is found to be within 1%.

### 3.3 Circuit Design II: Conventional GOC Biquads

As we mentioned earlier, conventional switched-capacitor circuits have a capacitance spread of approximately $1/(\Omega_0 T)$. This ratio is not problematic in the high frequency channels. Due to its

[2]SWITCAP-II is a simulation program of switched-capacitor circuits.

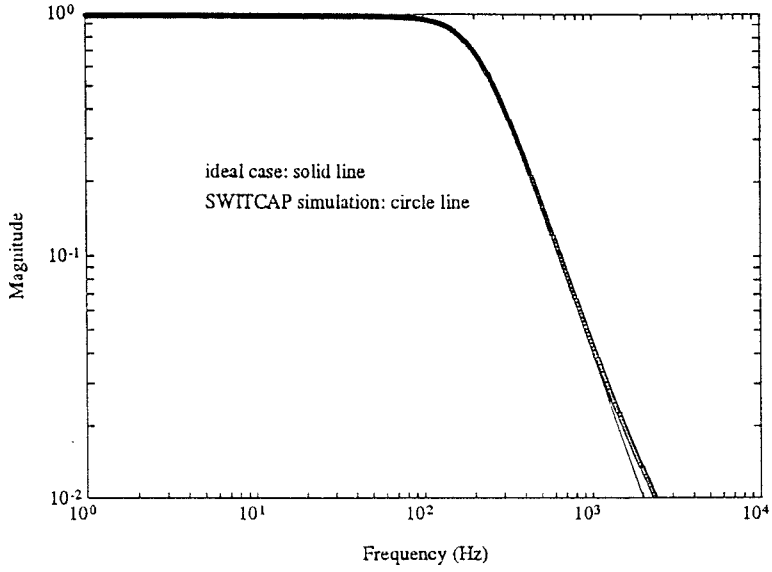


Figure 7: Simulation result of the area-efficient biquad.

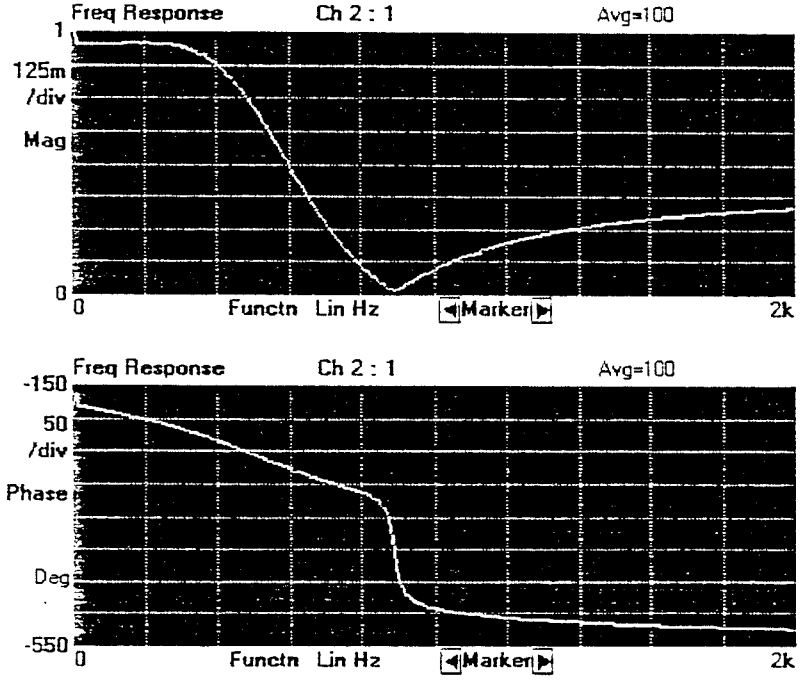


Figure 8: Measured frequency response of the integrated circuit Type-II area-efficient LPN biquad.

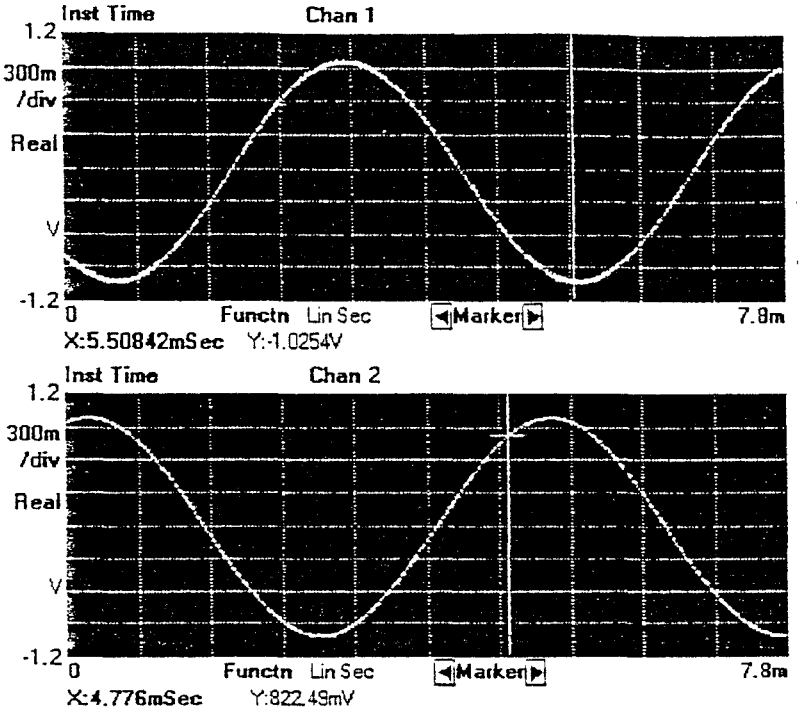


Figure 9: Measured time domain response of the integrated circuit Type-II area-efficient LPN biquad (input frequency: $200Hz$, input signal: lower trace, and output signal: upper trace).

simpler structure than VLT biquads, these kind of circuits are preferred in the applications of high frequency cochlear channels. The conventional Type-I and Type-II GOC biquads are designed and shown in in Figs. 10 and 11, respectively. The transfer function is given by

$$H(z) = -\frac{C_5}{C_2}\frac{\alpha_c}{\gamma_c}\frac{1-(2-\gamma_c-\eta_c)z^{-1}+(1-\eta_c)z^{-2}}{1-(2-\alpha_c-\beta_c)z^{-1}+(1-\beta_c)z^{-2}} \tag{36}$$

where,

$$\gamma_c = \frac{C_1C_5}{C_AC_6} \tag{37}$$

$$\eta_c = \frac{C_1C_7}{C_AC_6}. \tag{38}$$

For the Type-I biquad,

$$\alpha_c = \frac{C_1C_2}{C_AC_B} \tag{39}$$

$$\beta_c = \frac{C_1C_3}{C_AC_B}. \tag{40}$$

For the Type-II biquad,

$$\alpha_c = \frac{C_1C_2}{C_AC_B+C_AC_4} \tag{41}$$

$$\beta_c = \frac{C_AC_4}{C_AC_B+C_AC_4}. \tag{42}$$

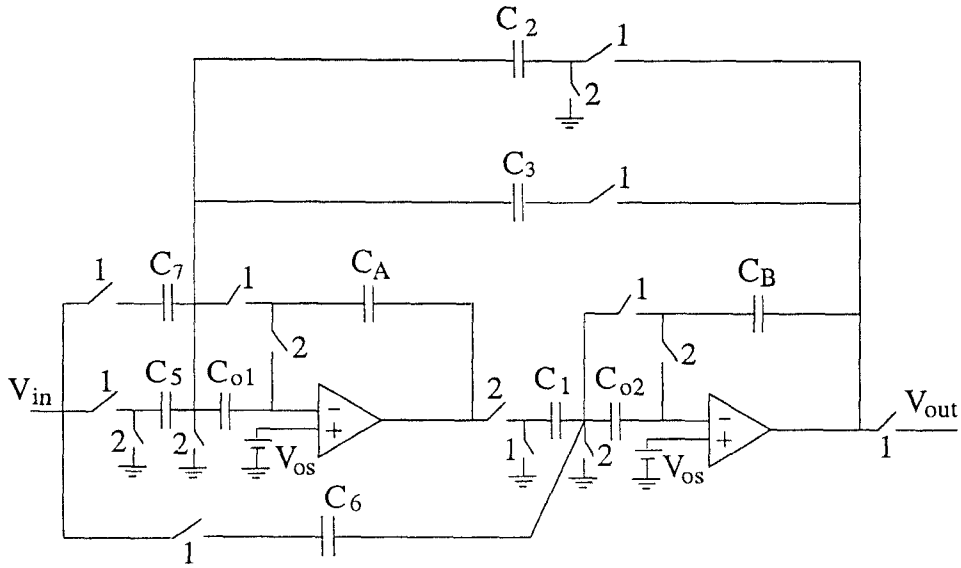


Figure 10: Type-I GOC conventional biquad.

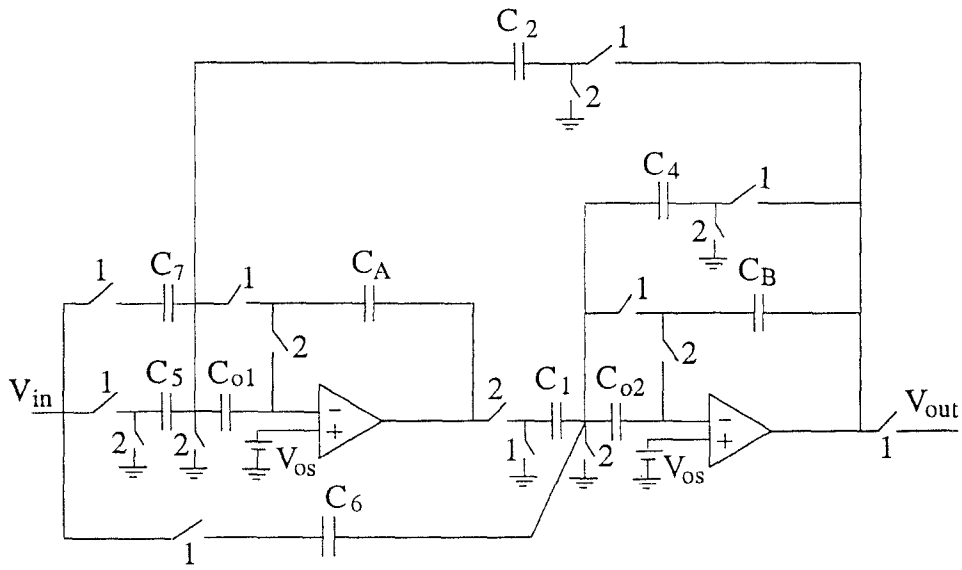


Figure 11: Type-II GOC conventional biquad.

Following the same derivation as that described in Section 3.2, and assigning $C_1 = C_2 = C_{o1} = C_{o2} = 1$, we obtain the following capacitor values for the Type-I biquad

$$C_A = C_B = \sqrt{\frac{1}{\alpha}} \approx \frac{1}{\Omega_0 T} \tag{43}$$

$$C_3 = \frac{\beta}{\alpha} \approx \frac{1}{Q_0}\frac{1}{\Omega_0 T}. \tag{44}$$

In the same way, if the Type-II biquad is used, the capacitor values are

$$C_A = C_B = \sqrt{\frac{1-\beta}{\alpha}} \approx \frac{1}{\Omega_0 T} \tag{45}$$

$$C_4 = \frac{\beta}{\alpha C_A} \approx \frac{1}{Q_0}. \tag{46}$$

Where,

$$C_5 = k \tag{47}$$

$$C_6 = \frac{C_5}{\gamma C_A} \tag{48}$$

$$C_7 = \eta C_6 C_A. \tag{49}$$

As mentioned earlier, the analysis illustrates that Type-I biquad is suitable for high Q realizations, while Type-II biquads are more appropriate for low Q filters. As an example, using a Type-II biquad to implement the earlier described lowpass filter but with a higher pole frequency ($\Omega_0 = 2\pi \cdot 6.4kHz$), we can obtain the simulation results of Fig. 12.

### 3.4 Circuit Design III: Highpass Filter

The function of the highpass filter is to pre-emphasize the input signal, and hence the corner frequency of this filter should be high enough to cover the entire signal bandwidth of interest. A pole frequency of $\Omega_0 = 2\pi \cdot 12.8kHz$ is used here. The GOC first order highpass filter which employs the offset storage capacitor is designed and shown in Fig. 13. The transfer function is given by

$$H(z) = \frac{-C_1(1-z^{-1})}{(C_A + C_2) - C_A z^{-1}}. \tag{50}$$

Considering the highpass transfer function in the s-domain where $k$ is the gain factor and $\Omega_0$ is the pole frequency,

$$H(s) = -k\frac{s/\Omega_0}{1 + s/\Omega_0}. \tag{51}$$

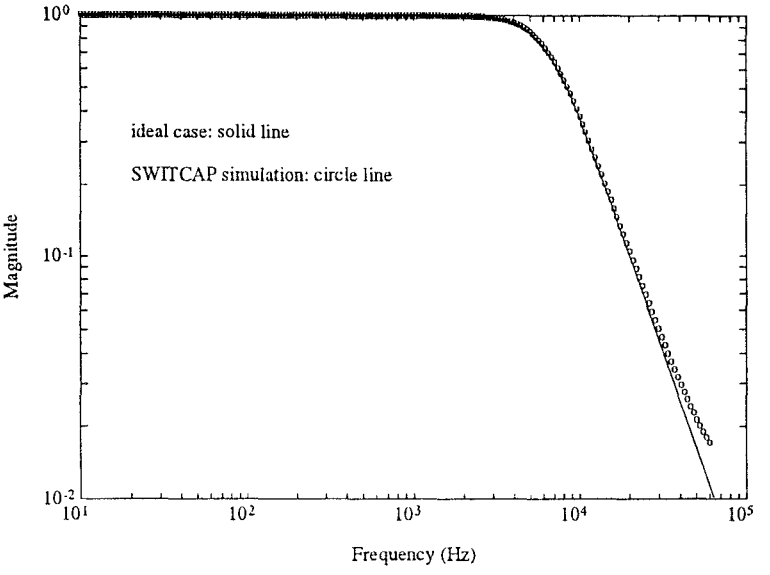


Figure 12: Simulation result of the conventional GOC biquad.

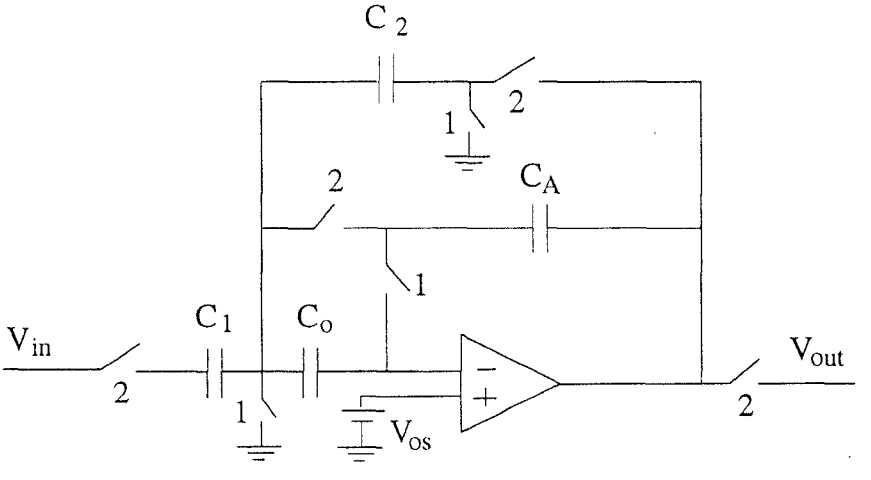


Figure 13: Conventional GOC first order highpass filter.

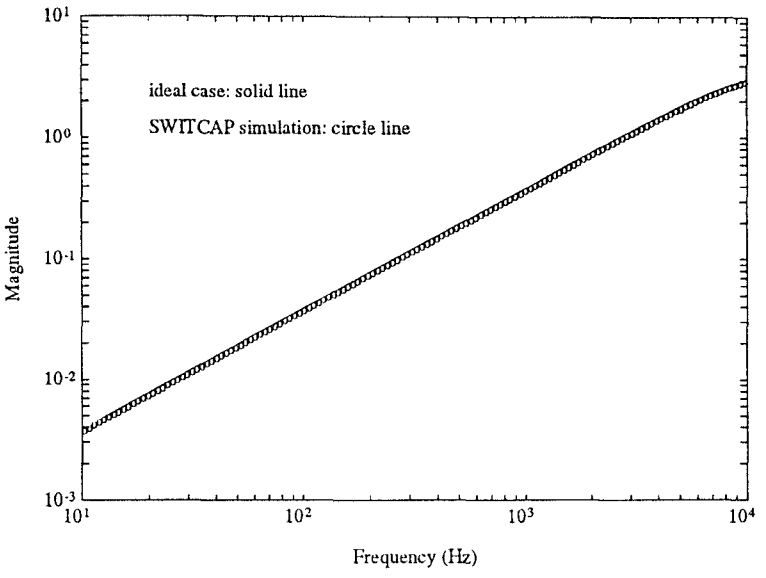


Figure 14: Simulation result of the conventional GOC first order highpass filter.

Performing the bilinear transformation, the transfer function in the z-domain is obtained as

$$H(z) = -k\frac{(1-z^{-1})x_0}{(1+x_0)-(x_0-1)z^{-1}}, \tag{52}$$

where, $x_0 = 2/(\Omega_0 T)$, and $T$ is the sampling period. Comparing the coefficients of eqns. 50 and 52, and choosing the capacitor $C_2$ as the unit capacitor, we obtain

$$C_A = \frac{x_0 - 1}{2} \tag{53}$$

$$C_1 = k\frac{x_0}{2}. \tag{54}$$

Because of the relative insensitivity of the circuit responses, $C_o$ and $C_m$ can also be chosen as the unit capacitors. SWITCAP-II simulations of the pre-emphasis filter with gain $k = 5$ are in Fig. 14. The unity gain is around the 2.8 $kHz$ in this case.

## 3.5 Circuit Design IV: Sum-Gain Amplifier

In a parallel filter bank in which biquads elements are shared among neighboring channels, it is essential to have a sum-gain amplifier which can sum the output signals of several biquads simultaneously. A new sum-gain amplifier (SGA-SI) which permits the inputs to be sampled with the same phase is proposed in Fig. 15. The operational principle of this SGA-SI can be stated as follows: Consider input $V_{in1}$ first, while $V_{in2}$ and $V_{in3}$ are set to zero. In phase 2, $C_{a2}$ is discharged.

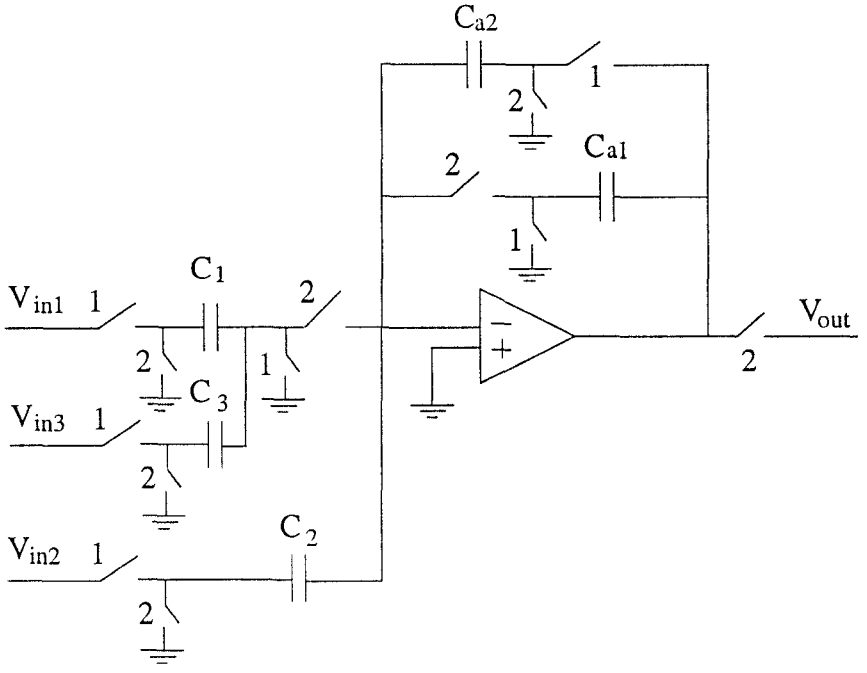


Figure 15: Sum-gain amplifier with same input phases (SGA-SI).

But, since in phase 1, its left plate is connected to the inverting terminal of the op-amp only, no charge can be injected into $C_{a2}$, and the output remains at ground level. This helps $C_{a1}$ to discharge in this phase. During phase 2, $C_1$, $C_{a1}$, and the op-amp constitute a non-inverting gain stage, which gives $V_{out}(n+1/2) = (C_1/C_{a1})V_{in1}(n)$. The input $V_{in3}$ can be analyzed in similar fashion. Next, set $V_{in1}$ and $V_{in3}$ to zero. In phase 2, $C_{a2}$ is discharged as in the previous case. But in phase 1, $C_2$, $C_{a2}$, and the op-amp constitute an inverting amplifier. Hence, $V_{out}(n) = -(C_2/C_{a2})V_{in2}(n)$. This voltage is stored in $C_{a1}$, and is to be held constant during the next phase 2. The final output is the superposition of all the 3 inputs. The transfer function is given by

$$V_{out}(z) = [\frac{C_1}{C_{a1}}V_{in1}(z) - \frac{C_2}{C_{a2}}V_{in2}(z) + \frac{C_3}{C_{a1}}V_{in3}(z)]z^{-1/2}. \tag{55}$$

Hence, the output is the sum of $V_{in1}$, $V_{in3}$, and $-V_{in2}$, all scaled by appropriate gain factors. The gain factors can be individually controlled through $C_1$, $C_2$, and $C_3$. Moreover, this sum-gain amplifier can be designed to include any number of inputs for either addition or subtraction. One important factor which needs to be considered carefully is the slew rate because the op-amp is reset in one phase. Taking this design for example, the clock period is $8\mu s$, and voltage level is 5. The slew rate is about 1.25 $V/\mu s$ and this can be easily achieved. Even so, the circuit should not be

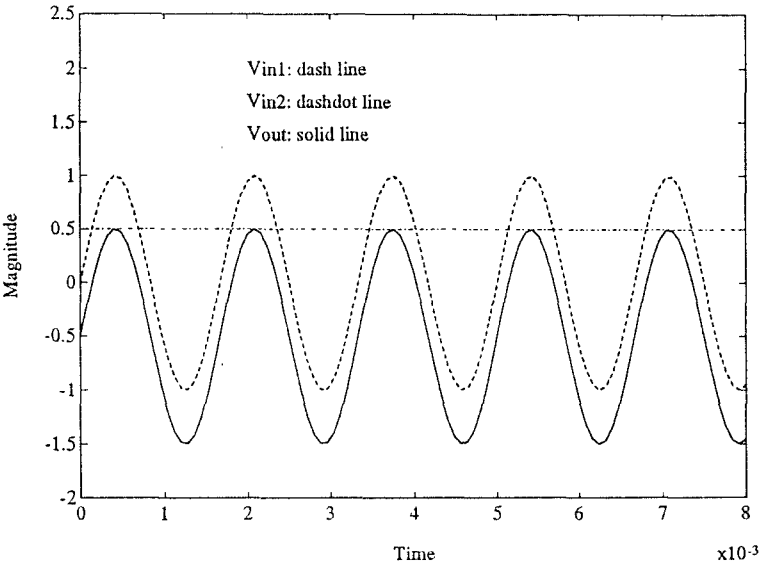


Figure 16: Simulation result of sum-gain amplifier with same input phases (SGA-SI).

used in high frequency applications because of the low effective op-amp gain. Simulation results with input $V_{in3} = 0$ are shown in Fig. 16. In addition, The responses of the fabricated sum-gain amplifiers are shown in Figs. 17 and 18. The testing results completely satisfy our designs.

## 3.6 Simulation Results of the Parallel Filter Bank

Combining all individual circuits described above, we have implemented the *shared* parallel filter bank shown earlier in Fig. 1. To demonstrate the validity of these designs, the parallel filter bank (including the pre-emphasis highpass filter) was simulated by SWITCAP-II and the responses are shown for 4 channels in Fig. 19. Note that the channel transfer functions are strictly translated relative to each other with a constant Q. The change in the relative amplitudes of the outputs is due to the pre-emphasis filter. This architecture saves at least 25% of the silicon area needed in the non-sharing topology.

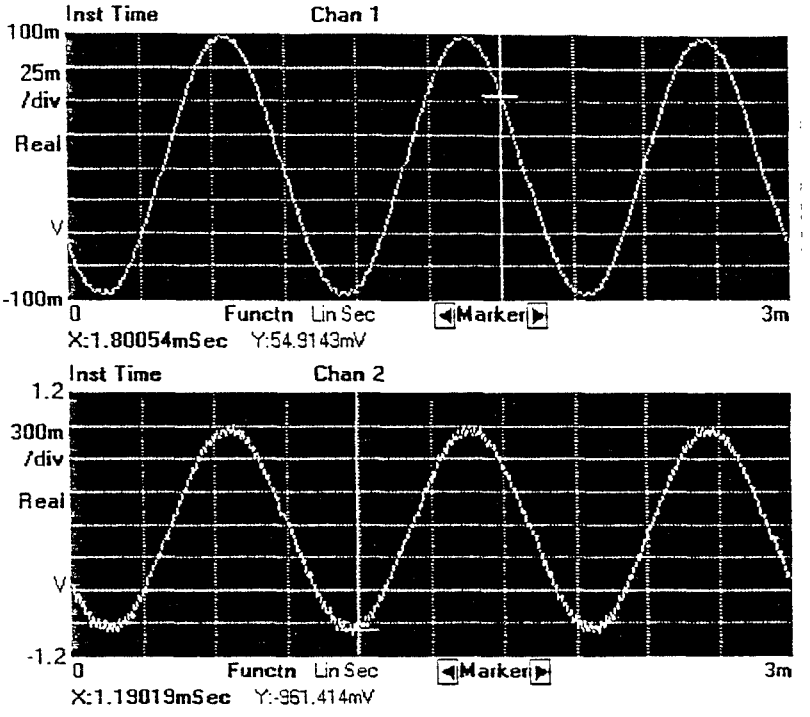


Figure 17: Measured response of non-inverting channel of the integrated circuit SGA-SI with input frequency $= 1kHz$ and gain $= 9.475$ (input signal: upper trace, and output signal: lower trace).

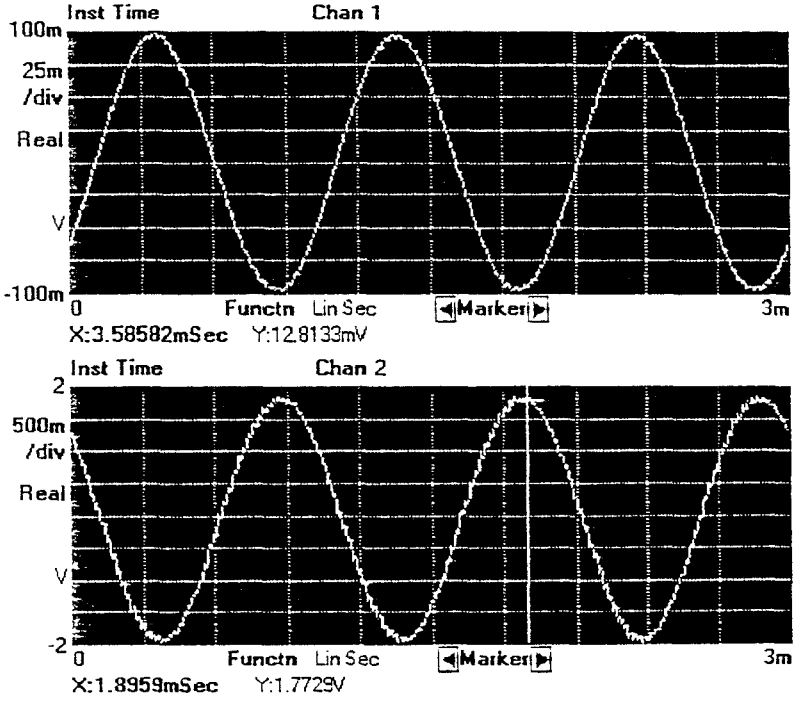


Figure 18: Measured response of inverting channel response of the integrated circuit SGA-SI with input frequency $= 1kHz$ and gain $= 18.8$ (input signal: upper trace, and output signal: lower trace).

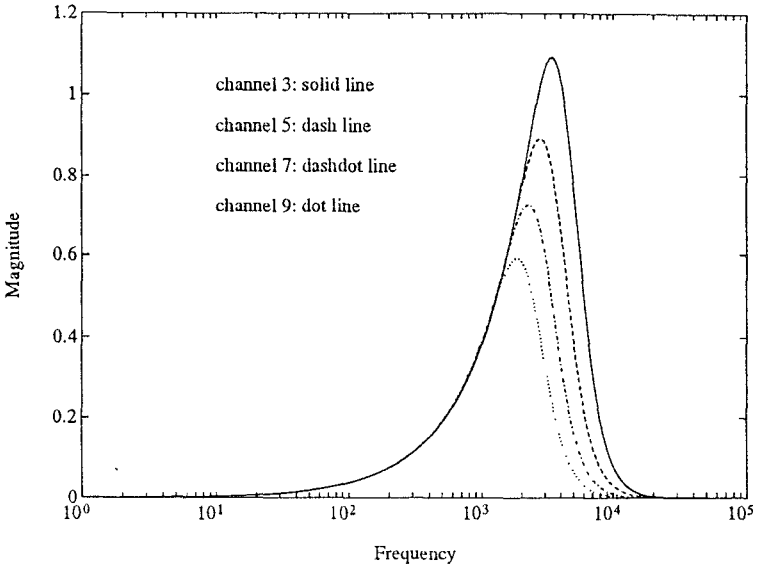


Figure 19: Simulation result of auditory wavelet transform using a parallel filter bank (including the pre-emphasis filter).

# 4 Cascade Filter Bank

## 4.1 System Design

The other possible architecture to implement wavelet transforms is the cascade filter bank. The system topology of a cascade filter bank implementation is shown in Fig. 20. This filter bank is made up of a first order pre-emphasis highpass filter followed by several cascaded second order lowpass filters. The advantage of this architecture is that it requires a smaller silicon area when compared to the parallel architecture. If the pole frequencies of the lowpass filter stages are chosen in an exponential relationship, the lowpass filters become dilated with respect to one another. But, the dilation relationship among the channels is no longer exactly preserved when the lowpass filters are cascaded. For instance, it can be expected that the last channel in the chain should have sharper roll-offs than earlier channels. However, this may not be a problem in some applications since most of the deviations from a strict wavelet transform occur in the stop-bands of the filter transfer functions. Finally, another important feature of the cascade architecture is that high gains can be achieved by combining modest gains of many stages like the pseudoresonance[3]. Thus, only small Q factors are needed compared to the values typically needed in the parallel filter bank.

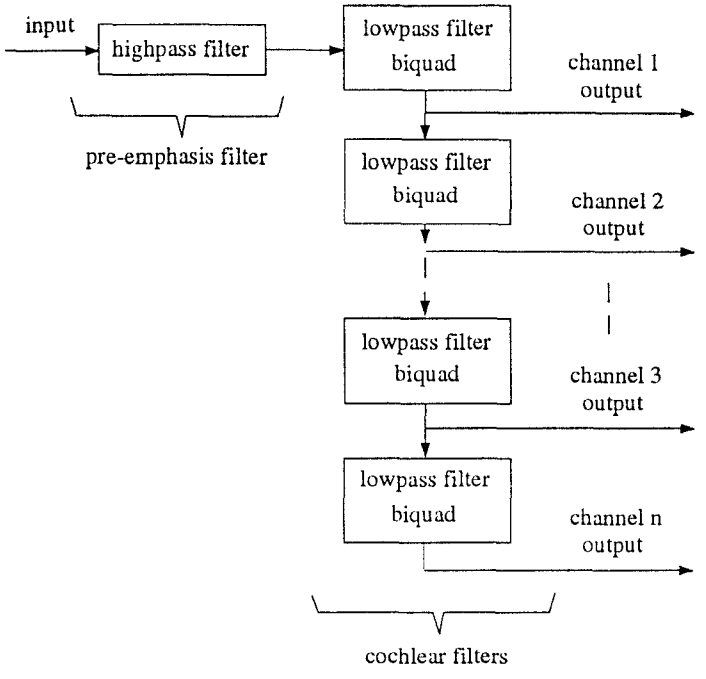


Figure 20: System topology of auditory wavelet transform using a cascade filter bank.

## 4.2 Circuit Design

The circuits designed in Section 3 can also be used to implement the cascade filter bank by modifying the sign of the transfer function. Since only lowpass filters are used, the forward path capacitors $C_6$ and $C_7$ of Figs. 3, 4, 10, and 11 can be omitted. To obtain positive transfer function, we take advantage of certain SC circuit properties. For instance, it is well known that by changing the switching phases associated with a capacitor, either positive or negative resistor can be simulated. Thus, interchanging the switching phases of LHS plate of capacitor $C_5$, the positive transfer function can be obtained easily without requiring an additional op-amp, and the design equations are the same as those described in Section 3. One of the important considerations when cascading SC circuits together is the ripple delay since it may make it necessary to use high speed op-amps. In our biquad circuit design, the outputs of op-amps are sampled in the different phases, hence no ripple delay will propagate across the biquads such that no fast op-amps are required. By using the same biquad circuit topology with a different clocking scheme (interchanging switches '1' and '2') as the adjacent lowpass filters, one can cascade these filters together easily.

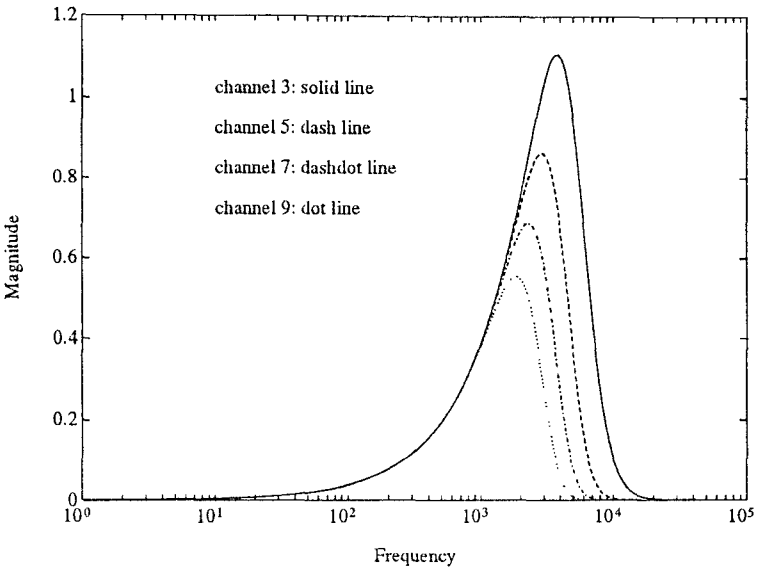


Figure 21: Simulation result of auditory wavelet transform using a cascade filter bank (including the pre-emphasis filter).

### 4.3 Simulation Results of the Cascade Filter Bank

To demonstrate the validity of such a system design, and in order to compare it to the parallel architecture, the cascade filter bank including the pre-emphasis highpass filter was simulated by SWITCAP-II. The responses are shown in Fig. 21. Note that, the capacitance spread ratio of less than 10 is needed in this example confirming the circuit area-efficiency which we mentioned earlier. Since no sum-gain amplifiers are required here, the entire silicon area is only about 64% of the parallel filter bank.

## 5 Conclusions and Discussions

We have discussed in this paper the hardware design and realization of auditory wavelet transforms using switched-capacitor circuits. The desired transfer functions could either be systematically decomposed into rational transfer functions by the recently-developed *wavelet system* (WS) technique[13, 14] as shown in Appendix A, or approximated by the proposed dilating-functions filter bank to allow for circuit-sharing. It was also noted in Appendix A that in some cases the dilations inherent WS approximations may also be exploited in the design of shared-component

parallel filter banks. In this paper, lowpass transfer functions were chosen as the desired filter shapes so as to facilitate the comparison between two possible architectures for implementing the wavelet transforms, namely as a parallel or as a cascade filter bank.

The hardware implementation was made possible by several new circuit designs. Specifically, extremely area-efficient designs were developed to implement very large time-constant filters. The designs employ a new charge differencing (CD) technique to reduce significantly the capacitance spread ratios needed in the filter banks. Also, a new sum-gain amplifier (SGA-SI) was designed which permits the inputs to be sampled with the same phase, thus facilitating the sharing of several biquads among neighboring channels in the parallel filter bank. All the proposed circuits have been successfully fabricated and tested. The precise responses of the IC chips show the advantages of the new designs. Furthermore, the circuit design equations were fully derived in order that arbitrary future designs of the wavelet transform filters can be implemented.

Based on these circuits, both the parallel and cascade filter banks were simulated (Figs. 19 and 21). The simulation illustrated that both filter banks have similar robust response characteristics. One difference between these two is that faster decaying slopes seen in the stop-bands of the cascade realization. Since the signal is very small in the stop band, this difference is generally not critical in computing the wavelet transform. The cascade filters also needed smaller silicon areas and lower Q circuits when compared to the parallel realization. However, more robust circuits with low DC offset voltages must be used in the cascade realization.

The other key feature of SC circuits from the viewpoint of wavelet transforms is that by changing the sampling frequency by a factor of $a$, all zero and pole frequencies can be changed by the same factor. Hence, by connecting several *similar* chips together, each with a *different* sampling frequency, more filter channels can be readily implemented. Besides, the dilation constant $a$ can be very precisely controlled by either the clock frequency or the capacitor ratios in SC circuits. For instance, in the many applications of the wavelet transforms where the dilation constant $a$ is equal to 2, simple frequency division digital circuits can be used.

## Acknowledgements

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# Appendix

## A Rational Wavelet System Approximations

Rational WS approximations to transfer functions are based on wavelet decompositions of the Hardy space $\mathrm{H}^2(\Pi^+)$, where $\Pi^+$is the open right-half complex plane $\Re e\ s > 0$, in the case where the analyzing wavelet is chosen to be rational.

**Definition A.1** *A function $F$ which is analytic in $\Pi^+$is said to belong to the class $\mathrm{H}^2(\Pi^+)$ if,*

$$\sup_{x>0} \int_{\mathbb{R}} |F(x+iy)|^2\, dy < \infty. \tag{56}$$

By the Paley-Wiener theorem, $\mathrm{H}^2(\Pi^+)$ is the image of $\mathrm{L}^2(0,\infty)$ under the Laplace transform. Hence $\mathrm{H}^2(\Pi^+)$ contains transfer functions of causal, linear, time-invariant systems with square-integrable impulse responses. We adopt the following notation.

$\mathrm{RH}^2(\Pi^+)$ : Real-rational functions in $\mathrm{H}^2(\Pi^+)$.

$\mathrm{H}^2_{\mathbb{R}}(\Pi^+)$ : Functions in $\mathrm{H}^2(\Pi^+)$ which are Laplace transforms of *real-valued* functions in $\mathrm{L}^2(0,\infty)$ .

WS approximations arise from specific truncations of decompositions of $\mathrm{H}^2(\Pi^+)$, via dilations and complex translations of a single real-rational analyzing wavelet. The set of dilations and translations of the real-rational analyzing wavelet are chosen so as to form a *frame* for $\mathrm{H}^2(\Pi^+)$. Frames are generalizations of orthonormal bases, which are defined below. We refer to [20] for further details.

**Definition A.2** *Given a Hilbert space $\mathcal{H}$, a sequence of vectors $\{h_n\}_n \subset \mathcal{H}$, is called a frame if there exist constants $A > 0$ and $B < \infty$ such that*

$$A\|f\|^2 \le \sum_n |\, < f, h_n > |^2 \le B\|f\|^2, \tag{57}$$

*for every $f \in \mathcal{H}$. $A$ and $B$ are called the frame bounds.*

Given a frame $\{h_n\}_n$ for a Hilbert space $\mathcal{H}$, any $f \in \mathcal{H}$, may be represented as

$$f = \sum_n \langle f, h_n \rangle\, S^{-1} h_n = \sum_n \left\langle f, S^{-1} h_n \right\rangle h_n,$$

where the *frame operator* $S$, is defined by $Sf = \sum_n \langle f, h_n \rangle\, h_n$. The following theorem summarizes the main ideas behind WS approximations.

**Theorem A.1** ([14]) *Let $\Psi \in \mathrm{RH}^2(\Pi^+)$ be an admissible analyzing wavelet, and let $a_0 > 0$, $b_0$ be such that $(\Psi, a_0, b_0)$ generates an affine frame for $\mathrm{H}^2(\Pi^+)$, i.e. $\{\Psi_{m,n}\} = \left\{a_0^{m/2}\Psi(a_0^m \cdot - inb_0)\right\}$ is a frame for $\mathrm{H}^2(\Pi^+)$. Let $S$ be the associate frame operator. Then, any $F$ in $\mathrm{H}^2_{\mathbb{R}}(\Pi^+)$ may be represented as,*

$$F = \sum_m \sum_{n=0}^{\infty} F^{m,n}, \tag{58}$$

*where, each $F^{m,n}$ $(\in \mathrm{RH}^2(\Pi^+))$ is defined by,*

$$\begin{aligned} F^{m,n} &= \left\langle F, S^{-1}\Psi_{m,n}\right\rangle \Psi_{m,n} + \overline{\langle F, S^{-1}\Psi_{m,n}\rangle}\Psi_{m,-n}, \ m \in \mathbb{Z}, \quad n \in \mathbb{Z}^+ \setminus \{0\} \\ F^{m,0} &= \left\langle F, S^{-1}\Psi_{m,0}\right\rangle \Psi_{m,0} \qquad m \in \mathbb{Z}. \qquad \blacksquare \end{aligned} \tag{59}$$

The right hand side of eqn. 58, is referred to as a *wavelet system (WS) decomposition* of $F \in \mathrm{H}^2(\Pi^+)$. WS decompositions represent systems with transfer functions in $\mathrm{H}^2(\Pi^+)$, via infinite sums of time-frequency localized finite-dimensional systems. Finite truncations of WS decompositions give real-rational approximations to transfer functions in $\mathrm{H}^2(\Pi^+)$. WS techniques are particularly well-suited to rational approximation of transfer functions which are well-localized in time-frequency (as is the case for the cochlear filters). Such finite truncations are also useful as 'linear-in-parameters' black-box models for system identification (c.f. [14]).

## A.1 WS Approximation of Cochlear Filters

For approximation of the cochlear filter, we use the following $\mathrm{H}^2(\Pi^+)$ analyzing wavelet $\Psi$;

$$\Psi(s) = \frac{1}{(s+\gamma)^2 + \xi^2}, \qquad \gamma, \xi > 0,$$

with $\gamma = 5.0, \xi = 1.0$. It is easily verified that $\Psi(s)$ is in $\mathrm{H}^2(\Pi^+)$ and furthermore $\Psi$ is an admissible analyzing wavelet i.e. $\int_{\mathbb{R}} \Psi(x+iy)dy = 0 \quad$ for $x \geq 0$. It can also be shown (see [14]) that for $a_0 = 2$, $0 < b_0 < 16.5$, $(\Psi, a_0, b_0)$, generates an affine frame for $\mathrm{H}^2(\Pi^+)$.

The specific cochlear filter shape of interest here (see Figure 23) takes the form of an unparameterized model derived from a combination of empirical data and mathematical modeling of the basilar membrane [21]. Figure 22 is a plot of the magnitudes of the wavelet expansion coefficients $\{\langle F, S^{-1}\Psi_{m,n}\rangle\}$ (using $a_0 = 2$, $b_0 = 1.0375$). A key feature of the decomposition shown in Figure

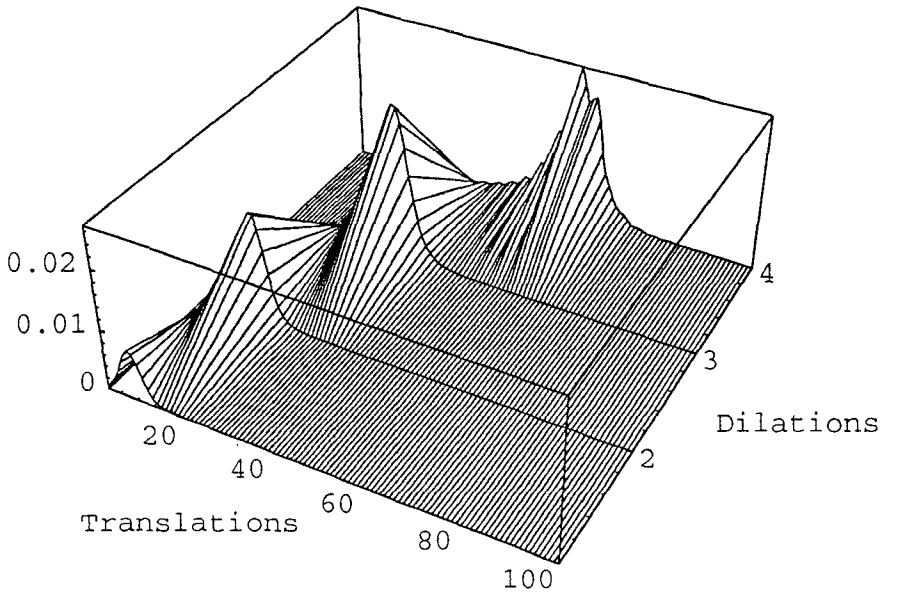


Figure 22: Magnitude of wavelet expansion coefficients for the cochlear filter transfer function.

22 is the large number of zero or negligible coefficients. This compactness of representation, which arises due to the time-frequency localization of both the cochlear filter transfer function and the analyzing functions (wavelets), allows us to construct low-order rational approximants to the cochlear filters. Figure 23 shows the frequency response magnitude of a 12th order rational approximation to the cochlear filter response in which three terms ($\{(m,n)\} = \{(0,7),(1,14),(2,28)\}$) from the WS decomposition are used. Note that the sharp cutoff on the high-frequency side is well-approximated by this scheme.

**Remark:** In general WS decompositions serve to provide rational approximations which are useful for independent implementation of filters in a parallel filter bank. However, the fact that the individual terms of a WS decomposition involve dilations of the analyzing wavelet may in some cases also be exploited in designing the economical shared-component form of a parallel filter bank implementation described in Section 3.

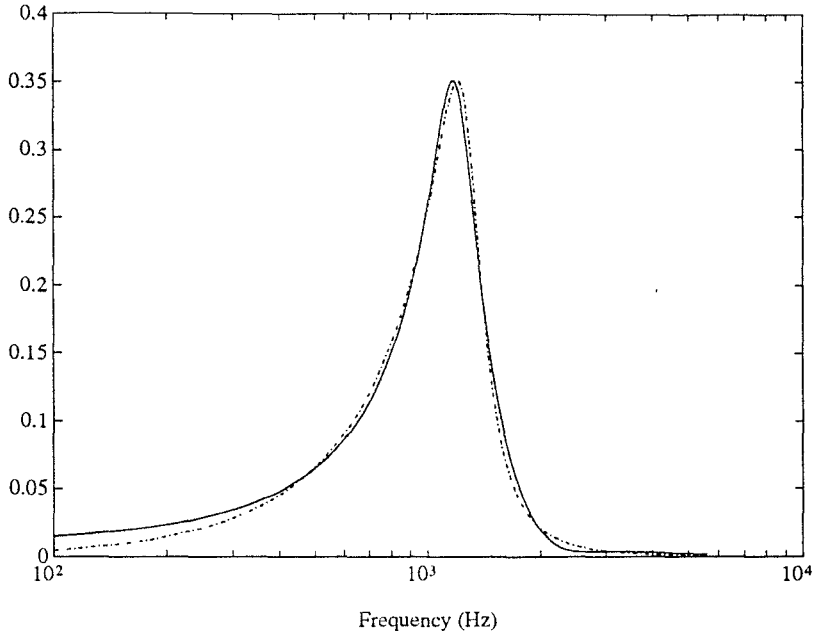


Figure 23: Frequncy response magnitude of: (i) unparameterized cochlear filter model (dashed line), (ii) 12th-order rational WS approximation to cochlear filter (solid line).

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