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MIXED-SIGNAL ELECTRONICS TECHNOLOGY FOR SPACE (MSETS)

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Final Report

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14. ABSTRACT

The purpose of this project was to stimulate development of analog and mixed-signal electronics technology for communications and other missions in space. The research was conducted by the Center for Design of Analog-Digital Integrated Circuits (CDADIC), headquarters at Washington State University, and consisting of multiple universities and industry partners. To accomplish the research goal, 14 projects were conducted by CDADIC university-industry teams in six major technical areas, as identified by AFRL. These six areas included: 1) System circuit modeling for VLSI circuit implementation; 2) Standard cell/topologies in radiation-hardened SOI; 3) Reconfigurable mixed-signal electronics; 4) System-on-a-chip; 5) Predictive radiation effects models; and 6) Ultra low-power technologies. Research covered all six areas.

15. SUBJECT TERMS Mixed Signal Electronics, Radiation Effects Modeling, Radiation Hardness, Radio Frequency Devices, RF Devices, Silicon on Insulator, SOI, Space Vehicles

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EXECUTIVE SUMMARY

Included in this final report are 14 projects resulting from research conducted during a three-year period (August 16, 2002 – August 15, 2005) of the "Mixed-Signal Electronics Technology for Space" project, funded by the Air Force Research Laboratory (AFRL), Space Vehicles Directorate. Project titles and university-industry research teams are provided for all 14 projects in Table. 1.

The research was conducted by the Center for Design of Analog-Digital Integrated Circuits (CDADIC), which was established in 1989 as part of the National Science Foundation's Industry-University Cooperative Research Center (I/UCRC) program. Research teams included university (faculty and students) and industry partners who are members of CDADIC. The university investigators were from CDADIC's six affiliated universities: Washington State University, University of Washington, Oregon State University, State University of New York at Stony Brook, Arizona State University, and the University of Tennessee. (Note: Arizona State University and the University of Tennessee joined CDADIC during the third year of this project and only conducted work in the final year of the program.) The industry partners were The Boeing Company and Honeywell, who have a rich history in circuit design for microelectronic systems for space applications. Each of these industry and university partners was engaged in this project as subcontractors.

The overall objective of this research was to develop analog and mixed-signal electronics technology for communication systems and other applications in space. To achieve this objective, CDADIC university-industry teams investigated six major research task areas that AFRL identified as being critical to meet future strategic space system applications. These six research task areas are identified in Table 2, "Statement of Work Fulfillment," along with all 14 projects as they relate to these six major task areas; all six task areas were investigated in this project.

An important element of this research activity was the emphasis placed on radiation tolerant or hardened mixed-signal circuit design. For some of the center's research faculty, it was their first exposure to the design of circuits to perform in radiation environments. Significant effort was devoted to the use of hardening-by-design techniques, while some projects utilized the Honeywell silicon-on-insulator (SOI) process technology as a first step in the design of circuits using a technology with the potential for achieving circuit hardness by process.

As stated, 14 research projects were conducted during the three-year performance period of this program. Each of these projects was selected through a proposal process in which they were evaluated by the center's Industrial Advisory Board and by AFRL representatives and guests. Final recommendations as to which proposals should be funded were made by an AFRL Selection Committee, composed of select faculty, industry members, and AFRL representatives. However, the final decision authority in the

Table 1. CDADIC/AFRL Research Projects

Project 1: **Reconfigurable RF Circuits for Low-Cost Phased-Array Systems**
Research Team*: Prof. David Allstot with Greg Kromholtz and Rod Bonebright*
Number of Years Funded: 2

Project 2: **Low Power Wireless Sensor for Space and Military Applications Communications System Specification and Simulation for Wireless Sensors**
Research Team*: Profs. David Allsot, Ward Helms, and Huaping Liu with Gary Nelson & Steve Fahley*
Number of Years Funded: 1

Project 3: **Circuit Design Techniques for Low-Voltage, Analog CMOS Integrated Circuits for Extreme Environments**
Research Team*: Prof. Benjamin Blalock with David Hogue*
Number of Years Funded: 1

Project 4: **Adaptive Regulation and Logic for Subthreshold Circuits**
Research Team*: Prof. Lawrence T. Clark with Intel*
Number of Years Funded: 1

Project 5: **SOI-CMOS Radiation Total Dose Device Models for Space Environment Applications**
Research Team*: Prof. R. Bruce Darling (University of Washington) with Fong Shi (Boeing*)
Number of Years Funded: 2

Project 6: **Radiation-Tolerant SiGe BiCMOS Smart MMICs for Space Communications**
Research Team*: Prof. Deuk Heo with Fong Shi*
Number of Years Funded: 2

Project 7: **Direct Digital Frequency Synthesizer for Reconfigurable Communication Systems**
Research Team*: Prof. George La Rue with Fong Shi*
Number of Years Funded: 3

Project 8: **SOI CMOS Continuous-Time Delta Sigma A/D Converters for Space Communication Radio Receivers**
Research Team*: Profs. Adrian Leuciuc and Alex Doboli with Bruce Ohme*
Number of Years Funded: 3

Project 9: **RF, Analog and Digital Array for Radiation-Hardened Communication Circuits**
Research Team*: Profs. Larry McMurchie and Carl Sechen with Andy Peczalski*
Number of Years Funded: 3

Project 10: **Radiation-Hard PLL Design Tolerant to Noise and Process Variations**
Research Team*: Profs. Un-Ku Moon and Karti Mayaram with Andy Peczalski*
Number of Years Funded: 3

Project 11: **Low Temperature RF Characterization and Design of MOI5 SOI CMOS Circuits and Devices**
Research Team*: Profs. Mohamed A. Osman and Deuk Heo with Andy Peczalski*
Number of Years Funded: 1

Project 12: **Reconfigurable Input/Output for Radiation Environments** (Demonstration Project)
Research Team*: Andy Peczalski (Honeywell) with Profs. Adrian Leuciuc, GaborTemes, Un-Ku Moon, Karti Mayaram, Larry McMurchie and Carl Sechen*
Number of Years Funded: 2

Project 13: **Radiation Hardening by Design for Data Converter**
Research Team*: Prof. Gabor Temes with Andy Peczalski*
Number of Years Funded: 2

Project 14: **Design of Radiation-Hard Analog/Mixed-Signal Circuits in Silicon-on-Insulator (SOI) Technology**
Research Team*: Profs. Gabor Temes and S. Subramanian with Andy Peczalski*
Number of Years Funded: 1

Table 2. Statement of Work Fulfillment

The 14 AFRL research projects conducted by CDADIC over the three-year period met requirements in all six of the AFRL research task areas. Below is a list of the six task areas and the CDADIC projects that met various tasks requirements in those focus areas.

AFRL Task Area 1: System Circuit Modeling for VLSI Circuit Implementation

Project 5: SOI-CMOS Radiation Total Dose Device Models for Space Environment Applications
Project 9: RF, Analog and Digital Array for Radiation-Hardened Communication Circuits
Project 12: Reconfigurable Input/Output for Radiation Environments (Demonstration Project)

AFRL Task Area 2: Standard Cell/Topologies in Radiation-Hardened SOI

Project 2: Low Power Wireless Sensor for Space and Military Application/Communications System Specification and Simulation for Wireless Sensors
Project 3: Circuit Design Techniques for Low-Voltage, Analog CMOS Integrated Circuits for Extreme Environments
Project 6: Radiation-Tolerant SiGe BiCMOS Smart MMICs for Space Communications
Project 7: Direct Digital Frequency Synthesizer for Reconfigurable Communication Systems
Project 8: SOI CMOS Continuous-Time Delta Sigma A/D Converters for Space Communication Radio Receivers
Project 9: RF, Analog and Digital Array for Radiation-Hardened Communication Circuits
Project 10: Radiation-Hard PLL Design Tolerant to Noise and Process Variations
Project 11: Low Temperature RF Characterization and Design of MOI5 SOI CMOS Circuits and Devices
Project 12: Reconfigurable Input/Output for Radiation Environments (Demonstration Project)
Project 13: Radiation Hardening by Design for Data Converters
Project 14: Design of Radiation-Hard Analog/Mixed-Signal Circuits in Silicon-on-Insulator (SOI) Technology

AFRL Task Area 3: Reconfigurable Mixed-Signal Electronics

Project 1: Reconfigurable RF Circuits for Low-Cost Phased-Array Systems
Project 6: Radiation-Tolerant SiGe BiCMOS Smart MMICs for Space Communications
Project 7: Direct Digital Frequency Synthesizer for Reconfigurable Communication
Project 9: RF, Analog and Digital Array for Radiation-Hardened Communication Circuits
Project 10: Radiation-Hard PLL Design Tolerant to Noise and Process Variation
Project 12: Reconfigurable Input/Output for Radiation Environments (Demonstration Project)
Project 13: Radiation Hardening by Design for Data Converters
Project 14: Design of Radiation-Hard Analog/Mixed-Signal Circuits in Silicon-on-Insulator (SOI) Technology

AFRL Task Area 4: System-on-a-Chip

Project 1: Reconfigurable RF Circuits for Low-Cost Phased-Array Systems
Project 4: Adaptive Regulation and Logic for Subthreshold Circuits
Project 6: Radiation-Tolerant SiGe BiCMOS Smart MMICs for Space Communications
Project 8: SOI CMOS Continuous-Time Delta Sigma A/D Converters for Space Communication Radio Receivers

AFRL Task Area 5: Predictive Radiation Effects Models

Project 5: SOI-CMOS Radiation Total Dose Device Models for Space Environment Applications
Project 8: SOI CMOS Continuous-Time Delta Sigma A/D Converters for Space Communication Radio Receivers
Project 11: Low Temperature RF Characterization and Design of MOI5 SOI CMOS Circuits and Devices

AFRL Task Area 6: Ultra Low-Power Technologies

Project 3: Circuit Design Techniques for Low-Voltage, Analog CMOS Integrated Circuits for Extreme Environments
Project 4: Adaptive Regulation and Logic for Subthreshold Circuits
Project 14: Design of Radiation-Hard Analog/Mixed-Signal Circuits in Silicon-on-Insulator (SOI) Technology

selection of the projects to be funded each year resided with AFRL and the designated AFRL Program Manager. The proposal selection process occurred at the beginning of each year of the three year program with all projects, continuing and new, under review. Consequently, some of the research projects were conducted for three consecutive years, while others were only funded for one or two years. Thus the research results from each of the projects varied according to the number of years a project was funded. Specifically, of the total number of projects in this program, four were funded for three years, five for two years, and another five for only one year (see Table 1).

Complete research results for all 14 projects are described throughout this report. These projects addressed topics that ranged from improved device models for use in SPICE-like simulators capable of addressing radiation effects, or improved models of devices using different geometric features known to minimize radiation effects, to specialized mixed-signal circuits such as digital-to-analog converters (DAC), analog-to–digital converters (ADC), phase-locked-loops (PLL) or voltage controlled oscillators (VCO), to more advanced circuit systems such as direct digital frequency synthesizers (DDFS). Two projects developed RF circuit designs suitable for incorporation into a low cost simplex transmitter/receiver to be used in a phased-array antenna system. When addressing requirements for circuit performance in a radiation environment, most of these designs incorporated some approaches using hardening-by-design technology. These approaches varied from the use of proven techniques using annular devices, to the use of creative architectures for redundancy or analog performance that incorporates more digital circuitry such as the digital PLL as a way to minimize the effects of energetic single particles to the design of circuits with self calibration and error correcting features allowing circuit performance across a range of extreme environments that includes radiation.

The above designs were realized as microelectronic circuits using a variety of fabrication process technologies. These processes included the Honeywell 3.3-V/0.35-μm PD-SOI (MOI5), IBM 7HP SiGe BiCMOS, IBM 0.13 μm process through the trusted foundry program, and the Jazz 0.18μm SiGe process. Complete details of the chips that were fabricated and circuit test results describing their measured performance are given in each report. Some of these results include performance measurement after exposing the test circuits to radiation.

Finally, upon the recommendation of the program manager, a “Demonstration Project” was developed and led by Honeywell investigators. In this project a portable test environment was developed to demonstrate the functionality and reconfigurability of selected ASICs that resulted from the individual faculty research efforts and were combined in a reconfigurable input/output system. The test environment is compatible with Single Event Effects (SEE), transient dose, and total dose radiation testing. The first generation of the reconfigurable demonstration consisted of a digital-to-analog converter (DAC) from Oregon State University, an analog-to-digital converter (ADC) from SUNY at Stony Brook, a phase-

locked-loop (PLL) from Oregon State University, and reconfigurable digital signal processing (DSP) from the University of Washington. The real time operation of the ADC/DAC and PLL was captured and displayed on a laptop computer. The ability to reconfigure the PLL was demonstrated. The benefit of a system such as this would allow reuse in numerous aerospace systems, reducing development and integration time as well as cost.

In summary, the mixed-signal circuit design research reported here as it relates to the six AFRL research themes resulted in improvements and innovations in the current state-of-the-art design of circuits used for space applications. However, to be affordable, radiation-hardened, mixed-signal technology must be adapted from the technology being developed for consumer products. The cost of developing an independent approach for defense systems is prohibitive. Therefore, the optimum approach is to leverage the investments and research and development activities of the consumer electronics industry. Thus, this research effort built upon the strong connection of CDADIC's industry members along with its research faculty that provided significant added value to the final research accomplishments. It was important that this research activity provide benefit for some commercial applications, which was also accomplished and described in this report. Examples include benefits to commercial satellite systems and wireless applications.

A final observation can be made as to the value to the sponsor of this research program. The totality of the value from 14 research projects over a three-year period is more than the technical results reported here, which are significant, but must also include the value to the government and defense industry resulting from the education and training of students who are available to enter the workforce. Forty-one (41) students participated in this research activity and supported the publication of 34 journal articles and conference proceedings, as well as theses and dissertations. In addition, two students were selected to serve as interns in AFRL's Space Scholars Program and worked directly in the sponsor's laboratory. Through the sponsors CDADIC membership, additional technology was transferred to the laboratory at no additional cost, resulting in a significant dollar savings to AFRL. One must therefore conclude that this approach of supporting research activity important for defense and space applications through an existing industry-university research consortium, such as CDADIC, is both a cost effective and operationally efficient approach that should be considered for future programs.

RESEARCH PROJECTS

PROJECT 1

RECONFIGURABLE RF CIRCUITS FOR LOW-COST PHASED-ARRAY SYSTEMS

Prof. David Allstot (University of Washington) with
Greg Kromholtz and Rod Bonebright (Boeing)

RESEARCH TIME PERIOD: Two years
RESEARCH FOCUS: AFRL Task Areas 3 and 4: Reconfigurable Mixed-Signal Electronics and System-on-a-Chip Design.

Figures and Tables

Abstract

The demand for spectrally efficient communication is the motivation behind the development of phased array systems. A phased array system with careful design can offer a low-cost means of increasing the efficient use of currently available bandwidth. Several key focus areas can greatly reduce the cost; for instance, by using a single die, with an integrated T/R switch, there is no necessity of two antennas. By using a silicon process, the cost of the die is decreased. The concerns of on-chip coupling can be mitigated using simplex operation, thus the TX and RX paths are never on at the same time.

Work completed on this subject during this project has greatly enhanced the ability to realize these systems. The PA and T/R switch have been realized on a silicon substrate and implemented for a practical system at frequencies approaching 15 GHz. The goal of this research was not only design these circuits to meet the specifications, but also to design compensation for variations due to process, voltage and temperature. The techniques developed have been fabricated on the IBM 7HP SiGe BiCMOS process.

Project Description

Integrated circuit technology, with its rapid advancement, has had a huge impact on daily life throughout the modern world. This impact is largely through the advent of advanced communications systems that allow for large amounts of data to be transmitted rapidly to any place in the world. Unfortunately with these advances, the amount of spectrum available for communications continues to shrink. This shrinkage is manifested most prominently in military communications. The modern battlefield consists of one in which ground-based infantry must coordinate rapidly with close air support, while simultaneously monitoring troops vital signs and broadcasting surveillance data to the command center, thus compounding the importance of highly efficient military communications systems.

In order to be effective, the communication must be able to reach all levels of a command structure, from the highest level command center to the individual soldier or aviator. Furthermore, the uplink of information is as important as the downlink, which means that all parties must have the ability to send and receive data simultaneously, requiring large amounts of bandwidth. The bandwidth crunch is becoming more evident despite the fact that, on average, American soldiers have hundreds of times more bandwidth today than they did in the first gulf war [1].

Due to the lack of available bandwidth, there is now more than ever a necessity for more spectrally efficient systems. Highly efficient systems, such as Space Division Multiple Access (SDMA), which reuse spectrum in areas that are physically close to one another by isolating the transmitted direction of the signals, have found heavy use in satellite communications. These systems, however, cannot achieve the additional spectral efficiency attainable from Time Division Multiple Access (TDMA), due to the bulky mechanically steered parabolic aperature antennas used. By mechanically steering the antenna, the beam simply cannot be moved fast enough to effectively change spatial signal paths to the multiple users.

Phased array systems offer the ability to create directional signals without physically moving the antenna. By increasing the frequency of operation, the array can be made physically small, which allows for easy integration into most aircraft and terrestrial vehicles. The direction of the antenna beam is steered electrically by controlling the phase and amplitude of the signal applied to each element in the array. This means that the beam can be steered virtually instantaneously, which allows for directional communication between vehicles, ground personnel and aircraft. The spectral efficiency is high, due to the directionality of the signal, the same frequency can be used by other nearby personnel. This type of communication is also more secure, due to the fact that the signal is only transmitted in one direction, thus making interception of the signals much more difficult. Another benefit is that communications between vehicles does not occupy valuable satellite bandwidth.

Though there are already commercially available phased array systems, such as those offered by Boeing [2], there are still several issues preventing their wide-scale implementation in the field. The antennas tend to be costly and bulky. This is mainly due to the fact that they are typically optimized for use in satellite communications, which means that the antenna must have low loss and high gain. By using the systems on a battlefield, the proximity of the users allows for degradation in the traditional performance of these systems.

The cost and size of the array can be greatly reduced by addressing a few necessities. Firstly, in the implementations available, the transmit and receive paths have been on separate ICs, due to the lack of isolation provided on a single die. Cost and size could be reduced if the ICs were able to be combined on one die. Next, the traditional processes used in manufacturing these ICs are more exotic, such as gallium arsenide (GaAs), and thus more expensive. This has been necessary in order to achieve high performance at microwave frequencies. Cost could be reduced if standard silicon processes could be used to replace GaAs. The antenna size has largely been dictated by the fact that geosynchronous satellites orbit at 36000 miles. The size requirement to achieve the same performance is much smaller when confined to a battlefield. Finally, packaging and assembly for such a low loss application has been expensive, but the packing requirements will be relaxed for closer proximity applications.

Addressing these issues will make the phased array viable for use, starting on the battlefield and moving into commercial options, such as wireless LANs. This research addressed some of the hurdles that needed to be cleared, as well as the achievements made as part of the continuing research to place the transmit and receive paths of a phased array communication system on a single SiGe IC.

Research Results and Discussion

Research has been on going at the University of Washington to improve the performance of the key circuits necessary to implement a phased array transceiver IC. The transceiver front-end IC consists of four key research topics, namely the Transmit-Receive (T/R) switch, the variable gain low-noise amplifier (VGLNA), the phase shifting network and the power amplifier (PA). As an additional goal, the circuits must be designed on a silicon based process, to achieve a more desirable die cost. Much progress has been made toward the design of the T/R switch, VGLNA and Power Amplifier. In the following paragraphs a summary of the work that has been performed on each of the stages will be detailed.

Furthermore, a general process comparison between two commercially available processes has been made, and the results will also be discussed. Lastly, work has been performed in conjunction with Boeing. Their contributions will also be briefly summarized

T/R Switch

The T/R switch is the most critical aspect to achieving a single die and single array solution for a phased array system. The T/R switch investigation began by looking into various topologies, using both HBT and MOS devices. In the end, the decision was made that the best solution was to optimize MOS transistors in standard gate controlled switch configurations. The bulk of progress made has been to resonate out parasitic effects, using cleverly placed passive circuitry. A complete CMOS switch has been processed in IBM7RF 0.18 mm CMOS. The work was presented at the 2005 ISCAS conference [3].

VGLNA

Several recent investigations into using commercially available CMOS processes have been conducted at the University of Washington. A test chip with two novel techniques for reducing the noise figure of the common gate topology was fabricated. Measured results showed that by using an inverting unity gain feedback loop, the NF of a CG stage could be reduced by almost a factor of two over the traditional CG stage. By optimizing the input impedance, a further reduction of the noise figure was possible, thus lowering the overall NF to approximately 2 dB at 5.6 GHz. Two topolgies were designed and fabricated, one using a transformer as the feedback mechanism, the other using cross-coupled NFETs. The design was completed using IBMs 7RF process. It shows that with clever topology design and improved processes, CMOS technology is moving in the right direction for use in terrestrial based phased array systems [10]-[11].

Work was also completed on the design of an LNA in IBMs 7HP SiGe process. The 7HP process has an ft of approximately 100 GHz, which allows for traditional topolgies to be used at very high operating frequencies. The design shows a NF of less than 2.5 dB across the band of operation, while also adding a gain of 15 dB. The design is a simple single-stage cascode with emitter degeneration, and a current steering mechanism that allows for 50 dB of gain control. By carefully choosing device size, bias current and matching network topology, it is possible to use SiGe transistors in the same way that standard Si transistors would be used at much lower operating frequencies.

Power Amplifier

There are several problems facing Power Amplifier design as processes are scaled to the deep-submicron level. The processes are operating with lower voltages and it is necessary to use many devices in parallel, due to current density limitations. Furthermore, the relatively poor passives available on a silicon based process do not compare to the passives available on III-V compound processes.

The main problem with the voltage scaling downward is that the optimum termination resistance must be reduced as the square of the voltage to achieve the same power output (i.e. more current must be forced through the output). This is a difficult issue to solve, because the common interface impedance with the outside world is 50 ohms, which is rather large impedance. For the typical 1.8 V process, in order to achieve an output power of 24 dBm, it is necessary to use a load resistance of approximately 1.5 ohms. This is without considering loss in the passive matching networks, thus in reality, the impedance would be much lower. One solution is to use a differential topology which has been demonstrated to increase the optimal termination by a factor of four. This is because the transformation from single-ended to differential gives a benefit of two times, coupled with the factor that each branch of the device only has to handle half the current of a single-ended stage [4].

The problem with differential designs on chip is that typically the interface to the antennas is single-ended, thus a conversion must be made, ideally on chip. Furthermore, for measurement simplicity, it is nice to have a single-ended input to the power amplifier, thus requiring two balanced-to-unbalanced converters (Baluns). Previous work has demonstrated that these can be implemented well on chip, utilizing a combination of LC-baluns and spiral transformer baluns [5]. Both designs offer absorption of

the some of the matching into the balun, through intelligent choice of components. The LC-balun (essentially a polyphase filter) is easy to design and is the preferable choice for the output of the power amplifier, due to more efficient power coupling to the output. The spiral transformer is more difficult to design, due to the necessity of electromagnetic simulations. Electromagnetic simulations result in frequency domain s-parameters, which are not compatible with the time domain simulations necessary to characterize distortion in a power amplifier. Thus the complexity of the problem is increased through the need for a compact model. The model chosen was presented in [6] and was augmented with the skin effect model described in [7].

The voltage problem can be further mitigated by utilizing the effect of impact ionization. The typical limitation of voltage in a bipolar device is the collector to emitter breakdown voltage which if exceeded results in avalanche breakdown. This limit is kept unnecessarily low by assuming that the base of the device is driven by a constant current source, rarely a good assumption. If driving the base with a constant voltage source, the device can be operated with much higher voltage limits [8]. Furthermore, cascoding the devices allows the collector to swing as high as $2V_{CE,MAX}$, thus causing the voltage to be limited by the larger collector to base breakdown potential.

The work presented herein details several techniques that allow for a power amplifier to operate into larger load terminations, while maintaining the ability to deliver an output power of over 250 mW with a power-added efficiency (PAE) above 20 %. The PA topology, shown in Figure 1 is similar to the design presented by Bakalski, et al. [12], with the exception that it is cascoded to enable the increased voltage swing when two devices are stacked. Furthermore, the work of Rickelt, et al. [13] shows that it is possible to drive a device beyond the standard collector-emitter breakdown voltage, BV_{CEO}, if the transistor bases are biased with a low-impedance source. This low impedance source allows holes generated by impact-ionization to flow out of the base. By utilizing a combination of these techniques, the breakdown limitation can be shifted from the much lower BV_{CEO} to the typically much larger collector-base breakdown, BV_{CBO}.

A differential topology is chosen so that the devices can be biased in a class-AB fashion while maintaining linear operation. Because each device in the differential pair only has to provide half the power of a single-ended topology the optimum termination impedance increases by a factor of four. The drawback of this approach is that a differential-to-single-ended conversion is typically required. As in [12], the conversion is made using spiral baluns at the input and between the driver and PA stage along with a lumped LC balun at the output. The spiral baluns provided both dc biasing and matching, essentially acting as a bias tee. The LC balun is used to provide matching from the optimal termination to the 50 ohm system interface. The spiral baluns were constructed over a deep trench isolation cross-hatch and modeled using the commercial electromagnetic software.

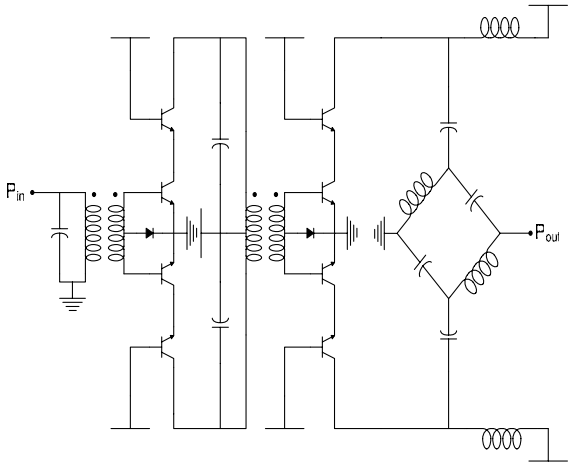


Figure 1. Power amplifier showing driver and output stages along with input, inter-stage, and output matching networks.

Passive Circuit Design/Optimization

Differential circuits are commonly converted to single ended using balanced-to-unbalanced converters (BALUNs). These devices are typically implemented with either a polyphase filter, or with center-tapped transformer devices. Both topologies require two inductors, but the transformer can utilize an interleaving structure, thus it is desirable for on chip applications, due to the reduced size. Transformers on chip are difficult to implement, due to the lack of models available from the manufacturer. This can be overcome, utilizing commercially available electromagnetic simulators, such as ADS Momentum. A substrate must be designed and optimized, usually by comparing Momentum simulations of spiral inductor structures with the corresponding IBM model. The result is a substrate definition that can be used to simulate interleaved spiral transformers. A previous IBM 7RF run has shown agreement within the expected process tolerance, between Momentum results and measurement. The IBM7HP process does, however, present a few more difficulties versus the 7RF process. Spiral structures in IBM SiGe processes are manufactured over a deep trench isolation. The substrate is broken up with deep trench cross hatches. Inside the cross hatch area is a lightly doped region, alternating between p and n type material. What results is reduction in capacitance, as well as smaller paths for eddy current loops. Though this is good for performance, it is a much more computationally intensive simulation than an inductor over a patterned ground shield (PGS) [9]. This is because, the simulator must calculate currents of any conducting structure, the deep trench structure adds many more elements than a PGS. Simulation substrates have been developed for this purpose, and have been tested through measurement on the IBM7HP manufacturing run. Measured results are depicted in Figures. 2-5.

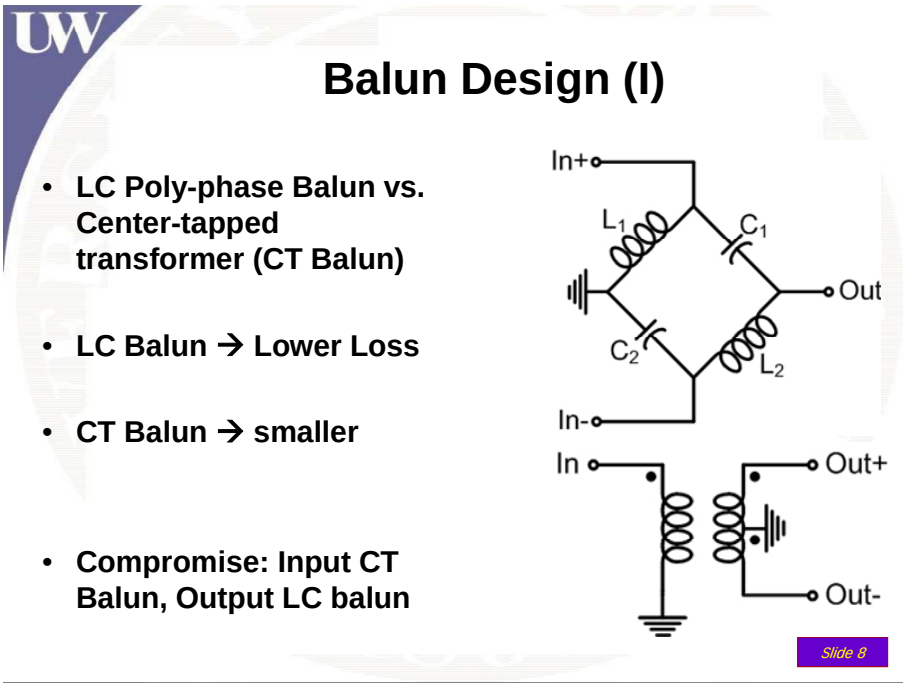


Figure 2. Measured output power vs. frequency.

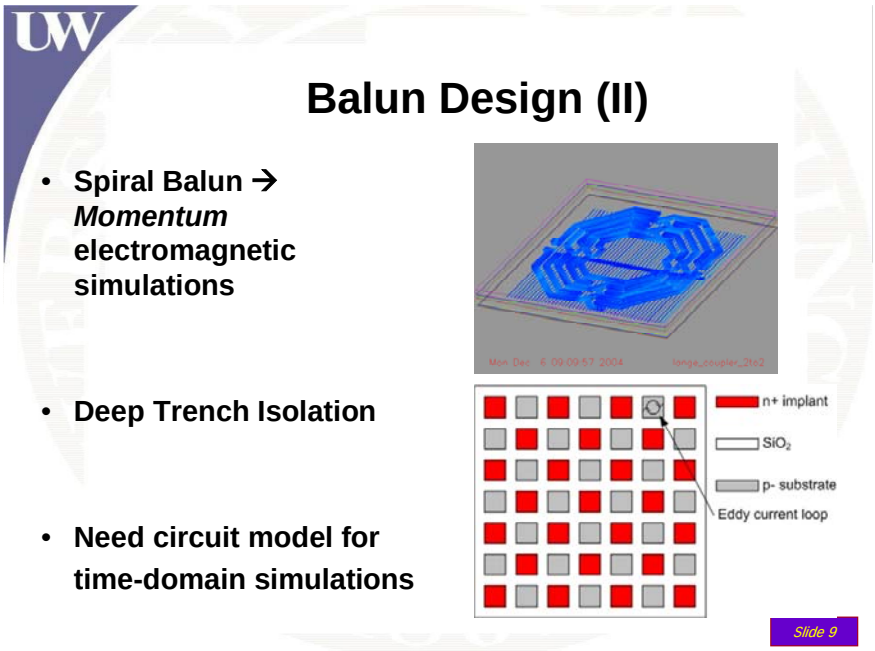


Figure 3. Measured output power vs. input power at three frequencies.

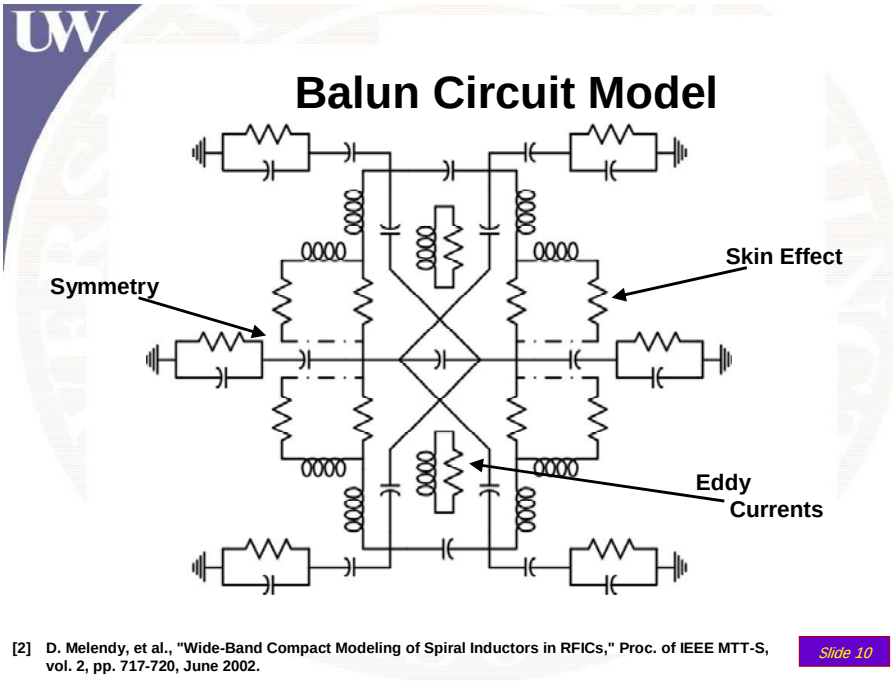


Figure 4. Measured PAE vs. input power at three frequencies.

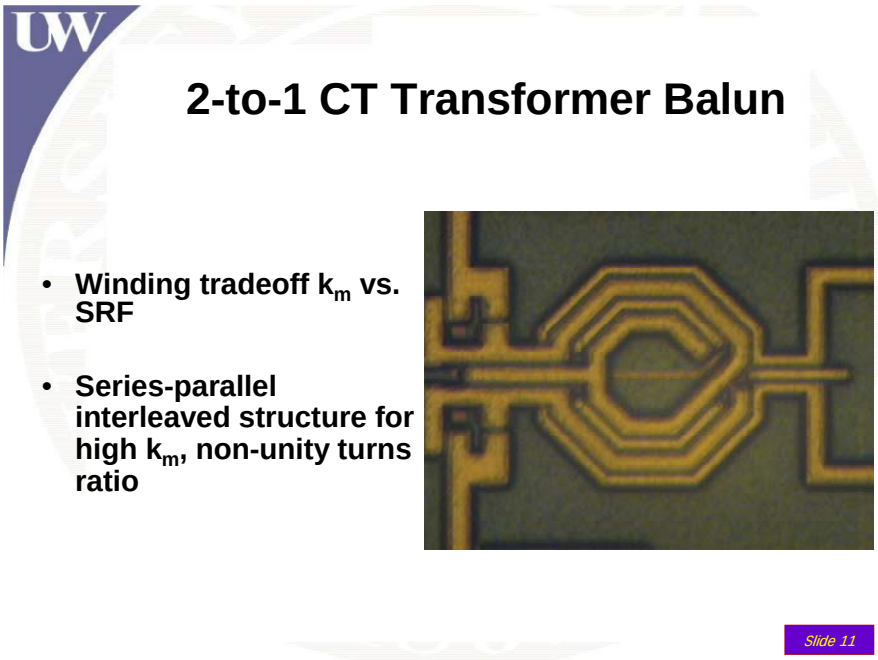


Figure 5. PA microphotograph; the die size is 2mm by 1 mm in a 0.18 μm SiGe BiCMOS process.

Test Chip

Power Amplifier Metrics

The power amplifier (Figure 9) was fabricated in a 0.18 μm SiGe BiCMOS process, with 7 layers of metal and inductors over deep trench isolation. The power amplifier operates from a 3.8-V supply, which is almost twice the BV_{CEO} for the process. The measured power output versus frequency is displayed in Figure 6, showing a peak output power of 25.5 dBm at 8 GHz. A detailed plot of the measured power transfer characteristic is shown in Figure 7, displaying the low, mid and high frequency performance of the PA. Finally, the PAE is plotted for three different frequencies in Figure 8, showing a peak PAE of 35% for the mid-band frequency.

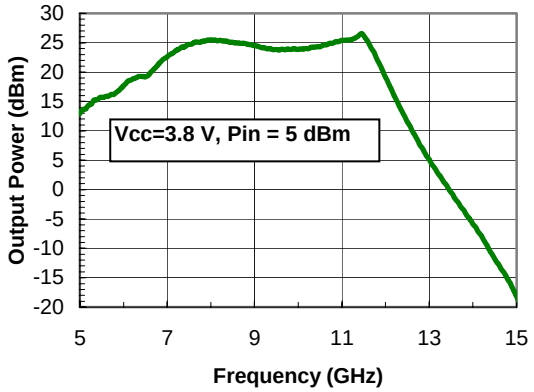


Figure 6. Measured output power vs. frequency.

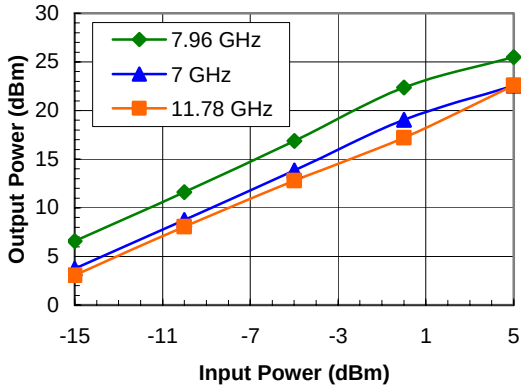


Figure 7. Measured output power vs. input power at three frequencies.

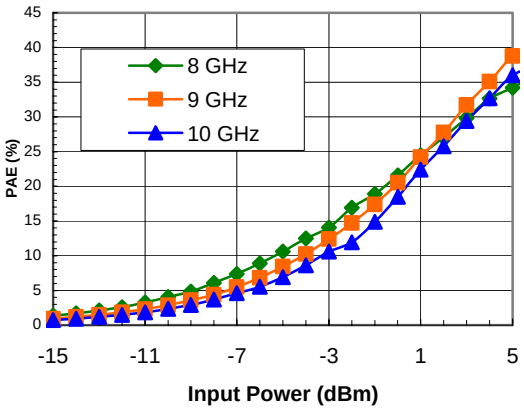


Figure 8. Measured PAE vs. input power at three frequencies.

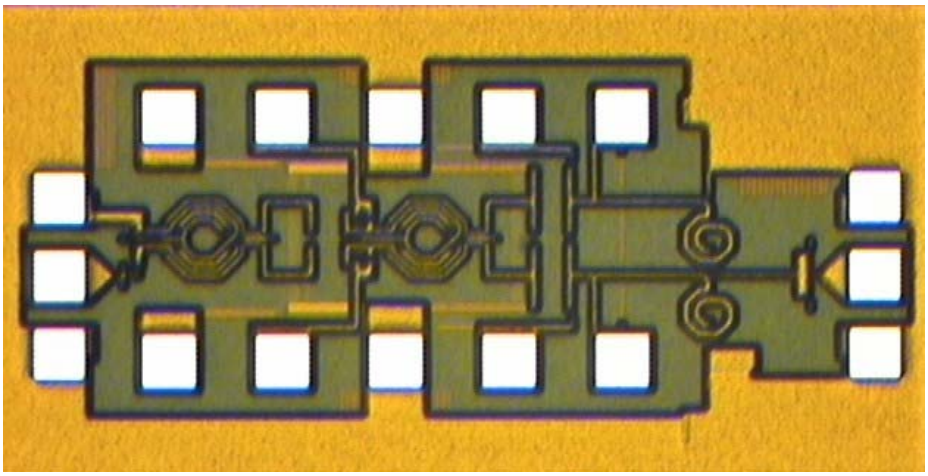
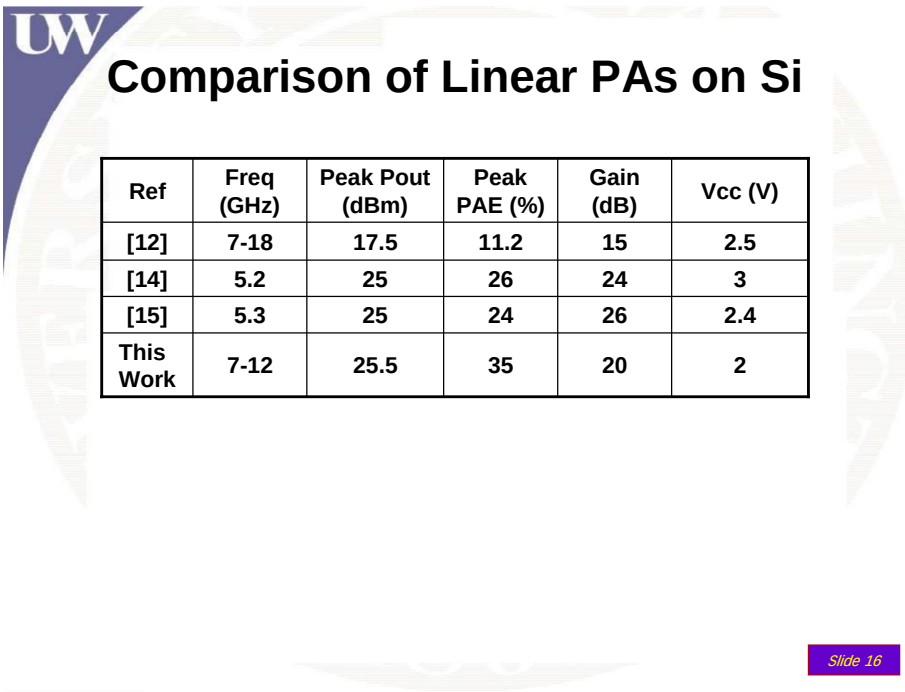


Figure 9. PA microphotograph; the die size is 2mm by 1 mm in a 0.18 μm SiGe BiCMOS process.

PA Comparison

A comparison to prior art is detailed in Figure 10. It is noted that the PA designed for this work compares well to other silicon based linear power amplifiers, offering the best reported PAE at the time of completion.



Ref	Freq (GHz)	Peak Pout (dBm)	Peak PAE (%)	Gain (dB)	Vcc (V)
[12]	7-18	17.5	11.2	15	2.5
[14]	5.2	25	26	24	3
[15]	5.3	25	24	26	2.4
This Work	7-12	25.5	35	20	2

Figure 10. Comparison of linear PAs on SI results.

Radiation Hardness

The fabricated chips were also measured for there radiation hardness. An experiment at Boeing was set up such that the chips were radiated with a Cobalt 60 radiation source set for a dose rate of 49.1 kRad/s. The chips were radiated for 33 minutes 53 seconds, resulting in a total dose of 100 kRad. Before each dosing began, the chips DC quiescent current was measured and recorded. The results of the experiment are detailed in Figure 11. It is noted that the measurement results do not vary significantly with total dose, which is expected due to the significant radiation hardness of the SiGe transistors.

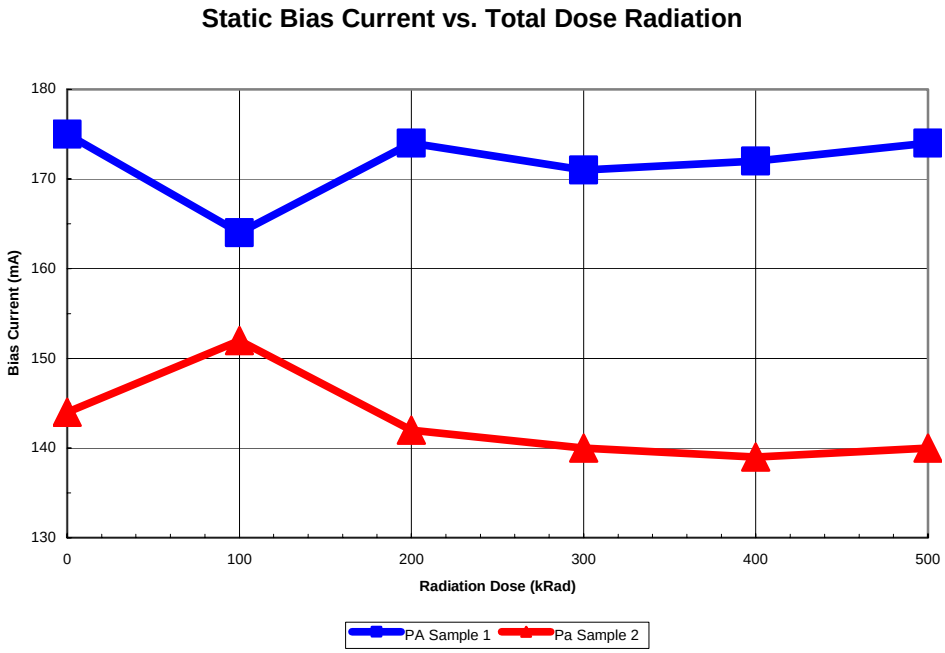


Figure 11. Static bias current vs. total dose radiation test results

Other Results

Technology Transfer/Intellectual Property

Not at this time.

Publications Resulting from Research

Not at this time.

Benefits to Commercial Sector

This work has potential for commercial WLANs operating in the microwave frequency range.

References

[1] Wired News: Military Faces Bandwidth Crunch, www.wired.com/news/infostructure/0,1377,57420,00.html, 31 Jan., 2003.

[2] Microelectronics Phased Array Antenna Center – Home Page, www.boeing.com/defense-space/infoelect/micro/flash.html, accessed 06 June, 2003.

[3] K. Naegle, S. Gupta and D.J. Allstot, "Design considerations for a 10GHz CMOS transmit/receive switch," *IEEE Int'l Symposium on Circuits and Systems (ISCAS)*, May 2005, pp. 2104-2107.

[4] Steve C. Cripps, RF Power Amplifiers for Wireless Communications, Artech House, 1999.

[5] Winfred Bakalski, Andriy Vasylyev, Werner Simburger, Ronald Thuringer, H. D. Wohlmuth, Arpad Scholtz and Peter Weger, "A fully integrated 7-18 GHz Power Amplifier with on-chip output balun in 75 GHz-f_T SiGe-Bipolar," *IEEE BCTM*, vol. 39, pp. 863-870, June 2004.

[6] Adam C. Watson, Daniel Melendy, Pascale Francis, Kyuwoon Hwang and Andreas Weisshaar, "A Comprehensive Compact-Modeling Methodology for Spiral Inductors in Silicon-Based RFICs," *IEEE Trans. Microwave Theory and Techniques*, vol 52, pp 849-857, March 2004.

[7] B. K. Sen and R. L. Wheeler, " Skin Effects Models for Transmission Line Structures Using Generic SPICE Circuit Simulators," *IEEE 7th Topical Meeting on Electrical Performance of Electronic Packaging*, pp 128-131, Oct. 1998

[8] M. Rickelt, H.-M. Rein and E. Rose, " Influence of Impact-Ionization-Induced Instabilities on the Maximum Usable Output Voltage of Si-Bipolar Transistors." *IEEE Trans. on Electron Devices*, vol. 48, pp 774-783, April 2001.

[9] C. A. Chang, S.-P. Tseng, J. Y. Chuang, S.-S. Jiang and J. A. Yeh, "Characterization of Spiral Inductors With Patterned Floating Structures," *IEEE Transactions On Microwave Theory and Techniques*, vol. 52, no. 5, pp. 1375-1381, May 2004.

[10] W. Zhuo, X. Li, S. Shekhar, S.H.K. Embabi, J. Pineda de Gyvez, D.J. Allstot and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low noise amplifier," *IEEE Trans. on Circuits and Systems I: Express Briefs*, vol. 52, pp. 875-879, Dec. 2005.

[11] X. Li, S. Shekhar and D.J. Allstot, "G_m-boosted LNA and VCO Circuits in 0.18um CMOS," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2609-2619, Dec. 2005.

[12] W. Bakalski, A. Vasyltev, W. Simburger, R. Thuringer, H.-D. Wohlmuth, A. L. Scholtz and P. Weger, "A fully integrated 7-18 GHz power amplifier with on-chip output balun in 75 GHz-f_T SiGe-bipolar," *IEEE Bipolar Circuits and Technology Meeting*, 2003, pp. 61-64.

[13] M. Rickelt, H.-M. Rein and E. Rose, "Influence of Impact-Ionization-Induced Instabilities on the Maximum Usable Output Voltage of Si-Bipolar Transistors," *IEEE Trans. on Electron Devices*, vol. 48, pp. 774-783, April 2001.

[14] A. Scuderi, et al., "A 5.2-GHz silicon bipolar power amplifier for IEEE 802.11a and HIPERLAN2 wireless LANs" *Proceedings of ESSCIRC 2004*, pp. 203-206, 21-23 Sept. 2004.

[15] W. Bakalski, et al., "A Fully Integrated 5.3 GHz, 2.4 V, 0.3 W SiGe-Bipolar Power Amplifier with 50 W Output," *IEEE Journal of Solid State Circuits*, vol. 39, pp. 1006-1014, July 2004.

PROJECT 2

LOW POWER WIRELESS SENSOR FOR SPACE AND MILITARY APPLICATIONS COMMUNICATIONS SYSTEM SPECIFICATION AND SIMULATION FOR WIRELESS SENSORS

Prof. David Allsot and Ward Helms (University of Washington) and Prof. Huaping Liu (Oregon State University) with Gary Nelson and Steve Fahley (Boeing)

RESEARCH TIME PERIOD: One year
RESEARCH FOCUS: AFRL Task Area 2: Standard Cell/Topologies in Radiation-Hardened SOI.

Figures and Tables

Abstract

The researchers of this project collaborated to develop an extremely low power wireless sensor communications system for space vehicle applications. The project builds on technology developed at Boeing for a Remote Sensor for wireless applications. This sensor requires a base station, called a HUB, for stimulating and receiving sensor information from up to 30 sensor modules, called remotes. The radio frequency (RF) circuits were implemented in the Honeywell MOI-V process. The wireless hub architecture was defined and simulated at the system level. Specifications for individual RF circuit blocks were derived from overall system specifications. The Honeywell MOI-V technology files were transferred to the University of Washington's CAD platforms and were used in preliminary RF circuit designs. Circuit design was implemented for the low-noise amplifier (LNA) and the mixer. A first-pass low-noise amplifier and harmonic mixer were designed and simulated in the MOI-V process.

During the first year of the project, which was the only year of this effort since the project was not continued (not granted further funding), the researchers accomplished system design and modeling, circuit design, layout, and release of mask designs for fabrication. Since the project was not renewed beyond the first year, fabrication and testing of the parts were not finalized. For the low power wireless sensor system, the preliminary system specification was completed, and both forward link and reverse

link communication blocks were specified. Characterization of in-band and out-of-band interference was finished. Circuit design was started for the major RF building blocks as well.

Project Description

This research focused on the development of an extremely low power wireless sensor communications system for space vehicle applications. The project built on technology developed at Boeing for a Remote Sensor for wireless applications. This sensor requires a base station, called a HUB, for stimulating and receiving sensor information from up to 30 sensor modules, called remotes. The Boeing work has been limited to the sensor module. The sensor module consists of a circular patch antenna, RF ASIC, several sensors, analog sensor processing and digital control circuits all packaged in a hybrid module approximately 1 inch by 1 inch square. The sensor module exists. This research advanced the design of the HUB. Basic architecture and fundamental RF concepts have been demonstrated in a Boeing lab where HUB RF functions have been emulated by RF test equipment.

The system developed is applicable to Space Station experiment monitoring and to space exploration where wiring additions pose difficult problems. (For example, on the Next Generation Space Telescope, NGST, the telescope operates at 35 °K, and the electronics for signal processing operates at 270 °K. Consequently, wires placed between these packages represent significant thermal isolation violations. Applications of the low power wireless sensor system also occur for helicopter rotor blades, aerial refueling gear, landing gear tire pressure and temperature profiles, brake temperature, etc.

Research Results and Discussion

Part I: Low Power Wireless Sensor for Space and Military Application

For this project, the Honeywell MOI-V process was found to be a useful process for RF circuits operating around 2.4 GHz. The process offers suitable passive components along with reasonably fast MOSFET devices. However, it should be noted that the 0.35 m minimum drawn channel length incurs significant power consumption penalties at higher frequencies. As faster circuits are designed, a CMOS process with smaller minimum dimensions is recommended.

Circuit designs and layouts are presented for a low-noise amplifier (LNA), an even-harmonic direct down-conversion mixer (EHM), and a voltage-controlled oscillator (VCO). These circuits are analyzed in detail in the following section under research results.

Low-Noise Amplifiers (LNA)

Common-source and common-gate LNA topologies were designed in the Honeywell MOI-V process and compared. The comparison is important because the common-source topology has a lower noise figure below a critical frequency, whereas the common-gate topology is superior at higher frequencies. However, this frequency is process-dependent and must be determined empirically. At 2.4 GHz, the common-source topology provided a lower noise implementation. Both topologies have been laid out and submitted for fabrication to Honeywell using their CMOS MOI-V process. Figures 1 and 2 show the common-source and common-gate LNAs, respectively, and Tables 1 and 2 summarize their simulated performance parameters.

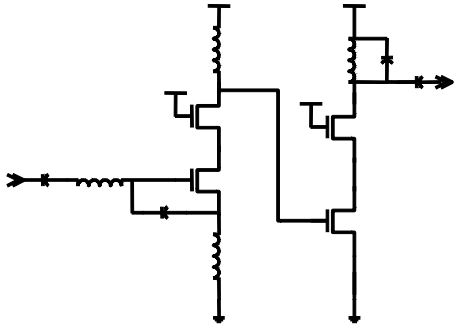


Figure 1. Common-Source LNA; biasing not shown.

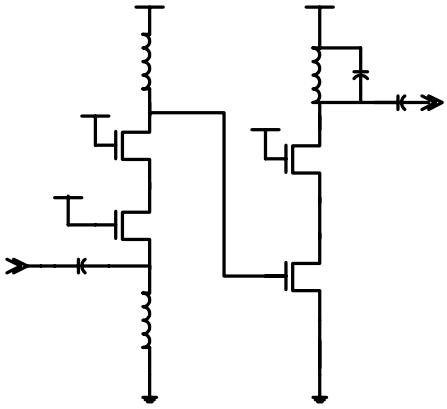


Figure 2. Common-gate LNA; biasing not shown.

Table 1: Common-Source LNA Simulation Results.	
S21 Gain	12 dB
NF (gamma=2)	3.5 dB
S22 match to 50Ω	-20.5 dB
S11 match to 50Ω	-11.9 dB
Power @ 3.3V	13.4 mW
Area	0.783 mm^2

Table 2: Common-Gate LNA Simulation Results.	
S21 Gain	13.8 dB
NF (gamma=2)	6 dB
S22 match to 50Ω	-21 dB
S11 match to 50Ω	-20 dB
Power @ 3.3V	19 mW
Area	1.05 mm^2

Direct Down-Conversion Mixer

The frequency translation mixer designed for this work utilizes a direct down-conversion approach. This topology offers several advantages over previous mixer architectures. (Note: For details, see S.J. Fang, et al., "A 2GHz CMOS Even Harmonic Mixer for Direct Conversion Receivers," IEEE International Symposium on Circuits and Systems, May 2002.) In addition, a new mixer is developed that is directly coupled to the LNA via an on-chip spiral transformer. This eliminates the cumbersome current-voltage conversion at the output of the LNA followed by voltage-current conversion at the input to the mixer.

In order to simulate the transformer-laden design prior to layout and fabrication, an accurate transformer needed to be designed and modeled. This step required the use of the Agilent ADS MOMENTUM electro-magnetic simulator to model the electromagnetic fields for the metal layer and substrate details characteristic of the Honeywell MOI-V process. The layout of the transformer is fully symmetric as shown in Figure 3. The circuit model used to simulate the performance of the inductor is given in Figure 5.

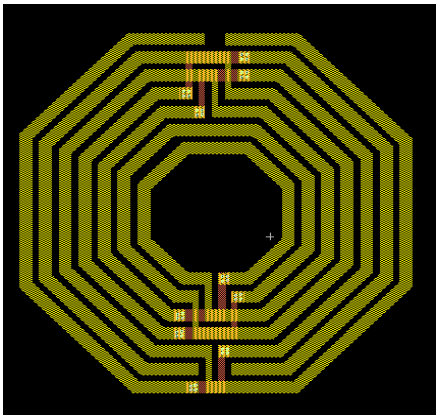


Figure 3. Symmetric on-chip spiral transformer layout.

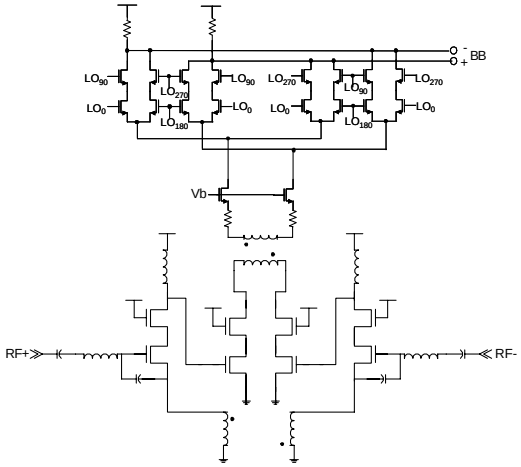


Figure 4. Differential common-source LNA and direct down-conversion mixer linked using an on-chip transformer.

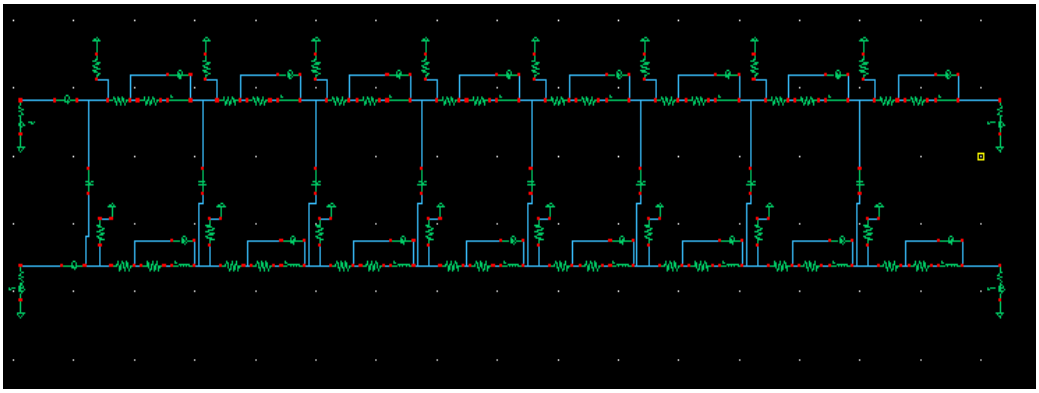


Figure 5. Simulation Model for Transformer in Figure 3.

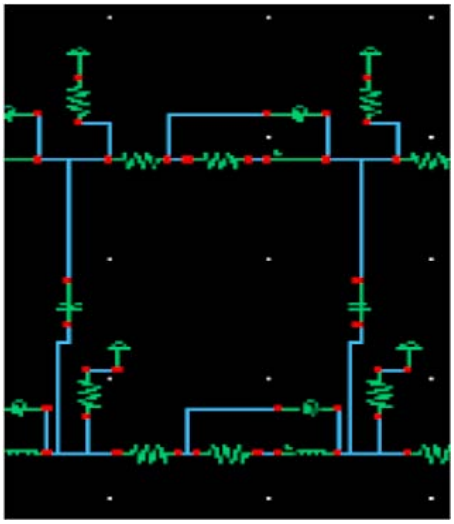


Figure 6. Closeup of transformer simulation element model.

Figure 6 contains a closer look at an individual lumped element approximation used in the transformer model. Each lumped element corresponds to one loop of the inductor. The typical inductive, resistive, and capacitive elements are readily seen in the figure. In addition, there are current-dependent current generators that inject current depending on the current in the other side of the transformer, modeling the mutual inductance of the system. Since the Honeywell MOI-V process does not have a standard substrate, there is no capacitor to AC ground required. However, since there are various couplings to other structures on-chip, a large resistor shunted to ground is used to model the small losses induced in these capacitive couplings at RF frequencies.

The complete schematic of the fully differential common-source LNA transformer coupled to the direct down-conversion mixer is shown in Figure 4. Note that the transformer described above is also used in the biasing the differential LNA to improve common-mode performance.

Simulation results of the transformer coupled LNA-mixer are presented in Table 3. In a follow-on design, the LNA gain should be increased because the resulting noise figure is higher than that of the LNA alone.

Table 3. Combined LNA-Mixer Simulation Results

Conversion Gain IF=40MHz	38 dB
NF (gamma = 2/3)	4.4 dB
S11 match to 50Ω	-10 dB
Power @ 3.0V	33 mW
Area	3.12 mm^2

Voltage-Controlled Oscillator

A voltage-controlled oscillator (VCO) was designed to enable operation at both the military band of 2.24 GHz and the unlicensed ISM band at 2.4 GHz. An LC-oscillator was chosen over a ring-oscillator in order to minimize phase noise.

Creating a varactor in the Honeywell MOI-V process proved to be difficult. Traditionally, varactors are created in one of two ways. One varactor option is a PN junction. A PN junction is useful because its capacitance depends on the DC voltage across its junction. However, this is not a good option in technologies that do not utilize bulk silicon substrates because there is only sidewall PN junction capacitance, whereas traditional bulk silicon technologies also have bottom-wall junction capacitance.

A second option for creating varactors is using MOSFET devices. The gate capacitance of a MOSFET depends on its region of operation, which can be controlled by the DC bias applied to the device. There are two common connections for the bulk terminal of the MOSFET used as a varactor: Short the bulk terminal to the source and drain terminals, or terminate the bulk connection on a known DC potential that maintains a reverse bias on the PN junctions in the device. However, the semi-insulating substrate of the MOI-V mandates the first option.

For comparison purposes, both types of varactors were designed and simulated. The PN junction varactor exhibits better controllability than its MOSFET counterpart and was therefore selected for the final VCO design even though a MOSFET varactor is expected to have better nominal characteristics.

To minimize phase noise by maintaining symmetric rise/fall times and to sustain oscillations, a complementary cross-coupled MOSFET VCO topology was used. The 3.3V power supply enabled the use of both PMOS and NMOS cross-coupled pairs. The final VCO schematic is shown in Figure 7, and its simulated performance specifications are given in Table 4.

The high gain of the VCO makes this circuit difficult to use without further modification in a complete receiver system. However, this design required a frequency range of 2.24 GHz to 2.40 GHz with tolerances for process, voltage, and temperature variations. An option to overcome this problem is to implement binary switched-capacitors in parallel with the varactors to lower the gain. This option will be included in future designs.

Table 4. Voltage-Controlled LC-Oscillator
Simulation Results

Frequency Range	2.18-2.48 GHz
VCO gain	225 MHz/V
Phase Noise @ 1 MHz offset	-100 dBc/Hz
Power @ 3.3V	17 mW
Area	0.8 mm2

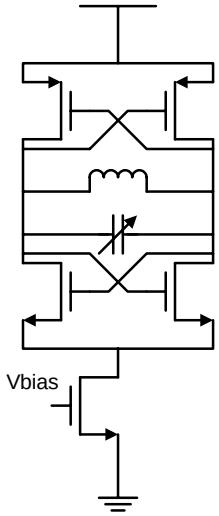


Figure 7. Complementary-MOS voltage-controlled LC-oscillator.

Test Chips

All of the circuits were laid out in the Honeywell MOI-V process and were submitted for fabrication. However, since the project was not renewed/funded beyond the first year, fabrication and testing of the circuits were not finalized.

The complete circuit layout is shown in Figure 8. The narrow design on the left is the VCO. The large bluish regions are the PN junctions required to create the required varactors. In the middle are the two LNA topologies. The large circuit on the right is the transformer-coupled differential LNA-mixer. The primary transformer in the LNA-Mixer circuit is the uppermost coiled structure.

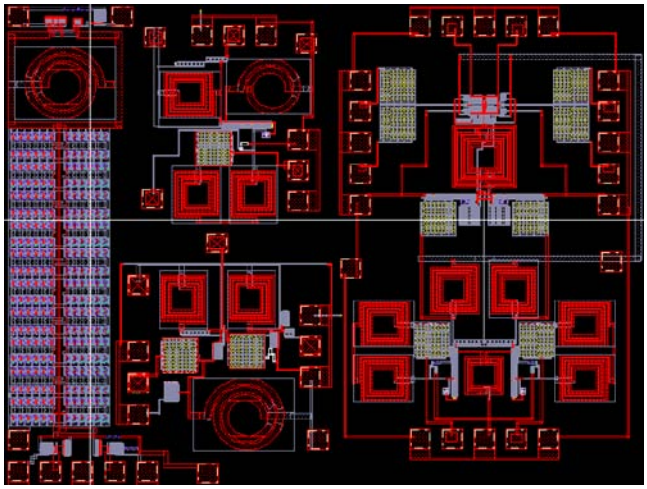


Figure 8. Completed circuit layout for fabrication in the 0.35μm Honeywell MOI-V process. The die size is 5.8 mm^2.

Part II: Communications System Specification and Simulation for Wireless Sensors

The HUB transceiver operates in a direct sequence spread spectrum mode in the unlicensed 2.20 – 2.29GHz NTIA (National Telecommunication and Information Administration) approved AF frequency band. The reverse link data bit rate is 100kbps. Spreading will be accomplished using a 64 chip Walsh code that results in a chip rate of 6.4Mcps.

The reverse link carrier is transmitted from the HUB. This carrier is referred to as the pilot carrier. The pilot carrier is generated by taking an IF carrier, e.g., 326MHz and up-converting it to RF. Eight bits of address and control information is amplitude shift key modulated onto the pilot carrier.

The remote sensor modules decode address and control information from the pilot carrier. This transmission is referred to as the forward link. When commanded by the HUB to transmit, a remote sensor module mixes the pilot carrier with a 20MHz local oscillator. Sensor data is frequency shift key modulated onto the local oscillator. The output of the mixer is two spread spectrum carriers modulated with the sensor data. Both carriers are applied to the sensor antenna and transmitted back to the HUB. This transmission is referred to as the reverse link.

The power level of the pilot carrier leaking into the HUB receiver antenna from the HUB transmitter antenna is likely to be much higher than that of the return link signal. The HUB receiver front end must be designed to tolerate the leakage from the transmitter while receiving the reverse link. The front end must have sufficient 1dB compression point performance to accept the pilot carrier leakage without experiencing gain compression.

The HUB receiver down-converts the signal to a suitable IF frequency, e.g. 326MHz. The IF section must have the selectivity to demodulate the reverse link signal while rejecting the pilot carrier that is 20MHz away. This will require 2 IF SAW filter stages. The received signal is despread in the IF section by applying the same Walsh code used in the transmitter. After despreading, the IF bandwidth is reduced by filtering to a suitable value, e.g. 200kHz. The sensor data and clock is processed and extracted from the signal by a digital signal processor. The reverse link data includes synchronization and error correction bits. The receiver can take advantage of the diversity in the reverse link with the two transmitted signals 40MHz apart.

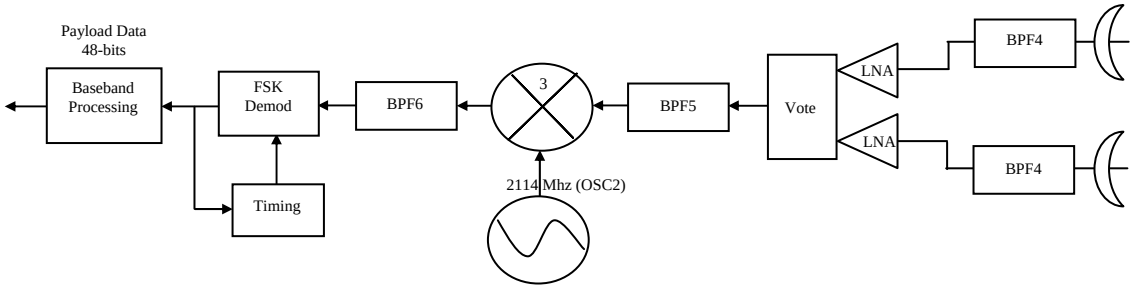


Figure 1. Block diagram of HUB transmitter forward link.

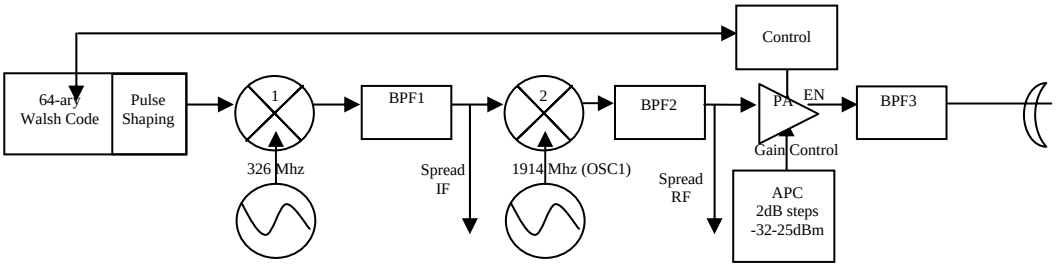


Figure 2. Block diagram of HUB receiver reverse link.

Data Rate Analysis

Each sensor cycle the will be composed of a 16 bit forward link data packet. The sensor rate will be 4 cycles per second, meaning each sensor will be accessed 4 times per second. Each hub may communicate with 8 sensors at a rate of 4Hz, which adds up to a hub cycle rate of 32 reads per second (8x4=32). This results in an average forward link data rate of 500bps. Therefore the instantaneous forward link data rate must be at least 500bps or greater.

Each sensor cycle will include 4 measurements of 12 bits each. The payload packet size is 48 bits and the channel packet size is 128 bits. This yields an average reverse link channel rate of 81.92kbps and a payload rate of 30.72kbps. As stated earlier, the instantaneous channel rate is 100kbps. Since the average channel rate is less than the instantaneous rate the data will be block bursty.

Forward Link Power Amplifier (PA)

The power amplifier will be designed to have 60dB of gain control. The transmitter will be designed with 3dB of margin to compensate for component tolerances and temperature effects. With this in mind the 60dB of gain control corresponds to a range of –32 to +28dBm under nominal conditions. There will also be a mechanism to limit the maximum transmitted power level to 25dBm. This limit is due to the 25dBm maximum input limitation on the transmitting antennas. The PA will use a tristate control as input for the forward link data and a 2-bit power up-down control for implementing the adaptive power control. The PA will remember the power level used for the last transmission to a particular sensor.

Reverse Link Base Band Processing Blocks

The frame synchronization block will find the synchronization preamble and align the interleaved and encoded data frame for the de-interleaver. A 23-bit barker word will be used for the synchronization preamble.

The de-interleaver will rearrange the data back into its original order and pass it to the decoder. A block interleaver will be used to interleave and de-interleave the data.

The Decoder will attempt to correct all of the errors and remove the error coding and correcting (ECC) bits. It will output the 48-bit payload (PL) data packet. A half-rate convolutional encoder with constraint length equal to 7 will be used in the sensor to encode the data. A Maximum Likelihood Viterbi Decoder will be used to decode the data.

The CRC Calculation will be used to calculate the reverse link frame error rate.
The received packet will have the following form:

Pilot Bits	23 sync bits	48 PL bits → 96 PL with ECC bits	9 bit CRC

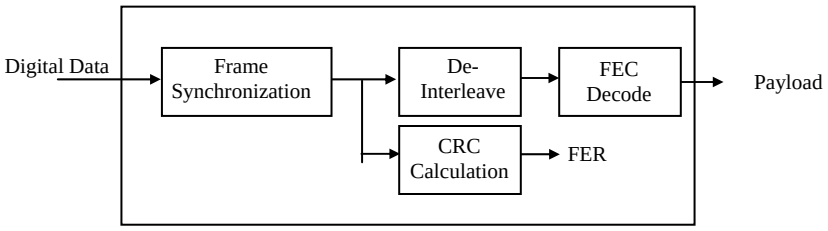


Figure 3. Block Diagram of baseband processing components

Reverse Link RF Frontend

The following blocks will reside in the receiver RF frontend.

FSK Demod (Non-Coherent): The FSK Demod will consist of four RF mixers and four integrate and dump circuits. The first input to all four mixers will be the baseband data. The second input to the first set of mixers will be the Delayed Spread IF (DSIF) signal. The second input to the second set of mixers will be the DSIF Signal shifted 80kHz down in frequency. A phase lock loop (PLL) timing circuit will drive the sample timing. The DSIF must be delayed to align its spreading code with the received spreading code.

FSK Binary Modulation Mapping (FSK separation is 80kHz)

0	19.920 Mhz
1	20.000 Mhz

Timing

The PLL timing circuit will be made up of a Phase Detector (PD), Loop Filter (LF), Voltage Controlled Oscillator (VCO), and Frequency Divider (FD).

Timing accuracy requirement is a quarter chip: $F_{reqd} = \frac{1}{R_b \cdot Chips \cdot 4} = \frac{1}{100kbps \cdot 64 \cdot 4} \cong 50\text{ns}$

Phase Detector- The PD will be implemented with a mixer.
Loop Filter- The LF will be implemented with a 2-order RC LPF.
Voltage Controlled Oscillator- The VCO will be designed to output a 100kHz clock.
Frequency Divider- The FD can be implemented with a standard D-type flip flop in a feed back configuration for dividing a clock.

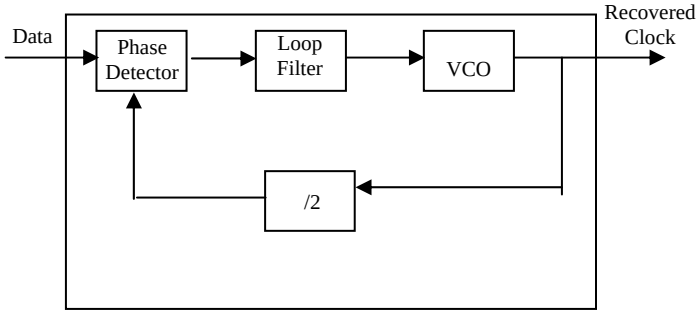


Figure 4. Timing recovery circuit

Mixer 3:

A 2.44Ghz doubled balanced CMOS even harmonic mixer will be used for this RF demodulation process.

Power Supply:	1.8V
Current Consumption:	1.71mA
RF Input Frequency:	2241 Mhz
LO Frequency:	1021 Mhz
Nominal Input Power:	-24dBm
DC Offset Cancellation @ 1% g_m mismatch:	86 dB
IIP2 @ 1% g_m mismatch:	40 dBm
Gain:	15.0 dB
Noise Figure (NF):	12.0 dB

FSK Mixer's:

The down converted IF signal will be simultaneously mixed with the spreading code and IF local oscillator to bring out the 20/19.92Mhz FSK signal.

Power Supply:	1.8V
Current Consumption:	1.21mA
RF Input Frequency:	346 Mhz
LO Frequency:	173 Mhz
Nominal Input Power:	-24dBm
DC Offset Cancellation @ 1% g_m mismatch:	86 dB
IIP2 @ 1% g_m mismatch:	40 dBm
Gain:	4.0 dB
Noise Figure (NF):	8.5 dB

Band Selection Filter (BPF4)

The bandwidth of the band selection filter is typically around the band of interest. We will make the bandwidth of this filter a little wider so that this filter is realizable, thus we will use 83.5Mhz. This gives us a Q-factor of about 30, for this filter (2240Mhz/83.5Mhz). The center frequency will be 2.24Ghz. The suppression only need to be large enough to ensure that the interference is suppressed to a point that it does not cause undesirable effects. To satisfy these specifications, BPF4 can be implemented using a passive LC filter. This LC filter can be combined with an input matching network in the LNA.

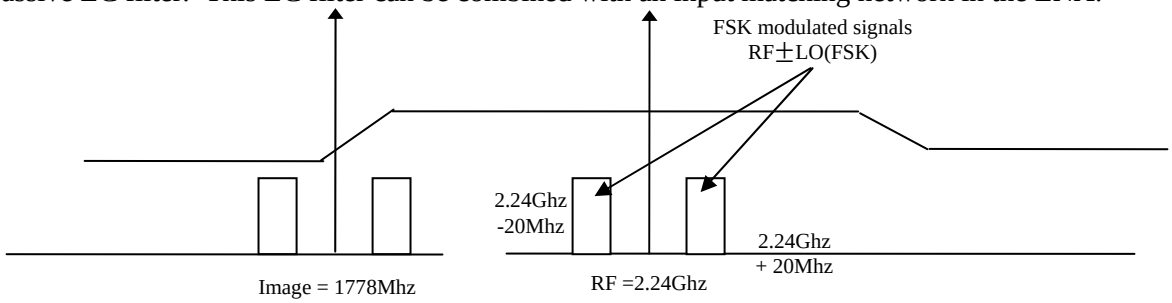


Image Reject Filter

During the down conversion process, the desired signal at w_{rf} , the radio frequency, and its image at w_{image} , the image frequency, are down converted to the same frequency of w_{if} , the intermediate frequency. Hence, the desired signal is corrupted. To avoid this interference we will design the image rejection filter (IRF) to suppress this image. Since the system has only one channel, the center frequency of IRF will be 2.24Ghz with a bandwidth (BW) of 83.5Mhz. This BW is smaller than necessary and can be increased if this filter is difficult to realize. The 83.5Mhz BW was chosen from a commercially available image rejection filter design. The image frequency is 652Mhz away from w_{rf} . IRF is typically designed using a surface acoustic wave (SAW) filter or ceramic filter. The output matching network of the LNA can also be used to provide some of this filtering.

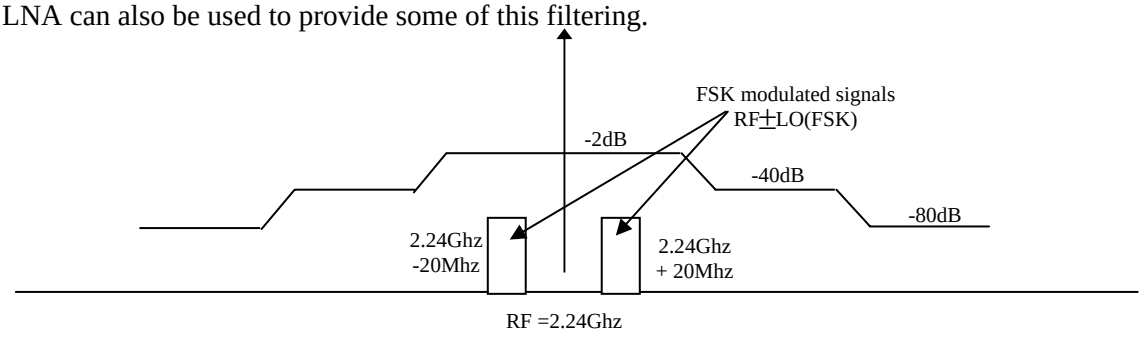


Figure 5. Image rejection filter parameters

Channel Filter (BPF6a and BPF6b)

The center frequency of these filters should be the intermediate frequency plus and minus the sensor FSK LO, 326Mhz ± 20Mhz, respectively. The bandwidth will be the RF BW of the spreading code, 12.8Mhz. The Q-factor for this filter should be about 26 (326Mhz/12.8Mhz). This filter may be designed with a surface acoustic wave filter, continuous time active filter, or ceramic filter. Filter 6 will be two separate filters, one filter for each FSK LO. We will use an equal gain combining scheme to combine these two signals to improve our SNR.

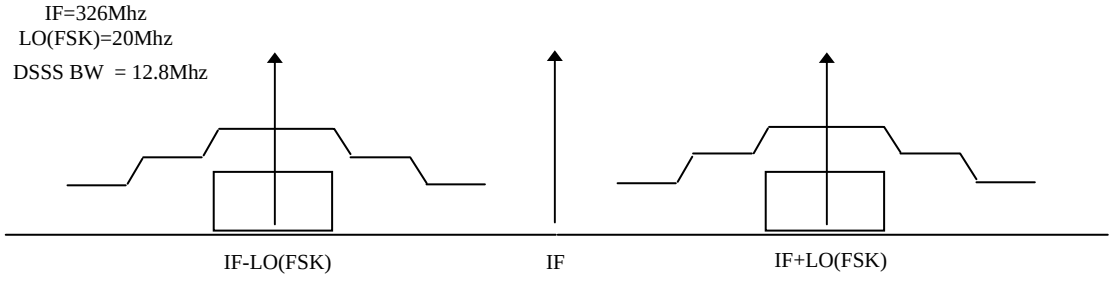


Figure 6. Channel filter parameters

Other Results

Technology Transfer/Intellectual Property

Not at this time.

Publications Resulting from Research

Not at this time.

Benefits to Commercial Sector

The methods and circuit design techniques being developed are applicable to all RF transceiver designs, including those in the commercial sector. Furthermore, companies involved in design of analog/mixed-signal circuits, integrated circuits (ICs), and communications systems will be able to use the research outcomes to specify requirements of new circuits, understand tradeoffs, and optimize a system architecture.

References

[1] Bosco Leung, VLSI for Wireless Communication, Upper Saddle River, NJ: Prentice-Hall, 2002

[2] Leon W. Couch II, Digital and Analog Communication Systems, 5th Edition,Upper Saddle River, NJ: Prentice-Hall, 1997

[3] John G. Proakis, Digital Communications, 4th Edition, Boston Burr Ridge, MA: McGraw Hill, 2001

[4] Bernard Skylar, Digital Communications, 2nd Edition, Asia, Pearson Education, 2001

[5] Steve Fahley, "Report on Channel Characterization and Interference in an Aircraft", Seattle, WA Boeing, 2002

[6] Alper Demir and Jaijeet Roychowdhury, "Modeling and Simulation of Noise in Analog/Mixed-Signal Communication Systems," presented at the *IEEE Custom Integrated Circuits Conference,* 1999

[7] Huaping Liu, Vinod Venkatesan, Curt Nilsen, Ron Kyker, and Mario E. Magana, "Performance of Frequency Hopped Non-coherent GFSK in Correlated Rayleigh Fading Channels," *ICC* 2003

[8] Jack H. Winters, "Optimum Combining for Indoor Radio Systems with Multiple Users," *IEEE Transactions on Communications,* Vol. COM-35, NO. 11, Nov. 1987

[9] S. A. Charles, E. A. Ball, T. H. Whittaker, and J.K. Pollard, "A Channel Sounder for 5.5 Ghz Wireless Channels," *IEEE* publications, 2002

PROJECT 3

CIRCUIT DESIGN TECHNIQUES FOR LOW-VOLTAGE, ANALOG CMOS INTEGRATED CIRCUITS FOR EXTREME ENVIRONMENTS

Prof. Benjamin Blalock (University of Tennessee) with David Hogue (Boeing)

RESEARCH TIME PERIOD: One year
RESEARCH FOCUS: AFRL Task Areas 2 and 6: Standard Cell/Topologies in Radiation-Hardened SOI and Ultra Low-Power Technologies.

Figures and Tables

Abstract

Interest in radiation hardening by design is continuing to increase. Factors motivating this include the high cost of radiation-hardened (rad-hard) semiconductor processing compared to standard commercial processing, as well as the technology lag (typically at least one generation) of rad-hard processes behind commercial manufacturing. In addition, the continued scaling of CMOS technology places severe voltage constraints on mixed-signal systems, prompting the need for new analog circuit design techniques to realize systems-on-a-chip on very deep submicron processes. Thus, two great challenges currently facing rad-hard mixed-signal design are the lack of available circuit-level hardening by design techniques for analog, and the need for robust analog circuit design techniques compatible with the low voltage constraints of scaled CMOS processes. This work has 1) compared three analog biasing techniques, including the fixed inversion coefficient biasing scheme, showing how they vary over a range of total ionizing dose (TID), and 2) developed a low-voltage pipeline ADC design incorporating hardening-by-design techniques.

Project Description

Applications such as space exploration and radiation sensor control circuitry require their electronics to be resistant to radiation. When bulk and SOI MOSFETs are irradiated, their electrical characteristics suffer in numerous ways based upon the total ionizing dose (TID). Decrease in the threshold voltage of MOSFETs can occur due to trapped charge in the interface and gate oxide, however it was shown that for gate oxide thicknesses less than 10nm, this effect was drastically decreased [1, 2] as CMOS technology scales further into the deep submicron regime. In SOI though, there is also a shift in the back gate threshold voltage for the same reasons. There is an increase of leakage current due to gate-induced drain leakage (GIDL) and charge buildup on the MOSFET sidewall oxide isolation [3]. Another important TID effect is that the subthreshold slope of the MOSFET will increase due to the charge buildup in the front (and back) oxide interfaces [4], hence the MOSFET will exhibit a degraded turn-on characteristic. There will also be a decrease in the channel mobility due to trapped charge at the oxide interface [3], which causes a decrease in transconductance. So far the only methods proposed to alleviate some of the TID effects are special layout techniques or altering the fabrication process. Seemingly most studies done on

the effects of radiation on analog circuits deal with commercial off-the-shelf amplifiers or application specific amplifiers, however none of these studies looked at it from the standpoint of bias circuits. Therefore we have characterized the constant current, constant g_m and fixed inversion coefficient (IC) bias techniques over different radiation levels. The advantage of biasing a MOSFET at a fixed inversion coefficient is that one will actually be controlling the MOSFET's transconductance efficiency, which is defined as the ratio of the transconductance to drain current. By controlling a MOSFET's transconductance efficiency it is possible to minimize variations in both drain current and transconductance, while neither one actually remains constant. The TID effects on each of the bias circuit schemes are demonstrated.

Another aspect of this research addresses the issue of voltage scaling in analog and mixed-signal design. Low voltage analog and mixed-signal circuits have many applications for space and defense, such as battery-powered compact low-mass soldier systems. This issue is addressed by investigating body-driven analog design techniques developed at UT. In addition to addressing low voltage circuit design, this research investigates the effects of radiation on circuits designed using body-driving techniques. Body driving is a circuit design technique in which the MOSFET body terminal is used as a signal input [5]. This technique allows robust CMOS mixed-signal systems to operate from a supply voltage of about 1V or less, representative of the low voltage constraints being imposed by CMOS process scaling in the immediate future. In bulk CMOS, typically only the pMOS device can be body driven, unless a twin-well process is used. Complementary body driving is readily viable in partially-depleted SOI CMOS. The low supply voltage is possible when body driving because there is no threshold voltage associated with the body terminal. This design technique optimizes dynamic range in voltage mode signal processing circuits. This is particularly important as shrinking supply voltage reduces the available swing available for voltage signals and if TID effects induce a shift in threshold voltage.

To test the body-driving design technique, an operational amplifier was fabricated in a Honeywell 3.3-V/0.35-µm PD-SOI process (MOI5). UT received the amplifier in May 2004. Initial testing showed full functionality, including proper operation from a power supply voltage ranging from 1 V to 3.3 V, rail-to-rail I/O over the entire power supply range, and a 10-MHz gain bandwidth product. UT has anticipated that circuits designed using this technique will enable ultra-low voltage, high-performance circuits in a wide range of analog/mixed-signal applications. The proposed effort includes irradiating this operational amplifier to characterize the TID effects on the circuit. To the best of our knowledge, this effort is the first time that TID effects on body-driven analog circuits will be demonstrated.

A 1.2 V pipeline ADC was also proposed. Instead of fabricating the ADC in MOI5 as originally proposed, an opportunity to fabricate the ADC in an IBM 130-nm bulk CMOS process was taken advantage of thanks to a synergistic effort through DARPA's Rad Hard By Design program in which UT is participating. This allowed the research to be expanded to include hardened-by-design (HBD) layout techniques, but body driving is not available in this process. According to "A survey of high performance analog-to-digital converters for defense space application [6]," there is a shortage of pipeline ADCs using HBD layout techniques. This work may be one of the first low voltage pipeline ADCs developed utilizing HBD layout techniques. The ADC will be fabricated in two forms: 1) using both traditional layout and 2) using HBD layout techniques. The ADC has a target resolution of 10 bits and a sampling rate of 1 MSps. The impact of TID effects on the ADC performance will be explored. In addition to the complete ADC, we plan to have standalone copies of the intrastage sub-blocks available on the test chip so that we may isolate the TID effects of the complete ADC from the TID effects of the individual intrastage sub-blocks.

Research Results and Discussion

To test the variation of the three different biasing scheme with increasing TID, DC characterization was performed for both nMOS and pMOS devices at 100 kRad, 200 kRad, 500 kRad, 700 kRad, and 1 MRad doses with a dose rate of 31.5 kRad / min. Per Boeing's suggestion for ITAR/Export Control ITAR compliance, however, only test results up to 500kRad are included in this report. The nMOS was sized at 8.0µm / 0.5µm × 16 (i.e., 16 gate finger device), and the pMOS was sized at 10.0µm / 0.5µm × 32 (i.e.,

32 gate finger device), both fabricated in Honeywell's commercial 0.35-μm process (MOI5). From that data, technology current (I_O), normalized technology current (I_O(TID) / I_O(100 kRad)), subthreshold slope (n), threshold voltage (V_T), and η (= g_{mb} / g_m) variations were extracted. Table 1 summarizes the maximum percent variation for the radiated MOSFET parameters. All of the device characteristic shifts due to radiation are relatively small, and they should not cause any major performance problems for a well-designed circuit. From the technology current data, it is possible to determine how the constant current, constant g_m, and constant IC biasing schemes will vary an operational amplifiers g_m and slew rate due to TID. Table 2 summarizes the extracted percent variation shifts of the three biasing techniques. Depending on the most important design specifications of an op-amp, it would appear that the constant current and constant g_m nMOS input pair op-amps would have the least variation over the applied TID range. However, it should be noted that the constant current and constant g_m results are ideal, and the constant IC results are from the actual bias circuit. The constant current and constant g_m bias circuits usually depend upon the absolute value of a resistor (whereas the constant IC does not), which will degrade the shown values. Other than the relatively low shifts due to TID in g_m and slew-rate for the op-amp biased with the constant IC bias generator, it should be noted that it is possible to develop a near perfect constant IC generator making it a good choice for TID resistant circuits. The data shown in Tables 1 and 2 are for SOI MOSFETs (MOI5) and represent our complete study of the radiation performance of different bias techniques on SOI. When we receive our IBM chips, we will complete our study of radiation performance of different bias techniques on bulk CMOS.

Table 1. Parameter summary for the radiated MOSFETs

	NMOS (% Variation)	**PMOS (% Variation)**
I_O	+ 0.61 %	– 7.8 %
Normalized I_O	+ 0.61 %	– 7.8 %
N	+ 1.4 %	+ 0.71 %
$\lvert V_T \rvert$	0 %	+ 2.20 %
η	0 %	+ 0 %

Table 2. Summary of the operational amplifier parameter shifts due to TID

	g_m (% Variation)	**Slew-rate (% Variation)**
Constant Current	– 1.2 % (nMOS) – 2.9 % (pMOS)	0 %
Constant g_m	0 %	+ 1.7 % (nMOS) + 4.1 % (pMOS)
Constant IC	– 0.76 % (nMOS) – 8.4 % (pMOS)	+ 0.61 % (nMOS) – 7.8 % (pMOS)

The body-driven operational amplifier was also irradiated at the same TID levels as previously described. Figure 1 shows the open-loop gain of the body-driven op-amp for the different TID levels with V_{DD} set at 1 V. The results show that there is a decrease of approximately 5 dB in the open-loop gain and around 10% for the bandwidth from pre-irradiation to 500 kRad.

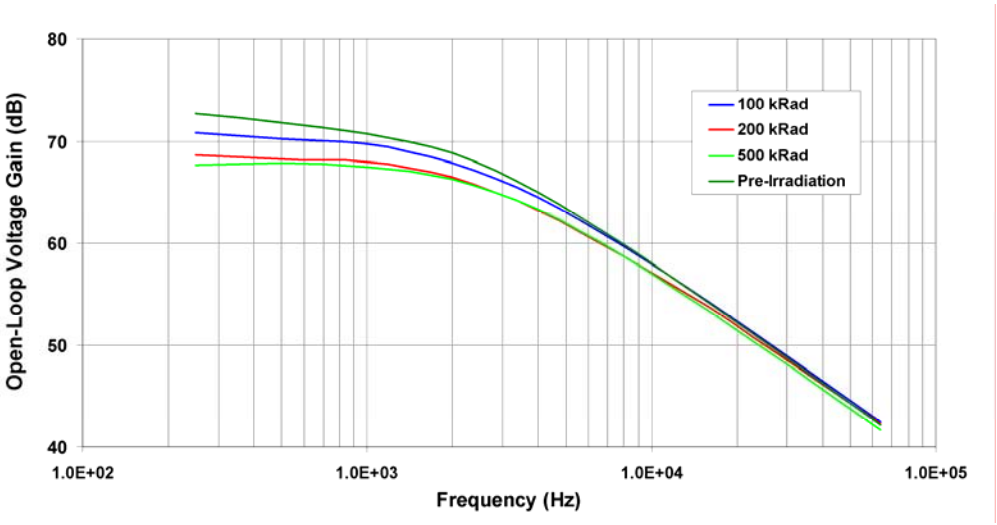


Figure 1. Open-loop gain measured results for the irradiated body-driven op-amp

An improved body-driven operational amplifier design was irradiated at the same TID levels. Figure 2 shows the open-loop gain of the op-amp for the different TID levels with V_{DD} set at 1 V. The results are shown for 2 chips. The results show that the open-loop gain of the op-amps shifted by 1.73 and 4.3 dB. Figure 3 shows the PSRR of one of the improved op-amps vs. V_{DD}. The data points are shown with a 4th order polynomial fit line, and are consistent with the PSRR measurements of three other chips. The results from these two op-amps show that body driving is a good option for ultra-low-voltage analog circuits in high-radiation environments.

The pipeline ADC chip is described in the following *Test Chips* section. Test results showed that the ADC using traditional layout techniques has 10-bit linearity. The ADC using annular gate switches has missing code problems. The test results are shown in the *Test Chips* Section.

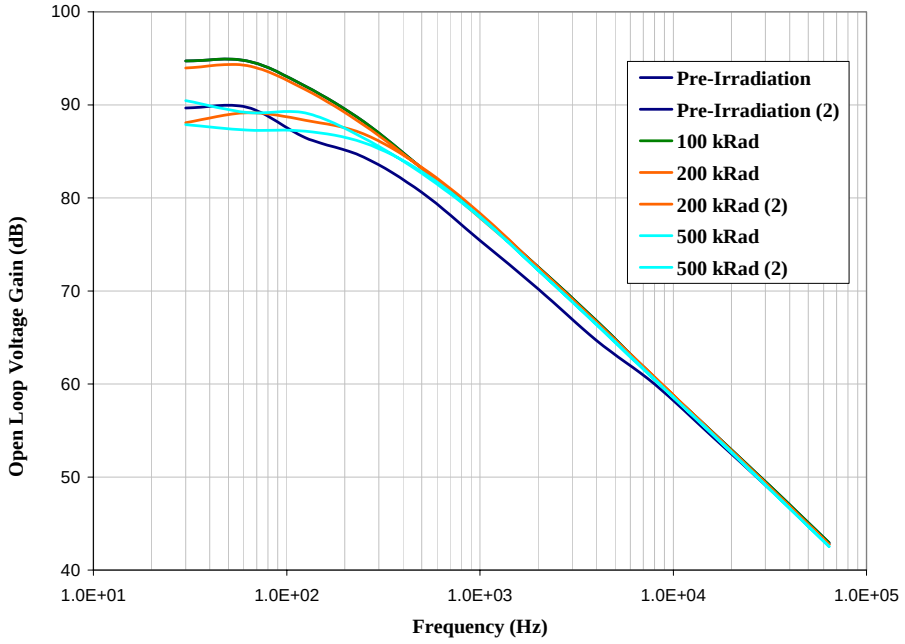


Figure 2. Measured open-loop gain for an improved body-driven op-amp design biased at 1 V

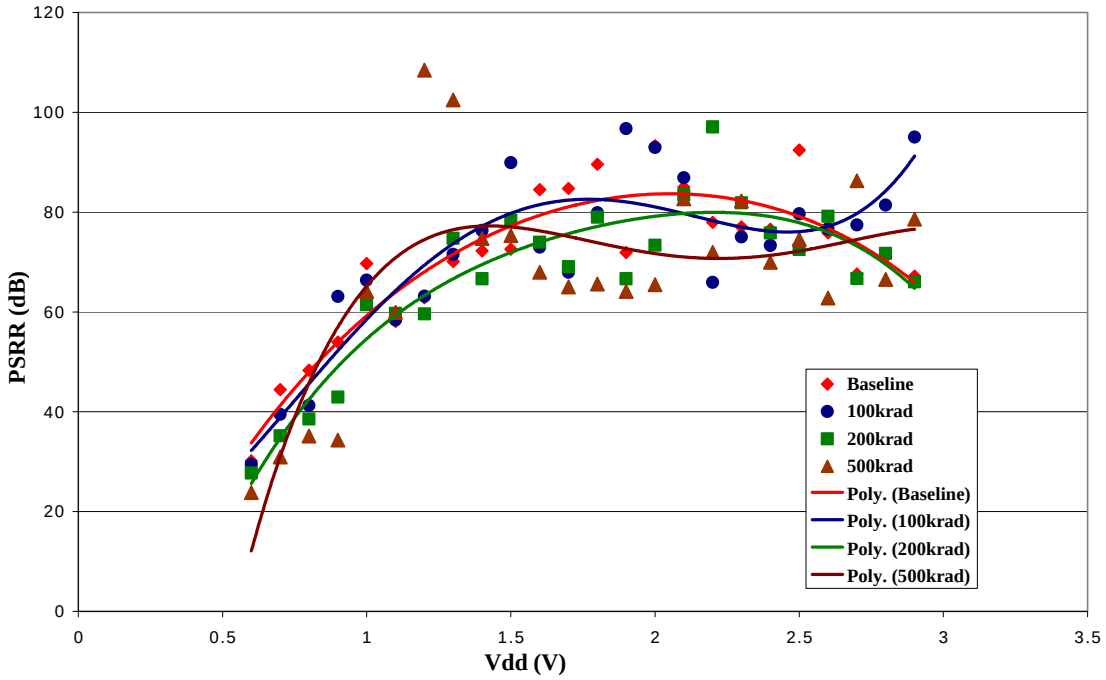


Figure 3. PSRR vs. V_{DD} for the improved body-driven op-amp

Test Chips

The 1.5 bit per stage ADC architecture was tested by building a prototype using discrete commercial components. The ADC prototype was functional and achieved 5-bit accuracy. The architecture of a single pipeline stage is shown below in Figure 4. Each stage has 2 digital outputs. The fully integrated ADC has nine stages, giving a total of 18 bits. Redundant bits will be removed using an error correction algorithm, which will be implemented using an off chip FPGA. The FPGA error correction program has been written and tested.

Simulations of the pipeline ADC show that the design is functional with 10-bit resolution. The maximum expected sampling rate is 2 MHz. The sub-ADC contains fully-differential comparators with switched-capacitor input differencing circuits. The comparators have differential inputs, reference voltages, and outputs. The simulated resolution and offset are sufficient for a 10-bit pipeline ADC. Additionally, large comparator offsets can be tolerated because they are corrected by the bit redundancy. The maximum simulated error in the output of the sub-DAC is 5μV.

The total area of the ADC chip is 3 mm by 3 mm. The layout is shown below in Figure 5. Two versions of the layout were submitted. One version uses HBD layout techniques. In this version, annular gate switches and numerous guard rings were used. These techniques should lessen TID effects and help to prevent single event effects. The circuits were fabricated in the IBM 8RF CMOS process. Both versions of the layout use gate lengths greater than 0.5 μm to provide good device matching while insuring low gate edge leakage (due to irradiation).

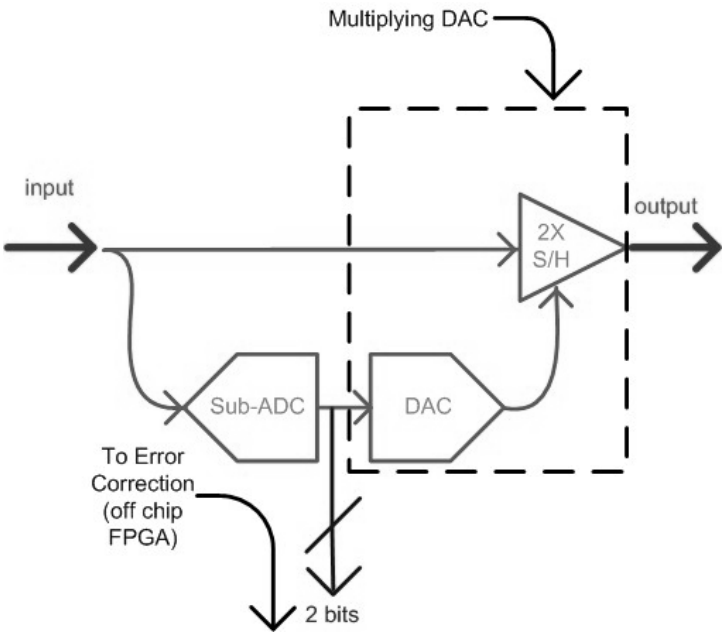


Figure 4. Single pipeline ADC stage architecture

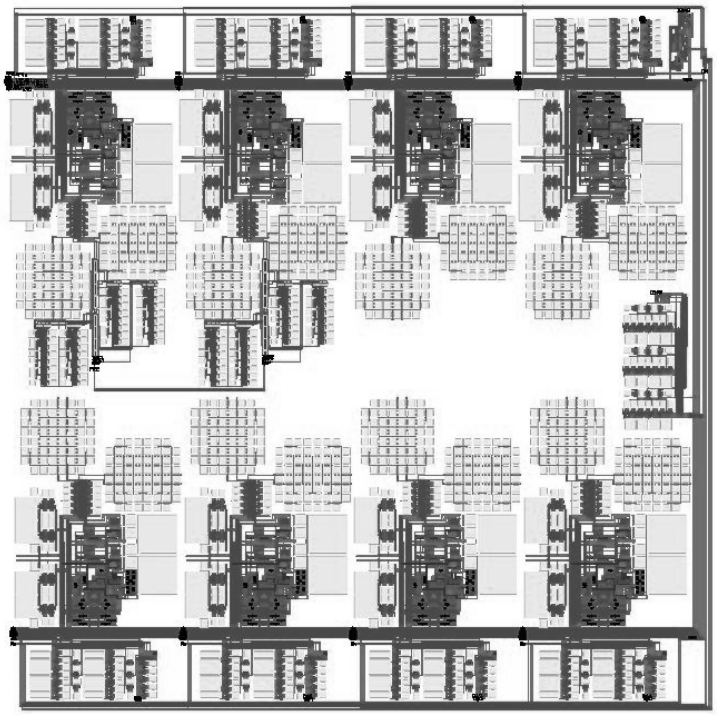


Figure 5. Pipeline ADC layout

Test results show that the non-HBD version of the ADC has 10 bit linearity. The DNL is shown in Figure 6 below. The DNL was measured using a sine wave histogram code density test. The ADC response to a sine wave input is shown in Figure 7 below.

There is a missing code problem with the RHBD version of the ADC, so there is not 10-bit linearity over the entire input range. The effect of the TID test can be measured on the RHBD version by observing the change in Differential Non-Linearity (DNL) in the linear regions of the input range. Figure 8 below shows the TID test results for both versions of the ADC. This figure shows that the ADC's DNL degrades with total dose, and the change in DNL for the RHBD version is less than that for the non-RHBD version.

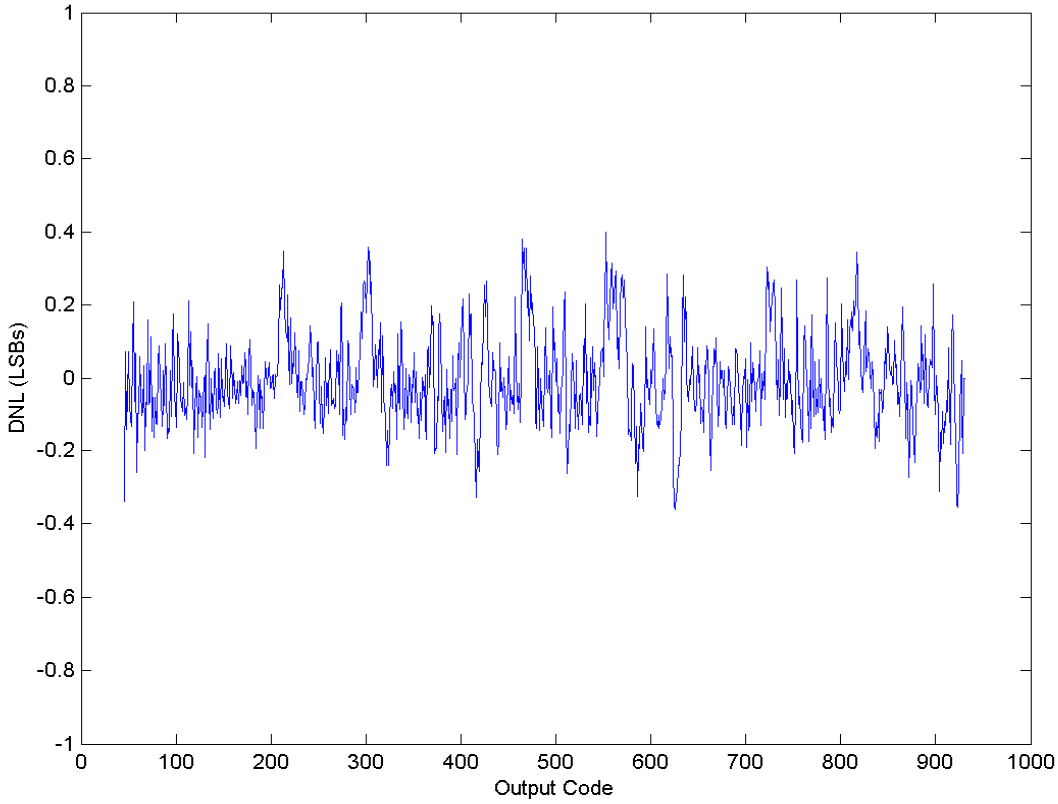


Figure 6. DNL test result (1 MHz clock)

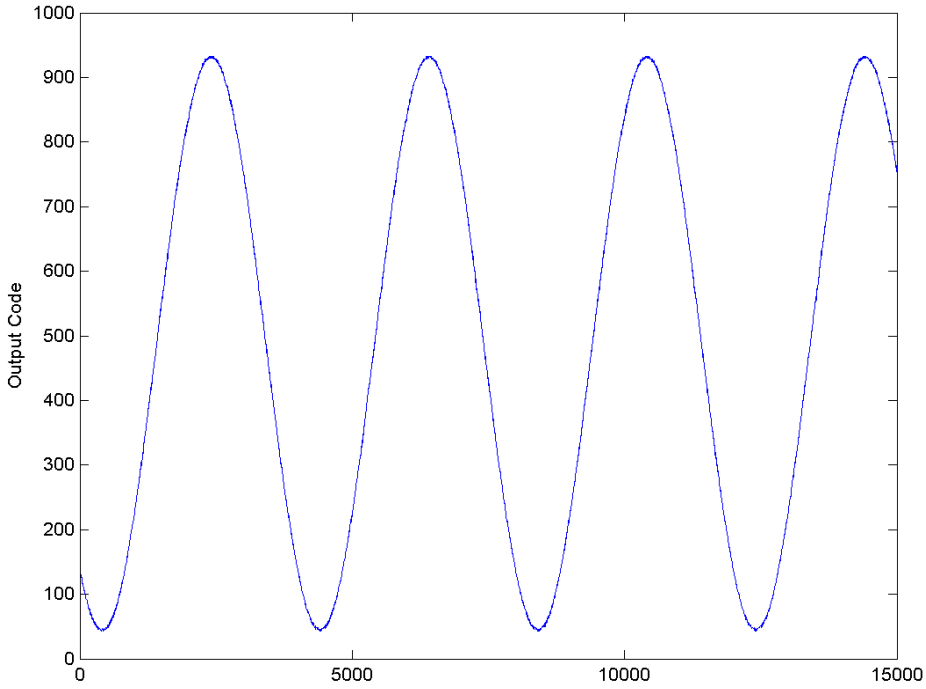


Figure 7. ADC Response to sine wave input

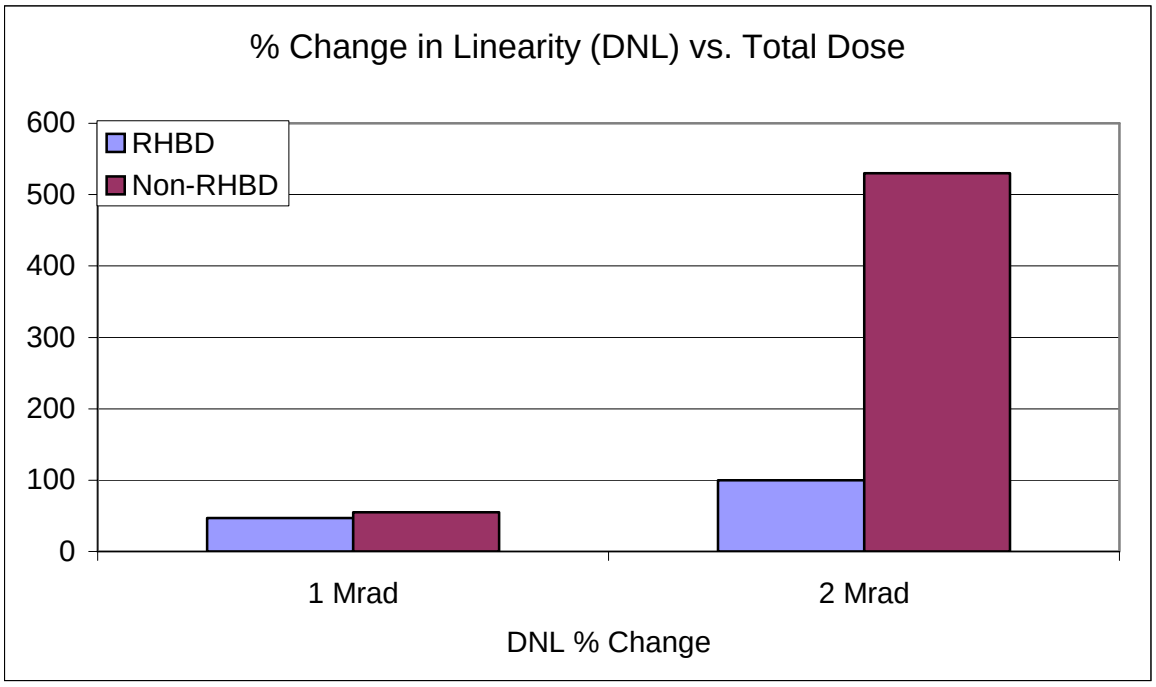


Figure 8. Change in ADC DNL vs. total dose

Other Results

Technology Transfer/Intellectual Property

Successful technology demonstration of this work includes UT's comparative study of analog biasing schemes toward a circuit-level HBD technique for extreme environment CMOS analog design, the use of HBD techniques to design and implement a 1.2 V pipeline ADC, and the measurement and characterization of TID effects exhibited by body-driven low-voltage analog circuits. Results will be presented at a follow-on CDADIC meeting and in any publications based on this work. Technology transfer should provide to AFRL, Boeing SSED and CDADIC partners a detailed description of the key circuits developed during this effort and the related design techniques. Boeing is developing a demonstration plan and identifying technology transfer opportunities, which they plan to discuss with AFRL and CDADIC leadership in an ITAR/Export Control compliant forum.

Pending the outcome of this research, patents and/or invention disclosures will be handled in manner compliant with CDADIC and UT procedures. Our industry partner will be included in IP discussions and their advice and guidance will enhance the potential IP development resulting from this work.

Publications and Presentations

A *NSREC 2005* paper submission describing the radiation test results of the body-driven op amp is currently being considered. In addition, the HBD version of 1.2 V pipeline ADC developed in this work should be applicable to *NSREC 2006*.

Benefits to Commercial Sector

While radiation immune electronics have a narrow commercial market, the proposed low-voltage analog design effort is certainly applicable to virtually any CMOS mixed-signal low-voltage system, including the battery-powered applications driven by the ever-increasing demand for portable devices.

UT originally developed the fixed inversion coefficient biasing technique for wide temperature range analog circuits needing to operate in extreme environments. All analog circuits, whether military, space, or commercial need optimum bias, and this technique promises to establish and maintain the desired bias point (selected level of inversion for critical devices) over variations in the environment. This technique does not add to the development cost, but should enhance the quality of the product by ensuring that a desired 'window' of performance can be maintained. Applications needing mixed-signal systems that should benefit from this technique include spacecraft to Jupiter's moons and to Mars, down-hole electronics, robots for nuclear power industry, *in situ* sensors in colliders, remote weather monitoring stations, and hazardous area sensors.

References

[1] N.S. Saks, M.G. Ancona, J.A. Modolo, "Radiation effects in MOS capacitors with very thin gate oxides at 80ºK," *IEEE Transactions on Nuclear Science*, vol. NS-31, no. 6, pp. 1249-1255, Dec. 1984.

[2] N.S. Saks, M.G. Ancona, J.A. Modolo, "Generation of interface states by ionizing radiation in very thin MOS oxides," *IEEE Transactions on Nuclear Science*, vol. NS-33, no. 6, pt. 1, pp. 1185-1190, Dec. 1986.

[3] H.L. Hughes and J.M. Benedetto, "Radiation Effects and Hardening of MOS Technology: Devices and Circuits," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 500-521, June 2003.

[4] D.C. Mayer, "Modes of Operation and Radiation Sensitivity of Ultrathin SOI Transistors," *IEEE Transactions on Nuclear Science*, vol. 37, no. 5, pp. 1280-1288, May 1990.

[5] B. J. Blalock, P. E. Allen and G. A. Rincon-Mora, "Designing 1-V op-amps using standard digital CMOS technology," *IEEE Transactions on Circuits and Systems II*, vol. 45, no. 7, pp. 769–780, July 1998.

[6] Merkel, K. G., Wilson, A.L., "A survey of high performance analog-to-digital converters for defense space applications," *IEEE Aerospace Conference Proceedings, 2003*, Volume: 5, March 8-15, 2003.

PROJECT 4

ADAPTIVE REGULATION AND LOGIC FOR SUBTHRESHOLD CIRCUITS

Prof. Lawrence T. Clark (Arizona State University) with Intel

RESEARCH TIME PERIOD: One year
RESEARCH FOCUS: AFRL Task Areas 4 and 6: System-on-a-Chip Design
and Ultra Low-Power Technologies.

Figures and Tables

Abstract

Low power system-on-chip (SOC) designs are increasingly important to diverse applications ranging from hand-held cell phones and PDAs, medical devices such as pacemakers, to military applications including wearable computing and communications, and space systems. Most of the IC's aimed at such applications must cope with limited battery capacity and thermal capability. Present commercial system-on-chip (SOC) designs have dozens of supply voltage domains for power savings, SRAM stability, and independent power down capabilities. Based on present trends, even more independent supplies can be expected in the future. This allows lower power, but invites the difficult problem of generating the supply voltages either at the board or die level.

The research here is developing radiation hardened by design CMOS circuit techniques to allow very low operating voltage, i.e., both in and/or near subthreshold operation with on-die voltage down conversion and high efficiency regulation. Integration with large mixed signal systems, including noise effects, will be investigated. The design, which will be a stand-alone die with digital circuits operating at subthreshold power supply voltages and integral on-die regulation, will include radiation hardened by design approaches. The low voltage (and variable voltage) operation will allow simulation and measurement of the hardening efficacy vs. voltage using the final fabricated die. This will also allow determination of radiation effects on very low voltage operation.

Project Description

A key aspect of very low voltage operation is the lack of commercially available regulators with high resolution and very low output voltage. To avoid a large increase in board level components and minimize system level bill of materials, a monolithic solution is desirable. The proposed project is concerned with development of a monolithic, radiation hardened by design, high efficiency switched capacitor DC to DC voltage down converter. The down converter is implemented fully on die with no external components, using intelligent digital control. Output voltage is adjustable and adaptable to system requirements and or die variation. The latter can be due to static variation such as fabrication differences or to dynamic variation such as environmentally induced variation due to temperature or total ionizing dose effects, e.g., increased leakage or transistor parameter variation. The resulting on-die down converter/regulator will utilize one input power supply voltage of 1.2 V, determined by the target process, and the output voltage will be programmable between 0.2 and 0.6 V. It is expected that the intelligent control will result in lower power supply ripple and more accurate tracking of the target voltage. The overall DC to DC converter block diagram is shown in Figure 1. Voltage controlled oscillators will be used as the analog to digital conversion function for the regulator feedback. This will necessarily include time averaging of the input voltage, increasing rejection of supply ripple and eliminates the need for high resolution comparators.

Very low operating voltages not only allow the square law active power savings, but can substantially lower transistor leakage by taking advantage of drain induced barrier lowering (DIBL) effects. In addition to saving about 20x in I_{off}, a 1V supply reduction can reduce gate oxide leakage by as much as 100x.

Impact of extreme voltage scaling (into the subthreshold regime) on radiation hardened by design techniques is explored. This includes both the impact of very low voltage operation on hardening and on the speed and power of a real design. The resulting die will be a mixed signal design, allowing exploration of effects on analog circuits such as VCO's operating at very low voltage as well as on digital circuits. One challenging aspect of the design is level shifting circuits interfacing the low voltage to high voltage domains. The wide range in operating voltages will not only allow a broad power and performance range for the digital circuits, but will also allow subsequent generation of radiation hardness vs. operating voltage curves for the chosen hardening techniques. The use of an advanced 0.13 μm process technology allows the prototype devices and the measured results to be directly applicable to future low power devices. The load circuit (besides the intelligent controller) will be a subthreshold operation microcontroller. This design will not be rad-hard, so the test chip will include facilities for external loading and measurements. These would be required regardless for full characterization of the test chip.

Research Results and Discussion

The overall system architecture is shown in Figure 1. Here, a monolithic system with integrated voltage down conversion supplies a very low supply voltage, e.g., 250 mV V_{DDL}, to the digital microcontroller operating in subthreshold. All control logic is also to operate in subthreshold and was to be hardened using RHBD techniques. For the target 0.13 μm process V_{DDH} = 1.2 V.

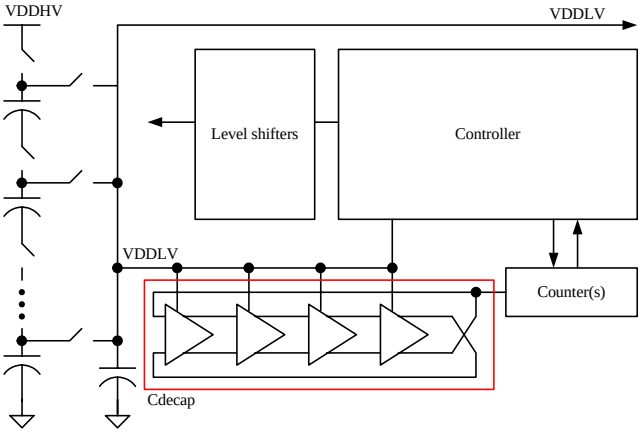


Figure 1. Adaptive regulator/down converter block diagram.

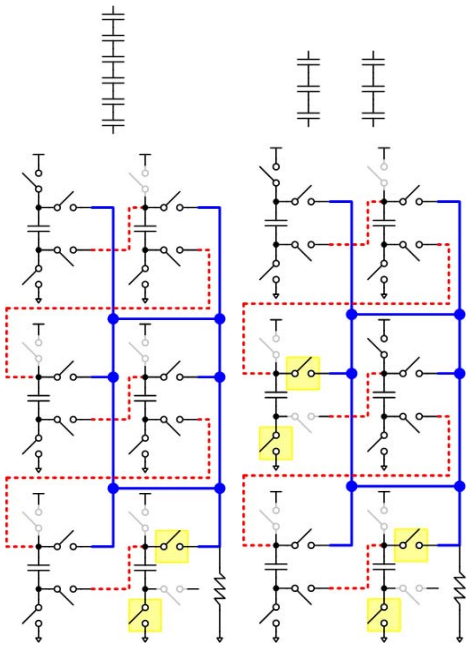


Figure 2. Down converter circuit in two of the possible configurations.

Due to the short project timeframe, the design was to be built and submitted to fabrication but it was assumed that the project could not complete in that time. The project was broken into pieces to take advantage of early silicon opportunities. Some have been tested but for some the testing is still in progress. At this point the nearly all of the constituent components of the entire system have been fabricated. Testing is under way, including TID and ion beam testing. Work on the complete microcontroller is ongoing. The smaller portions of the design, which have been completed and taped out are:

- Subthreshold memory tested to be capable of read and write operations at a minimum V_{DD} of nearly 200 mV at room temperature.
- A 32 entry subthreshold register file which is SEU protected by DICE cells and parity (to detect SET induced read errors) TID and latchup hardened by annular gates and guard rings. Simulation shows the design is protected even below 200 mV. Silicon is awaiting packaging.
- A non-subthreshold, RHBD 32x32 register file with provision for external EDAC, Minimum V_{DD} = 0.4 V.
- A robust subthreshold to non-subthreshold level shifter circuit. This design is RHBD. Functional and TID testing is complete.
- An RHBD voltage controlled oscillator for the feedback loop. Simulations have shown that this triple redundant design does not produce glitches due to SET.
- A monolithic programmable output, switched capacitor voltage down converter. This RHBD design can scale to different current demands by ganging multiple blocks in parallel. Silicon test is pending.
- Test structures to measure capacitances and transistor behaviors for calibration of the designs to the silicon. This structure has been tested to be very linear as expected.

Switched Capacitor Down Converter

Linear down conversion has been proposed for generation of supplies on die, but the efficiencies are low, on the order of 50% and diminish as the difference between the external and down converted voltage increases. Partially on die schemes allow higher drive buck-boost converters including discrete inductors.

While the former approaches are suitable for very low power standby modes, greater efficiency can

be obtained by switched capacitor techniques. The latter approaches are not sufficiently integrated for this application. An adaptive, configurable, switched capacitor (SC) down converter architecture has been developed that allows multiple output voltages (see Figure 2). Since the highest efficiency is obtained only at the exact integer values of series capacitors, the circuit can be reconfigured to different numbers from two to six. Figure 2 illustrates two of the possible configurations, delivering a voltage at 1/6 and 1/3 of the input voltage for peak efficiency. Switches in grey are always turned off, while switches in yellow are always on, and are used to configure the output voltage. The other switches are clocked to provide the output voltage. The switching frequency will be variable to adjust to differing power demands at low ripple. All switches are implemented as CMOS pass gates with annular NMOS and full guard-rings.

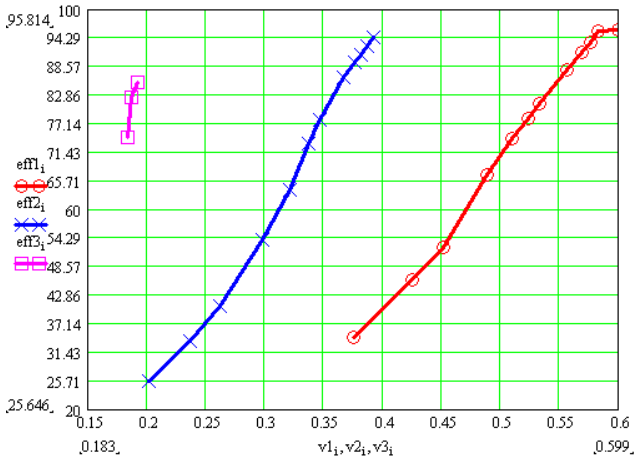


Figure 3. Down-converter efficiency vs. output voltage for three configurations.

The efficiency, obtained by circuit simulation of the circuit, comprises Figure 3. An analytical model has been developed and matches well. While the efficiency drops off rapidly as the required output voltage drops away from the capacitor voltage divider value, the total system power is still reduced, due to the quadratic dependence of the digital system power. Hence, while the highest efficiency can be supported only at a few values, overall system power can still be saved at low regulator efficiencies. The reduction of efficiency is due to linear-like behavior as the higher voltage is switched to a lower voltage. Since the converter will be controlled digitally, and the digital controller will in turn, be powered by the regulator, an appropriate startup circuit will be designed. The down-converter silicon is back and the test board is under construction.

Level Shifter

Level shifting from the subthreshold to above threshold voltage domain was expected to be a difficult part of the project. A simple circuit was developed, which starves the PMOS load transistors in a classical differential level shifter to achieve a wide operating range. The level shifter is fully RHBD. Simulation results are shown in Figure 4. The level shifter has been measured fully functional on silicon (see Figure5).

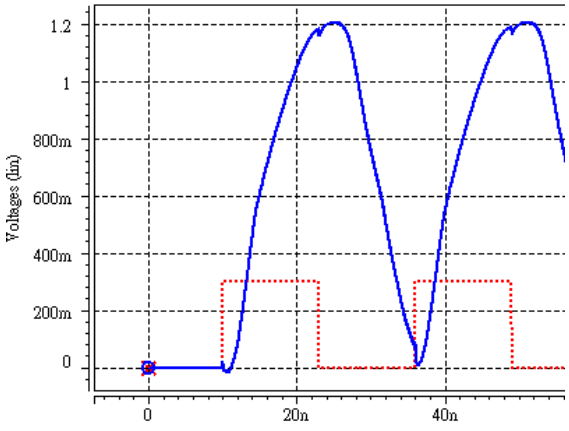


Figure 4. Level shifter operation with input and VDDL at 0.3 V and output at 1.2 V.

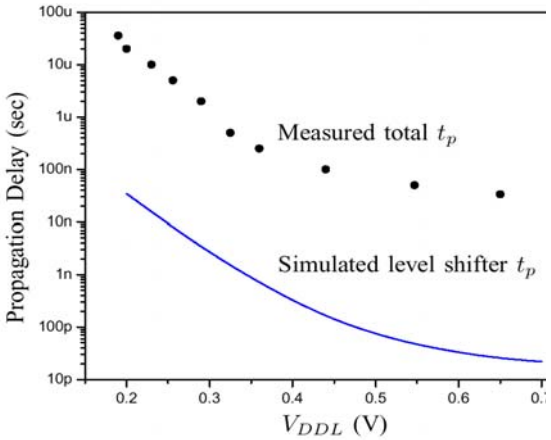


Figure 5. Level shifter measured delay path on chip vs. simulation. The extra delay is due to the subthreshold memory in the path. V_{DDH} is always 1.2V.

Subthreshold Memory and RHBD Register File

An area efficient very low voltage memory has been developed with as little as 1 nJ energy dissipation per operation as shown in Figure 6. The memory design is 512x12, with an extra bit per word for parity protection. The approach is more area efficient than previous designs with similar minimum operating voltage and demonstrably higher operating speed—approximately 30x faster than a previously published design as shown in Figure 7. The memory uses a new write scheme to avoid feedback contention during write and a register file type readout with modifications to support low voltage operation by limiting read bit-line (RBL) fan-out. This technique is also applicable to above threshold V_{DD} operation and can be applied to high performance designs. The primary issue that this circuit configuration addresses is variation between the keeper and pull-down devices, which is increasing generally. A single differential bit provides a self-timed signal to control the keeper devices. This signal can also be used to gate clocks for lessening readout power. Minimum memory operating voltage is limited by write bit-line (WBL) fan-out and two designs with differing WBL fan-out have been developed. A new self-timed feedback keeper scheme for domino has also been developed. The scheme, which alleviates feedback contention due to transistor variation, is applicable to high-performance as well as low-voltage digital integrated circuits. The memory will be used in the microcontroller design. 106-216 mV minimum operating VDD has been measured for one sub-bank as shown in Figure 8. This design has been measured fully functional at 216 mV operating at 28 kHz.

RHBD Feedback VCO: As shown in Figure 1, a VCO is to be used for feedback to the controller as

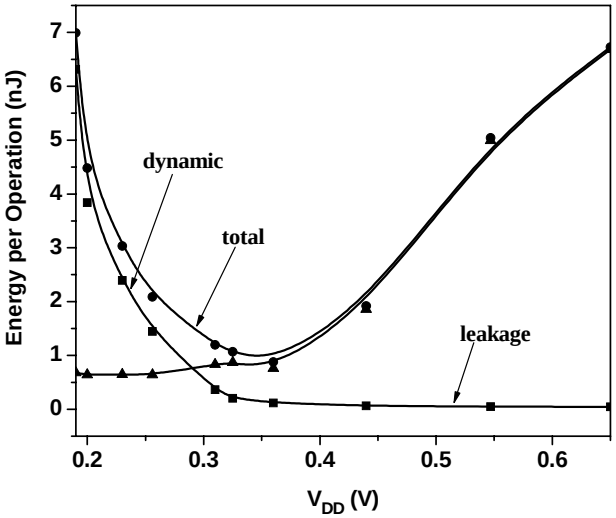


Figure 6. Energy per operation vs. V_{DD}. The circuit is operating at the maximum frequency at a each voltage.

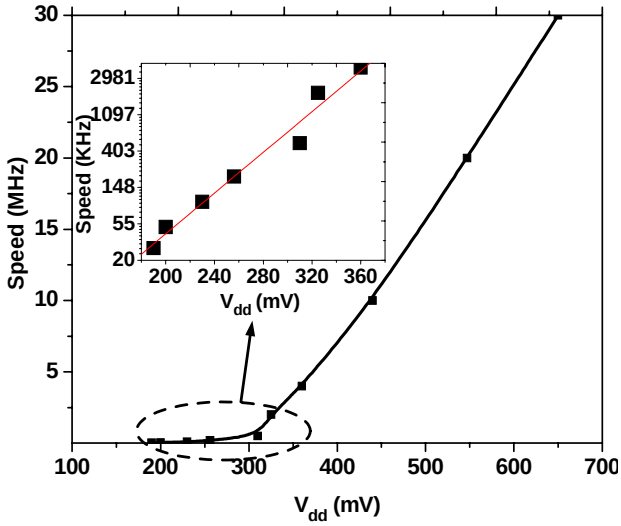


Figure 7. Measured read speed vs. V_{DD} for the subthreshold memory. The write speed is faster.

an analog to digital converter block that does not require any precision analog circuits. Since this VCO will control a digital counter, it is necessary to avoid glitches or erroneous clocks due to SET events. A VCO with highly linear response, using three interlocked majority gate style CMOS stages has been designed. The basic design is shown in Figure 9. The circuit is relatively unperturbed by simulated heavy ion strikes. Since each input A, B, or C, does not contribute substantial "on" resistance when driving the load, i.e., the current starve devices dominate, the impact of SET on phase error is minimal.

RHBD Subthreshold Register File

For the final subthreshold RHBD microcontroller design, a 32 entry, two port (one read and one write) design was taped out 6/30/05. This design utilizes spatially separated DICE cells for SEU immunity, SET on the readout path is provided by parity protection. The output circuits developed for the subthreshold SRAM described above were used in this design. The triple redundant decoders of the design mentioned above were used without modification. Power consumption of the design is shown to be well below 1 μW as shown in Figure 9. This design was done using annular NMOS gates. However, our recent measurements indicate that this is not necessary when operating in low voltage. The intrinsic leakage reduction, and low NMOS gate biases mitigates TID even in fully conventional transistor layout, as shown below.

Test Chips

Test chips were fabricated on the IBM 0.13 μm process through the trusted foundry program. A common pad ring was developed and modified to support both the all copper metallization 8LM and the aluminum top metal BICMOS8RF process. Both processes were used for test chips as available. The fabricated test chips and circuits supported for this research:

Test chip tape out 2/25/05 (CMOS8LM):

- Subthreshold memory capable of operating at a minimum V_{DD} of 160 mV at the typical process corner and room temperature. Not hardened, but since proven to be TID hard up to V_{DD} = 0.5 V.
- A non-subthreshold, RHBD 32x32 register file ready for external EDAC, Minimum V_{DD} = 0.4 V.
- The subthreshold to non-subthreshold level shifter. This design is RHBD.
- An RHBD voltage controlled oscillator for the feedback loop. Simulations have shown that this triple redundant design does not produce glitches due to SET.

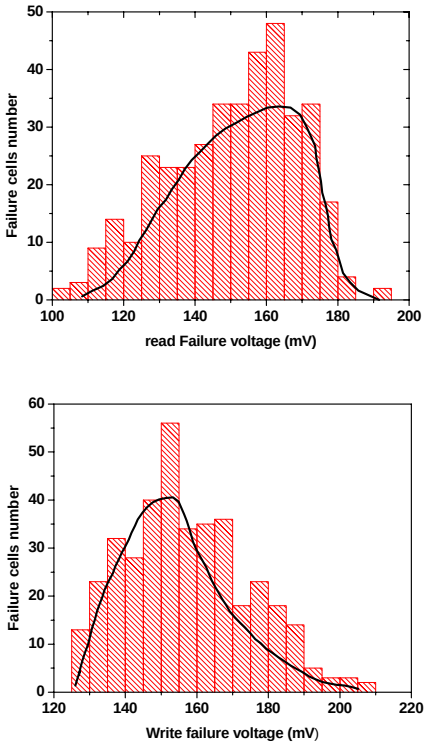


Figure 8. Measured sub-bank minimum read and write voltages. The design techniques were effective at producing excellent low voltage robustness.

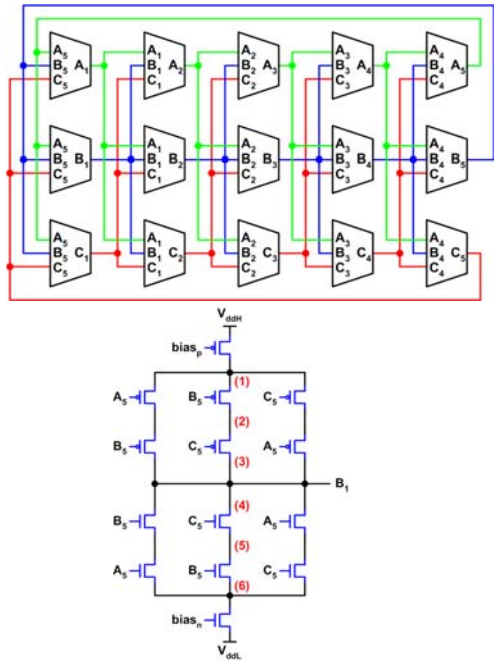


Figure 9. RHBD SET immune VCO circuit (top). Each block is comprised of the current starved majority gate as shown at the bottom of the figure.

Test chip tape out 3/30/05 (BICMOS8HP):

- A monolithic programmable output, switched capacitor voltage down converter. The design can scale to different current demands by ganging multiple blocks in parallel.

Test chip tape out 6/30/05 (CMOS8LM):

- A 32-entry subthreshold register file which is SEU protected by DICE cells and parity (to detect transient errors) TID and latchup hardened by annular gates and guardrings. Simulation shows the design is protected even below 200 mV.

Included on all test chips:

- Test structures to measure capacitances and transistor behaviors for calibration of the designs to the silicon.

The common pad ring for the test chips utilizes all RHBD hardened circuitry. All test chips have identical circuits. A representative test chip is shown in Figure 10. The power supplies are fully gridded on M5-M8 to ensure power supply integrity, speed assembly, and avoid dummification. The subthreshold memory is supplied by a separate power supply to avoid issues when SEE testing. A similar or identical approach was used on the other test chips.

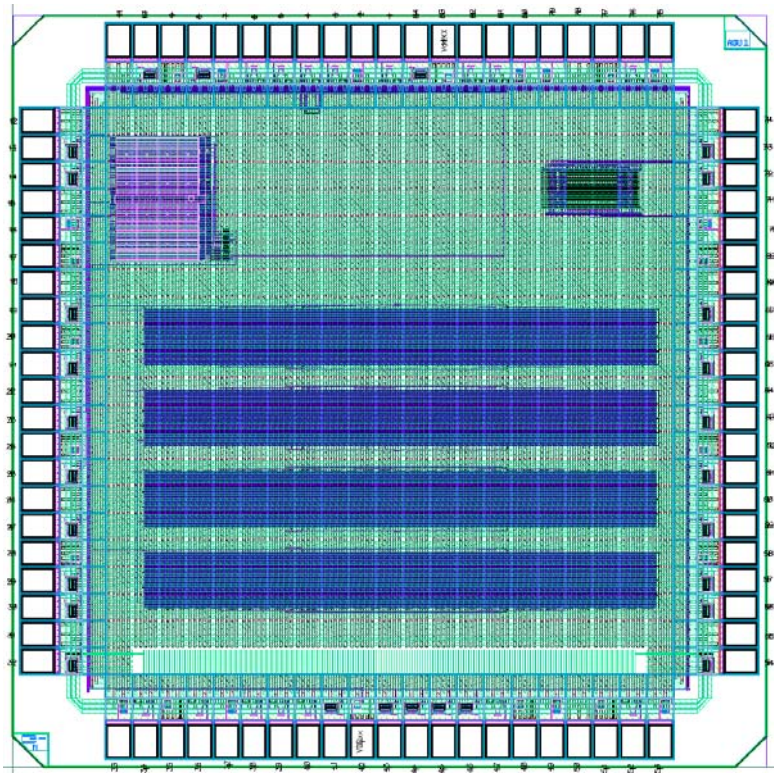


Figure 10. The 2/25/05 test chip. The subthreshold memory is at upper left and the RHBD register file is at upper right. The other structure is a set of four shift registers using novel differential temporal latches. At the bottom is an inter-digitated metal-metal capacitor test structure for the S-C downconverter.

Test chip tape out 6/30/05 (CMOS8RF):

- RHBD DICE Cell register file and level shifters. Different well spacings are supported to determine the range of ion strike collection vs. operating voltage.
- The programmable output S-C DC to DC downconverter. This design is fully hardened.

TID testing has been performed at ASU using the Gammacell. Ion testing has begun on some other but not these projects—No SEL has been observed on those. Pre and post TID measurements of the hardened VCO design are shown in Figure 11. The use of annular NMOS gates clearly mitigates TID induced leakage. However, as shown in Figure 12, this is also mitigated extremely well by low voltage operation. Measured subthreshold memory I_{DD} pre and post-radiation at 500 kRad shows that bias at 0.5 V is almost as effective as annular gate design. Thus, ultra-low power design may allow completely conventional layout to be used. It should be noted that the low voltage reduces the IDD about 2x, due to the relatively low DIBL on the target process. We expect that SEL will not be an issue, since a 0.5 V supply cannot support one, let alone two V_{BE}'s to allow latchup. Consequently, completely conventional design may prove to be TID hard when operated at low V_{DD}.

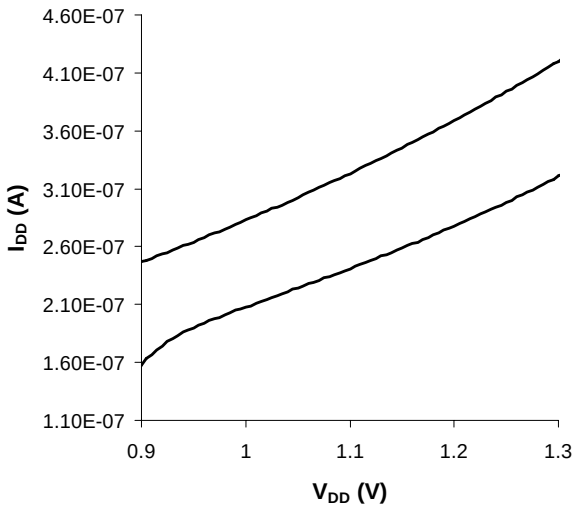


Figure 11. I_{DD} vs. V_{DD}.of the RHBD feedback ring oscillator measured pre-and post radiation. The leakage increase is negligible (upper line is 500 kRad, lower line is pre-TID test.

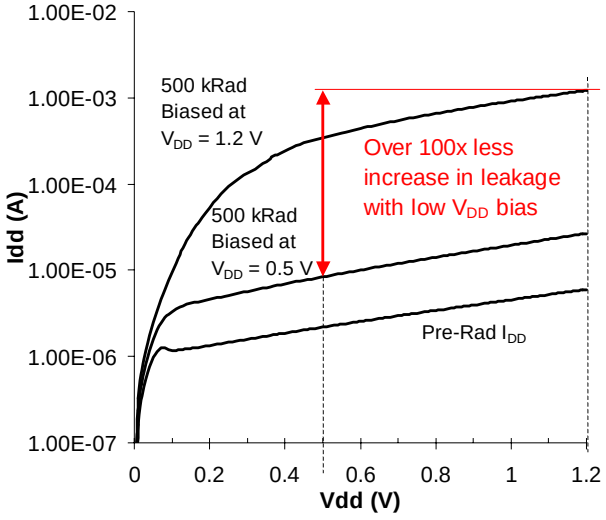


Figure 12. I_{DD} vs. V_{DD}.of the subthreshold memory measured pre-and post radiation. The leakage increase when operating at V_{DD} = 0.5 V at 500 kRad dose is 100x less than at 1.2 V.

Other Results

Technology Transfer/Intellectual Property

Presentations have been made at Intel in Portland, OR, and Chandler, AZ. Tom Mozdzen, Franco Ricci, Shay Demmons, Mike Kelly, and Neil Deutscher of Intel visited ASU for meetings. This pertained only to non-RHBD subthreshold circuit design aspects. The PI visited with members of the AFRL/SEAMS center in Albuquerque in the Fall to discuss all aspect of this and another project.

No patent filings are anticipated at this time.

Resulting Publications and Presentations

Papers developing and analytical model to guide subthreshold design were published at ICCD and in IEEE Circuits and devices, two are in review for IEEE JSSC and IEEE TCAS-II regarding the subthreshold memory and level shifter, respectively. We are working on a submission for NSREC'06 which describes the TID hardness and design for very low power space system IC's

Benefits to Commercial Sector

Commercial industrial applications include wearable, hand-held, and cellular communications IC's. This research is complimentary to an Intel Corp. funded project investigating subthreshold logic circuits for cellular communications SOCs. Military applications include ultra-low power modes for space applications, wearable and portable electronic systems. The expected results are development of practical micro-power conversion and regulation circuits, using subthreshold digital control that should be applicable to other mixed signal systems, e.g., data converters.

PROJECT 5

SOI-CMOS RADIATION TOTAL DOSE DEVICE MODELS FOR SPACE ENVIRONMENT APPLICATIONS

Prof. R. Bruce Darling (University of Washington) with Fong Shi (Boeing)

RESEARCH TIME PERIOD: Two years
RESEARCH FOCUS: AFRL Task Areas 1 and 5: System Circuit Modeling for VLSI Circuit Implementation and Predictive Radiation Effects Models.

Figures and Tables

Abstract

The rapid development of advanced electronic systems for space is now requiring faster turn, more complex integrated systems to be developed which rely increasingly upon circuit simulation. However, at present there do not exist any SPICE MOSFET models which accurately predict device behavior over the radiation exposure conditions of space. This project will develop predictive SPICE MOSFET models which include the effects of total dose device degradation arising from long term radiation exposure. These models will be modified versions of the industry standard Berkeley BSIM3 model which has been recently extended to the BSIM3SOI model for partially-depleted silicon-on-insulator (SOI) process technologies.

The effects of long-term total dose radiation exposure will be introduced into the BSIM3SOI model by additional front-end parameter calculations which will adjust the carrier lifetimes, trapped charges, carrier mobilities, and MOS threshold voltage to account for a given radiation dose. The models will be validated against measured total ionizing dose (TID) measurements made on generic partially-depleted SOI MOSFETs obtained from a state-of-the-art defense vendor. The models will also be implemented in a higher-level VHDL-AMS language which can be compiled for specific circuit simulators using the MCAST model compiler tool developed at the University of Washington.

The resulting validated SPICE MOSFET models will provide a circuit and system level simulation tool to be used for VLSI circuit implementations and will provide predictive radiation effects modeling to be carried out on these designs. These models can find immediate use in the simulation of other projects which involve the design of specific circuit modules.

Project Description

This project shall methodically develop improved device models for Honeywell's MOI5 SOI CMOS process over a much wider temperature range 65ºC to +200ºC and will include the effects of transient ionizing radiation on these device characteristics. Current SPICE MOSFET models for circuit design are inaccurate over the wider temperature range of space applications and do not address radiation effects. The BSIM3SOI SPICE model will be extended to include the effects of wider operating temperatures and ionizing radiation, making this model suitable for the simulation of circuits in space environment applications.

Research results and discussion

From the preceding year's work, improved device equations for temperature had been developed and validated. The electron and hole mobility equations were derived from the fundamental semiconductor carrier scattering mechanisms for acoustic phonons, 190K optical phonons, 630K optical phonons, and ionized impurities. The temperature dependence of the energy bandgap and the electron and hole effective masses were used to calculate the electron and hole mobilities as a function of both temperature and doping. The current electron and hole mobility equations are now valid over the range of −65ºC to +200ºC. These were mathematically compacted into a more efficient set for computations within the device models, and these mobilities agree well with the published literature values. In addition to carrier mobility, the more accurate energy bandgap, mobility, and intrinsic carrier concentration have been used to create more accurate device equations for the pn-junction leakage currents and MOSFET threshold voltages. All of these improved temperature dependencies have been integrated into the BSIM3SOI native C-code. Dynamic self-heating effects can be simulated using the built-in temperature node of the BSIM3SOI device model.

The NASA AE8 and AP8 electron and proton radiation flux models were obtained in their native C-code form and were used to calculate total dose exposures from various orbits that intersect the Van Allen radiation belts. The NASA SHIELDOSE model was also obtained to calculate the radiation penetration through aluminum enclosures surrounding the electronics payload. From published results on the measured effects of total radiation doses on SOI MOSFET performance, semi-empirical models were developed, and these models were compared against the direct calculations provided by AE8, AP8, and SHIELDOSE.

It is well known that one of the primary effects of ionizing radiation is to create oxide charges which can shift the threshold voltage of a MOSFET. Electron-hole-pairs which are generated in the SiO_2 gate oxide layer are the ultimate origin of this radiation-induced oxide trapped charge. While electrons are fairly mobile in the conduction band of SiO2, holes have a mobility of about 10^7 times less, and tend to reside in the oxide for much longer periods of time. When a small bias is applied across the gate oxide, generated holes will slowly drift toward the Si/SiO2 interface, where they can fall into interfacial traps. This positive oxide trapped charge causes a reduction in the threshold voltage for both NMOS and PMOS devices. The magnitude and polarity of the electric field in the SiO_2 gate oxide layer determines the rate at which generated holes drift to the interface. After the radiation induced generation rate ceases, some holes will de-trap from the interface and cause the threshold voltage to relax back toward its original value. The rate of this relaxation is also determined by the magnitude and polarity of the electric field inside the gate oxide, and also by the ambient device temperature. Data from the literature suggests that the net effect of the gate oxide electric field and the device temperature is related to the overall integrated time-temperature product, while other data shows that the integrated effect should more properly use the Arrhenius temperature dependence of the hole release energy from the traps. Our developed radiation equations allow either formulation to be used. Counteracting the oxide charging effect is the effect of radiation damage on the oxide and the Si/SiO_2 interface which increases the number of possible trapping and defect centers. Data from the literature suggests that the number of defect states caused by the radiation is proportional to the radiation dose, up to about 1-10 Mrad(Si). In principle, either the oxide charging or defect creation can dominate, although in practical space environments, oxide charging effects have tended to predominate. The overall radiation physics equations for the gate oxide radiation effects have included both oxide charging and additional creation of oxide defect states, and both of these processes can be fully parameterized with suitable weighting coefficients.

After the radiation physics equations had been developed for the BSIM3SOI model, the equations were then implemented into the device code itself in two methods. First, the native C-language code for the BSIM3SOI model was directly modified to implement the new radiation physics equations. Because of the inherent complexity of the BSIM3SOI model, this activity took many months to complete to produce a model which did not introduce any new mathematical or physical bugs. In a second method, the model compiler work of Prof. Richard Shi at the University of Washington was used to write the

BSIM3SOI model in VHDL-AMS which could then be compiled directly into any one of many possible circuit simulators, such as HSPICE, SPICE2G, or Spectra. Prof. Richard Shi's group had already developed the basic BSIM3 model in VHDL-AMS, so the radiation effects model equations only needed to modify this existing software code.

To validate the radiation effects model, total ionizing dose (TID) tests were performed on sample parts supplied by a generic SOI-CMOS vendor. These test devices were typical of those in a 3.3 Volt, 3.5 GHz partially depleted SOI foundry process with an 85 nm gate oxide. From a process monitoring die which contained a number of different MOSFET structures, smaller die were laser cut, each containing either 5 NMOS {G1, G2, G5, G6, G7} & {G9, G10, G13, G14, G15} or 5 PMOS {M1, M2, M5, M6, M7} & {M9, M10, M13, M14, M15} devices. The devices were chosen to give a selection of W/L ratios. The NMOS devices had W/L ratios of {2/0.35, 20/0.35, 5/0.35, 20/0.5, 20/0.8} and the PMOS devices had W/L ratios of {2/0.5, 20/0.35, 5/0.5, 20/0.5, 20/0.8}. Each die containing 5 MOSFETs was packaged into a gold-ceramic 14-pin DIP package with the help of Boeing. Boeing also wired up a custom test card for use with the TID testing and packaged devices.

TID testing was carried out at the Boeing Radiation Effects Laboratory (BREL) in South Park, WA. A gamma cell was used to expose the devices to successive 50 krad(Si) doses of gamma radiation from a Co^{60} source. This source produced a rate of about 60 rad(Si)/second, and was composed of the usual 1.173 MeV and 1.332 MeV gamma ray photons. Each dose involved an exposure time of 13 minutes and 55 seconds. Four successive doses were performed on both the NMOS and PMOS devices. Interleaved with each exposure were three parametric characterization measurements which were performed on an HP-4145B semiconductor parameter analyzer. Output characteristics, transfer characteristics, and threshold voltage extraction was performed on each of the 10 devices at each point in the dose profile. All data was recorded on the HP-4145B internal disk drive. During each 50 krad(Si) exposure, each of the devices was biased into the off-state, but a drain-to-source potential of 3.3 VDC was applied. The overall testing procedure followed the MILSTD 883E method 1019.5 protocol. The overall TID testing procedure produced completely characterized devices with successive radiation doses of {0, 50, 100, 150, and 200} krad(Si).

TID test results on the transfer characteristics are shown in Figure 1 and Figure 2 for a few typical NMOS and PMOS devices (G13, M10). Threshold voltage shifts caused by radiation dose are shown in Figure 3 and Figure 4 for the NMOS and PMOS devices. In both cases, the primary effect of the ionizing radiation is to shift the threshold voltage downward by an amount which approximately proportional to the dose.

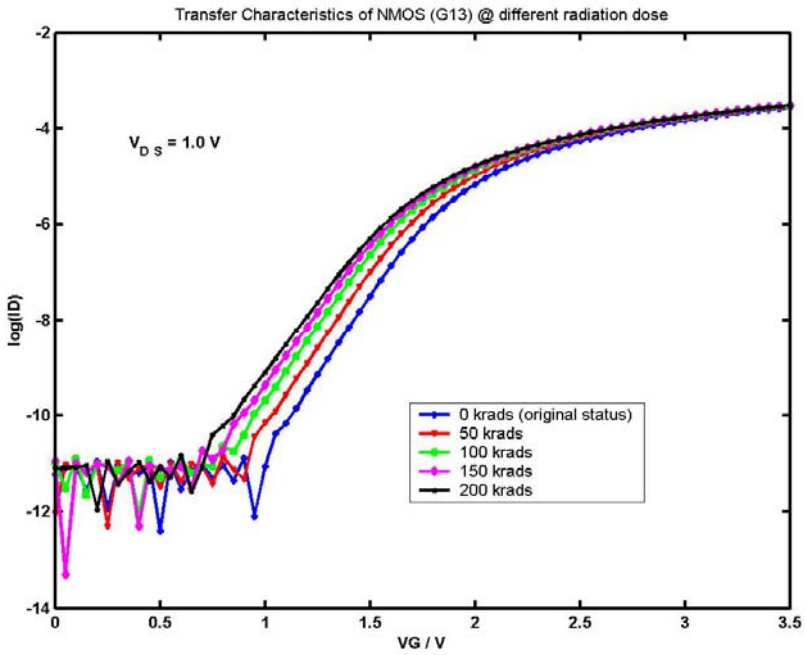


Figure 1: Total ionizing dose (TID) of NMOS.

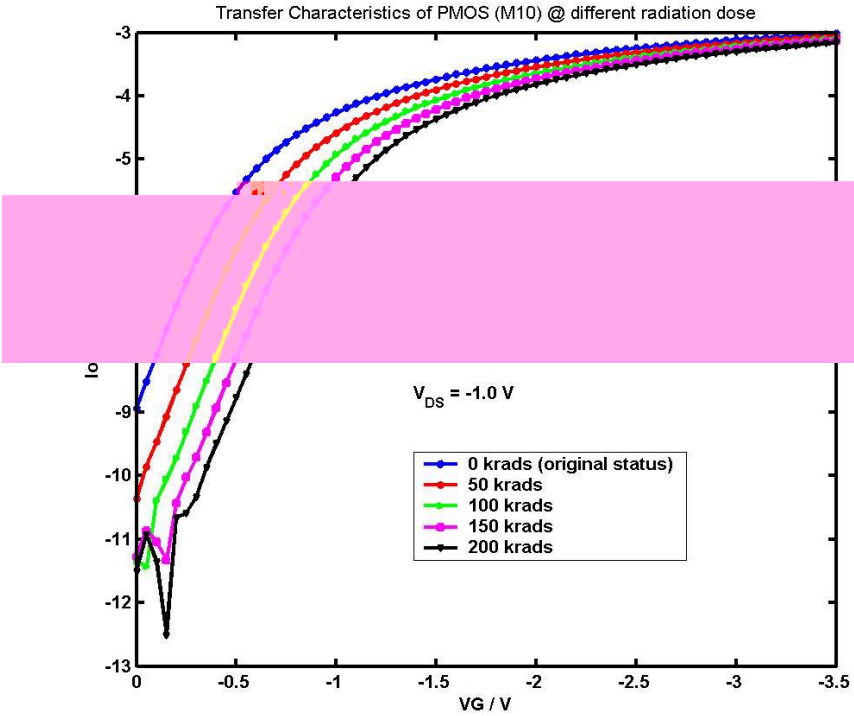


Figure 2: Total ionizing dose (TID) of PMOS.

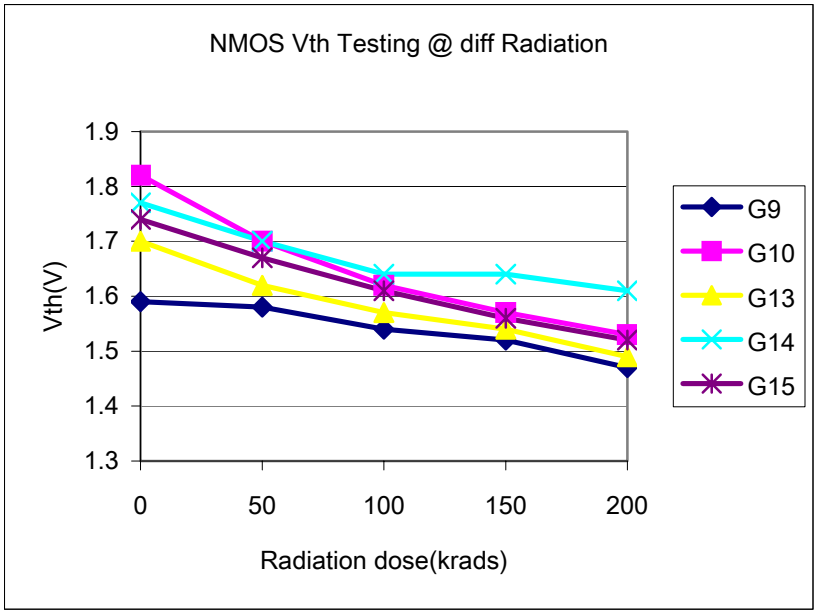


Figure 3: Total ionizing dose (TID) of NMOS with varying radiation dose.

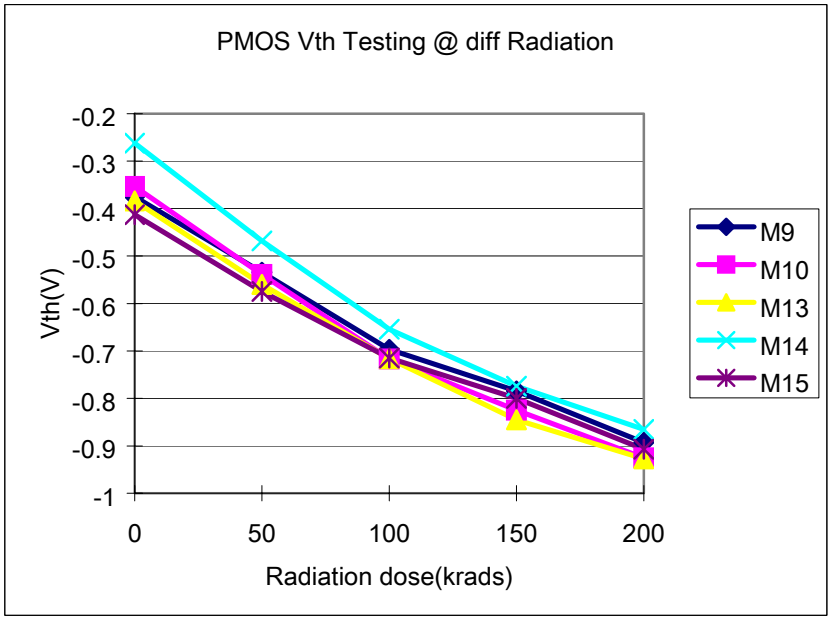


Figure 4: Total ionizing dose (TID) of PMOS with varying radiation dose.

The threshold voltage shifts were very consistent across the PMOS devices, but the NMOS device threshold voltage shifts varied considerably more across different W/L ratios. Some of this was identified with short-channel and narrow-width effects, but this could not explain the observations entirely. The NMOS devices also show a smaller sensitivity to the radiation dose, as well. Semi-empirical radiation effects equations were derived from this data and used to parameterize the BSIM3SOI radiation effects

model. The W/L dependences of the threshold voltage shifts have been left adjustable in the model. The majority of this effect is the variation in the un-exposed value of the threshold voltage with different W/L ratios, whereas the proportionality of the threshold voltage shift on radiation dose is fairly consistent among the measured devices. The match between the semi-empirical radiation effects model and the measured data is shown in Figure 5. It can also be noticed that the variation between different W/L ratio devices becomes less with higher radiation doses.

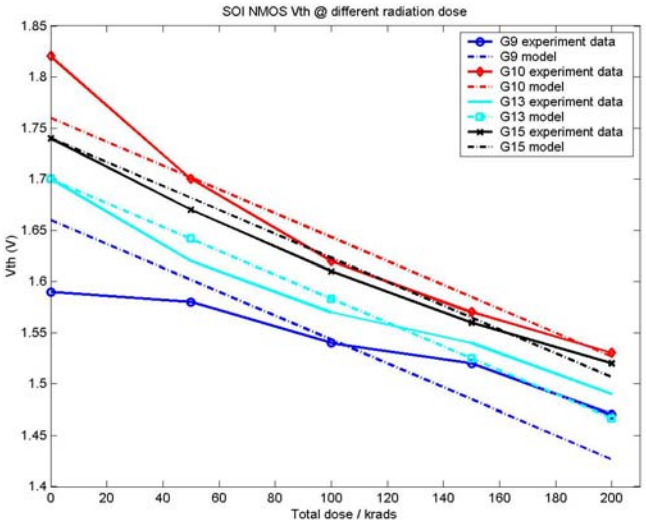


Figure 5: Semi-empirical radiation effects model versus measured data.

Test Chips

No test chips were fabricated as part of this work. However, generic SOI devices were obtained from a test wafer process monitoring area, and these test devices were further diced and packaged for total ionizing dose (TID) testing, as well as for overall validation of the simulation models under non-radiation conditions.

Other Results

Technology Transfer/Intellectual Property

Technology transfer to specific industrial and commercial firms is restricted by proprietary boundaries on the test devices, signed non-disclosure agreements (NDAs) with Honeywell and Boeing, and ITAR export restrictions. Possible Intellectual Property may include: Device equations which model total radiation dose effects in SOI MOSFETs; C-code for BSIM3SOI model that implements these device equations; and VHDL-AMS code that also implements the BSIM3SOI radiation effects model.

Publications Resulting from Research

Not at this time.

Benefits to Commercial Sector

These models will also be useful to any applications areas which subject SOI CMOS technologies to harsh environments of temperature and/or radiation. These include nuclear reactors, geophysical sensing, atmospheric telemetry, engine control, and scientific instruments.

References

[1] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd Ed. New York: McGraw-Hill, 1999.

[2] G. Massobrio and P. Antognetti, *Semiconductor Device Modeling with Spice*, 2nd Ed. New York: McGraw-Hill, 1993.

[3] J. Ogrodzki, *Circuit Simulation Methods and Algorithms*. Boca Ration: CRC Press, 1994.

[4] S. Cristoloveanu and S. S. Li, *Electrical Characterization of Silicon-on-Insulator Materials and Devices*. Boston: Kluwer Academic Publishers, 1995.

[5] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, 2nd Ed. Boston: Kluwer Academic Publishers, 1997.

[6] K. Bernstein and N. J. Rohrer, *SOI Circuit Design Concepts*. Kluwer Academic Publishers, 2000.

[7] A. Marshall and S. Natarajan, *SOI Design: Analog, Memory and Digital Techniques*. Boston: Kluwer Academic Publishers, 2002.

[8] C. T. Chuang, et al., "SOI for Digital CMOS VLSI: Design Considerations and Advances," *Proc. IEEE*, vol. 86, no. 4, pp. 689-720, Apr. 1998.

[9] N. Kistler and J. Woo, "Scaling Behavior of Sub-Micron MOSFETs on Fully Depleted SOI," *Solid-State Electron.*, vol. 39, no. 4, pp. 445-454, 1996.

[10] J. A. Burns, et al., "Design Criteria for a Fully-Depleted 0.1 μm SOI Technology," *Proc. 1997 IEEE Int. SOI Conf.*, pp. 78-79, Oct. 1997.

[11] S. Maeda, Y. Hirano, Y. Yamaguchi, T. Iwamatsu, T. Ipposhi, K. Ueda, K. Mashiko, S. Maegawa, H. Abe, and T. Nishimura, "Substrate-Bias Effect and Source-Drain Breakdown Characteristics in Body-Tied Short-Channel SOI MOSFET's," *IEEE Trans. Electron Dev.*, vol. 46, no. 1, pp. 151-158, Jan. 1999.

[12] D. Munteanu, D. A. Weiser, S. Cristoloveanu, O. Faynot, J.-L. Pelloie, and J. G. Fossum, "Generation-Recombination Transient Effects in Partially Depleted SOI Transistors: Systematic Experiments and Simulations," *IEEE Trans. Electron Dev.*, vol. 45, no. 8, pp. 1678-1683, Aug. 1998.

[13] H. Peters and P. Seegebrecht, "Compact SOI-MOSFET Model for High Temperature Circuit Simulation with Emphasis on Process and Layout Data," *Proc. 1998 IEEE Int. Electron Dev. Meet.*, pp. 101-104.

[14] P.-F. Lu, C.-T. Chuang, J. Ji, L. F. Wagner, C.-M. Hseih, J. B. Kuang, L. L.-C. Hsu, M. M. Pelella, Jr., S.-F. Sanford, and C. J. Anderson, "Floating Body Effects in Partially Depleted SOI Circuits," *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1241-1253, Aug. 1997.

[15] C. F. Edwards and W. Redman-White, "The Effect of Body Contact Series Resistance on SOI CMOS Amplifier Stages," *IEEE Trans. Electron Dev.*, vol. 44, no. 12, pp. 2290-2294, Dec. 1997.

[16] P. E. Dod, et al., "Impact of Technology Trends on SEU in CMOS SRAMs," *IEEE Trans. Nuclear Sci.*, vol. 43, no. 6, pp. 2797-2804, Dec. 1996.

[17] S. T. Liu, et al., "Radiation Response of SOI Materials," *Proc. Electrochem. Soc.*, pp. 225-230, 1999.

[18] M. S. L. Lee, B. M. Tenbroek, W. Redman-White, J. Benson, and M. J. Uren, "A Physically Based Compact Model of Partially Depleted SOI MOSFETs for Analog Circuit Simulation," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 110-121, Jan. 2001.

[19] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, R. J. T. Bunyan, and M. J. Uren, "Impact of Self-Heating and Thermal Coupling on Analog Circuits in SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1037-1046, July 1998.

[20] Berkeley Device Group web site: http://www-device.eecs.berkeley.edu/~bsimsoi/

[21] D. P. Foty, *MOSFET Modeling with SPICE – Principles and Practice*. Upper Saddle River, New Jersey: Prentice Hall PTR, 1997.

[22] W. Liu, *MOSFET Models for SPICE Simulation Including BSIM3v3 and BSIM4*. New York: John Wiley & Sons, 2001.

[23] B. J. Sheu, D. L. Scharfetter, P.-K. Ko, and M.-C. Jeng," BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 8, pp. 558-566, Aug. 1987.

PROJECT 6

RADIATION-TOLERANT SIGE BICMOS SMART MMICS FOR SPACE COMMUNICATIONS

Prof. Deuk Heo (Washington State University) with Fong Shi (Boeing)

RESEARCH TIME PERIOD: Two years
RESEARCH FOCUS: AFRL Task Areas 2, 3, and 4: Standard Cell/Topologies in Radiation-Hardened SOI, Reconfigurable Mixed-Signal Electronics and System-on-a-Chip Design.

Figures and Tables

Figure 30. Schematic of the 15GHz 6-bit pin-diode inductor-less phase shifter
Figure 31. Die photo of the 15GHz 6-bit pin-diode inductor-less phase shifter
Figure 32. The simulated performance of 15 GHz 6-bit phase shifter: (a). Relative phase shift (b) Insertion loss (S21) and (c) Return loss (S11)
Figure 33. Evaluation board for the 6-bit pin-diode phase shifter

Abstract

This AFRL project encompasses investigation and implementation of radiation-tolerant SiGe smart MMICs for upper X-band or lower Ku band LEO satellite phase array communication systems. SiGe MMICs such as SPDT T/R switches, phase shifter, and attenuator based on novel PIN diodes have been implemented. The octagonal PIN diode performance is an improvement over current state of the art in SiGe process. All designs are based on IBM SiGe 7HP BiCMOS process technology. Besides implementing the PIN diode in IBM SiGe process, the new PIN diode structure has also been implemented using the economical Jazz 0.18µm SiGe process and the measurement results show good performance.

Novel high isolation and low insertion loss PIN diodes are designed on SiGe substrate. The PIN diode models have been compiled and de-embedding structures for PIN diode have been implemented to extract an accurate device model in IBM 7HP BiCMOS process. As part of the project, a single pole double throw (SPDT) T/R switch using PIN diodes has been also implemented in the IBM 7HP to verify the PIN diode's performance. With the compiled small-signal model, PIN diode has been used to realize a 3-bit broadband attenuator operating between 10 GHz and 20 GHz with 1 dB step for normalized attenuation levels from 0 to 7 dB. In addition, PIN diode is used to realize 6-bit switched-filter type phase shifter to realize 0° to 360° phases with a resolution of 5.625°. An evaluation board has been designed and fabricated to characterize the phase shifter. The radiation tolerance measurement on MMICs has been performed in partnership with Boeing. The radiation tolerance of developed passives and RF SiGe subsystems has been verified with TID test up to 1000 Krad.

Key radiation-tolerant SiGe MMICs have been investigated for upper X-band or lower Ku band LEO satellite phase array communications focusing on radiation tolerance to the total dose effect. MMICs developed are radiation tolerant by design and have been fabricated and characterized under pre and post radiation conditions. Novel high-isolation and low-insertion loss octagonal PIN diodes are designed on SiGe substrate to improve on the current state of the art performance. For a typical 50-µm^2 octagonal PIN diode, the saturation current Is = 1.43 x 10^{-18} A, the ideal factor n = 1.047 at T = 300 K, and breakdown voltage is -11 V. It obtains the isolation of -19.21dB when V_{RB}=-1.5V at 18 GHz. After the de-embedding, the insertion loss of PIN diode is below 1dB from 1GHz to 18GHz. Based on novel PIN diode implementation, a single pole double throw (SPDT) switch is designed. The measurement data shows the SPDT switch can achieve the isolation of 48–26 dB over a wide frequency range (1–18 GHz). PIN diode is also used to realize 6-bit switched-filter type phase shifter to realize 0° to 360° phase range with a phase resolution of 5.625°. A 3-bit broadband PIN diode attenuator is also designed with 1dB resolution with attenuation levels ranging from 0 to 7 dB between 10 GHz to 20 GHz. The radiation tolerance measurement on developed passives and RF SiGe subsystems has been performed in partnership with Boeing with TID test up to 1000 Krad. Besides implementing the PIN diode in IBM SiGe process, the new PIN diode structure has also been successfully implemented using the economical Jazz 0.18µm SiGe process and achieves isolation of 13.67dB and the maximum insertion loss of 1.09dB at 18GHz.

Project Description

Phased-array antenna systems offer many significant advantages over those that utilize a conventional antenna in satellite space communications. The advantages include the ability to make multiple steered antenna beams from the same aperture, the ability to make antennas conformal with their mounting structure, and the ability to generate directive beams that can be electronically repositioned. Solid-state device technology has motivated phased arrays to overcome the low reliability inherent to tube-type transmitters and their associated high-voltage power supplies and also improves system efficiency.

Transmit/receive (T/R) module forms the final stage of the module for transmitted signals and the first stage of the module for received signals. Apart from amplification, it controls the amplitude and phase of the signals to steer the antenna beam. Low module cost is desirable due to the number of modules required in a general phased-array application. For these reasons, T/R modules significantly affect the entire phased-array antenna architecture and play a critical role in determining the overall system cost and performance for phased-array-based applications. Advancements in SiGe BiCMOS performance and cost, and packaging techniques have stimulated the production of high-performance T/R modules at lower cost compared to GaAs based technology node. Future developments will focus on providing current performance levels but at a lower cost and implementing higher performance technologies.

This research project is focused on development of low cost Smart SiGe MMICs for upper X-band or lower Ku band LEO satellite phased-array communication systems. We developed SiGe RF circuit blocks for compact T/R module such as SPDT switches, phase shifters, and attenuators based on novel PIN diodes. Innovative design and layout methodologies were also developed to improve the SiGe circuit performance for radiation tolerant space communication applications. TID test facilities for testing the developed SiGe circuit blocks is provided by the industry partner, Boeing, and they provided assistance in TID measurements.

Research Results and Discussion

Novel octagon PIN diode design, modeling and measurement results

PIN diode design and modeling

High frequency applications require switching devices with low insertion loss and high isolation to achieve good performance. High isolation and low insertion loss PIN diode is the right candidate for such purpose. It can be used in many MMICs like attenuator, phase shifter, T/R switch to achieve good performance. A PIN diode is formed by creating highly doped P and N junction with lightly doped intrinsic region as shown in Figure 1. In the IBM 7HP SiGe process, the PIN diode can be realized with HBT material layers, namely, the buried n+ subcollector layer, n-collector layer and p+ SiGe base layer. These layers have been used to form the cathode, I (Intrinsic), and anode region of the PIN diode, respectively. A novel octagonal pin diode is developed in IBM 7HP SiGe process in this project.

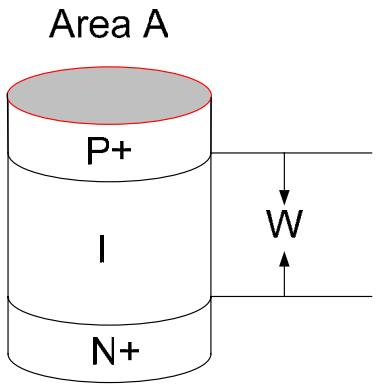


Figure 1.PIN diode structure

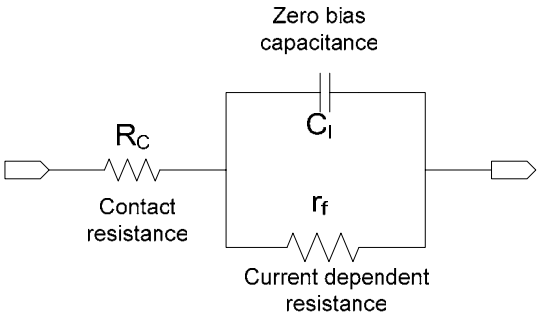


Figure 2. Forward bias model (on state) for the PIN diode

As shown in Figure2, in the forward bias condition, the PIN diode operates as a variable resistor. The total resistance of the PIN diode (R_f) is the sum of the current independent contact resistance R_C and current dependent resistance, r_f, caused by the conductivity modulation of the intrinsic region[1-2]. C_I is the diffusion capacitance which accounts for the charge storage in the undeleted intrinsic region.

$$R_C = (r_p + r_n) + (r_{cp^+} + r_{cn^+}) \quad (1)$$

$$r_f = \frac{l_i^2}{2\mu\tau I_{dc}} \quad (2)$$

$$R_f = (r_p + r_n) + (r_{cp^+} + r_{cn^+}) + \frac{cons\tan t}{I_{dc}} \quad (3)$$

$$C_I = \tau_t / r_f \quad (4)$$

where r_p is the resistance of the P+ region, r_{cp+} is P+ metal contact resistance, r_n is the resistance of the N+ region, r_{cn+} is N+ metal contact resistance, l_i is the thickness of intrinsic region, μ is average electron and hole mobility, τ is minority carrier life time and τ_t is carrier transit time in the intrinsic region.

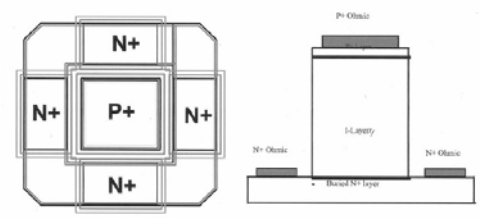
Compared with rectangular and square PIN diode layout, the new octagonal PIN diode layout has greatly reduced the current-based resistance due to its small periphery-to-area ratio for a given cross-sectional area (See Figure3). Additionally, the total subcollector contact area is also increased which results in low contact resistance. In doing so the insertion loss for the PIN diode is greatly improved. At given cross-section area, smaller periphery-to-area ratio will give larger minority carrier life, thus, the current based resistance is reduced according to equation (2). Minority carrier lifetime is proportional to the improbability that an electron and hole will recombine. The boundary of PIN diode causes the imperfections in the regular array of crystal atoms that creates energy states within the otherwise disallowed bandgap of the silicon. Therefore, its peripheral recombination probability is much larger when compared to silicon crystal of infinitely extended dimensions. The relationship between the minority carrier lifetime and the periphery-to-area ratio is given by equations (5)-(7) [3]:

$$R_{Eff}A = R_{Bulk}A + R_{Perim}P \quad (5)$$

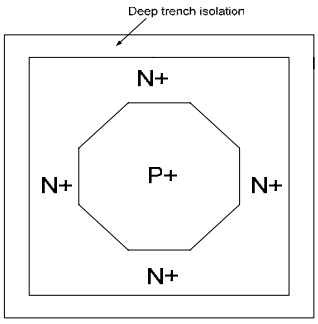
$$\frac{\Delta p_n}{\tau_{pEff}} \approx \frac{\Delta p_n}{\tau_{pBulk}}A + S_{Perim}\Delta p_n P \quad (6)$$

$$\frac{1}{\tau_{pEff}} \approx \frac{1}{\tau_{pBulk}} + S_{Perim}\left(\frac{P}{A}\right) \quad (7)$$

where R_{Eff} is the effective recombination rate of the device, R_{bulk} is the area normalized bulk minority carrier recombination rate, R_{perim} is the perimeter normalized minority carrier recombination rate, Δp_n is excess minority carrier concentration on the n-side of the junction, τ_{bulk} is bulk minority carrier lifetime, and S_{perim} is effective hole surface recombination velocity.



(a)



(b)

Figure 3. (a) Square and (b) Novel octagonal PIN diode layout

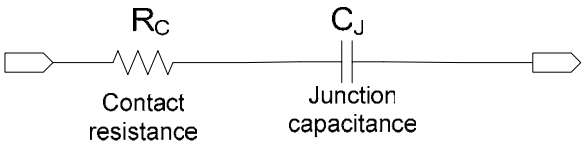
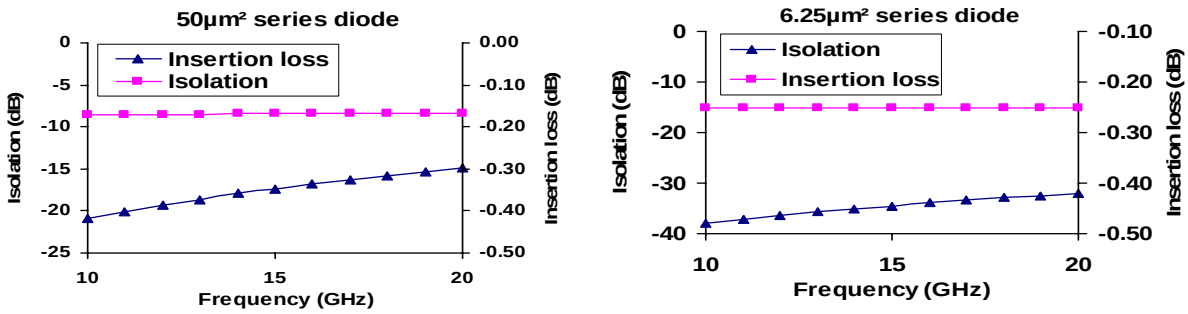


Figure 4. Reverse bias model (off state) for the PIN diode

In reverse bias condition (See Figure4), the small signal model is extracted at punch-through voltage where the PIN diode's junction capacitance is the smallest. This will help improve the diode isolation during the off-state. The junction capacitor for the PIN diode is given by equation (8),

$$C_J = \varepsilon A / W \qquad (8)$$

where A is the PIN diode's area and W is the intrinsic region width. Figure 5 shows the insertion loss and isolation performance for the octagonal PIN diode in series configuration for 50 μm^2 and 6.25 μm^2 diode geometry. Good broadband performance has been obtained for both diodes. For the 6.25 μm^2 diode, the isolation is higher than that for 50 μm^2 since it has smaller area and junction capacitance. Conversely, 6.25 μm^2 diode has high insertion loss since the current-based resistance at forward bias is a little bit larger than that for 50 μm^2 (see Figure5). This is because smaller device geometry will result in high periphery- to-area ratio. Figure6 shows the layout of the PIN diode.



(a) (b)

Figure 5. Simulated insertion loss and isolation for (a) 50 µm^2 PIN diode and (b) 6.25 µm^2 PIN diode

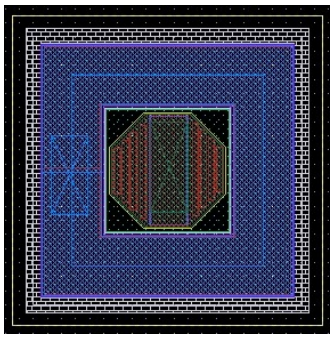


Figure 6. High performance PIN diode layout

PIN diode DC measurement Result:

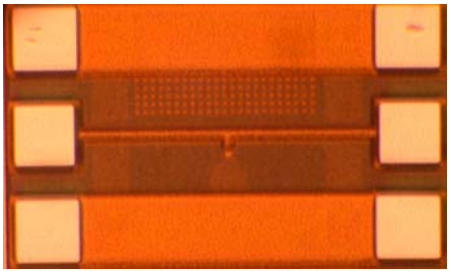
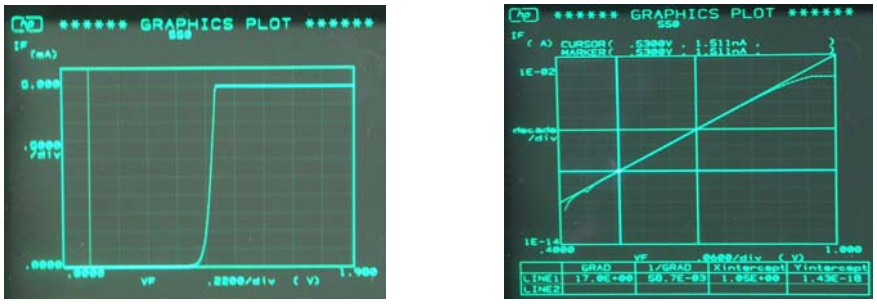


Figure 7. 50-µm^2 shunt diode with transmission line



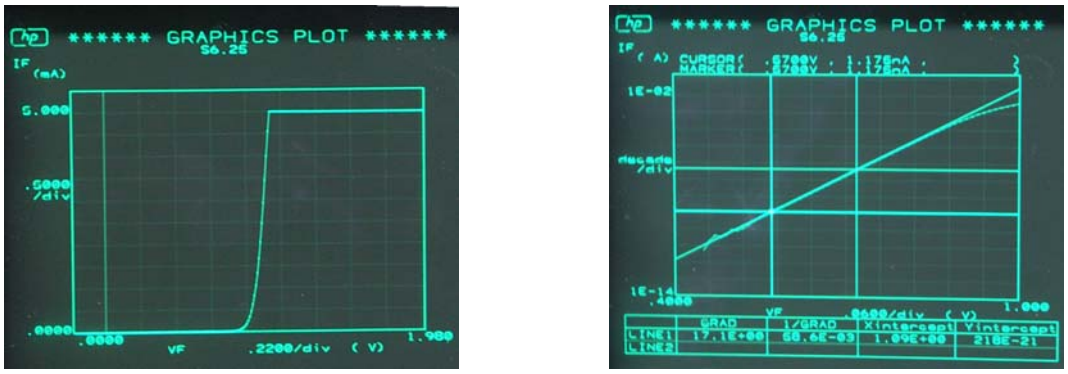
(a) (b)

Figure 8. 50-µm^2 shunt diode with transmission line (a) DC I-V characteristics, (b) log I versus voltage

Figure7 shows a 50-μm^2 and 6.25-μm^2 shunt PIN diode's chip diagrams. The PIN diode's anode is connected to the 50-Ω transmission lines and cathode is connected to the ground signal. The 50-μm^2 PIN diode DC measurement performance has been shown in Figure 8 (a) and (b). The diode follows a parallel plane diode behavior, given by

$$I = I_s(\exp(\frac{qV}{nKT}) - 1) \quad (9)$$

The measured data on saturation current *Is*, the ideal factor and the junction reverse breakdown voltage V_b are found to be *Is* = 1.43 x 10^{-18} A, *n* = 1.047, at *T* = 300 K, and V_b = -11 V.



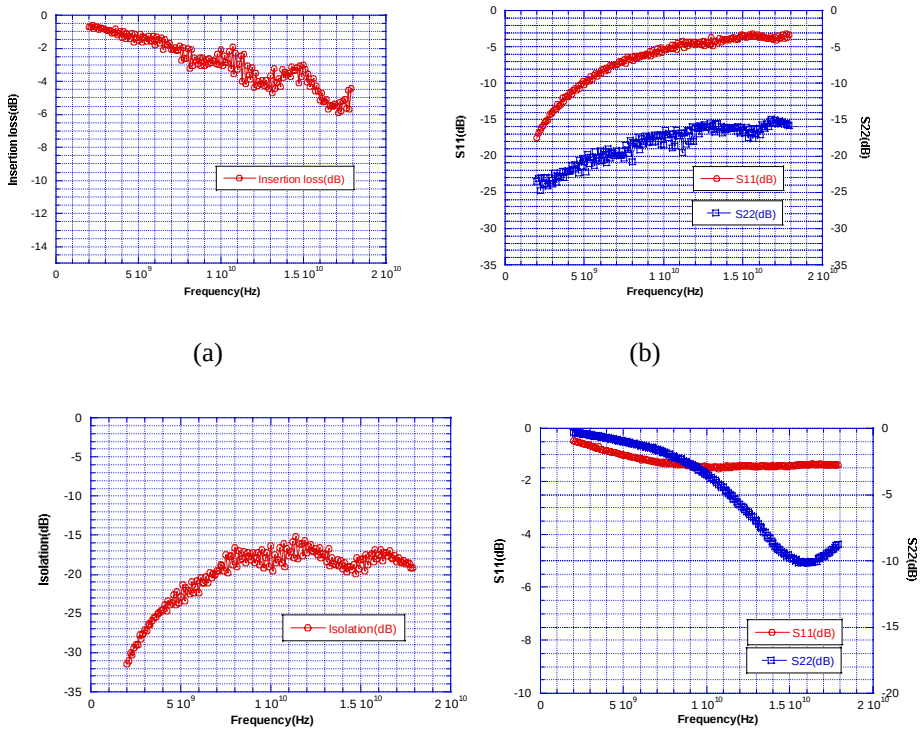
(a) (b)

Figure 9. (a) 6.25-μm2 shunt diode with transmission line (c) DC I-V characteristics (d) log I versus voltage

Figure9 (a) and (b) shows the DC performance of 6.25-μm^2 shunt diode. The measured data on saturation current *Is*, the ideal factor and the junction reverse breakdown voltage V_b are found to be *Is* = 2.18 x 10^{-19} A, *n* = 1.008, at *T* = 300 K, and V_b =-11 V. The value of n has a significant effect on the performance of the PIN diode. The measurement results show that the octagonal PIN diode fabricated in IBM 7HP process has a very good DC performance.

PIN diode RF measurement Result:

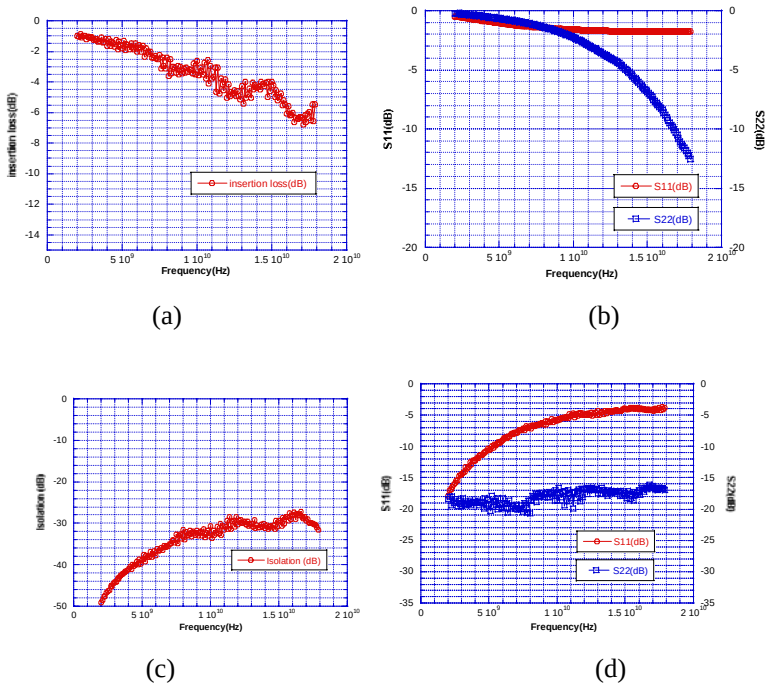
Figure10 shows the RF measurement results of 50-μm^2 series diode. It obtains the isolation of -19.21dB at V_{RB}=-1.5V at 18 GHz. Due to the inaccurate transmission line model in design, the insertion loss is rather high, but it will be improved after the de-embedding process when exclude the pad coupling effects and transmission loss. After the de-embedding process, the insertion loss drops below 1dB from 1 GHz to 18 GHz. It is same for 6.25-μm^2 PIN diode.



(a) (b)

(c) (d)

Figure 10. RF performance of 50-µm2 series diode: (a) Forward Bias Insertion Loss with transmission line without de-embedding, (b) S11 and S22 at forward bias condition, (c) Reverse Bias Isolation, and (d) S11 and S22 at Reverse Bias Condition.



(a) (b)

(c) (d)

Figure 11. RF performance of 6.25-µm2 series diode: (a) Forward Bias Insertion Loss with transmission line without de-embedding, (b) S11 and S22 at forward bias condition, (c) Reverse Bias Isolation, and (d) S11 and S22 at Reverse Bias Condition.

Figure 11 shows the RF measurement results of 6.25-μm^2 series diode. It obtains the isolation of -31.9 dB at V_{RB}=-1.5V and the insertion loss drops below 1dB from 1 GHz to 18 GHz after the de-embedding.

De-embedding test structure for PIN diode

In order to get the accurate model information about PIN diode, de-embedding test structures have been designed for the measurement. Three-step de-embedding method is used to build the test structure [4]. By using this technique, the parasitic components' influence on test structure stemming from the contact pads, the metal interconnection and coupling effects from the silicon substrate is subtracted from the RF behavior of the actual DUT.

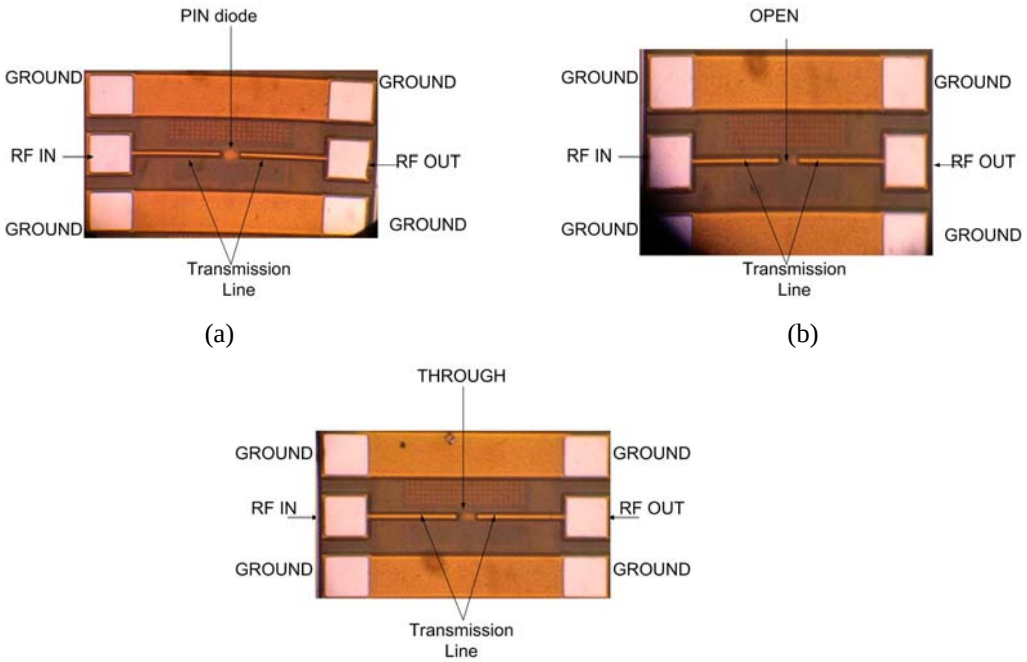


Figure 12. Chip diagram of (a) the PIN diode test structure, (b) open, and (c) through layout of the de-embedding structure.

For the PIN diode, bias voltages for anode and cathode are provided from the bias tee and only two ports are used in test structure. The chip diagram of the RF test-structure and the corresponding on-wafer de-embedding structure, i.e., open and through structures which are needed for the de-embedding procedure, are shown in Figure 12. The pads and the metal interconnections are identical for the test – structure and the de-embedding structure.

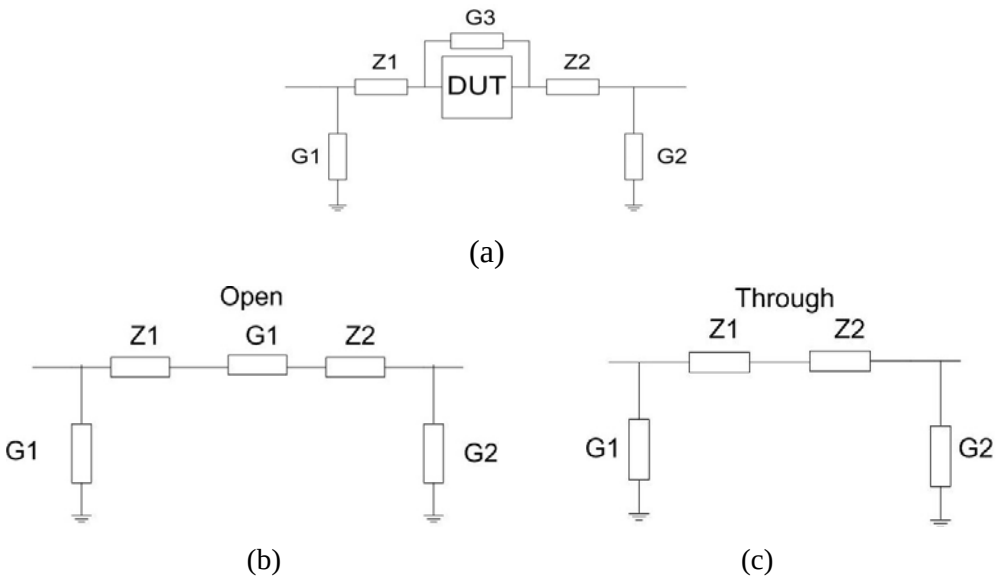


Figure 13. Equivalent schematic circuit of (a) RF test-structure,
(b) open de-embedding structure, and (c) through de-embedding structure

The basic assumption in the de-embedding procedure comes from the theory that the effect of parasitics in de-embedding chip diagram (Figure12) can be represented as equivalent admittances and impedances shown in Figure 13. Thus, the electrical behavior of the DUT is influenced by the parasitic admittance G_1, G_2 and G_3 and the parasitic impedances Z_1 and Z_2 .The admittance G_1 G_2 and G_3 represents the coupling via the metal interconnections and the silicon substrate between the pads of anode (port 1) and ground, cathode (port 2) and ground, and anode (port 1) and cathode (port 2), respectively. The impedances Z_1 and Z_2 originate from the metal interconnection's series impedance between port 1 and port 2, and actual DUT. By measuring the S-parameters of the on-wafer de-embedding structure and converting them to y-parameters, all parasitic admittance and impedance values can be calculated according to the following equations:

$$G_1 = y_{11op} + y_{12op} \qquad (10)$$

$$G_2 = y_{22op} + y_{12op} \qquad (11)$$

$$G_3 = (-1/\, y_{12op} + 1/\, y_{12th})^{-1} \qquad (12)$$

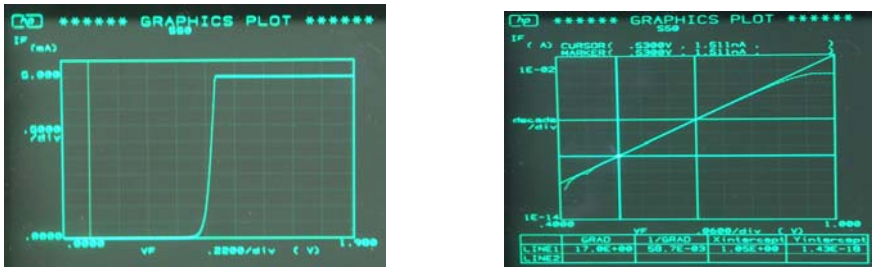
$$Z_1 = Z_2 = -1/(2y_{12th}) \qquad (13)$$

where the y_{11op}, y_{12op} and y_{22op} is measured y-parameter of the open structure and y_{12thr} is measured y-parameter of the through structure. After excluding the calculated parasitic admittance and impedance, accurate DUT model can be achieved. The calculation results show that after the de-embedding process, the insertion loss of PIN diodes (including both 50-μm^2 and 6.25-μm^2 series PIN diodes) drops to below 1dB.

TID test for PIN diode

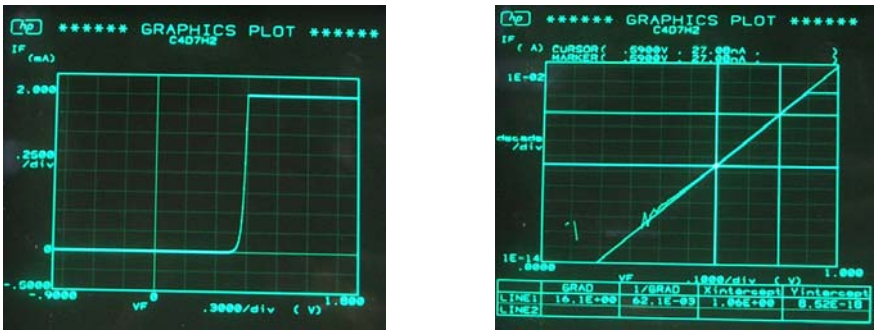
The PIN diode chip was measured for tolerance to total ionizing dose (TID) at Boeing Radiation Effects Laboratory. The irradiation was performed using a GAMMACELL 220 EXCEL (GC-220E) at 27°C producing a dose of 1000 krad. The power supply current had shown no changes up to 450 Krad but changed slightly at 1000 Krad. The DC performance showed only minor changes up through 1000 Krad Co-60 at Dose rate of 234 rad(si)/s. Due to time issues, the TID test stopped at 1000 Krad while the PIN

diode can still work properly. Figure14 and Figure15 show the 50-μm^2 shunt diode's DC performance before and after TIF test. Before the radiation, the saturation current *Is*, the ideal factor and the junction reverse breakdown voltage V_b are found to be *Is* = 1.43 x 10^{-18} A, *n* = 1.047, at *T* = 300 K, and V_b =11 V. After 1000 Krad dose radiation, *Is* = 8.52 x 10^{-18} A, *n* = 1.162, at *T* = 300 K, and V_b =10 V. These results shows that PIN diode built in IBM 7HP process has good radiation toleration performance and are suitable for the applications in next generation phase array satellite communication networks in outer space.



(a) (b)

Figure 14. 50-μm^2 shunt diode Before TID test (a) DC I-V characteristics, (b) log I versus voltage



(b) (d)

(c)

Figure15. 50-μm^2 shunt diode After 1000 Krad dose (a) DC *I-V* characteristics, (b) log *I* versus voltage

High isolation SPDT switch

A new high isolation SPDT switch has been designed based on the novel PIN diode model. In order to achieve high isolation, series-shunt-shunt switch arm configuration is chosen as shown in Figure 16. Compared with the conventional series-shunt switch architecture [2], one more shunt diode is added to increase the isolation [5]. Also, two different PIN diodes with different areas are used in the switch design, each tailored for optimum performance.

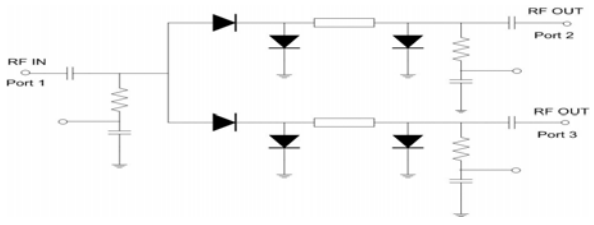
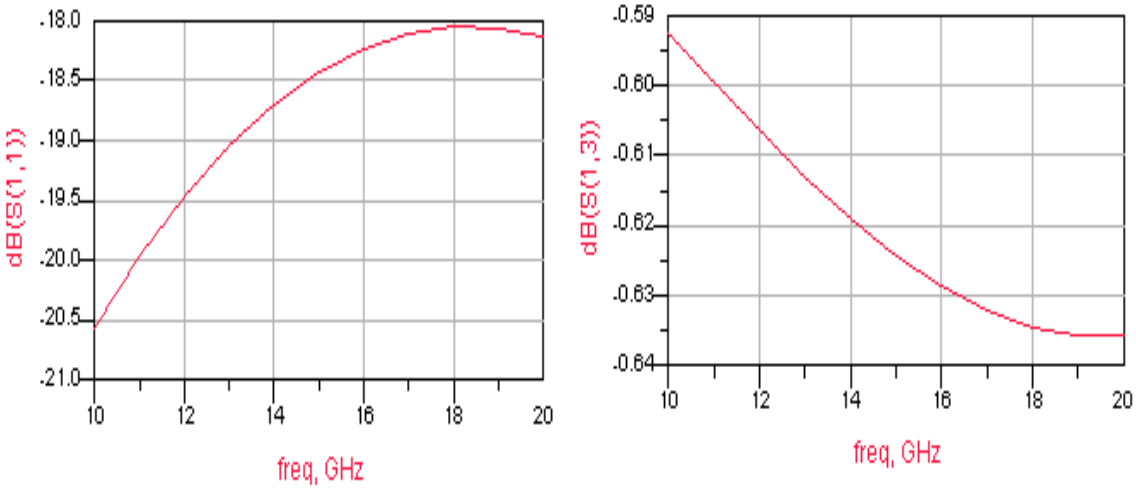


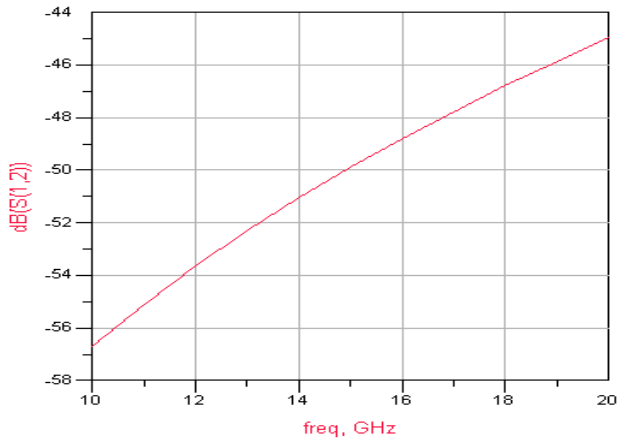
Figure 16. Series-shunt-shunt switch

For the series path, the PIN diode with 6.25μm^2 geometry is used since it has low junction capacitance and therefore high isolation. The 50μm^2 PIN diode is used for the shunt path since it has low insertion loss. This combination can result in high isolation while maintaining low insertion loss. The switch simulation shows worst case isolation of 45 dB in the 10 GHz to 20 GHz frequency range (see Figure 17), while achieving worst case insertion loss of 0.64 dB. The circuit has maximum return loss of 18 dB as shown in Figure 17(a).

In the SPDT chip diagram (see Figure 18), bended microstrip transmission lines are used for on-chip input and output matching. On-chip resistive bias networks are also employed to get small chip size and broadband switch performance. The layout size is 1045μm*710μm.



(a) Return loss (b) insertion loss



(c) Isolation

Figure 17. (a) Return loss (b) Insertion loss and (c) Isolation performance of the SPDT switch

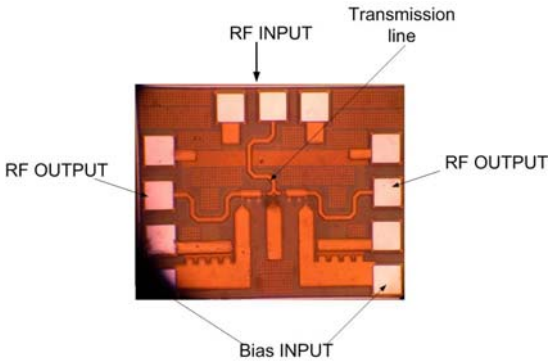


Figure 18. Chip diagram of high isolation SPDT switch with Novel PIN Diode

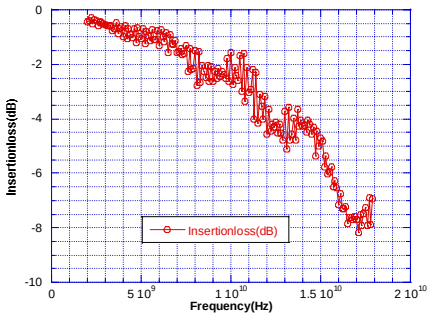


Figure 19. Insertion Loss of 450-μm Transmission Line

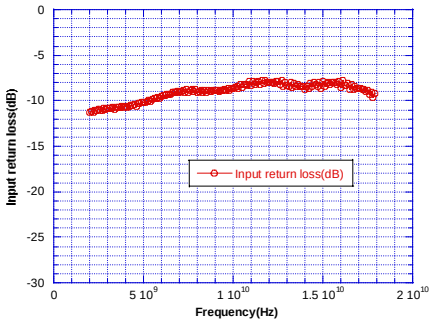


Figure 20. Input Return Loss of SPDT Switch

Referring to Figure 16, a through-path between ports 1 and 2 exists when V_{b2} = 2.52V and V_{b1} = 0 V and causing the series diode to become forward biased at 2mA while the shunt diode is reversed biased. Similarly, an isolation path exists between ports 1 and 3 when V_{b3} is set at = 4.1V. The measurement data shows the SPDT switch can achieve the isolation of 48–26 dB over a wide frequency range (1–20 GHz). The insertion loss is high because of the following reasons: 1) the transmission line model in IBM 7HP process is not accurate and very lossy. Figure19 shows that insertion loss of 450-μm transmission line is around 8dB; 2) The PIN diode model based on limited process parameter calculations is not accurate, it degrades the input return loss and worse the insertion loss further (shown in Figure20). When the low insertion loss transmission line and PIN diode accurate model is available, the SPDT switch will achieve much better performance.

3-bit inductor-less attenuator

A 3-bit attenuator consisting of 1 dB, 2 dB and 4 dB attenuation stages utilizing PIN diodes is developed. The attenuation functions are realized by two broad-band SPDT switches between the reference path and resistive attenuation path [2]. The SPDT PIN diode switches can give high isolation between the reference path and attenuation path and the symmetric structure reduces the phase difference between the reference and attenuation path. Most importantly, this structure works for inductor-less attenuator design. Compared with the structure in Figure 21 [6], the proposed SPDT attenuator structure (see Figure 22) only consumes half the current as required by the first one. This way, the voltage drop caused by the large resistor used to replace the ac blocking inductor is reduced to half. Thus, the proposed attenuator structure is more suitable for low power applications. Figure 23 shows combined 3-bit PIN diode attenuator.

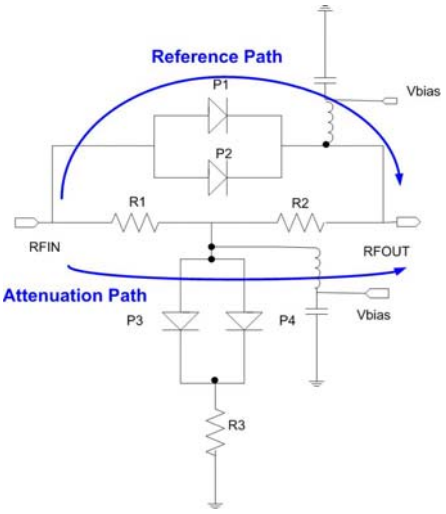


Figure 21. 1-bit attenuator with inductor

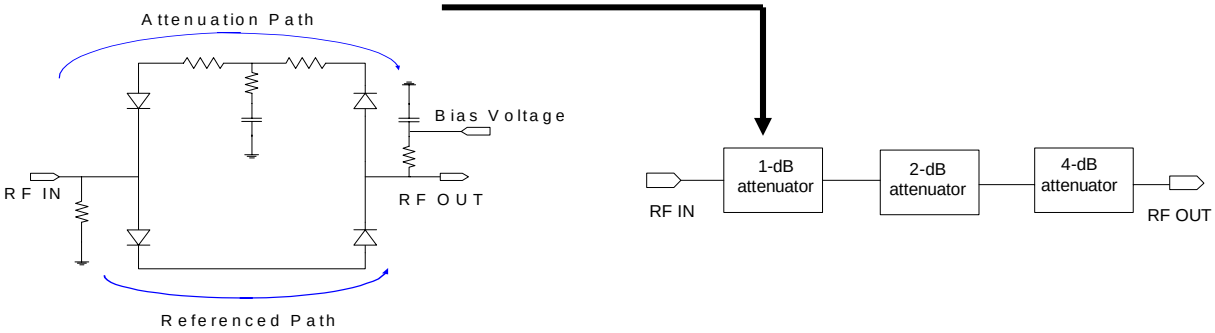


Figure 22. Schematic of one bit attenuator

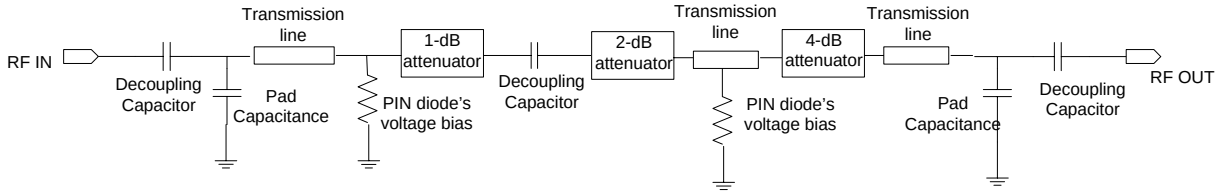
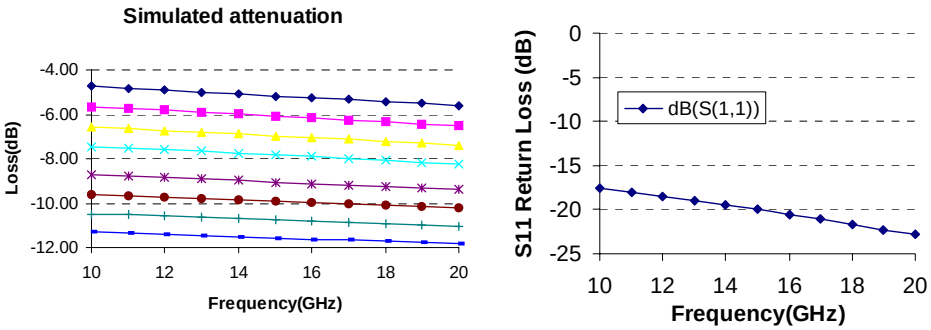


Figure 23. 3-bit combined PIN diode attenuator

In order to reduce chip size, large resistors are used instead of inductors as RF choke for dc bias network. The 50-μm^2 PIN diodes are used all through the attenuator for reducing the reference path insertion loss. MIM capacitors are used in the design to provide RF bypassing. Figure24 shows the simulated performance of the 3-bit attenuator. The attenuator achieves attenuation of 0 dB to 7 dB in steps of 1dB when normalizing the reference insertion loss (see Figure24(a)). All the attenuation bits show good relative attenuation performance and are broadband. Figure 24 (b) shows the return loss plot with maximum return loss of 17.5 dB.



(a) (b)

Figure 24. Simulated (a) attenuation loss (b) return loss for 3-bit attenuator

In the attenuator layout chip diagram (see Figure 25), 50 Ω bended microstrip transmission lines are used for on-chip input and output matching. On-chip resistive bias networks are also employed to get small chip size and broadband attenuation performance. The chip size is 1045μm*710μm, which is a significant improvement over the attenuator mentioned in [2], with a size of 1800μm*710μm. Measurement of attenuator is still in process.

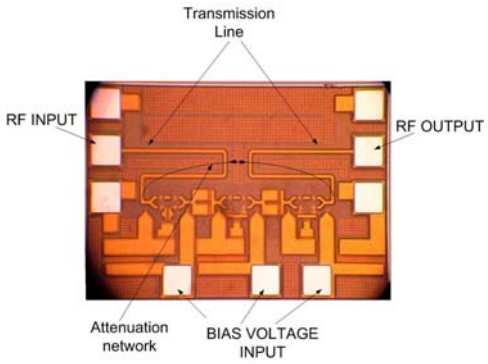


Figure 25. Chip diagram of PIN diode inductor-less attenuator

PIN diode research in Jazz process

In the phase array communication system, the large number of modules required in system needs more economical and high performance solution. Thus, we are prompted to explore the possibility of PIN diode implementation in other standard SiGe BiCMOS process. Jazz SBC18 SiGe process offers a good alternative. The availability of several high-performance microwave passive and active devices on the same wafer. With a maximum cutoff frequency f_t of 155GHz, it is a good choice for innovative, high-performance, low-power applications [7-8]. The only limitation is that Jazz process do not provide customized N-epi layer etching step to build a high performance vertical PIN diode.

A Jazz PIN diode with high isolation and low insertion loss has been implemented by optimizing the distance between the anode and the cathode. The performance of this PIN diode structure is comparable to the PIN diodes built in IBM 5HP process [1-2].

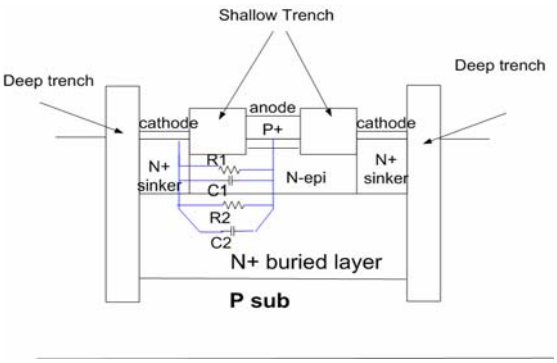


Figure 26. PIN diode cross-section in Jazz SBC180 process

Figure 26 shows a vertical PIN diode proposed in Jazz process. This PIN diode is realized with HBT material layers, namely, the buried n+ subcollector layer, n-collector layer and p+ SiGe base layer. These layers have been used to form the cathode, I (Intrinsic), and anode region of the PIN diode, respectively. However, in Jazz process, the N-epi layer between the anode and cathode can not be etched, optimization for the distance between them is necessary to achieve a high isolation and low insertion loss PIN diode.

In the forward bias condition, there are two current paths for Jazz PIN diode. One is from P+ anode through N-epi layer, to the N+ cathode(represented by resistance R1) and the other path needs to pass the N+ buried layer (represented by R2). Thus, R1 paralleled with R2 is the forward bias resistance. This reduces the forward bias resistance and improves the insertion loss. Another advantages of this deign is that its periphery to area ratio is very small and it helps to reduce the insertion loss further.

However, in the reverse bias condition, one extra capacitance generated by the un-etching N-epi layer (represented by C1) increases the reverse bias capacitance and decreases the isolation. Thus, the method to tradeoff between the insertion loss and isolation needs to be developed. In reverse bias case, PIN diode's junction capacitance is given by:

$$C_J = \varepsilon A / W \qquad (14)$$

where A is the PIN diode's area and W is the distance between the cathode and anode.

It is obvious that increasing the W will reduce the reverse junction capacitance and thus improve the PIN diode's isolation performance. But, the distance can not be very large since insertion loss will be increased with W.

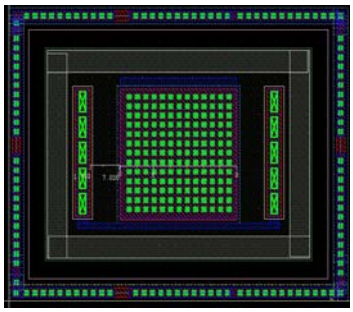
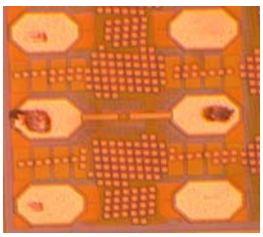
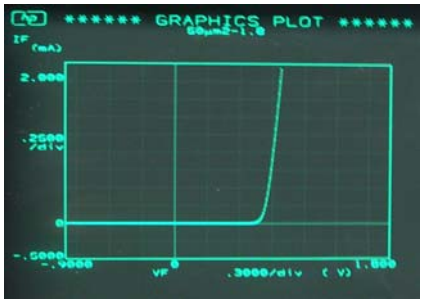


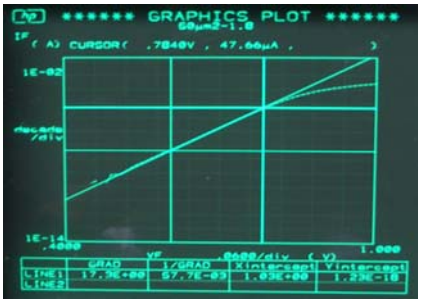
Figure 27. PIN diode layout in Jazz process

Based on the above analysis, two PIN diode devices with different anode to cathode distance, i.e., 1.8 μm and 2.7 μm which is the twice and triple of the minimum distance defined by the design rule are implemented in Jazz SBC18 process. The chosen of these two distances depends on the Jazz process parameters and EM simulation results to get a compromise between the insertion loss and isolation. Figure27 shows the layout of a Jazz PIN diode with 50μm^2 area and cathode to anode distance as 1.8μm. Square shape is selected for PIN diode due to its relatively smaller P/A ratio to rectangular ones. Besides high performance deep trench, double body-tie guard rings are used to improve the isolation further.



(a)





(b) (c)

Figure 28. (a) 50-μm2 series diode with transmission line,
(b) DC I-V characteristics, and (c) log I versus voltage

Figure28 (a) shows the chip diagram of a 50-μm^2 series PIN diode with cathode to anode distance as 1.8 μm. The transmission lines are connected to the PIN diode's anode and cathode. The PIN diode DC measurement performance has been shown in Figure28 (b) and (c). The diode follows a parallel plane diode behavior, given by:

$$I = I_s(\exp(\frac{qV}{nKT}) - 1) \qquad (15)$$

The measured data on saturation current I_s, the ideal factor and the junction reverse breakdown voltage V_b are found to be I_s = 1.23 x 10^{-18} A, n = 1.1, at T = 300 K, and V_b =10V. The value of n has a significant effect on the performance of the PIN diode.

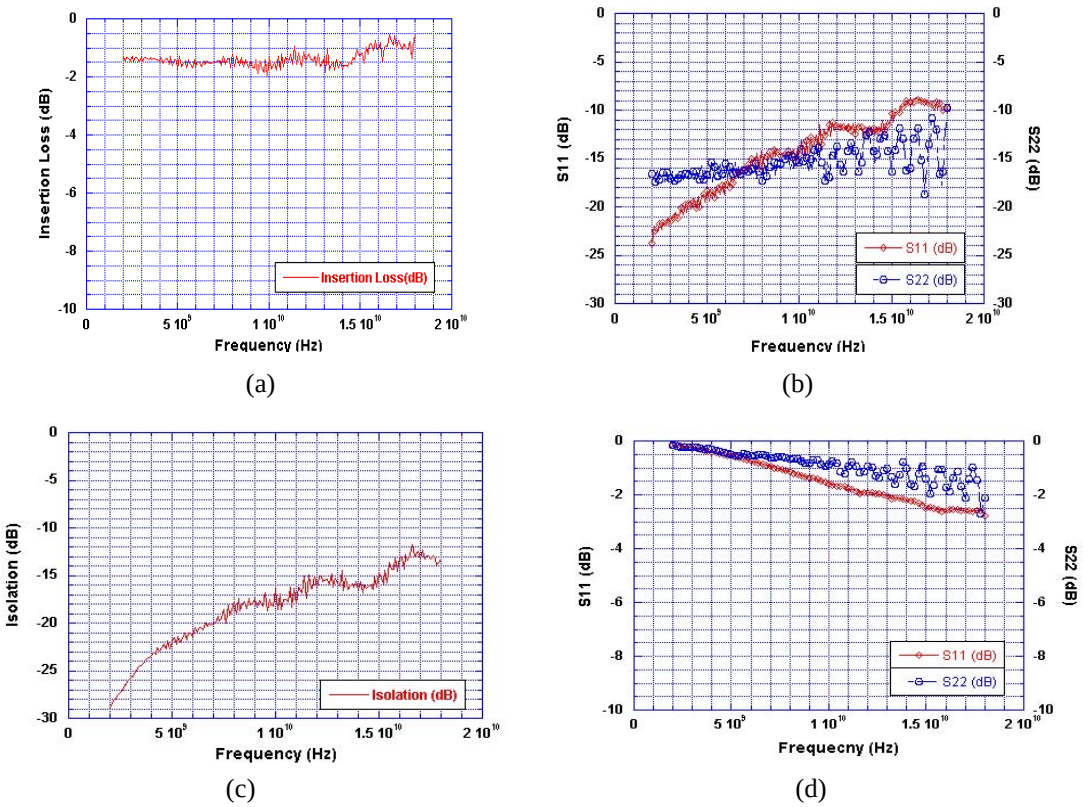


Figure 29. RF performance of 50-μm^2 series diode: (a) Forward Bias Insertion Loss with transmission line, (b) S11 and S22 at forward bias condition, (c) Reverse Bias Isolation, and (d) S11 and S22 at Reverse Bias Condition.

Figure29 shows the RF measurement results. The jazz PIN diodes with cathode to anode distance of 1.8-μm obtains the worst isolation of 13.67dB at VRB=-1.5V and insertion loss of 1.09 dB at IFB=2mA from dc to 18 GHz.

Compared with the Jazz PIN diode with cathode to anode distance of 1.8 μm, the PIN diode with distance of 2.7μm shows similar dc performance, but its insertion loss is one time worse than it and the isolation only improves 0.5dB. Thus, the PIN diode with cathode to anode distance of 1.8 μm gives a good compromise between the isolation and insertion loss. Even without using the special low insertion loss top-polymide transmission line, this measurement data is comparable to the PIN diode implemented in IBM process [1-2].

6-bit Switched-Filter type broadband phase shifter

A 6-bit PIN diode phase shifter has been designed, to operate in the 10GHz to 20GHz frequency range, in a Silicon Germanium (SiGe) BiCMOS technology. The phase shifter design consists of six digit bits for six phase shifts (180^o, 90^o, 45^o, 22.5^o 11.25^o, and 5.626^o) cascaded in a linear arrangement to generate 64 intermediate phases between 0 ^{o} and 360^o with the granularity of 5.625^o. The 180^o, 90^o, 45^o, and 22.5^o phase bits switch between PI and/or T-type highpass and/or low pass phase shift networks with two SPDT PIN-diode switches [9]. The 11.25^o and 5.626^o phase bits use a simplified topology of capacitive and inductive elements to achieve their phase shifts. These phase bit topologies are selected due to their broadband characteristics and relative insensitivity to process variations. The schematic and die photo for the 6-bit pin-diode phase shifter are shown in Figure 30 and 31, respectively.

SiGe pin-diodes (with area 50 um^2) are used for switching functions [10]. Diode biasing is provided through 2 K-ohm resistors in combination with 5pF MIM bypass capacitors [11]. All the 6 bits require 3.8V reverse bias input and the forward bias is selected by determining the total current flow through the

pin-diode. Figure 32 summarizes the simulated performance of the 6 elemental phase shifts over 10-20GHz frequency range, where 15GHz is the center frequency.

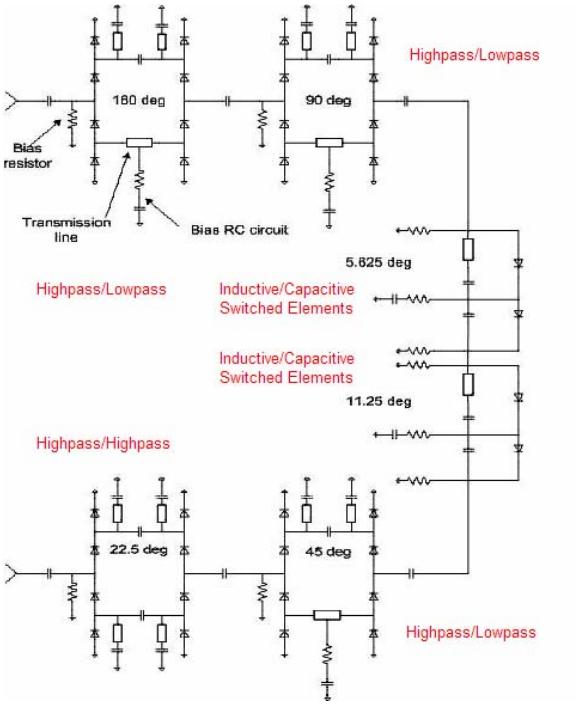


Figure 30. Schematic of the 15GHz 6-bit pin-diode inductor-less phase shifter

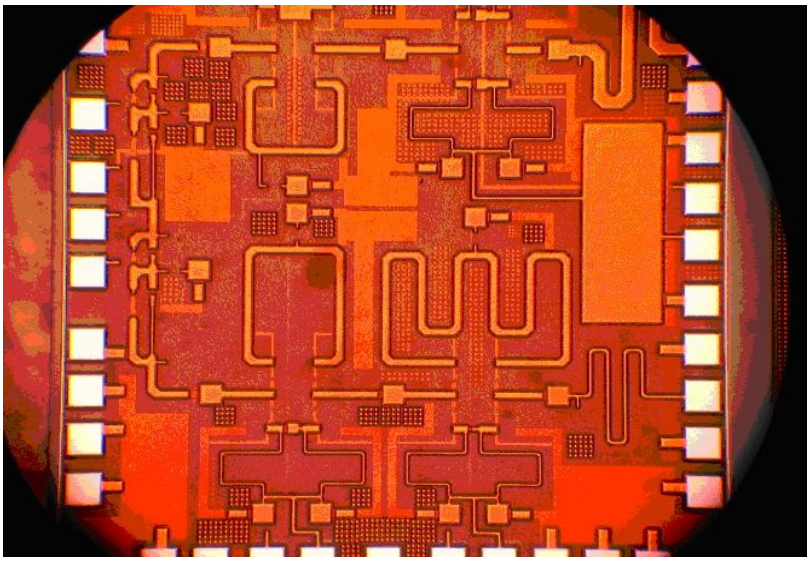
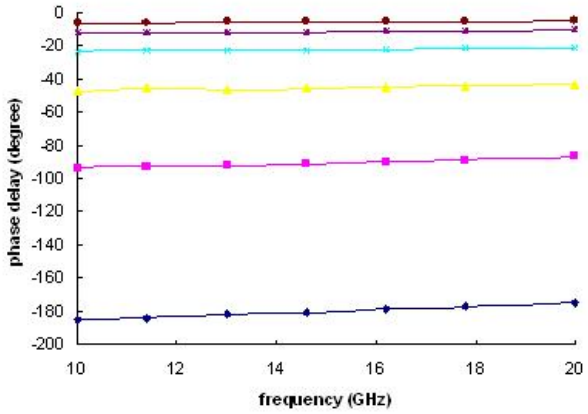
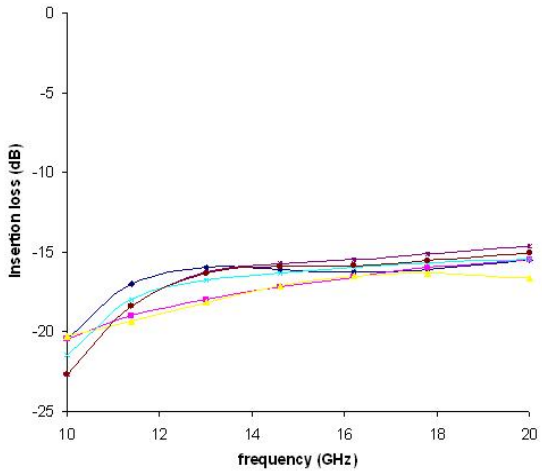


Figure 31. Die photo of the 15GHz 6-bit pin-diode inductor-less phase shifter



(a)



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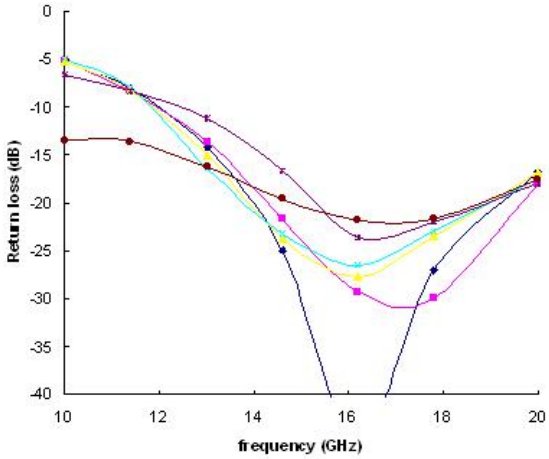


(c)

Figure 32. The simulated performance of 15 GHz 6-bit phase shifter: (a). Relative phase shift (b) Insertion loss (S21) and (c) Return loss (S11)

Evaluation board to validate the performance of the 6-bit pin-diode phase shifter has been designed using ADS and is shown in Figure 33. The evaluation boards use Rogers 3003 panel material (dielectric constant $\varepsilon_r = 3.00\pm0.04$) and the panel thickness is 0.031". There are ten DC biasing lines, which are used to serve the bit control. The RF signal will be supplied and measured directly using GSG (ground-signal-ground) on-wafer probes. Now the measurement is in process.

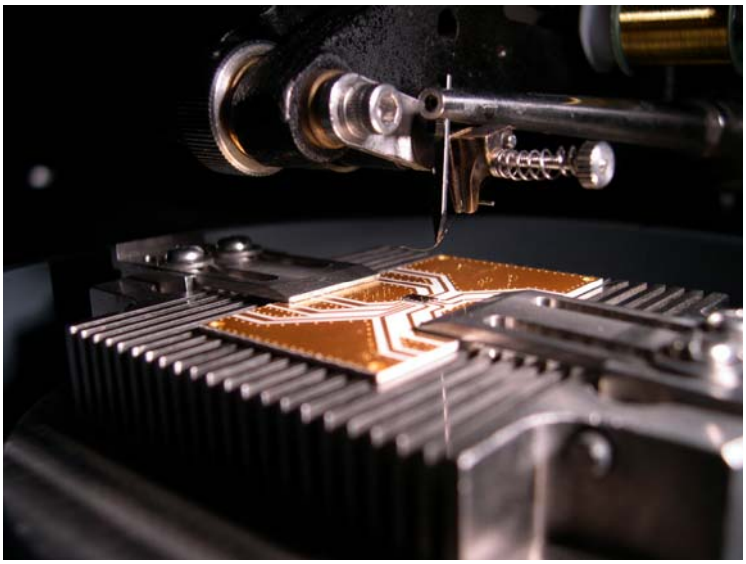


Figure 33. Evaluation board for the 6-bit pin-diode phase shifter

Other Results

Technology Transfer/Intellectual Property

The PIN diode may potentially be filed for IP protection. IP protection for attenuator, phase shifter and SPDT switches will also be considered.

Resulting Publications and Presentations

Le Wang, *et al.*, "A 15-GHz single-pole double-throw annular MOSFET switch for space application," *2005 IEEE workshop on Microelectronics and Electron Device.s*

Pinping Sun, *et al*., "High isolation 10HHz to 20 GHz SPDT switch design using novel octagonal pin diode structure," *2005 IEEE workshop on Microelectronics and Electron Devices.*

Pinping Sun, et al., "High Performance PIN Diode using 0.18-μm SiGe BiCMOS Process for Broadband Monolithic Control Circuits," submitted to *IEEE RFIC 2006 Symposium.*

Benefits to Commercial Sector

These radiation-tolerant SiGe BiCMOS MMICs are important building blocks for commercial space communication systems and they can be integrated with other functional components to implement system-on-a-chip solutions and reconfigurable systems for space communication, such as LEO satellite phase array communication systems.

Reference

[1] Reza Tayrani et al., "X-band SiGe monolithic control circuits," in *Proc. IEEE Topical Meeting Silicon Monolithic Integrated Circuits In RF systems*, 1998, pp: 126-134

[2] Reza Tayrani et al., "Broad-Band SiGe MMICs for Phased-Array Radar Applications," *IEEE Journal of Solid-state Circuits*, vol.38, No.9, Sept 2003, pp: 1462-1471

[3] Philip G. Neudeck, "Perimeter Governed Minority Carrier lifetimes in 4H-SiC p+n Diodes Measured by Reverse Recovery Switching Transient Analysis," *NASA Lewis Research Center*, 1998

[4] Ewout P.Vandemme et al., "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures," *IEEE Trans. Electron Devices*, vol.48, No.4, pp: 737-742

[5] David D. Heston et al., "100 MHz to 20 GHz Monolithic single-pole, two-, three- and four-throw GaAs PIN diode switches," Microwave Symposium Digest, 1991., *IEEE MTT- International*, vol.2, June 1991, pp:429 – 432

[6] Dave Krafcsik et al., "Broadband, low-loss 5- and 6-bit Digital Attenuators," *Microwave Symposium Digest, 1995., IEEE MTT-S International*, vol.3, May 1995, pp:1627-1630

[7] K.Oda et al., "DC and AC performance in Selectively grown SiGe-Base HBTs," *IEICE Trans. Electron*, vol. E82-C, pp. 2013-2020, 1999

[8] K. Washio et al., " A 0.2-μm 180GHz-fmax 6.7-ps-ECL SOI/HRS self-aligned SEG SiGe HBT/CMOS technology for microwave and high-speed digital applications," in *IEDM Tech. Dig*., 2000, pp.741-744

[9] M. Teshiba, R.-V. Leeuwen, G. Sakamoto, and T. Cisco, "A SiGe MMIC 6-Bit PIN Diode Phase Shifter", *IEEE Microwave and Wireless Components Letters*, vol. 12, issue 12, Dec. 2002

[10] R.-B. Garver, "Broadband diode phase shifter," *IEEE Trans. Microwave Theory Tech*., vol. MTT-20, pp. 314-323, May 1971

[11] Skyworks Corp. Application Note, "Design with PIN Diodes", Part No. APN1002

PROJECT 7

DIRECT DIGITAL FREQUENCY SYNTHESIZER FOR RECONFIGURABLE COMMUNICATION SYSTEMS

Prof. George La Rue (Washington State University) with Fong Shi (Boeing)

RESEARCH TIME PERIOD: Three years
RESEARCH FOCUS: AFRL Task Areas 2 and 3: Standard Cell/Topologies in Radiation-Hardened SOI and Reconfigurable Mixed-Signal Electronics and System-on-a-Chip Design.

Figures and Tables

Abstract

This project was to investigate direct digital frequency synthesizers (DDFSs) for space applications. DDFSs provide very fast frequency hopping, low phase noise and high frequency resolution, which are important requirements for many modern wireless communication systems. DDFSs are more versatile than VCO based synthesizers and are reconfigurable after deployment to meet a wide variety of

applications. This is important for space applications where the life of a mission can be very long, requirements may change and replacing electronics after deployment is usually not an option.

We investigated binary DAC and nonlinear DAC approaches for the implementation of DDFSs. The non-linear 12-bit DAC approach was selected and fabricated using Honeywell's radiation-tolerant MOI5 0.35 micron SOI CMOS process. This approach implements a 32-segment piecewise linear approximation to the sinusoid and only requires a lookup table of about 600 bits. The phase accumulator did not work properly but the DAC is functional. Measurements of DAC INL and DNL are less than ½ LSB at 12 bits after digital trimming. High speed testing shows good performance up to 600 MHz. With the DAC operating at 600 MHz, the spurious free dynamic range (SFDR) is above 70 dB for output frequencies below 3 MHz, above 60 dB for output frequencies below 20 MHz, and 47 dB at 100 MHz. Measurements at Boeing Radiation Effects Laboratory showed the DDFS could withstand a total ionizing dose of 200 krad Si with negligible degradation.

An improved DDFS was fabricated using Jazz Semiconductor's 0.18 micron process. Improvements include increased resolution of 14 bits yielding an SFDR above 80 dB in simulation, lowering power dissipation by at least a factor of three, and adding dynamic calibration capability for differential outputs. Radiation-hardened-by-design (RHBD) techniques are employed to provide total dose and single event upset tolerance. A method to generate accurate SPICE models of annular and other geometry FETs was developed. This increased the accuracy of performance predictions and allowed the optimization of the analog portions of the DDFS design.

Project Description

This project was to investigate low-power high-performance direct digital frequency synthesizers (DDFSs) implementations in silicon-on-insulator (SOI) CMOS technology for space applications. DDFSs allow for very fast frequency hopping, a requirement for many modern wireless communication systems. In addition, they have higher frequency resolution along with lower phase noise than phase-locked loop (PLL) solutions. High speed DDFSs can produce sinusoidal waveforms over a wide range of frequencies in addition to their high frequency resolution. As a result, communication systems that use DDFSs are more versatile than VCO based synthesizers and are reconfigurable after deployment to meet a wide variety of applications.

Fast frequency switching (hopping) is very important in modern wireless communication systems. Linear phase shifting is also critical in any system that uses phase shift keying modulation techniques. DDFS can achieve fast frequency switching in small frequency steps, over a wide band. It also provides linear phase and frequency shifting with quite good spectral purity. An additional requirement for DDFS is low power consumption.

A non-linear DAC DDFS was designed, laid out and fabricated using Honeywell's MOI5 0.35 m SOI CMOS process. This approach uses a piecewise-linear approximation (PLA) of the sine function which is implemented in analog circuitry inside the DAC. There have been many approaches to reduce the amount of look-up ROM. Some reduce ROM size at the expense of additional hardware such as adders and multipliers [1,2]. Other designs [3] use non-linear DAC architectures but limit performance far more than our non-linear DAC approach, which has performance comparable to binary DACs. With 32 segments an SFDR of about 80 dB is obtained assuming an ideal implementation of the 12-bit DAC. The ROM size is 32 by 19 bits for a total of 608 bits. Simulations show an SFDR of greater than 70 dB for differential outputs up to 300 MHz. The phase accumulator is 24 bits and provides a frequency resolution of 128 Hz.

Measurements of the DAC integral nonlinearity (INL) and differential nonlinearity (DNL) errors are less than ½ LSB at 12 bits after digital trimming. Tests of the phase accumulator show some pattern dependent errors and could not be used to stimulate the DAC at high speed. Measurements show that with the non-linear DAC operating at 600 MHz, the SFDR is above 70 dB for output frequencies below 3 MHz, above 60 dB for output frequencies below 20 MHz, and 47 dB at 100 MHz. The DAC was stimulated with the top 8 bits of the binary portion of the DAC along with the nonlinear portions of the DAC in these tests. Measurements at Boeing Radiation Effects Laboratory showed the DAC could

withstand a total ionizing dose (TID) up to 200 krad Si while the phase accumulator could withstand a total dose of up to 400 krad Si.

An improved DDFS was fabricated using Jazz Semiconductor's 0.18 micron process. We used hardening-by-design techniques to mitigate both TID and single event effects (SEE). A method to generate accurate SPICE models of annular and other geometry FETs was developed. This allowed us to better predict performance and optimize the analog portions of the DDFS design. Simulations show at least 80dB SFDR beyond 100 MHz, commensurate with the higher resolution. We have reduced the look-up table size to 480 bits with a 16-segment piecewise-quadratic approximation (PQA). We are using RAM instead of ROM to allow flexibility in waveform generation. The squaring of a 5-bit number is required in the PQA but can be implemented in about 50 logic gates. We have developed an approach that allows the phase accumulator (PA) to be implemented in parallel to lower power dissipation. The number of bits in the phase accumulator will be increased to 32 bits to provide a frequency resolution of 0.5 Hz. Triple-mode redundancy is implemented on the critical logic and registers for SEU mitigation. Digital trimming will be implemented with dynamic calibration for differential outputs. After packaging and performance characterization, measurements of the tolerance to total dose radiation are planned at the Boeing Radiation Effects Laboratory (BREL). Measurements of the tolerance to single-event upsets are also planned.

This work, in conjunction with Boeing, will result in radiation-hard high-performance DDFSs with low power and high SFDR. The circuit fabricated at Honeywell has resulted in a state-of-the-art radiation-hard nonlinear 12-bit DAC. The 14-bit DDFS being laid out has several innovative features providing higher frequency resolution, higher speed, lower power dissipation and increased SFDR along with SEU and total-dose hardness. As a byproduct of this research, a state-of-the-art technique was developed for accurate modeling of FETs with annular and other arbitrary gate geometries commonly used in hardened-by-design circuits. A DDFS is an important building block that is reconfigurable after deployment to meet a wide variety of applications in space communication systems. Its superior hopping ability allows for use in more system applications than analog synthesizers. This building block can later be integrated with more functions to provide system-on-a-chip solutions.

Research Results and Discussion

DDFS Architecture

VLSI technology has supported the wide use of DDFSs, but the new requirements of modern communication systems are imposing stringent demands on DDFSs' agility and power consumption. Most DDFSs are composed of the same building blocks, based on an idea presented by Tierny et al. [4]. The first block is an m-bit phase accumulator (θ), while the second block is a sine function ROM lookup table. The accumulator is updated on each clock cycle, and w ($<$m) of its output bits addresses the ROM lookup table, generating a digitized sine value. This is converted by a DAC to analog form and filtered. The ROM-based conversion of the phase θ into $\sin(\theta)$ is a crucial step because the size of the ROM directly influences power, area and performance.

For a DDFS with a 12-bit DAC and a phase resolution for a period of the sine wave also of 12-bits, a brute force approach would require a ROM with a 12-bit address and 11-bit words for a total of 44K bits. The most significant bit (MSB) of the address is the MSB of the amplitude and does not require any ROM. Using quarter wave symmetry of the sine wave and a complementor on the lower 10 bits, the ROM can be reduced to 11K bits with a 10-bit address and 11-bit words. Figure 1 shows a block diagram of the DDFS using quarter wave symmetry.

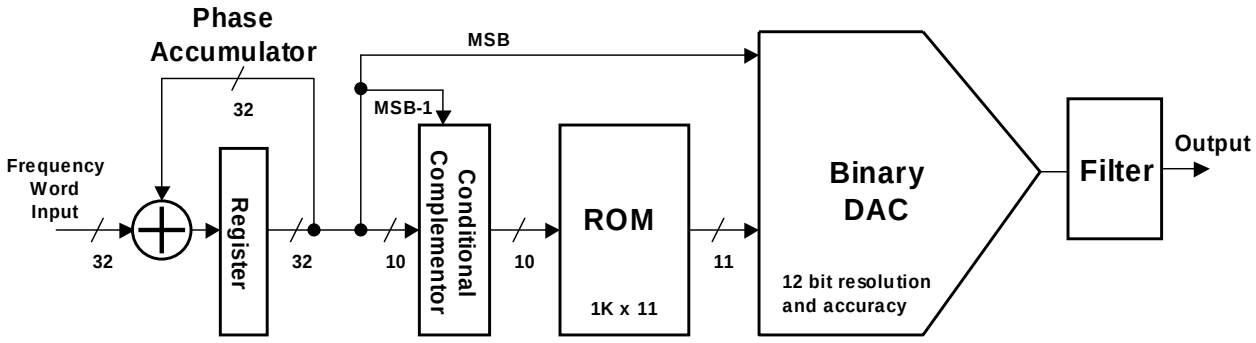


Figure 1. Block diagram of DDFS with quarter wave symmetry to reduce ROM size

When a standard binary DAC is used, many different approaches can reduce the size of the ROM lookup table(s) at the expense of higher power dissipation for the additional computation units. The research started with reviewing the state-of-the-art DDFSs and comparing the many different solutions-with a strong emphasis on recent ones. A first evaluation of the different solutions was done at the block level, trying to understand their strengths and weaknesses. As a result, ROM-less solutions were identified as prime candidates (mainly due to their drastically reduced power consumptions). Simpler architectures were than selected by a closer comparison of the remaining ROM-less solutions. This second filtering step revealed that some ROM-less solutions require multiplication (e.g., those using the parabolic approximation). These were discarded, as there are other solutions requiring only additions. Finally, the ROM-less solutions requiring only additions were ranked with respect to the number of adders they used, and the length of these adders. The conclusion of this analysis was that ROM-less solutions using only one multi-input adder (beside the phase accumulator) are feasible. These are based on piecewise linear approximations.

Matlab simulations were performed to compare the precision achievable with different approaches. Enhancements over the results reported in the literature were obtained, related only to the digital part of the DDFS. Our simulations show than an 8-segment approximation can achieve and SFDR only slightly over 60 dB. For a 16-segment approximation the SFDR is over 70 dB. A VHDL implementation of the digital part was tested on a Xilinx FPGA. Our solution reduces the maximum absolute error by almost a factor of 10 when compared with three segment, a different 8-segment and parabolic approximations.

The second approach is to use a non-linear DAC. Mortezapour and Lee [3] used a non-linear DAC, which employs many switches to directly fit a sine function. Because of the capacitive loading of all the switches it has a lower speed than a standard binary DAC. We developed a novel non-linear DAC architecture concept that is speed competitive with a standard binary DAC. The non-linear DAC architecture implements a piecewise linear fit to a sine wave using a small lookup table for the gain and offset of each segment. The gain and offset is then converted directly to analog with no digital adders or multipliers needed. Matlab simulations of our non-linear DAC approach show that a ROM lookup table of 672 bits is sufficient to obtain an SFDR near 80 dB with an ideal digital-to analog converter. Figure 2 shows a block diagram of the DDFS using the nonlinear DAC approach. The phase accumulator is the same as in Figure 1 and is not shown. The digital adder and multiplier are only shown for functionality and are implemented as part of the nonlinear DAC.

We chose to implement the DDFS using the non-linear DAC approach because the complexity of the digital circuitry and the power dissipation are lower.

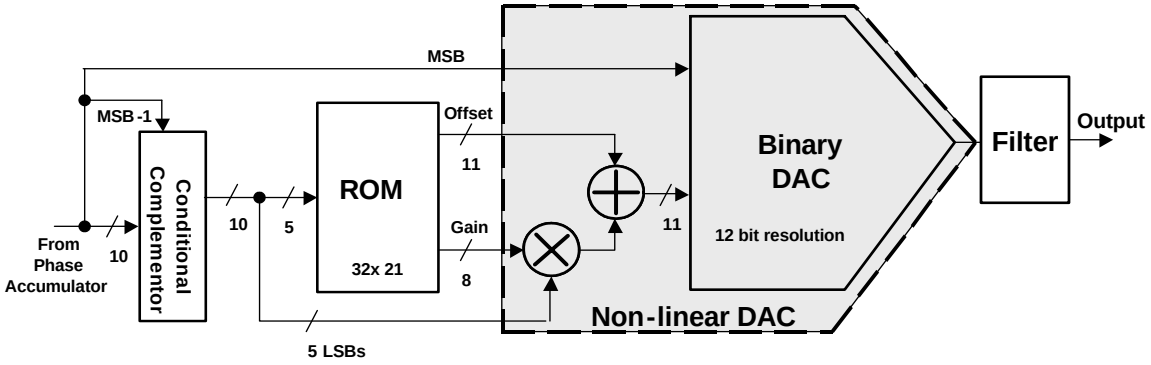


Figure 2. Equivalent block diagram of DDFS with nonlinear DAC architecture (PA not shown). The digital adder and multiplier are only shown for functionality and are implemented as part of the nonlinear DAC.

Digital-to-Analog Converter Design

A 12-bit DAC was designed to operate up to 2 Giga-samples per second (GSps) in Honeywell's radiation-tolerant MOI5 0.35 µm SOI CMOS process. A current steering design was chosen to achieve this performance [5]. The upper 5 bits are implemented as unary current sources in order to reduce glitches. Seven binary weighted current sources implement the lower 7 bits. The unary current sources and the 2 upper current sources on the binary portion are trimmed digitally to 1/8 LSB to ensure at least 12-bit accuracy.

The vernier DAC design was modified so that switching all occurred at the top level. An earlier design used vernier DACs for each of the 5 LSBs to form the linear term and only required 5 output switches. The drawback to this approach is that there is a delay from the vernier DAC outputs through the LSB switches that can cause timing errors, which can degrade the SFDR. To overcome this problem, we switched appropriately sized currents only at the top level with the partial products formed by the gain and the 5 LSBs. This is essentially a multiply but with the summing of the partial products done by adding currents. The drawback of this approach is that there are now 27 more switches at the top level. The binary DAC has 39 switches, 7 from the lower 7 bits and 32 from the top 5 MSBs, which are unary encoded to reduce glitches. The transmission lines for the differential outputs and the clocks to the final latches became 70% longer, which was acceptable.

Figure 3 shows simulation results of the DAC's spurious-free dynamic range (SFDR). SPICE simulations predict a differential SFDR greater than 70 dB up to 300 MHz assuming that an output filter attenuates the higher order harmonics above 300 MHz. Single-ended SFDR should be greater than 60 dB.

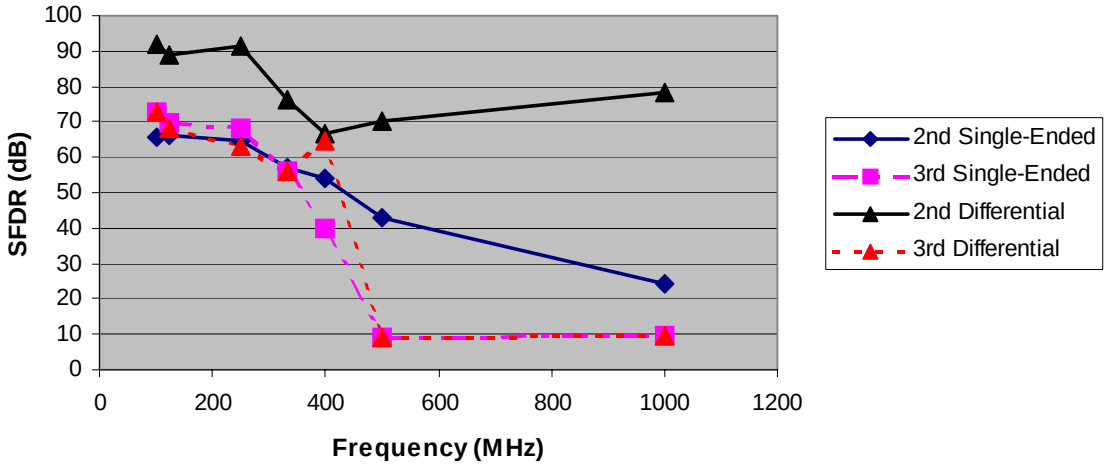


Figure 3. SPICE simulation results of SFDR using 12-bit non-linear DAC

Phase Accumulator

The phase accumulator adds the input phase word to the accumulated phase each clock cycle. It outputs the upper 12 bits to the ROM lookup table. In order to obtain phase accumulator operation near 2 GHz commensurate with the DAC, extensive pipelining was needed with the 0.35 micron MOI5 process. Four bit conditional sum adders were used in each pipeline stage.

The pipelining requires a substantial number of synchronizing registers, each of which is clocked at the maximum rate. The device sizes in these registers must also be large enough to drive the circuit at this maximum rate, resulting in substantial capacitance that must be charged and discharged each clock cycle. Not only did these extra registers add to the area but also there are only 2 levels of metal available with the MOI5 process making the area become even larger. The PA was limited to 24 input bits because of area considerations on the die. Simulations showed operation up to only 1.4 GHz. and power dissipation in excess of 1 W, primarily for the clock drivers.

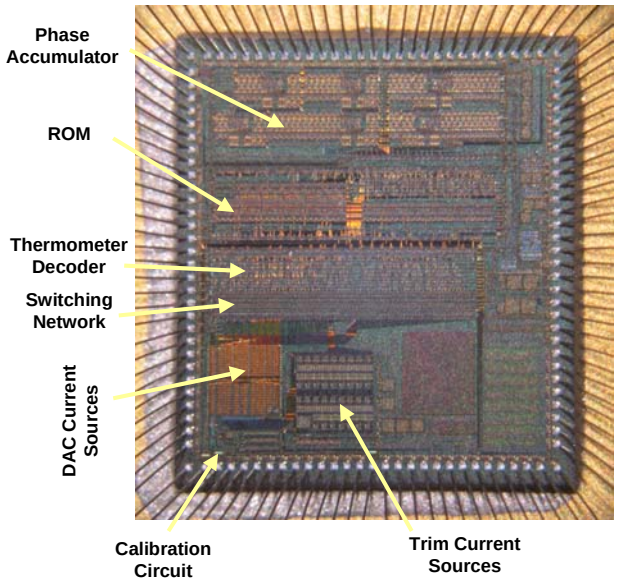


Figure 4. Microphotograph of the DDFS with major circuit blocks indicated

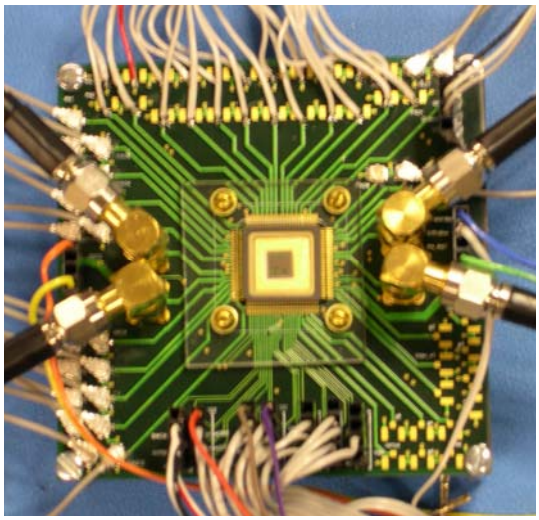


Figure 5. Photograph of DDFS mounted on printed circuit test fixture.

Figure 4 shows a chip microphotograph of the DDFS. The die size is 4.9 mm by 4.6 mm. The chip was packaged in a 128 pin quad flat pack. We added multiplexers between the output of the ROM and the binary and vernier DACs so the DACs can be tested separately from the DDFS. Simulations show operation up to 2 GSps for the DACs. The decoders have only 2 gate delays between pipelined registers for DAC operation up to 2 GHz. The phase accumulator has 3 gate delays between registers and limits the operation of the DDFS to about 1.4 GSps. Limiting the number of gate delays to 2 in the phase accumulator would have increased the number of pipeline stages, the area and also the power dissipation. Only a 24-bit phase accumulator was implemented due to area limitations.

A circuit board test fixture was designed and fabricated to test the DDFS chip at high speed. A socket was purchased and after extensive modification to accommodate longer lead lengths, provided reliable contact to the DDFS. A second circuit board was designed for low speed test to interface this socket to the test equipment. After a working chip was found, the packaged DDFS was soldered to the text fixture for high-speed test.

DC Test Results

A ripple counter used in the digital trimming circuit did not operate correctly due to unequal loading on the differential clock lines. The digital trimming circuit worked but the counter has large jumps in the output, which did not allow for very accurate trimming of the current sources. We were able to correct this by cutting traces in the counter using focused ion beam technology.

The differential non-linearity (DNL) and integral non-linearity (INL) of the 12-bit offset DAC was measured. The initial result showed very poor matching. The INL for the 31 unary current sources is within +12 LSBs and -20 LSBs, which is shown in Figure 6. The cause of the problem is due to the on-chip output resistors. After removing the on-chip output resistors using laser cutter, the INL is reduced to within +/- 4 LSBs, within the trimming range. The DNL is within +/- 1.2 LSB.

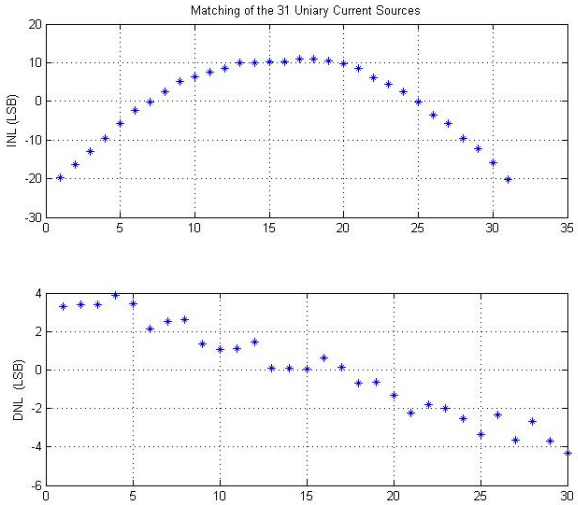


Figure 6. DAC DNL/INL with on-chip output resistors before trimming

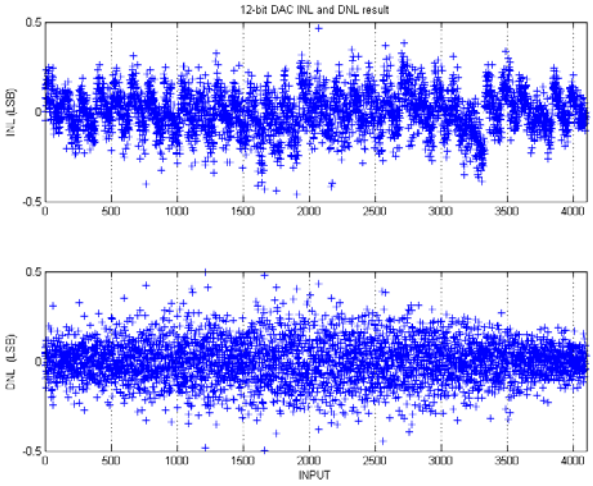


Figure 7. Measured DAC INL/DNL after trimming

The DAC DNL/INL measurement after calibration, including both the unary and binary weighted current sources, is shown in Figure 7. The overall DNL/INL errors are within ±0.5 LSB, verifying 12-bit accuracy.

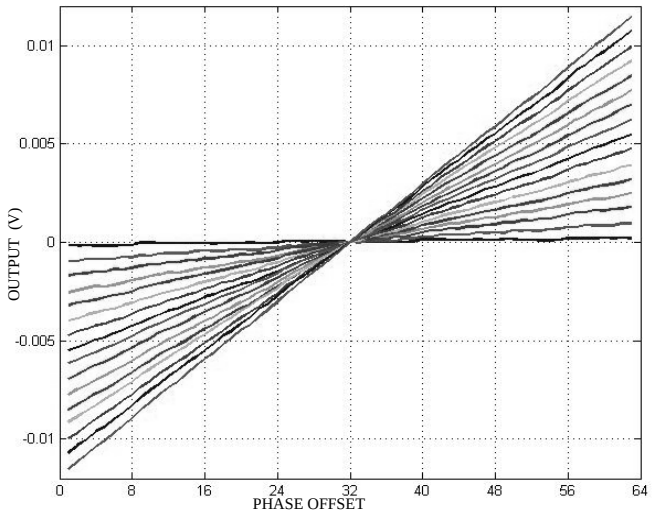
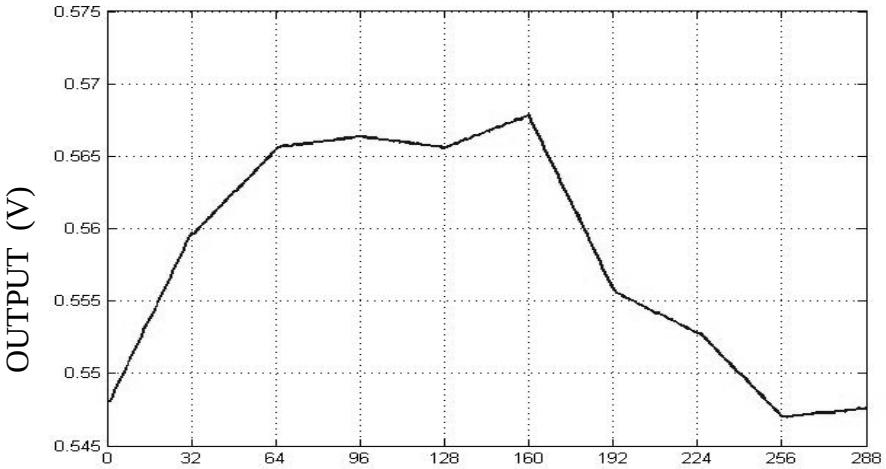


Figure 8. Variable gains of the vernier DAC

Operation of the vernier DAC was tested by providing gain bits and segment offset bits. Figure 8 shows 16 of the 256 possible gains. The figure was obtained by sweeping the segment offset from -31 to +31 for each of the 16 gains.

The non-linear DAC can generate a piecewise linear function and is not limited to just generating a sine wave. As an illustration, the combined output of the offset DAC and vernier DAC is shown in figure 9 with various offsets and gains to form a continuous waveform. Each segment consists of 32 points. The offset and gain words for each segment are shown in the table below the graph.



Offset	**2048**	**2172**	**2234**	**2234**	**2234**	**2134**	**2103**	**2041**	**2041**
Gain	**63**	**31**	**4**	**-4**	**12**	**-63**	**-15**	**-31**	**3**

Figure 9. Output wave with different offsets and gains

AC Test Results

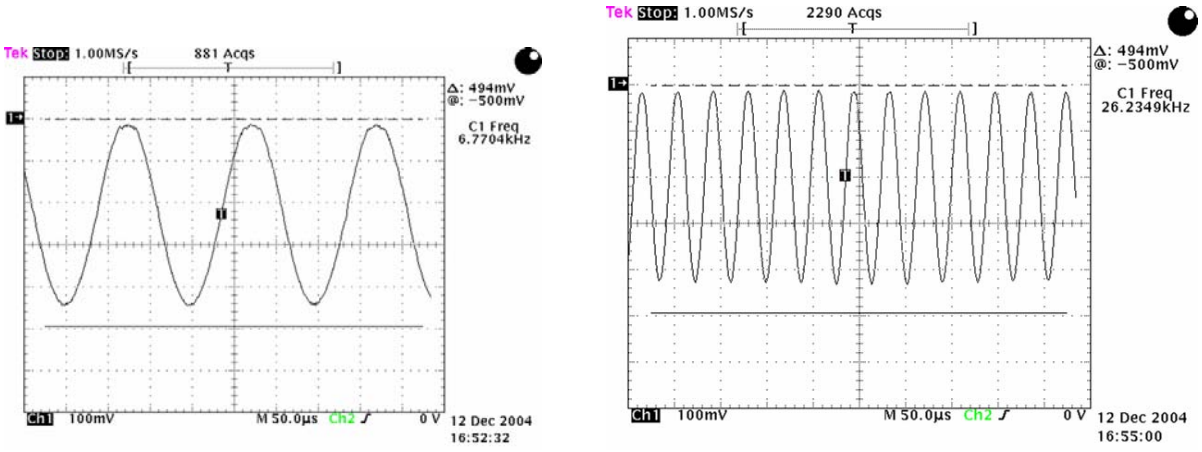


Figure 10. Two output waveforms of DDFS with a 20 MHz clock

The DDFS was tested with an input word applied to the phase accumulator and the output waveform is monitored on an oscilloscope. Figure 8 shows two waveforms from the DDFS operating at a 20 MHz clock frequency. The frequency of the sine wave changes with accordance to the control code. The system seemed functional. However, when the phase accumulator was measured by itself, we found its operation was not stable. Certain phase output bits were occasionally incorrect. We suspect errors are occurring due to timing mismatches due to high resistance in the long wiring runs along with the high capacitance of the large transistors used in the pipeline stages. We had widened the clock lines in the layout but were limited by area from increasing width further.

The non-linear DAC can be tested independently from the phase accumulator; driven with external inputs. Testing showed the non-linear DAC can be clocked up to 600 MHz. The spurious-free dynamic range (SFDR) at low output frequency is up to 72 dBc. Fig. 11 shows the spectrum of 98 MHz output frequency at 600 MHz clock. The second harmonic is -48.33 dBm while the fundamental is -1 dBm, which gives an SFDR of 47.33 dBc. Fig. 12 (a) and (b) show the waveforms of 27 MHz and 166 MHz outputs, respectively. When the chip is clocked at 600 MHz, the measured spectrum of 1.25 MHz, 13.5 MHz and 166 MHz outputs are shown in Fig. 13, Fig. 14 and Fig 15 respectively. At 1.25 MHz output, the third harmonic is dominant and the SFDR is 69.17 dBc. The second harmonic becomes the dominant one at 13.5 MHz output. The SFDR is measured to be 64 dBc. Fig. 16 shows the relationship between the SFDR and output frequencies.

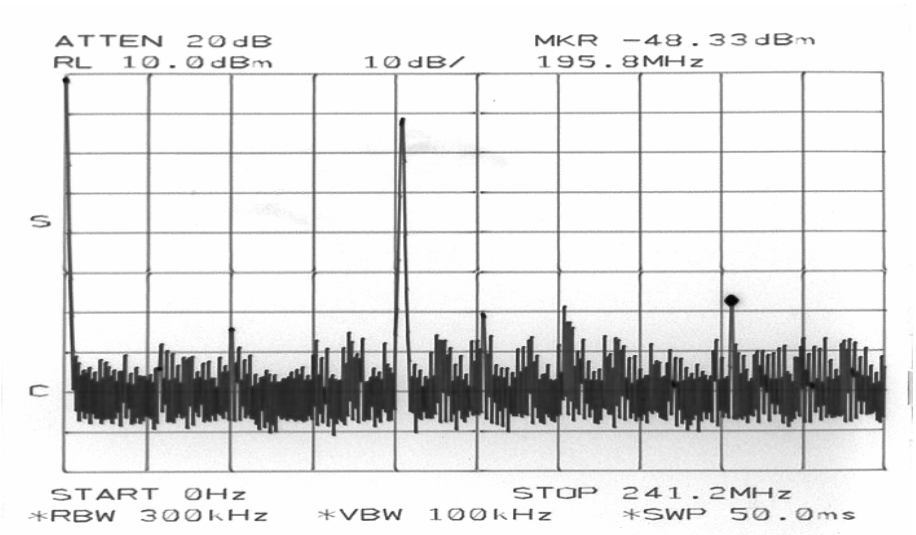
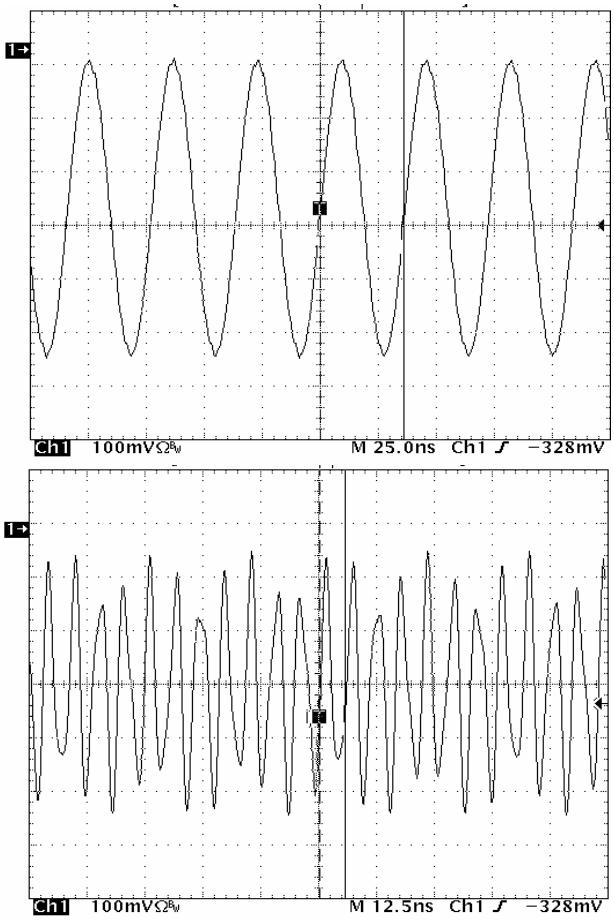


Figure 11. Spectrum of 98 MHz output frequency at 800 MHz clock



(a) (b)

Figure 12. Output waveform of 27 MHz and 166 MHz

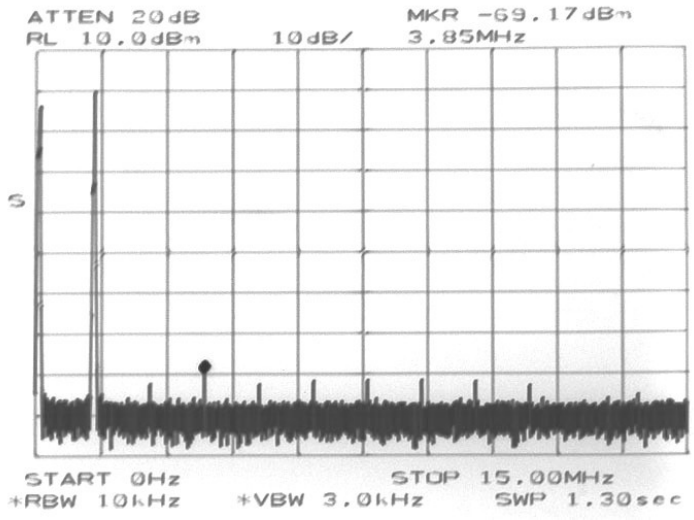


Figure 13. Spectrum of 1.25 MHz output frequency at 600 MSps

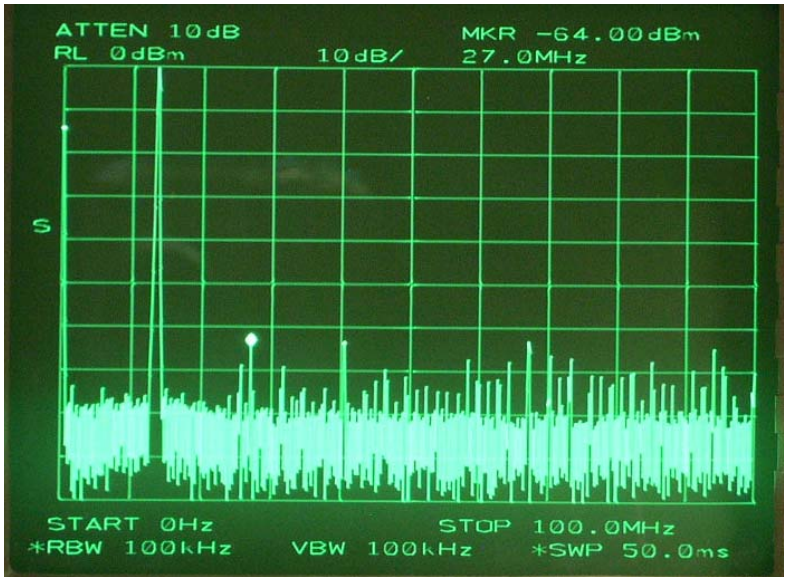


Figure 14. Spectrum of 13.5 MHz output frequency at 600 MSps

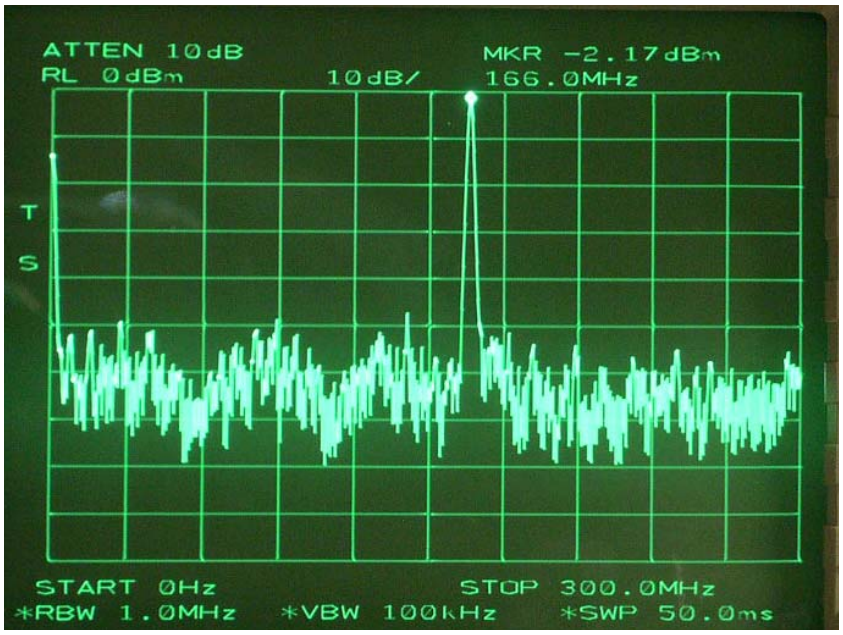


Figure 15. Spectrum of 166 MHz output frequency at 600 MSps

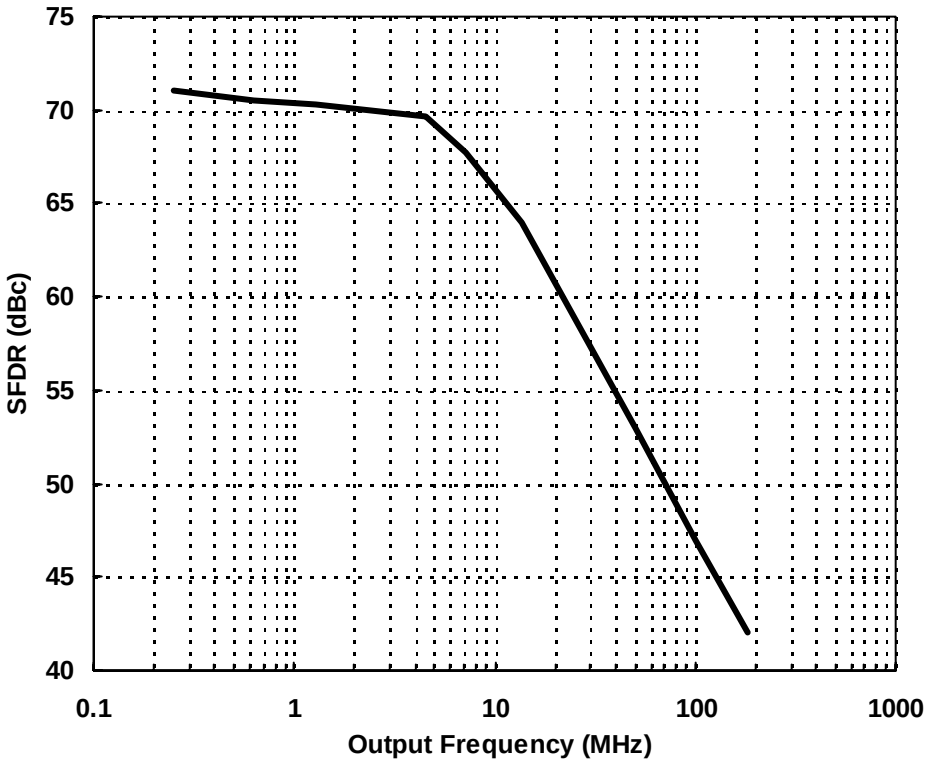


Figure 16. SFDR versus output frequency at 600 MSps

It took much longer to characterize and debug the DDFS chip. Finding a solution for mounting the packaged chip to the test fixtures added time. Waiting for the laser cutter to be repaired, attempting to fix the counter and then sending the chip to be repaired using focused ion beam technology added another 4 months. Reducing noise in the dc test setup and learning how to digitally trim the DAC required more

time than expected. Testing at high speed is made difficult because the phase accumulator does not working properly. The nonlinear DAC has 24 external inputs that must be provided for characterization at high speed. We used 8 channels from a 2.5 GHz pattern generator and used digital outputs from a TEK AWG520 arbitrary waveform generator to provide 14 more outputs up to 1 GHz.

Radiation Testing

A Honeywell DDFS chip was measured for tolerance to total ionizing dose (TID) at Boeing Radiation Effects Laboratory. The DAC current sources showed only minor changes up through 150 Krad Si. The INL error of the lower 6 bit binary DAC increased 30% at 200 Krad but was still much less than 0.5 LSB. Fig. 17 shows the lower 6-bit binary DAC measurements before and after 200 Krad Si total dose. At 250 Krad Si TID, two current sources in the lower 6 bit DAC turned on hard, causing very poor DNL and INL. For the 5-bit unary DAC, only minor changes occurred up through 200 Krad but 2 current sources started leaking significantly at 250 Krad. The power supply currents had shown no changes up to 250 Krad but changed slightly at 300 Krad. The DDFS worked up to 300 Krad but after another 100 Krad dose, it was not working. Power supply currents were significantly different. Varying power supply voltages did not help the device to function. The phase accumulator continued to operate, even at 400 Krad Si.

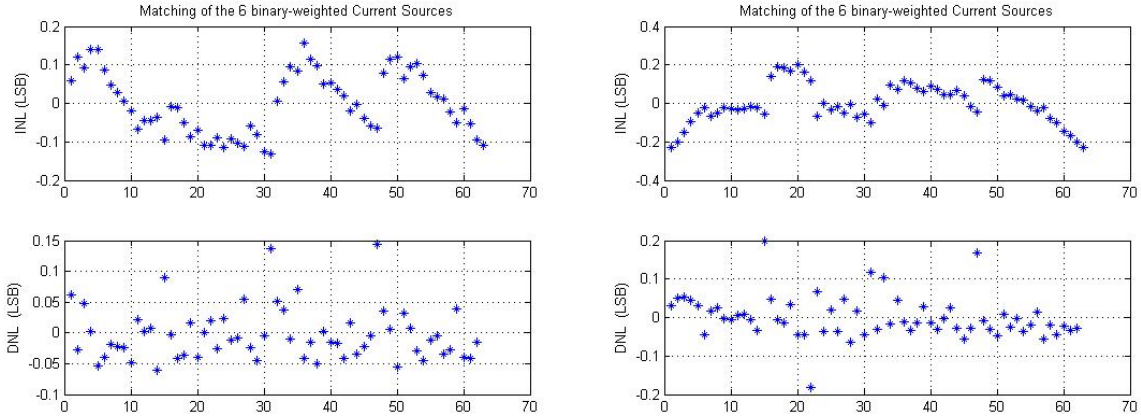


Figure 17. INL and DNL at before radiation and after a total dose of 200 Krad Si showing only small changes

Comparison with other DDFSs

The non-linear DAC chip is compared with other DDFS DACs in Table I. Since the DAC is the limiting factor of the DDFS performance given the digital processing is accurate enough. The DAC will determine the overall performance of a DDFS. Compared with other DDFS DACs, our non-linear DAC achieves the highest SFDR at very high operating clock frequency. The non-linear DAC can perform multiplication in the analog domain and simplifies the digital circuit design and increases the potential to operate at higher speed.

TABLE I. COMPARISON WITH OTHER DDFS DACS

Chip	Technology	Core area	Power supply	Clock	Resolution	SFDR (dBc)
Yang [6]	0.35 um CMOS	1.3 mm^2	3.3 V	800 MHz	9 bits	55
Vankka [7]	0.8 um BiCMOS	3.9 mm^2	5 V	170 MHz	10 bits	60
Yamagishi [8]	0.5 um CMOS	15.0 mm^2	2V	80 MHz	10 bits	69
Edman [9]	0.8 um CMOS	3.8 mm^2	5 V	350 MHz	8 bits	50
Kosunen [10]	0.5 um CMOS	9.0 mm^2	3.3 V	150 MHz	10 bits	57
Jiang [11]	0.25 um CMOS	1.4 mm^2	2.5 V	300 MHz	11 bits	62
This work	0.35 um CMOS SOI	5.0 mm^2	3.3 V	600 MHz	12 bits	72

Improved DDFS

We investigated ways to improve the performance of the first DDFS. The goal was to improve the SFDR to 80 dB, lower power and die area, increase speed to 2 GHz and harden the design against SEUs. We chose to implement the second DDFS using Jazz Semiconductor's 0.18 micron CMOS process to achieve 2 GHz operation and decrease power and die area. With this commercial process, hardness by design techniques must be used for total dose and SEU hardness. A method to generate accurate models of annular and other enclosed gate geometry FETs was developed to provide the precision required in this mixed-signal design. We investigated approaches to achieve the increased SFDR with minimal increase in circuit complexity and ways to decrease phase accumulator power.

Accurate SPICE Models of FETS with Arbitrary Geometry

For deep sub-micron technologies, the gate oxide is thin enough so that charge trapping from total ionizing dose (TID) is minimal and device thresholds do not change significantly. However, after exposure to TID radiation, rectangular-gate n-channel transistors exhibit large threshold shifts where the gate overlaps the thicker field oxide and leads to high leakage between source and drain. High tolerance to TID can be achieved by laying out the n-channel transistors by surrounding the source and/or drain with thin gate oxide. Fig. 18 and 19 show layouts of two such edgeless transistors, an annular FET and gate-around-source (GAS) or gate-around-drain (GAD) FETs. The foundry SPICE models are for transistors with rectangular gates and accurate SPICE models are needed for analog design.

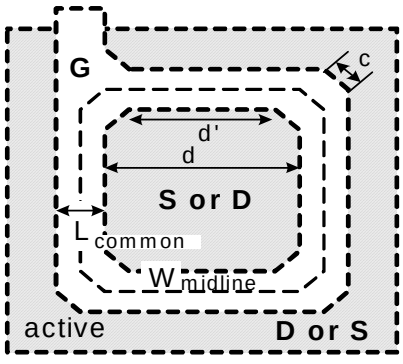


Figure 18. Annular FET layout showing the common length and midline width.

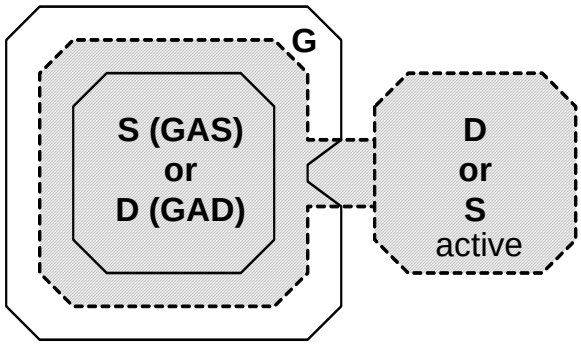


Figure 19. Layout of a GAS or GAD FET

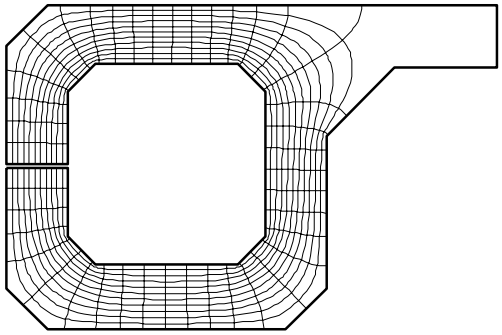


Figure 20. Equipotential and field lines for an annular FET generated with conformal mapping using the SC transformation.

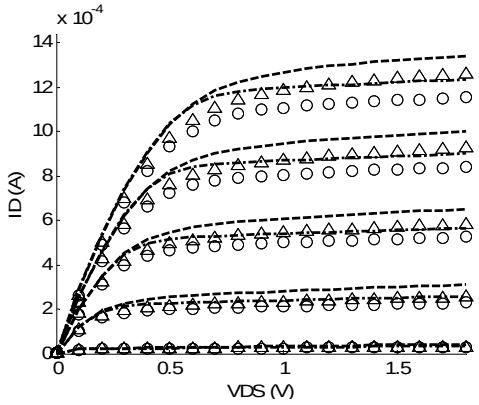


Figure 21. Measurements of small 0.18 μm annular in 0.18 μm process. Drain inner/outer measured (triangle/ circle) and modeled with current limiting correction (bold dashed/bold dot-dashed lines).

We use conformal mapping with the Schwartz-Christoffel (SC) transformation to solve for the potentials and field lines in the gate region. Fig. 20 shows the equipotentials and field lines of an annular FET. We divide the channel into N regions along the field lines and model the transistor as N transistors in parallel. The length Li for region i is determined by the average length of 10 field lines. The width Wi is determined by the length of the equipotential at 50% of the voltage between the source and drain, VDS. The output resistance ro is asymmetric due to the effect of channel length modulation being different depending on what side of the transistor is being used as the drain. We correct the output resistance in each region based on the length of the drain in that region. For annular gates, it was found that a single FET with appropriate W, L and PCLM values fits well to the models with many parallel FETs. This decreases SPICE simulation times and reduces the number of models required. The capacitances are also modeled more accurately than previously reported. Model generation is computationally efficient, taking only minutes on a laptop computer.

For annular FETs, model predictions for the average of IDS over several gate-source voltages is within 17% and the average ro is within 16% of measured annular devices on two wafers in TSMC's 0.18 μm and 0.25 μm technologies. An empirical correction to account for current crowding reduces differences in the averages of IDS to 9% and typically within 10% for averages of ro. Output resistance predicted by other models for annular FETs often has errors in the 20% to 40% range. Fig. 21 shows the measured and predicted values for a small annular FET in TSMC's 0.18 25 μm technology. The errors in IDS are the largest for this device among all 8 annular devices characterized.

The minimum W/L ratio of annular devices is large and the DDFS needs devices with smaller W/L ratios. We use GAS or GAD transistors and use our model generation routines on these channel shapes. Accurate modeling of the capacitance for the gate around FETs requires an additional device. The potential of the channel is nearly that of the surrounded node along the sides and opposite of the opposite node in the GAS or GAD device shown in Fig. 19. This region behaves like a MOS capacitor and can be modeled as a FET with source and drain both tied to the surrounded node.

Nonlinear DAC Design

We investigated piecewise linear and piecewise quadratic approximation approaches to achieve the increased SFDR with the least amount of ROM. The piecewise linear approximation (PLA) for the 12-bit DDFS required 32 segments with 12-bit offsets and 7-bit slopes for a total of 32 x 19 = 608 bits of ROM. The SFDR is about 78 dB with an ideal DAC and drops about 8 dB in our implementation according to SPICE simulations. Simulations show using a PLA with an ideal 14-bit DAC has an SFDR of 84 dB with 32 segments and SFDR of 96 dB with 64 segments. There is not sufficient margin to achieve 80 dB with only 32 segments. 64 segments are required and the amount of ROM is 1400 bits with the PLA.

Simulations using a piecewise quadratic approximation with an ideal 14-bit DAC and 16 segments achieves an SFDR of 98 dB with only 480 bits of ROM. 14-bit offsets, 11-bit linear and 5-bit quadratic coefficients are needed. There are 256 values per segment, an 8-bit number, but only the top 5 bits are squared and multiplied by the 5-bit quadratic coefficient to form the quadratic term. The squaring of a 5-bit number is implemented as discrete logic and can be implemented in under 50 gates. The complexity of the squaring circuit is much less than the additional 920 bits of ROM needed with the PLA. SPICE simulations of the improved DDFS show an SFDR is over 80 dB with a 14-bit DAC.

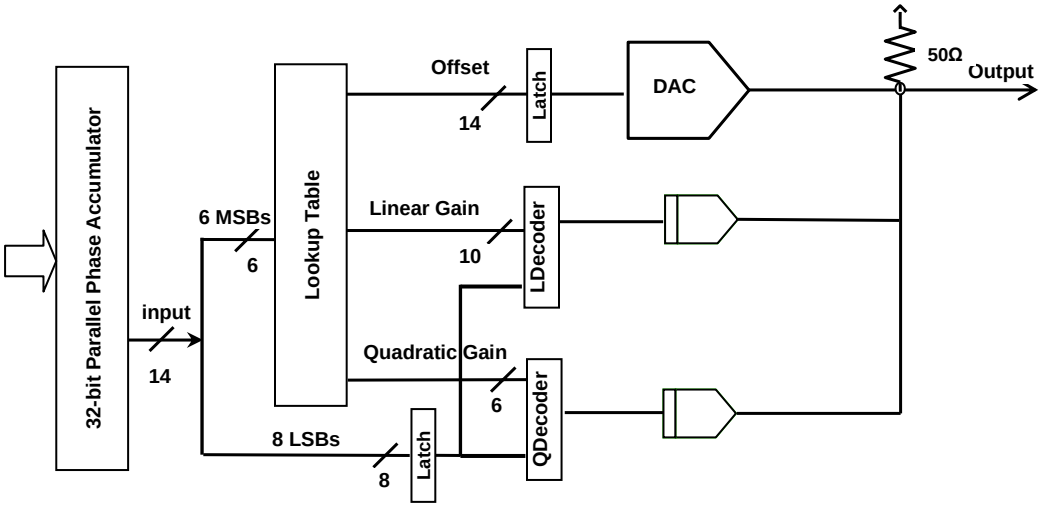


Figure 22. DDFS using 16-segment PQA approach

Figure 22 shows the block diagram of the DDFS consisting of a 32-bit parallel phase accumulator, a look-up table and a 14-bit non-linear DAC, which implements the 16-segment PQA. The non-linear DAC consists of three DACs: an offset DAC, a linear term DAC and a quadratic term DAC. Since the DACs are designed using current steering architecture, the addition of the terms is performed by summing the current at the output node.

The offset DAC is implemented as a 14-bit hybrid current-steering DAC. The top 5 MSBs are implemented using unary current sources and the 9 LSBs consists of 9 binary-weighted current sources. This hybrid architecture reduces the amplitude of glitches at the output. The linear term DAC is also a current DAC. It consists 9 sets of binary-weighted current sources with sizes in LSBs shown in Table 2.

Table 2. Multiplication by Summing Partial Products

	X_s	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1
G_{10}	510	256	128	64	32	16	8	4	2
G_9	255	128	64	32	16	8	4	2	1
G_8	128	64	32	16	8	4	2	1	1
G_7	64	32	16	8	4	2	1	1	
G_6	32	16	8	4	2	1	1		
G_5	16	8	4	2	1	1			
G_4	8	4	2	1	1				
G_3	4	2	1	1					
G_2	2	1	1						
G_1	1	1							

The multiplication in the linear term DAC is done by summing partial products instead of using a digital multiplier. Table 2 helps to show how this is implemented. In Table 1, Xi (i=1 to 8) denotes the ith bit of the phase offset within a segment and Gk (k=1 to 10) the kth bit of the gain for the segment. Xs is the sign bit. These bits control 62 current sources with relative sizes given in the table. Current is switched to the output when both row and column control bits are high. Otherwise the current is switched to the complementary output. The LDecoder in Figure 22 consists only of AND gates. This implementation of multiplication enables the DAC to operate at high speed.

The quadratic term DAC was designed using a similar approach for multiplication. Note that quadratic gain coefficients are 6-bit words. Thus, only the lower 6 rows in Table 1 are implemented. The QDecoder has a 5-bit squaring circuit in addition to the partial product AND gates. The top 5 significant bits of the segment phase offset are fed into the squaring circuit, the output of which is then fed to the partial product AND gates. Only the top 6 bits of the squared result are needed to provide enough resolution, simplifying the implementation.

The look-up table is implemented using RAM instead of ROM to facility versatile operations. This DDFS can be programmed to output any periodic function approximated by the 16-segment PQA. This includes wavelet basis functions.

Because $\cos(\theta)=\sin(\pi/2 + \theta)$, the same table can be used to generate the complementary output. The RAM lookup table is broken up into two tables, one below 45˚ and one above 45˚. The sine lookup will access one table and the cosine lookup will access the other table. Therefore, the RAM can be designed to output the sine and cosine values at the same time and no extra RAM is needed.

To compensate for the current source matching error during the fabrication process, digital calibration and trimming is used. All unary current sources and the three largest of the binary-weighted current sources are digitally trimmed to a matching error of less than 0.5 LSB. Figure 23 shows one unary current source with the digital trimming circuit.

An additional reference current source, identical to the unary current sources, is used to calibrate the unary current sources. To ensure the unary current sources match the binary ones after calibration, the reference current source is can also be trimmed and must be calibrated to a value that equals the sum of all binary current sources plus 1 LSB (512 LSB or a unary current). Before calibrating the reference current source, the largest 3 binary current sources must be first calibrated to the sum of all lower LSBs plus 1 LSB. Therefore, three steps are required to calibrate the DAC. First, the largest binary current sources are calibrated using other binary current sources and an additional 1 LSB current source. Second, the reference is calibrated using all binary current sources and the one LSB current source. Finally, all the unary current sources are calibrated to the reference.

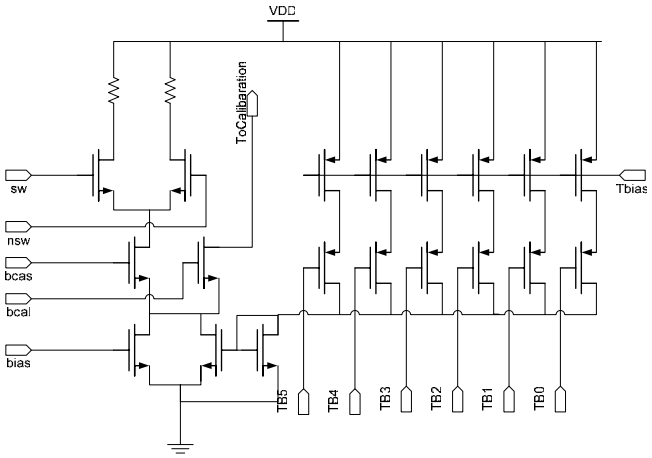


Figure 23. A current source with trimming circuit

It was difficult to obtain 80 dB SFDR using annular and gate around transistors. The W/L of the annular FETs is too large for switching the DAC current on the lower bits. Gate around source transistors were used for these switches, but they have a much higher C_{GS} capacitance and lead to transients in the output that give lower SFDR. The special flip-flops that drive the switches had to be customized for each of the four lower LSBs to reduce these transients and finally achieve the goal of 80 dB SFDR after filtering up to a bandwidth 500 MHz.

Parallel Phase Accumulator

We have also developed an approach that allows the phase accumulator (PA) to be implemented in parallel so that no pipelining is required. A block diagram of the PA with a parallelism of 4 and triple mode redundancy (TMR) is shown in Figure 24. The input phase control word is first demultiplexed into registers A1 – A4. Adding A1, A2, A3 and A4 to the previous value of register PA4 forms every fourth output. Adding the previous value of register PA4 to A1, A1 plus A2, and A1 plus A2 plus A3 form the other PA outputs. Additions with more than 2 inputs are required in determining all but the first output. The additional propagation delay is small compared to the increase in clock period due to parallelism. Compared to a 32-bit pipelined PA with TMR, power dissipation is about 30% less.

Upsets in pipeline registers in the nonlinear DAC logic and all but the last PA output only cause a single output glitch in the DAC. This may cause a bit error in communication applications but can be corrected using error-correcting codes along with the other errors from noise in the channel. The critical register is the PA4 register and the registers and logic that feed into it. An error here will cause a long-term phase error, which can cause many bits to be in error and may affect clock recovery. TMR is used to protect the input registers and the PA4 result from SEUs and SETs. Three different versions of the input into PA4 is be computed. Only A4 and A3 plus A4 need to be added to the results for PA3 and PA2 respectively in order to get two additional versions of PA4. The parallel approach reduces the overhead of generating additional PA4 inputs for voting.

The trim registers in the DAC and the RAM lookup tables will use hardened memory cells. SPICE simulations of the phase accumulator using TMR and annular FETs shows a power dissipation of 270 mW at 2 GHz. This is much lower power dissipation than the first DDFS design without TMR and operation much closer to 2 GHz is expected.

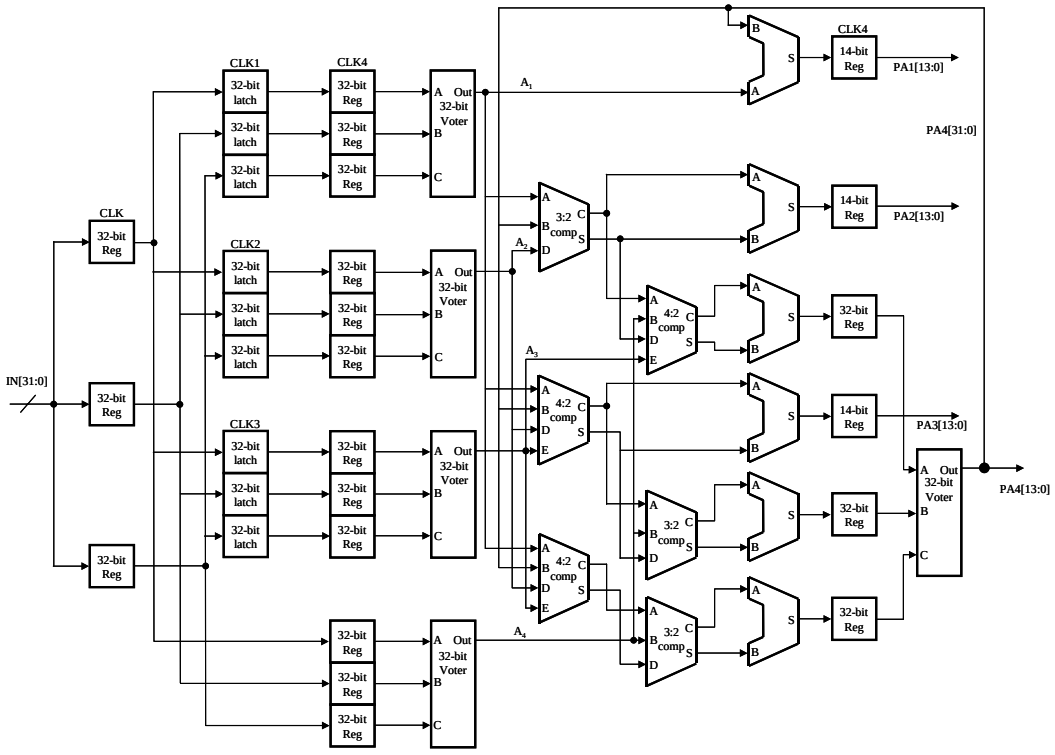


Figure 24. 32-bit M=4 Triply Redundant Parallel Phase Accumulator

Layout

The analog portions use guard rings for reduced inter-device leakage and use annular, GAS and GAD FETs. The digital portion of the DDFS uses digital standard cells with annular, GAD and GAS n-channel FETs along with guard rings to address radiation-induced latch-up and leakage. The digital standard cell library contains over 80 different cells. With the exception of latches and flip-flops, all of the cells were laid out using a program, called LGEN, written in C++. LGEN contains a hierarchical layout database and routines to add geometrical objects, ports, cells, text and attributes to the database. It outputs data in standard CIF format. With LGEN, the layout can be parameterized in terms of design rules and user parameters so that the layouts are independent of the process used. Figure 25 shows from left to right an inverter, a 2-input nand gate, a 2-input nand gate with twice the drive strength and a latch. The cell height is 11.4 microns. Guard rings surround the n-channel FETs in each cell. The latch uses GAS devices for the n-channel pass transistors in the latch. The time to initially develop this radiation-hard standard cell library using LGEN takes longer than using a traditional layout editor. However, subsequent changes to adjust transistor sizes for different drive strengths or to port the library to a different process are significantly reduced.

The 14-bit DDFS circuit has been fabrication at Jazz Semiconductor and a die photograph is shown in Figure 26.

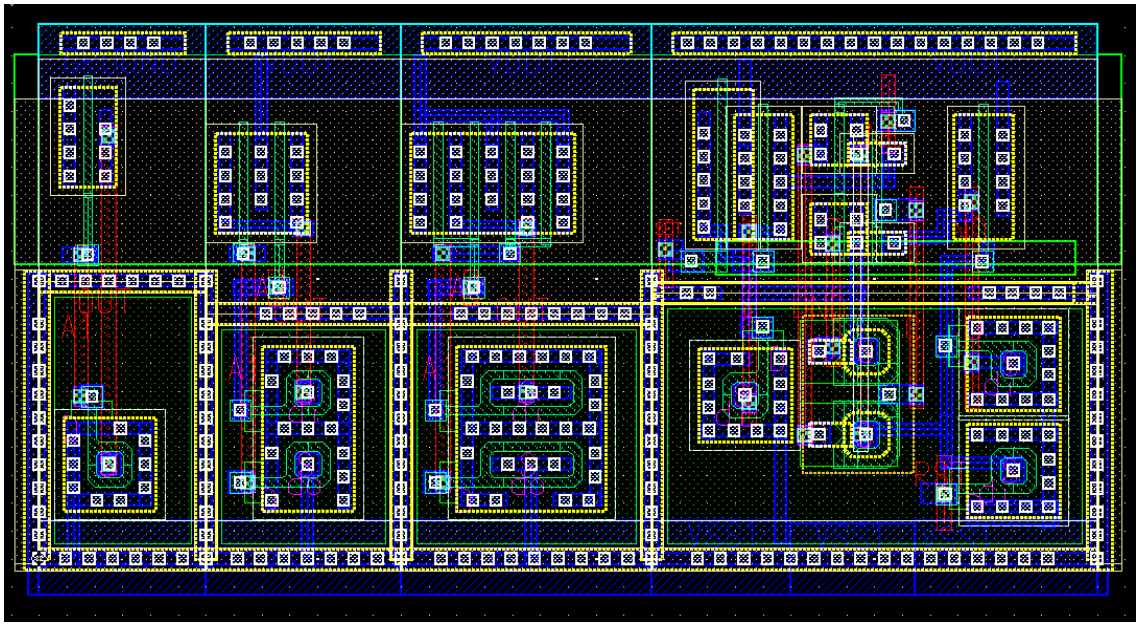


Figure 25. Layouts of 4 standard cells showing the guard rings and the use of annular and GAS FETs.

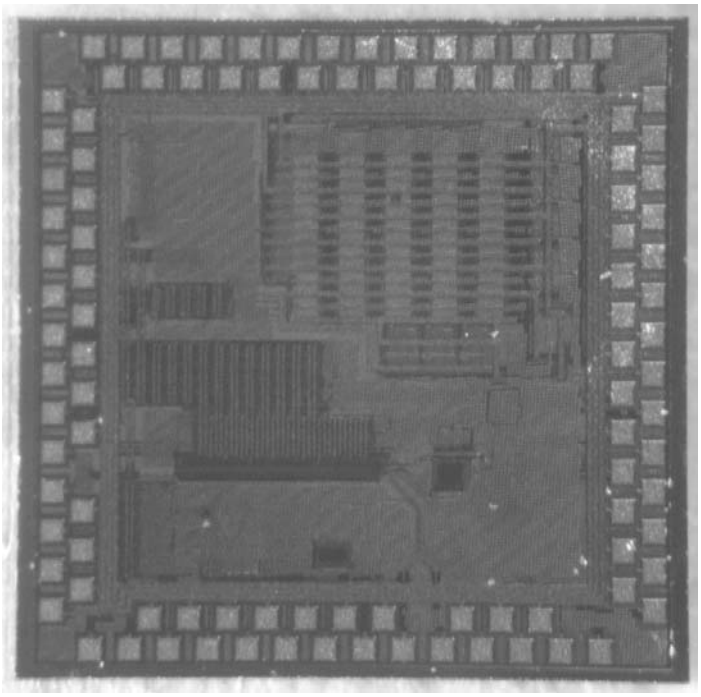


Figure 26. Die photograph of 14-bit DDFS

Summary of Results

A radiation-hard DDFS was designed, laid out, fabricated in Honeywell's MOI5 SOI process and tested. The approach of using a nonlinear DAC to reduce the size of ROM to 608 bits was verified. The nonlinear current-steering DAC operates to 600 MHz and showed a maximum SFDR of 72 dB, provides an SFDR of over 70 dB at output frequencies below 3 MHz and above 60 dB at output frequencies below 20 MHz. An accuracy of 12-bits was obtained by digital trimming the large current sources with current sources having 1/8 LSB resolution. Total ionizing dose testing at BREL showed the DDFS could withstand 200 Krad Si before the current sources were beyond the maximum trimming range. Table 3 shows a summary of the results of the 12-bit non-linear DAC.

An improved DDFS has been designed and fabricated which incorporates lessons learned from the first DDFS. The power dissipation of the phase accumulator led to the development of a lower power parallel phase accumulator architecture. The performance limitations of the 0.35 m MOI5 process with only 2 levels of metal led us to develop a method to generate the most accurate SPICE models for annular and other arbitrary gate geometry FETs used in radiation-hard-by-design. The SFDR is very sensitive to the design of the DAC current source switches and how they are driven. The accuracy of the capacitances and current-voltage characteristics in the models are critical in the improved design for obtaining an SFDR of 80 dB up to a 250 MHz output waveform. We also saw a need to add a bandgap reference to increase the power supply rejection on the bias of the 14-bit DAC.

TABLE 3. PERFORMANCE SUMMARY OF THE NON-LINEAR DAC

Technology	0.35 µM CMOS SOI
Core area	5mm^2
Power supply	3.3V
Power dissipation	120 mW at DC, 480 mW at 600 MHz
Resolution	12 bit
Maximum Clock Frequency	600 MHz
Output swing	0.5 Vpp
Output Resistance	50 Ω
SFDR	72 dBc at low output frequency 47 dBc at 100 MHz output
Radiation tolerance	Up to 200 krad Si total ionizing dose

This work, in conjunction with Boeing, has resulted in a state-of-the-art radiation-hard nonlinear DAC for DDFS applications. The improved DDFS design incorporates several innovative approaches and will provide higher bandwidth, higher SFDR, lower power and will be hardened against single event effects in addition to total ionizing dose radiation. A DDFS is an important building block for agile space communication systems. Its superior hopping ability allows for use in more system applications than analog synthesizers. This building block can later be integrated with more functions to provide system-on-a-chip solutions.

Other Results

Technology Transfer/Intellectual Property

Presentations

G. La Rue and V. Beiu, "Direct Digital Frequency Synthesizers," Boeing, February 5, 2003.

G. La Rue, "Direct Digital Frequency Synthesizers and SiGe Track and Hold Amplifiers," Boeing, April 26, 2005.

L. Champion and G. S. La Rue, "Accurate Modeling of FETs with Arbitrary Gate Geometries for Radiation Hardening," 4th Annual Rad Hard By Design Workshop, August 2004.

Intellectual Property

An invention disclosure was filed through Washington State University's Office of Intellectual Property Administration for a patent related to this project, entitled *High-Bandwidth Direct Digital Frequency Synthesizer*. U.S. Government DD Form 882, "Report of Inventions" is included in Appendix A of this report.

Publications Resulting from Research

Z. Zhou and G. S. La Rue, "A Radiation-Hard Non-linear DAC for DDFS," 12th NASA Symposium on VLSI Design, Coeur d'Alene, ID, October, 2005.

I. Howowitz and G. La Rue, "Parallel Phase Accumulator for DDFS," IEEE/EDS Workshop on Microelectronics and Electron Devices, April 2005.

Z. Zhou, I. Howowitz, G. La Rue, "Design of a Radiation-Hard DDFS," IEEE/EDS Workshop on Microelectronics and Electron Devices, April 2005.

Z. Zhou, I. Howowitz, G. La Rue, "Non-linear DAC Implementations in DDFS," IEEE/EDS Workshop on Microelectronics and Electron Devices, April 2004.

Z. Zhou, D. Betowski, X. Li, G. La Rue, V. Beiu, "High Performance Direct Digital Frequency Synthesizers," Proc. University/Government/Industry Microelectronic Symposium UGIM'03, June 30 – July 2, 2003.

S. Tatapudi and V. Beiu, "Split-Precharge Differential Noise-Immune Threshold Logic Gate (SPD-NTL)," Proc. International Work-Conference on Artificial Neural Networks IWANN'03, June 3-6, 2003.

V. Beiu, J.M. Quintana, M.J. Avedillo, and R. Andonie, "Differential Implementations of Threshold Logic Gates," Proc. International Symposium on Signal, Circuits and Systems SCS'03, July 10-11, 2003.

Benefits to Commercial Sector

DDFSs are an important building block in modern wireless communication systems. The result of this project will be a high-speed DDFS with low power dissipation. This will be of interest to the commercial wireless communication market, especially for mobile applications. At 2 GSps, the DDFS will provide the highest bandwidth of any CMOS DDFS and therefore have more potential applications.

References

[1] de Dinechin, F., and Tisserand, A., Some improvements on multipartite table methods. Technical Report RR-4059 [http://www.inria.fr/rrrt/rr-4059.html], CNRS-INRIA-ENS Lyon, France, Nov. 2000.

[2] Sodagar, A.M., and Lahiji, G.R., Mapping from phase to sine-amplitude in direct digital frequency synthesizers by using parabolic approximation. IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, 47(12), 1452-1457, 2000.

[3] Mortezapour, S., and Lee, E.K.F., Design of low-power ROM-less direct digital frequency sinthesizer using nonlinear digital-to-analog converter. IEEE J. Solid-State Circuits, 34(10), 1350-1359, 1999.

[4] Tierney, J., Rader, C.M., and Gold, B., A digital frequency synthesizer. IEEE Trans. on Audio and Electroacoustics, 19(1), 48-57, 1971.

[5] A. Van den Bosch, et.al., "A 10-bit 1 GSample/s Nyquist Current-Steering CMOS D/A Converter", IEEE J. Solid-State Circuits, vol. 36, pp. 315-324, March 2001

[6] B. D. Yang, J. H. Chois, S.H. Han, etc., "An 800-MHz low-power direct digital frequency synthesizer with an on-chip D/A converter", *IEEE J. Solid-State Circuits*, vol 39, no. 5, May 2004, pp. 761-774

[7] J. Vankka, M. Waltari, M. Kosunen, and K. A. I. Halonen, "A direct digital synthesizer with an on-chip D/A-Converter," in *IEEE Journal of Solid-State Circuits*, vol. 33, February 1998, pp. 218-227

[8] A. Yamagishi, M. Ishikawa, T. Tsukahara and S. Date "A 2-V, 2-GHz low power direct digital frequency synthesizer chip-set for wireless communication," in *IEEE Journal of Solid-State Circuits*, vol. 33, February 1998, pp. 210-217

[9] A. Edman, A. Bjorklid, and I. Soderquist, "A 0.8 µm CMOS 350 MHz quadrature direct digital frequency synthesizer with integrated D/A converters," in *Symp. VLSI Circuits Dig. Papers*, June 1998, pp.54-55

[10] M. Kosunen, J. Vankka, M. Waltari, L. Sumanen, K. Koli and K. Halonen, "A CMOS quadrature baseband frequency synthesizer/modulator," in *Analog Integrated Circuits Signal Processing*, vol. 18. pp. 55-67, Jan. 1999

[11] J. Jiang, and E. K. F. Lee, "A Low-Power Segmented Nonlinear DAC-Based Direct Digital Frequency Synthesizer," in *IEEE Journal of Solid-State Circuits*, vol. 37, October 2002, pp. 1326-1330

PROJECT 8

SOI CMOS CONTINUOUS-TIME DELTA SIGMA A/D CONVERTERS FOR SPACE COMMUNICATION RADIO RECEIVERS

Profs. Adrian Leuciuc and Alex Doboli (State University of New York at Stony Brook) with Bruce Ohme (Honeywell)

RESEARCH TIME PERIOD: Three years
RESEARCH FOCUS: AFRL Task Areas 2, 4, and 5: Standard Cell/Topologies in Radiation-Hardened SOI, System-on-a-Chip, and Predictive Radiation Effects Models.

Figures and Tables

Abstract

The research effort within this project is focused on developing low-power radiation-hardened Delta-Sigma A/D converters using SOI CMOS technology. Thorough analysis and design methodologies for the SOI analog cells based on the transistor-level simulation results and behavioral simulations at the system-level for a modulator have been developed and published. We have designed and simulated all individual analog cells and a complete continuous-time ΔΣ modulator for both radiation-free and single-event hits environments. All have been laid out and included on a test chip fabricated with Honeywell using radiation tolerant MOI5 process. The test and characterization of the prototype chip have been carried out. We also performed the radiation test using Tandem Van de Graff accelerator and found some errors under the single event hits.

Radiation hardening by design techniques are investigated, both at the system and circuit levels, for a specific class of mixed-signal systems: oversampling delta-sigma A/D converters. We are using a bottom-up approach for obtaining behavioral single-effect radiation models for all analog cells used in continuous-time ΔΣ modulators implemented in SOI CMOS technology. Behavioral simulations at the system-level characterize the effects of single event hits and maximal values for the duration and amplitude of the single-event transients are obtained for each building block in the system. The analog cells are then designed to meet the requirements of both radiation-free specifications and to achieve the

desired radiation immunity. Finally the fabricated prototype chip is tested in the radiation environment to check the effects of single event hits.

Project Description

This project responds to the AFRL solicitation on mixed-signal electronics technology for space by approaching a research topic concerning the design of radiation hardened, low-power, re-configurable A/D converters for radio receivers in space communications. To achieve the above requirements, our project focus on the Delta-Sigma oversampling A/D converters, which can realize an optimum trade-off between circuit complexity, cost, and power dissipation, high accuracy being achieved with low precision analog components [1].

Especially we select the continuous-time implementations of Delta-Sigma modulators proven to offer the advantages of lower power consumption and higher frequency operation compared to their switched-capacitor counterparts [2,3]. Moreover, considering the advantages the SOI technology presents in terms of power consumption, high frequency performance, and radiation hardness [4,5], our designs and simulations are based on Honeywell radiation tolerant MOI 5 process.

Basic analog cells for implementing continuous-time ΔΣ modulators have been designed in Honeywell's radiation tolerant MOI5 process: operational transconductance amplifier, biasing circuitry, comparator, current-steering DAC. The effect of radiation single events has been tested on these analog cells. We used the single event hit model for SOI transistors introduced in [6,7] to identify the critical devices in our circuits and to obtain behavioral models of the analog cells affected by single events. These models have been used to characterize the single event effects on ΔΣ modulators by appropriately augmenting the Simulink block-level diagrams. Extensive simulations have been carried out for single- and multi-bit Delta-Sigma modulators with different topologies, of different orders, using different oversampling ratios. The objective of this analysis is to be able to qualitatively and quantitatively predict the performance drop of Delta-Sigma A/D converters when affected by radiation single event transients. Based on the obtained results we are capable to predict maximal radiation single event induced errors for a prescribed ADC performance. Design methodologies for the SOI analog cells have been developed based on the behavioral simulation results. Power vs. speed and radiation hardness trade-offs have to be considered, depending on the specifications of the final application.

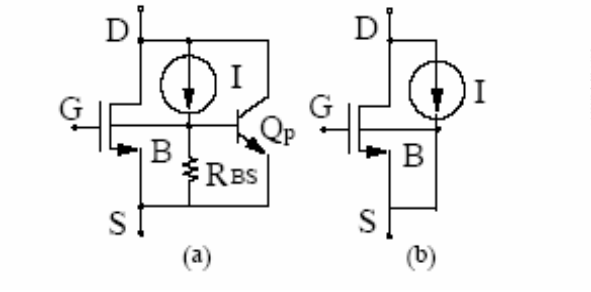
A prototype chip has been fabricated in Honeywell's MOI5 0.35μm partially depleted SOI CMOS process. The prototype chip includes operational transconductance amplifiers with different topologies to improve the linearity, the comparator that is used in the realization of the ΔΣ modulator, and the fourth-order, single-bit, continuous-time low-pass ΔΣ modulator. The modulator has been designed to achieve a signal-to-noise ratio of approximately 60dB (10-bits) in a bandwidth of 500kHz (1Msamples/sec), operating with an oversampling ratio of 32 (f=32MHz). For the first prototype, we didn't target a high-performance implementation, but only a vehicle to verify experimentally our behavioral simulations regarding the effects of single event hits. The fabricated continuous-time modulator achieves 63dB dynamic range (resolution >10bits), 63.73-dB SNR, and 59.84-dB SNDR over 500KHz signal bandwidth, while dissipating 12mW from a 3.3-V supply. We also performed the radiation test by using the Tandem Van de Graff accelerator in Brookhaven National Lab. With the constant DC input to the modulator, we found some errors from the decimated output.

Our work is innovative because it proposes to develop design methods to achieve radiation hardening for analog cells in SOI. Since the Honeywell's SOI process is relatively hardened to dose-rate and total dose effects, our work is focused on single event effects. The literature abounds in scientific papers dealing with single event effects in both digital and analog circuits. However, at least for the analog part, the majority of these papers are presenting experimental results obtained by irradiating commercial devices (op-amps, comparators, A/D converters) with heavy ions. Extremely few articles perform analytical studies (at the circuit level!) of single event effects on analog circuits and no design methodologies (excepting some layout techniques) are available for achieving single-event immune circuits. The main goal of our work is to develop such design methods and to apply them in the design of radiation hardened continuous-time ΔΣ A/D converters for space communications.

Research Results and Discussion

Analog cell design of continuous-time Delta-Sigma modulators and SET characterization.

Honeywell provided to the university team the Cadence process design kit for its MOI-5 process. All the basic building blocks required in a continuous-time ΔΣ modulator have been designed, simulated and tested for single event effects (a simplified model of the one introduced in [6] has been used, as shown in Figure1). Although the obtained results are not quantitatively precise (more accurate models, including the parasitic bipolar transistor parameters and the value of the body-source tie resistance, are needed), one could determine the shape, duration and amplitude of the transients induced by single-event hits. Figure 2 is an example of the single event current pulse represented by a double exponential with time constant s of t_1=10psec and t_2=200psec associated to the rise and fall times respectively. Some design rules for minimizing the single event effects are summarized below:



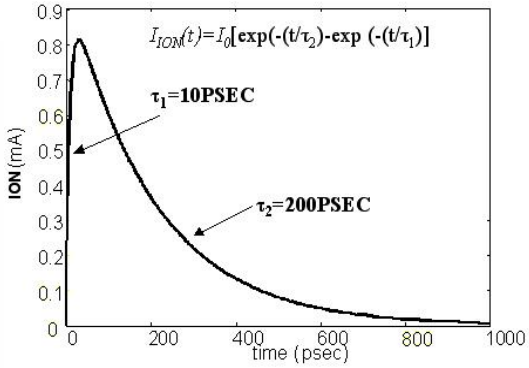


Figure 1: Single event effect model of SOI MOSFETS (a) proposed model (b) simplified model

Figure 2: Single event current pulse

Amplifiers

Single stage amplifiers are preferred for implementing the integrator (either active-RC or OTA C). In a single stage amplifier the charge generated within the body of the hit device will be dumped on the integrating capacitor. By choosing a large enough capacitor value, one can minimize the voltage error at the output of the integrator. In the case of a multi-stage amplifier, the error voltage generated in the first stage (which can be large if the capacitance at the output of the first stage is small) is amplified by the subsequent stage(s) and can eventually latch the amplifier. Therefore the amplitude and duration of the generated transients can be bigger. One has also to consider the fact that the single event transients generated in the biasing circuit (see discussion below) can affect the MOSFET transconductance. In the case of an OTA-C integrator this can affect its unit gain frequency, and consequently can change the frequency response of the filter the integrator is part of. One can eliminate this drawback by using resistor-based transconductors, solution that is also advantageous from the linearity point of view.

Biasing circuit

The errors introduced by the biasing circuitry into the main circuit are common-mode errors. Therefore, one can mitigate their effect by designing the main circuit with a high CMRR. However, the amplitude of the transients generated within the biasing circuitry should be maintained to a low enough level guaranteeing the correct operation of the main circuit. Therefore, large biasing currents (to increase the tranconductance of transistors) and large size devices (to increase their capacitance) are needed.

Comparator

The single-event transient has been analyzed in a high-speed comparator. A behavior single-event effect model for the comparator is proposed and Hspice simulations have been carried out to verify the validity of the proposed model. The concept of critical time is introduced and evaluated for a given circuit topology and parameters. It is a measure called critical time and defined as the time window around the regeneration-to-latch transition moment within which a SEE hit of a certain energy generates upset. The critical time can be used to predict the bit error rate by assuming a certain probability distribution function for the energy and the rate of single event hits. The total critical time is the sum between the critical time in the regeneration phase t_{cr1} and the critical time in the latch phase t_{cr2}. Modeling the preamplifier in Figure3 (a) as a voltage controlled current source driven by the input voltage v_{in}, and R_{latch} is the equivalent input resistance of the latch, having a R^+ positive value in the reset phase, respectively a negative value $-R^-$ in the latch phase as shown in Figure4 (a) and (b). The critical time in the regeneration phase is the solution of the equation

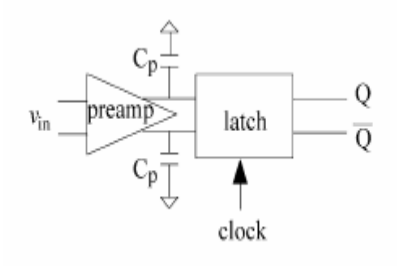


Figure 3: Simplified high-speed comparator structure.

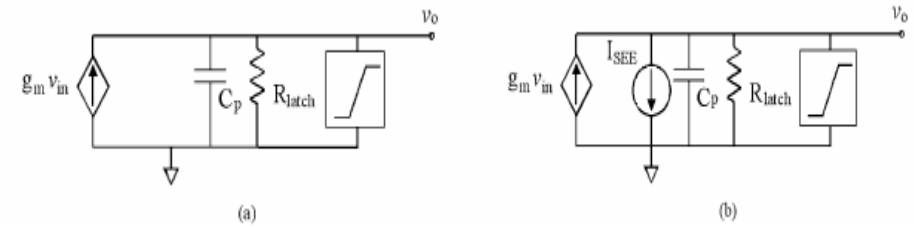


Figure 4: Equivalent single-ended model for a latched comparator:
(a) radiation free environment; (b) affected by SEE

$$-g_m R^+ v_{in} - \frac{R^+ I_0 \tau}{\tau - \tau^+}\left(e^{-t_{cr1}/\tau} - e^{-t_{cr1}/\tau^+}\right) = 0 \quad (1)$$

which does not have a closed analytical solution but in a single case, $\tau = 0$. This corresponds to modeling the SEE current pulse by a Dirac impulse carrying the finite charge $Q_{SEE} = I_0 \tau$. Thus, replacing $I_0 \tau$ by

Q_{SEE} in (1) and making $\tau = 0$, one has

$$t_{cr1} = \tau^+ \ln\left(\frac{Q_{SEE}}{g_m \tau^+ v_{in}}\right), \text{ where } \tau^+ = R^+ C_p \quad (2)$$

The critical time in the latch phase is the solution of

$$V_{reg} e^{t_{cr2}/\tau^-} - \frac{R^- I_0 \tau}{\tau + \tau^-} = 0 \quad (3)$$

or

$$t_{cr2} = \tau^- \ln\left[\frac{R^- Q_{SEE}}{g_m R^+ \left(\tau + \tau^-\right) v_{in}}\right] \tag{4}$$

If we assume $\tau << \tau^-$, the critical time in the latch phase is

$$t_{cr2} = \tau^- \ln\left[\frac{Q_{SEE}}{g_m \tau^+ v_{in}}\right] \tag{5}$$

Therefore, by modeling the SEE current waveform by a Dirac impulse, the total critical time t_{cr} becomes:

$$t_{cr} = t_{cr1} + t_{cr2} = \left(\tau^+ + \tau^-\right) \ln\left[\frac{Q_{SEE}}{g_m \tau^+ v_{in}}\right] \tag{6}$$

The larger the comparator time constants, the larger the critical time will be. This implies that the probability of the bit error will also be larger. Assuming that the amplitude of the current pulse which simulates the effect of the radiation has a normal distribution, the charge Q_{SEE} will also be characterized by a normal distribution with mean and standard deviation. A simple calculus shows that the distribution function of the critical time is:

$$F(t_{cr}) = P(t_{cr} \le t) = \Phi\left[\frac{v_{in} g_m \exp\left(\frac{t}{\tau^+ + \tau^-}\right)}{\sigma_Q} - \frac{\mu_Q}{\sigma_Q}\right] \tag{7}$$

where Φ is the cumulative distribution function of the normal distribution. If we assume that N is the number of particles per (second *mm^2) and the area of the tested device is A_{device}, then the bit error rate (BER) can be expressed as number of particles hitting a transistor with area A_{device} during $t_{cr}\left(NA_{device} t_{cr}\right)$. The distribution function of the bit error is:

$$P\left(e \le e_x\right) = \Phi\left[\frac{v_{in} g_m \tau^+ \left[\frac{e_x}{\left(\tau^+ + \tau^-\right) NA_{device}}\right]}{\sigma_Q} - \frac{\mu_Q}{\sigma_Q}\right] \tag{8}$$

where is e_x an imposed bit error rate (BER) value.

The above analysis shows that the comparator is quite insensitive to radiation single event effects occurring during the latch phase, but it is very sensitive to even small amplitude pulses that occur around the transition between the reset and latch phases. In order to decrease the probability of the error caused by radiation effect, the comparator should be designed as high-speed one (with very short regeneration and latch times), but it should be operated at low clock rates because our analysis shows that the SEU probability is directly proportional to the clock frequency and inversely proportional to the speed of comparator.

<u>One-bit D/A converter</u>

A couple of topologies implementing one-bit current steering DACs have been tested for single event effects. Since the need for a high output resistance requires the use of cascode configurations for the unit current sources, we have been faced with a critical issue. If the bottom transistor in a cascode stage is hit, one can rapidly eliminate the charge through the source of the top transistor that presents a low resistance. However, when the top transistor is hit, the charge accumulated within its body can be eliminated at a constant current, the one supplied by the bottom transistor that

operates as a current source. Thus, one can face long recovery times if the current source delivers a small current. One possible solution is to use voltage mode D/A converters and converting to currents through resistors connected at low impedance nodes within the integrators (lower speed operation). A possible solution is shown by figure5. By adding the operational amplifier *A*, the voltage at node 3 and node 4 will not change (virtual ground), due to the high gain of the operational amplifier. Then the voltage-mode feedback DAC can be achieved through resistor *R*1 and *R*2 by connecting their terminals to some reference voltage. The current generated by the input signal and the feedback DAC can still charge the integrating capacitor through transistor *M*3 and *M*4.

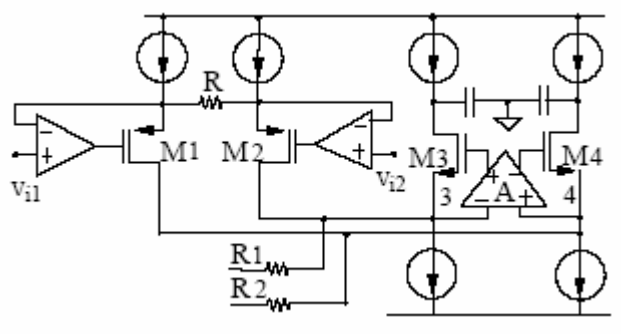


Figure 5: The voltage mode feedback DAC for Gm-C modulator

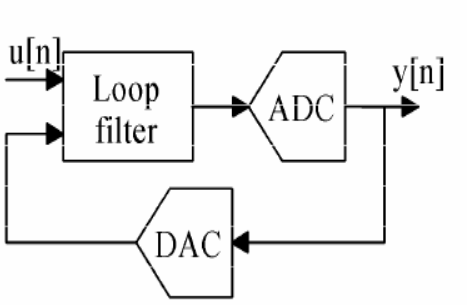
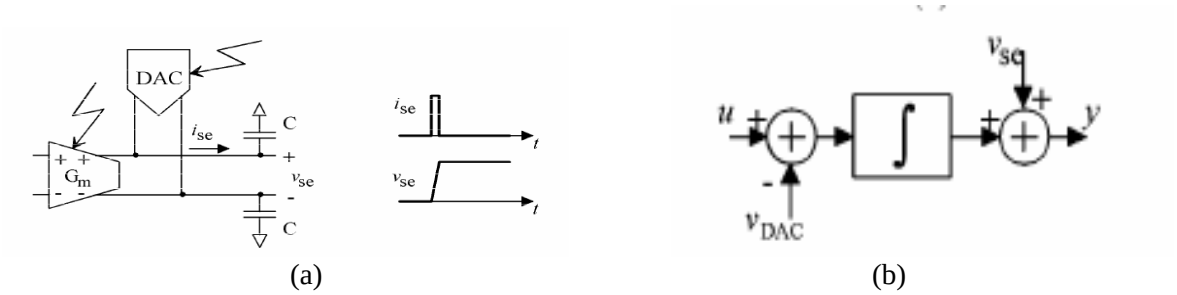


Figure 6: Diagram of Delta-Sigma

ΔΣ modulator system level design and SEE characterization

In a radiation environment, depending on what subsystem within the Delta–Sigma modulator is affected, one can have different effects. Figure 6. is the diagram of Delta-Sigma modulator. If the loop filter is hit the amplifier gain can change and the frequency response of the loop filter can be modified. Alternatively, the amplifier offsets can change or single-event transients (SET) can occur. In the case the internal ADC is irradiated, the comparators can exhibit larger offsets and/or bit flip-flops are induced (single-event upset, or SEU). The radiation effects on the feedback DAC include increased jitter, nonlinearity errors, and glitches.

The transconductor-C (or Gm-C) approach is the preferred one for implementing high frequency continuous-time filters. If the integrator is realized as a Gm-C one, a current-mode feedback DAC can be directly connected at the output of the transconductor, as shown in Figure 7(a). For high-speed operation both the operational transconductance amplifier (OTA) and the DAC require topologies without any high-impedance internal nodes. In this case, an ionizing particle hitting one device within the transconductor or DAC will ultimately generate a current pulse i_{se} flowing through one of the integrating capacitors (see Figure 7). Because the duration of the single-event current pulse is short in comparison with the time constant associated to the output node of the integrator and it is restricted to a single clock cycle, one can approximate the change v_{se} in the output voltage as a step function. Therefore, we developed a single-event behavioral model for the integrator–DAC stage shown in Figure 7(b). The amplitude of the perturbing voltage v_{se} depends on the amount of charge carried by the current pulse i_{se} and the value of the integrating capacitor.



(a) (b)

Figure 7: (a) Topology and single-event transients in a Gm-C integrator of a ΔΣmodulator; (b) behavioral model.

A database of Simulink diagrams for several single-bit, multi-bit, single-loop Delta–Sigma modulators (both low-pass and band-pass) of different orders and topologies [1] has been developed. These ideal modulator diagrams have been augmented with blocks modeling the SEEs at the cell level and the setup depicted in Figure 8 has been used to characterize the magnitude of the errors induced by SEEs. Two identical structures are driven by the same input signal, one of them being affected by single-event hits, and the other one assumed to operate in a radiation-free environment. Because we are interested only in characterizing the SEEs in the analog circuitry, it is assumed that the digital decimation filter is radiation hardened and no errors occur within. The output of the oversampling ADC affected by SEE is compared to the output of its error-free counterpart and the amplitude and duration of the SEE-induced error is measured. One has to remark that one cannot compare directly the outputs of the modulators because of their inherent operation principle. Two different one-bit output streams can carry the same information of the input analog signal, the difference between the modulator outputs being the result of the random quantization error. Therefore, any small transient in one of the two modulators or a different initial condition in one of the integrating stages will cause a permanent divergence in their output signals, although the decimated outputs may not be affected. The setup for testing band-pass Delta–Sigma ADCs includes a digital mixer for down-converting the input modulated signals before the decimation filter. Because all tested band-pass modulator structures employ a center frequency equal to one fourth of the sampling frequency, the mixing operation reduces to multiplying the signal at the output of the modulator with the repeating sequence (+1,0, -1,0).

For both low-pass and band-pass oversampling Delta–Sigma ADCs, the decimation filter has been implemented as a cascade between a finite impulse response (FIR) section with a sink^K type of frequency response, a down-sampling by (OSR/2) block, an infinite impulse response (IIR) filter with Butterworth frequency response, and a down-sampling by two block. The order of the FIR filter is large; therefore one can remark a delay between the SEE hit and moment the error occurs at the output. The effect of the IIR filter consists in propagating indefinitely very small errors at the decimated output. Therefore, errors of one least significant bit (LSB) will not be considered significant..

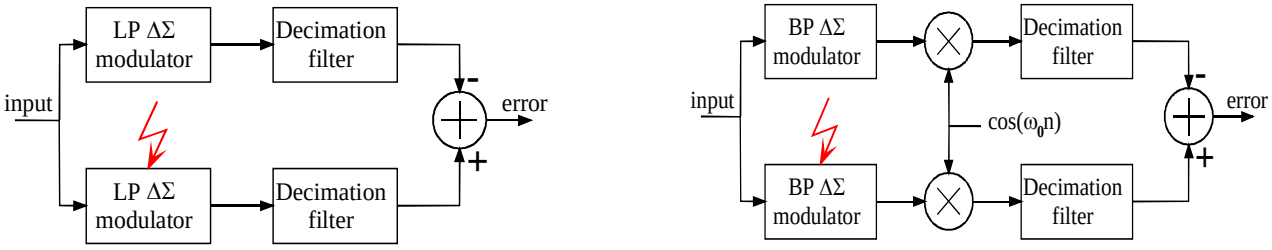


Figure 8: Testing the Delta-Sigma ADCs for single-event effects

SEE Affecting the Internal ADC

Figure 9 shows two decimated error transients from single-bit Delta-Sigma modulators. If the output of the single-bit ADC is upset, affecting the output of the feedback DAC as well, the error at the output of the decimation filter is only ±1 LSB (low-pass case) or up to ±5 LSB (band-pass case). The conclusion is that the internal ADC has no major influence on the decimated output, the error being slightly larger in the case of a band-pass modulator. We have also observed that the amplitude of the transients is independent of the oversampling ratio and/or order of the modulator. However, if the SEUs of the comparator occur when the input signal of the modulator is large, the modulator may become unstable.

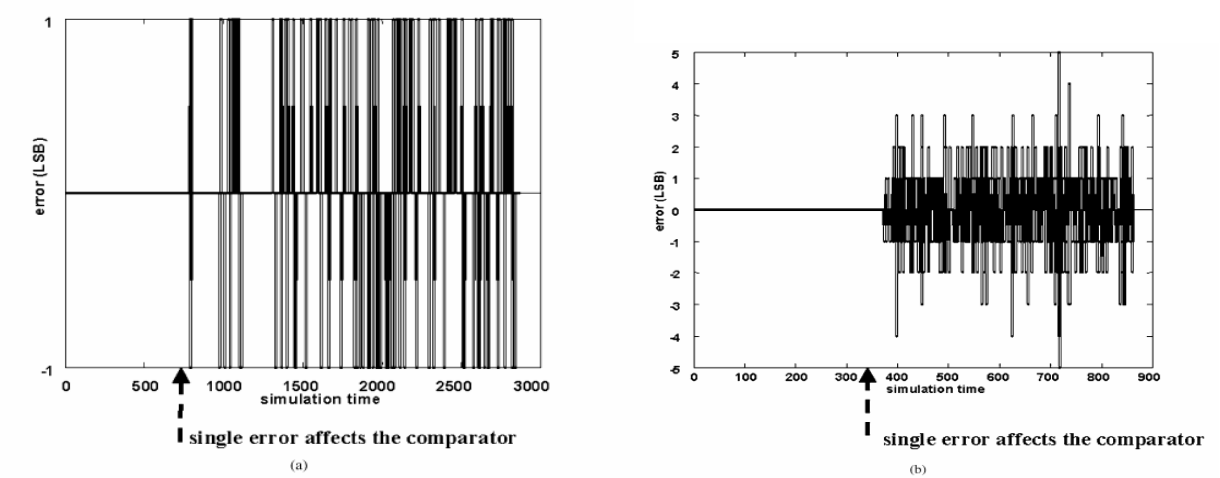


Figure 9: Decimated output error induced by the SEU of the comparator:
(a) low-pass case and (b) band-pass case.

SEE Affecting the Integrator–DAC Structure

If radiation single events occur at the integrator or feedback DAC level, the error at the decimated output is much larger and it can affect several output digital codes. Simulations have been carried out for:

- different values of v_{se} (normalized to the output voltage swing of the integrating stages);
- different orders of the modulators;
- different oversampling ratios;
- SEE affecting different integrating stages;
- different topologies of Delta–Sigma modulators;
- different input signal levels.
- different quantization levels.

In Figure 10(a) the effect of the hit location within the loop filter is depicted. The case of a single-bit feedback topology of order 4 and OSR = 64 is shown. As expected, the first integrating stage is the most critical one, whereas SEEs in subsequent stages are generating lower amplitude errors at the decimated output. In the following two plots only the results showing the effects of single-event hits in the first integrating stage will be presented, with these hits inducing to the largest errors. In Figure 9(b) the maximum values of the error at the decimated output are plotted, for different orders and oversampling ratios of the single-bit modulator. The results obtained for the feedback topology are presented, with similar results being valid for the feed-forward topology. The chosen system parameters (order and OSR) achieve the same final resolution N=14 bits. This plot shows that lower order and higher oversampling ratio offer better SEE immunity. In Figure 9(c), a comparison between the feedback and feed-forward topologies for single-bit modulator is presented. One can see that the feed-forward topology is less sensitive to the SEE affecting the integrating stages. This can be explained by the fact that, for the same OSR, the gain of the first integrating stage of the feed-forward topology is larger than the one in the

feedback topology. Therefore, the amplitude of the single-effect transient at the output of the first integrator is reduced more when reflected back at the global input of the modulator. These results allow us to determine the maximal error v_{se} affecting each integrating stage of a Delta–Sigma modulator, an error that does not decrease the overall resolution of the ADC below an imposed threshold. The maximal values of v_{se} sets the minimum value of the capacitors used in the integrating stages, and therefore the power consumption of the modulator.

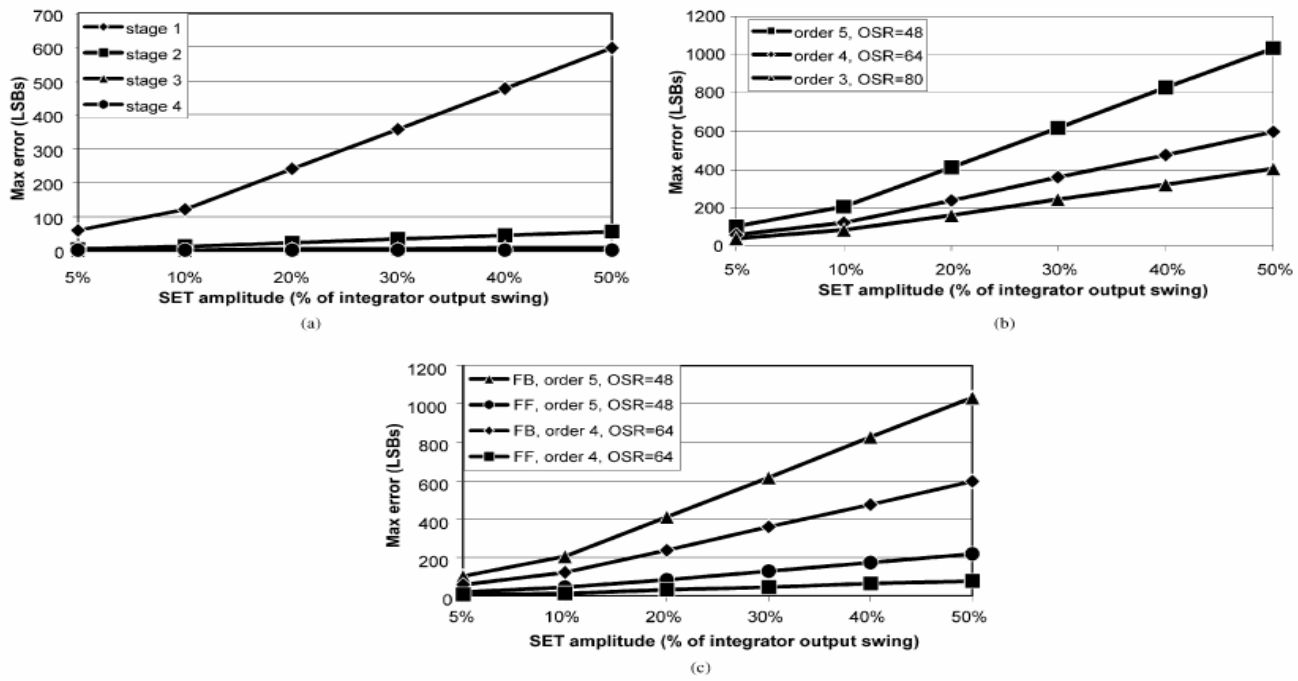


Figure10: Maximum error induced by SEE: (a) different hit locations; (b) different system parameters, same resolution; and (c) feedback versus feed-forward topologies.

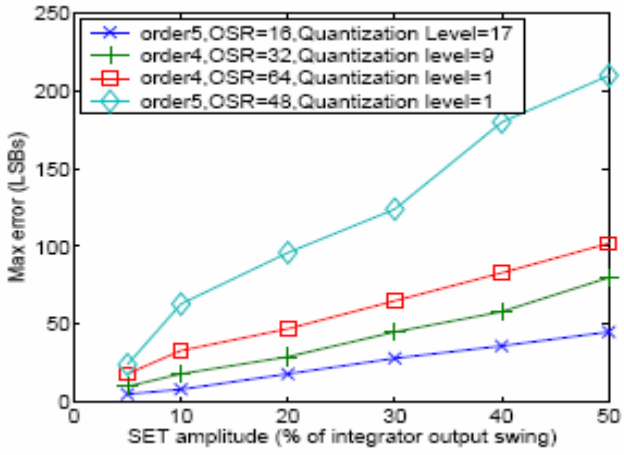


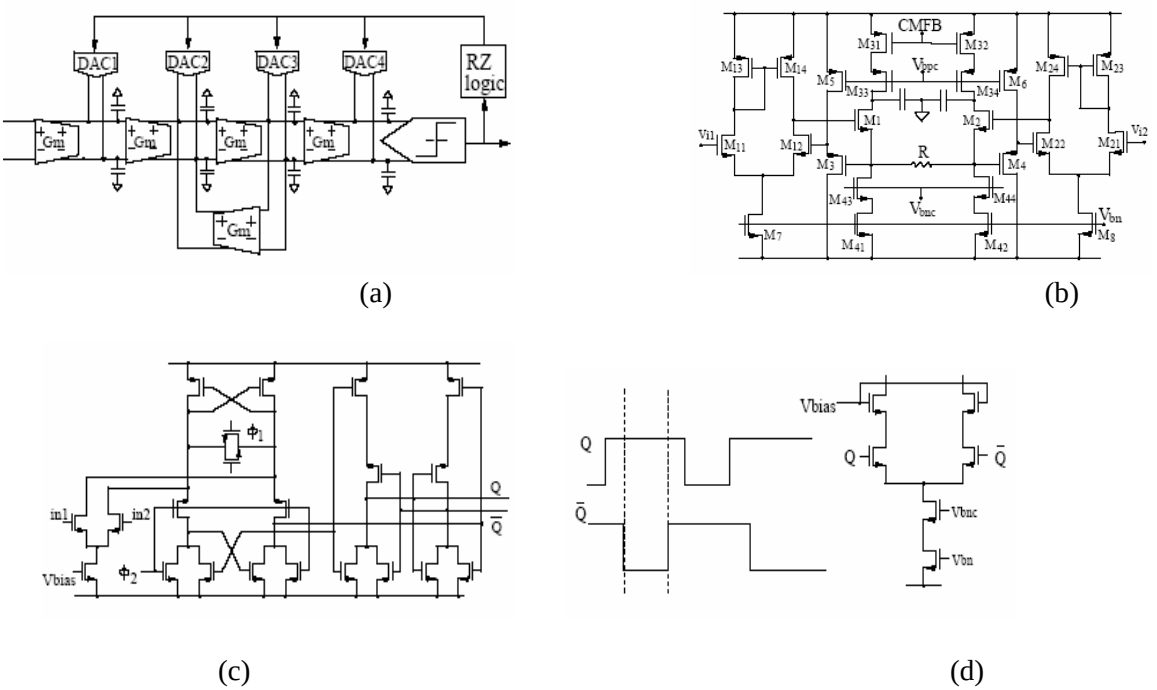
Figure 11: Maximum errors induced by SEE for different orders, different OSRs and different quantization levels

In Figure11, the maximum values of the error at the decimated output are plotted versus the voltage error *Vse* generated by SEE, for different orders, different oversampling ratios and different quantization levels of the quantizer. We can see here, to mitigate the SEE on the decimated output, instead of increasing the *OSR*, increasing the quantization levels of the internal A/D converter is more effective.

Test chips

A prototype chip has been fabricated in Honeywell's MOI5 0.35μm partially depleted SOI CMOS process. The layout of the designed prototype is shown in Figure14, where each cell or sub-system has been clearly identified:

1. Fourth-order, single-bit, continuous-time low-pass ΔΣ modulator. The modulator has been designed to achieve a signal-to-noise ratio of approximately 60dB (10-bits) in a bandwidth of 500kHz (1Msamples/sec), operating with an oversampling ratio of 32 (f_s=32MHz). For the first prototype, one didn't target a high-performance implementation, but only a vehicle to verify experimentally our behavioral simulations regarding the effects of single event hits. The four integrating stages (G_m-C approach) are placed from left to right as shown by Figure12 (a), the input stage having the largest integrating capacitors (2x40pF). The value of the capacitors in the first integrating stage has been evaluated both from noise requirements and from SEE immunity points of view. Based on our previous SEE simulations for the transconductor topology used in this modulator, a SEE hit generating at most 1pC of charge in any of the transistors in the employed OTA [6] does not produce an output voltage transient larger than 25mV, which is less than 10% of the maximum output voltage swing for integrating stages. This error guarantees that in the worst case the accuracy of the overall ΔΣ ADC (after decimation) does not decrease at any time below 7 bits [8]. Such a maximal error can occur only when one of the most critical devices in the transconductor is hit and the charge generated within is 1pC, lasting for only one output digital code. To monitor the correct operation of the modulator, the outputs of all integrating stages have been buffered before being connected to output pads. The building blocks of the modulator are shown in Figure12 (b)-(d).



(a) (b)

(c) (d)

Figure 12: (a) diagram of the prototype modulator (b) integrators[9] (c) high-speed comparator (d)feedback DAC with return-to-zero waveform

2. Operational Transconductance Amplifier, topology shown by Figure12 (b).
3. Output buffer. A separate buffer, identical to all the others used for the main analog cells on the chip, has been included.
4. Capacitive array for testing G_m-C integrators based on different transconductor topologies. Two 40pF capacitive arrays are provided and they can be connected to the outputs of each of the five operational transconductance amplifiers through CMOS switches controlled by an external digital code. This solution was chosen because one didn't have enough area to provide each OTA with its own integrating capacitors.
5. Operational Transconductance Amplifier, topology in [10].
6. Operational Transconductance Amplifier, topology shown in Figure13 (a).
7. Operational Transconductance Amplifier, topology in [11].
8. Operational Transconductance Amplifier, topology shown in Figure13 (b).
9. Comparator. The same comparator that is used in the realization the fourth-order, single-bit, continuous-time low-pass ΔΣ modulator has been separately implemented on chip.
10. Array of wide-bandwidth, high linearity buffers connected to the outputs of operational transconductance amplifiers.

The fabricated continuous-time modulator achieves 63dB dynamic range (resolution >10bits), 63.73-dB SNR, and 59.84-dB SNDR over 500KHz signal bandwidth with an oversampling ratio of 32, while dissipating 12mW from a 3.3-V supply.

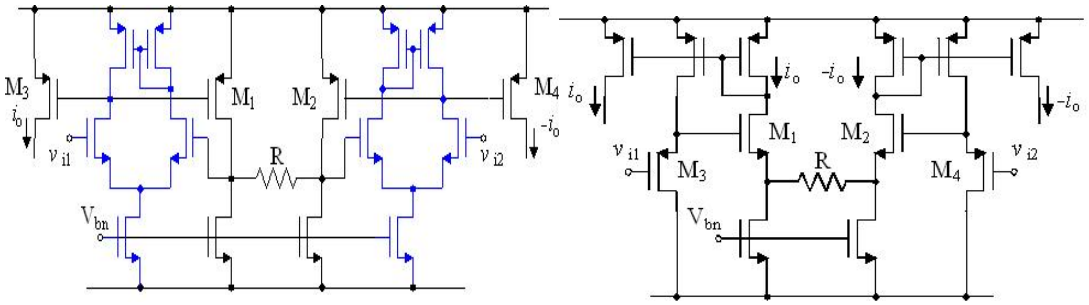


Figure 13: Two OTAs in the test chip

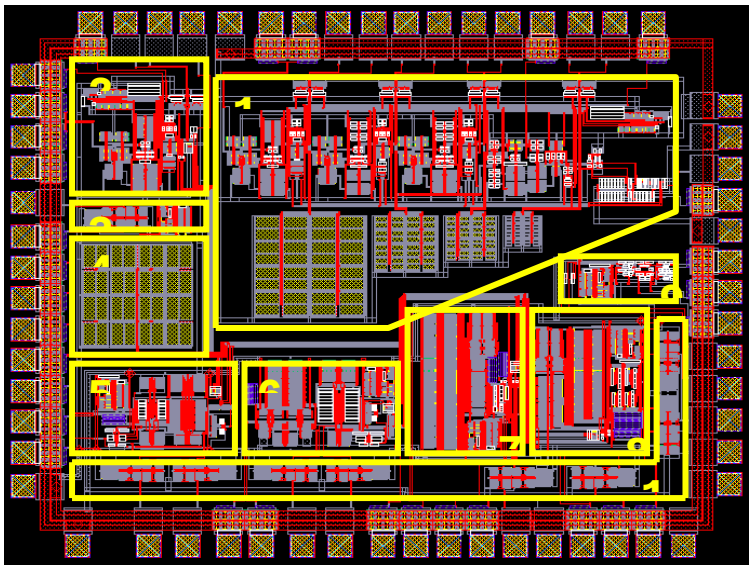


Figure 14: Layout of the test chip

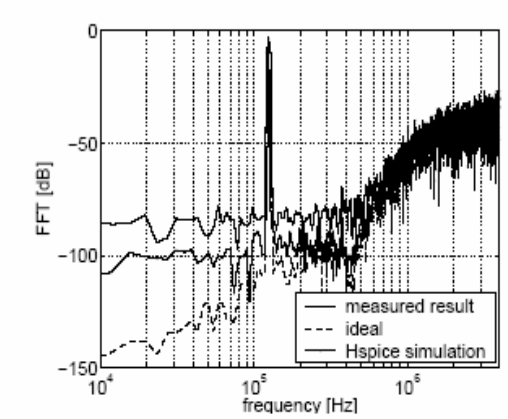


Figure 15: Simulated and measured spectra of the modulator

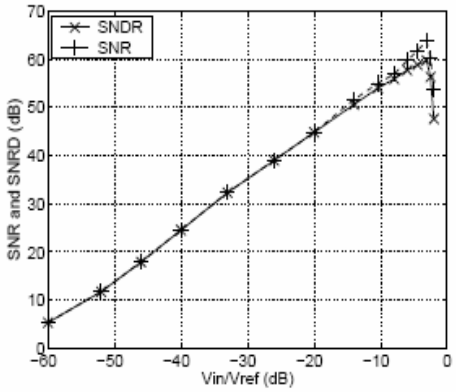


Figure 16: Measured SNR and SNDR vs. input level

Figure 15 shows the spectrum of the output signal in the case of a single-tone test (f_{in}=*125KH,z* v_{in}=*-3dBFS*). Figure 16 shows the resulting SNR and SNDR versus the normalized input signal, for a single-tone test using a 125-KHz input frequency. Up to *-3 dBFS* input, the quantization noise energy is dominant over the level of the harmonics. For larger input amplitudes, the internal ADC goes into overload and distortions increase. From Figure 16, the input amplitude for which SNR=0dB can be extrapolated to -66dB.

The radiation test for the prototype modulator was performed by using the Tandem Van de Graff accelerator in Brookhaven National Lab. To find the SEEs, only constant DC inputs are fed to the modulator. The digital output data stream of the modulator was captured using a HP 1660A logic analyzer and the post-processing was performed using MATLAB. The decimation filter mentioned above is used to filter the modulator outputs. In case of no SEEs happening, a constant DC voltage should be found at the output of the decimation filter. Three kinds of ions are selected to hit our circuit. They are F (with LET 3.38 Mev.cm^2/mg), Cl (with LET 11.73 Mev.cm^2/mg), and Br (with LET 37.46 Mev.cm^2/mg). We tried 3 different constant DC input values for our modulator, 0v, 0.4v and –0.4v. For each ion and each constant DC input, 6 groups of data are captured and processed to check SEEs. The experiment data are shown on Table 1. The mark ‘X’ on the table cells of column ‘Error found’ corresponds to the groups of data from which we observed error. Figure 17 shows an example of the error.

Table 1: Radiation test for the modulator

Input DC(v)	Ion	Sample#	Energy (MeV)	LET(si) Mev.cm^2 /mg	Flux #/cm^2/sec	Fluence #/cm^2	Dose RAD(si)	TotalDose RAD(si)	CrossSec cm^2	Error found
0.4	F	D2801f	140	3.38	1.402E+5	1.045E+6	5.559E+1	2.202E+2	2.679E-3	
0.4	F	D2802f			5.798E+4	1.015E+6	5.520E+1	3.305E+2	2.760E-3	
0.4	F	D2803f			1.455E+5	1.022E+6	5.606E+1	3.866E+2	2.743E-3	
0.4	F	D2804f			2.143E+5	1.035E+6	5.626E+1	4.428E+2	2.710E-3	
0.4	F	D2805f			1.953E+5	1.054E+6	5.606E+1	4.989E+2	2.661E-3	
0.4	F	D2806f			1.960E+5	1.030E+6	5.559E+1	5.549E+2	2.726E-3	
0	F	D3201f			2.173E+5	1.046E+6	5.689E+1	9.474E+2	3.060E-3	
0	F	D3202f			2.169E+5	1.043E+6	5.671E+1	1.004E+3	3.070E-3	
0	F	D3203f			1.917E+5	1.040E+6	5.654E+1	1.061E+3	3.081E-3	
0	F	D3204f			1.927E+5	1.035E+6	5.631E+1	1.117E+3	3.094E-3	
0	F	D3205f			2.079E+5	1.040E+6	5.657E+1	1.174E+3	3.081E-3	
0	F	D3206f			2.166E+5	1.037E+6	5.639E+1	1.230E+3	3.092E-3	
-0.4	F	D3601f			1.309E+5	1.018E+6	5.597E+1	6.108E+2	3.538E-3	
-0.4	F	D3602f			4.777E+4	1.051E+6	5.471E+1	6.655E+2	3.426E-3	
-0.4	F	D3603f			2.106E+5	9.998E+5	5.597E+1	7.215E+2	3.604E-3	
-0.4	F	D3604f			2.083E+5	1.044E+6	5.679E+1	7.783E+2	3.451E-3	
-0.4	F	D3605f			1.769E+5	1.030E+6	5.603E+1	8.343E+2	3.499E-3	
-0.4	F	D3606f			2.080E+5	1.033E+6	5.618E+1	8.905E+2	3.491E-3	
0.4	Cl	D2801cl	199	11.73	5.139E+5	1.010E+7	1.906E+3	2.977E+4	2.773E-3	
0.4	Cl	D2802cl			4.649E+5	1.010E+7	1.907E+3	3.168E+4	2.774E-3	
0.4	Cl	D2803cl			5.132E+5	1.007E+7	1.901E+3	3.358E+4	2.783E-3	
0.4	Cl	D2804cl			5.054E+5	1.008E+7	1.903E+3	3.548E+4	2.781E-3	
0.4	Cl	D2805cl			4.715E+5	1.010E+7	1.906E+3	3.739E+4	2.777E-3	
0.4	Cl	D2806cl			4.174E+5	1.007E+7	1.900E+3	3.929E+4	2.787E-3	
0	Cl	D3201cl			5.589E+5	9.698E+6	1.905E+3	3.135E+3	3.301E-3	
0	Cl	D3202cl			5.142E+5	1.009E+7	1.904E+3	5.039E+3	3.173E-3	
0	Cl	D3203cl			4.944E+5	1.007E+7	1.901E+3	6.940E+3	3.179E-3	
0	Cl	D3204cl			3.545E+5	1.005E+7	1.896E+3	8.836E+3	3.189E-3	
0	Cl	D3205cl			5.214E+5	1.008E+7	1.902E+3	1.074E+4	3.179E-3	
0	Cl	D3206cl			5.133E+5	5.223E+6	1.904E+3	8.839E+3	3.147E-3	
-0.4	Cl	D3601cl			5.136E+5	1.007E+7	1.901E+3	1.645E+4	3.576E-3	
-0.4	Cl	D3602cl			4.703E+5	1.011E+7	1.907E+3	2.026E+4	3.564E-3	
-0.4	Cl	D3603cl			4.829E+5	1.006E+7	1.899E+3	2.216E+4	3.581E-3	
-0.4	Cl	D3604cl			5.109E+5	1.008E+7	1.902E+3	2.406E+4	3.575E-3	
-0.4	Cl	D3605cl			5.210E+5	1.008E+7	1.902E+3	2.596E+4	3.577E-3	
-0.4	Cl	D3606cl			5.012E+5	1.007E+7	1.900E+3	2.786E+4	3.582E-3	
0.4	Br	D2801br	278.5	37.46	3.858E+5	5.326E+6	3.054E+3	4.234E+4	5.259E-2	
0.4	Br	D2802br			3.806E+5	5.087E+6	3.066E+3	4.541E+4	5.508E-2	
0.4	Br	D2803br			3.507E+5	5.069E+6	3.055E+3	4.846E+4	5.530E-3	
0.4	Br	D2804br			3.187E+5	5.035E+6	3.035E+3	5.150E+4	5.569E-2	
0.4	Br	D2805br			3.626E+5	5.071E+6	3.056E+3	5.455E+4	5.532E-2	
0.4	Br	D2806br			3.742E+5	5.072E+6	3.057E+3	5.761E+4	5.532E-2	
0	Br	D3201br			3.637E+5	5.062E+6	3.051E+3	6.066E+4	6.323E-2	X
0	Br	D3202br			3.617E+5	5.079E+6	3.061E+3	6.372E+4	6.305E-2	X
0	Br	D3203br			3.569E+5	5.048E+6	3.043E+3	6.676E+4	6.345E-2	X
0	Br	D3204br			095E+5	5.073E+6	3.058E+3	6.982E+4	6.316E-2	X
0	Br	D3205br			1.827E+5	5.036E+6	3.035E+3	7.286E+4	6.365E-2	X
0	Br	D3206br			2.270E+5	5.072E+6	3.038E+3	7.589E+4	6.321E-2	
-0.4	Br	D3601br			1.503E+5	5.023E+6	3.028E+3	7.892E+4	7.168E-2	
-0.4	Br	D3602br			2.141E+5	4.333E+6	2.763E+3	8.168E+4	8.321E-3	
-0.4	Br	D3603br			6.046E+5	5.307E+6	3.084E+3	8.477E+4	6.789E-2	
-0.4	Br	D3604br			4.491E+5	5.090E+6	3.067E+3	8.784E+4	7.081E-2	
-0.4	Br	D3605br			2.766E+5	5.033E+6	3.033E+3	9.087E+4	7.163E-2	
-0.4	Br	D3606br			2.120E+5	5.034E+6	3.034E+3	9.390E+4	7.163E-2	

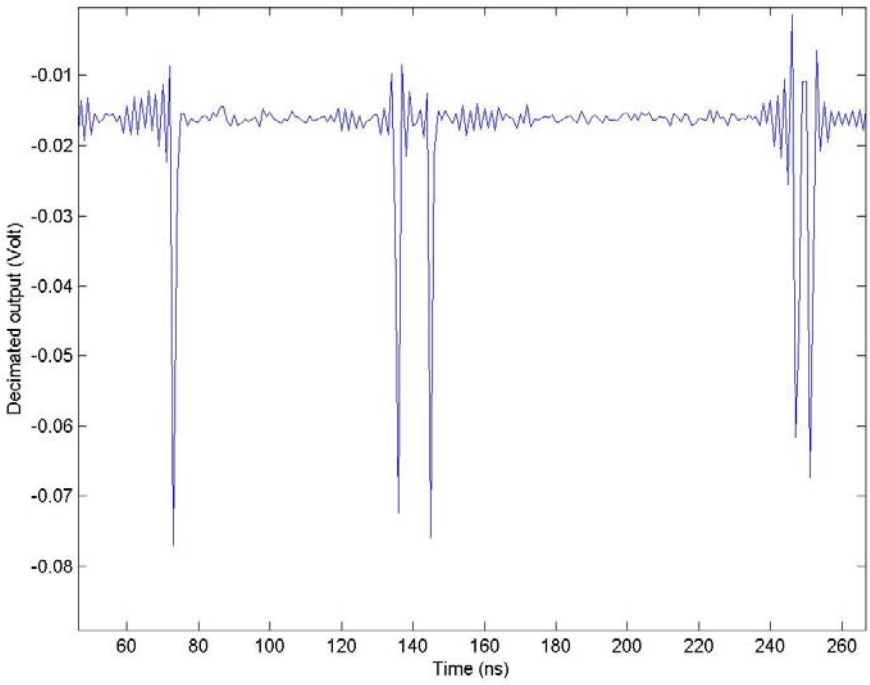


Figure 17: Error observed with ion Br and constant DC input 0volt

Other Results

Technology Transfer/Intellectual Property

The work resulting from this project will support Honeywell in providing mixed-signal ASIC support for space-based electronics. Honeywell is working to develop mixed-signal ASIC capability for 0.35 μm SOI CMOS targeted to radiation-hardened space systems. This includes developing custom analog/mixed-signal cells and sub-components. With incremental additional development, the sigma-delta modulators and/or sub-cells developed by this project may be included with other such cells as library elements for insertion into mixed-signal ASICs. Applications for low-power, moderate resolution, and high bandwidth sigma-delta ADC's may include signal processing for focal-plane arrays, signal processing for distributed control systems, and signal processing for satellite wireless communications.

Publications Resulting from Research

1. B. Zhao, A. Leuciuc - "Single Event Transients Characterization in SOI CMOS Comparators", accepted for presentation at the IEEE Nuclear and Space Radiation Effects Conference NSREC'04, Atlanta, July 19-23, 2004.
2. A. Leuciuc, B. Zhao, Y. Tian, J. Sun - "Analysis of Single Event Effects in Delta-Sigma Modulators", accepted for presentation at the IEEE Nuclear and Space Radiation Effects Conference NSREC'04, Atlanta, July 19-23, 2004.
3. J. Sun, Yi Zhang, A. Leuciuc " A 11-bit 4th-order continuous-time Delta-Sigma Modulator on 0.35um SOI technology", submitted to MWSCAS symposium in 2005

Benefits to Commercial Sector

The commercial sector will have access to the library of analog cells we are developing in SOI CMOS (OTAs, one-bit DACs, comparators). At the same time, we will provide a comparison between the parameters of similar analog cells implemented in bulk CMOS and SOI CMOS.

References

[1] S.R. Norsworthy, R. Schreier, and G.C. Temes (eds.), "Delta-Sigma Data Converters: Theory, Design, and Simulation", New York: *IEEE Press*, 1997.

[2] O. Shoaei, "Continuous-Time Delta-Sigma A/D Converters for High-Speed Applications", Ph.D. dissertation, Carleton Univ., Ottawa, Canada, 1996.

[3] L.J. Breems and J.H. Huijsing, "Continuous-time Sigma-Delta modulation for A/D Conversion in Radio Receivers", Kluwer Academic Publishers, Boston, 2001.

[4] K. Bernstein and N. J. Rohrer, "SOI – Circuit Design and Concepts", Kluwer Academic Publishers, 2000.

[5] A. Marshall and S. Natarajan, "SOI Design: Analog, Memory and Digital Techniques", Kluwer Academic Publishers, 2001.

[6] S.E. Kerns et al., "Model for CMOS/SOI Single-Event Vulnerability," IEEE Trans. Nuclear Science, vol. 36, no. 6, Dec. 1989.

[7] L. W. Massengill et al., "Single-Event Charge Enhancement in SOI Devices," IEEE Electron Dev. Let., vol. 11, no.2, Feb. 1990.

[8] A. Leuciuc, B. Zhao, Y. Tian, J. Sun - "Analysis of Single Event Effects in Delta-Sigma Modulators", accepted for presentation at the IEEE Nuclear and Space Radiation Effects Conference NSREC'04, Atlanta, July 19-23, 2004.

[9] Z. Y. Chang, D.Haspeslagh, and J. Verfaillie, "A High Linear CMOS Gm-C Bandpass Filter with On-Chip Frequency Tuning,"*IEEE J. Solid-State Circuits*, vol. 32, pp. 388–397, Mar.1997.

[10] S.D. Willingham, K. W. Martin, and A. Ganesan, "A BiCMOS low-distortion 8-MHz low-pass filter", *IEEE J. Solid-State Circuits*, vol. SC-28, no. 12, pp. 1234-1245, Dec. 1993.

[11] A. Worapishet and C. Naphaphan, "Current-feedback source-degenerated CMOS transconductor with very high linearity", Electronics Letters, vol. 39, no. 1, Jan. 2003, pp. 17-18.

[12] K.G. Merkel II and A. L. Wilson, "A Survey of High Performance Analog-to-Digital Converters for Defense Space Applications", 2003.

PROJECT 9

RF, ANALOG AND DIGITAL ARRAY FOR RADIATION-HARDENED COMMUNICATION CIRCUITS

Larry McMurchie and Carl Sechen (University of Washington)
with Andy Peczalski (Honeywell)

RESEARCH TIME PERIOD: Three years
RESEARCH FOCUS: AFRL Task Areas 1, 2, and 3: System Circuit Modeling for VLSI Circuit Implementation, Standard Cell/Topologies in Radiation-Hardened SOI, and Reconfigurable Mixed-Signal Electronics

Figures and Tables

Abstract

The first goal of this project has been to investigate remediation techniques for Single Event Effects (SEEs) in digital circuits. While the effects of radiation on RAM cells has been thoroughly studied and numerous remediation techniques proposed, Single Event Transients (SETs) have not been widely studied. Few remediation techniques other than TMR-in-hardware have been proposed. We believe that a variety of techniques, particularly TMR-in-time, register filtering, and dual-mode redundancy (DMR), can achieve the same radiation hardness as TMR-in-hardware, without incurring a 3X area/throughput/power hit.

As a demonstration vehicle, we chose a coarse-grained reconfigurable analog/digital architecture. We believe that such a reconfigurable architecture has a large power/speed/area/functionality advantage over existing fine-grained commercial FPGAs. In terms of radiation hardness, the reconfigurability of the architecture allows an additional potential benefit: the degree of radiation hardness can be a programmable feature.

Project Description

The demonstration vehicle for our work is a Reconfigurable Analog/Digital Array for Radiation-hardened signal processing circuits (RADAR). RADAR is a linear array of programmable functional units connected by a programmable segmented-bus routing structure. Examples of (digital) functional units that might be included in RADAR are registers, SRAMs, ALUs, and multipliers, as well as ADCs and DACs.

In RADAR the various blocks communicate via the programmable, segmented-bus structure. In contrast to a fine-grained, bit-level FPGA such as a Xilinx Virtex part, the coarse-grained RADAR array achieves very high performance for computationally intensive applications. A bit-level FPGA has high configurability, but the logic and routing overhead for this configurability can sacrifice a factor of 10 or more in speed, throughput, and area. With the routing architecture defined in terms of buses of signals, RADAR routing resources are simplified and thus the number of programming bits is greatly reduced.

We have developed several techniques for radiation-hardening the components of RADAR. Below we summarize the results we have obtained for SEU hardness of combinational logic and SRAMs as well

as total dose hardness.. Note that these techniques are generally applicable to most digital CMOS logic circuits in addition to RADAR.

SEU Hardness in Combinational Logic

The first approach we investigated was a temporal approach to filtering radiation-induced transients in combinational logic at register boundaries. This work utilizes three registers employing delay-separated clocks. The advantage of this scheme over a straightforward TMR-in-hardware approach is that by adjusting the separations of the clocks, transients of varying duration can be filtered. Therefore, by making the clock separations programmable, the degree of radiation hardness can be programmed. Another advantage of the temporal approach is lower power. In the absence of any radiation-induced transients, all the data switching occurs on only one copy of the logic and only at the beginning of the clock cycle. In contrast, a TMR-in-hardware approach results in switching on three copies of the hardware.

We have also developed a completely new approach -- double-mode redundancy (DMR) in time -- mitigate single-event effects in combinational logic in pipelined systems. SETs of the order of the clock period are eliminated in this approach, yielding quite a high LET threshold. The cost is only a 2X reduction in the theoretical maximum throughput and a minimal increase in power.

SEU Hardness in RAMs

The standard approach to SEU-hardness in SRAM design is to employ error-correcting codes (ECC). Unfortunately, the ECC approach offers no SEU protection for peripheral circuitry such as row and column decoders. We have developed a very low overhead scheme for hardening the decoders that requires no extra area and does not degrade read/write times. We have also found a simple solution to hardening the ECC circuitry that adds only a single gate delay. The self-scrubbing process adds only a small amount of area, virtually no additional power (the scrubbing circuitry is normally quiescent), and only a single gate delay to the read and write times.

We have explored the merits of utilizing some concepts from DRAM technology to save considerable area/bit and to increase radiation hardness in comparison to the standard 6T SRAM. Our new memory cell design utilizes only 2 transistors (an nMOS as a pass transistor switch and a pMOS device as an enhancement mode capacitor) and a conventional ASIC fabrication technology (e.g. TSMC).

Total Dose Hardness

We have developed a cell layout generator that constructs total-dose-hardened standard cells (in bulk CMOS) using annular devices and guard rings. The generator is parametrized so that cells with a range of drive strengths may be generated. When coupled with an efficient sizer (another project within our group) and commercially available place and route software, the generator can produce circuits optimized for a particular power/delay goal.

Applications

In a white paper submitted to AFRL entitled “Mixed Mode, Radiation Hard ASICs for Reconfigurable I/O,” Dr. Andrzej Peczalski describes a reconfigurable I/O subsystem that incorporates the necessary functions to perform conditioning and conversion of analog and discrete signals for a wide range of applications. This subsystem will be formed of blocks currently under development by 4 University groups: ADC (Adrian Leuciuc, SUNY), DAC (GaborTemes, OSU), programmable PLL (Un-Ku Moon and Karti Mayaram, OSU), and Reconfigurable DSP (Larry McMurchie and Carl Sechen). The benefits of this subsystem are several. Its reconfigurable nature allows reuse in numerous aerospace systems, reducing development and integration time as well as cost. Reconfigurability also allows in-orbit remote repair and upgrade as well as dynamic reconfigurablity for mode and task agility.
A version of the RADAR system has been designed to perform FIR and correlation functions for this reconfigurable I/O subsystem. This chip design will be fabricated during the summer of 2005. Testing of the chip and integration into the reconfigurable I/O subsystem will be completed during fall of 2005.

Research Results and Discussion

Radiation-Hardened Self-Scrubbing SRAM

There has been considerable work with the goal of making SRAMs radiation tolerant. Many efforts have focused upon cell design with the goal of making cells immune to upset. EDAC techniques have also been developed and are widely used. Despite the success of such techniques at eliminating errors on the outputs, these techniques by themselves do not scrub the SRAM of accumulated errors. As a result, errors can build up over time in the array, potentially creating multiple errors in a single word that cannot be corrected. The most common approach to scrubbing is to periodically take the SRAM offline and read/correct/write each memory location. This approach, however, may be unacceptable in a variety of situations. One is a mission-critical component where such downtime may not be acceptable. Another situation is the case of a dedicated block of SRAM that is used in a pipelined, high-throughput datapath. The datapath throughput and SRAM access frequency may be such that the SRAM block has no idle cycles to allow correction. What is needed here is a minimal overhead hardware solution that allows the SRAM to continue normal operation while error scrubbing occurs.

In general, standard EDAC schemes do nothing to correct radiation–induced transient errors in the detection and correcting circuitry itself. Row and column decoders and other peripheral circuitry are also vulnerable to transient errors. Such transient errors in combinational logic have been largely neglected up to the present because feature sizes have been large enough to allow gates to overpower any radiation-induced transients. With smaller feature sizes and dynamic circuitry, transients will propagate and become a serious source of error. One researcher [Baumann 2002] has suggested that such transient errors in peripheral logic will soon become the dominant source of error in SRAMs. We have looked at a variety of radiation-hardening-by-design techniques for such peripheral logic.

Our first generation self-scrubbing SRAM consisted of two banks that can work independently. You can read or write one bank of the memory while the other bank is being corrected. No downtime is required while making the correction. Hamming codes are used to detect and correct the single bit error. Scrubbing prevents errors from building up over time and causing data corruption that cannot be corrected or detected. This first generation SRAM (Figure 1) has been implemented and verified at the layout level. The worst-case read and write times of this version are 1500ps and 480ps respectively (in 0.18 micron CMOS). The size of the 512bit SRAM is 182um by 185 um. The disadvantage of this SRAM design is that some parts in the memory, particularly the decoder and other peripheral circuitry are vulnerable to radiation-induced transients.

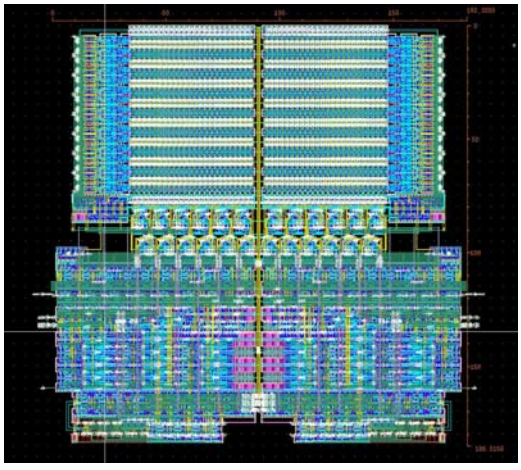


Figure 1. Dual-bank self-scrubbing SRAM

In a subsequent quad-bank SRAM design all peripheral circuitry is hardened including state machine, control unit, row decoders, correction and Hamming encode/decoder. The second improvement is that the SRAM contains four banks of memory compared to two banks in the old generation. Only one bank of the SRAM will be accessed or written under normal operation. However, the decoders in all banks will be active, providing triple mode redundancy to maintain the correctness of the word lines in the event any one decoder is hit. In the event a scrub is required of a single bank, that bank will be taken offline.

The design of the dual- and quad-bank architectures led us to several observations. Hardening of the word line drivers through sizing degrades speed, increases area, and can result in increased vulnerability of word lines to upset or partial upset for larger LET values. Also, these architectures may be vulnerable to multiple-bit upsets if cells containing bits in the same word are close to each other. These observations led us to develop a new architecture – the 1bit/bank architecture. If the word size including EDAC bits is w, then we utilize w banks of memory, the i'th bank storing the i'th bits for every word. Each bank has its own decoder. This architecture allows any errors in the decoders or word lines to be corrected by the EDAC structure. By separating the bits for each word into separate banks, multiple bit upsets in the same word are effectively eliminated. This 1 bit/bank approach is a natural organization in medium-to-large SRAMs where the use of multiple banks is advantageous to minimize R/C on both word and bit lines.

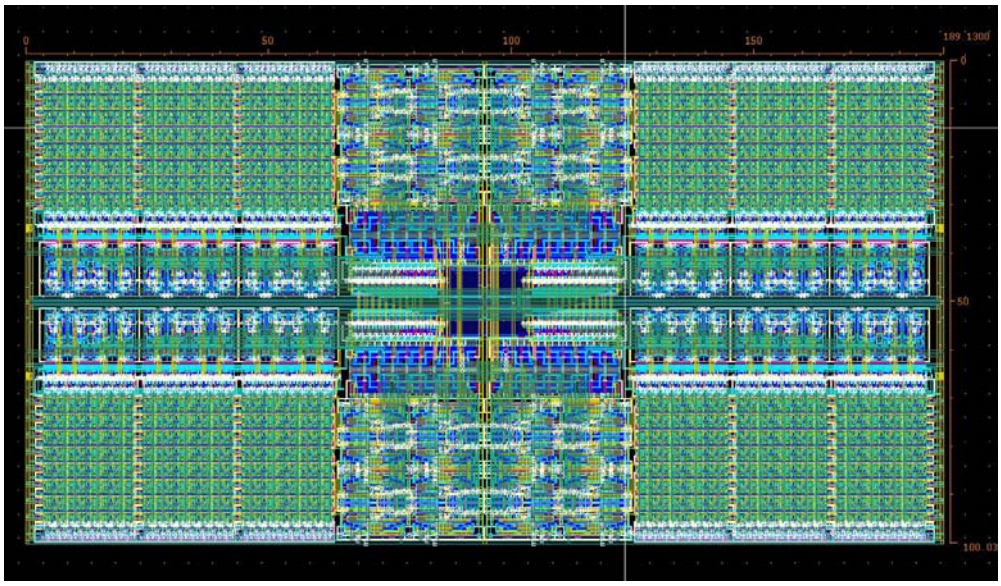


Figure 2. Quad-bank self-scrubbing SRAM

In order to perform scrubbing in the 1 bit/bank architecture, we added a "scrub decoder" that is given an address to be scrubbed. A 2:1 multiplexor is added on each row that selects between the voted decoder outputs and the scrub decoder output. Scrubbing (writing) is performed on a bank whenever there is a bit to be corrected in a bank and the normal operation is a read. Note that this will mean that the data word being read will have an error because the bank being scrubbed cannot be read. The EDAC circuitry corrects for the missing bit in the word currently being read, and the controller nullifies the scrub of this data word.

Figure 3 shows a layout in .13 micron CMOS for a 21-bank (16 for words + 5 for Hamming codes) memory containing 256Kbits. Read time from simulations of extracted layout is 2.5ns and write time is 1.0ns. The distinctive area near the center of the block comprises the controller and all EDAC circuitry. It is apparent that the area occupied by this circuitry is relatively small compared to the area occupied by the memory banks.

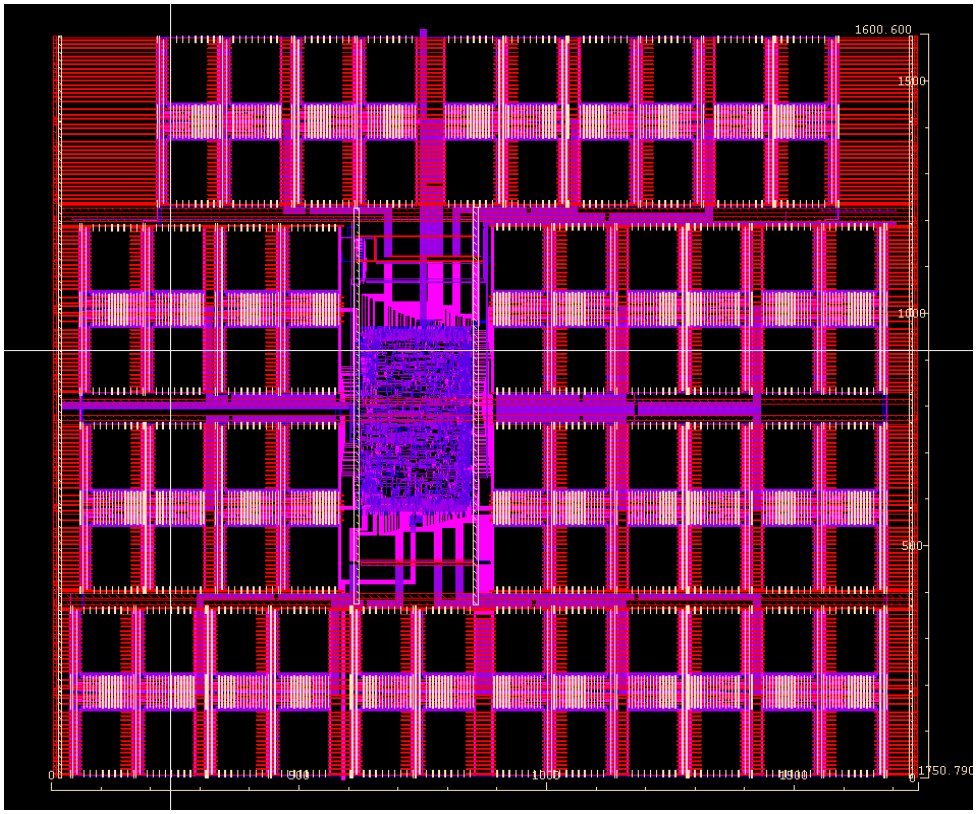


Figure 3. 1 bit/bank SRAM architecture (256Kbits)

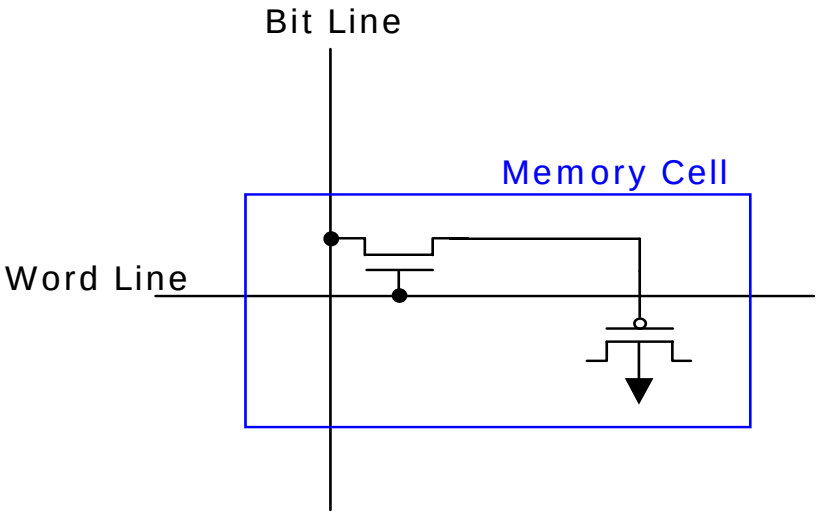


Figure 4. The 2T memory cell

Radiation-Hardened By Design DRAM – 2T Memory Cell

We have explored DRAM technology to save considerable area/bit and to increase radiation hardness in comparison to the standard 6T SRAM. Our memory cell design utilizes only 2 transistors (an nMOS as a pass transistor switch and a pMOS device as an enhancement mode capacitor) and a conventional ASIC CMOS fabrication technology (*e.g.* TSMC). The schematic diagram of the memory cell is shown in Figure 4.

The enhancement mode pMOS capacitor has almost no depletion-region area, greatly reducing the effective cross-section with respect to radiation sensitivity. The two terminals of the capacitor are the poly gate of the pMOS and its n-well. The drain and source are left to float. Our layout of this 2T memory cell is shown in Figure 5.

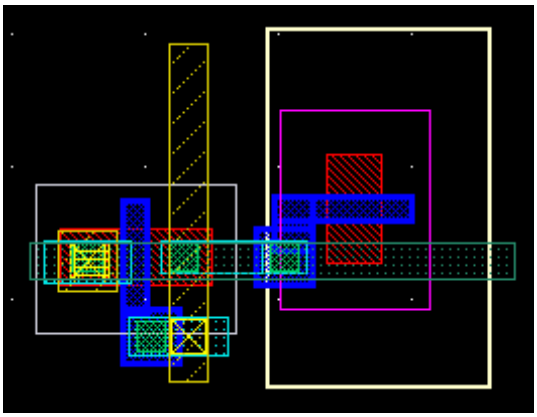


Figure 5. Layout of the 2T memory cell

This 2T RAM memory cell occupies an area of 2.65um^2 for the TSMC 0.18um process. In contrast, our best 6T SRAM memory cell has an area of 7.40 um^2. This means that our 2T RAM memory cell is 2.80 times smaller than the 6T memory cell, almost equal to the ratio of the number of transistors. Hence the effective radiation cross-section is 3X smaller per bit, simply on the basis of size. But, since the pMOS device is largely devoid of depletion regions, the effective radiation cross-section should be 6X less than a conventional 6T SRAM.

Besides the cell design, the major design difference between the 6T SRAM and the 2T RAM is the sense amplifier. During a read operation of a 2T RAM memory cell, the word line transitions HIGH, turning ON the nMOS and allowing charge on the bit line (pre-charged to Vdd/2) and in the memory cell to share. This causes a small voltage shift on the bit line but destroys the data in the memory cell. Therefore, the 2T RAM requires a sense amplifier design that can detect small voltage swings on a bit line and consequently drive the bit line to its corresponding full-rail voltage for write-back.

Because it must detect small voltage swings, the delay of the sense amplifier for an area-efficient SRAM is a significant portion of the total access time. The large capacitive, and also resistive, loads on the sense amplifier make it difficult to achieve sharp slew rates. Furthermore, due to the large number of sense amplifiers needed, the sense amplifier transistor sizes have to be small to reduce area overhead, thus reducing the drive. Simulations of the 1T1C design have shown that the access time is about 2ns (in .18 micron CMOS), about 0.5ns slower than that of the 6T SRAM design.

Using Register Filtering for Radiation-Hardening of pipelined systems

Until the past few years, much of the work in creating radiation-hardened circuitry has been focused upon storage elements. As feature sizes shrink, however, the reduced stored charge on logic gates becomes more susceptible to radiation-induced single event transients (SETs) in combinational logic. Increasing clock rate also plays a significant role in increasing the susceptibility of logic gates to SETs.

As shown by [Buchner 1997], the error rates in combinational logic are proportional to clock frequency, whereas error rates in sequential storage elements are independent of frequency.

Total dose hardening of combinational logic gates has been investigated by [Lacoe 2000], who used a combination of edgeless transistors and guard bands. Such total-dose-hardened logic gates may be larger by a factor of 2X while consuming up to 2X the power of non-hardened gates. These figures are, of course, very dependent upon circuit and process.

Mitigating SETs at the gate level can be performed by resistive and/or capacitive filtering, as well as upsizing devices. Such techniques can be effective at eliminating the possibility of transients, but often result in large increases in area, power and delay. [Baze 2000], for example, found a speed penalty of 5X, an area penalty of 3X, and a power penalty of 5X. These penalties, combined with those incurred by total-dose hardening, are unacceptable.

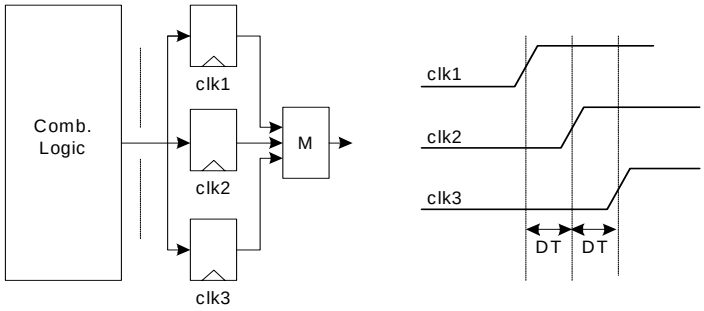


Figure 6. Concept of register filtering

Applying architectural solutions is a well-established alternative. Triplicating each combinational logic block as well as sequential storage elements yields a high degree of radiation-hardness with respect to SETs at the expense of a ~3X increase in power and area as well as an increase in delay due to the voting circuitry. TMR-in-hardware, as it is called, incurs an additional area /power penalty due to the layout techniques required for total dose hardening.

TMR-in-time is another alternative. This can be easily formulated as triplicating the computation on the singlet hardware by applying the same data on three successive clock cycles and applying majority functions. Penalties of ~3X in delay are incurred, as well as a penalty in power mostly due to the requirement of providing 3 clocks for every data computation. If the radiation-induced transient is short in duration relative to the clock cycle, a more efficient approach is suggested, wherein successive “minor” clocks are used to latch the outputs of the combinational logic, as shown in Figure 6. As long as the transient is shorter than the clock separation times, only one of the three registers will contain incorrect data and the majority function will filter it out, producing the correct result. Since the duration of the transient is dependent upon the LET of the incident energy, adjusting the clock separation provides a means of adjusting the radiation hardness of the circuit.

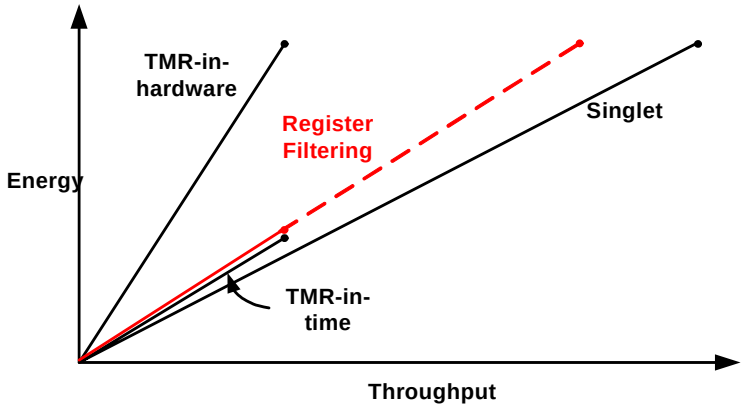


Figure 7. Schematic of Energy vs. throughput diagram for various radiation-hardening schemes as applied to a fixed size pipeline such as RADAR.

Figure 7 shows a comparison of various techniques for radiation hardness. The figure assumes a fixed size pipelined datapath such as RADAR. TMR-in-hardware exhibits 3X energy relative to the singlet and reaches a maximum throughput at 1/3 the throughput of the singlet. TMR-in-time approaches the singlet in terms of energy, but reaches a maximum throughput also at 1/3 the throughput of the singlet. Register filtering (dashed line), on the other hand, provides a variable throughput (and proportional power) based upon the length of transient (i.e. degree of radiation hardness) that must be accommodated. The intent is to make the degree of radiation hardness a programmable feature, just the same as the particular DSP operation. In this way the energy and throughput can be optimized for the radiation environment in which the RADAR implementation will be employed.

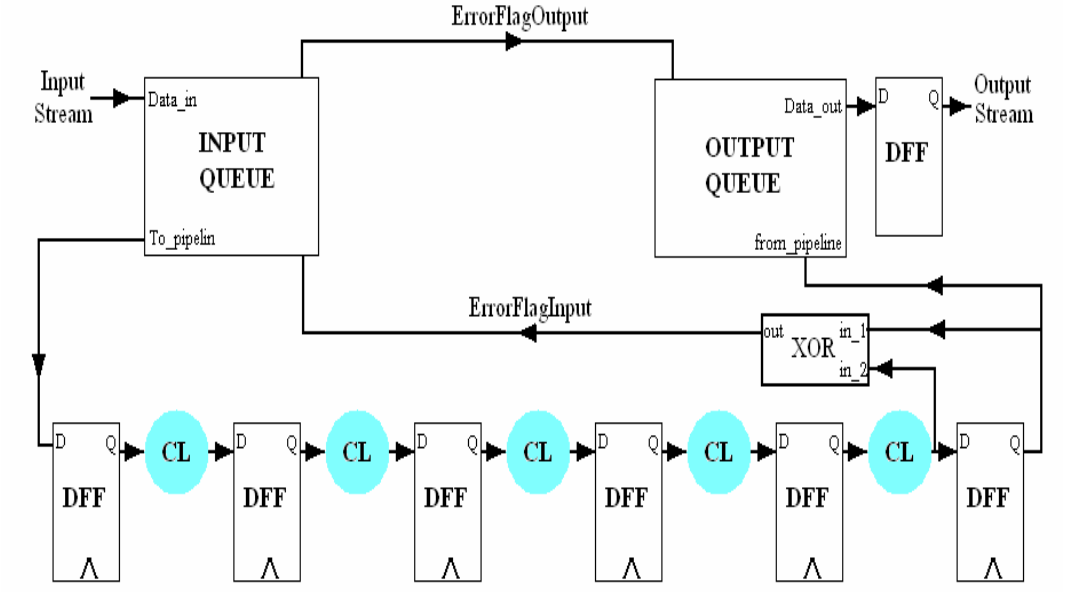


Figure 8. Example of simple DMR pipeline

Double-Mode Redundancy (DMR) in Time

We have developed a completely new approach, double-mode redundancy (DMR) in time, to mitigate single-event effects in combinational logic as well as in pipelined and sequential systems. Figure 8 shows a simplified representation of a DMR pipeline. In DMR-in-time, each input vector is issued twice in succession, requiring 2 clock cycles. Note that there is no additional power consumption for the second issuance of each vector since the static CMOS gates have already reacted to the first vector (assuming no error occurred and ignoring the additional clock power). At the end of the pipeline, an XOR gate is used on consecutive output vectors to check for an error due to a SEU.

If an error occurs, we need to re-run the last *N*/2 input vectors since there was an SEU in one of the *N* stages. This new technique uses primary input and primary output queues; the length of each queue is equal to *N/2*, the number of unique vectors present in the pipeline. The input queue retains the last *N*/2 input vectors that were issued, enabling the vectors to be rerun in event of an SEU. The output queue must contain N/2 entries in order to continue to supply output values to the output stream while vectors are being rerun (Note that *N*/2 input vectors fully populate the pipeline since each was issued twice).

If an SEU is detected by the XOR, we run the pipeline at full speed, the input queue re-issuing the (retained) last *N*/2 vectors, one per clock cycle. Meanwhile, the output queue continues to produce valid outputs, one every two clock cycles. By the time the output queue empties of vectors produced prior to the error, new (corrected) output vectors will be made available (due to the full speed operation during correction), at which time the pipeline reverts to half-speed, computing again in dual-mode. In this way steady-state operation is achieved. From the outside world, there is no interruption of input and output streams.

SETs of the order of the clock period are eliminated in this approach, yielding quite a high LET threshold. The cost is only a 2X reduction in the theoretical maximum throughput and a minimal increase in power due to clocking. Meanwhile, SEU hits only need to be spaced by *N*/2 clock cycles to assure correct operation.

The input queue, shown in Figure 9, is implemented using an SRAM since this is far more area and power efficient compared to a shift register constructed of D flip-flops. The input queue SRAM does not need to be hardened. If the input queue is hit, this means no hit occurred in the pipeline so the input queue will be flushed of the erroneous values anyway. The output queue will also be implemented using an SRAM. In contrast to the input queue, the output queue does need to be hardened. Hence we will use our area and power efficient SEU-hardened SRAM to implement this output queue.

We have already designed a prototype DMR system and simulations have successfully demonstrated that SEUs are mitigated as expected. Given the very high speed of nanometer technologies, combinational logic running at ½ of its maximum possible speed can easily maintain system throughput requirements. Hence this DMR-in-time approach is quite attractive going forward since very large LET threshold SETs are filtered successfully.

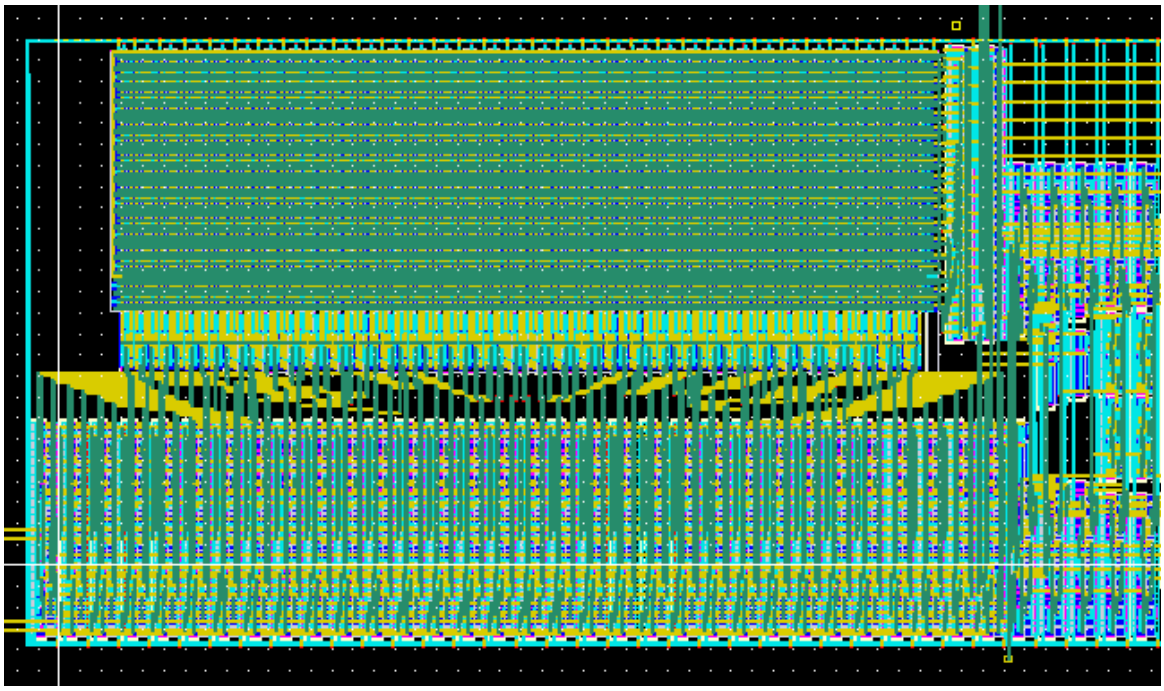


Figure 9. Input queue for DMR-in-time

Test Chips

During the first half of 2005, we designed a test chip in the IBM 8RF (.13 micron) process, which utilizes 8 metal layers (6 thin and 2 thick). The layout is shown of the test chip is shown in Figure 10. Total die area is 4.035 mm X 4.035 mm. The blocks on the test chip included:

1) 256Kbits SRAM (6T design) with EDAC and self-scrubbing (Lower Left, Figure 10).
2) 256Kbits DRAM (2T design) with EDAC and self-scrubbing (Upper Left).
3) A RADAR array employing TMR-in-time, capable of FIR and correlation functions for use with the Honeywell reconfigurable I/O subsystem (Lower Right).
4) A DMR-in-time input queue implementation (Middle Right).
5) A DMR-in-time output queue implementation (Upper Right)

An initial fab of this test chip (tapeout in Feb., 2005) contained an error in the I/O multiplexing scheme that allows blocks to share I/Os. This error currently prevents us from testing chips from this fab. We investigated the feasibility of using focused ion beam (FIB) facilities at ASU to repair the multiplexing circuitry, however the extent and type of errors effectively prevented any kind of repair.

In the meantime we made a number of improvements to the blocks, corrected the multiplexing scheme, and submitted a revision of the chip design for another fab (tapeout in June, 2005). We received the fabricated chips late in Nov., 2005 and since then have performed tests upon several of the blocks. At

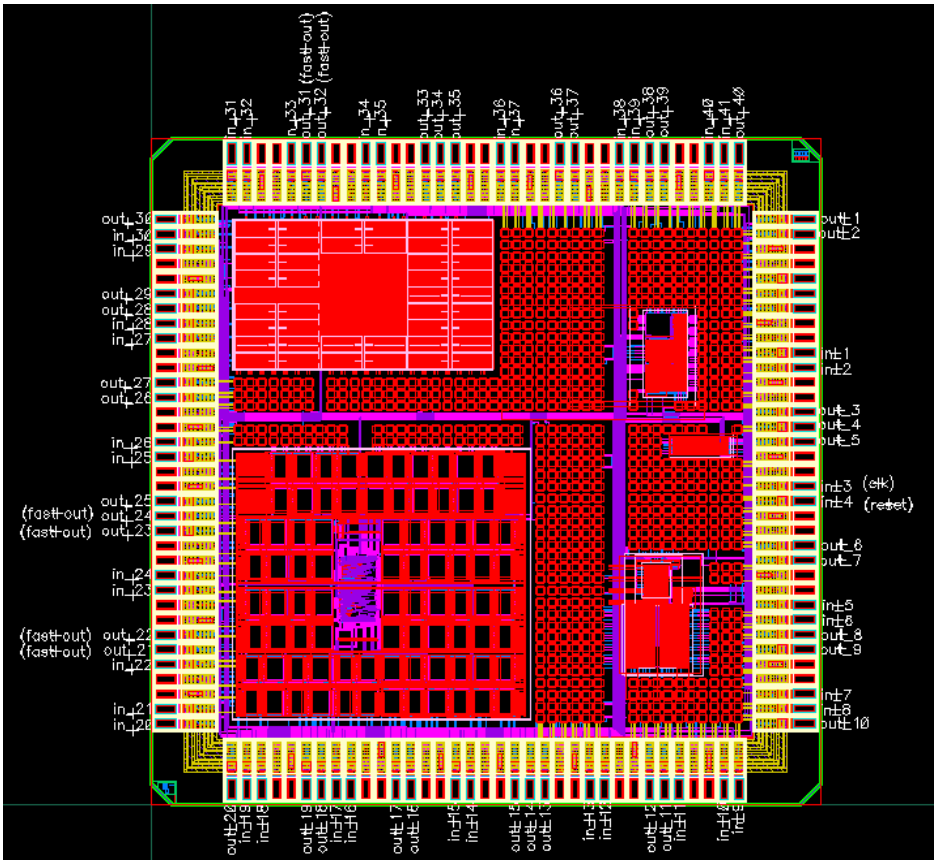


Figure 10. Layout of the UW RHBD test chip

this point (Mar., 2006), we have determined that the DRAM block is partially functional. Tests on it pointed to a charge-sharing problem that has been confirmed through simulation. The SRAM block is fully functional. We have artificially introduced errors into the memory array and verified that the EDAC circuitry successfully corrects these errors upon reading these locations. We have also verified that the scrubbing circuitry writes back the corrected words into the memory locations while the SRAM continues normal operation. The RADAR block and the DMR-in-time blocks remain to be tested.

Other Results

Technology Transfer/Intellectual Property

In a white paper submitted to AFRL entitled "Mixed Mode, Radiation Hard ASICs for Reconfigurable I/O," Dr. Andrzej Peczalski (Honeywell) described a reconfigurable I/O subsystem that incorporates the necessary functions to perform conditioning and conversion of analog and discrete signals for a wide range of applications. This subsystem was to be formed of blocks developed by 4 University groups: ADC (Prof. Adrian Leuciuc, SUNY), DAC (Prof. Gabor Temes, OSU), programmable PLL (Profs. Un-Ku Moon and Karti Mayaram, OSU), and Reconfigurable DSP (Profs. Larry McMurchie and Carl Sechen). The benefits of this subsystem are several. Its reconfigurable nature allows reuse in numerous aerospace systems, reducing development and integration time as well as cost. Reconfigurability also allows in-orbit remote repair and upgrade as well as dynamic reconfigurablity for mode and task agility. This reconfigurable I/O subsystem was assembled by Honeywell. Honeywell coordinated the University teams through a set of initial requirements and participation in design reviews, assuring that their ASICs will be compatible with the breadboard. The breadboard itself was designed and built at Honeywell Labs. Because of the error in the first tapeout and the late return of the chips from the second tapeout, we were not able to incorporate the RADAR reconfigurable FIR block into this reconfigurable I/O subsystem.

Publications Resulting from Research

L. McMurchie, C. Sechen, "RADAR – Reconfigurable Analog and Digital Array for Radiation Hardened Circuits," Proc. of the 2004 IEEE Aerospace Conference, Mar. 2004, Paper #7.0603.

D. Lam, L. McMurchie, C. Sechen, "SEU Hardening of Peripheral Circuitry in Self-Scrubbing SRAMs," Fourteenth Biennial Single Event Effects Symposium, Manhattan Beach, CA., April 2004.

James Lan, Duncan Lam, Victor Tang, L. McMurchie, C. Sechen, "Low-Overhead SEE-Hardened Programmable DSP Array," Fourteenth Biennial Single Event Effects Symposium, Manhattan Beach, CA., April 2004.

D. Lam, J. Lam, L. McMurchie, and C. Sechen, "SEE-Hardened-by-Design Area-Efficient SRAMs," Proc. of the 2005 IEEE Aerospace Conference, Mar. 2005, Paper #7.0302.

J. E. Kim, J. H. Lin, L. McMurchie, and C. Sechen, "Mitigation of Single- and Multiple-Cycle-Duration SETs using Double-Mode Redundancy (DMR) in Time," Proc. of the 2005 IEEE Aerospace Conference, Mar. 2005, Paper #7.0701.

Benefits to Commercial Sector

There are several novel aspects of this work that we intend to transfer to the commercial sector. One is the underlying architecture of the DSP subsystem. The RaPiD architecture is a hybrid FPGA/ASIC that provides some of the flexibility of an FPGA while obtaining the high-throughput and performance of an ASIC. We believe that many DSP applications can be mapped to this architecture more efficiently (in terms of power and delay) than commercial off-the-shelf DSPs. The second aspect of this work that we believe is transferable to the commercial sector is the way in which we have implemented radiation hardness. We have developed several techniques that result in modest energy/throughput degradation. All our techniques are designed to perform error correction with zero downtime.

PROJECT 10

RADIATION-HARD PLL DESIGN TOLERANT TO NOISE AND PROCESS VARIATIONS

Profs. Un-Ku Moon and Karti Mayaram (Oregon State University)
with Andy Peczalski (Honeywell)

RESEARCH TIME PERIOD: Three years
RESEARCH FOCUS: AFRL Task Areas 2 and 3: Standard Cell/Topologies in Radiation-Hardened SOI and Reconfigurable Mixed-Signal Electronics.

Figures and Tables

Abstract

This project addresses the design of radiation hard and noise tolerant phase-locked loops (PLLs) for frequencies greater than 1GHz in the Honeywell 0.35μm SOI CMOS (MOI-5) process. The overall focus is on a systematic design methodology for radiation-hard, noise tolerant PLLs in SOI CMOS processes. New circuits and architectures will be developed and combined with self-calibration methods and radiation hardened layout techniques. The self-calibration methods will enable tuning out process,

temperature, threshold voltage, and supply voltage variations yielding a robust design. Floating-body devices were compared with body-tied devices in the context of the PLL design and their effect on the PLL jitter/phase noise performance has been evaluated.

A brief summary of the effects of radiation on analog and digital circuits is given for background. The constituent parts of digital phase-locked loops (DPLLs) are described and their impact on the overall radiation tolerance is reviewed. A statistical time-to-digital converter (STDC) architecture intended to improve the DPLL performance is introduced. Layouts are shown for the test chip that has been taped out in the Honeywell 0.35µm SOI CMOS process. The test-chip includes a previously designed analog PLL and the new DPLL for comparison. Also included is the statistical time-to-digital converter.

Project Description

Phase-locked loops (PLLs) are key building blocks of frequency synthesizers and clock generators and they are used in nearly all analog, digital, and RF ICs. Although extensive work has been done in PLLs [1], very few radiation-hard PLL designs are available [2, 3]. A first step to achieving a certain degree of radiation hardness is the use of an SOI technology [4]. However, SOI CMOS processes introduce design challenges associated with the floating body, kink effect, and self-heating. These are characteristics specific to SOI MOSFETs and bulk CMOS designs cannot be readily transferred to SOI processes. Although options are available for body ties, these can introduce additional noise due to the large body resistance, whereby options of whether and how body ties should be used have to be evaluated [5]. These problems are further complicated by process variations encountered in scaled technologies. For these reasons, it is necessary to investigate circuits and architectures that result in PLLs that are insensitive to the process variations and noise in CMOS SOI processes. These designs will pave the way for high performance radiation-hard PLL designs.

One specific aspect that is being addressed is the sensitivity of the PLL to single-event effects (SEE). From simulations we have found that a single event can affect the function of the charge pump and hence the control voltage for the VCO. The effect can persist for a long time depending on the loop filter design and the overall bandwidth of the PLL. To overcome this particular problem we have proposed the use of digital control for the oscillator in our designs [6, 7]. These oscillators referred to as digitally controlled analog oscillators (DCAO) allow us to design an all digital PLL that will be significantly robust to SEEs.

Self-calibration methods enable tuning out process/temperature/threshold voltage and supply voltage variations yielding a robust design. This will be particularly important for radiation hard designs, since threshold voltage shifts due to total dose effects will be automatically compensated. Total dose leakage can be prevented by special layout techniques [8, 9, 10, 11].

We have developed an all digital PLL based on the initial results presented in [13] and designed the various sub-blocks such as the digitally controlled analog oscillator and the time-to-digital conversion circuitry including a statistical approach for time-to-digital conversion. The all digital PLL architecture combined with self-calibration methods [12] and radiation hard layout techniques [7, 11] will lead to radiation hard PLL design. This project addresses Task 2 of the AFRL Research Areas - *Standard Cell/Topologies in Radiation-Hard SOI*: Develop radiation-hard SOI analog or mixed signal sub-circuits and architectures for RF, communication, and signal processing applications. There is also an overlap with Task 3 - *Reconfigurable Mixed-Signal Electronics*: Develop radiation-hard SOI analog or mixed-signal sub-circuits or architectures capable of adapting to changing applications. The latter is addressed by the digital calibration/programmability that is being used in our approach. A systematic study of SOI and radiation specific issues will lead to a better understanding of how SOI CMOS can be best used for radiation hard PLL design – an important circuit block. The resulting knowledge base of radiation/noise tolerant PLL architectures, circuit techniques, and self-calibration methods will facilitate implementations of PLLs in SOI CMOS processes. Since our focus is on radiation hardness by design, our designs could be easily migrated to a radiation-hard process for additional radiation hardening.

Research Results and Discussion

The effect of radiation on electronic circuits is twofold: (a) total-ionization dose (TID) and (b) single event. Total-ionization dose causes a gradual shift in device threshold voltages and eventually causes failure. A single event hit causes transient errors. Radiation hardened blocks need to be tolerant to both single-event and total ionization dose.

TID causes the VCO characteristics to shift, charge-pump currents to change and hence alters the loop parameters of a PLL. This can also cause eventual failure in a charge-pump. These effects have been summarized in the testing results of our earlier test chip. Analog blocks are very sensitive to threshold voltages of active devices. TID over a prolonged period of time can prevent the transistors from switching properly. Unlike analog circuits, digital circuits are less susceptible to threshold voltage variations and can take larger doses of TID. Similarly, digital circuits can withstand single event transients. Hence, a digital phase locked loop is ideal for radiation hardening.

Digital phase locked loops (DPLLs) have a number of advantages. Their inherent digital nature makes them easy to design and implement. They are mostly composed of conventional digital logic gates. The loop-parameters of a digital phase locked loop can be controlled by modifying digital bits. Self-calibration can be implemented to overcome the effects of TID. Furthermore, redundancy can be built into the system to make it single event tolerant. Figure 1 shows the schematic of a typical digital phase locked loop [14].

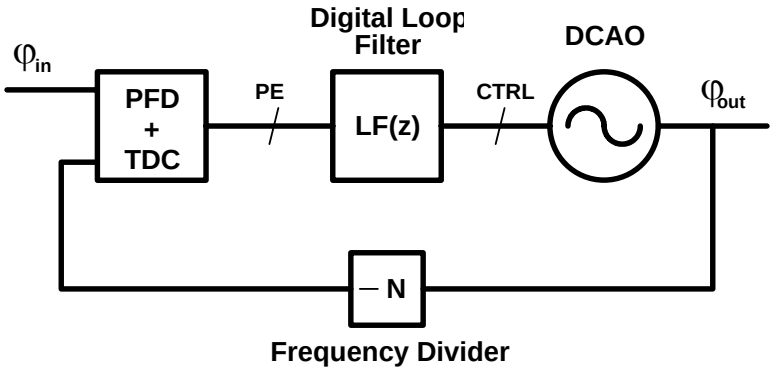


Figure 1. Digital phase locked loop.

DPLLs are composed of: (a) digitally controlled analog oscillator (DCAO), (b) frequency divider, (c) time-to-digital converter (TDC), and (d) digital loop filter (LF). The DCAO is an analog oscillator whose frequency is controlled by a digital word. The intrinsic oscillator can be an LC-tank or ring type architecture. Frequency tuning in an LC-tank oscillator is achieved by switching a parallel bank of capacitors. Similarly, a ring oscillator can be controlled by switching parallel current sources to control the tail current in the delay element. The output of the DCAO is divided to enable comparison with the reference input. The TDC compares the phases of the reference and the DCAO divided output to generate the phase error as a digital word. The LF filters the phase error to produce the control word for the DCAO. These building blocks have been described in detail in the following section.

DPLL Building Blocks

Digitally controlled analog oscillator

The DCAO is implemented as a three stage differential ring oscillator. It has undergone a substantial redesign since the winter meeting to allow greater frequency resolution. The differential delay elements are Lee/Kim type with dual control inputs, which allow for fine and coarse tuning. The schematic of the delay element is shown in Figure 2. Two banks of current mirrors allow digital control of the fine and coarse tuning voltages. The tuning circuits convert the two 6-bit words into the analog VCOARSE and VFINE voltages. The schematic of the fine tuning circuit is shown in Figure 3. The coarse tuning circuit

is identical. The operation is as follows: The digital input, DF[0-N], determines which current sources are drawing current from PM1. This sets the voltage at VFINE and controls the speed of the oscillator. The resistor, R1, determines the unit value of current to be mirrored on the right half of the circuit. This resistor is off-chip to allow control of the trade-off between gain, resolution and tuning range. Figure 4 shows the tuning curves using two different resistor values. The top curve has a high gain and high tuning range, but low frequency resolution and a large overlap between adjacent coarse tuning ranges. The bottom curve has better resolution and a smaller overlap, but sacrifices tuning range to achieve this. We intend to vary the resistors in our testing to find the optimal operating point.

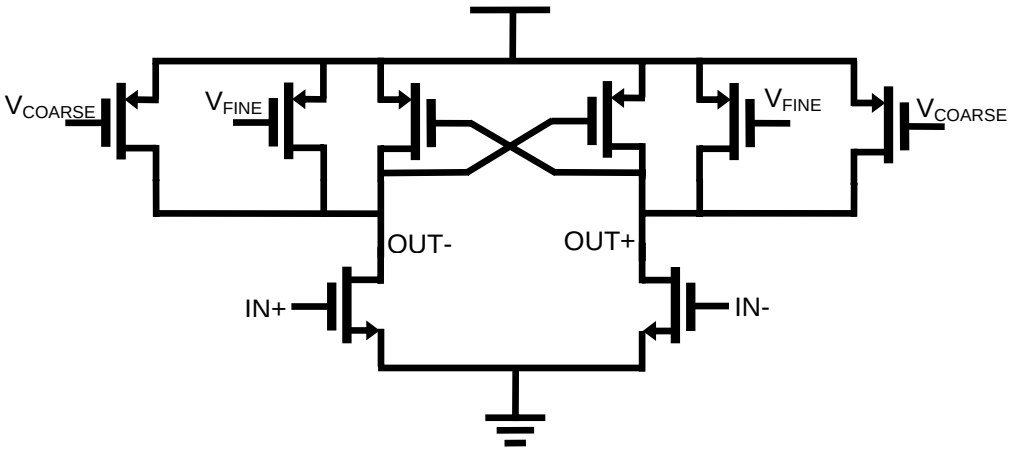


Figure 2. Lee/Kim differential delay cell with dual tuning inputs.

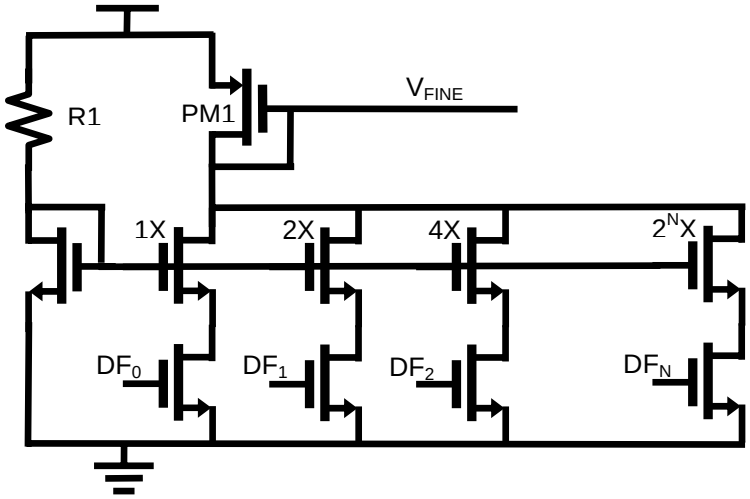


Figure 3. Fine tuning control circuit.

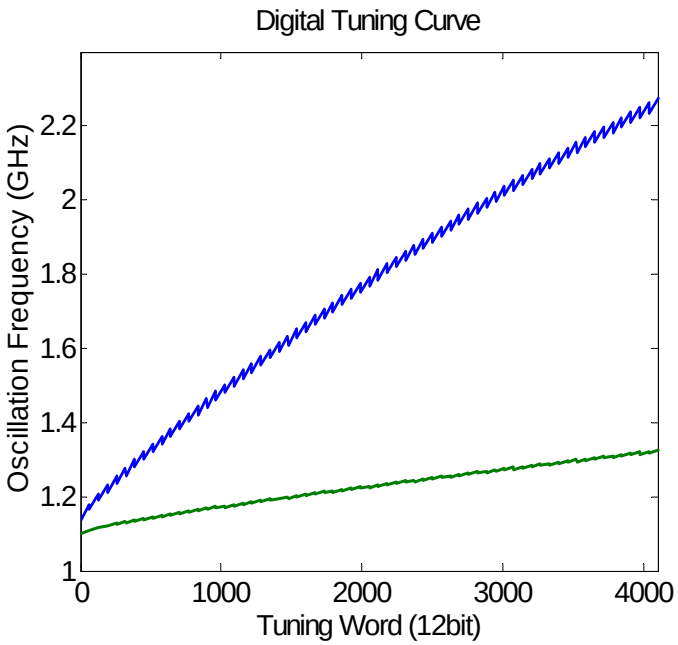


Figure 4. Tuning range control with off-chip resistors.

Frequency divider

The frequency divider is implemented as a cascade of divide-by-two stages. Each stage is a *true single phase clock* logic flip-flop [18] in feedback. A circuit diagram of the flip-flop and a single divide-by-two stage is shown in Figure 5. The output of the displayed stage toggles at every rising edge of the clock. Hence, the output frequency is half that of the input frequency. Higher frequency division ratios can be achieved by cascading such stages. In order to make the division ratio programmable a multiplexer has been added to enable us to select from a choice of division ratios. The schematic diagram of the programmable frequency divider is shown in Figure 6. The possible division ratios are 8, 16, 32 and 64. They can be selected using the control bits S1 and S0.

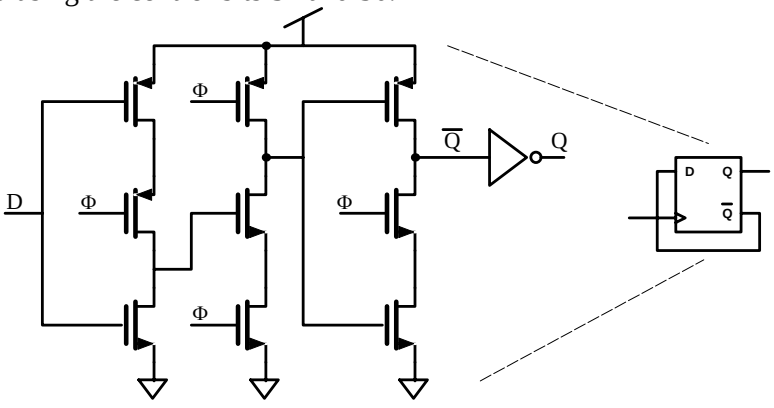


Figure 5. TSPC flip-flop and a divide-by-two stage.

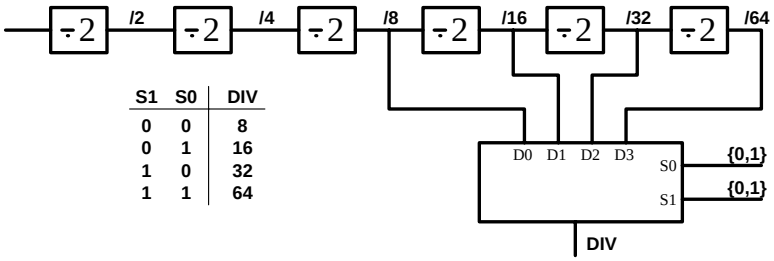


Figure 6. Programmable frequency divider.

Time-to-digital converter

The time-to-digital converter compares the input reference clock and the oscillator divided output and generates the phase difference word. The operation is performed as follows. The phase/frequency detector (PFD) at the input of the TDC generates UP & DN pulses. A digital OR gate generates a pulse whose width is equal to the width of the wider of the two pulses. The delay chain in a TDC generates delayed versions of the OR pulse. When these delayed versions are latched by the falling edge of the OR pulse, the number of latch outputs that are high is the width of the OR pulse expressed in number of inverter delays. A matching delay circuit is implemented using current starved inverters to compensate for the finite width of the UP/DN pulses in a PFD. A linear delay chain would require a large number of inverters and latches to cover the entire range. An exponential delay chain, however covers a wider range with fewer stages. The initial stages of the exponential delay chain have minimum possible delays to provide finer resolution and the subsequent stages have larger delays to cover a wider range.

The minimum delay is the resolution of the TDC. It is denoted by dT and is about 80-100ps in the given process. This delay includes the effects of the loading of the subsequent stages and the latch. The value of the delay elements in the delay chain are dT, dT, dT, 4dT, 8dT, 16dT, 32dT, 64dT and 128dT. These nine stages cover a delay range of dT-256dT. The sign of the phase error is evaluated by latching the DN pulse with the UP pulse. The output would be high (sign is negative) when the DN pulse comes before the UP pulse. This occurs when the oscillator divided output leads the reference clock. The possible output values of the TDC are -256 to 256 in conjunction with the sign bit. The latch outputs are converted to 10-bit 2's complement signed digital word through the pseudo-thermometer encoder. Due to the exponential nature of the delay chain, the design of the encoder is greatly simplified. Figure 7 shows the schematic of the TDC.

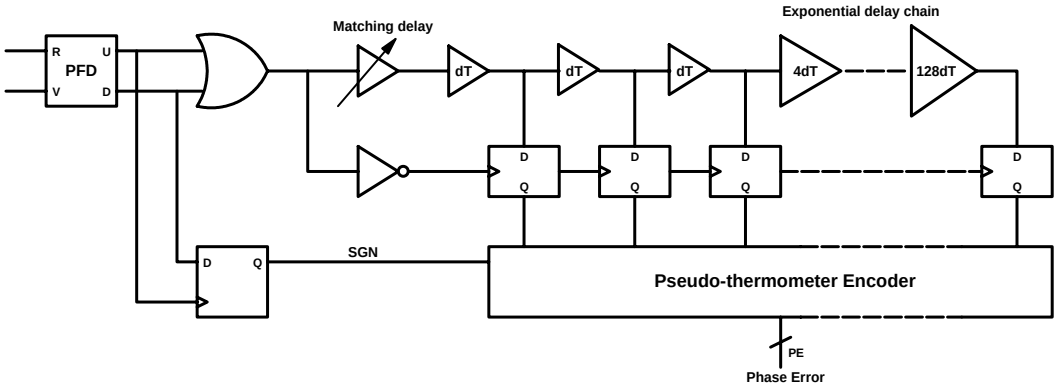


Figure 7. Time-to-digital converter.

The implementation of the TDC transfer function has a significant influence on the performance of a digital PLL. The inherent digital nature of the TDC introduces quantization into the output of the TDC. TDC implemented with a dead-zone entails the openloop operation of the digital PLL. For small phase errors, the digital PLL does not correct itself. This continues until sufficient phase error accumulates to produce an output. This greatly deteriorates the performance of the PLL. This can be prevented by making the TDC bang-bang. When in lock, the digital TDC would generate +1 and -1 outputs alternatively. The input output transfer functions of both such TDCs are shown in Figure 8.

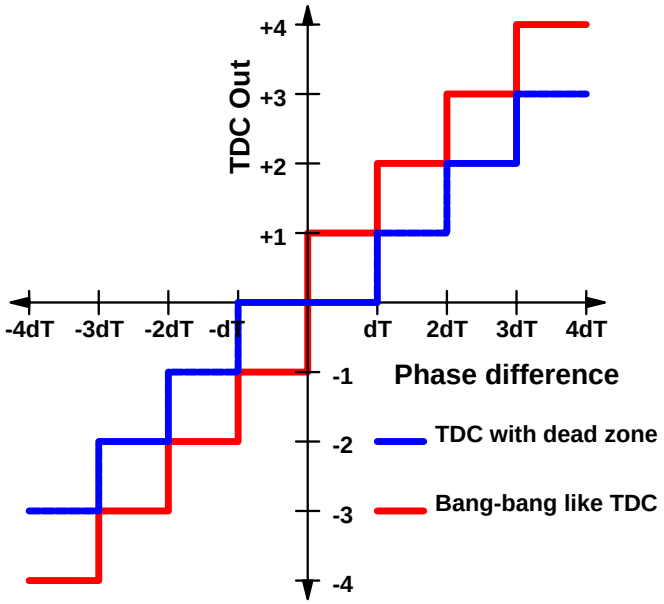


Figure 8. Input output transfer function of the TDC.

Digital proportional-integral controller

The loop-filter in the digital PLL is a proportional-integral (PI) controller with a proportional and an integral path. The former is analogous to the resistor in a charge-pump PLL, while the latter is comparable to the capacitor. Figure 9 shows the architecture of the loop-filter. The integral path consists of an accumulator and a gain "**β**". The proportional path has a gain "**α**". The outputs of the proportional path and integral path are added and normalized to give the control word. The length of the accumulator register is 16-bits. This accumulator is implemented by stacking 16 single-bit accumulators. A schematic showing the single-bit accumulator and the 16-bit accumulator is shown in Figure 10. The latch used in the accumulator was shown in Figure 11 and the mirror adder circuit has been shown in Figure 12. Implementing the proportional and integral gains requires digital multipliers. However, multiplication by powers of two can be achieved by adding zeros at the end of the word or truncating bits. The proportional gain is set to one and the integral gain was set to 2^{-5}. To keep the jitter arising from the discrete nature of digital PLL low, the normalizing gain has to be less than 1 and has been set to 0.5. Figure 13 shows the implementation of these gains in the digital PLL.

The accumulator and the adder in the loop filter can overflow and give erroneous outputs. This can be prevented by implementing saturating adders. Overflow occurs when the inputs are positive and the output is negative. Similarly, underflow occurs when the inputs are negative and the output is positive. Error cannot occur when the inputs have opposite signs. The saturating adder detects overflow or underflow and limits it to the highest (2^N-1) or lowest (-2^N) values. The schematic of the saturating adder implemented is shown in Figure 14.

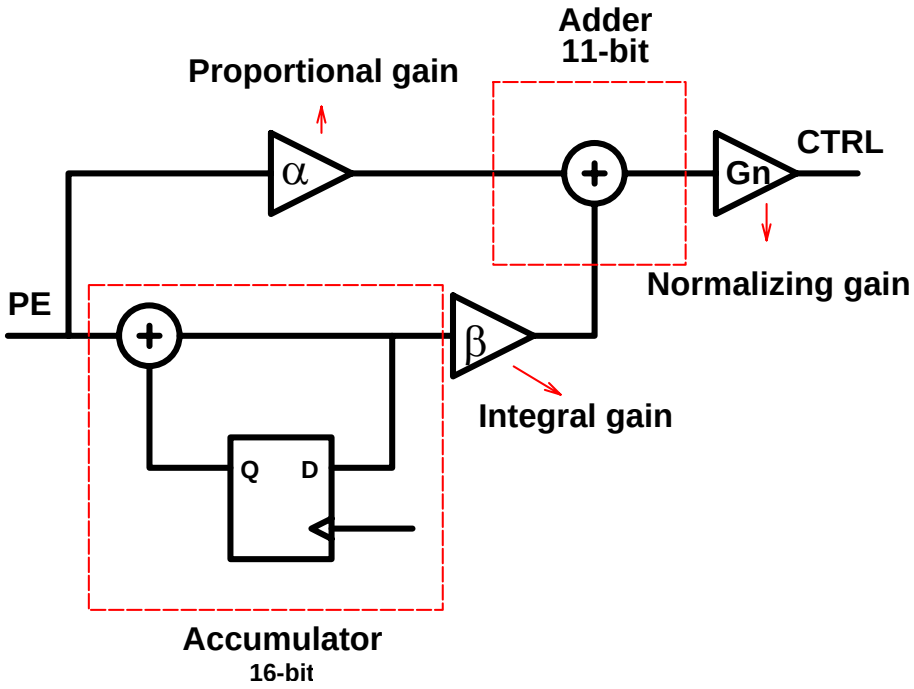


Figure 9. Proportional-integral controller loop filter.

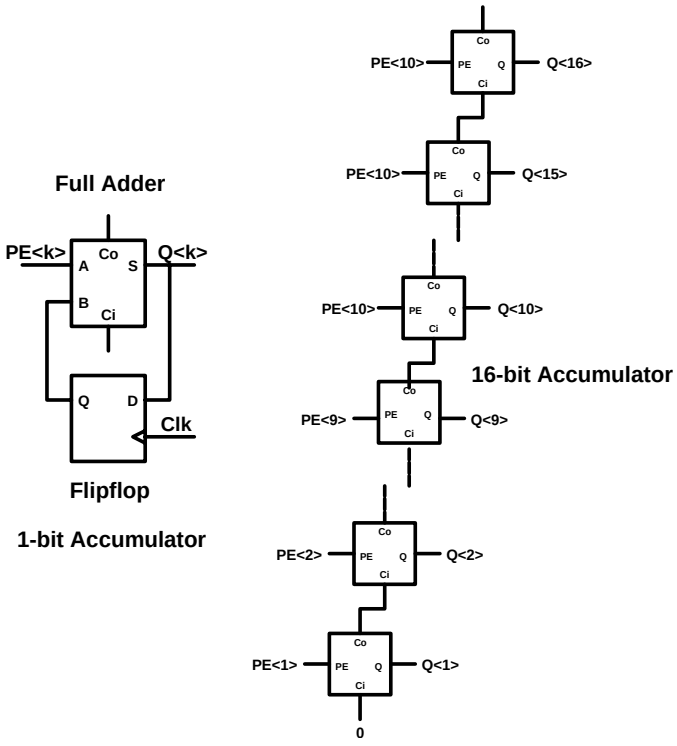


Figure 10. 1-bit accumulator and 16-bit accumulator.

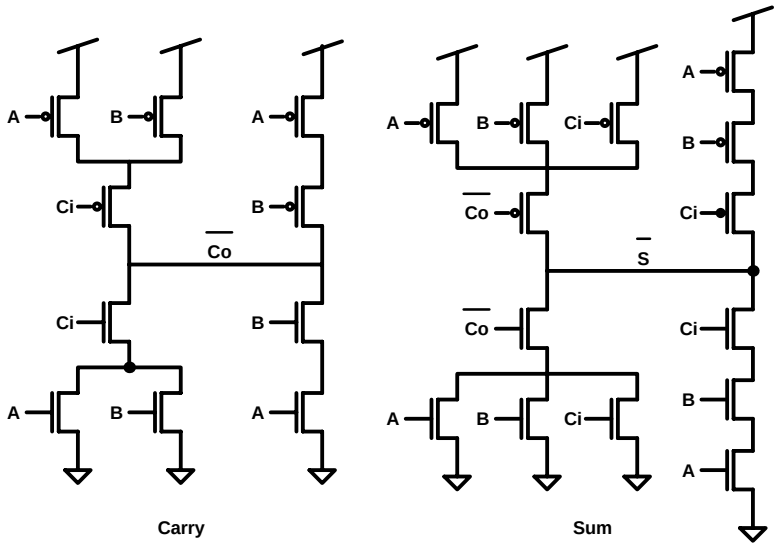


Figure 11. CMOS mirror adder circuit.

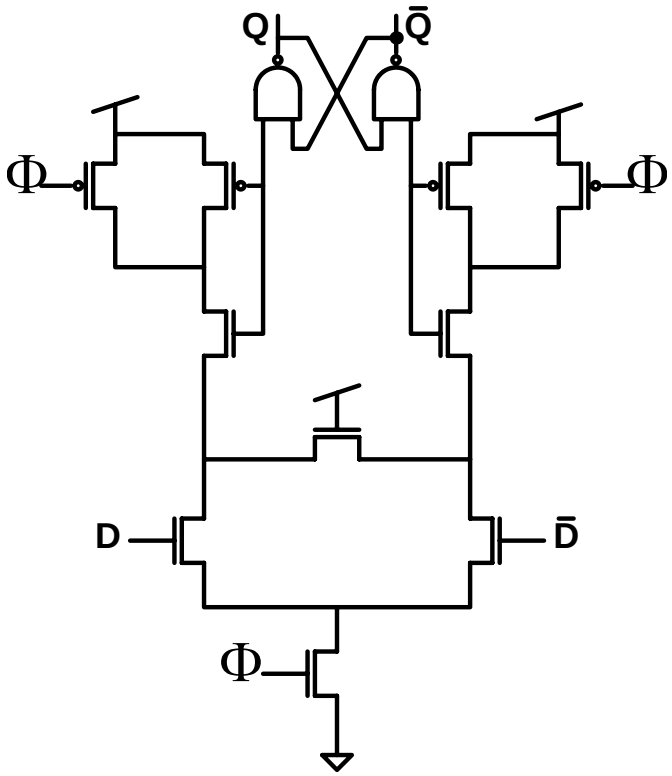


Figure 12. Sense-amplifier flip-flop.

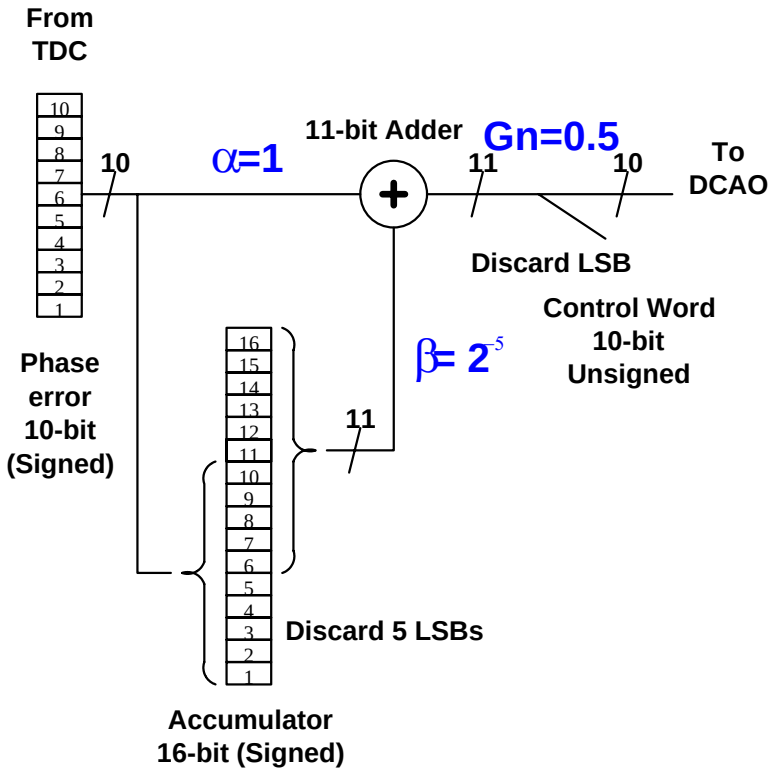


Figure 13. Digital PLL controller.

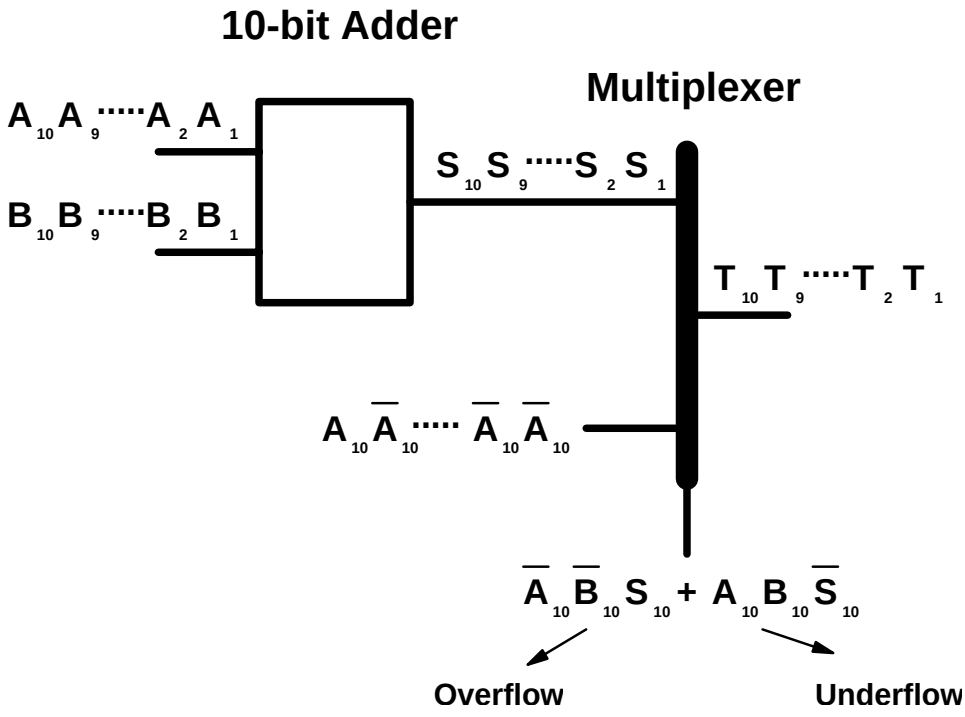


Figure 24. Saturating adder.

Single Event Tolerance

Single event effects are transient errors caused in a system as a result of a radiation strike. After a heavy metal ion hits a node, charge is accumulated. This sudden accumulation of charge causes transients in the circuit. These transients can cause errors in a system. The effect of such transients on various blocks of a phase locked loop has been described in [15]. In summary, a hit on the VCO causes small phase disturbance which is quickly restored by the loop. Similarly, a hit on the first few stages of the frequency divider is not severe. However, a hit on the last stages of the frequency divider or PFD can cause phase errors of up to half a reference cycle (π radians). However, the most critical node in a PLL is the output of a charge-pump. This is by far the most sensitive node in a PLL. A hit on this node can cause a significant disturbance in the control voltage. The loop would require several time-constants to restore the system to lock. Redundancy in the frequency divider and PFD can make these blocks robust to single events. However, the control node in a conventional PLL cannot be completely shielded from a single event strike. Increasing the loop capacitance can reduce the amount of disturbance, but this reduces the bandwidth and slows down the response of the system.

Digital circuits are inherently robust to single event hits. The amount of transient error voltage required to upset a digital bit is large. A single event strike on combinational circuits is less harmful. Such circuits are driven and their normal states are restored almost immediately. However, a hit on latches can be permanent. The saved state of a digital latch can be altered by a single event strike. Redundancy and error correction mechanisms are readily available for digital circuits and are amenable for implementation.

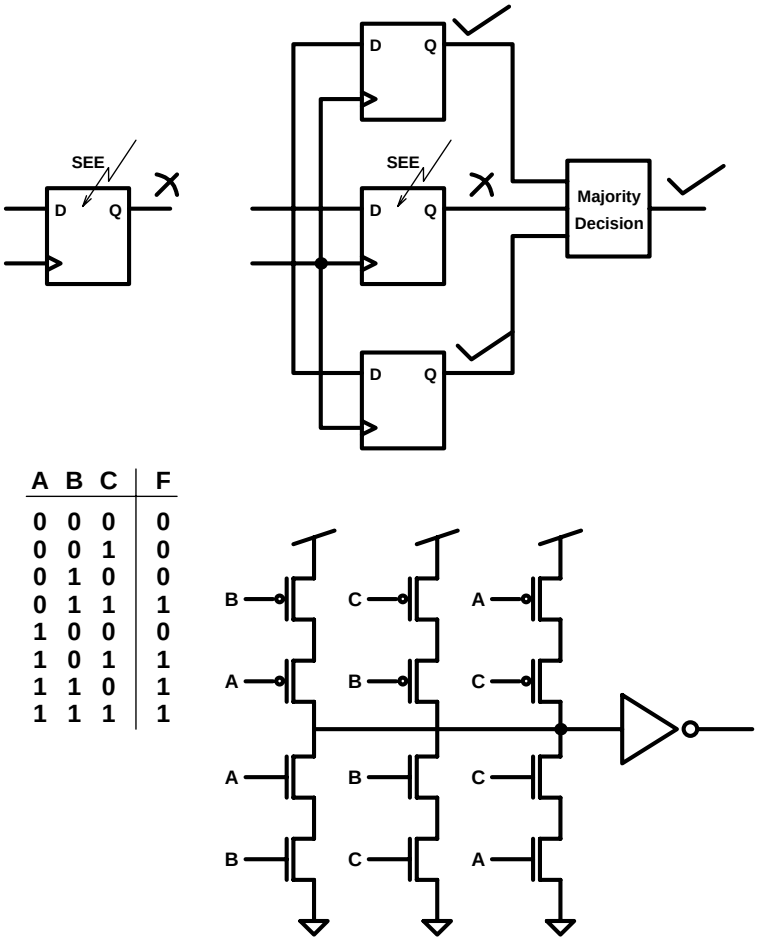


Figure 15. Majority decision circuit.

Figure 15 shows the schematic of a majority decision circuit. The figure shows that an error caused in a single latch cannot be prevented. However, if the latch is duplicated and a majority vote is implemented such an error can be prevented. Every latch which is susceptible to a single event strike has to be replaced by the above block to make it single event-tolerant.

As described earlier, the last stages of the frequency divider, the phase detector and the loop filter have sensitive digital values. These blocks have to be modified to make them single event tolerant. A hit on the first three stages of the frequency divider causes phase errors less than one-eight of the reference cycle. However, these stages account for up to 80% of the power consumption in the frequency divider. Duplication of these blocks doubles the power consumption of the frequency divider. Hence, a trade-off has been made between the power consumption and the severity of the hit. In conclusion, only the last three stages of the frequency divider have been made single event tolerant. Figure 16 shows the implementation of redundancy on a frequency divider stage.

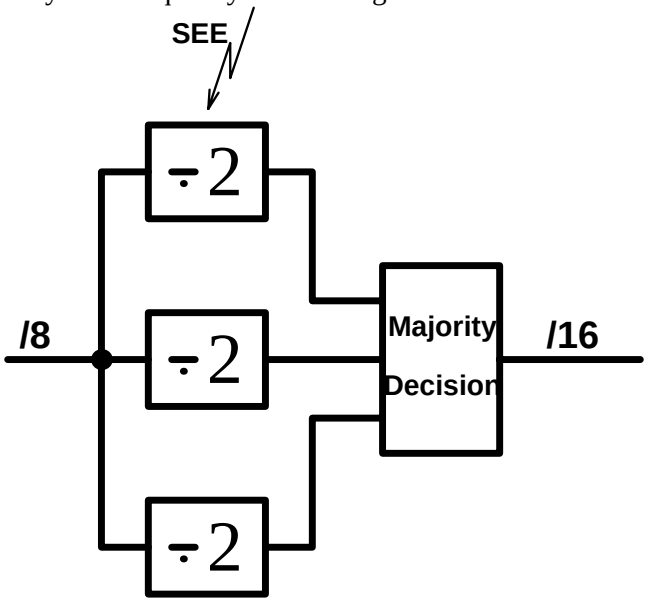


Figure 16. SEE hardening of a frequency divider.

Similarly the PFD has also been made single event tolerant. A bit flip on the MSBs of the TDC can cause an error transient. These bits can be secured by duplicating and implementing majority vote. Similarly a bit flip on the accumulator can cause the PLL to go out of lock. The MSBs of the accumulator have also been made single event tolerant. Figure 17 shows the radiation hardening of the TDC and loop-filter by duplicating the susceptible and sensitive latches.

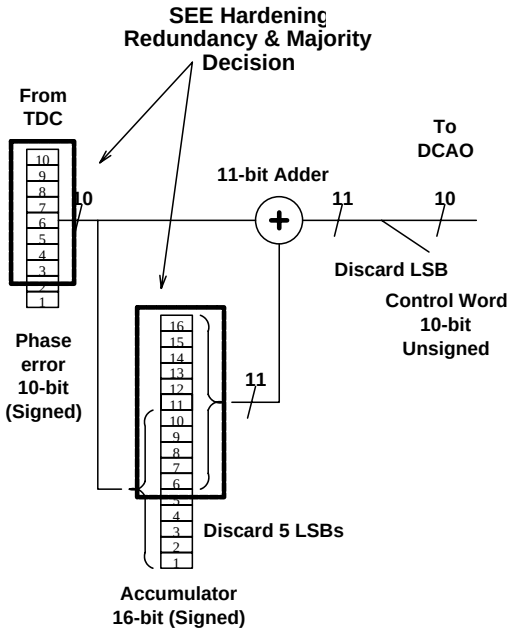


Figure 17. SEE hardening of TDC and loop-filter.

Digital PLL Analysis

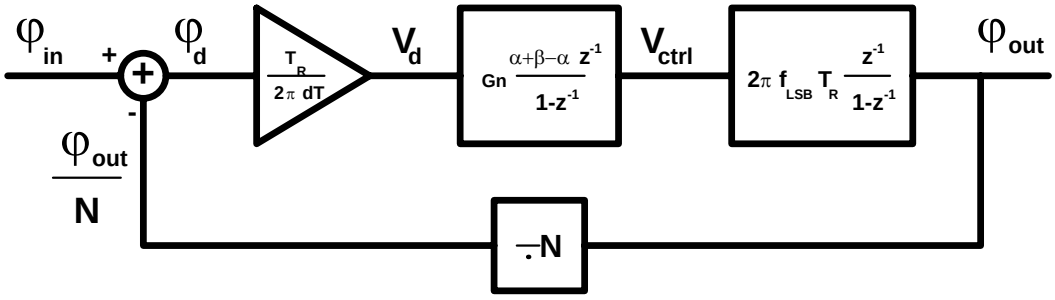


Figure 18. z-domain model of the digital PLL.

The z-domain model of the digital PLL can be seen in Figure 18. This can be analyzed as follows. Let $\varphi_i[n]$ and $\varphi_o[n]$ be the input and output sampled at every reference cycle. The phase accumulated by the output of the DCAO every reference cycle is proportional to the control word:

$$\varphi_o[n+1] - \varphi_o[n] = 2\pi f_{LSB} T_R v_{ctrl}[n]$$

$$\frac{\varphi_o(z)}{V_{ctrl}(z)} = 2\pi f_{LSB} T_R \frac{z^{-1}}{1-z^{-1}}$$

where, f_{LSB} is the resolution of the DCAO and T_R is the period of one reference cycle. For a phase error of 2π, the output of the TDC is T_R/dT. Here, dT is the resolution of the TDC.

$$v_d[n] = \frac{1}{2\pi}\frac{T_R}{dT}\varphi_d[n]$$

The output of the loop-filter is the scaled sum of the proportional and integral paths.

$$\frac{V_{ctrl}(z)}{V_d(z)} = G_n\left(\alpha + \frac{\beta}{1-z^{-1}}\right)$$

$$\frac{V_{ctrl}(z)}{V_d(z)} = G_n\frac{\alpha+\beta-\alpha z^{-1}}{1-z^{-1}}$$

The loop gain of the digital PLL is given by

$$\frac{\varphi_o(z)}{\varphi_i(z)} = \frac{1}{N}G_n\frac{T_R}{dT}f_{LSB}T_R\frac{\left(\alpha+\beta-\alpha z^{-1}\right)z^{-1}}{\left(1-z^{-1}\right)^2}$$

and the closed loop gain is

$$\frac{\varphi_o(z)}{\varphi_i(z)} = \frac{K_{dig}\left(\alpha+\beta-\alpha z^{-1}\right)z^{-1}}{1-\left(2-\frac{K_{dig}}{N}(\alpha+\beta)\right)z^{-1}+\left(1-\frac{K_{dig}}{N}\alpha\right)z^{-2}}$$

where, $K_{dig} = G_n(T_R/dT)f_{LSB}T_R$.

This is analogous to a charge-pump PLL where the loop gain is

$$\frac{\varphi_o(z)}{\varphi_i(z)} = \frac{1}{N}\frac{K_{CP}}{s^2}(s+\omega_z)$$

At low frequencies, the s-domain and z-domain models are connected by the following equations.

$$\frac{\beta}{\alpha} = \frac{\omega_Z}{F_R}$$

$$K_{CP} = K_{dig}F_R$$

where, F_R is the update frequency of the digital PLL ($T_R = 1/F_R$).

A method to evaluate the loop parameters for a given DCAO & TDC resolution and phase margin is described below. Figure 19 shows the magnitude and phase response of a 2nd order PLL. In a 2nd order system, the phase margin is the contribution of the zero at the unity gain frequency.

$$\Phi_M = \tan^{-1}\left(\frac{\omega_{UGB}}{\omega_z}\right)$$

And the unity gain frequency is given by

$$\omega_{UGB} = \frac{K_{dig} F_R}{N} \sqrt{1 + \tan^2(\Phi_M)}$$

The above equations give the unity gain frequency and the maximum value of the zero frequency that gives the required phase margin. These equations can be used to estimate the required value of β.

For a digital PLL with f_{LSB}=200kHz, dT=50ps, N=20, F_R=50MHz (F_{vco}=1GHz), Φ_M=80°, G_n=0.5 and α=1, the estimated value of β=0.01432 and f_{UGB}=646kHz. Simulink models for this digital PLL were simulated and the transient performance of the model agrees with the z-domain model. Figure 20 shows the response of the digital PLL plotted using MATLAB.

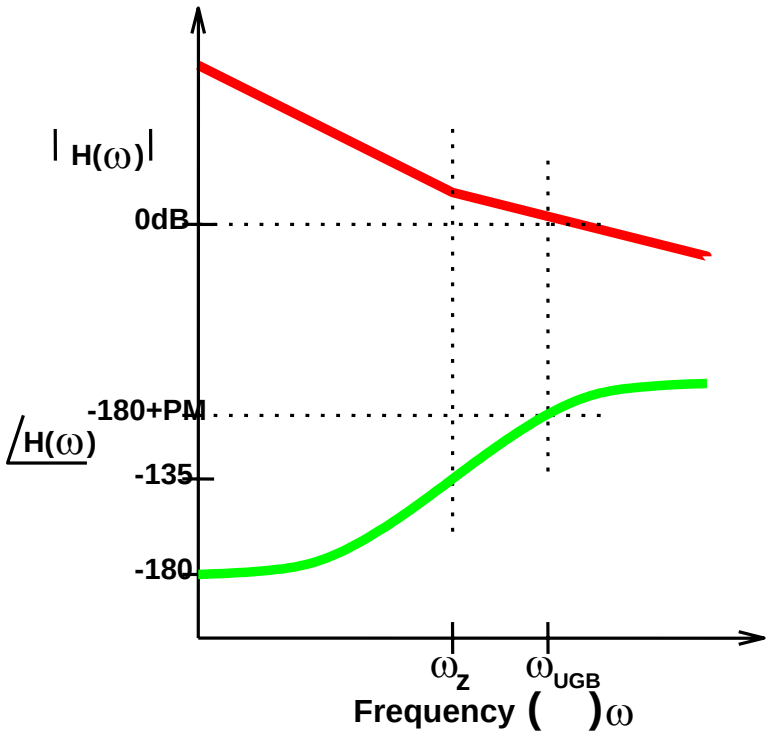


Figure 19. Magnitude and phase response of a 2nd-order PLL.

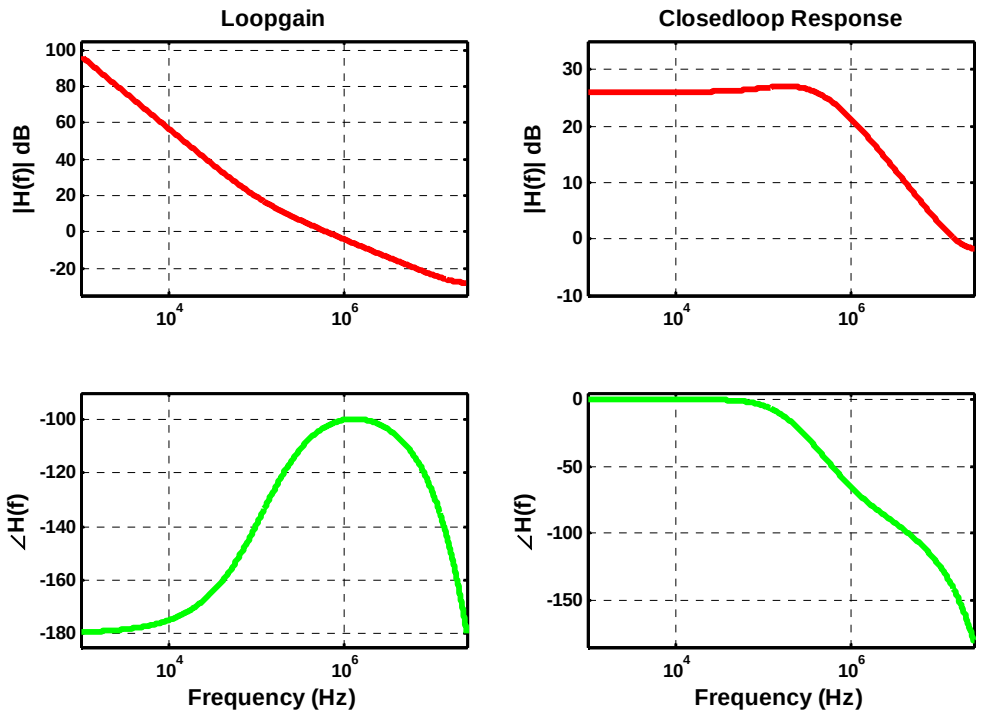


Figure 20. Magnitude and phase response of digital PLL.

Digital PLL Layout

Frequency Divider

The layout of the frequency divider can be seen in Figure 21. It shows the six stages of the frequency divider and the multiplexer to choose different division ratios. The last three stages of the frequency divider are duplicated and redundancy has been implemented.

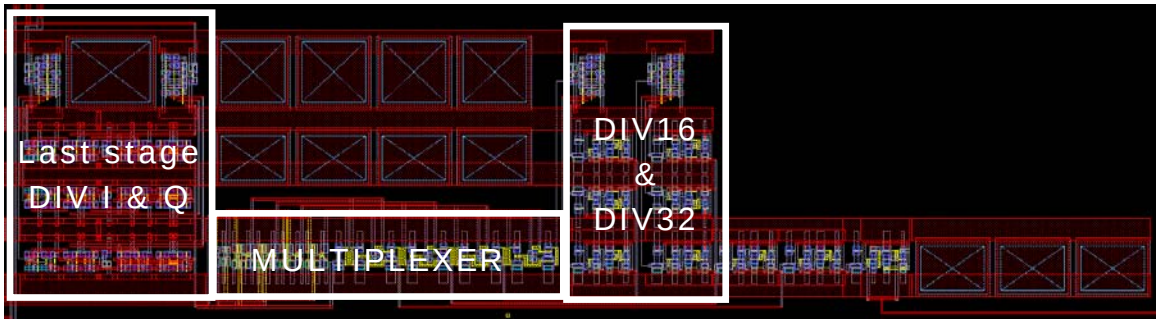


Figure 21. Layout of frequency divider.

PFD & TDC

Figure 22 shows the layout of the PFD and the TDC. The PFD has been duplicated and majority vote has been implemented. The layout also shows the exponential delay chain, the latches and the encoder. The MSB latches have been duplicated and majority vote has been implemented.

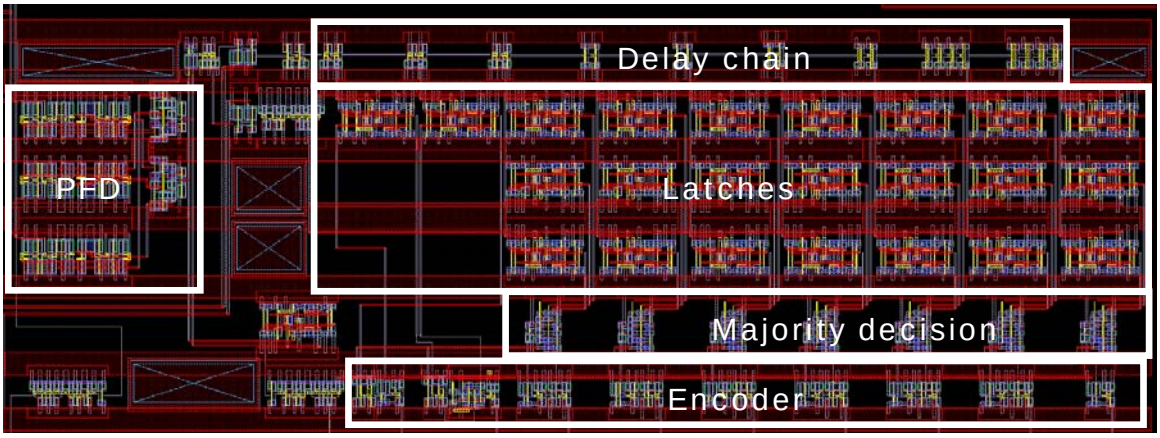


Figure 22. Layout of the PFD & TDC.

Loop Filter

The layout of the loop filter can be seen in Figure 23. This shows the 16-bit accumulator and the 11-bit saturating adder.

Digital PLL

The layout of the digital PLL can be seen in Figure 24. It shows all the building blocks of the digital PLL and the I/O buffers. The area of the digital PLL is 1.8x1.2mm^2. This excludes the area of the decoupling capacitors and the I/O buffers.

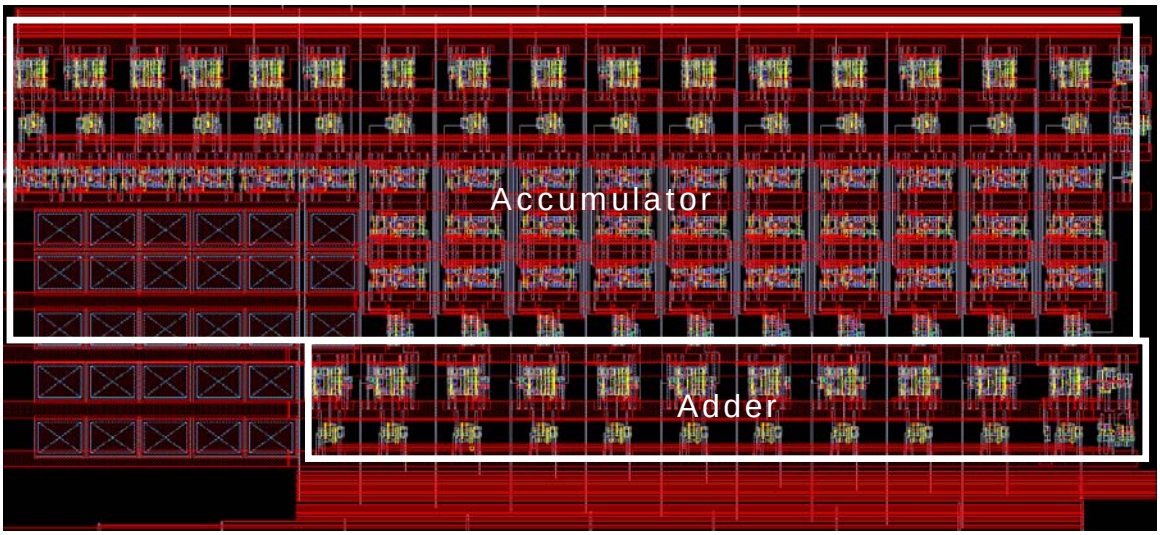


Figure 23. Layout of the loop-filter.

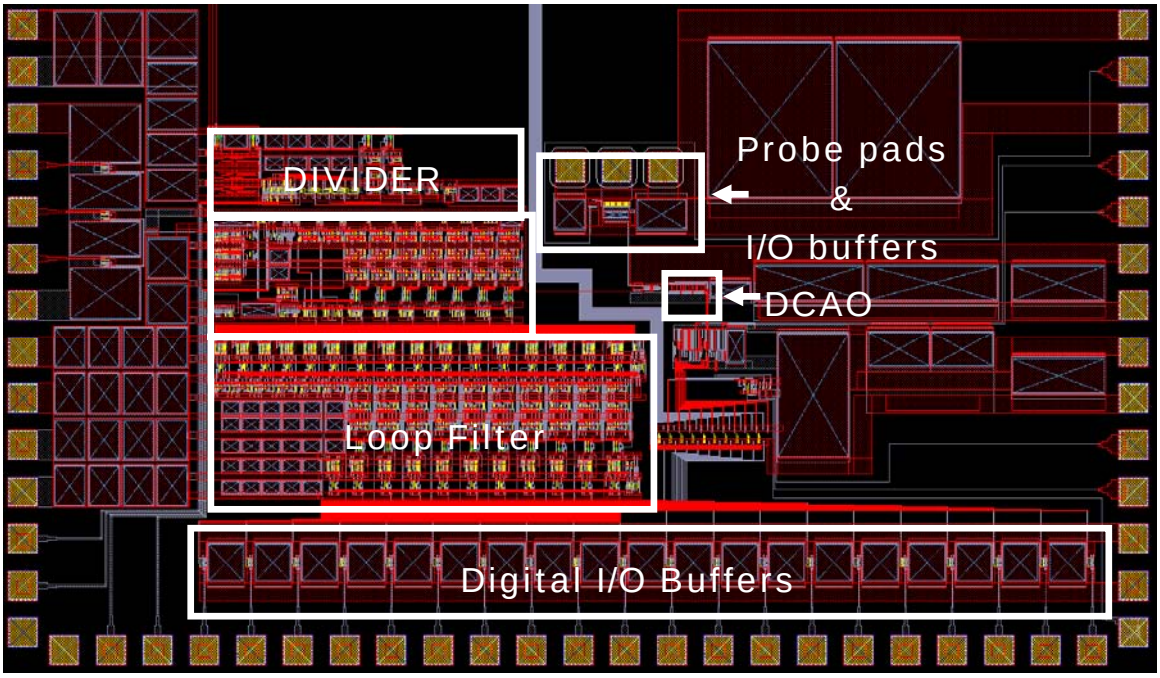


Figure 24. Layout of the digital PLL.

DCAO Core

The DCAO layout is shown in Figure 25. Parasitic capacitance on the switching path is critical in determining the speed of oscillation so great care is taken to minimize the size and the length of the interconnects between stages. The core is fully symmetric leading to matched differential loading and delays. A large bypass capacitor is placed nearby to keep the supply clean. The core size is 125µm X 40µm.

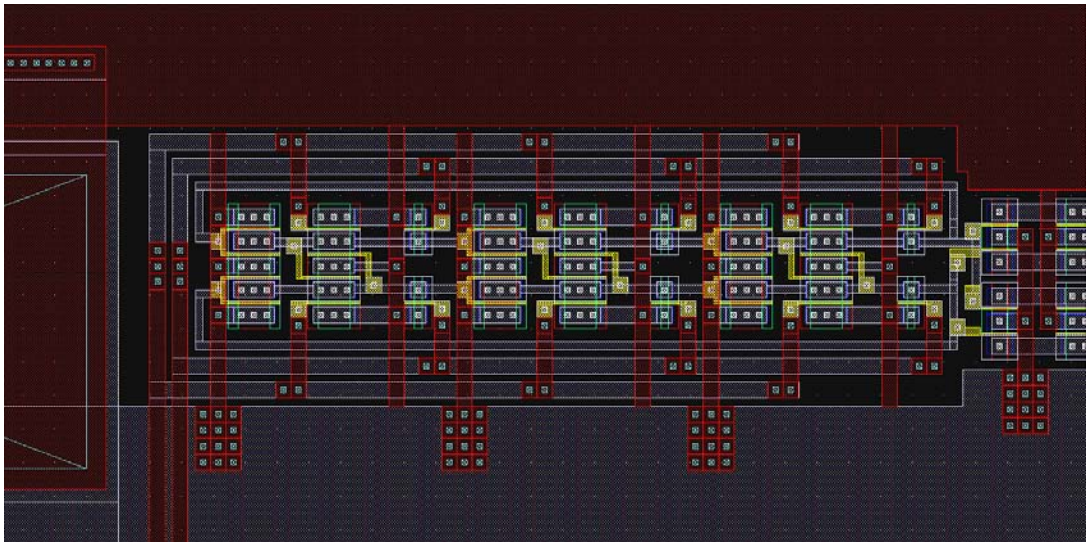


Figure 25. Layout of the DCAO core.

Statistical Time-to-Digital Converter

The statistical time-to-digital converter (STDC) is intended to make up the fine loop of the phase detector in a DPLL. This block aims to increase the resolution of time detection beyond a single inverter delay, which is the best that can be expected from the inverter chain approach used in the coarse loop. A high resolution in time detection improves the noise performance of the overall system and is thus desirable.

The theory behind the operation of the STDC was described in [16] and will be briefly summarized here. The STDC relies on the finite voltage offset between two inputs of a set of arbiters on a given wafer. These arbiters have as their inputs the two rising edges that define the time window to be digitized by the STDC. These circuits report which edge arrives first by latching a 1 or a 0 at the output.

As there will be finite mismatch between the arbiters, they will never be identical and thus exhibit an input voltage offset with a certain statistical distribution. This suggests that identical inputs to separate latches may generate conflicting output bits. The information contained in the distribution of these output bits can be used to represent the timing difference between the incident edges in a digital fashion. Using a decision scheme that processes all the latch outputs and produces an output word corresponding to the majority of the latch decisions, the time window of interest can be digitized with higher precision than possible with a chain of inverters.

The statistical distribution of the offsets significantly affects the distribution of the output codes. This offset is modeled as a normal distribution with properties that depend on device sizing. Specifically, the expected offset distribution for a given design can be calculated using the Pelgrom coefficients [17], which can be obtained from process data. As described in [16], a larger standard deviation in the input offset voltages of the arbiters implies a larger dynamic range in the transfer response of the STDC, at the expense of lower resolution.

Another point to note is that input signal rise times affect the transfer curve similarly. A large rise-time implies larger dynamic range with the STDC saturation points pushed out. Conversely a fast rising signal is less susceptible to arbiter offsets and thus the dynamic range is reduced. Thinking at the extreme case of an infinitely fast signal makes this effect easier to understand. Considering a square wave input to the arbiters, we can deduce that regardless of the offset, the arbiter output trips when the square wave rising edge arrives. Hence for signals with a rise time of zero, offsets would change nothing. In this respect, a large (small) rise time has the same effect as a large (small) distribution in the arbiter offsets.

Implementation

The implementation in this test chip is intended to enable testing with external stimuli as well as observing the output codes when the STDC is operated along with the DPLL. Both situations make use of the same circuitry, which is described next.

Delay and Slew Control

For characterizing the STDC, it is desirable to have a means of controlling the phase delay to be digitized. Moreover, the rise time of the input signals needs to be controllable to enable comprehensive testing, because as described earlier, signal rise times have the same effect as offset voltage distributions within the STDC. This functionality is incorporated using a set of current starved inverters and a common-source (CS) amplifier stage with controllable bias current. The inverters give programmable delay while the CS stage enables variable slew rate. Both inputs to the arbiters pass through an independent delay and slew control stage, with a total of four controls overall. With this arrangement, one edge can be advanced or delayed with respect to the other, and the slew rate can be modified as desired to test the dynamic range of the converter.

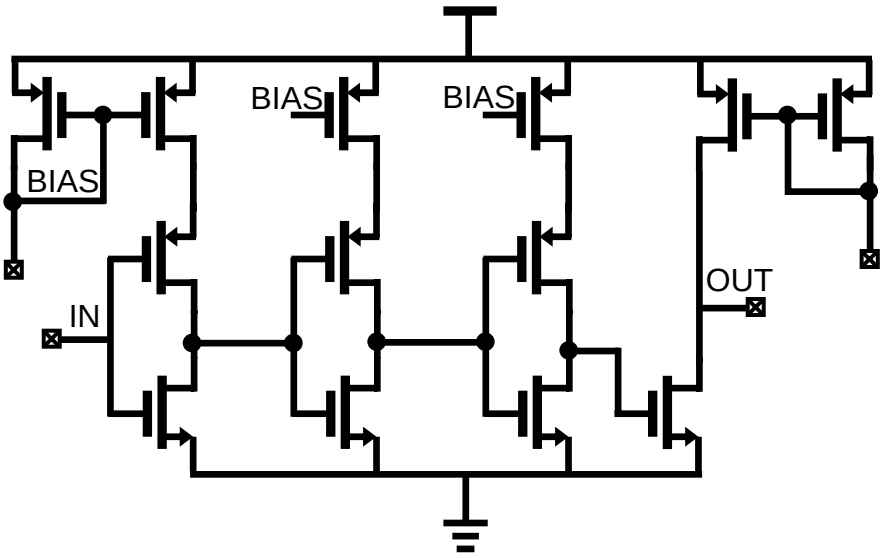


Figure 26. Delay and rise time control circuit.

The circuit diagram is shown in Figure 26. The control currents are generated using off-chip variable resistors. Decoupling capacitors are placed between the bias nodes and VDD to minimize noise on supplies affecting the bias point and corrupting measurements. When testing the STDC with the ADPLL reference and DCAO output, the delay controls can be shorted together at the output so as to not introduce any extra delay into the measurements. The delay components can generate a total delay between the signals of up to 1.2ns, which is more than enough to cover a coarse TDC bin of about ±100ps. The slew rate is adjustable between 1ns and 7ns.

Latch and Sampling Flip-Flop

The latch is comprised of a cascade of the arbiter and an SR-latch. The SR-latch is included to help reduce metastability problems. A standard TSPC flip-flop implementation stores the output bits that come from the arbiter/SR-latch combination, before they are fed to the 84:7 encoder. The arbiter schematic is shown in Figure 27.

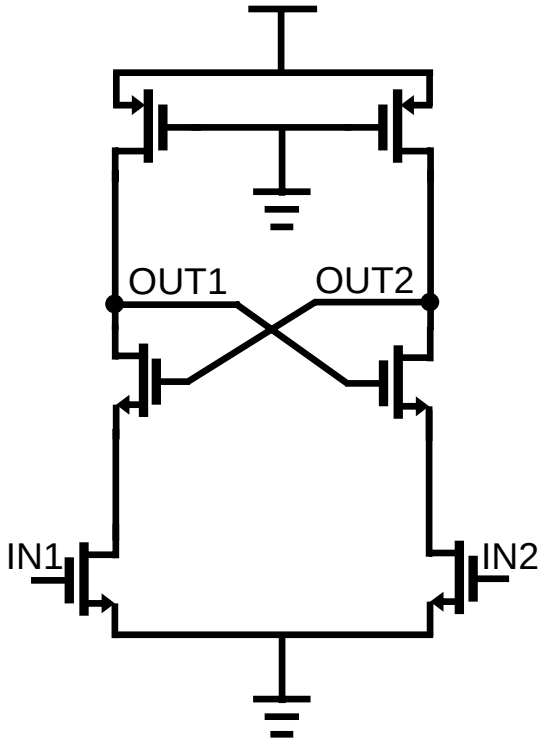


Figure 27. Arbiter schematic.

84:7 Encoder

This circuit converts the 84 output bits coming from the flip-flops into 7 binary-weighted output bits. Low speed operation makes a straightforward implementation possible. The 84 bits are handled in three groups of 28. The 28 bits are first divided into groups of 7 and converted into 3 bits using full-adders. Four 3-bit operands result, which are combined into two 4-bit operands using two 3-bit ripple carry adders. Now these 4-bit operands are combined using a single 4-bit adder to produce a 5-bit result. At this point, 28 output bits are represented as a 5-bit binary signal. Three such blocks are used to generate three 5-bit operands, which are combined using a three input 5-bit adder to finally produce a 7-bit word that represents the 84 output bits. Block diagrams for the 28:5 encoder and the 84:7 encoder are shown in Figs. 28 and 29 to clarify signal flow.

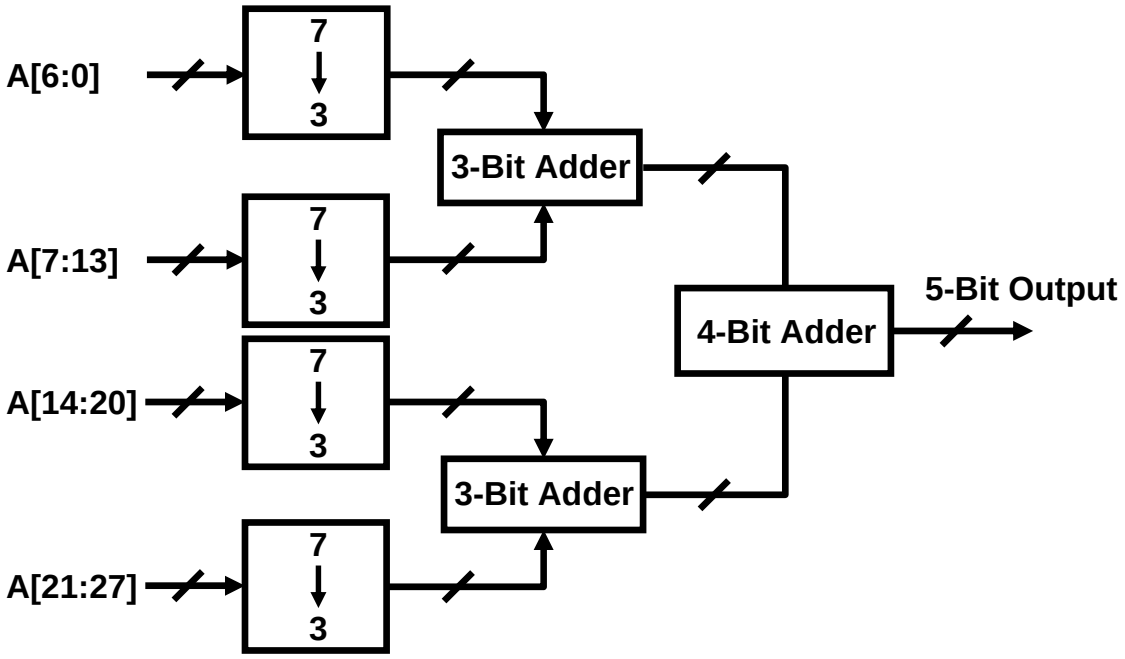


Figure 28. 28-to-5 encoder.

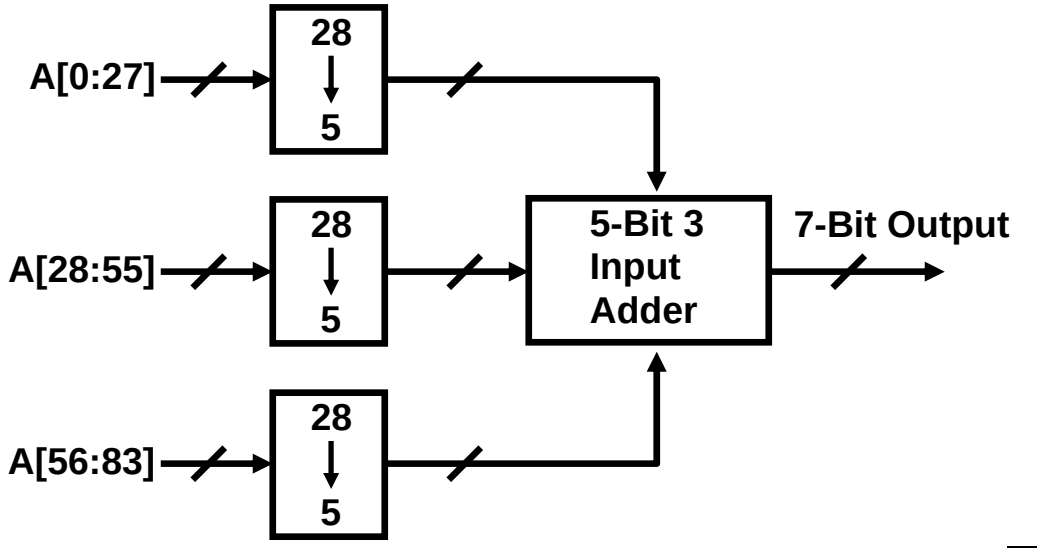


Figure 29. 84-to-7 encoder.

Master-Slave Flip-Flop

This configuration is used to generate the input signals to the slew and rise time control circuitry, as well as to generate the quadrature sampling edge that is used to capture the output bits in the sampling flip-flops. The low speed of operation enables using these cross-coupled NAND based latches to build a divide-by-2 circuit. The last stage of the divider in the PLL is implemented in the same way. The configuration is shown in Figure 30.

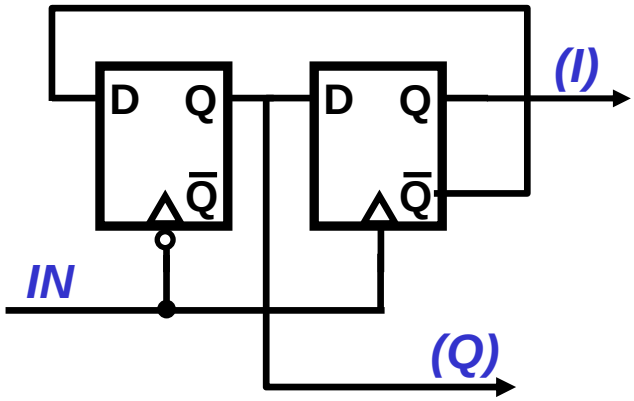


Figure 30. Master-slave divide-by-2 flip-flop.

Layout

The STDC layout is shown below in Figure 31. Most of the implementation is digitally intensive and thus not very susceptible to corruption by noise. The most important matching consideration in this layout is that the routing delays of the two arbiter inputs need to be as similar as possible. If one of the inputs is delayed differently than the other, an offset error will be introduced into the measurement. To minimize this, matching layout techniques are employed and the arbiter inputs are routed very closely, which also reduces the effects of noise coupling.

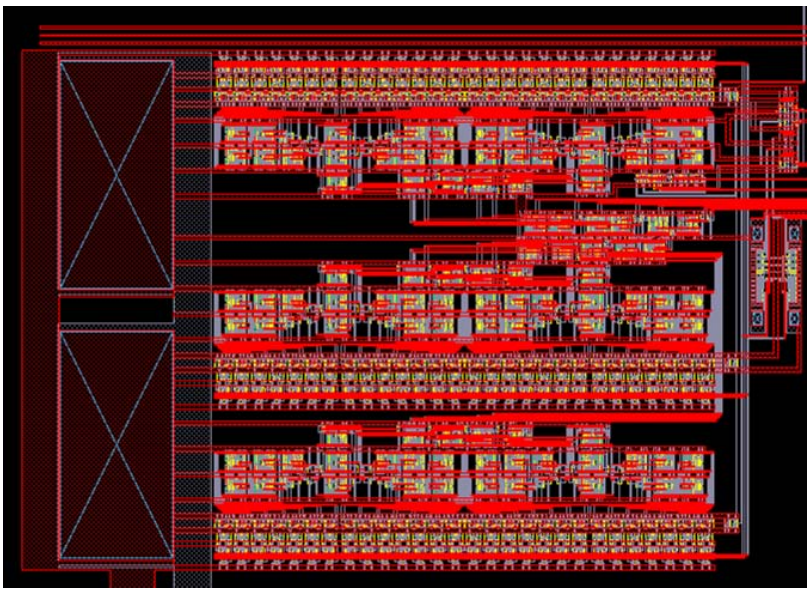


Figure 31. Layout of the STDC core

Separate buffer and chip supply rails are used, with extensive supply decoupling placed on both. The SOI process exhibits low capacitance between traces and the bulk, which was partly the reason why the test chip from last year has supply noisy problems [16]. The core die area is approximately 1150µm x 1700µm. A 2-to-1 multiplexer switches between an external stimulus or the PLL reference and the DCAO divided output to be able to test the circuit under both configurations.

Simulations

MATLAB simulation results with different input voltage offset distributions and different input signal rise times were presented in the February meeting [16]. Figure 32 shows the results of full transistor level simulations of the system in Spectre. Three cases are presented, one with the lowest expected offset amount of 20mV 1-σ and the others with the highest expected value of 40mV 1-σ tested for two different rise times. The offsets are introduced to the latches through a brute force method of including 84 voltage sources before the latches, whose values generate the desired offset characteristics. As seen in the plots the dynamic range for the 20mV case is much less than that in the 40mV case. The effect of the changing rise time on the dynamic range can also be observed.

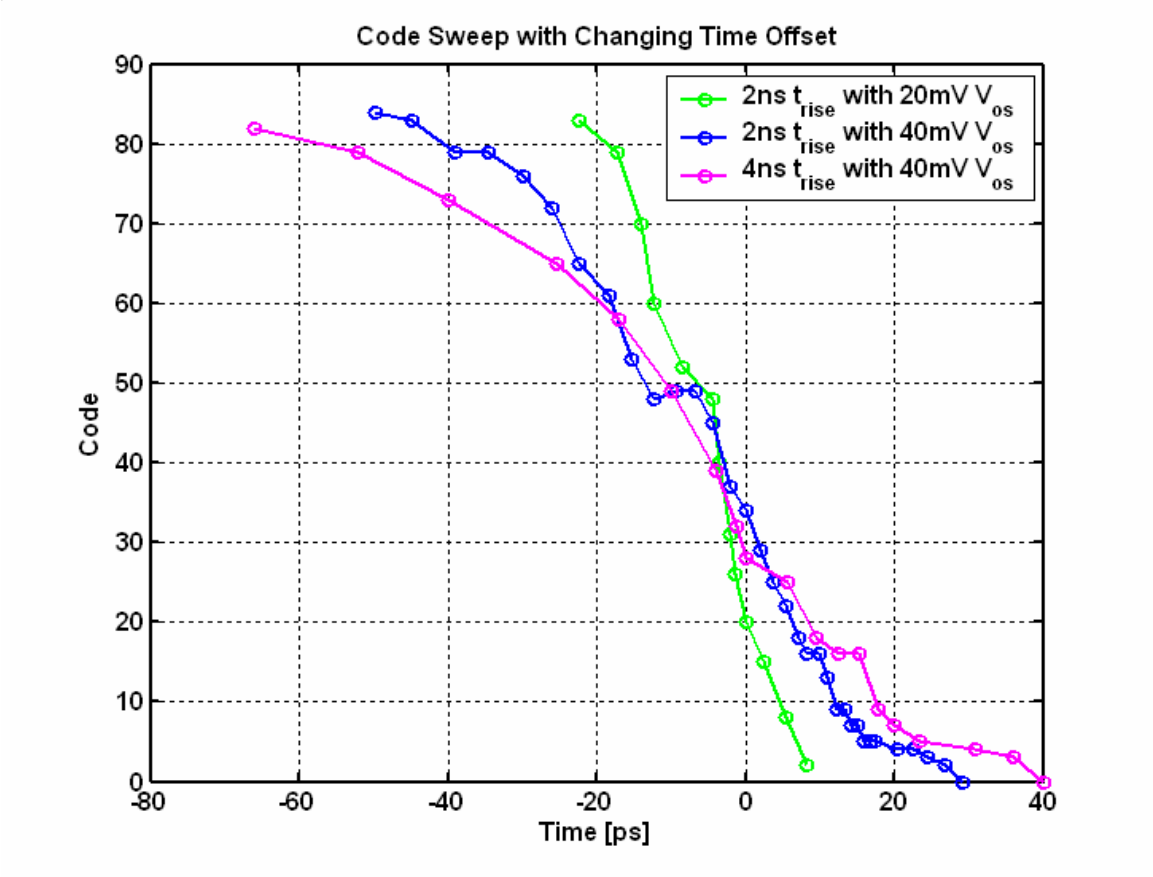


Figure 32. Transistor level simulation results for different rise times in Spectre.

Test chips

Layouts are shown in the above section for the test chip that has been taped out in the Honeywell 0.35µm SOI CMOS process. The test chip includes a previously designed analog PLL and the new DPLL for comparison. Also included is the statistical time-to-digital converter.

Other Results

Technology Transfer/Intellectual Property

The first test chip has been provided to Honeywell for evaluation of the PLL design in their application. No intellectual property at this time.

Publications Resulting from Research

M. Brownlee, P. K. Hanumolu, U. Moon, and K. Mayaram, "The effect of power supply noise on ring oscillator phase noise," *Proc. NEWCAS 2004*, pp. 225-228, June 2004.

Nemmani, M. Vandepas, K. Ok, K. Mayaram, and U. Moon, "Design techniques for radiation hardened phase locked loops," *Mil. Aero. Prog. Logic Dev. (MAPLD) Int. Conf.*, to appear, 2005.

M. Vandepas, K. Ok, A. Nemmani, K. Mayaram, and U. Moon, "Characterization of 1.2GHz phase locked loops and voltage controlled oscillators in a total dose radiation environment," *Mil. Aero. Prog. Logic Dev. (MAPLD) Int. Conf.*, to appear, 2005.

Benefits to Commercial Sector

A systematic study of SOI specific issues has led to a better understanding of the best use of SOI CMOS for PLL design. The resulting knowledge base of radiation/noise tolerant PLL architectures, circuit techniques, and self-calibration methods will facilitate implementations of PLLs in SOI CMOS processes. These designs could be easily migrated to a radiation-hard SOI process for additional radiation hardening. In addition, all digital PLL designs lays the foundation for radiation hard PLLs in standard CMOS technologies.

References

[1] B. Razavi, Editor, Monolithic Phase-Locked Loops and Clock Recovery Circuits, IEEE Press, 1996.
[2] T. Toifl and P. Moreira, "A radiation-hard 80 MHz phase locked loop for clock and data recovery," Proc. 1999 ISCAS, pp. 524 –527, 1999.
[3] G. Lyons, G. Wu, T. Mellissinos, J. Cable, "A high performance rad hard 2-3 GHz integer N CMOS phase lock loop," Radiation Effects Data Workshop, pp. 41-45 1999.
[4] L. Dayaratna, S. S. Seehra, A. Bogorad, L. G. Ramos, "Single event upset characteristics of some digital integrated frequency synthesizers," Radiation Effects Data Workshop, pp. 46-52 1999.
[5] J. P. Eckhardt and P. D. Muench, "A SOI specific PLL for 1GHz Microprocessors in 0.25µm 1.8V CMOS," 1999 IEEE ISSCC, pp. 436-437, Feb. 1999.
[6] J. Lin, B. Haroun, T. Foo, J.-S. Wang, B. Helmick, S. Randall, T. Mayhugh, C. Barr, and J. Kirkpatrick, "A PVT tolerant 0.18MHz to 600MHz self-calibrated digital PLL in 90nm CMOS process," in ISSCC Dig. Tech. Papers, Feb. 2004, pp. 488-489.
[7] R. B. Staszewski, D. Leipold, C.-M. Hung, and P. T. Balsara, "A first digitally-controlled oscillator in a deep-submicron CMOS process for multi-Ghz wireless applications," in Proc. 2003 IEEE Radio Frequency Integrated Circuits (RFIC) Symp., June 2003, pp. 81-84.
[8] M. Dentan, "Radiation effects on electronic components and circuits," European Organization for Nuclear Research CERN Training, April 2000.
[9] G. M. Anelli, "Conception et characterisation de circuits integres resistants aux radiations pour les detecteurs de particules du LHC en technologies CMOS submicroniques profondes," Ph. D. Thesis, Institut National Polythechnique Grenoble, Dec. 2000.

[10] R. C. Lacoe, J. V. Osborn, R. Koga, S. Brown, and D. C. Mayer, “Application of hardness-by-design methodology to radiation-tolerant ASIC technologies,” IEEE Trans. Nuc. Sci. vol. 47, pp. 2334-2341, Dec. 2000.
[11] W. J. Snoeys, T. A. P. Gutierrez, G. Anelli, “A new NMOS layout structure for radiation tolerance,” IEEE Trans. Nuc. Sci. vol. 49, pp. 1829-1833, Aug. 2002.
[12] W. B. Wilson, U. Moon, K. R. Lakshmikumar, and L. Dai, “A CMOS self-calibrating frequency synthesizer,” IEEE J. Solid-State Circuits, pp. 1437-1444, Oct. 2000.
[13] J. Lin, B. Haroun, T. Foo, J.-S. Wang, B. Helmick, S. Randall, T. Mayhugh, C. Barr, and J. Kirkpatrick, “A PVT tolerant 0.18MHz to 600MHz self-calibrated digital PLL in 90nm CMOS process,” in ISSCC Dig. Tech. Papers, Feb. 2004, pp. 488–489.
[14] B. Razavi, Editor, Monolithic Phase-Locked Loops and Clock Recovery Circuits, IEEE Press, 1996.
[15] T. Toifl and P. Moreira, “A radiation-hard 80 MHz phase locked loop for clock and data recovery,” Proc. 1999 ISCAS, pp. 524 –527, 1999.
[16] G. Lyons, G. Wu, T. Mellissinos, J. Cable, “A high performance rad hard 2-3 GHz integer N CMOS phase lock loop,” Radiation Effects Data Workshop, pp. 41-45 1999.
[17] L. Dayaratna, S. S. Seehra, A. Bogorad, L. G. Ramos, “Single event upset characteristics of some digital integrated frequency synthesizers,” Radiation Effects Data Workshop, pp. 46-52 1999.
[18] J. P. Eckhardt and P. D. Muench, “A SOI specific PLL for 1GHz Microprocessors in 0.25μm 1.8V CMOS,” 1999 IEEE ISSCC, pp. 436-437, Feb. 1999.

PROJECT 11

LOW TEMPERATURE RF CHARACTERIZATION AND DESIGN OF MOI5 SOI CMOS CIRCUITS AND DEVICES

Profs. Mohamed A. Osman and Deuk Heo (Washington State University)
with Andy Peczalski (Honeywell)

RESEARCH TIME PERIOD: One year
RESEARCH FOCUS: AFRL Task Areas 2 and 5: Standard Cell/Topologies in Radiation-Hardened SOI and Predictive Radiation Effects Model.

Figures and Tables

Abstract

This project characterized an MOI5 SOI CMOS process at low temperatures using DC measurement results. Prototype circuits will be designed and demonstrated using the measured model parameters. These include: (1) Focal plane readout (2) Analog signal transmission out of low temperature environment.

The goals of the project included low temperature characterization and design of a readout block of infrared image sensor for operation at 77K, RF and DC characterization of SOI CMOS devices and components at 77K, develop the models required for circuit design in collaboration with the group at UW. These include focal plane readout and signal transmission out of the Dewar. Figure 1 shows the block diagram of a typical IR image sensor [2]. Rather than repeating the characterization of the process at low temperatures, which has already been done by a group at JPL and Honeywell, we focused on analog signal transmission to match the funding level.

Project Description

SOI CMOS is the technology of choice for radiation-hard, low power and hostile environment applications. This is especially true for space and low temperature applications where on-board electronics have to survive temperatures as low as 77K. An important application of low temperature semiconductor electronics is processing of signals from infrared detector arrays. The most sensitive infrared detectors must be operated cold in order to achieve the desired sensitivity by reducing thermally generated noise and parasitic currents [1]. However, long wires between the detectors and warm electronics could cause capacitive loading and electromagnetic interference. Another requirement for any system where part of the electronics operates at low temperature is interfacing to the electronics that remains at room temperature. Special techniques need to be used that can efficiently transfer the high speed or high frequency signals to room temperature electronics, but do not transfer heat.

The goals of the project included low temperature characterization and design of a readout block of infrared image sensor for operation at 77K, RF and DC characterization of SOI CMOS devices and

components at 77K, develop the models required for circuit design in collaboration with the group at UW. These include focal plane readout and signal transmission out of the Dewar. Figure 1 shows the block diagram of a typical IR image sensor [2]. Rather than repeating the characterization of the process at low temperatures, which has already been done by a group at JPL and Honeywell, we focused on analog signal transmission to match the funding level.

As can be seen in Figure 1, in a typical focal plane readout circuit, the analog column readout signal after passing through the sample and hold circuit, converts to digital data and can be sent in parallel or serial [2]. Although, using digital communication protocols makes the signal transmission immune to noise, it requires an analog to digital converter in the low temperature part. High speed sampling time A/D consumes significant amount of power compared to other electronic circuitry, while operating in the low temperature environment. In low power applications, the power budget is very tight and any power that is dissipated within the Dewar (at 77K) has to be effectively multiplied by at least factor of 10, which represents efficiency of the cooling system. Consequently, the best approach is to keep the ADC off chip, which makes it necessary to employ a communication link that would handle analog signal with at least 8-bit resolution and can transfer the signal at a maximum required speed of 100 frames per second for an array of 512X512. This requires an approximate settling time of at most 35 nanoseconds for the whole analog signal transmission circuitry. Therefore a part of the project involves review of techniques for analog transmission over wires such as twisted pair and characterization of channels for analog signal transmission up to 1 GHz.

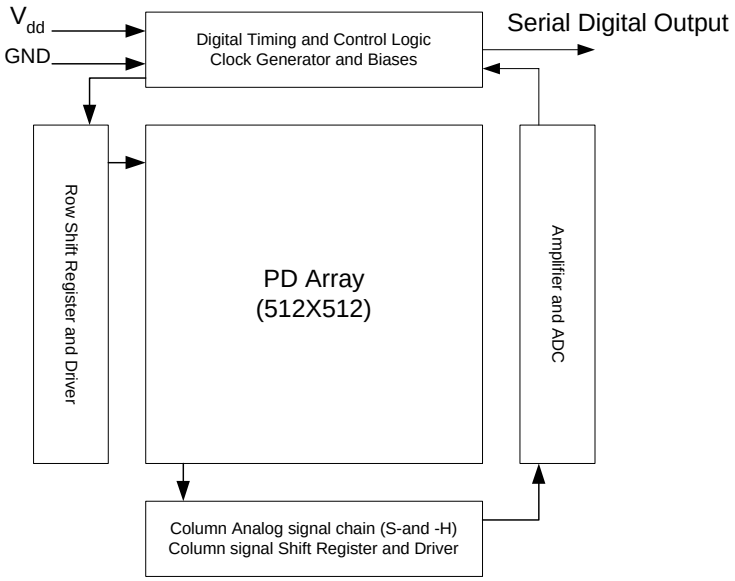


Figure 1: Typical sensor array Block Diagram

Current loop method for analog signal transmission was considered. In this method, current is the same everywhere in a series transmission loop and none of the current will be lost due to the line resistance or poor connections. By using a floating load, a common mode rejection technique at the receiver can be used to reduce the induced noise. Since using coaxial cable is not an option, twisted wire lines were investigated and our measurement showed that one-meter of CAT-5e cable has 150MHz 3dB bandwidth. This makes the cable suitable for the required speed of operation.

Research Results and Discussion

Low temperature SOI device Models and characterization

The low temperature limit of the MOI5 SOI device models under development by Prof. Bruce Darling's group at University of Washington is –65C (208). We have collaborated with them to extend

the model to 77K. This amounted to calibrating their model with the low temperature published on MOI5 SOI process [3]. This was completed for the NMOS model. Low temperature PMOS devices models and verification of model compatibility with Spectre has been a problem and therefore the models could not work with CADENCE. In order to proceed with our low temperature circuit designs and simulations, we used the same models available at Honeywell and modified the temperature parameter only, which does not provide accurate prediction of circuit parameters. Figure 2 shows the threshold voltage and mobility variation versus temperature for nMOSFET and pMOSFET SOI devices [3]. Note that the electrons mobility significantly increases at 77K comparing with 273K.

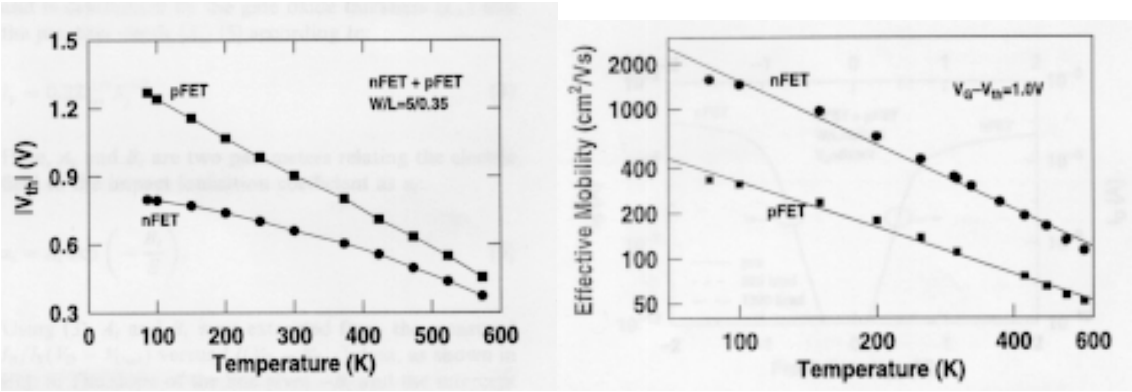


Figure 2: Threshold voltage and Mobility dependence on Temperature [3]

The I_{ds}-V_{ds} characteristic of MOI5 SOI NMOS device is shown in Figure 3. At low temperatures, the current increases due to mobility increase. Measurements of small signal and noise parameters are required for accurate RF models. As a result, good device model suitable for simulation at 77K is required for any future design of low temperature circuits.

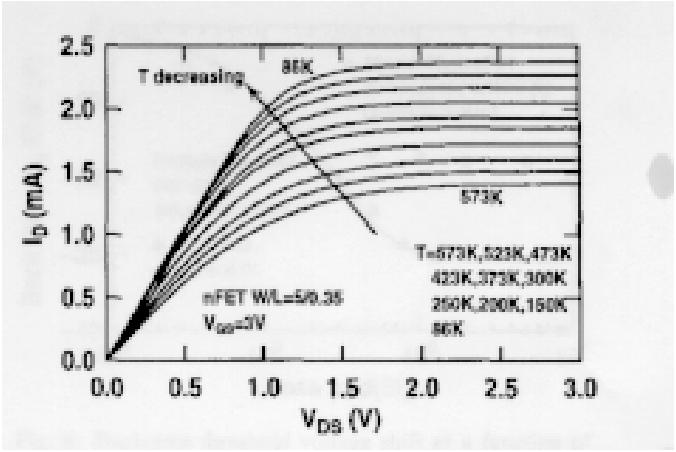


Figure 3: Temperature dependence of I_{ds}-V_{ds} Characteristics of MOI5 SOI NMOS device [3]

Analog signal transmission/ Circuit topology

Different analog signal transmission topologies were reviewed and a current loop topology was chosen. Wireless communication or using signal power lines and a method of up-converting the signal were also examined. Unfortunately, these methods require a fast phase lock loop system with the settling time of less than 35nSec. Our literature search showed that fastest designed PLLs have settling time of several hundred nanoseconds, making these methods unrealizable. Consequently, a separate line for transmitting signal was considered. Frequency response measurement on one meter of a twisted wire line was performed and 150MHz measurement bandwidth was obtained. For connecting low temperature electronics to the room temperature electronics, using a coaxial cable is not an option due to the high thermal conductivity of the metal and large area of the shield cover. There are three general methods for transmitting an analog signal using twisted pair wires [4]:

- *Differential Voltage:*

Shown in Figure 4-a, analog voltage is transmitted and the receiver detects the differential voltage. Using this method, the common mode noise introduced in the transmission line can be reduced. But the signal level is still sensitive to the resistance of the wire, interconnections and any ground voltage difference.

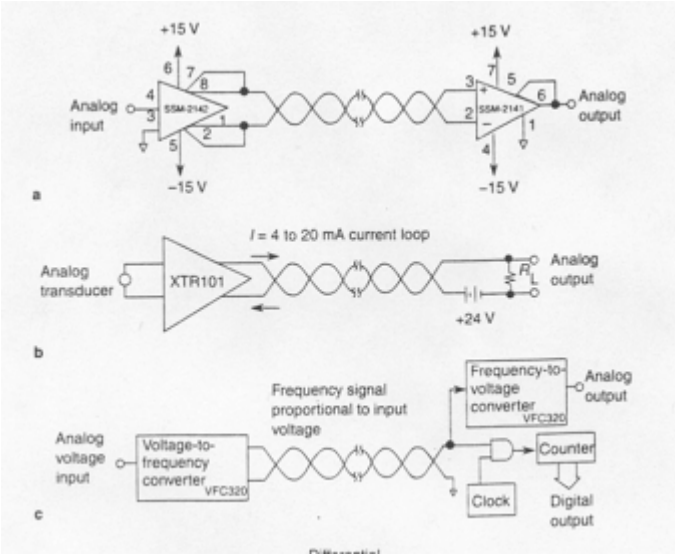


Figure 4: Analog Signal transmission [4]

- *Converting Voltage to Current:*

Illustrated in Figure 4-b, voltage signal can be converted to current and send it through twisted wires to a long distance [5]. In this method current is the same everywhere in a series transmission loop and none of the current will be lost due to the line resistance or poor connections. By using a floating load, a common mode rejection technique at the receiver can be used to reduce the induced noise (Figure 5). As can be seen in Figure 5, the non-inverting configuration buffers the voltage source, preventing it from loading. An offset voltage can be used to differentiate between “no signal” and “zero signal”. Figure 5 shows the floating voltage to

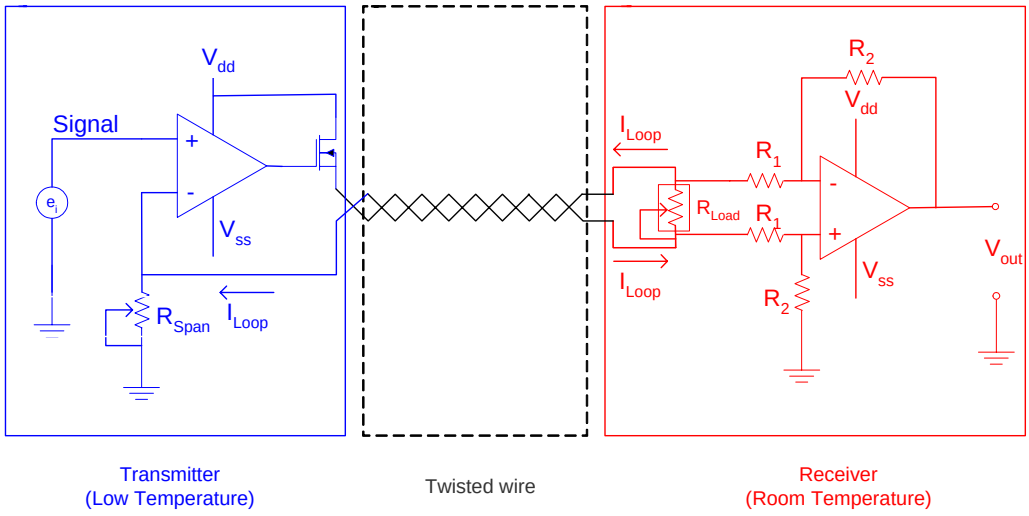


Figure 5: Converting voltage to current

current converter. By using an instrumentation amplifier at the load, any common mode noise picked up on both lines during transmission can be rejected. Differential nature of floating current transmission allows the use of an instrumentation amplifier's high common mode rejection ratio to reduce noise coupled into the loop. This method has been widely used in industry to transmit analog and digital signals.

- *Converting Voltage to Frequency:*

In some applications, using the above method, the transmission loop noise can't be adequately reduced. To provide high noise immunity, analog voltage from the sensor and signal conditioner is converted to frequency (Figure 4-c). At the receiver end, by using a frequency to voltage converter, the original analog signal can be recovered. Shown in Figure 6 is the block diagram of PLL. One factor in PLL design is the lock time or an indication of how fast

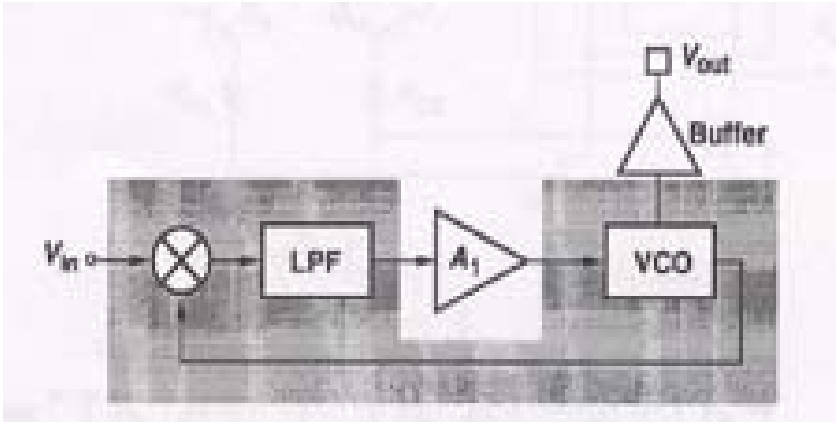


Figure 6: PLL Block Diagram

a new frequency will be stabilized. Lock time required in typical RF systems vary from a few tens of milliseconds to a few tens of microseconds [6]. Figure 7 shows a typical response of a PLL operating at 2GHz [7].

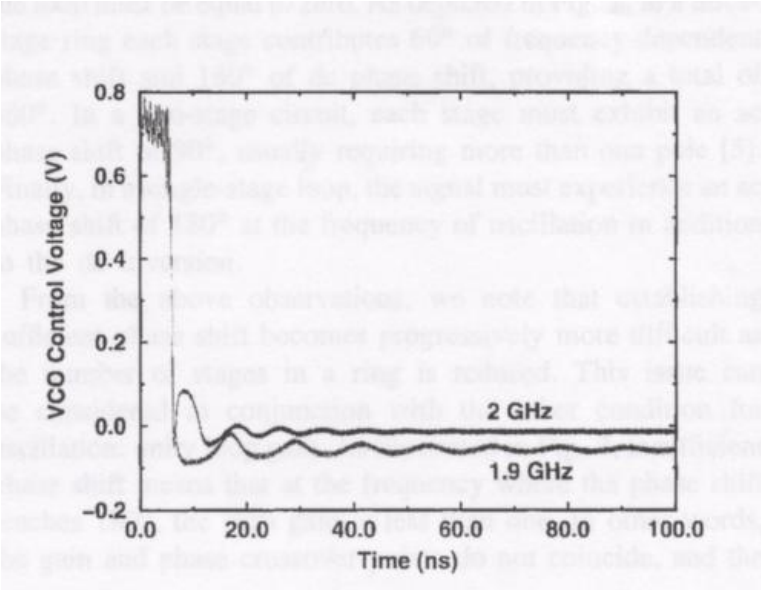


Figure 7: Typical PLL response time

For the 512X512 image array operating at maximum 100 frames per second, the total settling time of transmit circuitry, wire line and receiver circuitry should be less than 35nSec, which makes the above method unsuitable.

Transmission Channel Characterization

Figure 8A shows some of the early work on the practical frequency range using twisted pair which shows an upper limit ranging from to 100KHz to at most 10 MHz [4] which is well below the desired bandwidth for this project. However, the length and size of cables were not

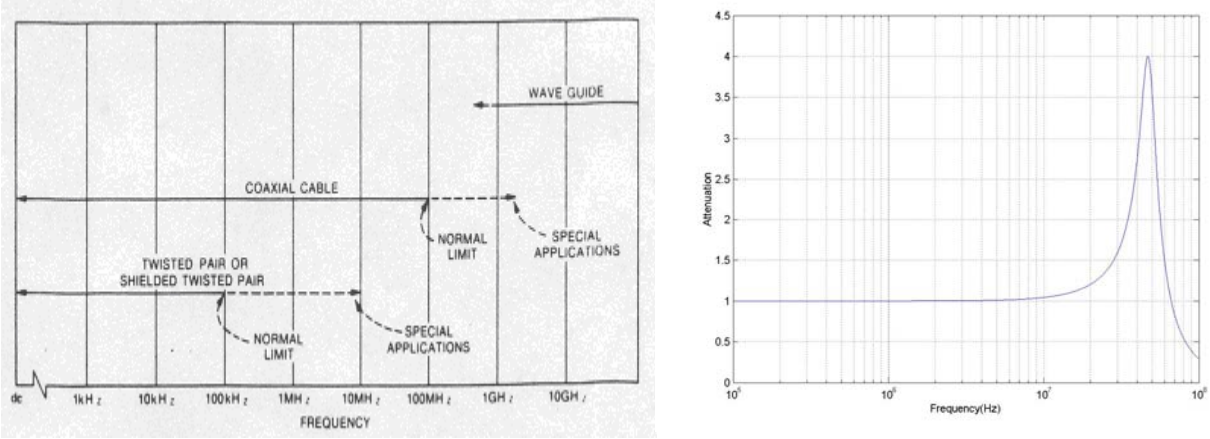


Figure 8: A) Useful frequency range for various transmission lines [4] B) Two-wire line attenuation

mentioned. Consequently, attenuation of short length of different wires was measured using HP85046A network analyzer. Our measurement and simulation on one meter of two-wire line showed less than 30MHz 3dB bandwidth (Figure8B). In order to measure the bandwidth of twisted wire line, one-meter of CAT-5e cable was chosen. As can be seen from Figure 9, the 3dB frequency is about 150MHz, which makes it possible to use up to one meter of the cable for analog signal transmission at the above speed.

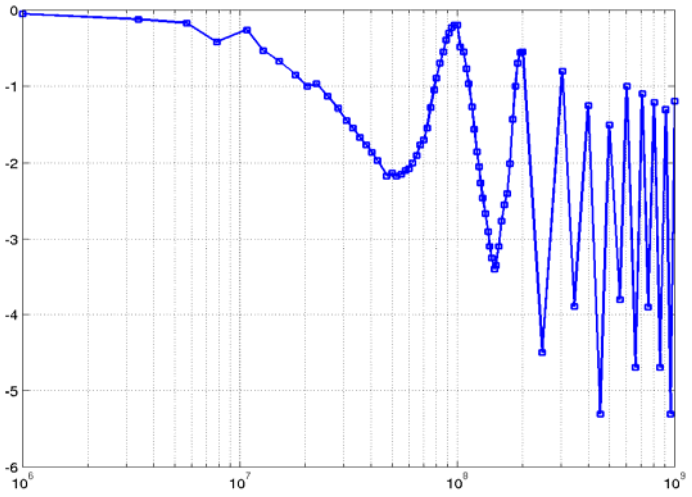


Figure 9: Twisted wire line attenuation

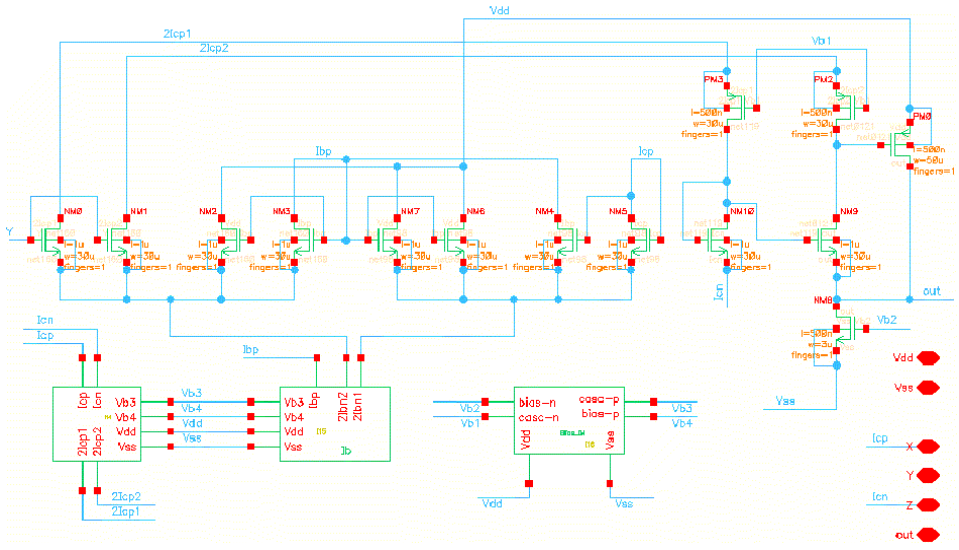


Figure 10: Schematic of the simulated CFOA

Current Feedback Amplifier Design

A bandwidth of 150 to 200 MHz is required for the receiver and transmitter op-amps while the transmitter op-amp characteristic can be completely different from the receiver side. This may make the receiver and transmitter circuit topologies different especially when we notice that the transmitter is operating in the low temperature environments. For the receiver side, we considered CMOS current feedback op-amp, which is suitable for high frequency applications. The current feedback op-amp (CFOA) topology can achieve large slew rate and their closed loop bandwidth remains virtually constant as closed loop gain is increased [8]. These make CFOA better than classical voltage mode operational amplifiers, which are limited by a constant gain bandwidth product. The schematic of CFOA is shown in Figure 10, [9]. The simulated result for the amplifier is shown in Table 1.

Table 1- Amplifier Specification

Parameter	Condition	Value
3dB Bandwidth	Gain=2	**228MHz**
	Gain=5	**142MHz**
	Gain=10	**92MHz**
Power	530μA, 5V	**2.7mW**
CMRR	Gain=5,	**73dB**
Linearity	Gain=5,	**0.04%**
Settling	Gain=5,	**25nSec**

Test Chip

The entire circuit was laid out based on MOI5 design rule. Since the circuit was supposed to operate at high-speed, parasitic capacitances could influence the circuit performance. For this reason, these capacitances were extracted and the entire circuit including the parasitic was simulated. The important signal routes that parasitic had the strongest influence were identified and the layout design were several times modified to have the smallest parasitic. Figure 11 shows the layout of the transmitter side. The receiver side layout was identical in most of the parts to the transmitter. The whole chip layout was submitted on May 7 for the fabrication.

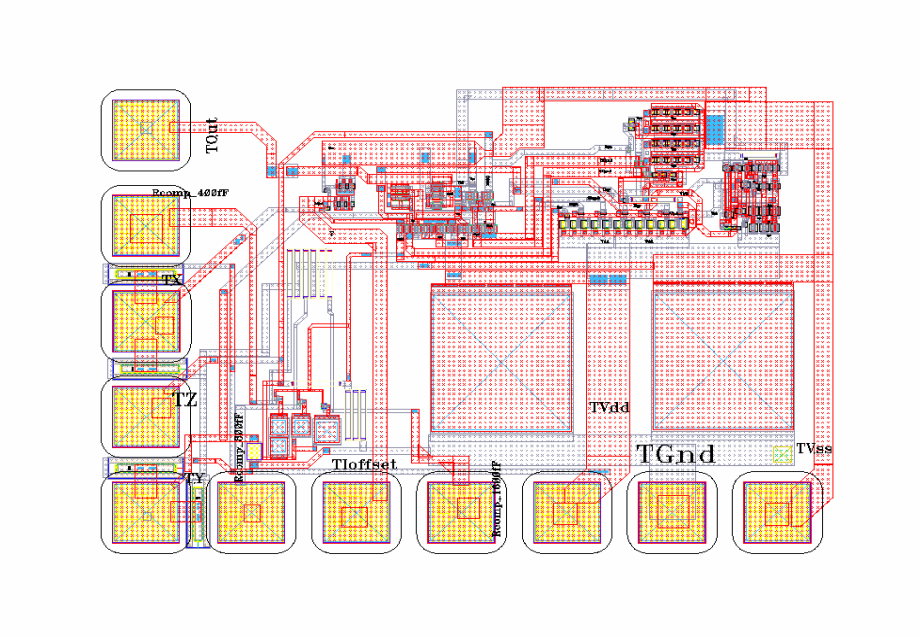
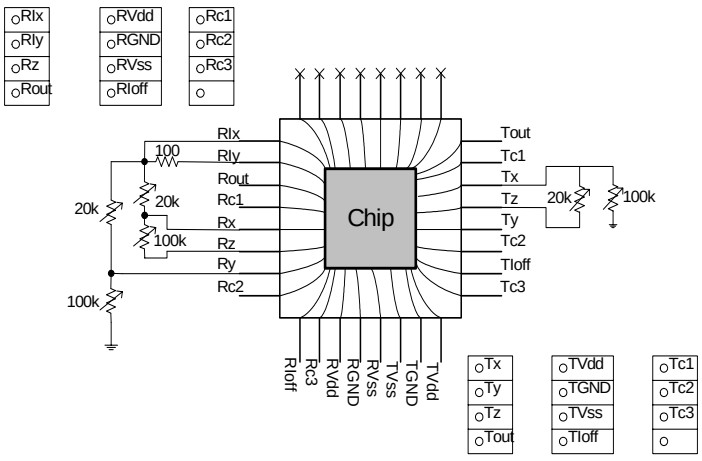


Figure 11: Transmitter layout

The delivery date of the fabricated chip has been delayed by Honeywell from June 2004 to September 2004 and as result the circuit's performance was not characterized. The details of the pad assignments and the test board designs are included in the appendix.

Test Board Layout:



Other Results

Technology Transfer/Intellectual Property

Not at this time.

Publications Resulting from Research

Not at this time.

Benefits to Commercial Sector

The model parameters will help designing circuits near 77K. Prototype circuits, if successful, will lead to ultra low power image sensor designs.

References

[1] R.K. Kirschman, Low temperature electronics, *Circuits and Devices*, 1990.
[2] K. Cho, A. I. Krymski and E.R. Fossum, A 1.5V 550 W 176X144 autonomous CMOS active pixel image sensor, *IEEE Trans. Electron Devices*, Vol. 50, pp. 96-105, Jan. 2003.
[3] Y. Li, G. Niu, J.D. Cressler, J. Patel, S.T. Liu, R.A. Reed, M.M. Mojarradi, B.J. Blalock, The operation of 0.35 m partially depleted SOI CMOS technology in extreme environments, *Solid-State Electronics*, 47, 2003.
[4] K.R. Fowler, Electronic instrument design, Oxford University Press, 1996.
[5] J.M. Jacob, Industrial control electronics, Prentice-Hall International Edition, 1989.
[6] B. Razavi, RF Microelectronics, Prentice Hall, 1998.
[7] A 2GHz, 1.6mW Phase-locked loop, *IEEE Journal of Solid State Circuits*, Vol. 32(5) 1997.
[8] J. Mahattanakul,C. Toumazou, A Theoretical Study of Stability of High Frequency Current Feedback Op-amp Integrators, *IEEE Trans. on Circuit and Systems-I*, Vol. 43(1), Jan. 1996.
[9] A.M. Ismail, A.M. Soliman, Novel CMOS Current Feedback Opamp Suitable for High Frequency Applications, *IEEE Trans. on Circuit and Systems-I*, Vol. 47(6), June. 2000.

PROJECT 12

RECONFIGURABLE INPUT/OUTPUT FOR RADIATION ENVIRONMENTS (A Demonstration Project)

Andy Peczalski (Honeywell) with Profs. Adrian Leuciuc (SUNY), GaborTemes (OSU), Un-Ku Moon/Karti Mayaram (OSU), and Larry McMurchie/Carl Sechen (UW)

RESEARCH TIME PERIOD: Two years
RESEARCH FOCUS: AFRL Task Areas 1, 2, and 3: System Circuit Modeling for VLSI Circuit Implementation, Standard Cell/Topologies in Radiation-Hardened SOI, and Reconfigurable Mixed-Signal Electronics.

Figures and Tables

Abstract

We have developed a portable test environment to demonstrate the functionality and reconfigurability of the ASICs developed under AFRL program and potential for combining those chips as reconfigurable I/O and other functions relevant to AFRL mission. The test environment is compatible with Single Event Effects (SEE), transient dose and total dose radiation testing. Those features are directly supporting the major AFRL tasks: Standard Cell / Topologies in radiation-hard SOI and Reconfigurable mixed signal electronics. The first generation of the reconfigurable demonstration consists of Phase Locked Loop (PLL) and Delta Sigma Demodulator/Analog to Digital converter (other AFRL developed functional ASICs were not available at that time). Together with University of Washington we have also designed a new board that will enable demonstration of the radiation hard SRAM and reconfigurable digital/analog array when available.

Project Description

The major tasks of the project included designing the architecture for the reconfigurable I/O demonstration, designing the custom daughter boards compatible with the specific university ASICs, developing the imbedded and computer software and integrating the demonstration test bed. The reconfigurable I/O subsystem incorporates the necessary functions to perform conditioning and conversion of analog and discrete signals for a wide range of applications. This subsystem will be formed of blocks currently under development by 4 University groups: ADC (Adrian Leuciuc, SUNY), DAC (GaborTemes, OSU), programmable PLL (Un-Ku Moon and Karti Mayaram, OSU), and Reconfigurable

DSP (Larry McMurchie and Carl Sechen). The benefits of this subsystem are several. Its reconfigurable nature allows reuse in numerous aerospace systems, reducing development and integration time as well as cost. Reconfigurability may also allow in-orbit remote repair and upgrade as well as dynamic reconfigurability for mode and task agility. The examples of the reconfigurable functions of the I/O include the following:

Input	Output	Closed-Loop Control	Formatting/Processing
A/D	D/A	Servo/Pico-Servo	Compression
Discrete	Discrete	Steppers	Transformation
Serial	Serial	Linear/Wedge	DL/UL Formatting
Parallel	Parallel	Rotaries	Filters/Protocol
Formatted/Mux'd	Formatted/Mux'd	Propulsion Control	Waveform Generation/ Detection
Coded/Filtered	Coded/Filtered	Tracking	Targeting
			Template Processing

Research Results and Discussion

Architecture of the Reconfigurable I/O Demo

The reconfigurable I/O consists of the functional blocks under development by different CDADIC teams as shown in Figure 1.

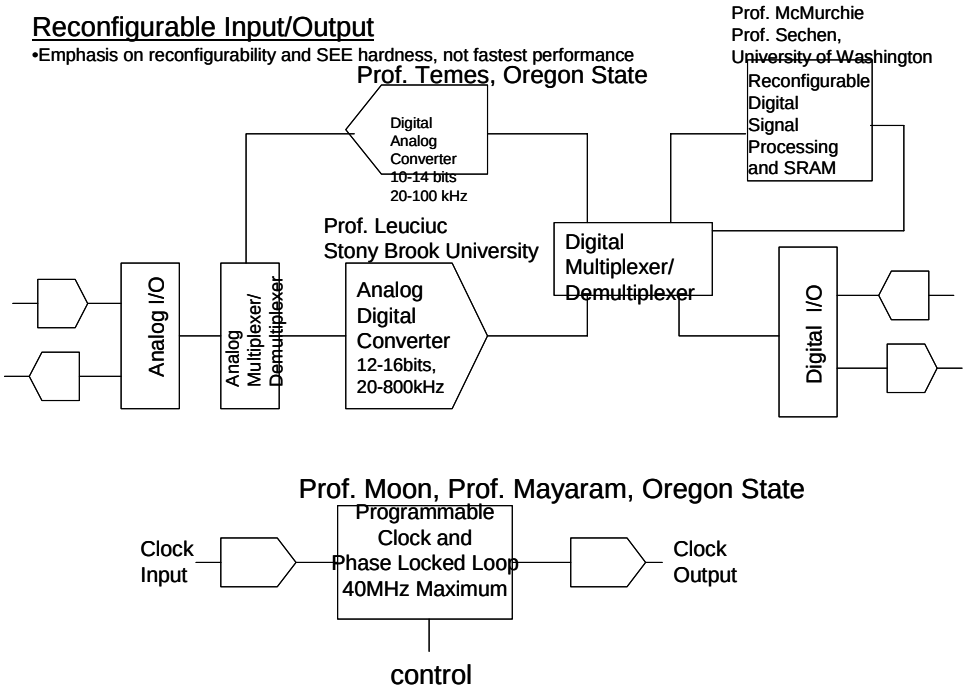


Figure 1. Partitioning of the reconfigurable I/O according to the functionality developed at different universities.

In view of the incremental nature of the university ASIC development we adopted a DSP board with the same functional features as the building blocks of the I/O. Therefore our demo can be tailored to any desired application even if the university ASIC are not available at the given time. The hardware and software of our demonstration test bed include:

Hardware

- COTS 32 bit DSP board with high speed pc connection
- Socketed COTS ADC, DAC, and Digital IO modules for DSP board
- Socketed custom daughter board with demo ASIC and support electronics
- JTAG DSP debugger
- WinXp based pc for display

Software (DSP Target)

- TI Code Composer Studio
- Innovative Integration Zuma Toolset: Target
- Xilinx ISE (optional)
- Code Composer Matlab Plug-in (optional)

Software (PC / Host)-Innovative-Integration Armada Component Set

- 20 MSamples/sec. continuous stream
- 64 MSamples/sec. snapshots to RAM
- Real time hardware running with Native C++
- MMX optimized Intel signal processing libraries
- C++ Development S/W for Data Acq/DSP
- Borland C++ Builder Support
- Comprehensive Toolset with Software Components for Data Acquisition, Analysis, Display and Recording (Windows2000/XP Compatible)

The full traveling demo of the reconfigurable I/O consists of a laptop, DSP board and custom ASIC board. The photograph of the traveling demo is shown in Figure 2.

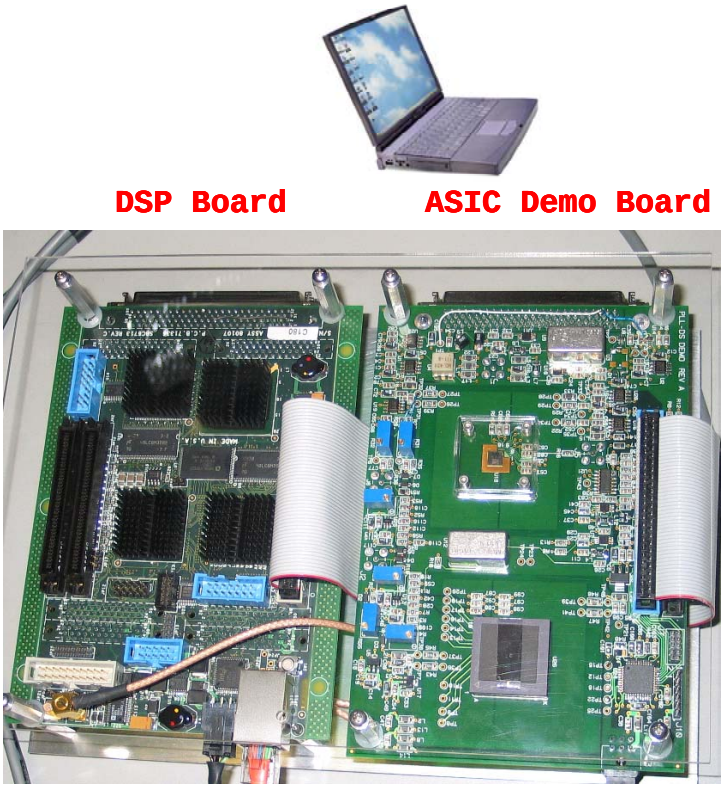


Figure 2. Photograph of the portable demonstration of the reconfigurable I/O.

The architecture of software that resides on the laptop and on the DSP board is shown in Figure 3.

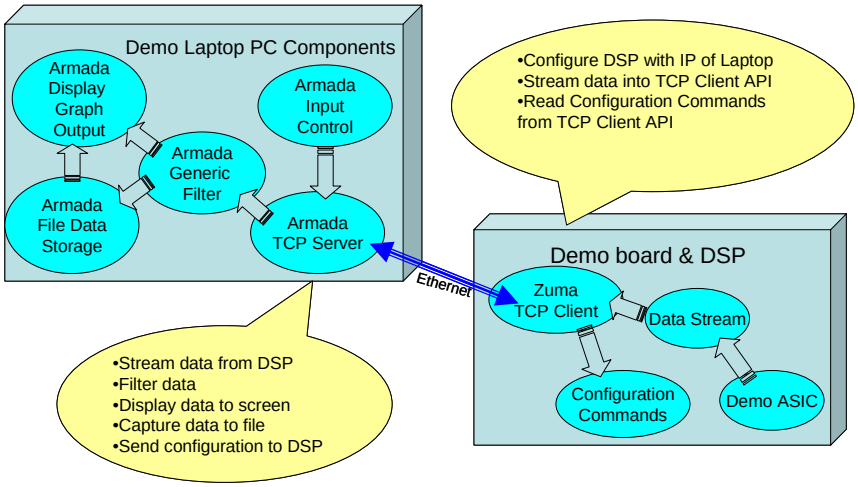


Figure 3. Software architecture for the reconfigurable I/O demo.

We have developed custom circuit daughter-boards to host the ASICs that can plug in the DSP mother boards. The first board houses the PLL and Demodulator chips to emphasize the integration trend of the reconfigurable I/O. The block diagram of the ADC and PLL custom board integrated with the DSP board and lap top is shown in Figure 4. The photograph of the custom board with the ASICs marked is shown in Figure 5.

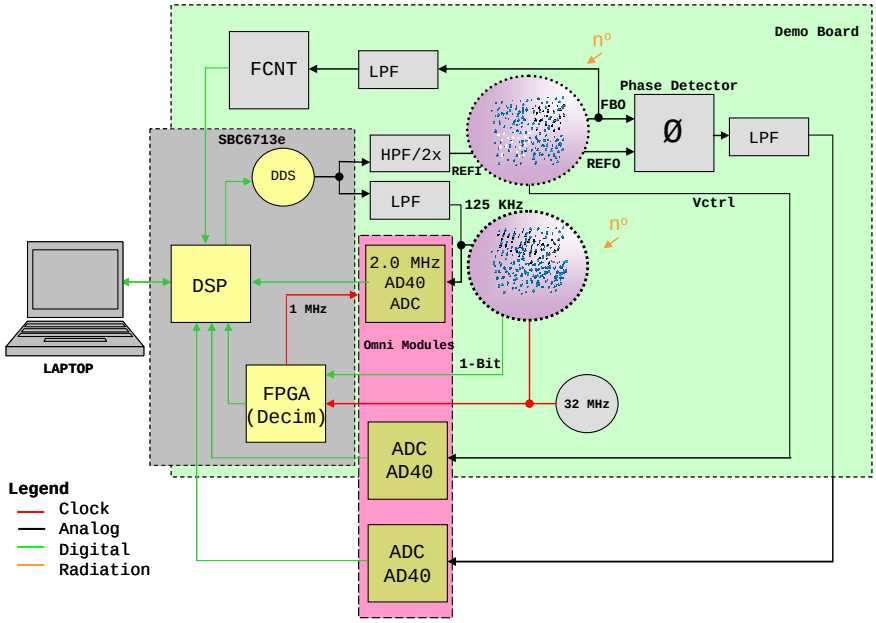


Figure 4. Block diagram of the laptop, DSP board and PLL/ADC board that corresponds to the photograph in Figure 2

However the present implementation of the PLL cannot work below 45 MHz and the present demodulator input frequency is 125 kHz. Therefore we are forced to show the functionality of the chips separately. The second board is intended for the rad-hard SRAM and processing array from University of Washington. This is a separate board since those chips are not available until fall. The radiation requirements were addressed by modified layout of the circuit board. Firstly we secured a sufficient unpopulated perimeter around the ASIC on the board to allow for the component free room for the radiation beam (see Figure 5).

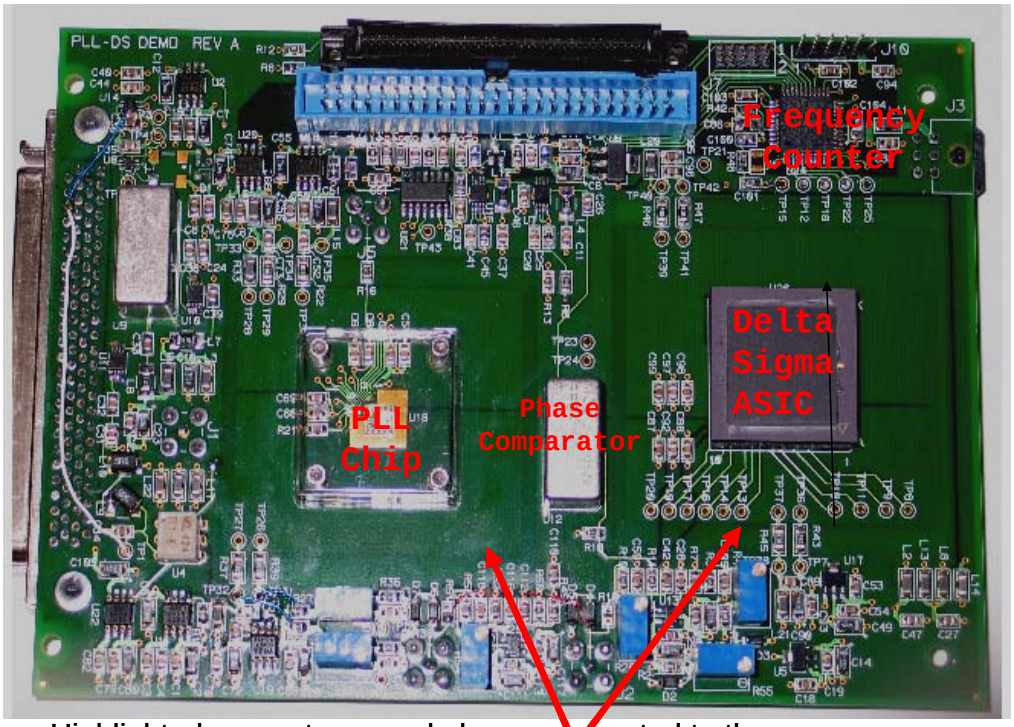
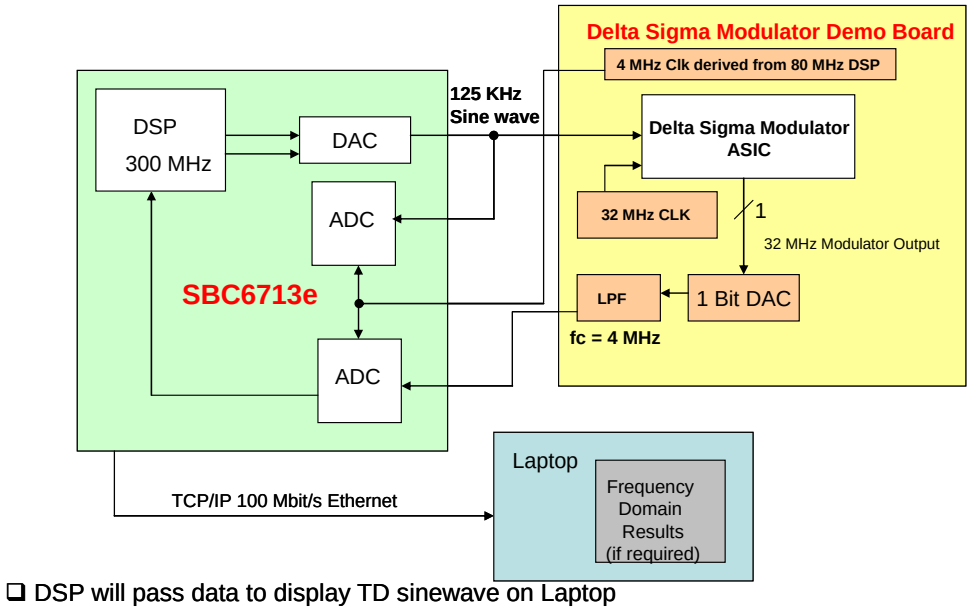


Figure 5. Custom PLL and ADC board with device-free periphery and individual ground planes for the radiation testing.

Secondly we separated the ground plane of the ASIC from the ground of the board by very small resistors. This arrangement allows to measure the radiation generated currents. Those individual demonstrations are described separately in the sections below.

Delta Sigma Demodulator and ADC

A fourth order, continuous time delta sigma modulator has been developed by Stony Brook University, New York. Together with a decimating and low pass filter the demodulator constitutes an analog to digital converter. As shown in Figure 6 we have implemented the decimating filter on the custom board with a one bit digital to analog converter and low pass filter. Therefore we demonstrated the full functionality of the ADC.



- DSP will pass data to display TD sinewave on Laptop
- DSP will pass data to display 1024 point Real FFT waveform on laptop

Figure 6. Demo architecture for the delta-sigma modulator ASIC

The graphic user interface for the ADC demonstration is shown in Figure 7. On the top screen we display the life input and output of the ADC. The input is the 125 kHz sinusoidal waveform. The output is the output of the ADC that has been converted to analog domain by the DAC on the DSP board. We have shown in real time demonstration that those two waveforms are identical thus verifying the functionality of the ADC. The digital output of the ADC is analyzed in the bottom window with a Fourier transform. We could therefore measure the power of the output frequency signal versus the power of the spurious outputs and verify the resolution of the ADC during life demonstration.

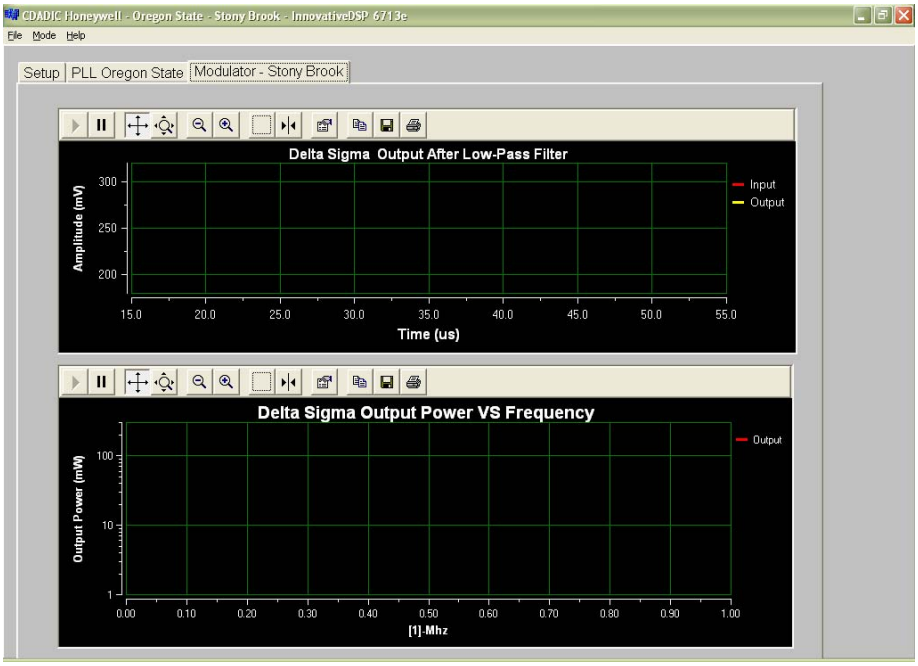


Figure 7. Graphic user interface for the ADC demonstration

Reconfigurable Phase Locked Loop

The reconfigurable PLL has been designed at Oregon State University with adjustable current of the charge pump that will affect the SEE and transient radiation sensitivity and recovery time. We also have the control over the divide ratio to generate different output frequency. Because of the frequency limitation of the DSP board we can only operate with the highest division factor. The block diagram of the PLL demo is shown in Figure 8.

We have demonstrated the functionality and reconfigurability of the PLL with the graphic user interface shown in Figure 9. The green button in the left upper corner indicates that the PLL is in lock and operating. the top life waveform is the output of the loop filter pin on the ASIC. The PLL is locked if the phase signal is steady. We also captured the phase difference between the frequency source and the loop signal with the phase comparator and the low pass filter on the custom board. We can also vary the reference signal frequency and measure the frequency of the divided output of the in-the-loop signal with on-board frequency counter. The frequencies of the reference and in-loop signal are displayed in the two windows at the top of Figure 9. The output frequency counter displays 0 when the PLL is out of lock.

We have demonstrated the reconfigurability of the PLL in two was: by changing the frequency divider in the loop from 1 to 16 and by changing the current in the charge pump to 12.5, 50, 100 and 200 micro Amps. Because of the maximum frequency limitation of the DSP and low divide ratios we achieved lock only for the ratio of 16. Therefore we could break the lock changing the divider to 1 and then recover the lock by programming the divide ratio back to 16. However, the PLL operated for all values of the charge pump current. We have demonstrated that the lower charge pump current slower the PLL is to recover the lock. The waveforms of the phase difference signal during the lock recovery for different current settings are shown in Figure 10.

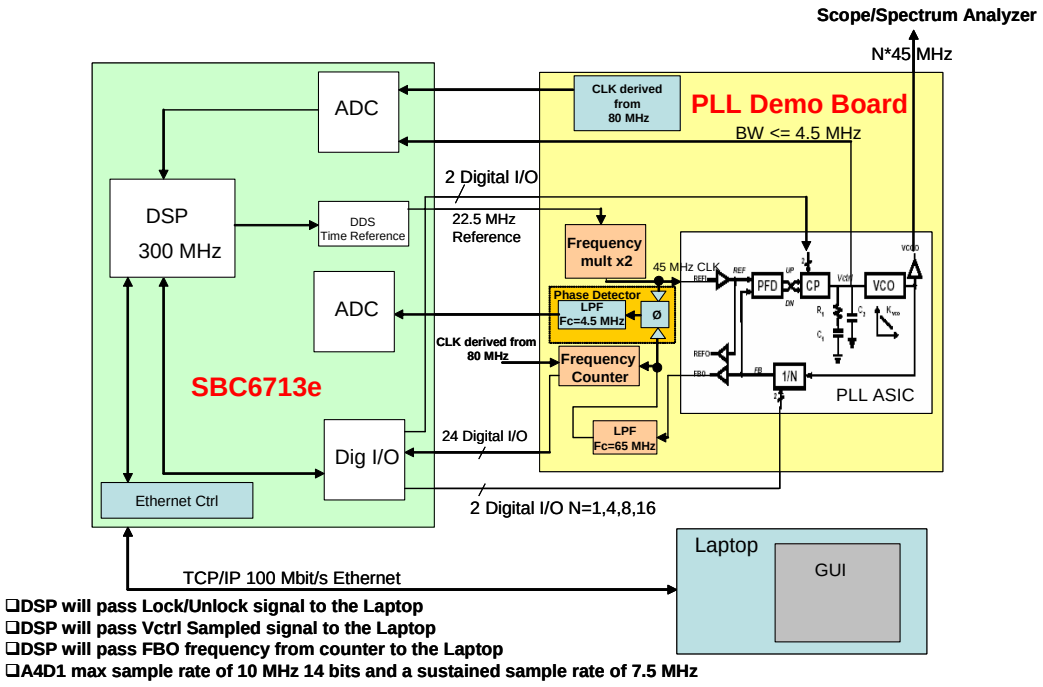


Figure 8. Block diagram of the PLL demo demonstration.

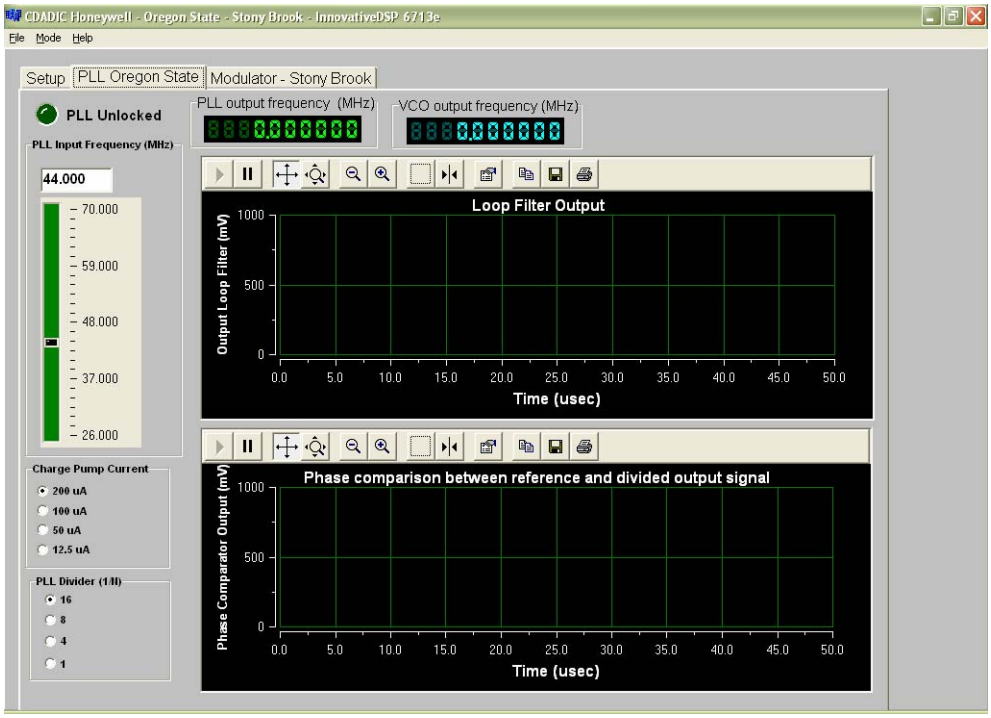


Figure 9. Graphic user interface for the PLL life demonstration

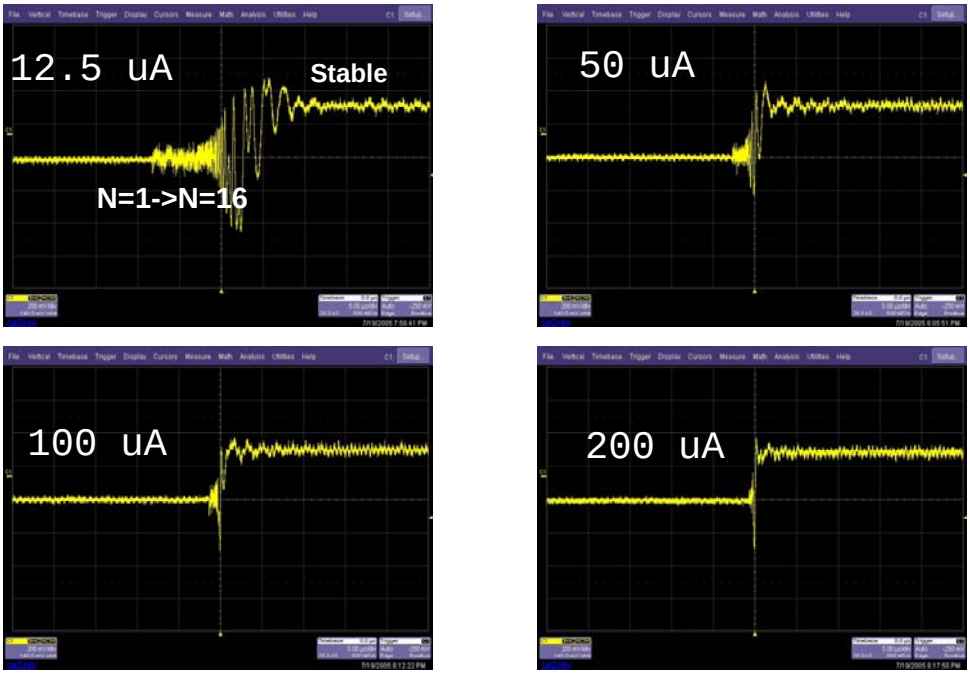


Figure 10. Transient waveforms of the phase detector of the PLL during reconfiguring the divider from 1 to 16 for the 4 different charge pump currents.

The effects of different charge pump current value on the recovery duration of the PPL are indicative of the radiation recovery characteristics. We expect that the PLL with higher charge pump values would be less sensitive to the transient radiation effect bur it would consume more power.

Radiation Hard Reconfigurable Processing Array and SRAM

In close cooperation with University of Washington we have designed and laid out the custom board for testing the reconfigurable processing array and SRAM. The reconfigurable processing array could be tested in two different modes of operation: as a 200 tap FIR filter and as a correlator. The block diagram of the FIR demo and correlator demo are shown in Figures 11 and 12 respectively.
The functionality of the FIR filter could be for the sensor signal conditioning or for the communication signal processing. The intention of the correlator function is to emulate the GPS receiver locking to the GPS satellite signal.

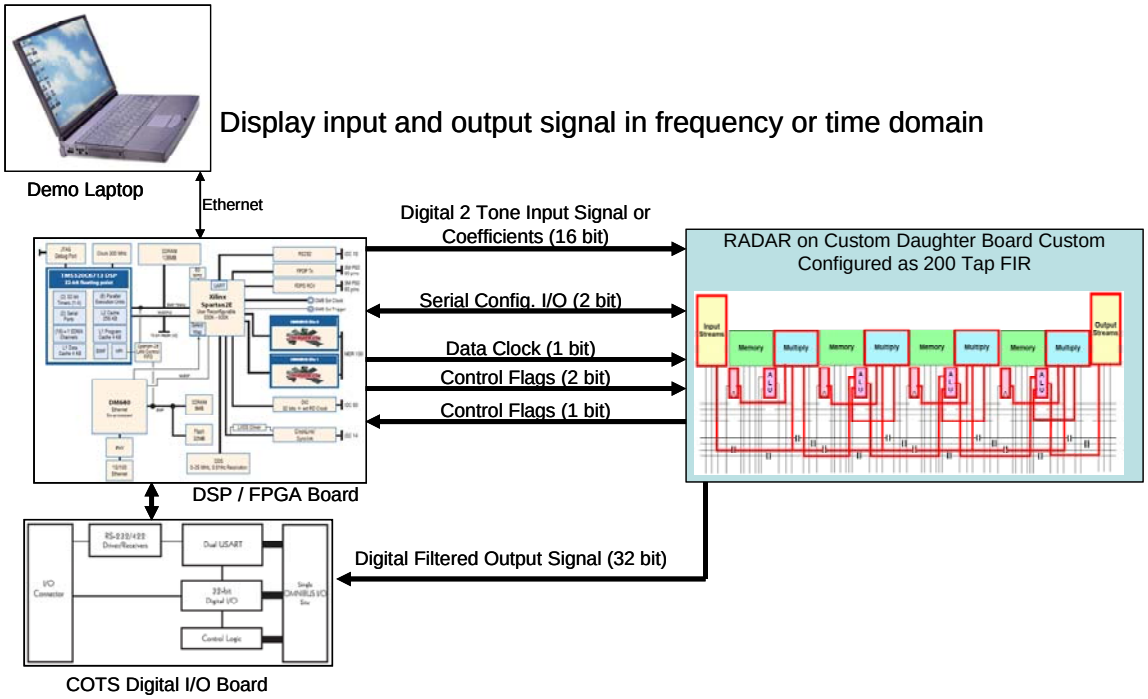


Figure 11 Block diagram of 200 tap FIR filter demo

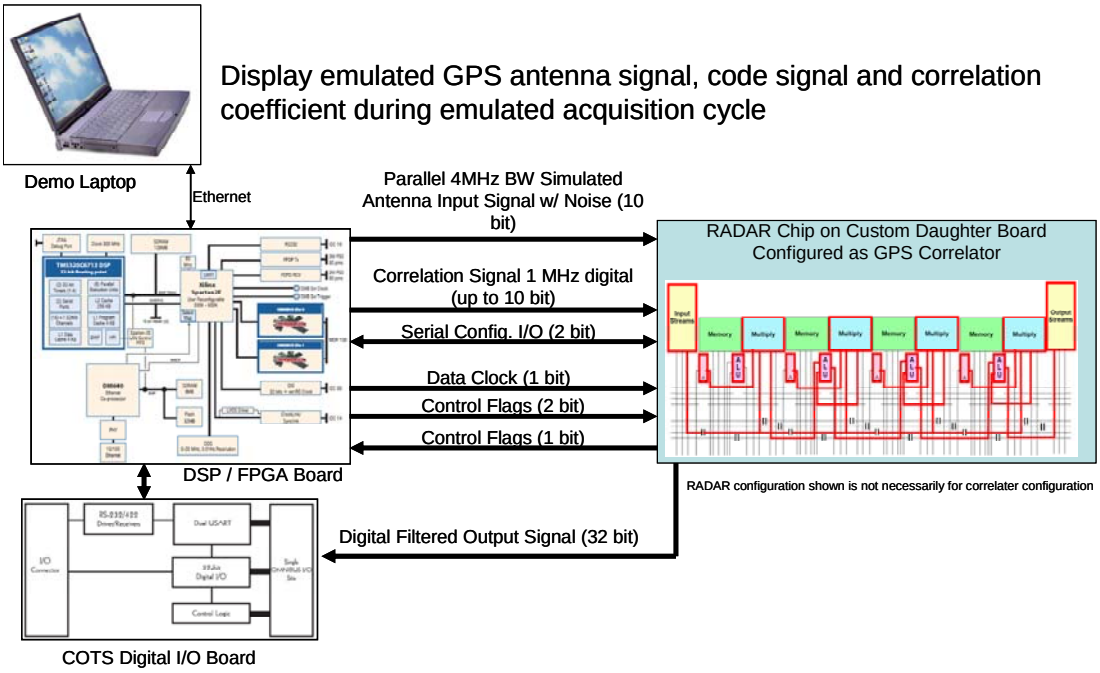


Figure 12. Block diagram of the demo of 1024 point correlator.

SRAM is fabricated on the same ASIC as the reconfigurable array. The demo architecture for the SRAM test is shown in Figure 7. The SRAM test could include the writing and reading the memory and detecting any errors by observing the flags coming from the ASIC. We expect that the SRAM test could be performed in a radiation beam. Then the Single Event Effect immune architecture could be tested.

Digital to Analog Converter Test Compatibility

The test bed could also be used for the demonstration of DAC functionality as shown in Figure 13.

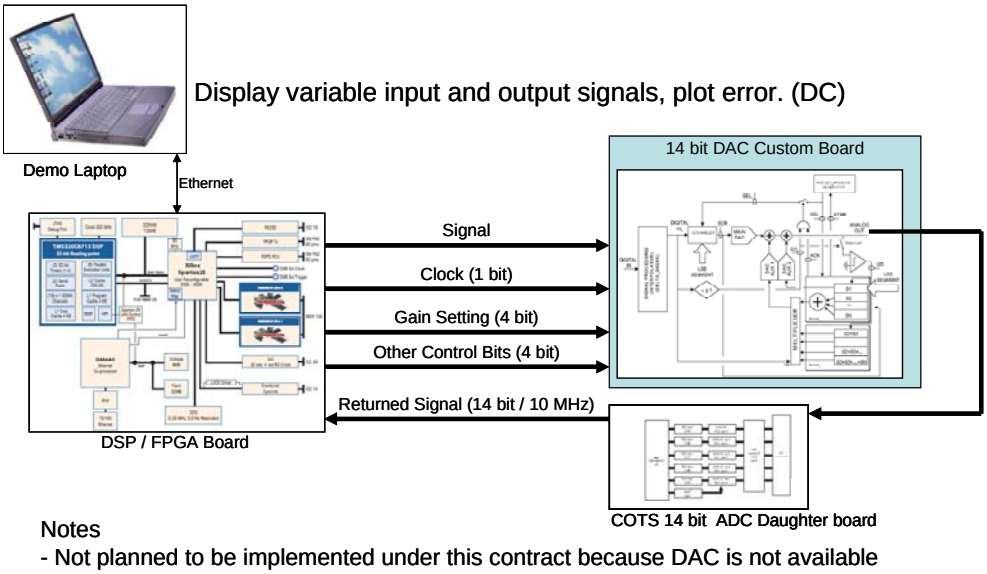


Figure 13. Test bed configuration for testing of DAC

Research Results and Technology Demonstrations

The demonstration of the PLL and demodulator ASICs' implementation of the reconfigurable I/O test bed has been given at the July, 2005 meeting of CDADIC. The test bed was also demonstrated at the AFRL, Kirtland on 8/17/05

Future Work Recommendations

The developed test bed is compatible with many configurations that could be exercised in the future (see Figure 14)

Even though the goals of the current program have been accomplished we recommend the following important future extensions of the program:

- fabricate SRAM/RADAR board and develop software for the demonstration
- design and fabricate DAC board and develop software for demonstration
- download decimating filter on the Xilinx chip to demonstrate true 10 bit ADC
- design and fabricate board for combined functionality demonstration

	Board								Comments
Demo	COTS DSP Mainboard	COTS Digital I/O	COTS ADC / DAC	Custom SRAM / RADAR	Custom PLL	Custom ΔΣ Modulator	Custom DAC	Combined Functionality	
PLL	✓				✓				Demonstrates reconfigurability: Icp, N
ΔΣ Modulator	✓		✓			✓			
RADAR	✓	✓		✓					Demonstrates reconfigurability: FIR and GPS Correlator
SRAM	✓	✓		✓					
DAC	✓	✓	✓				✓		
Combined Functionality	✓	✓	✓					✓	Include RADAR, SRAM, and modulator
Baseline Approach									
Possible Extension									

The baseline approaches consist of a COTS mainboard and daughter boards and custom ASIC boards

Figure 14. Possible test bed configurations for the future work.

PROJECT 13

RADIATION HARDENING BY DESIGN FOR DATA CONVERTERS

Prof. Gabor Temes (Oregon State University)
with Andy Peczalski (Honeywell)

RESEARCH TIME PERIOD: Two years
RESEARCH FOCUS: AFRL Task Areas 2 and 3: Standard Cell/Topologies and Reconfigurable Mixed-Signal Electronics.

Figures and Tables

Abstract

Our research program has as its main goal the development of novel architectures, circuitry and design methodologies for radiation-hardened, high-speed and high-linearity, current-steering digital-to-analog (DACs) interfaces realized in conventional CMOS technology. The key target of the project is the design and implementation of a radiation-insensitive delta-sigma (Δ-Σ) digital-to-analog modulator, using digital correction to enhance linearity and to correct for radiation and mismatch effects. It also utilizes a novel unit-element current matrix for the reduction of total-dose-effects (TDE). Δ-Σ converters are not strongly affected by single-event-effects (SEE), since they operate on the principle of storing and averaging many input signal samples to obtain each output sample [11]. The linearity correction developed by us has similar properties. The effects of radiation have been addressed also at the circuit level, and investigated based on device physics considerations. Specialized circuitry with low sensitivity to radiation is being developed. Finally, the dimensions and layout of the devices was established so as to minimize radiation effects and to maximize the yield. The critical components which are subject to single-events-upset (SEU) in the modulator, in the correction circuitry, and in the digital interpolation filters associated with the design have been identified. These will be designed with special care, and (if necessary) will incorporate redundant elements.

The devices were designed for fabrication in a well characterized and inexpensive commercial CMOS technology (such as a 4M-2P 0.35μm one), and will be tested at OSU for electrical performance. We also plan to perform laser testing for single-event effects using the University of Oregon's picosecond laser facility, as soon as testable chips are available.

The key feature of this project is the use of an inexpensive commercial CMOS process, rather than the less widely available SOI technology.

Project Description

The long-term goal of this research is to develop hardened-by-design (HBD) mixed-mode architectures and design techniques for CMOS digital-to-analog converters (DACs). In the research, HBD not only included special layout techniques, as is currently practiced, but also the development of special structures and topologies to overcome variations due to the presence of radiation. The motivation behind the task is mostly economical; it is also highly relevant to the AFRL solicitation and goals, as reflected in the specification of mixed-signal electronics, as it is shown in TABLE I [3]. It was shown recently [1] that in state-of-the-art deep-submicron thin-oxide CMOS technology, the total-dose effects on properly laid out (edgeless, guard-banded) MOS devices were markedly reduced. This was confirmed by the successful implementation of a 10-bit, 30 MHz serial ADC in 0.25μm CMOS, using radiation-tolerant layout, which retained full accuracy after a total dose of 10 Mrd(Si) [2].

The tasks involved in the project included:

1. A survey of available data on radiation effects in CMOS.
2. The acquisition of simulation methods and tools for radiation effects on CMOS devices.
3. A continued survey, and additional research, on radiation-tolerant layout techniques for both analog and digital circuitry.
4. Architectural study for digitally-corrected data converters which are minimally sensitive to radiation effects.
5. Circuit design for the data converters, incorporating HBD techniques.
6. HBD layout and fabrication of the data converter.
7. Testing and evaluating the device under various radiation conditions.

Research Results and Discussion

The researchers of this project developed a highly accurate HBD CMOS DAC. The target specifications were:

- ENOB ≥ 14-Bits
- Bandwidth = 10 MHz
- Sampling Frequency = 160 MHz
- Single Supply =3V
- Minimum Power Consumption
- Minimum Area

The HBD methodology that was followed includes the following key features:

1. Algorithm: by using digitally corrected oversampling data conversion, the sensitivity to single-event effects (SEE) can be reduced, so that accurate operation can be obtained. (The relative immunity of oversampled converters to SEE is due to the averaging of many samples inherent in the principle.)
2. Digital correction: by using digital correction, the task of maintaining accuracy is transferred from the inaccurate and sensitive analog circuits to the much more robust digital ones.
3. Circuit design: in the design of analog circuits, bootstrap techniques and PMOS switches will provide insensitivity to total-dose-effects (TDE). In the design of digital circuitry, redundant circuitry and majority voting can be used to obtain immunity to SEE.
4. Layout: new layout schemes were found for the current-source matrix, which is the key block of the DAC. The pattern provides reduced sensitivity to TDE as well as to linear and quadratic mismatch errors. The existing methods (edgeless layout, guard rings, etc.) which can be used to desensitize MOS devices to total dose radiation [5, 8-9, 12-13] will also be used for individual devices.
5. Because we use a 0.35μm technology, SET (Single-Event Transients) is not of big concern, as can be inferred from Figure 1 [7]. For faster technologies, the use of DICE (Dual Interlocked Cells) and/or temporal sampling techniques can be implemented.

Table 1: DoD Space and Missile Requirements

System	Req'd Part	Bit Res. (Bits)	Sample Rate (Msps)	Power (mW)
A	DAC	10-14	40	Not Spec'd
A	ADC	8-12	50 - 100	Not Spec'd
B	ADC	12	25	25
B	ADC	8	100	250
C	ADC	12-16	25	Not Spec'd
D	ADC	10	500	Not Spec'd
E	ADC	10-16	100	Not Spec'd
F	ADC	14	40	Not Spec'd
G	ADC	16	0.2	Not Spec'd

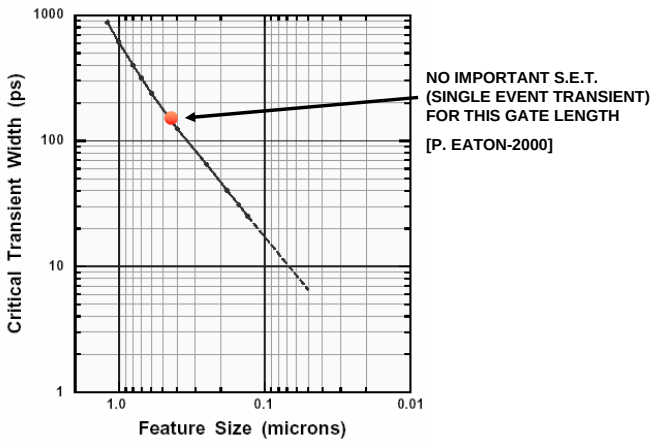


Figure 1: Critical transient width [ps] vs. feature size for combinatorial logic (from [7])

Figure 2 illustrates the overall block diagram. The interpolation filter increases the effective number of bits (ENOB), hence, increasing the stability margin of the delta-sigma loop. The developed chip implements the digital correction system, based on correlation procedures. The delta-sigma loop has been described in VHDL language, and it has been implemented in a commercial FPGA.Figure3 shows the details of the interpolation filter, and Figure4 the noise-shaping loop, which uses feed-forward branches to improve the effectiveness of the in-band noise reduction. The frequency responses of the digital systems working together are shown in Figure 5.

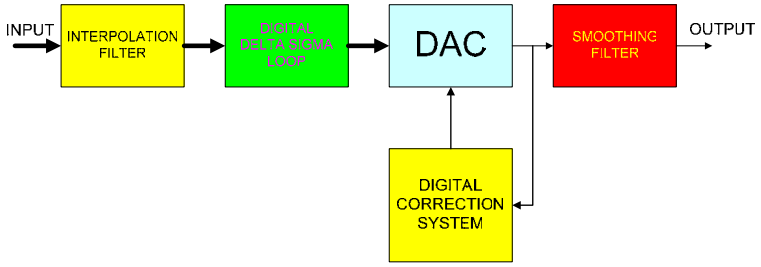


Figure 2: DAC system under development

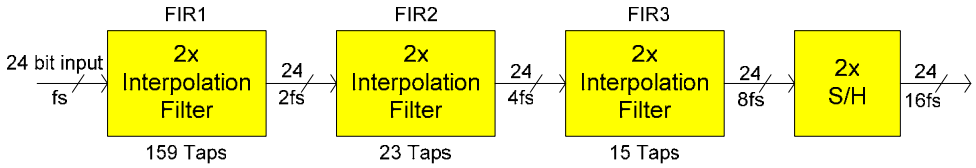


Figure 3: Interpolation filter details

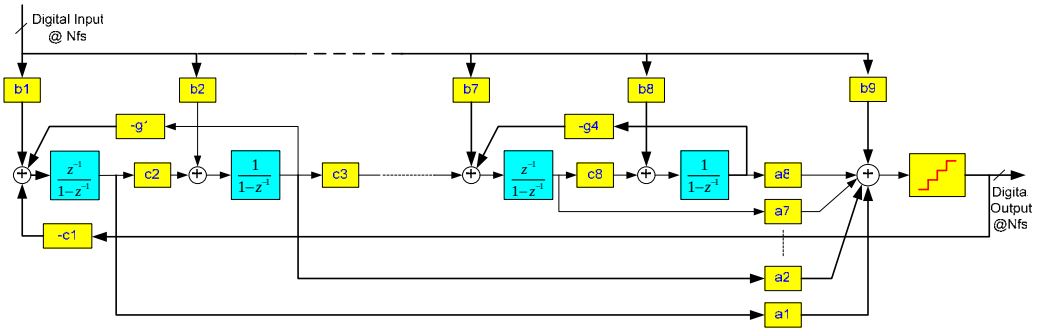


Figure 4: Block diagram of the digital delta-sigma loop.

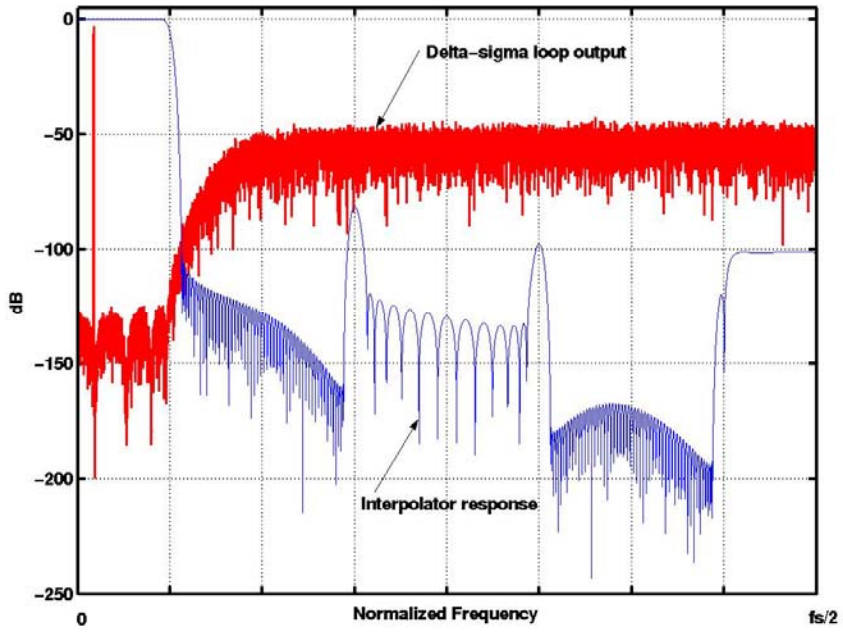


Figure 5: Output spectrum of the interpolation filter and of the digital delta-sigma

A novel digitally-corrected topology was found for a multi-bit DAC. The idea is illustrated schematically in Figure 6. The main components are the Main DAC composed of N unit elements, an Auxiliary (low-resolution) DAC, 2 banks of registers (BANK1 to store the DAC elements errors and

BANK2 to store the total errors for the different codes), a Scrambler to randomize the use of the unit elements, and associated logic.

The operation of the system is as follows. The Digital Input is preprocessed: data is passed through an interpolation filter and a digital delta-sigma loop, raising the Effective Number of Bits (ENOB) and the dynamic range. At the same time (in a parallel process) a Pseudo-Random Code is generated for a selected mid-range code. Assuming bipolar operation, the mid-range code is the zero code, and it corresponds to the use of half (N/2) of the total number of unit elements contained in the Main DAC. Also, this code will select the corresponding registers in BANK1 (line SEL) to update. This operation is realized in advance, that means that once the addition is completed then the system will wait until a middle code appears. At this point the digital value of the correction will be converted to an analog one (by means of the Auxiliary DAC), the Main DAC will use the corresponding elements (signal SEL will be copied to SEL1 and will command the Scrambler) and a comparison will be performed. The Scrambler will select the corresponding elements in the Main DAC only if SEL1 is active, and this will occur only if the code is the middle one (signal EQ active) and at the same time the correction in BANK1 is ready (signal ACK).

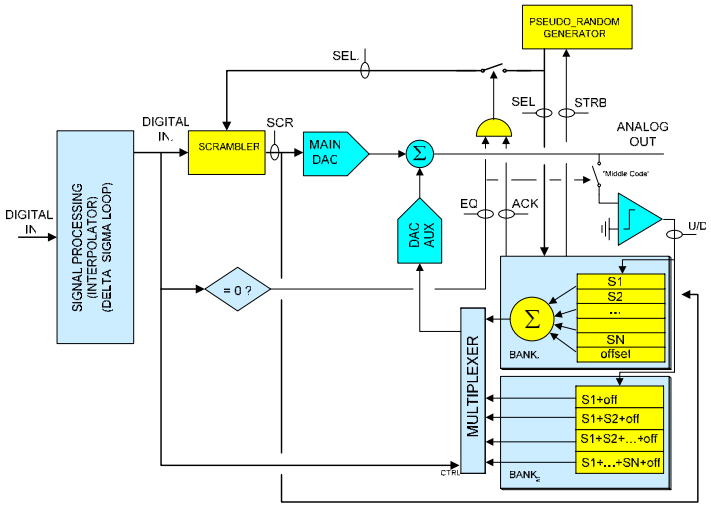


Figure 6: Schematic representation of the whole system. The Signal Processing block may contain an interpolator and a modulator to improve the ENOB

After this occurs, the 1-bit comparison will tell whether the corresponding registers in BANK1 must be increased or decreased. In BANK2 the registers will be modified as follows: referring to the Figure, it is shown that the first register of BANK2 will contain the error corresponding to the first element in the Main DAC, the second register will contain the error for the 1st and the 2d elements added together, and so on, until the last register that will contain the error of the sum of all the unit elements. When a specific unit element is used, then in accordance with the comparator output, the registers in BANK2 that contain this element will be increased/decreased. The idea behind this procedure is that the error is reduced when the comparison is carried out. Thus, in steady state the registers in BANK1 will contain a scaled version of the errors of the unit elements. If the registers in BANK1 and BANK2 have been updated in the same way and at the same time, then BANK2 will contain the scaled version of the errors for the N possible combinations (digital codes without being scrambled) of additions for the unit elements of the Main DAC. If the code is not the middle one, or if the system is busy, then the Auxiliary DAC will use the corresponding output from BANK2 (passing through a Multiplexer), and the correction will be performed. When the addition and the update of the registers in BANK1 and BANK2 are completed, then a signal (STRB) tells the registers are ready to perform another operation.

SEE is not a major hazard in the digital signals processed because the use of the oversampled system (ΔΣ DAC), where a single error is reduced in the averaged result. The higher the OSR, the higher the immunity to SEE. Any error introduced in the loop after the first integrator is shaped, i.e., its power is moved out of the signal band to high frequency, and will be easily filtered out with the smoothing-reconstruction filter at the output. For stored data, triple redundancy and majority voter circuitry can be used.

A study of radiation effects in the new architecture was performed. Two architectures, one for low speed and another one for high speed, were derived and simulated at the system level. A simple representation of SEE was found for unit-element DACs, and used to simulate the expected effects. Figure 7 shows the simplified schematic of the implemented low-speed system. Fully differential operation reduces common mode effects, and doubles the output amplitude.

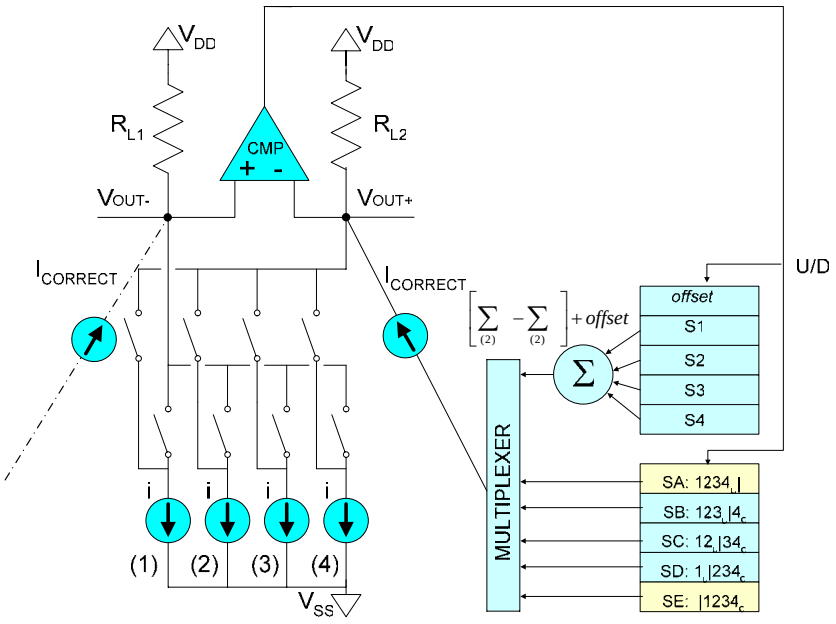


Figure 7: Simplified schematic of a 2-bit current-steering corrected DAC system. The offset compensation stabilizes the system.

Simulations have shown the feasibility of the correction process. As an example, Figure 8 shows the actual original errors in the current sources, the estimated corrections, and the residual errors for a 3-bit DAC. Figure 9 shows the convergence process for the same device. In Figure 10, three cases of the system frequency response are shown: a) ideal, b) real, c) corrected. Three sinusoids were used in order to observe intermodulation products due to the nonlinear characteristics of the real device.

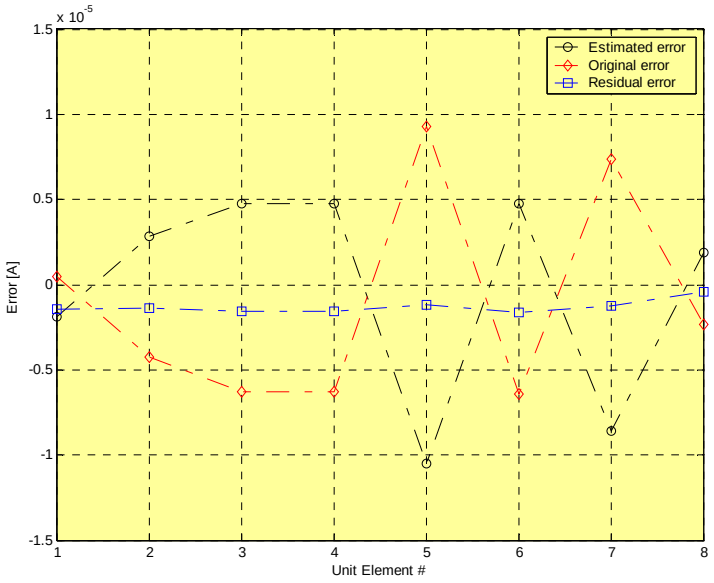


Figure 8: Static linearity improvement after convergence.
The unit current sources had a nominal value of 2.5mA. 8-bit deviation from ideal values. The output was taken over a 50Ω differential resistive load.

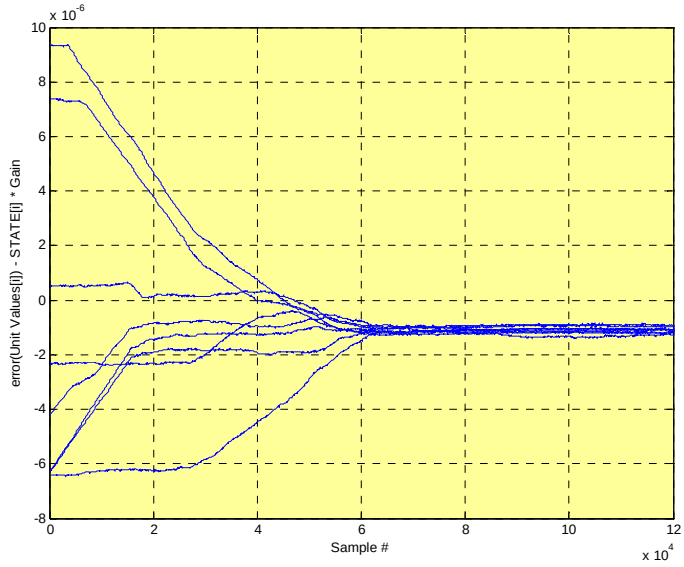
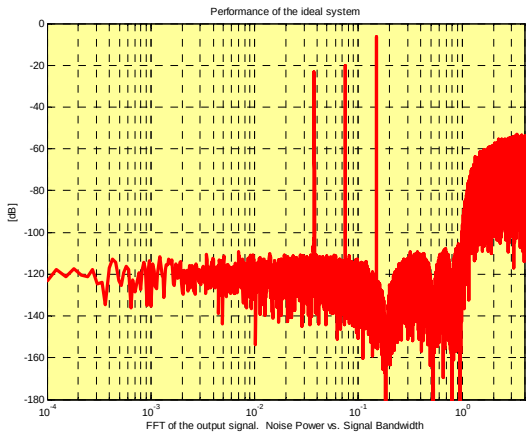
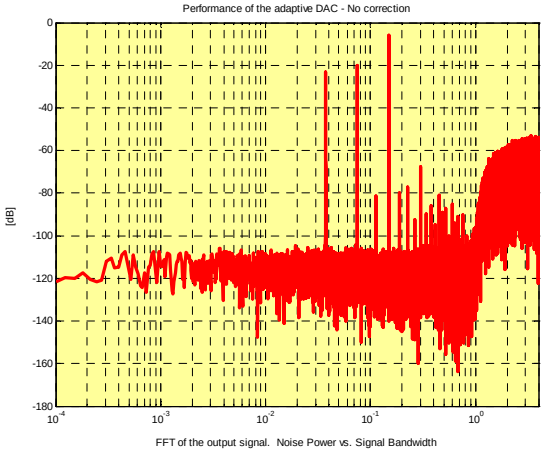


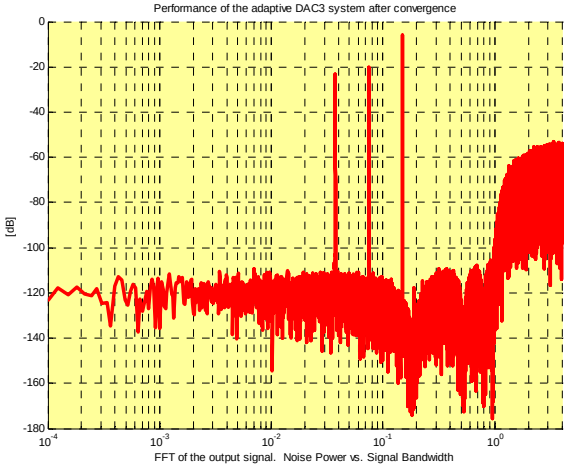
Figure 9: Convergence of the system vs. number of samples (timeless scale) for the previous system



(a) Ideal System



(b) 8-bits of linearity system



(c) Corrected system

Figure 10: High level simulation of the whole system. Realistic models for the current sources, the comparator and the resistors were implemented. 3 tones used to visualize intermodulation products

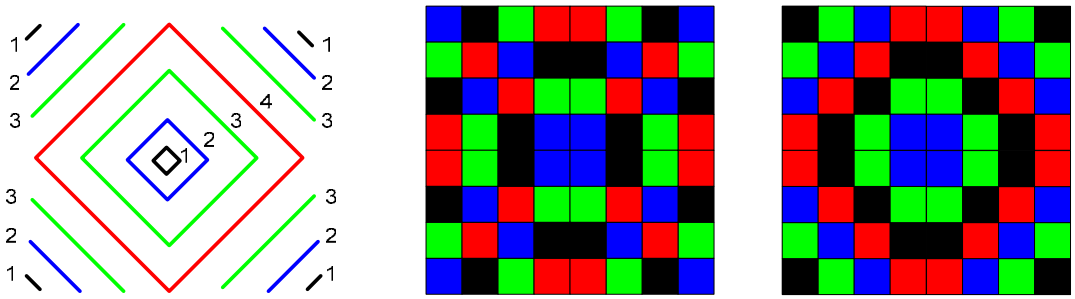


Figure 11: Quadratic and linear effects insensitive layout.
a) Main idea; b)Two possible examples for a 2-bits (four unit elements) design.

The use of an analog unit-element matrix, Figure 11, mitigates individual errors, whether due to radiation or mismatch. TDE problems can be reduced by choosing the devices' geometric structure (layout) appropriately. Dividing each unit element into several subunits located at remote places, combined with a special switching sequence, creates another averaging, but this time a spatial one. Large gate areas will be used in the current sources, and edgeless or H-shaped layouts could be realized to decrease leakage currents.

The use of guard rings to collect minority carriers in the substrate will avoid latch-up and also reduce the propagation of currents through the substrate and below the field oxide.

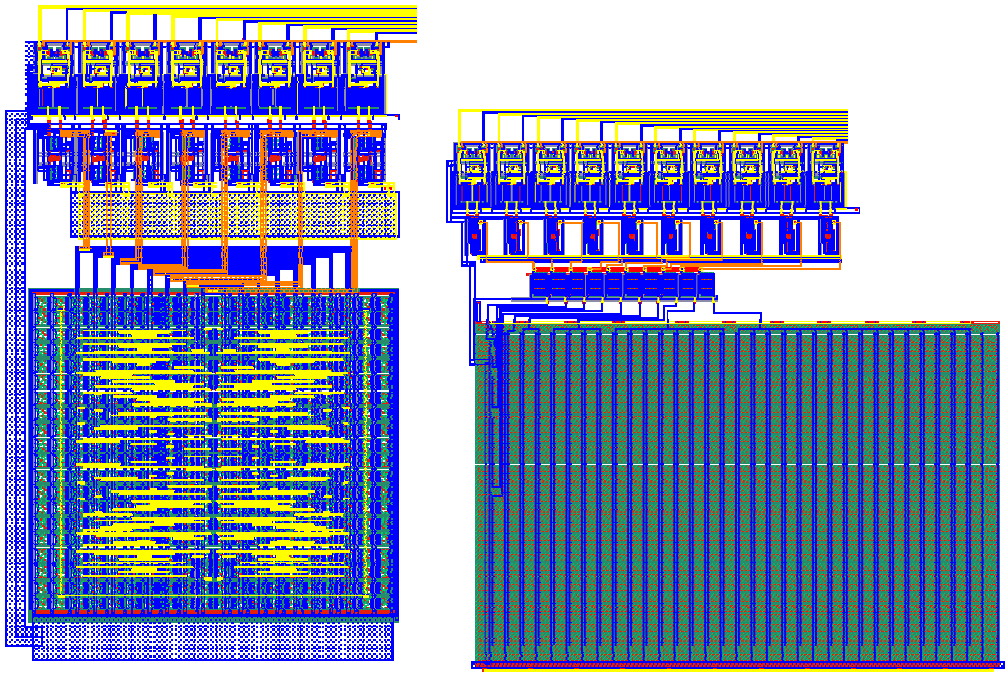


Figure 12: Layout of the mismatch tolerant DACs
a) 20mA, 3-bits thermometer decoded DAC, with 10-bit linearity;
b) 1mA, 10-bits, 10-bit linear binary weighted DAC for correction purposes.

Figure 12 shows the special layout for the two DACs: the main DAC and the auxiliary DAC. The main DAC uses the proposed technique; meanwhile the compensation DAC uses a binary weighted scheme. Matching layout rules were applied in both cases, to get at least 10-bts of static integral nonlinearity (INL) by construction.

In each DAC, a novel high speed latch is used to accurately set the crossover point for the switches that command the current steering process (this increases the maximum converter frequency, and at the same time reduces the glitch power, reducing hence the overall harmonic distortion at the output). Figure 13 shows the idea and the simplified schematic of the proposed device.

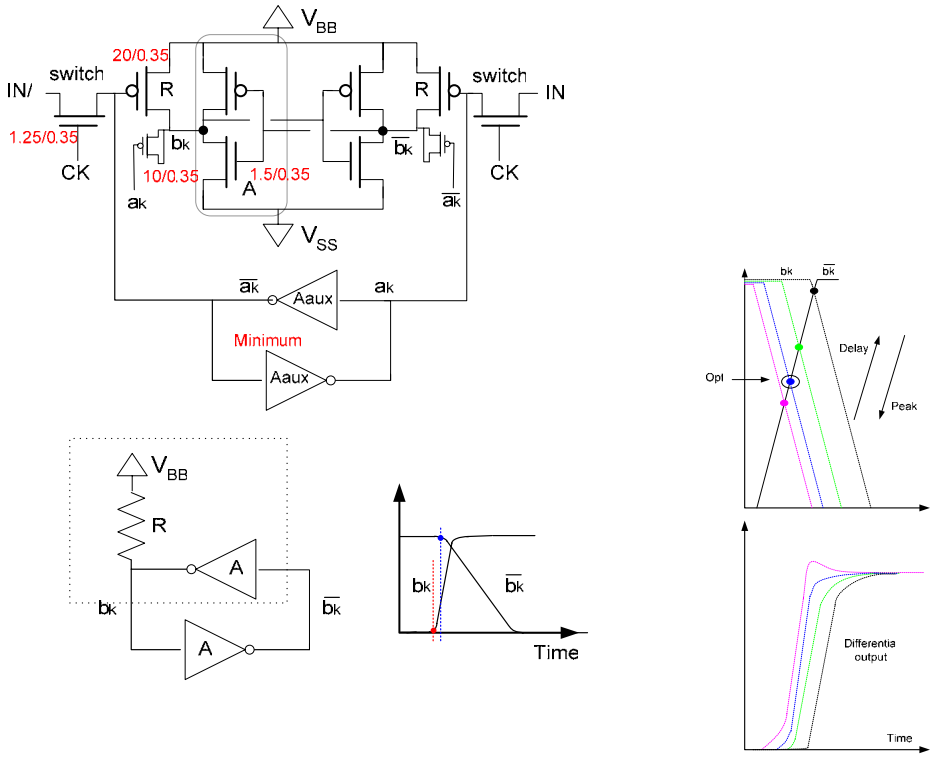
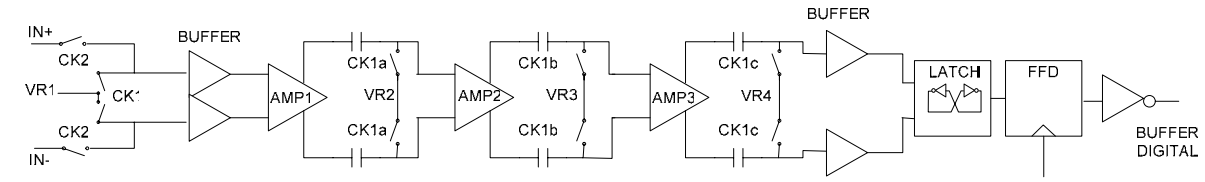
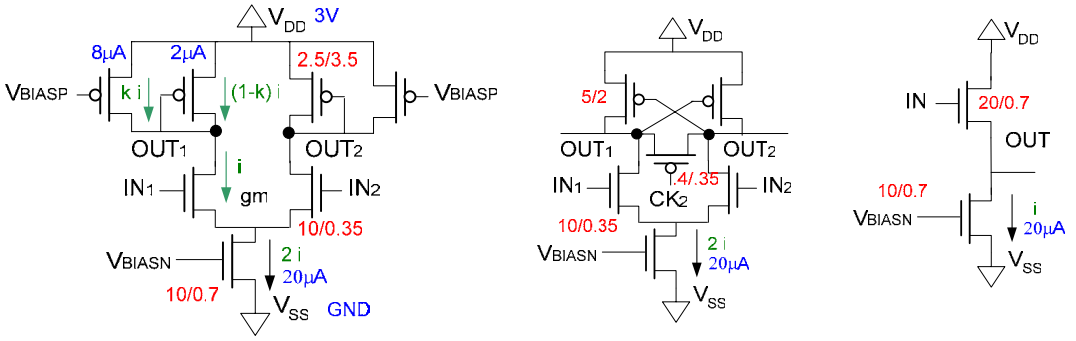


Figure 13: New high-speed latch for the current sources, with feed-through compensation and optimized crossover point (as depicted in the inset).

The critical blocks in the system have been identified The CMOS analog comparator is one of these. Radiation-induced memory effects in it will lead to big offset voltages. A possible solution is trying to keep the average value of its input constant. The comparator output does not need to be SEE insensitive, since the correction system also performs averaging. The comparator is a 3-stage offset-compensated circuit. We developed three different comparators, depending on the application. The main schematic of the device is depicted in Figure 14, together with its main constitutive blocks. It is a 3-stage output offset compensated comparator. Figure 15-a shows the comparator layout of the on-chip implemented version, specially suited for high-resolution, moderate-speed operation (mismatch optimized). Figure 15-b shows the layout for a high-speed design (routing matching). Figure 15-c shows the HBD version of the comparator (Figure 16 shows some critical details).



(a)



(b)

Figure 14: Schematic of the high resolution comparator.
a) Block diagram, showing a 3-stage output-offset-compensated device, followed by a latch to avoid meta-stability problems; b) Schematic of the building blocks

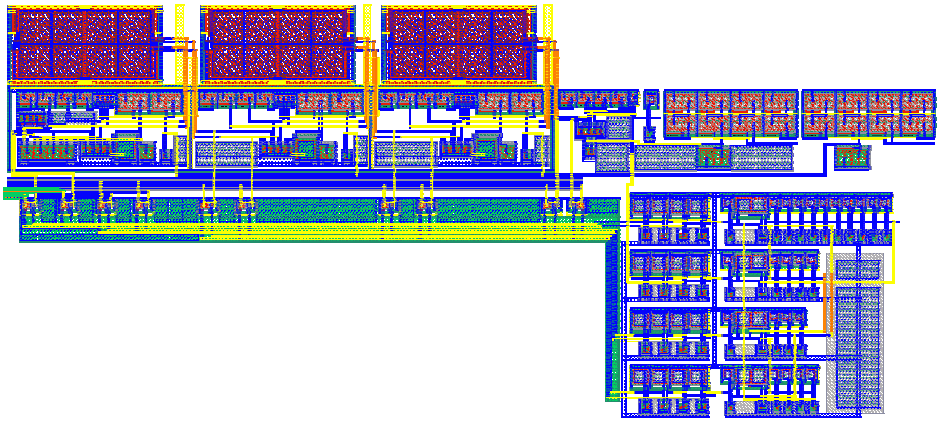
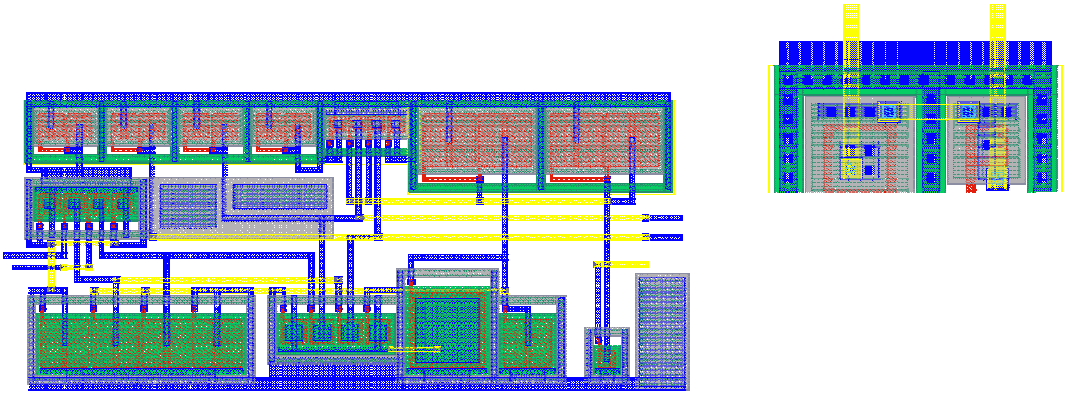


Figure 15: Comparator layouts.



Test Chips

Figure 17 shows the fabricated chip. Figure 18 shows the simulated response (more than 20dB of improvement).

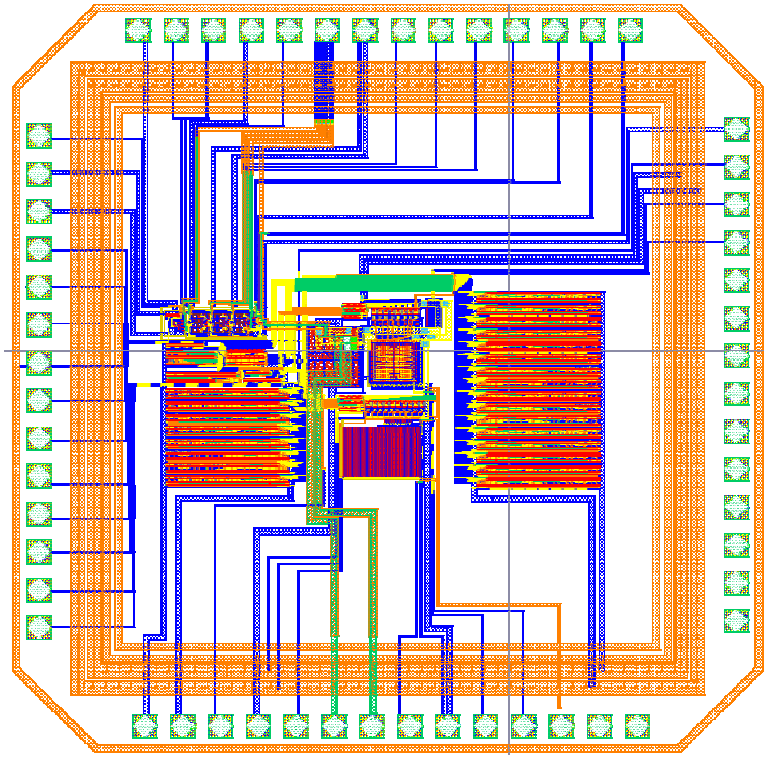


Figure 17: Layout of the chip

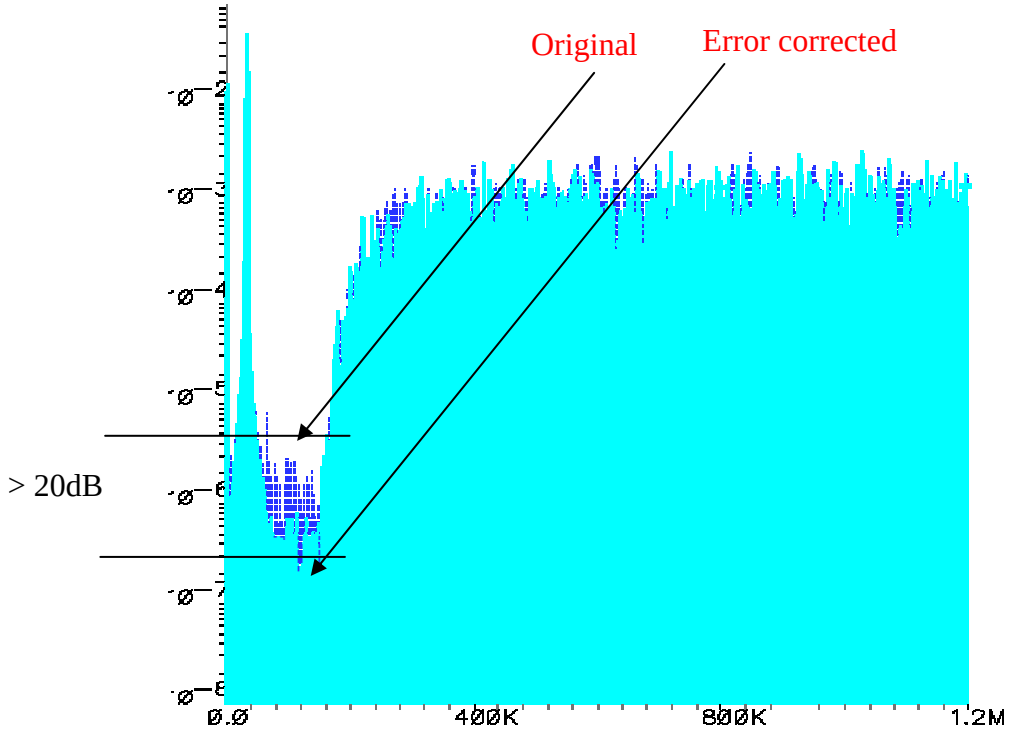


Figure 18: Low frequency sinusoidal input.

Increase of the SFDR in more than 20dB (more than 3-bits of linearity improvement)

OTHER RESULTS

Technology Transfer/Intellectual Property

This work will be used by Honeywell to incorporate our DAC into their unified demonstration application vehicle, and to take advantage of their accumulated know-how on radiation effects and rad-hard testing. In addition, ADI (Analog Devices, Inc.) has provided funding for the first prototype of our CMOS DAC. Right now, the researchers on this project are in close contact with Jazz Semiconductor for the fabrication of our next generation of rad-hard data converters.

Publications Resulting from Research

None at this time.

Benefits to Commercial Sector

The principles applied in this research for the design of circuits working under radiation conditions remain valid for the design of data converters and other mixed-mode circuits operating in other hostile environments found in the commercial sector, such as automotive electronics.

References

[1] R. C. Lacoe et al, “Application of Hardness-By-Design Methodology to Radiation-Tolerant ASIC Technologies,” IEEE Transactions on Nuclear Science, Vol. 47, NO. 6, Dec. 2000.

[2] A. Rivetti et al, “A Low-Power 10bit ADC in a 0.25-µm CMOS: Design Considerations and Test Results,” IEEE Transactions on Nuclear Science, Vol. 48, NO. 4, Dec. 2001.

[3] K. G. Merkel II & A. L. Wilson, “A Survey of High Performance Analog-to-Digital Converters for Defense Space Applications”, 2003.

[4] K. Avery and R. Turfler, “Point of Application Controller (POAC) for Space Systems”, ©IEEE 2003.

[5] D. Mavis & D. Alexander, “Employing Radiation Hardness By Design Techniques with Commercial Integrated Circuits Processes”, Mission Research Corp (MRC).

[6] D. Mavis et al, “A Reconfigurable, Nonvolatile, Radiation Hardened Filed Programmable Gate Array (FPGA) for Space Applications”, (MRC).

[7] D. Mavis & P. Eaton, “Soft Error Rate Mitigation Techniques for Modern Microcircuits”, (MRC)

[8] Giovanni M. Anelli, PhD Thesis: *Conception et Caractrisation des Circuits Integres Resistants aux Radiations.…*, Institut National Politechnique de Grenoble, December 2000.

[9] http://rd49.web.cern.ch/RD49/RD49Docs/anelli/a_Index.pdf

[10] Feliciano Giustino, Tesi di Laurea, *Radiation Effects on Semiconductor Devices*, Politecnico Di Torino, Italy, March 2001.

[11] F. Faccio,“Future Trends in Radiation Hard Electronics,” http://ssd-rd.web.cern.ch/ssd-rd/rd/talks/faccio-rd-2001.pdf

[12] C. Edwards et al., “A Multibit ΣΔ Modulator Floating-Body SOS/SOI CMOS for Extreme Radiation Environments,” C. F. Edwards et al., *IEEE JSSC*, Vol 34, No. 7, July 1999.

[13] Martin Dentan, ”Radiation Effects On Electronic Components And Circuits,” http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/Tutorial/Coursedentan2.pdf

[14] B. W. Offord, J.S. Ruthberg, “Radiation-Hardened Silicon-on-Insulator 0.8 µm Technology Design Rules,” May 1999. http://www.spawar.navy.mil/sti/publications/pubs/td/3065/td3065.pdf

[15] P.A. Frances, P. Ferrat & Q. Huang, “A 13b 1.1MHz Oversampled DAC with Semidigital Reconstruction Filter,” Proceedings of ISSCC 2004, paper 20.6, pgs 370-371.

PROJECT 14

DESIGN OF RADIATION-HARD ANALOG/MIXED-SIGNAL CIRCUITS IN SILICON-ON-INSULATOR (SOI) TECHNOLOGY

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RESEARCH TIME PERIOD: One year
RESEARCH FOCUS: AFRL Task Areas 2, 3, and 6: Standard Cell/Topologies in Radiation-Hardened SOI, Reconfigurable Mixed-Signal Electronics, and Ultra-Low-Power Technologies

Figures and Tables

Abstract

State-of-the-art DAC was developed, using novel radiation-hardened analog and digital stages and building blocks. The impact of both CMOS fabrication device issues and device-level radiation effects on the performance of these circuits were examined. A special design technique was incorporated in the analog circuits, which involved the use of digital correction to monitor and overcome the effects of parameter variations due to radiation exposure.

This project was only funded for one year and not all of the goals were met, however. Progress of the research included: the study of SOI technology devices and circuits; different devices and layouts were proposed in order to reduce leakage paths and the parasitic effect of the associated BJT in each SOI transistor device; a study and simulation of a new charge transfer amplifier (CTA) were conducted and modification of a known CTA, incorporating chopping at the input, and reducing the memory effects were completed. In addition, the study and simulation of new architectures for amplifiers with high linearity, based on direct feedback and dynamic bias concepts were conducted, and a simulation and layout of a 3-bit flash ADC in SOI were finalized. A 0.5 μm SOI technology was assumed for this architecture. A study and simulation of a new architecture for a multibit Δ-Σ ADC with low DAC distortion were also conducted. The use of a multi-bit quantizer, together with a 1-bit feedback DAC, enables the architecture to reduce the DAC non-linearities. The compensation of the scheme is entirely performed in the digital domain

Project Description

The goal of this research was to use hardening-by-design (HBD) methodology for the development of analog-to-digital as well as digital-to-analog data converters. A key feature is the use of digitally-corrected analog circuitry and implementation methodologies. Specialized layouts as well as circuit techniques was utilized to achieve robustness against radiation effects, while using only inexpensive commercial CMOS technology.

Research Results and Discussion

A novel digitally-corrected topology was found for a multi-bit DAC. The idea is illustrated schematically in Figure 1. The main components are the Main DAC composed of N unit elements, an Auxiliary (low-resolution) DAC, 2 banks of registers (BANK1 to store the individual errors and BANK2 to store the errors for the different codes), a Scrambler to randomize the use of the unit elements, and associated logic.

The operation of the system is as follows. The Digital Input is preprocessed: data is passed through an interpolation filter and a digital delta-sigma loop, raising the Effective Number of Bits (ENOB) and the

dynamic range. At the same time (in a parallel process) a Pseudo-Random Code is generated for a selected mid-range code. Assuming bipolar operation, the mid-range code is the zero code, and it corresponds to the use of half (N/2) of the total number of unit elements contained in the Main DAC. Also, this code will select the corresponding registers in BANK1 (line SEL) to update. This operation is realized in advance, that means that once the addition is completed then the system will wait until a middle code appears. At this point the digital value of the correction will be converted to an analog one (by means of the Auxiliary DAC), the Main DAC will use the corresponding elements (signal SEL will be copied to SEL1 and will command the Scrambler) and a comparison will be performed. The Scrambler will select the corresponding elements in the Main DAC only if SEL1 is active, and this will occur only if the code is the middle one (signal EQ active) and at the same time the correction in BANK1 is ready (signal ACK).

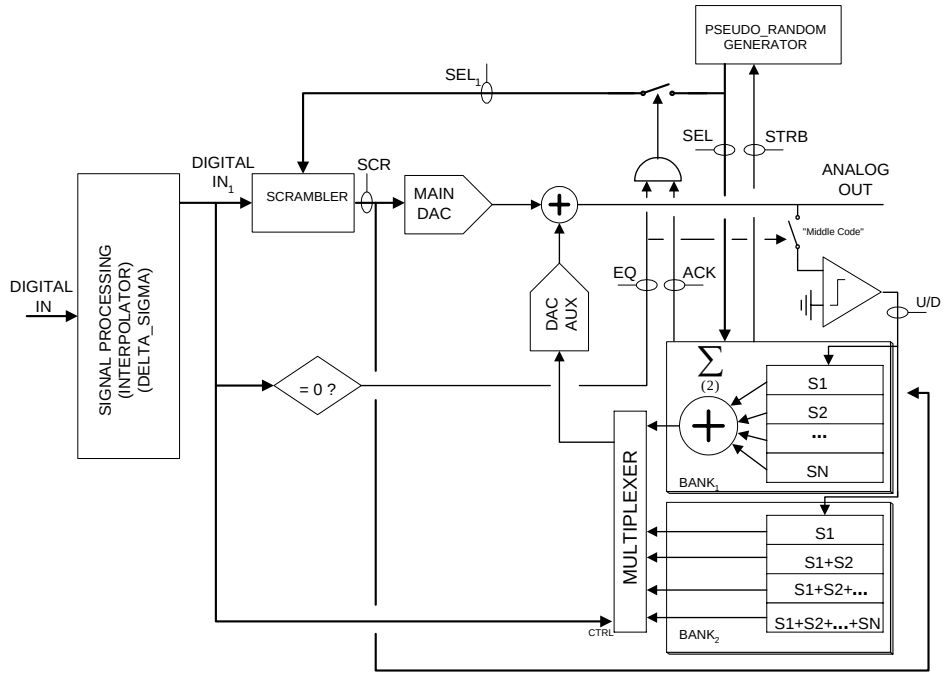

Figure 1: Schematic representation of the whole system.
(The Signal Processing block may contain an interpolator and a modulator to improve the ENOB.)

After this occurs, the 1-bit comparison will tell whether the corresponding registers in BANK1 must be increased or decreased. In BANK2 the registers will be modified as follows: referring to the Figure, it is shown that the first register of BANK2 will contain the error corresponding to the first element in the Main DAC, the second register will contain the error for the 1st and the 2d elements added together, and so on, until the last register that will contain the error of the sum of all the unit elements. When a specific unit element is used, then in accordance with the comparator output, the registers in BANK2 that contain this element will be increased/decreased. The idea behind this procedure is that if the error is reduced when the comparison is carried out. Thus, in steady state the registers in BANK1 will contain a scaled version of the errors of the unit elements. If the registers in BANK1 and BANK2 have been updated in the same way and at the same time, then BANK2 will contain the scaled version of the errors for the N possible combinations (digital codes without being scrambled) of additions for the unit elements of the

Main DAC. If the code is not the middle one, or if the system is busy, then the Auxiliary DAC will use the corresponding output from BANK2 (passing through a Multiplexer), and the correction will be performed. When the addition and the update of the registers in BANK1 and BANK2 are completed, then a signal (STRB) tells the registers are ready to perform another operation.

Simulations have shown the feasibility of the correction process. As an example, Figure 2 shows the actual original errors in the current sources, the estimated corrections, and the residual errors for a 3-bit DAC.

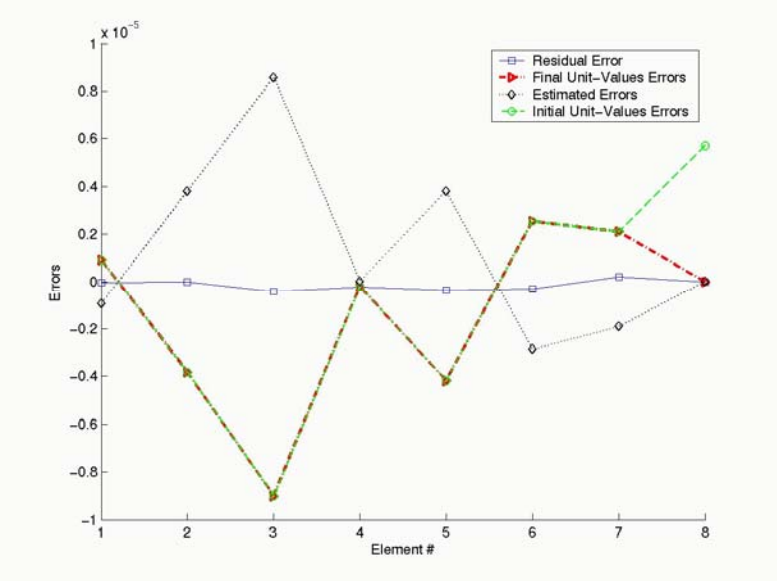

Figure 2: Errors in the 3-bit simulated system.

A formula for the minimum requirements (in terms of area) for the unit current sources of the DAC was also found, and was verified with extensive Monte Carlo simulations.

The noise-shaping loop and the interpolation filter are also under study and development, in order to obtain an optimized design. The hardening-by-design (HBD) concept followed here is: triple redundancy with majority vote, to desensitize the structure against SEE. The same technique will be employed in the digital section of the analog/digital correction loop.

Considering layout techniques, square transistors and/or guard rings will be employed in the layout of the digital transistors (analog ones should not be square, for matching reasons). Also, a new strategy will be followed to desensitize the DAC's unit-current-source structure against total-dose effects (TDE). This is depicted schematically in Figure 3 for a 2-bit DAC. The idea is to transform quadratic errors (which may be caused by stress in the packaging, and may get increased by continuous TDE) into a linear gain error, thus obtaining good linear matching. The linear errors can be cancelled using common centroid structures, which is a usual practice.

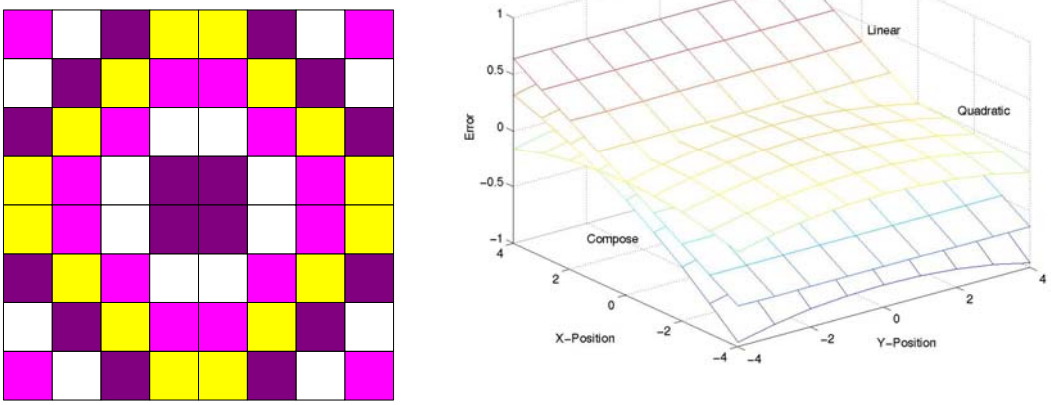

Figure 3: Example of layout for a 2-bit DAC.
*Quadratic errors are transformed into a constant gain error. Linear errors are cancelled by means of common centroid layout. b) Simulated matrix.)

Other Results

Technology Transfer/Intellectual Property

Not at this time.

Publications Resulting from Research

Not at this time.

Benefits to Commercial Sector

Commercial benefits can be anticipated, since the novel digital techniques used to correct the behavior of analog components will allow the use of inexpensive CMOS technology in radioactive environments, thus allowing robust system-on-chip (SOC) developments. Also, it is likely that the idea can be extended to Nyquist-rate data converters (rad-hard or otherwise), with high speed and accuracy.

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