AFRL-SN-WP-TP-2005-1164

AEROSPACE SENSOR COMPONENT AND SUBSYSTEM INVESTIGATION AND INNOVATION-2 COMPONENT EXPLORATION AND DEVELOPMENT (ASCSII-2 CED)

Delivery Order 0002: Volume 3 – Reconfigurable Aperture Antenna Virtual Prototyping (General Techniques For De-Embedding RF Passive Devices)

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SEPTEMBER 2005

Final Report for 30 March 2001 – 31 Mar 2005

Approved for public release; distribution is unlimited.

STINFO FINAL REPORT

SENSORS DIRECTORATE
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WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7320

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

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1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
September 2005	Final	30 Mar 2001 – 31 Mar 2005

4. TITLE AND SUBTITLE

Aerospace Sensor Component And Subsystem Investigation And Innovation-2 Component Exploration And Development (ASCII-2 CED)

Delivery Order 0002: Volume 3 – Reconfigurable Aperture Antenna Virtual Prototyping (General Techniques For De-Embedding RF Passive Devices)

5a. CONTRACT NUMBER F33615-00-D-1726-0002

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER 62204F

6. AUTHOR(S)

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5d. PROJECT NUMBER 2002

5e. TASK NUMBER 06

5f. WORK UNIT NUMBER 08

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Systran Federal Corp.
4027 Colonel Glenn Highway, Suite 210
Dayton, OH 45431-1672

Information Electronics Group
Electrical and Computer Engineer
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Columbus, OH 43212

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

SENSORS DIRECTORATE
AIR FORCE RESEARCH LABORATORY
AIR FORCE MATERIEL COMMAND
WRIGHT-PATTERSON AFB, OH 45433-7320

10. SPONSOR/MONITOR'S ACRONYM(S) AFRL/SNDM

11. SPONSOR/MONITOR'S REPORT NUMBER(S) AFRL-SN-WP-TP-2005-1164

12. DISTRIBUTION / AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

13. SUPPLEMENTARY NOTES

See also Volume 1, AFRL-SN-WP-TR-2005-1162 and Volume 2, AFRL-SN-WP-TR-2005-1163.
This report contains color.

14. ABSTRACT

In this report, a rigorous investigation of the de-embedding of RF inductors and capacitors was presented. The typical parasitic impedances present in an RF test structure were discussed. Basic knowledge of these parasitics allows the designer to effectively adjust the test structures to account for any limitations imposed by the probe technology being used. Some technologies allow traces to be etched at arbitrary angles, making it possible for a coplanar waveguide interconnect to be used, thus minimizing the interconnect impedance.

15. SUBJECT TERMS:

De-embedding Techniques, RF passives, RF inductors, parasitic impendence, coplanar waveguide

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Gregory L. Creech
Unclassified	Unclassified	Unclassified	SAR	21	19b. TELEPHONE NUMBER *(include area code)* (937) 255-4831 X3486

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std. 239.18

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Chapter 1 De-embedding Techniques for RF Passives

There are many published methods that deal with the de-embedding of active devices at higher frequencies [1]. However, locating de-embedding techniques that deal with larger RF passive devices such as inductors and capacitors is difficult. The techniques for de-embedding smaller active devices cannot be blindly applied to RF inductors and capacitors. In the case of inductors, the length of a thru de-embedding structure would add too much inductance and cause error in the de-embedded result. For capacitors, especially MIM capacitors, the ohmic loss is so small that it is easy to over-estimate the loss of the test structure, resulting in a negative real part in the 2-port differential impedance. It is sometimes better to neglect de-embedding this loss, as it is so small to begin with that the de-embedded result is usually no more accurate than the raw measured value.

We begin with a diagram in Figure 1 showing the typical parasitics that need to be de-embedded from an RF passive device measurement made on a ground-signal-ground test structure such as the one shown in Figure 2. It is observed from the figure that there are only four parasitics that need to be de-embedded. The coupling from port to port can be neglected due to the large size of the test structure.

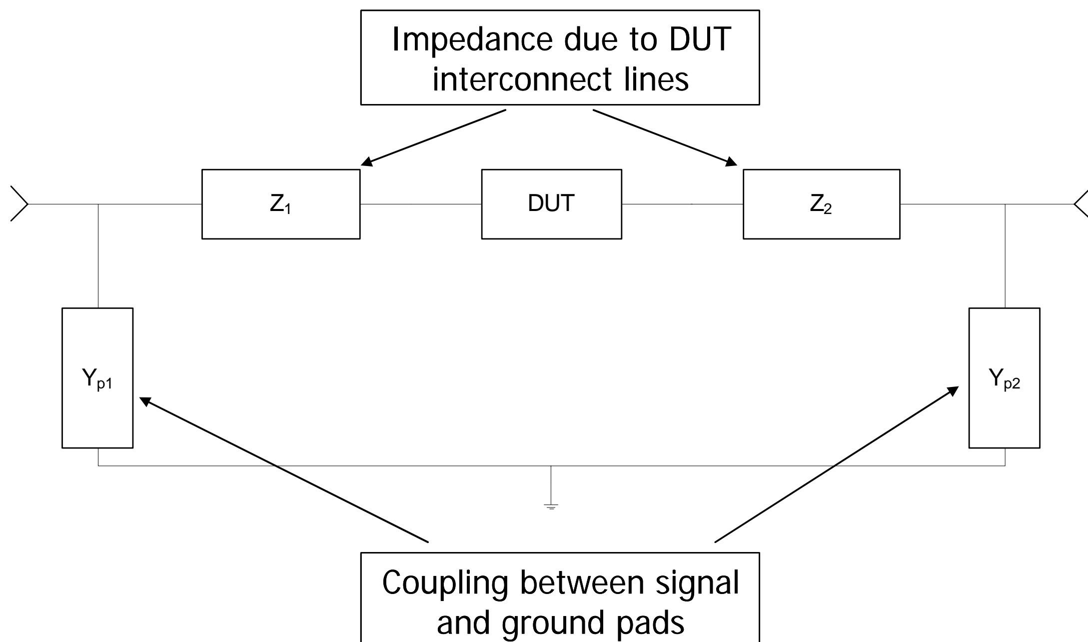

Figure 1 - RF passive device testbed parasitics

The test structures fabricated and measured in this study use a BiCMOS process with seven available metal layers. The design and measurement was performed by the Mixed Signal Design Team at the AFRL at Wright Patterson Air Force Base. The silicon bulk is lossy with a resistivity of $13.5\,\Omega\cdot cm$. For the inductors, a non-conductive deep trench is used beneath for the ground-plane. For the capacitors, a conductive ground-plane is used.

1.1 Capacitor Test Structure

We first discuss a technique for calculating the parasitics for a capacitor test structure shown in Figure 2. To de-embed the coupling from the ground pads to the middle signal pad, we use the open test structure shown in Figure 3. The parasitics of the open structure are given in Figure 4.

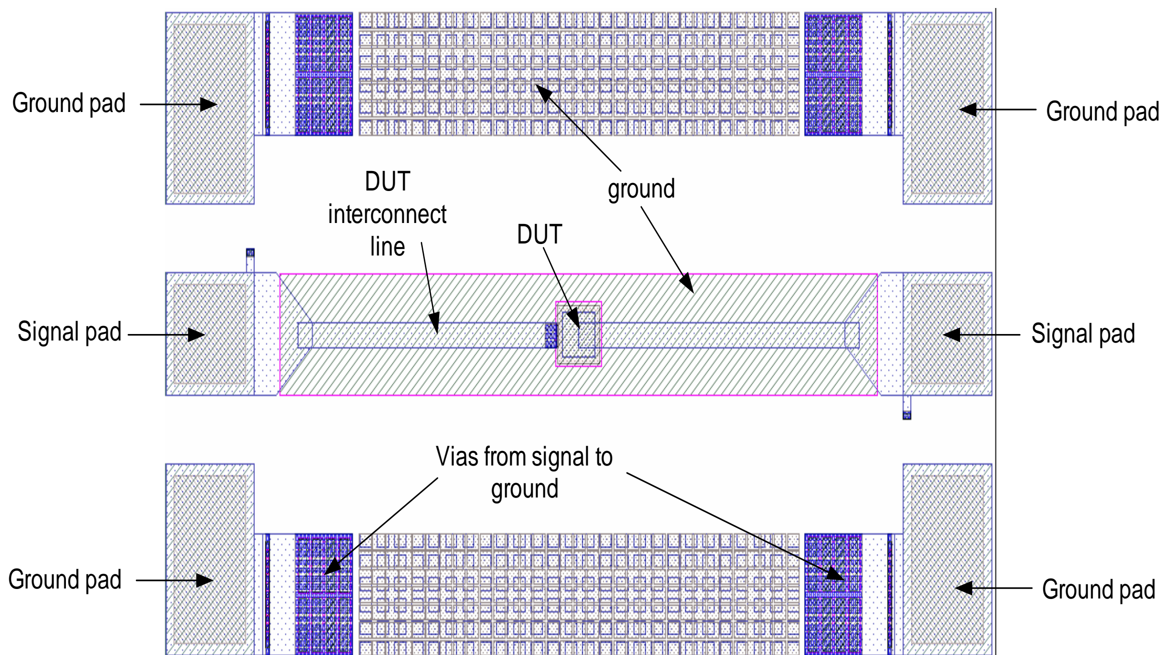

Figure 2 - Capacitor test structure

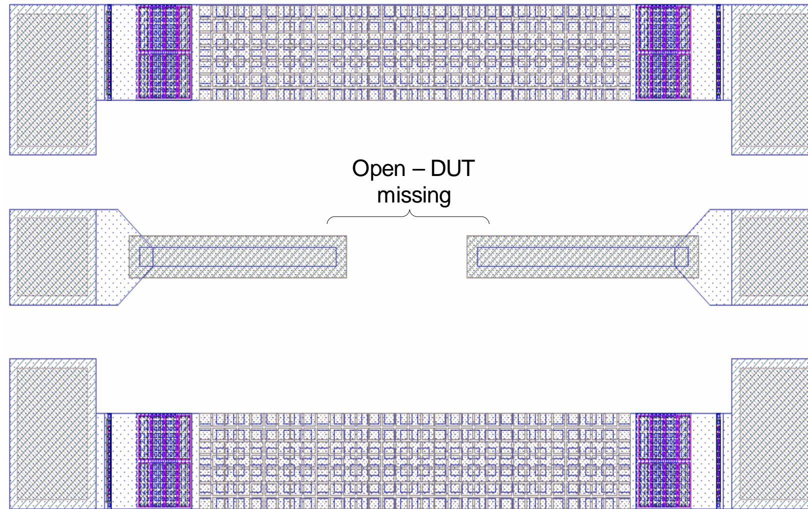

Figure 3 - Capacitor open

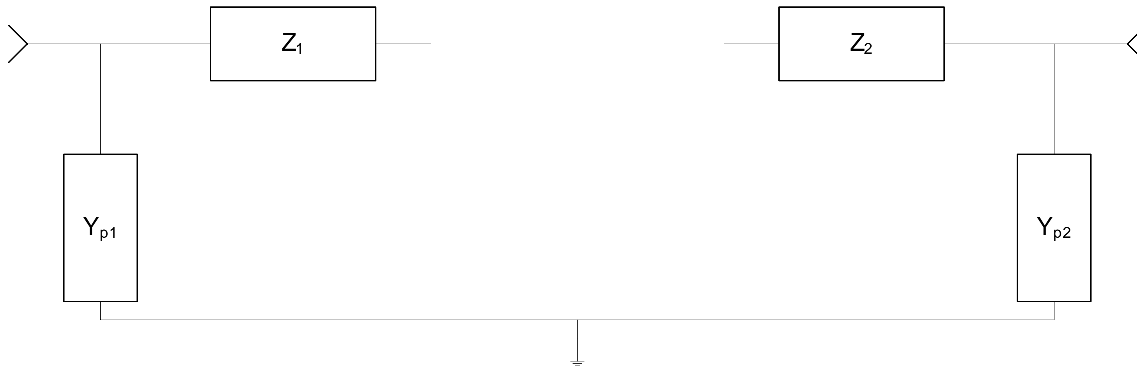

Figure 4 - Parasitics for open test structure

From the open test structure, we obtain the Y-parameters and the value of the parasitics Y_{p1} and Y_{p2} are found as

$$Y_{p1} = y_{11,open} + y_{12,open} \approx y_{11,open} \tag{1.1}$$

$$Y_{p2} = y_{22,open} + y_{12,open} \approx y_{22,open} . \tag{1.2}$$

where $y_{12,open}$ is neglected due to the negligible coupling between the ports. The next step is to determine the values of the impedance from the DUT feed-lines Z_1 and Z_2. Due to the capacitors small size, we have two options: a thru or a short test structure. First we will discuss the thru method. The thru test structure used for this fabrication is given in Figure 5. It is actually a transmission line test structure, since the thru test structure that was designed was erroneous and could not be used. The transmission line was used in its place to obtain measured data for the thru.

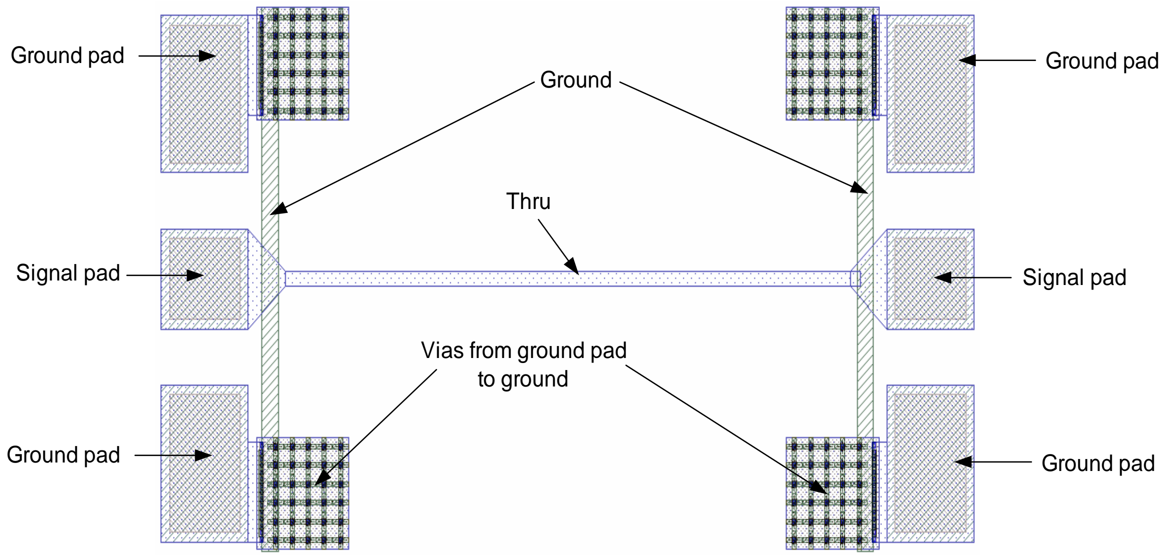

Figure 5 - Capacitor thru

Obviously, the layout of the “thru” line being used is not identical to the DUT interconnect line of Figure 2. However, we will see from the results that this still gives reasonably accurate de-embedding. The thru test structure should be identical to the open shown in Figure 3 with the exception that the transmission line continues through the open area where the DUT would be. A schematic showing the parasitics of the thru is given in Figure 6.

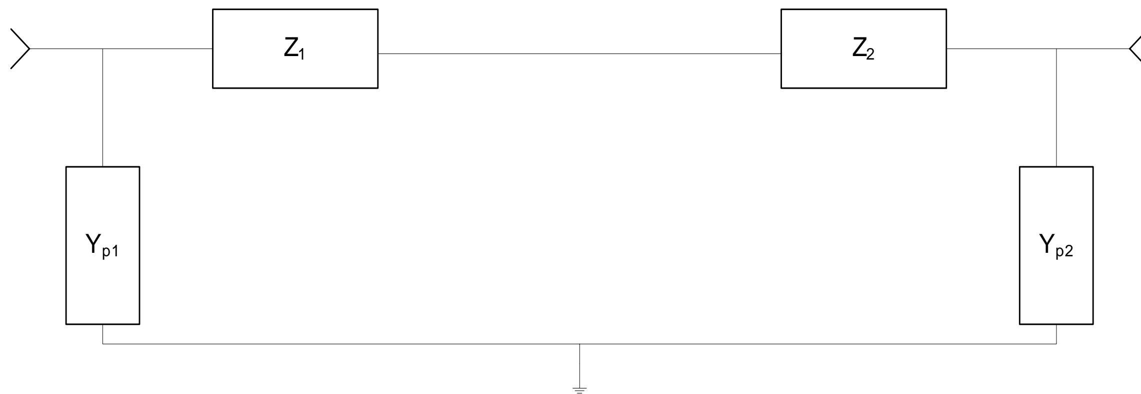

Figure 6 - Thru test structure parasitics

To determine the value for Z_1 and Z_2 using the thru, we measure the Y-parameters of the device and obtain Y_{12}. The impedance of Z_1 in series with Z_2 and the thru is equal to $-1/Y_{12}$. We can then get Z_1 and Z_2 as

$$Z_1 = Z_2 = \alpha\left(\frac{1}{2}\right)\left(\frac{-1}{y_{12,thru}}\right) \tag{1.3}$$

The variable α in equation (1.3) accounts for the length of the thru. We find α as

$$\alpha = \frac{length(Z_1 + Z_2)}{length(Z_1 + Z_2) + length(thru)}. \tag{1.4}$$

The above formula is exact when the width of the lines for the thru and the impedances Z_1 and Z_2 are the same as shown in Figure 5; otherwise, it is an approximate formula.

The short test structure for the capacitor is given in Figure 7. It is important to keep in mind where the reference planes for the device are located. This is not too important for the open structure, but for the short structure we must insert the short at this reference plane. If we insert it too close to the signal pad (away from the device), we include too much of the DUT feed-line in our de-embedded measurement, resulting in added inductance and loss to our de-embedded measurement.

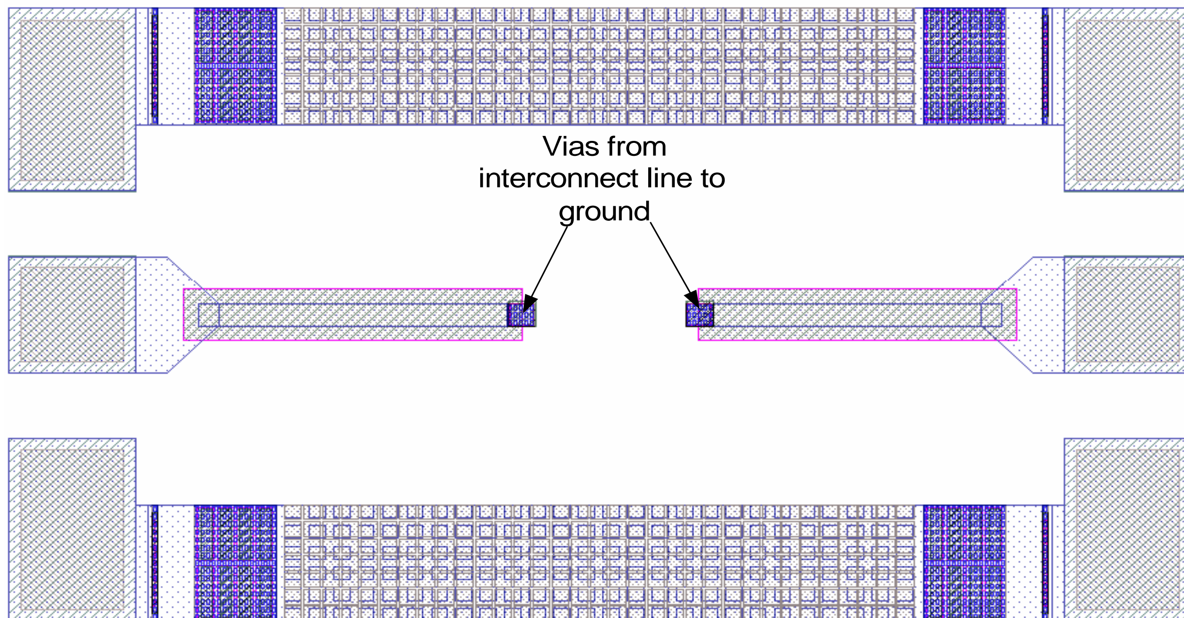

Figure 7 - Capacitor short

The squares at the end of the feed-lines represent vias to ground, as noted on the figure. The parasitics of the short structure are given in Figure 8. There are some losses and inductance (Z_3) in the vias as well as the return path from the vias to the ground pads. However, for the capacitor, they are ignored ($Z_3 \approx 0$)

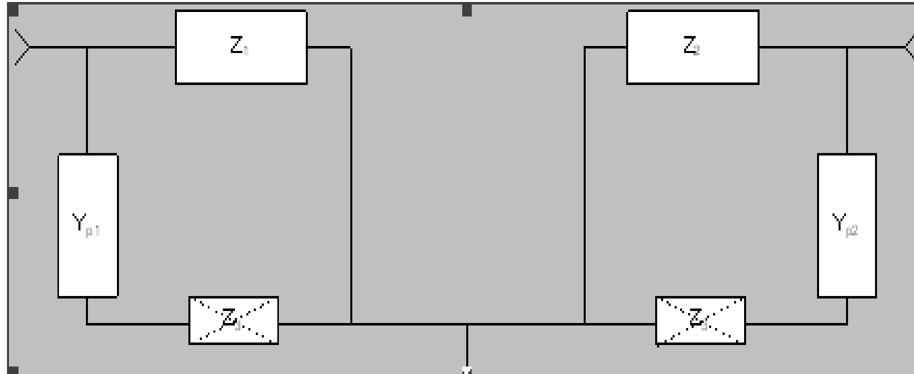

Figure 8 - Short structure parasitics

We calculate Z_1 and Z_2 from the measured port 1 and port 2 input impedances, Z_{11} and Z_{22}, and the previously calculated Y_{p1} and Y_{p2} (assuming Z_3=0):

$$Z_{11,short} = Z_1 // \frac{1}{Y_{p1}} \Rightarrow Z_1 = \frac{\left(Z_{11,short} / Y_{p1} \right)}{\left(\frac{1}{Y_{p1}} - Z_{11,short} \right)} \quad (1.5)$$

$$Z_{22,short} = Z_2 // \frac{1}{Y_{p2}} \Rightarrow Z_2 = \frac{\left(Z_{22,short} / Y_{p2} \right)}{\left(\frac{1}{Y_{p2}} - Z_{22,short} \right)} \quad (1.6)$$

1.2 Inductor Test Structure

Next we will apply the open/short method to an inductor test structure. The test structures as laid out are not correct, but they still give reasonable results. Corrected test structures will be shown as well, with simulated results to support their design. One obstacle with the inductors fabricated is that there is no metal ground plane (lossless deep trench used instead) beneath the inductor to put our short at the proper reference plane. This causes an error in the de-embedded inductance due to a shift in the reference plane towards the signal pads. The inductor test structure is given next.

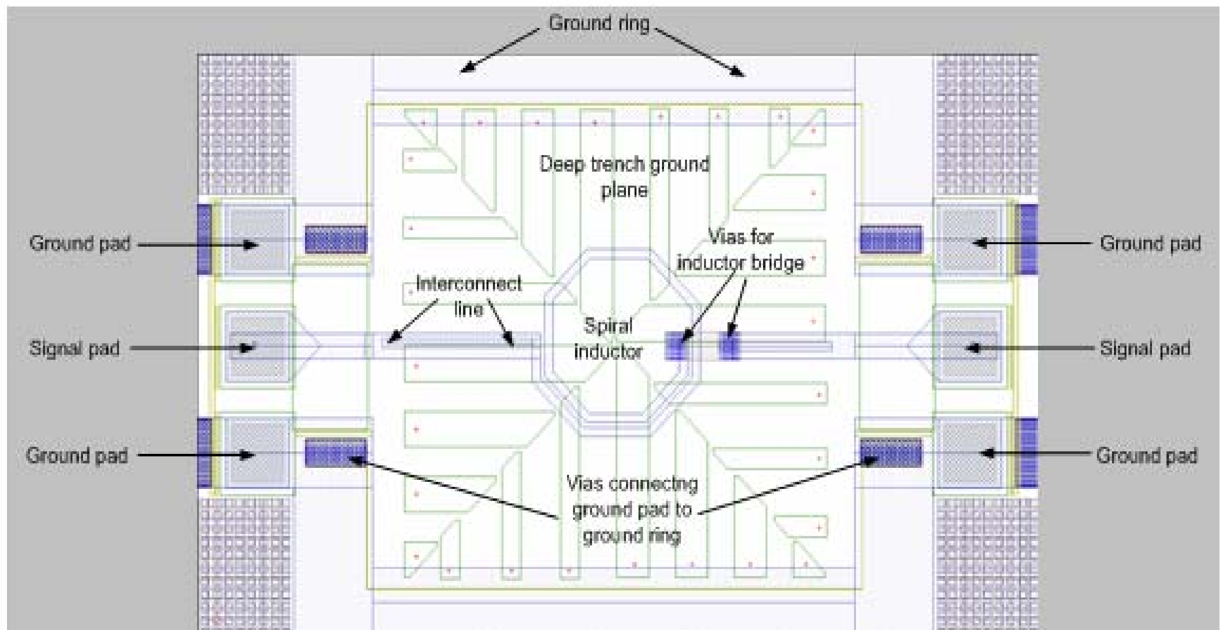

Figure 9 - Inductor test structure

The parasitics of the test structure are the same as for the capacitor, shown in Figure 1. The open test structure is given in Figure 10. The parasitics are the same as that shown in Figure 4. The parasitics Y_{p1} and Y_{p2} are calculated from the open in the same manner as for the capacitor.

$$Y_{p1} = y_{11,open} + y_{12,open} \approx y_{11,open} \quad (1.7)$$

$$Y_{p2} = y_{22,open} + y_{12,open} \approx y_{22,open} \quad (1.8)$$

The next step is to determine the values for Z_1 and Z_2. For the inductor, we use the short test structure as the thru is too long to be used accurately. The calculation for these parasitics is the same as for the capacitor. The inductor short is shown in Figure 11.

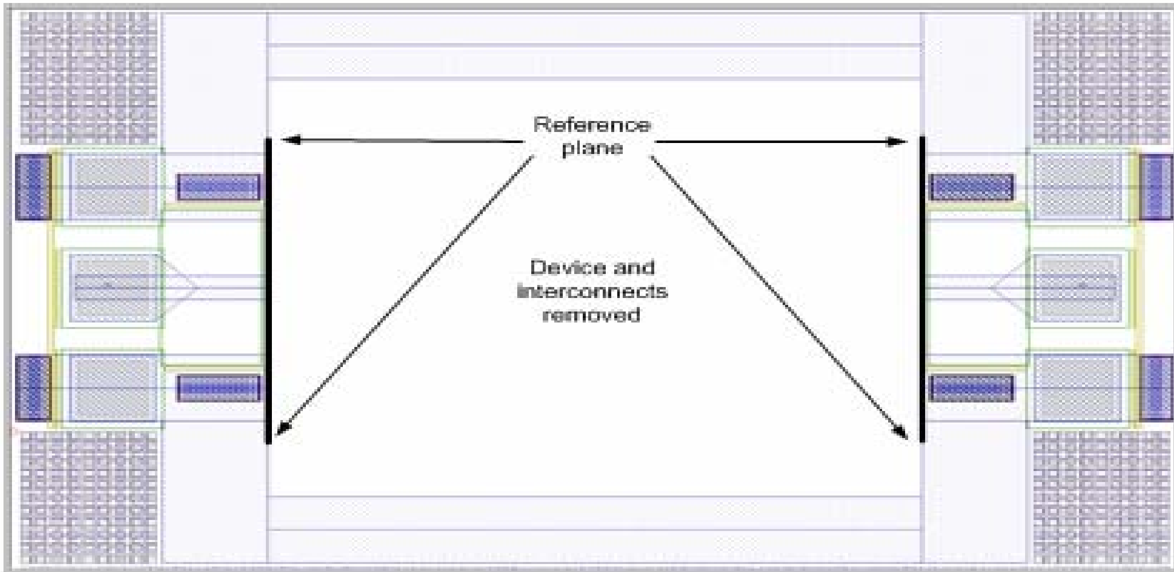

Figure 10 - Inductor open

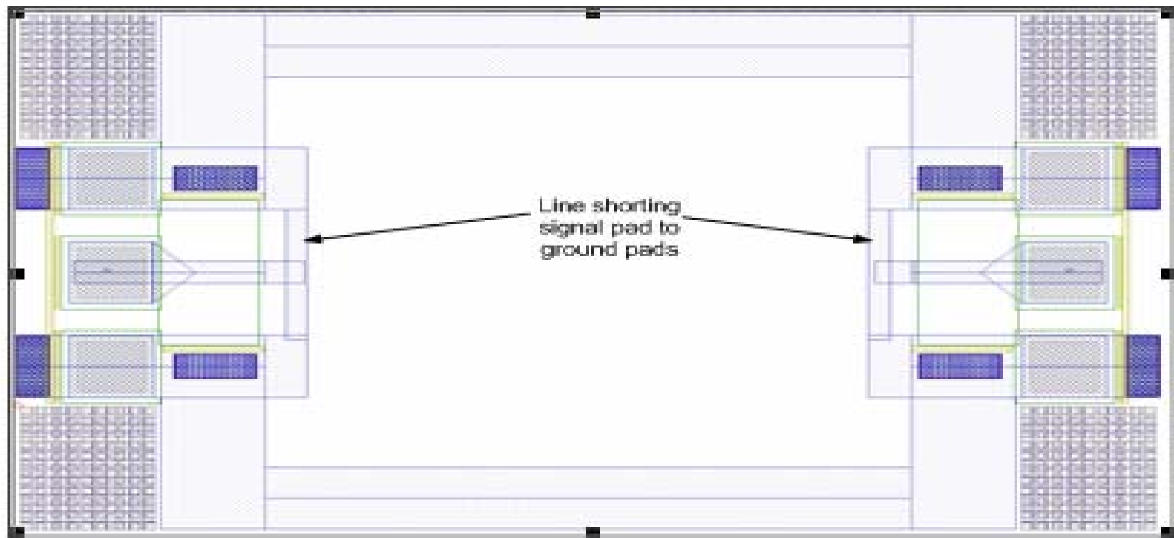

Figure 11 - Inductor short

As with the capacitor, we calculate Z_1 and Z_2 from the measured port 1 and port 2 input impedances, Z_{11} and Z_{22}, and the previously calculated Y_{p1} and Y_{p2}.

$$Z_{11,short} = Z_1 // \frac{1}{Y_{p1}} \Rightarrow Z_1 = \frac{\left(Z_{11,short} / Y_{p1} \right)}{\left(\frac{1}{Y_{p1}} - Z_{11,short} \right)} \tag{1.9}$$

$$Z_{22,short} = Z_2 // \frac{1}{Y_{p2}} \Rightarrow Z_2 = \frac{\left(Z_{22,short} \big/ Y_{p2} \right)}{\left(\frac{1}{Y_{p2}} - Z_{22,short} \right)} \tag{1.10}$$

If the technology allows, it would be better to use vias to short to ground instead of the bar across the pads shown in Figure 11. The length of the bar, and the current loop caused by it, introduces too much inductance and causes an error in our de-embedding. Also, if a conductive ground plane beneath the inductor is present, the vias should be placed at the DUT so that a proper reference plane is provided. If vias cannot be used, then a wider bar, inserted right after the pads is preferred as it introduces less impedance.

1.3 De-embedding the Parasitics

Now that we have determined the parasitics, the next step is to subtract their values from the raw measurement. The method is a simple two-step procedure and is the same for inductors and capacitors.

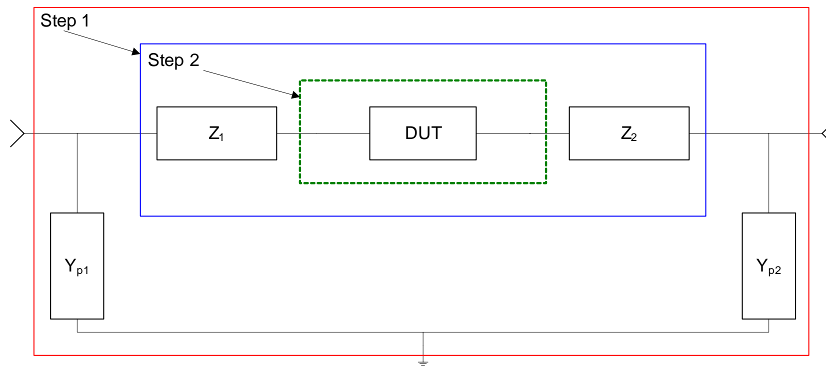

Figure 12 - 2-step de-embedding procedure

Step 1 de-embeds the parasitic pad coupling. Its calculation is given as

$$Y_A = Y_{meas} - \begin{bmatrix} Y_{p1} & 0 \\ 0 & Y_{p2} \end{bmatrix} \rightarrow Z_A \tag{1.11}$$

Step 2 de-embeds the DUT feed-lines and gives the final de-embedded measurement, Z_{DUT}. Its calculation is given as

$$Z_B = Z_A - \begin{bmatrix} Z_1 & 0 \\ 0 & Z_2 \end{bmatrix} \rightarrow Z_B = Z_{DUT} \tag{1.12}$$

Note that for the capacitor, a device that generally has small losses, the additional losses in Z_1 and Z_2 cause an error in the de-embedding. For this reason, we only subtract the imaginary part, the reactance of Z_1 and Z_2 in equation (1.12). The results for de-embedding the capacitor are given in Figures 13 and 14 using the open/short method. The effective capacitance and capacitor Q are shown first. We compare our de-embedded measurement (in blue) with the values generated by the process design kit (PDK) (in black).

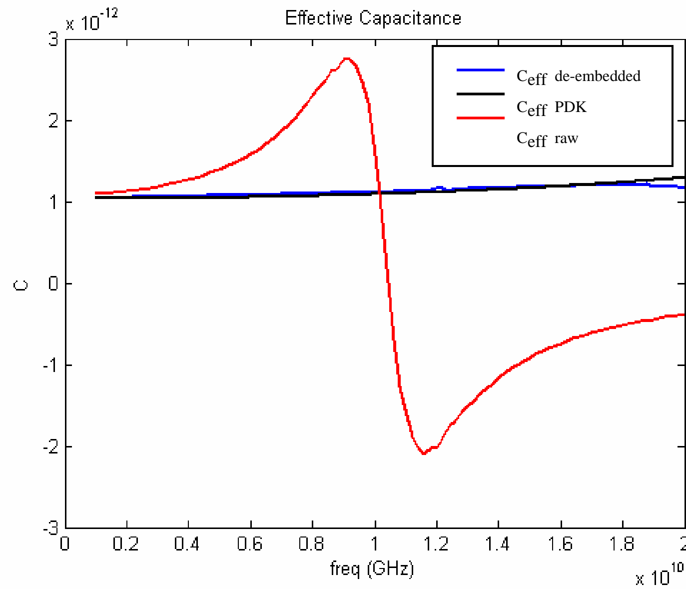

Figure 13 - Effective capacitance – capacitor open/short

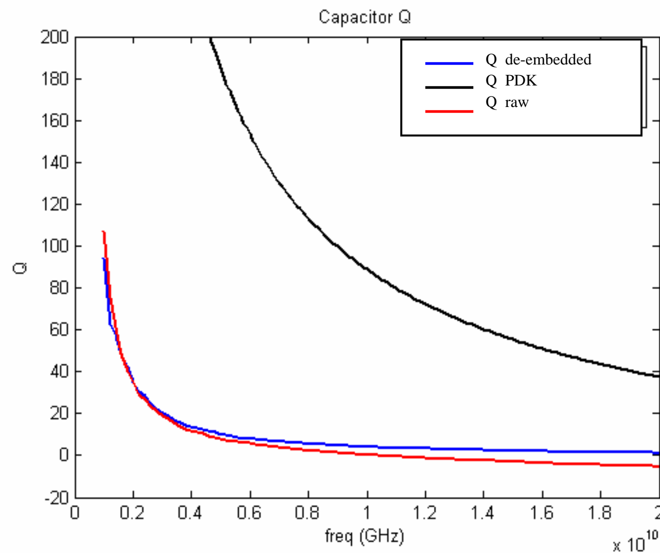

Figure 14 - Capacitor Q – capacitor open/short

As mentioned previously, the loss de-embedding is very difficult interdigitated capacitors due to the inherently low loss. Any error in the loss is magnified due to its small value. There is a slight improvement in Q visible in Figure 14, but it is small. The de-embedded S-parameters are given in Figure 15. Good agreement between the de-embedded measurement and the design kit is obtained

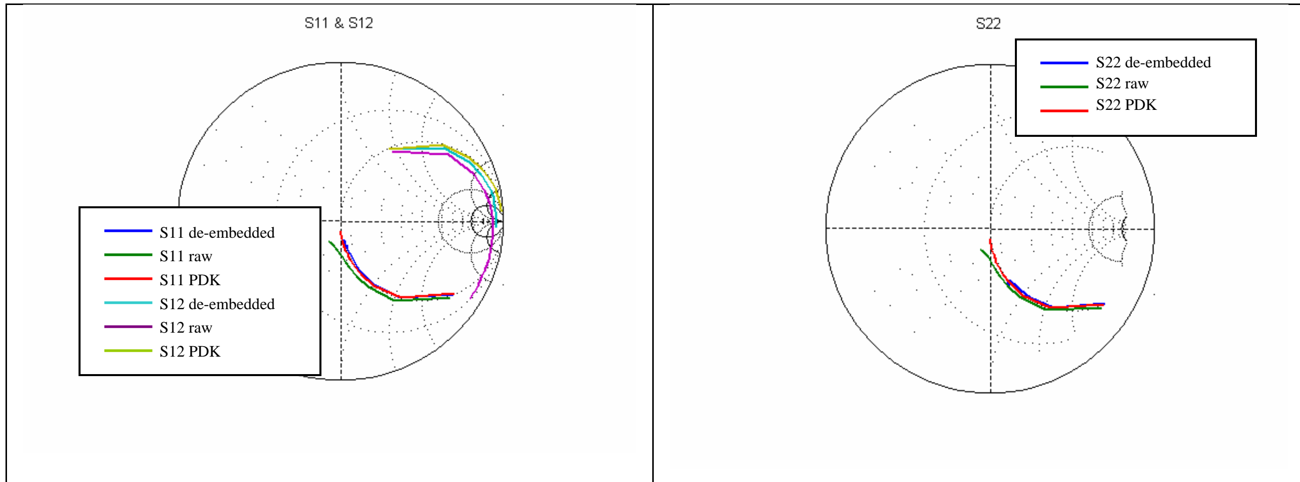

Figure 15 - S-parameters – capacitor open/short

Using the open/thru method for the capacitor provides slightly better results for the Q (see Figure 17) due to the lack of error introduced by the return path of the short. However, the effective capacitance is not as good (see Figure 16) as with the open/short, and the S-parameters are basically the same (see Figure 18).

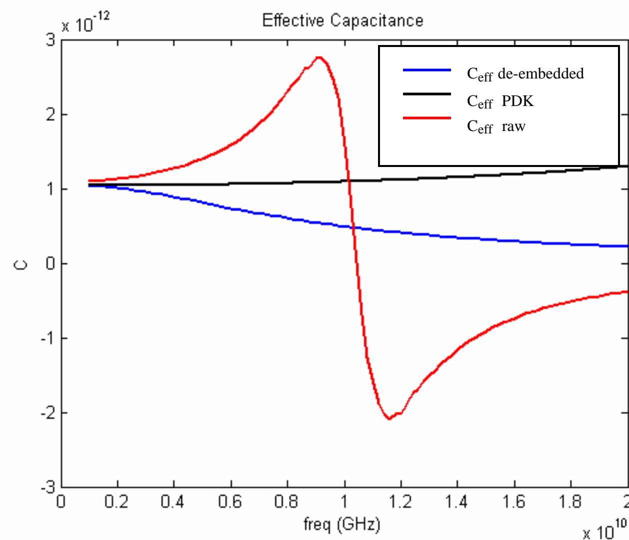

Figure 16 - Effective capacitance – capacitor open/thru

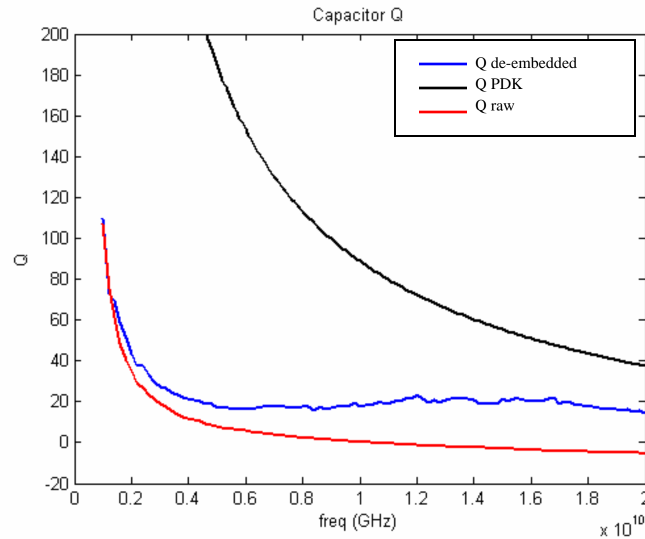

Figure 17 - Capacitor Q – capacitor open/thru

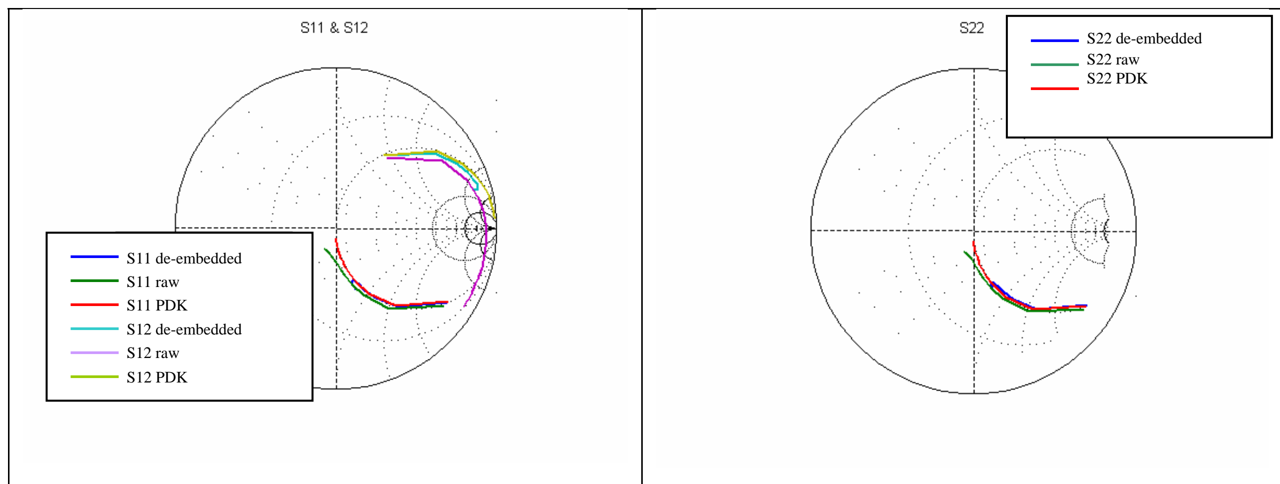

Figure 18 - S-parameters – capacitor open/thru

Our de-embedding of the inductor measured data did not turn out as well. This is due to the error in the layout of the short test structure, as well as the shift in reference plane due to the location of the short. For this type of inductor, there is little that can be done about the shift in reference plane due to the lack of a conductive ground plane beneath the inductor to form a short. The results are given in Figures 19 through 21.

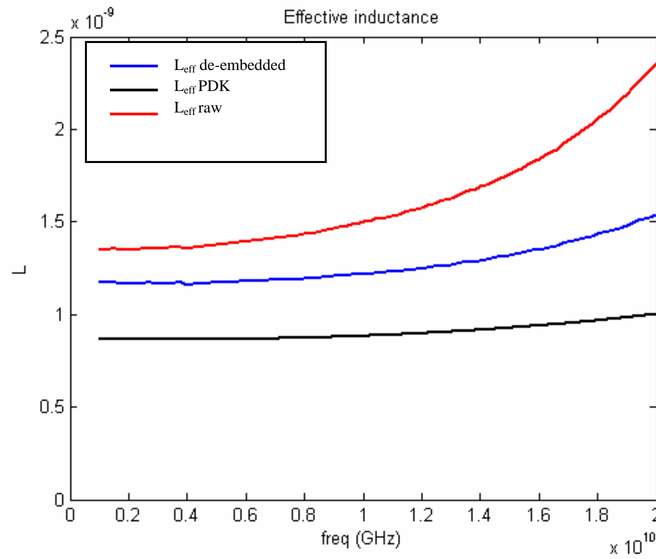

Figure 19 - Effective inductance - inductor open/short

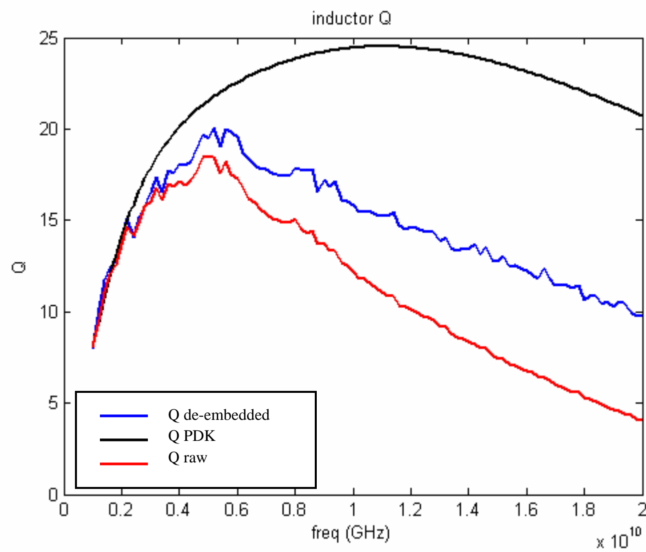

Figure 20 - Inductor Q - inductor open/short

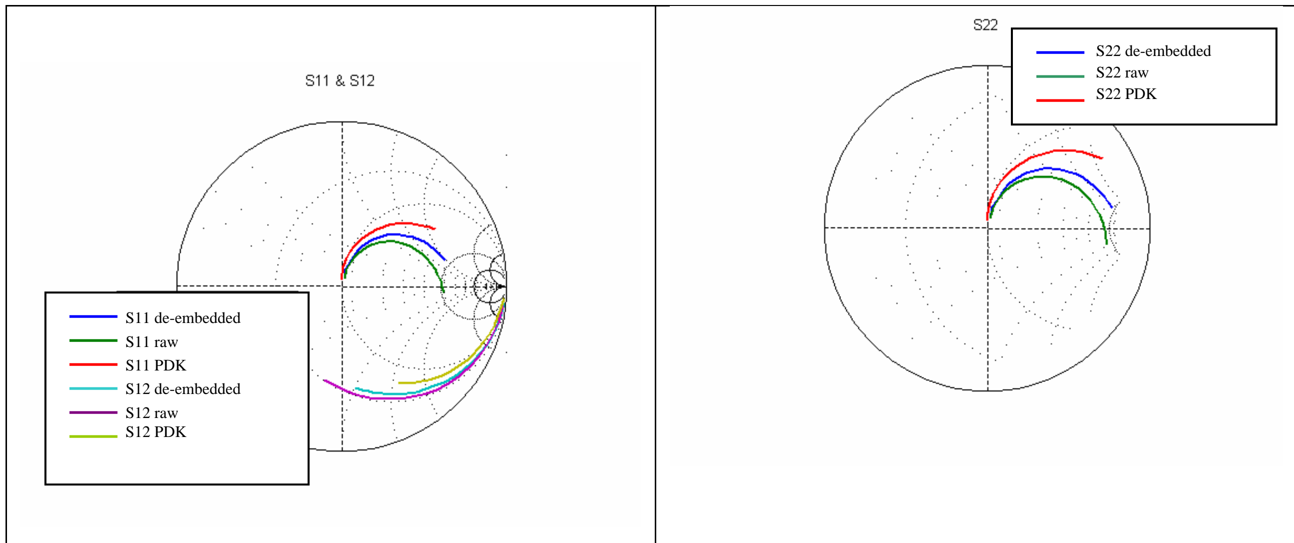

Figure 21 - S-parameters – inductor open/short

1.4 Improved Inductor Test Structures for Open/Short Technique

A suggested set of test structures for better inductor de-embedding will now be given. The modified test structures are given in Figures 22 through 24. The only change is in the short test structures. As mentioned in Section 1.2, the vias provide a better short because they introduce an impedance that is smaller than that introduced by the short bar across the GSG pads. If the technology does not allow vias as in Figure 24, then a line across the ground-signal-ground test pads can be used. As mentioned previously, the line should be as wide as possible to introduce the smallest impedance possible. Like the test structures used in Section 1.2, the reference plane will still be shifted because of the deep trench ground plane; however, the ideal values we will compare to will be arrived at from an ADS RF Momentum simulation that also has its reference plane shifted. This could have been done with the ideal values given above using the design kit if we used a model for a length of transmission line equal to the shift in reference plane.

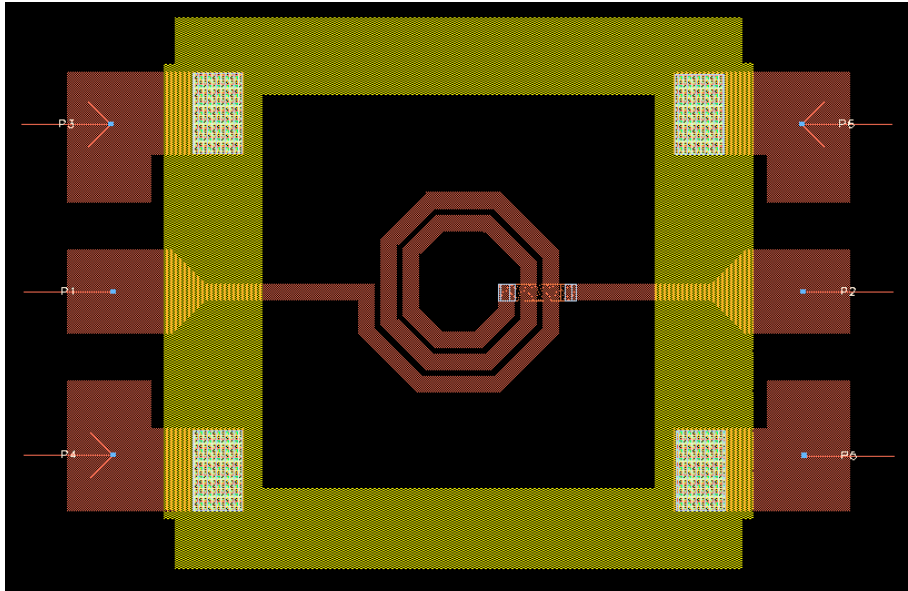

Figure 22 - Improved inductor test structure

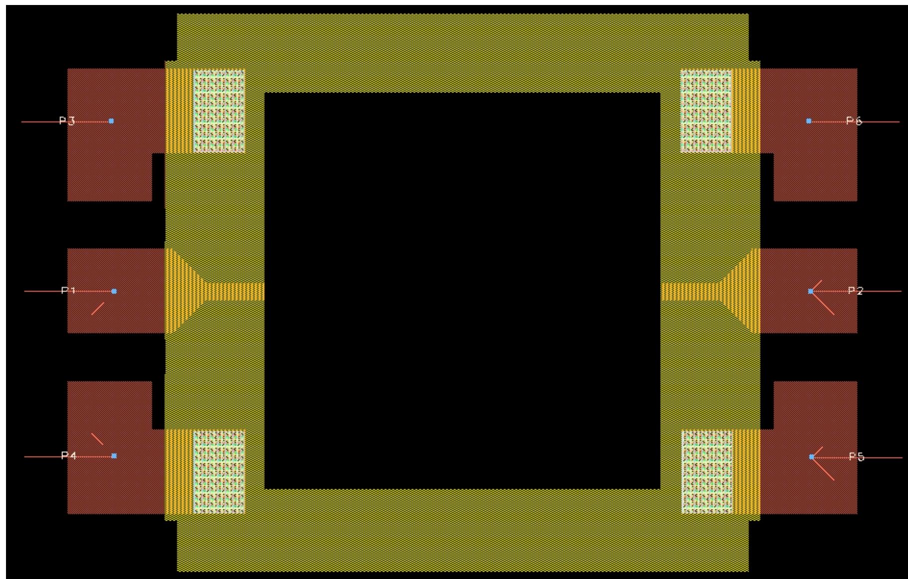

Figure 23 - Improved inductor open

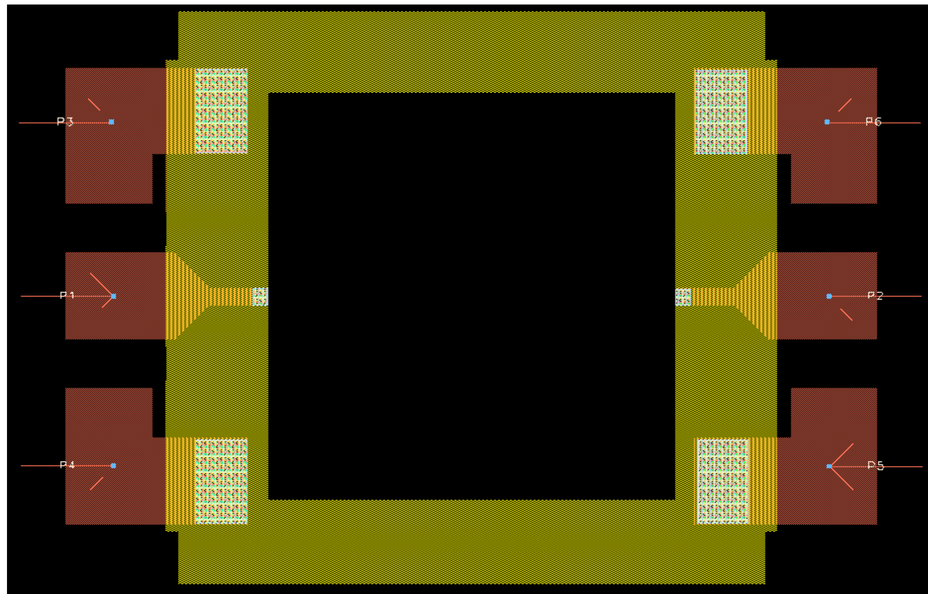

Figure 24 - Improved inductor short

Applying the de-embedding procedure, we get very good simulated results as shown in Figures 25 - 27. The effective inductance is better compared to the method used in Section 1.2, but this is only due to the shift in reference plane being accounted for in the comparison. A large improvement in de-embedding the loss is achieved. This is because the vias in the short test structure of Figure 24 introduce much less impedance than the short method used in Figure 11.

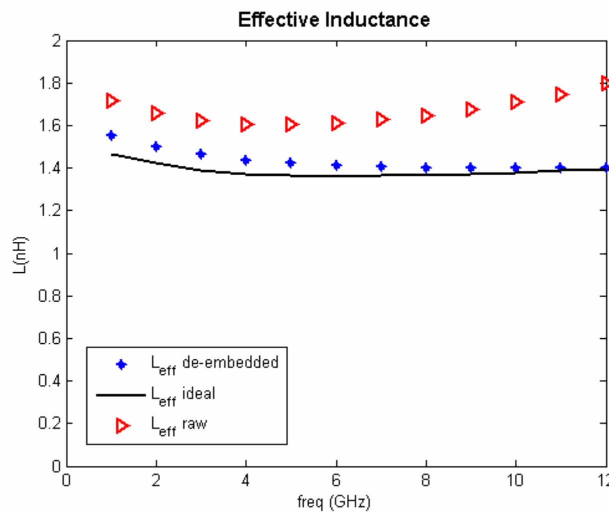

Figure 25 - Effective inductance - improved inductor open/short

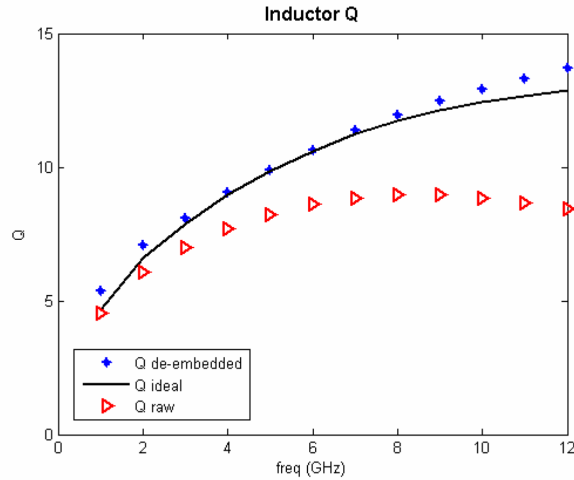

Figure 26 - Inductor Q - improved inductor open/short

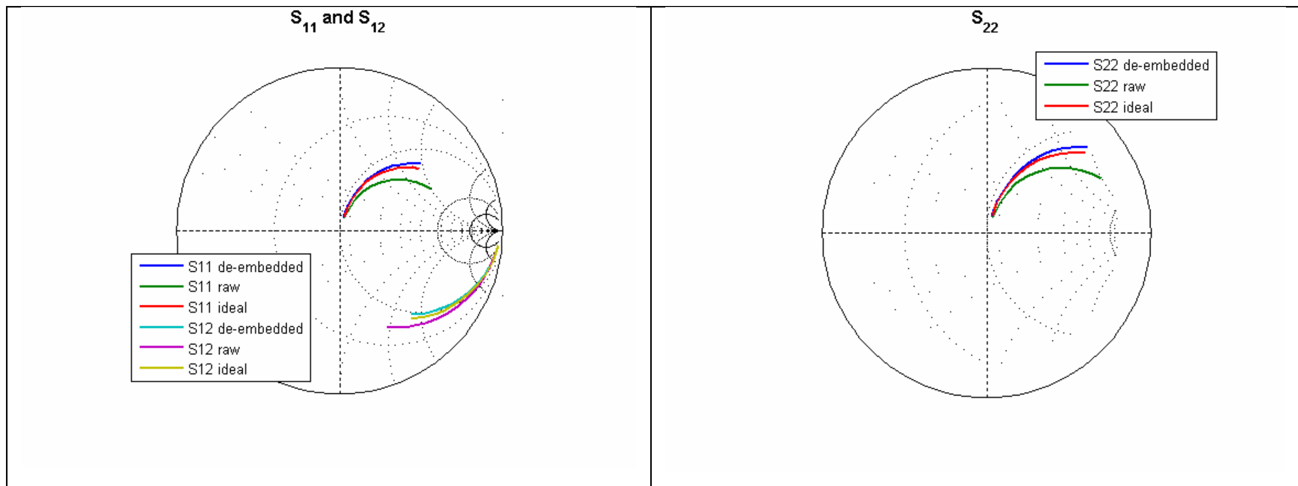

Figure 27 - S-parameters - improved inductor open/short

Another option for accurate de-embedding is the use of coplanar waveguide tapers from the pads to the DUT interconnects. This results in the parasitic impedance of the device feed-lines being negligible, making only the use of open de-embedding necessary. Some processes do not allow traces at arbitrary angles, making this option process-dependent.

Chapter 2 Conclusion

In this report, a rigorous investigation of the de-embedding of RF inductors and capacitors was presented. The typical parasitic impedances present in an RF test structure were discussed. Basic knowledge of these parasitics allows the designer to effectively adjust the test structures to account for any limitations imposed by the technology being used. Some technologies allow traces to be etched at arbitrary angles, making it possible for a coplanar waveguide interconnect to be used, thus minimizing the interconnect impedance.

Chapter 3 Bibliography

[1] E. P. Vandamme, D. M. M.-P. Schreurs, and S. van Dinther, "Improved Three Step De-Embedding Method to Accurately Account for the Influence of Pad Parasitics in Silicon On-Wafer RF Test-Structures," IEEE Trans. Electron Devices, vol. 48, pp.737-742, Apr. 2001.