

**REPORT OF  
DEPARTMENT OF DEFENSE  
ADVISORY GROUP ON ELECTRON DEVICES**

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**SILICON-BASED  
MULTIMATERIAL TECHNOLOGY**

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## PREFACE

In the U.S., Japan and elsewhere, the race is on to find a practical replacement for the conventional silicon integrated circuit, which is beginning to run out of steam as a means of reaching ever-higher plateaus of operating speed and circuit density. Showing great promise as a possible replacement are silicon-based composites which combine the well-known attributes of silicon with the higher speed and other special capabilities of gallium arsenide, germanium, sapphire, and other materials. The purpose of this study was to examine this area of technology in terms of its potential applicability to future electronic systems, both commercial and military, and to help OUSDA formulate an appropriate investment strategy for the area.

The study was performed by DoD's Advisory Group on Electron Devices—specifically by AGED's Working Group B, which is responsible for coordinating microelectronic device development for DoD. The conclusions and recommendations that emerged stem mainly from: (1) the information presented at AGED's 11-12 October 1989 "Special Technology Area Review" (STAR) on Silicon-Based Multimaterial Technology, and (2) continuing review of this area by the Working Group since that time.

The editor wishes to express his sincere appreciation to all the contributors—identified on the next page—for their kind assistance and cooperation. This applies particularly to Dr. Michael Strocio of the U.S. Army Research Office, principal organizer of the above-mentioned STAR. In addition, the support and encouragement of Dr. John MacCallum, ODDRE/R&AT/ET (Electronic Sensors and Devices), and Mr. E.C. Urban, DoD Technology Analysis Office, have been essential to this effort.

*Warner Kramer  
Palisades Institute  
for Research Services, Inc.  
(AGED Secretariat)  
Arlington, VA*

## CONTRIBUTORS

**Dr. John M. MacCallum, Jr.**

*Executive Director, Advisory Group on Electron Devices  
ODDDRE/R&AT/ET, The Pentagon  
Washington, DC*

**Dr. William G. Howard, Jr.**

*Chairman, Working Group B  
National Academy of Engineering  
Washington, DC*

**Dr. R. M. Burger**

*Semiconductor Research Corp.  
Research Triangle Park, NC*

**Dr. G. Cullen**

*David Sarnoff Research Center  
Princeton, NJ*

**Dr. A. M. Goodman**

*Office of Naval Research  
Arlington, VA*

**Prof. J. S. Harris**

*Department of Electrical Engineering  
Stanford University  
Stanford, CA*

**Prof. N. Holonyak, Jr.**

*Department of Electrical Engineering  
University of Illinois  
Urbana, IL*

**Dr. J. M. Killiany**

*Naval Research Laboratory  
Washington, DC*

**Dr. I. Lagnado**

*Naval Ocean Systems Center  
San Diego, CA*

**Dr. W. Lynch**

*Research Triangle Park, NC*

**Dr. J. Phillips**

*AT&T Bell Laboratories  
Murray Hill, NJ*

**Mr. R. Reitmeyer**

*U.S. Army LABCOM  
Fort Monmouth, NJ*

**Dr. D. Shaw**

*Texas Instruments, Inc.  
Dallas, TX*

**Dr. W. Shedd**

*Air Force RADC/ESR  
Hanscom AFB, MA*

**Dr. S. Shichijo**

*Texas Instruments, Inc.  
Dallas, TX*

**Dr. M. Stroschio**

*U.S. Army Research Office  
Research Triangle Park, NC*

**Dr. J. Szedon**

*Westinghouse Science & Technology Center  
Pittsburgh, PA*

**Dr. A. F. Tasch**

*University of Texas  
Austin, TX*

**Prof. K. L. Wang**

*School of Engineering & Applied Science  
UCLA  
Los Angeles, CA*

**Mr. R. M. Werner**

*Air Force WRDC/ELA  
Wright-Patterson AFB, OH*

## CONTENTS

	<u>Page</u>
<b>I. EXECUTIVE SUMMARY</b> .....	1
<b>II. GENERAL DISCUSSION</b> .....	4
A. Introduction and Summary .....	4
B. Military Interest .....	5
C. Extending Conventional IC Capabilities .....	5
D. Tomorrow's Materials: Requirements and Opportunities .....	7
E. Epitaxy: Key to Multimaterial Devices .....	9
F. MOCVD Consortium: An Example of Government-Industry Cooperation .....	10
<b>III. REVIEW OF SPECIFIC TECHNOLOGY AREAS</b> .....	11
<b>A. Gallium Arsenide-on-Silicon Device Technology</b> .....	11
1. Introduction .....	11
2. Existing Problems .....	12
a. Dislocation Density and Other Lattice-Mismatch-Induced Defects .....	12
b. Thermal Incompatibilities .....	14
c. Antiphase Domains .....	14
d. Cross-Doping, Defect Propagation and Other Process-Induced Defects .....	14
e. Limited Applicability .....	15
3. GaAs/Si "Microelectronics" Activity .....	15
4. Other Device Activity .....	17
5. Size and Distribution of Present Effort .....	19
6. Summary .....	20
<b>B. Germanium/Silicon Device Technology</b> .....	21
1. Introduction .....	21
2. Growth of Ge/Si Device Structures .....	21
3. Ge/Si Heterojunction Bipolar Transistor (HBT) .....	22
4. Size and Distribution of Present Effort .....	23
5. Summary .....	25
<b>C. Silicon-on-Insulator (Including Silicon-on-Sapphire) Technology</b> .....	25
1. Introduction .....	25
2. Background .....	26
3. Competing SOI Approaches .....	27
4. SOS Technology .....	28
5. SIMOX Approach .....	29
6. Bonded Wafers .....	30
7. ZMR/ISE Material .....	31

CONTENTS (CON'D)

	<u>Page</u>
8. Examples of Current SOI/SOS Device Activity .....	32
a. 64K Static RAMs .....	32
b. Bipolar Devices .....	32
c. Higher-Frequency Silicon Devices .....	32
d. "Title 3" SOS Program .....	34
e. Radiation-Hardened Power Integrated Circuits .....	34
f. SOI and GaAs .....	34
9. Government-Sponsored SOI/SOS Program .....	35
10. Worldwide Activity .....	36
11. Summary .....	36
<b>D. Fluoride Technology .....</b>	<b>37</b>
1. Introduction .....	37
2. Background .....	37
a. Lattice Mismatch .....	38
b. Chemical Mismatch .....	38
c. Thermal Expansion Mismatch .....	39
d. Ionicity Problem .....	39
e. Growth Asymmetry .....	39
3. Potential Applications .....	39
a. Buffer Layers .....	39
b. 3-D Epitaxial Heterostructures .....	40
c. Other New Multimaterial Device Structures .....	40
d. Dielectric Isolation .....	40
e. Semiconductor Passivation .....	40
f. Electron Beam Resists .....	40
g. Superconductor Applications .....	41
4. Review of Recent Activity .....	41
a. Fluorides as Buffer Layers .....	41
b. Si Grown on CaF <sub>2</sub> .....	41
c. Growth of Other Semiconductors on F/Si Layers .....	42
5. Size and Distribution of Current Effort .....	43
6. Summary .....	45
<b>IV. CONCLUSIONS AND RECOMMENDATIONS .....</b>	<b>46</b>
<b>ATTACHMENTS</b>	
A. STAR Agenda	
B. STAR Goals and Guidelines	

CONTENTS (CON'D)

Tables

	<u>Page</u>
1. Heteroepitaxial Integration vs Hybrid Interconnection .....	8
2. Funding for GaAs/Si Multimaterial Research .....	19
3. GaAs/Si Technology: Principal Research Centers .....	20
4. Funding for Silicon-Based Column IV Multimaterial Research .....	23
5. Leaders in Column IV Heteromaterial Research .....	24
6. Demonstrated SOI Circuit Capability .....	32
7. SOI Programs .....	35
8. Funding plans for SOI/SOS Materials Research .....	35
9. Level of Activity in SOI/SOS .....	36
10. Fluorides and Associated Compatible Semiconductors .....	38
11. Linear Expansion Coefficients .....	39
12. U.S. Effort in Epitaxial Fluorides .....	43
13. Japanese Effort in Epitaxial Fluorides .....	44
14. European Effort in Epitaxial Fluorides .....	44
15. DoD Funding of Fluoride Research .....	45

Figures

1. Further downscaing of conventional bulk silicon integrated circuits will cease to be a viable option by the year 2000. ....	6
2. Co-integration of multiple materials could eventually lead to a single-chip focal plane imager. ....	8
3. Monolithic integration of GaAs on silicon. ....	11
4. Curve showing progress in reducing dislocation density in GaAs-on-Si heterostructures. ....	13
5. Monolithic co-integration of GaAs MESFET and Si CMOS structures (developed by TI). ....	16
6. MOCVD $Al_xGa_{1-x}$ p-n QWH on MBE GaAs-Si ( $L_z \approx 125\text{\AA}$ ). ....	18
7. Cross-section of a heterojunction bipolar transistor. ....	21
8. Schematic cross-section of two transistors comprising a CMOS/SOI inverter. ....	26
9. Frequency range of present Si and GaAs technologies. ....	33
10. Cross-section of Westinghouse "MICROX" transistor structure. ....	33
11. Example of an SIO-based power IC co-integrated with logic circuitry. ....	34
12. Si/CaF <sub>2</sub> /Si FET built by Tokyo Institute of Technology. ....	42

## I. EXECUTIVE SUMMARY

Although bulk silicon continues to be the preponderant semiconductor material used in electronic devices and systems for both commercial and military applications, there are many applications for which it is inadequate. Among these are light emitting devices (both coherent and incoherent), long wavelength detectors and arrays, high temperature applications, extremely high frequency digital and analog applications, and use in the most demanding radiation environments. To meet these needs, other materials must be used either alone or in combination with silicon. Although the use of other materials with silicon is usually easiest to implement in a hybrid configuration (interconnecting separate devices), optimal performance, reliability, and cost/benefit are usually achieved only in fully integrated configurations (including silicon-based multimedia technology involving single or multiple epitaxial depositions). These heteroepitaxially integrated configurations typically require extensive processing and fabrication research and development (R&D) efforts. Thus, military system needs must be considered a strong driver for integrated multimedia technology R&D, to the extent that those needs can be met only in this way.

Specifically, four classes of heteroepitaxially integrated structures were considered in this study:

- Gallium arsenide-on-silicon (GaAs/Si) structures capable of integrating optoelectronic, microwave and conventional digital logic circuits on a single substrate.
- Column IV engineered materials capable of duplicating electronic and optical capabilities previously available only from compound (III-IV and II-VI) semiconductors.
- Silicon-on-sapphire (SOS) and other silicon-on-insulator (SOI) structures for enhanced radiation hardening of integrated circuits and high-voltage, low-leakage isolation.
- Deposited fluoride materials capable of providing interlayer insulators for three-dimensional device structures.

Several associated areas were also examined during the course of the study, including:

- Silicon epitaxial processes that take place at temperatures far lower than those usually required to produce silicon and other semiconductor layers of high quality.
- New directions and requirements in materials research needed for tomorrow's nanoelectronic devices.

Based on information gathered at several meetings dealing with this topic—including a "Special Technology Area Review" (STAR) held in October 1989—plus numerous subsequent discussions and other research, the following conclusions and recommendations (unprioritized) have emerged from this study:

1. GaAs/Si structures may provide a critical element in future optoelectronic and electronic systems. Devices made using such heterogeneous structures may open the way to faster circuit switching times, forms of integration not achievable by other, more conventional means, and new device functions. To realize these advances, research and exploratory



development efforts must emphasize a variety of approaches for improving the materials properties of GaAs films grown on Si. Full exploitation of GaAs/Si technology requires discovery of means for reducing the density of dislocations produced as a result of the inherent lattice mismatch at the GaAs/Si interface from approximately  $10^6$  to  $10^4$  defects/cm<sup>2</sup>. In short, GaAs/Si structures may open the way to enormous payoffs in electronics and optoelectronics integration if improved materials properties can be realized. The findings of this study indicate that progress is being made, as measured in terms of laser device performance. Other data presented indicate that selective deposition of GaAs islands on Si may be a more likely choice for deposited devices. Work on this technology is showing promising results and should be continued at current levels of effort (approximately \$1.6M per year).

2. High performance silicon-germanium (Column IV) devices are possible using heterostructures to modify band structures (for lower effective mass, improved mobility, etc.) or abrupt heterojunction interface structures (useful in heterojunction bipolar transistors) that have properties similar to those previously available only in compound semiconductor materials. The possibility of using Column IV technology to replace devices made using more exotic compound materials can ease processing problems in fabricating compatible microwave and optical devices (such as high efficiency photodetectors) on the same chip with conventional integrated circuit devices. Logic devices constructed from these heterostructured materials have speed-power performance beyond that attainable with conventional silicon devices. One heterojunction transistor development project has already demonstrated Si-Ge HBT's with cutoff frequencies of 75 GHz. Development of Si-Ge technology for fabrication of strained-layer quantum-well and other superlattice devices also looks promising. Increased research in this area should be encouraged—that is, the current rate of approximately \$3.5M per year should be raised to \$4.5M.
3. The study produced no clear resolution among the primary developmental SOI activities: BE (bond and etch), ZMR and SIMOX. SOS technology is still the best available radiation-hardened integrated circuit technology for many critical military applications; however, SOS remains more expensive than conventional (bulk silicon) processes—a barrier to its attracting wide commercial interest. The successful completion of any of the alternative SOI developments considered during this study would likely result in alternative device technologies to replace SOS technology in the long run for cost and flexibility reasons. Work in SOI technologies should continue at present levels—that is, at approximately \$4.5M per year.
4. The full potential of fluoride-on-silicon semiconductor technology is unknown but studies to date indicate that fluorides are more likely to be useful as relative passive layers than as active layers. Deposited fluoride materials together with metals and semiconductors may provide performance and density improvement alternatives to simple device shrinking (through nanolithography) and avoid voltage scaling problems. As these fluoride materials are at a primitive state of development, work should be continued at a modest level—approximately \$500K, up from the current \$200K per year—to sustain further development for evaluation.

5. Deposition technology is undergoing substantial improvements with the development of low-temperature epitaxy and remote plasma technologies. The potential impact of these developments on low-temperature processing of integrated circuits is substantial, as it would allow use of material combinations not now possible with processes requiring higher temperatures. In addition, defects induced by thermal cycling during fabrication can be substantially reduced. Work in this area is making good progress and should be continued.
6. The study did not cover alternative insulator materials or deposited ferroelectric and ferromagnetic materials (covered in an earlier Nonvolatile Memory STAR). New dielectric materials for denser DRAMs were also not considered, nor were materials treated in earlier STARs such as SiC and deposited diamond films. The recommendations of earlier STARs stand.
7. Multimaterial research can be advanced more rapidly through synergistic combination of both laboratory experiments and simulation techniques. Existing computer simulation is sufficiently well developed to predict characteristics of many heterostructures before they are fabricated.
8. Manufacturability of the deposition technologies being developed must be kept in mind early in the development activity—and certainly must be addressed before the technology is committed to high volume applications. Research activities in this process development area should look forward to equipment development options necessary to carry out the materials deposition processes with production process controls. Attention should especially be focused on process margins, throughput, impurity control and general compatibility with other process steps.
9. In order to ensure the most effective possible transfer of these new materials technologies, a strong effort should be made to disseminate the results of DoD-supported research—as well as an appreciation of the application potential of those results—to commercial and defense device producers. The Advisory Group recommends that, in addition to reliance on the open literature and regular conferences, there be a series of research technology transfer conferences put on by DoD or an independent organization, such as SRC, to allow open discussion of the results of these Si-based multimaterial research efforts.
10. Stability of funding is a critical issue. A sustained, high-quality effort of modest size in these mixed material technologies, given their fabrication-intensive nature, will bear better results than research at a higher funding level that is periodically stopped and restarted. It is essential that planners of future development programs keep this in mind.

## **II. GENERAL DISCUSSION**

### **A. Introduction and Summary**

The purpose of this study was to review the state of the art of silicon-based multimaterial technology, determine its importance for future weapons systems, and, based on that determination, help DoD formulate an appropriate investment strategy for that area. To gather the necessary information, the Advisory Group on Electron Devices—specifically, AGED's Working Group B (Microelectronics)—convened a "Special Technology Area Review" (STAR) on this topic in October 1989 (see Attachments A and B), at which experts from industry, academia and government presented their views on current and projected developments in key areas of that technology. Based on the information presented, subsequent discussions and other inputs, the Working Group has concluded that these silicon-based multimaterial technologies promise to provide both revolutionary and evolutionary changes in digital microcircuit device performance. Additional benefits to microwave and optoelectronic devices also are likely, but those device areas were not as thoroughly considered during the course of this study.

Specifically, the following four technology areas were examined:

- Gallium arsenide-on-silicon structures capable of integrating optoelectronic, microwave and conventional digital logic circuits on a single substrate.
- Column IV engineered materials capable of duplicating electronic and optical capabilities previously available only from compound (III-IV and II-VI) semiconductors.
- Silicon-on-sapphire and other silicon-on-insulator structures for enhanced radiation hardening of integrated circuits and high-voltage, low-leakage isolation.
- Deposited fluoride materials capable of providing interlayer insulators for three-dimensional device structures.

A number of associated areas also were examined during the course of this study, including:

- Silicon epitaxial processes that take place at temperatures far lower than those usually required to produce silicon and other semiconductor layers of high quality.
- New directions and requirements in materials research needed for tomorrow's nanoelectronic devices.

The above areas are discussed in detail in Section III. For each area, the salient technological issues are analyzed, centers of excellence identified, and current level of direct DoD support is specified. The Working Group's overall conclusions and recommendations are given in Section IV.

## **B. Military Interest**

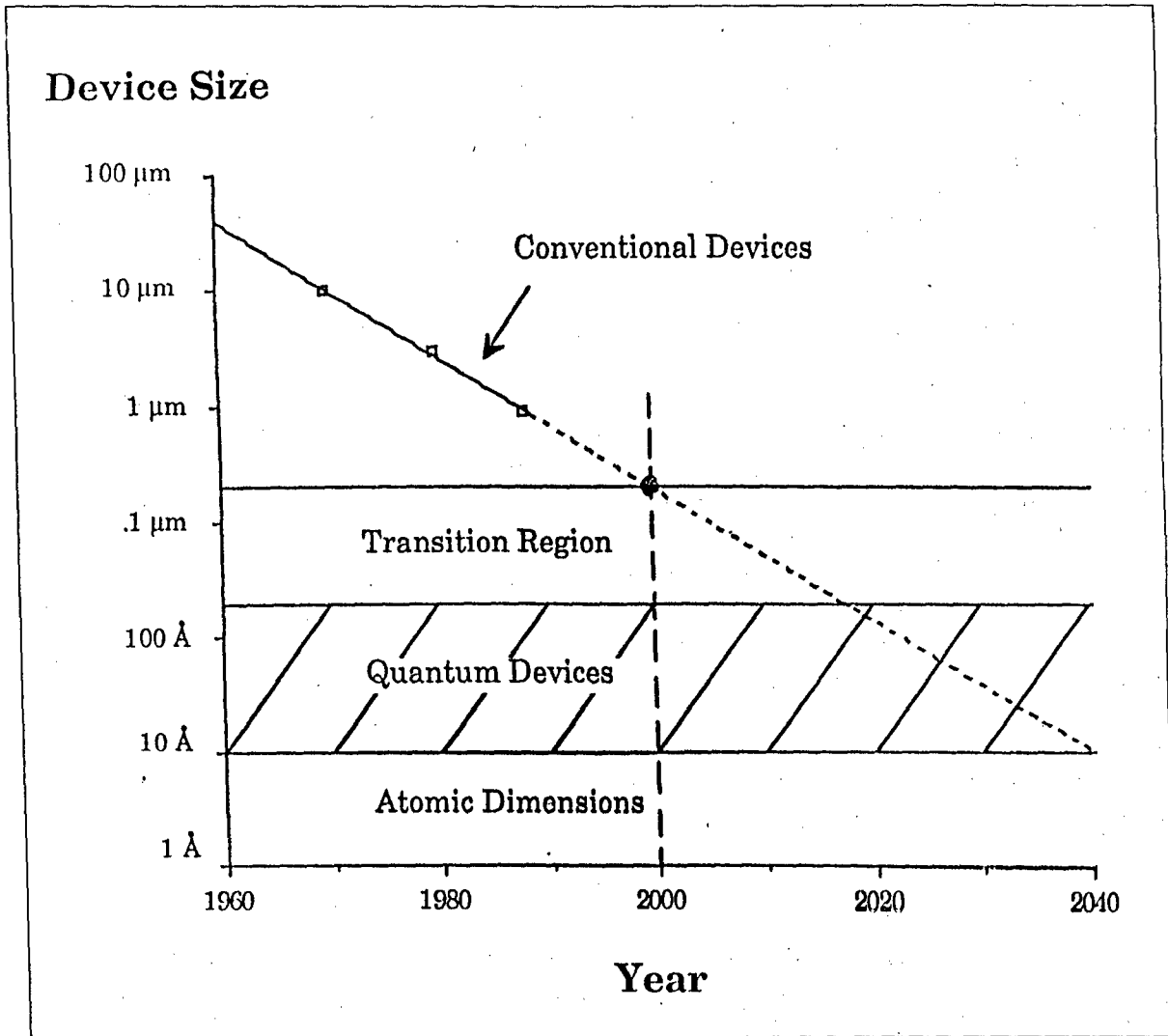
Of the several semiconductor materials employed today, silicon is used in the vast majority of solid state electronic devices, particularly monolithic integrated circuits (ICs). Although other semiconductor materials such as gallium arsenide (GaAs) may be theoretically superior in speed and a few other respects, silicon is unmatched in the ease with which it can be grown and processed and in its ability to satisfy, at minimum cost, all but the most stringent performance requirements. As a result, silicon has become the technology of choice within the semiconductor industry, as well as within DoD, and a tremendous body of knowledge bearing on silicon microelectronics has been developed by both U.S. and foreign (particularly Japanese) chipmakers.

Although bulk silicon continues to be the preponderant semiconductor material used in electronic devices and systems for both commercial and military applications, there are many applications for which it is inadequate. Among these are light emitting devices (both coherent and incoherent), long wavelength detectors and arrays, high temperature applications, extremely high frequency digital and analog applications, and use in the most demanding radiation environments. To meet these needs, other materials must be used either alone or in combination with silicon. Although the use of other materials with silicon is usually easiest to implement in a hybrid configuration (interconnecting separate devices), optimal performance, reliability, and cost/benefit are usually achieved only in fully integrated configurations (including silicon-based multimedia technology involving single or multiple epitaxial depositions). These heteroepitaxially integrated configurations typically require extensive processing and fabrication research and development (R&D) efforts. Thus, military system needs must be considered a strong driver for integrated multimedia technology R&D, to the extent that those needs can be met only in this way.

## **C. Extending Conventional IC Capabilities**

As stated above, although bulk silicon will undoubtedly continue to be the primary IC semiconductor material for the foreseeable future, there are other materials that can perform functions that silicon is ill-suited to perform, such as certain microwave and optoelectronic functions. But even in the case of conventional ICs, bulk silicon is beginning to run out of steam as a means of providing indefinitely greater speed, increased functionality and lower cost. This is not to say that further downscaling of bulk silicon devices will not be possible. Indeed, through use of new design tools, advanced nanolithography and innovative packaging, it is widely expected that silicon MOS ICs with 0.5  $\mu\text{m}$  minimum geometries will reach general production by 1991-1993. And by reducing operating voltage below 5 volts, along with possible use of cryogenic techniques, chipmakers should be able to produce silicon MOS devices with 0.25  $\mu\text{m}$  minimum feature sizes by the year 2000 (see Fig. 1). Beyond that, however, future downscaling of conventional silicon IC technology will cease to be a viable option because of quantum effects and other physical limitations. At that point, additional improvement—in device cost, speed and functionality—will have to come from new materials (or new combinations of existing materials), new architectures, three-dimensional and other unconventional structures, and/or new physical phenomena (quantum effects, superconductivity, etc.).

For this study, attention was confined to several types of materials used in conjunction with silicon since they appear to offer the most immediate way to extend the performance capabilities



**Fig. 1. Further downscaling of conventional bulk silicon integrated circuits will cease to be a viable option by the year 2000.**

of conventional bulk silicon technology while at the same time retaining most of its advantages. These multimaterial structures have been made possible by new deposition technologies—principally molecular beam epitaxy and metal-organic chemical vapor deposition (see Section D)—which have enabled researchers to fabricate heteromaterials with specially engineered bandgap properties not found in naturally occurring substances. Such heteromaterials—composites of thin regions of dissimilar materials whose energy bands are tailored to produce unique properties such as ultra-high carrier mobility—could lead potentially to the development of solid state devices with substantially higher frequency/speed and power efficiency performance than would otherwise be obtainable from conventional silicon technology. Moreover, some of these epitaxially grown silicon-based structures

offer the possibility of combining both optical and logic functions on a single chip (see Fig. 2, next page), as compared to the lesser performance available from today's more costly hybrid configurations, typically characterized by several interconnected components, optical interfaces, etc. (An overall comparison of these two competing approaches—in terms of speed, reliability, ease of manufacture, etc.—is given in Table 1.)

In general, work on heteroepitaxial integration is still in its early stages in this country, with most of the effort under way within university and government research labs and within the advanced research departments of a few companies. In contrast, work in this area is considerably more advanced in Japan, where it is assigned relatively high priority and is much better coordinated.

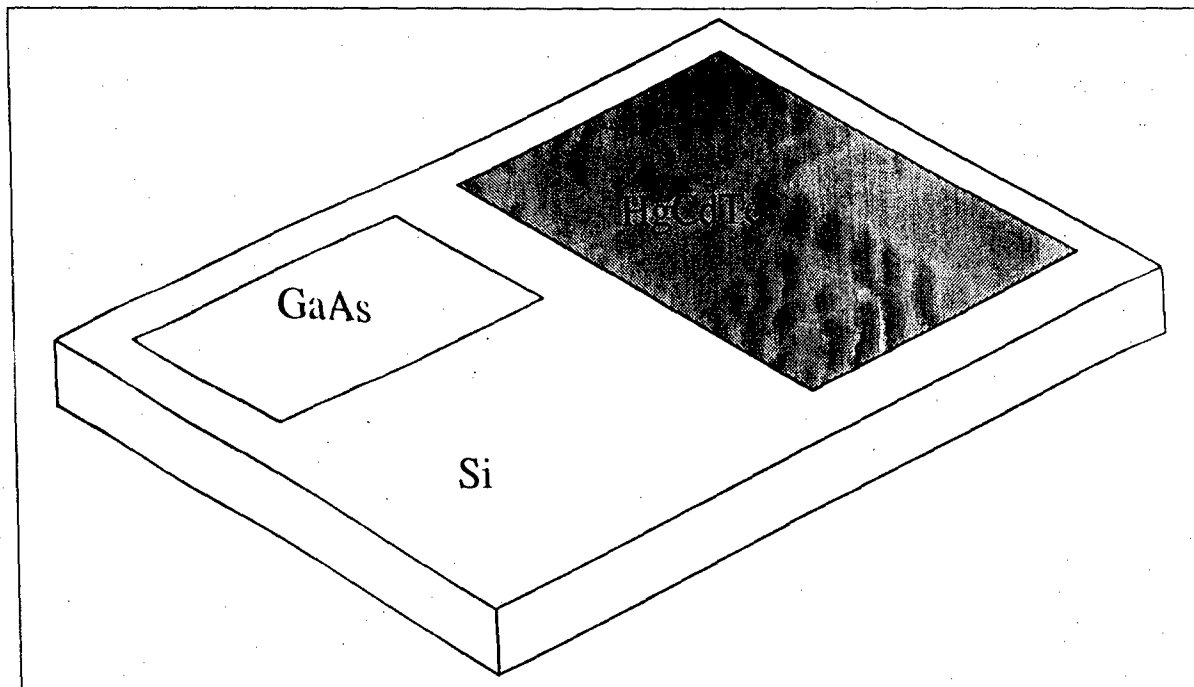
#### **D. Tomorrow's Materials: Requirements and Opportunities**

In its second annual Critical Technologies Plan, which was released in April 1990, DoD selected four areas of materials science—semiconductors, photonic materials, composites, and superconductors—among some 22 technologies deemed critical to the long-term strength of the U.S. military capability. The report found, however, that federal support of materials science and engineering had declined 11% from 1976 to 1987, with a 23% decline in civilian research. This is a dangerous trend, the report warned, and should be corrected. It called for funding to be increased to the mid-1970s level of support, pointing out that other nations, including Japan and West Germany, have targeted materials science as one of three top scientific priorities, along with biotechnology and information science.

Nowhere is material science more important than in microelectronics. As in the past, new materials will be the key to future device advancement. From a device standpoint, a promising new material should offer one or more of the following properties:

- High mobility, enabling low power operation.
- High saturated velocity, enabling high speed.
- Small effective mass, facilitating tunneling in quantum devices.
- Direct bandgap in the case of optical integration, enabling efficient optical emission and absorption (and tunability through use of different materials).
- Large intraband energy gap (that is, a wide separation between the conduction band minimum and the next highest minimum) for high velocity and tunneling.
- Semi-insulating substrate, resulting in low parasitic capacitance.
- High doping levels to ensure low contact resistance as dimensions continue to shrink.

In the search for new materials, the issue of impurity content, now measured in parts per million (ppm), is becoming increasingly important. It is expected that semiconductor device fabrication in the 1990s will require materials exhibiting impurities in parts per billion (ppb or  $10^{-9}$ ) in addition to ultra-clean rooms to minimize in-process contamination. To gain a perspective of what such purity entails, consider a 1- $\mu\text{m}$ -thick film of silicon that is 1  $\mu\text{m}$  square. Its volume is 1  $\mu\text{m}^3$ , or  $(10^{-4})^3\text{cm}^3 = 10^{-12}\text{cm}^3$ . Since a cubic centimeter of silicon contains about  $5 \times 10^{22}$  atoms, a 1  $\mu\text{m}$  cube will contain  $5 \times 10^{22} \times 10^{-12} = 5 \times 10^{10}$  atoms of silicon. At the 1 ppb level, this 1  $\mu\text{m}$  cube would therefore contain about  $5 \times 10^{10} \times 10^{-9}$  or 50 atoms or molecules of impurities. Thus, even at these levels a large number of impurities are still present.



**Fig. 2. Co-integration of multiple materials could eventually lead to a single-chip focal plane imager.**

**Table 1. Heteroepitaxial Integration vs Hybrid Interconnection**

	<b>Heteroepitaxial Integration</b>	<b>Hybrid Interconnection</b>
<b>System Speed</b>	Fast. Easy fabrication of interconnects with low inductance and capacitance.	High speeds only with precise impedance matching and careful bonding.
<b>Reliability</b>	Excellent for thermal or physical shock. Defects may reduce lifetime. (Lasers)	Bonds susceptible to thermal or physical shock.
<b>System Yield</b>	Reduced. Tradeoff between yield and sophistication.	Excellent. Preselection of functional chips.
<b>Flexibility</b>	Limited to compatible material and technology combinations.	Arbitrary combinations of materials or technologies.
<b>Alignment (Optical)</b>	Easily accomplished lithographically.	Difficult, lossy and costly.

Looking ahead to the advent of nanoelectronic devices (structures with dimensions below 0.1  $\mu\text{m}$ ), not only will these super-miniature devices exhibit new electrical properties, their physical and chemical properties will also be markedly different from those of today's microcircuits—the result not only of quantum effects but of the tendency of small numbers of atoms to arrange themselves in new and unusual ways. For example, when only 10 or so atoms form a cluster, a single atom more or less can have a drastic effect on the cluster's shape, and consequently on the material's chemical properties. Indeed, the shape of compounds has been found to be of major importance in molecular biology, prompting hopes that we may eventually learn how to duplicate the molecular assembly process of biological organisms.

In the not-too-distant future, it may also be possible to use the scanning tunneling microscope (STM) to fabricate "designer" materials one atom or molecule at a time. Here again, when so few atoms or molecules are involved, material purity becomes enormously important—to the point where it may eventually be necessary to specify impurities in parts per trillion (ppt or  $10^{-12}$ )!

### **E. Epitaxy: Key to Multimaterial Devices**

Epitaxy is the ordered deposition of a material on a single-crystal substrate. It differs from standard chemical vapor deposition in its ability to replicate the single-crystal lattice of the substrate material. Because of epitaxy's ability to precisely control compositions and doping, electronic and optical properties of a material can be engineered to create new device structures with unique characteristics.

The two main epitaxial processes in use today are molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD). Capable of producing an extremely abrupt interface, MBE, which was developed in the 1960s at Bell Labs, forms epitaxial layers from a few nanometers to hundreds of nanometers thick by directing beams of the requisite elements or compounds at a heated substrate (inside an evacuated stainless-steel vessel) where they condense in the form of a single crystal. Growth proceeds at approximately one atomic layer per second. In the MOCVD process, the heated substrate sits in a chamber at or near atmospheric pressure into which the gaseous constituents of a semiconducting compound are introduced, such as arsine and trimethyl gallium in the case of GaAs. In both processes, the stoichiometry of the deposited epilayer is controlled by the ratios of the elements transported onto the heated substrate and the composition is varied by varying the flow of those elements into the chamber.

A third process, called ultra-high-vacuum chemical vapor deposition (UHV-CVD), is rapidly gaining favor. In this method, invented by IBM, deposition occurs at lower temperatures and in a far cleaner environment than is the case with other growth techniques. A fourth epitaxial system, limited reaction processing (LRP), also is in current use. A combination of two other semiconductor growth processes—rapid thermal annealing and chemical vapor deposition—LRP is a rapid-thermal chemical process that uses a cold wall reactor, but it requires a relatively high temperature ( $\sim 740^\circ\text{C}$ ).

A number of additional epitaxial processes have recently been developed, including metal-organic MBE (MOMBE), chemical beam epitaxy (CBE), gas-source MBE (GSMBE), remote plasma CVD (RPCVD), and atomic-layer epitaxy (ALE). The RPCVD process holds the world's record for lowest temperature Si epitaxy ( $150^\circ\text{C}$ ). ALE is no less interesting, differing from other



epitaxial processes in its ability to deposit atomic species individually under near-equilibrium conditions. For example, in the case of GaAs, first a layer of arsenic is deposited, followed by a layer of gallium, etc. The result is an exceedingly uniform series of layers. The principal limitation of ALE is its slow growth rate. In an MOCVD or MBE process, growth rates of 0.1 to 10  $\mu\text{m}$  per hour can be achieved, whereas only a few nanometers per hour can be grown with ALE.

In general, it should be noted that in these epitaxial technologies and associated processing areas (focused ion beam, reactive etching, etc.), the Japanese effort is relatively aggressive compared to the effort going on in this country. If the U.S. wishes to remain competitive in these multimaterial device technologies, some of the areas that will have to be particularly emphasized are:

- Lower temperature epitaxial crystal growth
- Selective epitaxy
- Low temperature processing
- Selective in-situ processing
- Extension of silicon "micromachining" techniques to other materials

#### **F. MOCVD Consortium: An Example of Government-Industry Cooperation**

In recognition of the importance of the MOCVD growth process as it relates to GaAs, the U.S. Army Electronics Technology and Devices Laboratory (ETDL) has announced the formation of a new government/industry/university consortium that seeks to: (1) improve the MOCVD growth of advanced high-speed electronic devices such as high electron mobility transistors (HEMTs), and (2) develop a less hazardous MOCVD process which utilizes liquid replacements for the toxic compressed gases arsine and phosphine.

The four-member consortium consists of ETDL, EMCORE (Somerset, NJ), American Cyanamid (Wayne, NJ) and Polytechnic University (Brooklyn, NY). ETDL will be responsible for material characterization, device fabrication and evaluation, and overall program coordination. The MOCVD thin film growth will be carried out by EMCORE, a leading supplier of advanced MOCVD systems. American Cyanamid will provide the MOCVD precursor chemicals, particularly TBA (tertiarybutylarsine) and TBP (tertiarybutylphosphine), less hazardous liquid replacements for the toxic gases. Polytechnic University will carry out basic investigations into the MOCVD process, including mechanisms and modeling, utilizing these chemical sources.

"This consortium is an important demonstration of the way government, industry and academia must work together to keep the U.S. competitive in this strategic area," notes Dr. C.G. Thornton, ETDL Director. "Advancing our MOCVD tech base in critical gallium arsenide device programs, particularly if this can be achieved with a safer and more secure process, is a vital task."

Adds Dr. Kenneth Jones, consortium coordinator at ETDL: "We are hopeful that the outcome of the consortium's activities will feed directly into supporting the MIMIC program. The Japanese have recently demonstrated large-scale MOCVD growth of HEMT structures as well as the potential performance and safety benefits of using TBA in this process. We feel that we can become competitive with our consortium's collaborative approach."

### III. REVIEW OF SPECIFIC TECHNOLOGY AREAS

#### A. Gallium Arsenide-on-Silicon Device Technology

##### 1. Introduction

As noted above, bulk elemental silicon continues to be the predominant semiconductor material for electronic devices; however, its ability to provide ever-greater speed and density through further downscaling is coming to an end. Gallium arsenide (GaAs), on the other hand, is a semiconductor material that not only enables faster ICs and better radiation hardness than bulk silicon devices, it is also useful—along with other III-V compounds such as indium phosphide (InP)—for microwave, optical, and optoelectronic applications, applications for which silicon is ill-suited because of its intrinsic bandgap limitations. The problem, however, is that neither GaAs nor any other semiconductor material can match silicon's low cost, heat dissipation, mechanical strength, potential for scaling (though now somewhat limited at submicron geometries), and overall knowledge base. For example, whereas silicon wafers can now be readily grown as large as eight inches in diameter and are easy to work with, GaAs slices are still limited to three to four inches and the resultant substrates are easily scratched, generally more difficult to work with, and thus far more expensive than silicon substrates.

The ideal solution would seem to be some sort of combination of the two materials. Since almost all electronic and photonic activity occurs within the top few microns of a GaAs IC anyway, why not simply grow a layer of GaAs onto a silicon base and thereby get the best of both materials? More generally, why not simply "wafer engineer" materials of various types to produce devices that respond optimally to the requirements of any given application? An example of such a possibility, GaAs and Si devices co-integrated on a silicon substrate, is shown in Fig. 3.

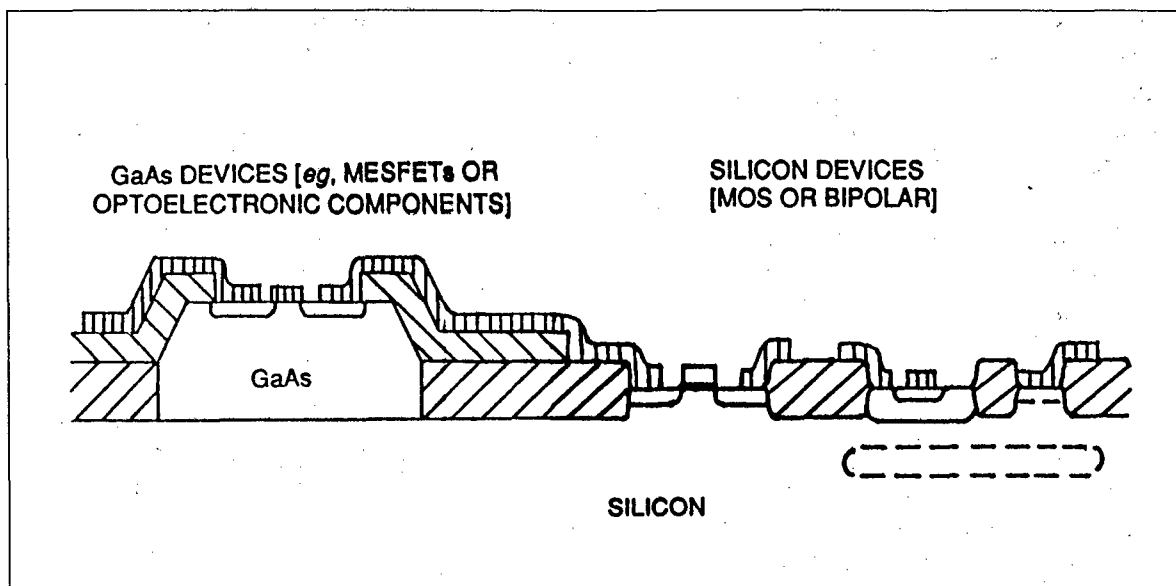


Fig. 3. Monolithic integration of GaAs on silicon.

Unfortunately, it turns out that the lattice constants (atomic spacings) of these materials are quite dissimilar, making it exceedingly difficult to grow heterojunctions that are sufficiently free of defects. Since the fabrication of reliable devices at reasonable yield levels requires relatively defect-free materials, until as recently as 1984 it was generally felt to be hopeless to try to produce useful heterointegrated devices. However, the advent of molecular beam epitaxy and other new epitaxial and surface processes has enabled the heterointegration of these previously incompatible materials, and has given rise to a number of promising silicon-based device structures—notably GaAs/Si, Ge/Si (see Section B), and Si-on-insulator (SOI)/Si-on-sapphire (SOS) structures (Section C). In addition, the device potential of fluoride technology, also considered in this study, is addressed in Section D.

## 2. Existing Problems

Ideally, from a device standpoint, GaAs-on-Si wafers should be able to combine the high speed and optoelectronic capabilities of GaAs with the many benefits of silicon—that is, provide the same mechanical strength, thermal conductivity and large size of silicon wafers, and, with volume production, a much lower price than bulk GaAs wafers. In actuality, however, despite the many promising device and circuit results that have been demonstrated, several difficult problems remain, seriously impeding further development of this technology in all but a few device areas. Chief among these problems are the following:

### a. Dislocation Density and Other Lattice-Mismatch-Induced Defects

It turns out that the number of atoms per unit length in a crystal lattice of GaAs is slightly greater than the number in silicon. Specifically, there are 24 gallium and arsenic atoms for every 25 silicon atoms at any GaAs/Si interface. Because of this 4% lattice mismatch between GaAs and Si, numerous misfit dislocations are generated when the two materials are combined epitaxially. Unless reduced to a low enough number or deflected away from active junctions, these defects can lead to device failure. As shown in Fig. 4, progress in reducing dislocation density in GaAs/Si was fairly rapid initially, but has slowed markedly in recent years. Starting at around  $10^9$   $\text{cm}^{-2}$  in 1985, when people really begin to work this problem, it has essentially leveled off at approximately  $10^7$   $\text{cm}^{-2}$ . This leveling off is probably why no one has been able to make a laser in GaAs/Si better than one that was made at the University of Illinois (Urbana) back in 1987. (It should be noted that lasing in GaAs/Si structures tends also to be seriously affected by the stresses created by the thermal expansion mismatch between Si and GaAs, as described in the following section. Thus, the GaAs layer that is grown is under significant tensile stress, typically ranging between 0.5 and  $2 \times 10^9$   $\text{dyne/cm}^2$ . In general, for a reliable laser, one should not exceed tensile stresses of  $1 \times 10^8$   $\text{dyne/cm}^2$ .)

As indicated in Fig. 4, at  $10^7$   $\text{cm}^{-2}$  the dislocation density of GaAs/Si devices is about three orders of magnitude higher than that achievable in regular bulk GaAs ICs, making it very difficult to realize certain classes of devices. For example, in the case of majority carrier devices, a  $10^7$   $\text{cm}^{-2}$  level reduces by tenfold the minority carrier lifetime—which corresponds to a two-orders-of-magnitude reduction in the electroluminescence efficiency of an all-GaAs LED. For heterojunction bipolar transistors, the effect of a  $10^6$ - $10^7$   $\text{cm}^{-2}$  dislocation density is less severe: dc current gain falls from 300 at  $10^5$   $\text{cm}^{-2}$  to 275 at  $10^6$  and to 150 at  $10^7$ .

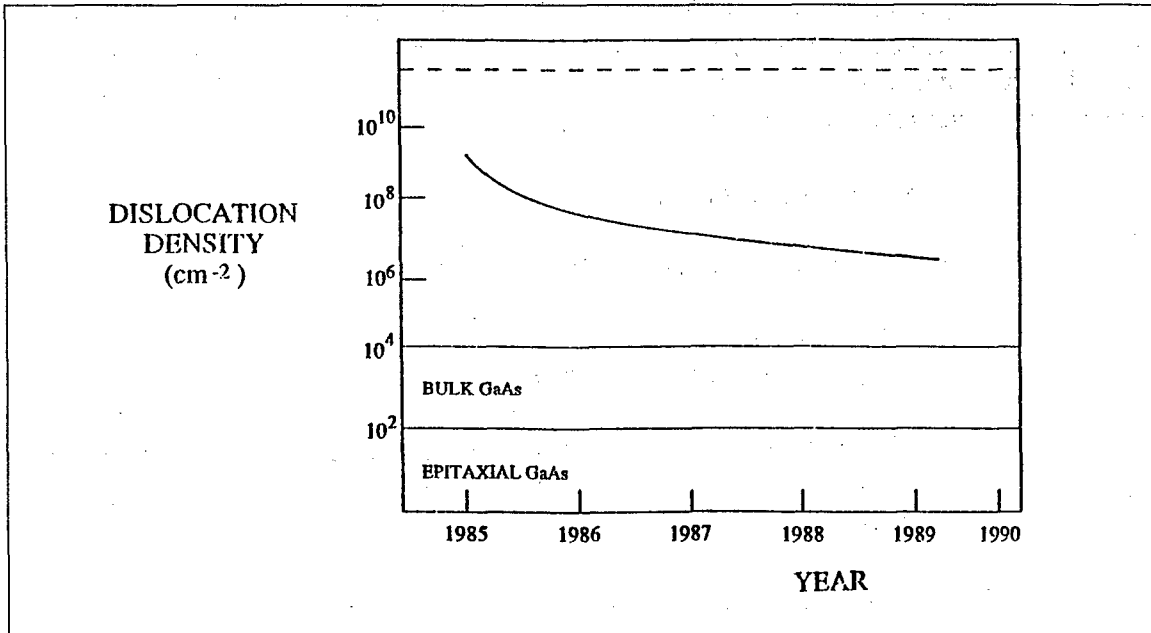


Fig. 4. Curve showing progress in reducing dislocation density in GaAs-on-Si heterostructures.

In the case of majority carrier devices such as MESFETs, the impact of a  $10^7 \text{ cm}^{-2}$  dislocation density on electron mobility is relatively slight because of the overriding effect of the n-type doping—particularly at doping levels above  $10^{16} \text{ cm}^{-3}$ .

The lowest dislocation density reported to date in any GaAs/Si device structure has been  $2 \times 10^6 \text{ cm}^{-2}$ . Accomplished by a Japanese research group, it was achieved through use of an extremely complicated process involving up to 20 iterations of a succession of growth/cooling/heating/annealing steps. But even that level turns out to be far too high for conventional lasers, which nominally require dislocation densities below  $10^5 \text{ cm}^{-2}$ .

One way to ease the problem is to introduce a buffer layer—or series of layers—of transitional material between the GaAs and silicon. Typically, a layer of gallium phosphide (GaP) is deposited on the silicon substrate, followed by a series of very thin layers of GaAsP, each containing a higher ratio of arsenic to phosphorus, until the top layer is pure GaAs. Such a "strained-layer superlattice" acts to smooth away the abruptness of the GaAs/Si lattice mismatch and thereby reduce the number of dislocation defects arising from that mismatch. However, although this technique has provided some improvement, it is doubtful that it alone will be capable of reducing dislocation density by another three orders of magnitude—to  $10^4 \text{ cm}^{-2}$  (needed for reliable IC operation), down from current  $10^7 \text{ cm}^{-2}$  levels.

It is now fairly clear that further significant reduction of dislocation density will not be achievable by traditional thermal annealing and strained layer superlattice techniques. Two courses of action therefore suggest themselves. One is to try to live with present dislocation density levels ( $\sim 10^7 \text{ cm}^{-2}$ ), confining attention to those device types and applications that can tolerate those levels.

The other course of action is to seek some new and innovative approaches for reducing these defect densities. One of the most promising approaches is the use of patterned growth—that is, either deposit a very localized GaAs area or deposit on a sheet basis and then come back and form a very localized area. The benefits of such patterned growth are:

- Fewer dislocation nucleation sites are produced.
- Significantly reduced probability of dislocations intersecting active device areas.
- The pattern edges attract most of the dislocations and enhance the thermal annealing and strained layer superlattice effects.
- Where areal dimensions become comparable to the thickness of the GaAs epilayer, significant stress relief can be obtained—perhaps down to the  $10^8$  dyne/cm<sup>2</sup> level needed for lasing.

b. Thermal Incompatibilities

GaAs expands with heat about twice as fast as silicon. Thus, the cool-down to room temperature after high-temperature deposition of GaAs in silicon tends to produce significant tensile stress in the GaAs layer (typically ranging between  $0.5$  and  $2 \times 10^9$  dyne/cm<sup>2</sup>). This stress results in a concave or bowed wafer that is very prone to cracking and breakage. However, it has been found that this warping problem can be eased considerably by limiting the growth of GaAs only to those areas of the silicon wafer containing active circuitry. This "local growth" technique seems to lessen the buildup of these warp-generated cracking problems and, accordingly, is drawing major attention at TI, Stanford University, and other centers.

c. Antiphase Domains

In growing GaAs on conventionally sliced silicon wafers, it turns out that some areas of the silicon surface bond first to Ga atoms while other areas bond first to As atoms, resulting in an asymmetrical matrix of Ga and As atoms throughout the GaAs epilayer. These so-called "antiphase domains" weaken the material and impede current. However, it has been found that by slicing the silicon along a different crystal plane (a few degrees off conventional orientation), a stepped surface can be produced that attracts As atoms primarily, significantly relieving this problem.

d. Cross-Doping, Defect Propagation and Other Process-Induced Defects

There are still many unanswered questions relating to the process compatibility of GaAs and Si. For example, the processing temperatures of the two materials are such that local growth of GaAs will generally be required—and require that Si devices be present during GaAs growth. Moreover, the need for high temperature oxide desorption raises questions about the diffusion of junctions and contact areas. Then there is the problem of Si autodoping into GaAs and Ga and As doping into the Si areas. More fundamentally, it is still not fully known how much the Si device properties will be altered because of the use of an off-axis Si substrate, which, as stated

above, is needed to prevent anti-phase domains and provide smoother layers. Finally, because these devices are so surface and interface dominated and because interfaces and surfaces are far more controllable and reproducible when processed without exposure to air, in-situ processing is likely to become increasingly vital in the future.

e. Limited Applicability

The above-cited difficulties raise serious questions about the attainable yields, cost of fabrication and hence ultimate competitiveness of these multimaterial devices in single-function (all-electronic) applications. For example, even if the current size advantage of Si wafers were to hold indefinitely (eight inches vs. four inches for GaAs), there is considerable doubt that GaAs/Si technology would ever succeed in reducing the cost of bulk GaAs ICs, given the added cost of epitaxy and additional mask levels required in fabricating GaAs/Si devices. As a result, many experts see this technology attractive only as a single-chip solution of a multifunction requirement—electronic/optical, digital logic/microwave, etc.

3. GaAs/Si "Microelectronics" Activity

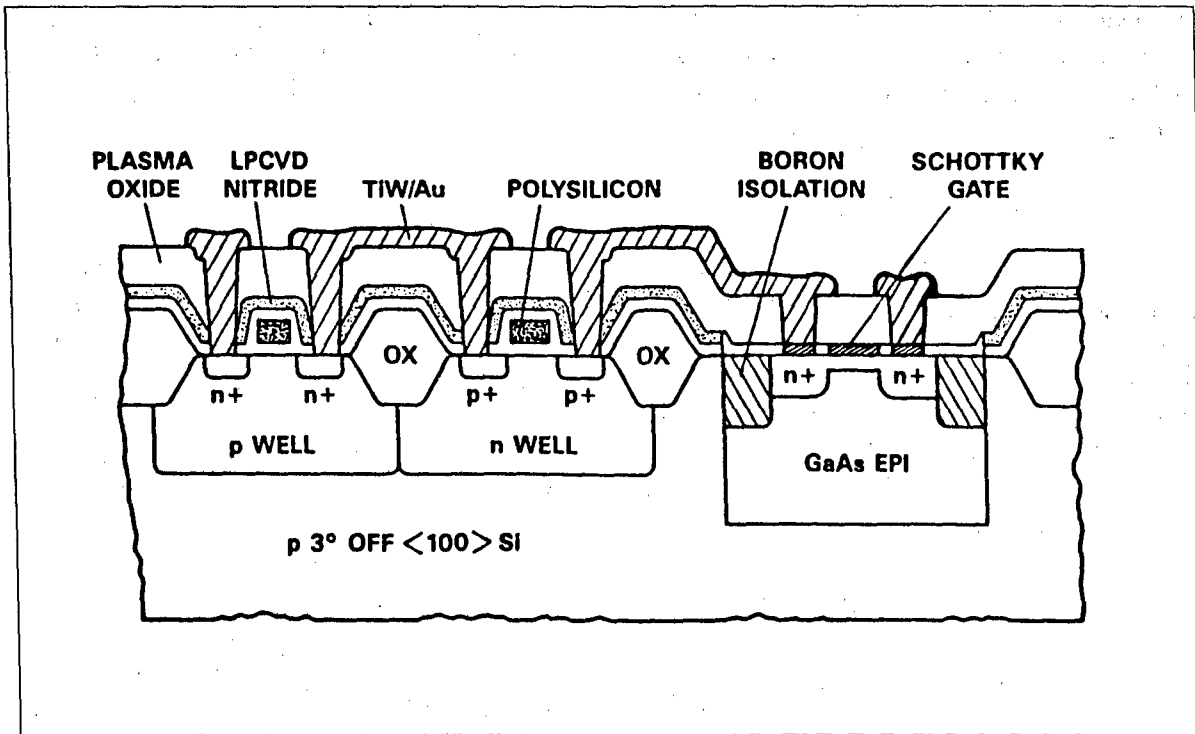
As stated above, it appears at this point that the big advantage of adding GaAs and other III-V materials to Si will be in satisfying multifunctional requirements, such as creating optoelectronic ICs. Primarily because of the dislocation density problem, the potential advantages of this technology are just not as convincing in purely electronic or optical areas. Some of the mixed applications that would appear to take maximum advantage of the speed and optoelectronic strengths of GaAs and high density capability of Si are:

- GaAs MESFET logic + Si CMOS memory
- GaAs HBT A/D converter + Si CMOS memory
- GaAs LEDs/Lasers + Si VLSI circuits
- GaAs photodetector + Si VLSI circuits

An example of the first-mentioned device structure, a GaAs MESFET co-integrated with Si CMOS circuitry on a Si substrate, has been fabricated at TI (see Fig. 5), where some of the most advanced GaAs/Si work in this country is being performed. At TI's Central Research labs, for example, principal emphasis is being placed on selective/patterned growth of GaAs film on prefabricated Si wafers, on having the GaAs and Si circuit share the same interconnection, and on an overall process that adds no more than five extra mask levels to the company's conventional CMOS process.

As of late 1989, TI's GaAs/Si program had advanced to the point where:

- The basic process flow had been established.
- To a first order, GaAs processing and growth had been shown to be compatible with Si devices—although some shifting of threshold voltages was still seen after the GaAs processing.



**Fig. 5. Monolithic co-integration of GaAs MESFET and Si CMOS structures (developed by TI).**

- A GaAs/Si interfacing circuit, which provides conversion between GaAs and Si (CMOS) levels in just one gate, had been developed and demonstrated.
- Small co-integrated circuits (ring oscillators) had been demonstrated.

Advanced research in GaAs/Si technology also is under way at Stanford University, where device and circuit investigations have taken four directions:

- (1) GaAs bipolar structures for high-speed applications. According to Prof. J. Harris, principal investigator, two main reasons prompted the work: (1) no one else was doing it, and (2) as minority-carrier devices, bipolars are a lot more sensitive to problems with the electrical properties of the device than are FET structures. Stanford, working alone on this project, uses a full-wafer epi process to deposit a GaAs layer across the entire silicon wafer.
- (2) Silicon bipolar optical receiver (in collaboration with Hewlett Packard). The device uses silicon bipolar devices and GaAs as the detector. It will eventually use an FET front end. Local epitaxial deposition is used.
- (3) Investigation, in collaboration with Intel, of the possible incorporation of GaAs bipolar or FET devices in an otherwise CMOS microprocessor

architecture. Local epi is used to incorporate small amounts of GaAs amid hundreds of thousands of silicon transistors.

- (4) GaAs FET structures, in collaboration with Vitesse. The project, which features a full-wafer epi process, also is being used by Stanford as a check of its material—to see how it compares to what others have done, etc.

The Stanford researchers have found, on the basis of these and other GaAs/Si projects, that best results are obtained when an approximately 3  $\mu\text{m}$  buffer layer is placed between the GaAs and silicon interface, with the Si devices not stacked below but placed off to the side and interconnected laterally. In general, it is felt that any kind of stacked structure, in which there are silicon devices below and GaAs above, will not be practical.

Although Stanford has managed to reduce the number of dislocations by a factor of two to three through use of a variety of both strained and unstrained superlattice structures and has made working devices from material with very high dislocation density, researchers there emphasize that much more improvement will be needed if good, yielding devices are to be reliably fabricated. Specifically, no less than three orders of magnitude additional improvement in dislocation density will be needed—which may or may not be achievable by simply devising some better recipe of superlattice steps.

As things stand now, the Stanford researchers consider the promising application opportunities for GaAs/Si technology to be in the areas of optical interconnects, creating different types of sensors, mixing, and creating visible light sources. With further significant defect reduction, etc., there is of course the prospect of increasing the speed of conventional Si devices while maintaining the capability in dynamic circuits (particularly in memory) that is simply lacking in Schottky-barrier-type approaches.

#### 4. Other Device Activity

Other types of GaAs-on-Si devices also are under investigation, including multiple quantum well (MQW) lasers and monolithic microwave ICs (MMICs). In the laser area, for example, work at the University of Illinois (Urbana) has demonstrated lasing in an  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ -GaAs quantum well heterostructure grown by MOCVD and employing as the "substrate" GaAs grown on Si by molecular beam epitaxy (see Fig. 6). Led by Prof. N. Holonyak, the research at Urbana has been concerned of late with making an MQW laser superior to—or even as good as—one made there in 1987, and at trying to extend the short lifetime of the lasers built to date (ranging from minutes to a few tens of hours at 77K). As indicated previously, the lack of significant progress since 1987 in this particular area of laser technology is in large measure attributable to the lack of significant improvement in dislocation density reduction in GaAs/Si heterostructures since that time. One possible way around the problem is to reduce the dimensions of these lasers to just a few square micrometers, making it less likely that a dislocation will intersect the active junction region of the device. Indeed, such small "surface emitting lasers" were recently built and demonstrated in CW operation at AT&T/Bell Labs.



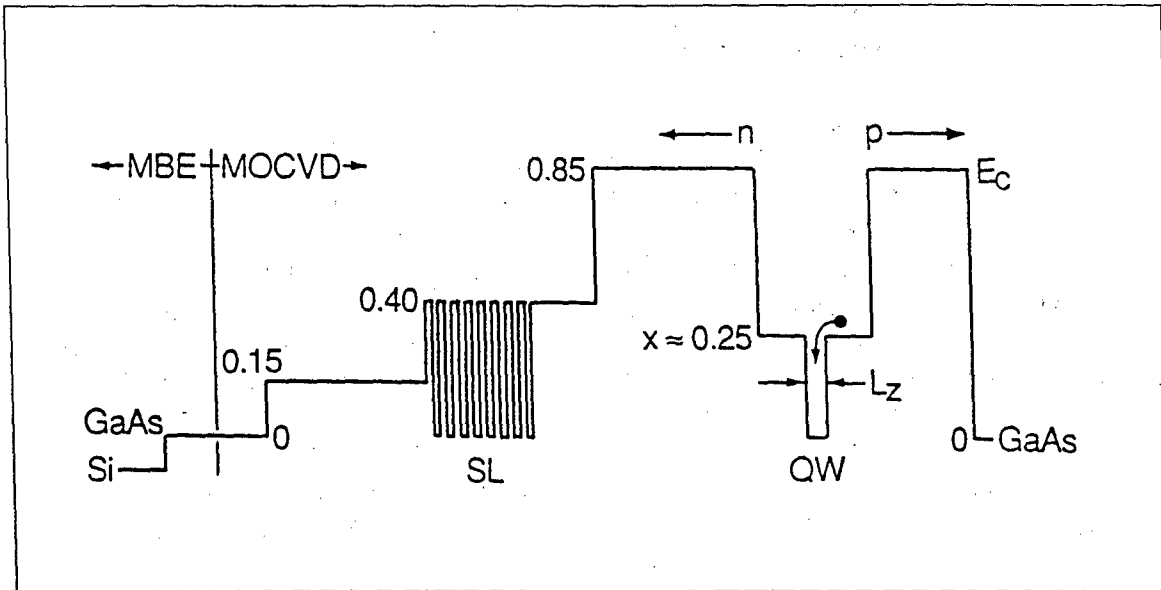


Fig. 6. MOCVD  $\text{Al}_x\text{Ga}_{1-x}\text{As-GaAs}$  p-n QWH on MBE GaAs-Si ( $L_z \approx 125 \text{ \AA}$ ).

In the microwave area, there has long been interest in the possibility of making GaAs MMICs on a Si substrate. Although MMICs are not high-density circuits, they do require a large amount of real estate. However, by switching to large-wafer Si, a device designer would forfeit one of the biggest advantages of GaAs: a  $10^8$  ohm-cm semi-insulating substrate.

One possibility is to use very high resistivity silicon—say, float zone material at  $10^4$  ohm-cm. If it could be kept from converting during the processing, it might lead to a viable GaAs MMIC-on-Si device, particularly at frequencies at or above 30 GHz. The problem, however, is that the large-diameter wafers desired cannot be realized with float zone material at this time—at least not at a price that would be cost-competitive with an all-GaAs approach.

Some researchers have tried depositing GaAs on sapphire directly, but the results have not been very promising. One can also buy silicon-on-sapphire (SOS) substrates and deposit GaAs on the SOS. This, potentially, has some value for microwave applications but the silicon layer is very thin. However, one of the nice surprises is that the magnitude and sign of the thermal expansion coefficient of sapphire is essentially opposite that of GaAs. By adjusting the Si thickness, one could conceivably control the stress in the GaAs layer, possibly reducing it to as low as  $10^6$  dyne-cm<sup>-2</sup>.

Another possible approach is to deposit GaAs on SOI substrates. TI has tried this using SIMOX wafers (see Section C). In general, it is still not clear whether GaAs-on-SOI devices will prove useful for microwave applications. The problem is getting a clean, oxide-free surface, which is needed to maintain surface mobility. One possibility is to grow a very thin layer of Si onto the SOI substrate prior to depositing the GaAs.

5. Size and Distribution of Present Effort

DoD support of GaAs/Si multmaterial research is currently running at just over \$1.5M per year (see Table 2). Besides this government-supported research, there are a number of company-supported efforts in this area, such as the aforementioned work at Stanford University supported by H-P, Intel and Vitesse. While almost all of this effort (both government and company-sponsored) is concerned with GaAs/Si materials and processing issues, much of the thrust of that effort is directed at co-integrated optoelectronic applications as opposed to merely extending the performance capabilities of silicon microelectronics. Examples of these new, optical-oriented applications are the multmaterial focal plane imager shown earlier in Fig. 1 and new laser devices based on quantum well heterostructures (QWHs) grown on GaAs/Si substrates (Fig. 6). Although several optical and optoelectronic areas were considered during this study, along with some microwave areas, the attention of the Working Group was largely confined to non-microwave electronic applications, and the conclusions and recommendations that were reached (Section IV) pertain mainly to conventional microelectronic issues.

**Table 2. Funding for GaAs/Si Multmaterial Research**  
(6.1 funds unless otherwise noted; in \$thousands)

	<u>FY90</u>	<u>FY91</u>
N(ONR)	*300	*300
AF(OSR)	650	500
A(ARO)	350	350
AF(WRDC)	**260	**300
NRL Internal	100	100
Totals	1660	1550

\* Includes funds from DARPA, SDIO and DNA

\*\* 6.2 funds

The principal U.S. and Japanese research centers concerned with GaAs/Si multmaterial technology are identified in Table 3. In Japan, the Optoelectronics Research Laboratory is generally regarded to be at the forefront of research in GaAs/Si materials and processing technology. Oki, on the other hand, is farthest along in terms of commercializing this technology. The company is actively marketing GaAs/Si devices.

**Table 3. GaAs/Si Technology: Principal Research Centers**

<u>United States</u>	<u>Japan</u>
• AT&T Bell Labs	• Kyoto University
• Bellcore	• Nagoya Institute of Technology
• California Institute of Technology	• Oki
• Kopin	• Optoelectronics Research Laboratory
• MIT-Lincoln Lab	• Osaka University
• North Carolina State University	• Tokyo Institute of Technology
• Sandia	
• Stanford University	
• Texas Instruments	
• University of California (Berkeley and Los Angeles)	
• University of Illinois (Chicago and Urbana)	

## 6. Summary

In summary, GaAs/Si structures promise to provide a critical element in future optoelectronic and electronic systems. Such systems may open the way to: higher data processing rates, levels of integration not achievable by other means, and new device functions. To realize these advances, research and exploratory development efforts must emphasize a variety of approaches for improving the materials properties of GaAs grown on Si. The full exploitation of GaAs/Si technology cannot be achieved without discoveries leading to the reduction of the density of dislocations produced as a result of the inherent lattice mismatch at the GaAs/Si interface. In short, GaAs/Si structures may open the way to enormous payoffs in electronics and optoelectronics but many such advances cannot be realized without discoveries leading to greatly improved properties.

Specifically, the following steps need to be taken:

- Emphasize materials development
- Demonstrate larger scale integration.
- Develop complete compatibility of GaAs and Si devices—by gaining a better understanding of the effect of GaAs growth/processing on Si devices, etc.
- Investigate the effect of parasitic capacitance from the Si substrate on GaAs circuit speed. (For microwave applications, continue study of SOI and SOS substrates.)
- Demonstrate manufacturability.
- Most importantly, develop a far better understanding of the reliability of these devices.

## B. Germanium/Silicon Device Technology

### 1. Introduction

Recent progress in the epitaxial growth of strained layers of silicon and germanium, two Column IV elements, has given rise to a number of advanced heterojunction structures and may lead eventually to optoelectronic devices that do not require the direct-bandgap properties of GaAs or any other III-V material to provide the optical function. Examples of the structures built with this technology are Ge/Si heterojunction bipolar transistors (HBTs), avalanche photodiodes, high-electron mobility transistor (HEMT) devices, and, most recently, a variety of tunneling structures, quantum wells and superlattices. We will now go on to discuss the materials- and structural-related characteristics of these Ge/Si devices, paying particular attention to the Ge/Si HBT (see Fig. 7) since it is clearly the most important of all these Ge/Si devices in terms of its potential ability to advance conventional IC technology.

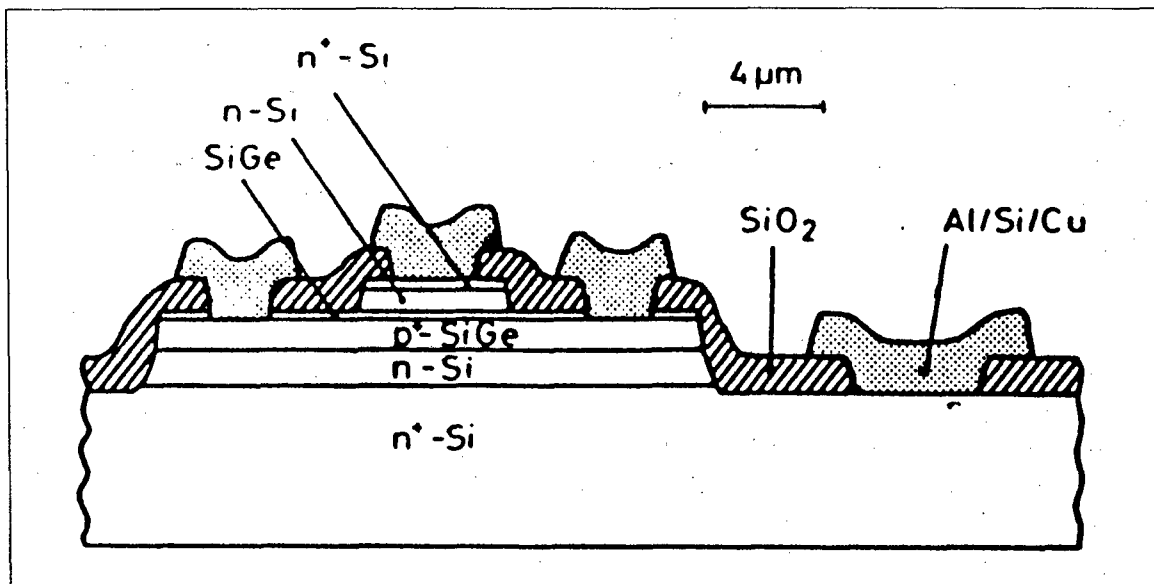


Fig. 7. Cross-section of a heterojunction bipolar transistor.

### 2. Growth of Ge/Si Device Structures

Because there is a 4.17% lattice mismatch between Ge and Si (at room temperature), epitaxial growth of  $\text{Ge}_x\text{Si}_{1-x}$  on Si must be carefully controlled to minimize the generation of misfit dislocations and other defects. Growth in the in-plane lattice will be strained to match that of the substrate and the vertical lattice constant will be elastically strained, producing tetragonal distortion of the cubic lattice. This growth mode proceeds until the strain energy in the layer exceeds the energy needed to generate dislocations. At that point, islanding and 3-D growth occurs, along with the generation of misfit dislocations at the interface. The "critical thickness" at which these defects

occur depends on the Ge content of the layer. In the case of Ge/Si HBTs, the Ge content is usually kept below 30% to minimize these defects.

The strain in a strained layer will relax with the generation of misfit dislocations when the critical thickness is exceeded or when the layer is subjected to high temperature. For  $\text{Ge}_x\text{Si}_{1-x}$  grown on Si, a low Ge fraction is used to allow attainment of an adequate film thickness. As in the case of GaAs/Si structures, when growing multiple layers, strain relief can be provided by the use of buffer layers. For each layer, the Ge fraction is the average of that of the two adjoining layers. Using this procedure, the strain of multiple layers can be eliminated, along with limitations on the thickness of the layer. Of course, the  $\text{Ge}_x\text{Si}_{1-x}$ /Si structure should still be processed with a short thermal budget to minimize the generation of dislocations.

Currently, the two most popular techniques for epitaxially growing Ge/Si structures are molecular beam epitaxy (MBE) and ultra-high-vacuum chemical vapor deposition (UHV-CVD). Both are low temperature processes.

As indicated earlier, MBE is a physical, surface controlled doping process that is capable of producing an extremely abrupt interface. Interestingly, initial attempts to produce  $\text{Ge}_x\text{Si}_{1-x}$  by MBE failed because growth temperatures had to be kept above 750° C. It was not until the early 1980s, when growth temperatures could be reduced to 580° C, that smooth, high-quality GeSi films were first obtained. Today, MBE processes are usually run at temperatures below 550° C with pressures at about  $10^{-10}$  torr.

By contrast, UHV-CVD, developed by IBM, is a chemical process involving a hot wall reactor. Normally run at temperatures below 550° C, with pressures below  $10^{-3}$  torr, the process is capable of depositing up to about 5 angstroms/min (at 500° C). As in the case of MBE, low-temperature deposition is required to keep the larger Ge atoms in place, while the high vacuum is needed to prevent incorporation of contaminants. Using the UHV-CVD process, IBM recently fabricated the world's fastest silicon-based transistor. The device, a Ge/Si HBT, exhibited a maximum cutoff frequency of 75 GHz, nearly twice as high as the previous record (see next section).

### 3. Ge/Si Heterojunction Bipolar Transistor (HBT)

The HBT, first proposed in the 1950s, offers higher speed and lower power consumption than is obtainable from conventional transistor structures. To date, most high-performance HBTs have been built in GaAs to take advantage of that material's superior speed capability relative to silicon. But although faster than comparable Si circuits (100 GHz vs. 40 GHz), GaAs ICs are generally more expensive and difficult to fabricate; hence, there continues to be intense interest in developing higher-speed Si-based HBTs.

Ge/Si bipolar transistors were first grown with MBE. Both npn and pnp transistors have been successfully fabricated. A dc gain of over 1000 for an npn transistor has been reported. The device was grown using MBE and had equal base and emitter doping densities of  $1 \times 10^{18} \text{ cm}^{-3}$ . Other HBTs grown using the limited reaction process have exhibited speeds up to 28 GHz. The 28 GHz device featured two  $1 \times 11 \mu\text{m}$  emitter stripes, a  $\text{Ge}_{0.2}\text{Si}_{0.8}$  base 250 angstroms wide, and a doping density of  $7 \times 10^{18} \text{ cm}^{-3}$ .

In March 1990, IBM announced fabrication of the world's fastest silicon-based transistor. The device, a Ge/Si HBT, operated at a maximum frequency of 75 GHz, nearly twice as fast as the previous record. The company's UHV-CVD process was used to grow a 500-angstrom-thick Ge/Si base region, with the Ge suitably graded across the base to reduce the bandgap and, consequently, the base transit time and emitter charge storage. Because of the bandgap reduction at the base, higher gains at low temperatures are possible with Ge/Si, compared to straight silicon devices. That has important implications for supercomputers and other cooled systems, given the fact that silicon performance normally degrades at low temperatures.

The first implementation of the Ge/Si HBT was demonstrated in 1987 by IBM researchers in Yorktown. In 1989, Ge/Si transistors operating at 40 GHz were built at IBM's East Fishkill lab.

4. Size and Distribution of Present Effort

DoD support of all Column IV multimaterial research is currently running at about \$3.5M per year (see Table 4). Most of the research in the U.S. involves the growth of  $Ge_xSi_{1-x}$  alloys on Si substrates and much of that work is concerned with the development of optoelectronic systems, putting it outside the main field of interest of this study.

Table 4. DoD Funding for Silicon-Based Column IV Multimaterial Research

	<u>FY90</u>	<u>FY91</u>
N(ONR)	*2400	*2550
AF(OSR)	550	>550
A(ARO)	300	300
AF(WRDC)	0	0
NRL Internal	150	150
Totals	3400	>3550

\*Includes funds from DARPA, SDIO and DNA

Table 5 identifies the world's leading research groups in this area of technology. It also identifies other major groups active in this area.

**Table 5. Leaders in Column IV Heteromaterial Research**

<b>LEADING CENTERS</b>	
UCLA Electrical Eng. Dept. 405 Hilgard Avenue Los Angeles, CA 90024-1594	Hitachi, Ltd. Central Research Laboratory Kokubunji, Tokyo 185 Japan
IBM/Thomas J. Watson Research Center PO Box 218 Yorktown Heights, NY 10598	NEC Corporation Semiconductor Rsch Laboratory 4-1 Miyazaki 4-Come Miyamae-Ku, Kawasaki Kanagawa 213 Japan
University of Warwick Department of Physics Coventry CV4 7AL United Kingdom	California Institute of Technology Pasadena, CA 91125
Daimler-Benz Research Center (formerly AEG Rsch Ctr) Wilhelm-Runge Str. 11 Postfach 23 60 D-7900 ULM Federal Republic of Germany	National Research Council 75 de Mortgage Boulevard Boucherville J4B 6Y4, PQ Canada
AT&T 600 Mountain Avenue Murray Hill, NJ 07974-2070	Tokyo Institute of Technology 2-12-1 Ookayama, Meguro-ku Tokyo 152 Japan
<b>OTHER ACTIVE CENTERS</b>	
Texas Instruments PO Box 655936 Dallas, TX 75265	Hewlett Packard 3500 Deer Creek Road Palo Alto, CA 94304
Stanford University 226 McCullough Building Stanford, CA 94305	University of Tokyo Institute for Solid State Physics Tokyo 106 Japan
Philips Research PO Box 80.000 5600 JA Eindhoven The Netherlands	Hiroshima University Higashi-Senda-Machi Hiroshima 724 Japan
Hughes Research Laboratories 3011 Malibu Canyon Road Malibu, CA 90265	

## 5. Summary

It is now possible to combine formerly incompatible materials like germanium and silicon using low-temperature growth techniques such as molecular beam epitaxy. This capability has led to a variety of improved and new devices and systems, including Ge/Si HBTs, strained-layer quantum well and superlattice devices, and, potentially, optoelectronic systems (where strain effects lead to enhanced optical interactions in these indirect-bandgap semiconductors). Although the processes involved in growing these Column IV structures are not as advanced as those used to fabricate the III-V compound semiconductors, important progress is being made. To realize the full potential of these Column IV heteromaterials in electronic and optoelectronic applications, it will be necessary for future research and development efforts to emphasize improved control of the processes used to grow these structures.

### C. Silicon-on-Insulator (Including Silicon-on-Sapphire) Technology

#### 1. Introduction

Silicon-on-insulator (SOI) technology, which has long been of interest to DoD because of its superior radiation-hardness characteristics (relative to bulk silicon), could well become the dominant semiconductor technology of the 1990s. Besides improved radiation resistance, it offers a technology route for further increasing the density of Si chips without having to resort to difficult isolation techniques (trench, LOCOS, etc.) and without having to give up the 5 volt supply option at 0.5  $\mu\text{m}$  geometries and perhaps beyond. In fact, there are practically no isolation constraints until the devices get so small or close together that direct tunneling may occur.

On the negative side, however, is the high cost of SOI starting material, particularly silicon-on-sapphire (SOS) wafers, and the added cost of SOI processing. Consequently, as SOI technology develops further, its acceptance will increasingly depend on the balance achieved between the density and performance advantages it offers and the cost of deviating from standard (bulk silicon) processing.

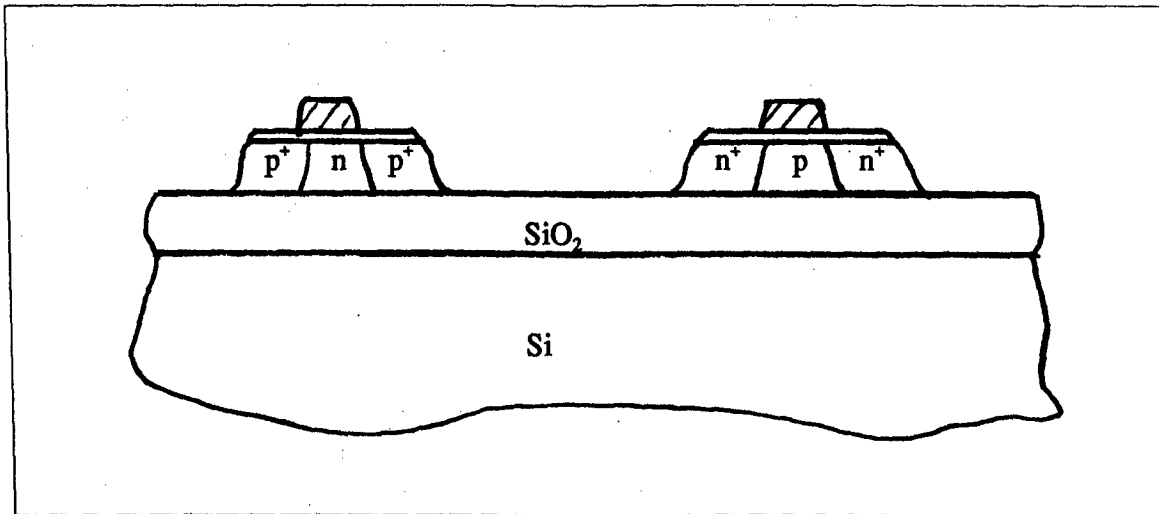
To further advance rad-hard device technology as well as help keep SOI/SOS technology in the competition with bulk Si technology, continued DoD support of this area will be necessary, aimed primarily at:

- Continuing the drive to smaller SOI geometries, maintaining competition with bulk silicon.
- Demonstrating the manufacturability of these device structures.
- Proving their reliability by demonstrating that there are no new unique failure mechanisms in SOI.
- Assuring a supply of qualified SOI materials.



## 2. Background

Traditional bulk Si technology is showing signs of limitations for future high speed requirements. One promising alternative involves epitaxially depositing Si on an insulating base of  $\text{SiO}_2$ . An example of a typical SOI (silicon-on-insulator) device, a CMOS inverter built in a thin Si film on  $\text{SiO}_2$ , is shown schematically in Fig. 8.



**Fig. 8. Schematic cross-section of two transistors comprising a CMOS/SOI inverter.**

The SOI concept has its roots in silicon-on-sapphire (SOS) technology, which RCA developed in the 1960s and 1970s for high-speed commercial applications—but which owes its survival to its superior hardness characteristics. Although it never caught on commercially, SOS continues to be the technology of choice for applications where radiation hardness (improved immunity to ionizing radiation) is essential.

SOI permits near-total electrical isolation of devices, smaller junction areas and, consequently, circuits that are "harder," denser and almost twice as fast as bulk Si devices. Specifically:

- Because there is no carrier mobility from the underlying Si substrate to the epitaxial layer, which is what interferes with normal device operation under alpha particle radiation, SOI offers three to four orders of magnitude improvement in SEU (single event upset) and transient radiation hardness relative to bulk silicon. (This radiation resistance results from the carriers being trapped under the oxide, unable to reach the surface epilayer where the active circuits reside.)
- SOI can provide CMOS and BiCMOS device densities that are 30% greater than comparable bulk Si densities without having to decrease device geometries. This is possible because there is no need to devote substantial real estate to the

insulating oxide trenches and other dielectric isolation structures now used to prevent latchup between nearby devices. (The SiO<sub>2</sub> layer itself prevents latchup.)

- The high voltage and isolation characteristics of SOI will permit integration of bipolar and CMOS devices on the same substrate and even allow fabrication of power (up to 5 kV) integrated circuits with monolithically co-integrated logic circuits.

### 3. Competing SOI Approaches

Four SOI technologies are currently being pursued, each providing its own special set of characteristics:

- SOS: Established, most favored rad-hard technology. Relatively expensive, but offers the possibility of new applications in available material.
- SIMOX: The current preference of the SOI community. Offers versatility, present adequacy for CMOS and potential suitability for bipolar and BiCMOS.
- Bonded: Provides bulk-like microstructure and purity which may be needed for bipolar and advanced (closely spaced) devices.
- ZMR/ISE: Low cost process. Its microstructure appears to be acceptable for CMOS.

At this point, functionality has been demonstrated in all four of these materials. For example, working CMOS devices have been built in SIMOX, ZMR, and SOS structures, and bipolar devices have been built in SOS, bonded, and SIMOX structures. For further significant progress to occur, however, a much better understanding of these SOI materials and device structures will have to be achieved, particularly as regards:

- Yield and reproducibility related to material control.
- Definition and achievement of materials properties for higher density circuits.
- Determining minimum requirements associated with various applications.

It should be noted that despite what seems to be a do-or-die competition among these four approaches, there is not likely to be an ultimate single "winner." Chances are two or more of these materials will always be needed to satisfy different sets of requirements.

In the following sections, each of these SOI approaches will be described more fully, specific programs will be discussed, and the size and scope of current government-funded effort in this area will be indicated.

#### 4. SOS Technology

Silicon-on-sapphire (SOS) wafers composed of silicon films (0.4 to 0.6  $\mu\text{m}$  thick) grown epitaxially on sapphire substrates are commercially available from a few suppliers, including Union Carbide and Kyocera. Hewlett Packard and RCA pioneered early work in this area and even developed a few products for industrial and commercial applications; however, the economic forces of the late 1970s and early 1980s, combined with advances in silicon LSI/VLSI technology, caused the demise of the commercial SOS thrusts at those companies. In any case, 0.4  $\mu\text{m}$  thick Si film on sapphire remains the only fielded technology satisfying requirements in military and space electronics where radiation hardness is essential.

Burdened with keeping up with the pace of IC downscaling, SOS-material companies failed to invest adequately in thinner-film improvement techniques and in fundamental material studies relating to the Si/sapphire system. Although Hughes Aircraft did win a VHSIC Phase 1 contract focused on SOS implementation of VHSIC-class functions, the company failed to transition the results of its complementary VHSIC Phase 3 effort—aimed at "productizing" the SPEAR (Solid Phase Epitaxy and Regrowth) and DSPE (Double Solid Phase Epitaxy) material improvement techniques—to its pilot line/manufacturing operation at Carlsbad, CA. Hughes ultimately delivered to the Services under the VHSIC Phase 1 program a correlator and other functions in SOS, but failed to gain commercial acceptance of its 40K-gate array chip in SOS outside of a few rad-hard applications. Similar problems were experienced by the other military system houses skilled in SOS, including GE/RCA (another VHSIC Phase 1 contractor pursuing the SOS approach), Rockwell, Harris, and Westinghouse.

Several additional factors have impeded the commercialization of SOS, including: the high density of defects in the non-SPEAR and non-DSPE Si films, the relatively high cost of the sapphire substrates, wafer size limitations (four inches), the need for dedicated processing lines, and the fact that the scaling of device dimensions requires thinner ( $< 0.4 \mu\text{m}$ ) silicon films on sapphire, which in turn requires improved material techniques. Without these thinner films (100 nm), it will be difficult for SOS, which is still largely rooted in 10- to 15-year-old material technology—essentially thick silicon films ( $\geq 0.4 \mu\text{m}$ ) on sapphire—to evoke commercial interest for anything significantly beyond the few niche applications it has captured to date.

Despite the above-cited problems, the outlook for SOS does appear to be improving, thanks to the advent of 100 nm thin silicon films on sapphire and to the lessons learned from the VHSIC era, which clearly showed the need for:

- Early establishment of quality control to prevent unacceptable SOS material from getting into the device processing lines.
- Extensive use of feedback from the circuit designer (SPICE parameter extractor, for example) to the device technologist—and to the material supplier.
- Allocation of realistic, critical-mass resources to device processing development beyond those reserved for materials development.

- Timely availability of simulation and circuit design to demonstrate the applicability of the enhanced properties of the materials and devices—for example, analog to digital (A/D) converters; two-transistor, four-quadrant analog multipliers; MOSFETs and bipolars.
- Acceptable balance between performance enhancement and simplicity/cost of insertion.

As a result, SPEAR and DSPE material technology—which initially provided the 0.25 to 0.3  $\mu\text{m}$  thick films needed for VHSIC Phase 1 (1.25  $\mu\text{m}$ ) design rules—has since been advanced to the point where thinner material for 0.5 and sub-0.5  $\mu\text{m}$  ICs can now be demonstrated. (Present SOS products, at 1.25  $\mu\text{m}$  design rules, continue to be implemented in  $\geq 0.4$   $\mu\text{m}$  thick silicon films on sapphire.) These SPEAR and DSPE improvement techniques have allowed SOS to evolve toward higher-density, smaller-design-rule ( $\leq 0.5$   $\mu\text{m}$ ) circuit applications; moreover, the prospective fabrication of 100 nm silicon film on sapphire promises to provide GaAs-class speed and radiation hardness (transient, SEU and neutron) at low power dissipation using low-cost silicon-based IC manufacturing technology.

Driven by military system requirements, DSPE-improved thin film silicon (TFS) on sapphire has been demonstrated in several application areas, extending down to 0.2  $\mu\text{m}$  minimum-feature-size analog and digital VLSICs, such as:

- A/D converters (4 bit, 2 Gbps; 16 bit, 100 Msps)
- Analog/artificial neural networks ( $10^3$ -synapse, 30-neuron self-learning arrays)
- Various computing devices
  - 16 x 16 multipliers
  - Very high speed SRAM (access time as low as 450 ps)
  - Low noise, high speed op amps ( $f_t = 4\text{-}5$  GHz, slew rate = 2.5 V/ns)
  - Digital filters

These high-performance complex circuits, recently demonstrated in this technology (in some instances with high yield and reliability), confirm the inherent scalability and simplicity of fully depleted structures, especially as applied to deep-submicron design rules.

##### 5. SIMOX Approach

To produce SIMOX (separation by implantation of oxygen) material, ion implantation of oxygen is used to form a buried insulating layer of  $\text{SiO}_2$  in a Si substrate at an energy of about 200 keV. Since two oxygen atoms are needed for each Si atom, a dose of about  $1.8 \times 10^{18}$  ions/cm<sup>2</sup> is nominally used. To preserve the crystallinity of the Si surface, the wafers are preheated and maintained at 600-625°C during the implantation. The material is then annealed to chemically bond the  $\text{SiO}_2$  layer and recrystallize the Si surface.

Device fabrication typically begins by implanting the buried layer in a lightly doped p-type wafer. Epitaxial Si is then grown to a starting thickness of about 0.5  $\mu\text{m}$ . Because of the configuration, no npn devices can form, and therefore latchup cannot occur.

Despite a susceptibility to carbon impurity and other problems, SIMOX offers several attractive characteristics. For one thing, SIMOX does not need to be thinned; the SIMOX process can be carefully controlled to provide the desired as-implanted Si thickness. In CMOS applications, for example, SIMOX and SOS do not require thinning of the Si layer down to about 0.2  $\mu\text{m}$ —nor down to 0.08  $\mu\text{m}$  for fully depleted devices.

Besides adding to cost, the thinning step adds another complication: maintaining thickness uniformity as the layer is thinned. Whereas nonuniformity of the initial (pre-thinned) topography is generally a smaller percentage of the total thickness, the same topography may result in a nonuniformity that is an unacceptably large percentage of the total thickness after thinning. Since fully depleted MOS devices require very thin ( $< 0.10 \mu\text{m}$ ) Si layers, maintaining thickness uniformity can be a difficult problem in the case of those device structures. (Thin Si layers are needed in such devices to minimize source/drain parasitics, hot carrier effects, and short-channel effects, all of which reduce speed and output current.)

In general, whether for military or commercial applications, SOI materials with silicon thickness less than 0.15  $\mu\text{m}$  are desired in order to achieve the advantages of high speed, high packing density, superior cost/performance trade-off, an ability to scale to deep-submicron geometries, simple processing, and, as stated above, an ability to produce fully depleted device structures. Such materials will also be best able to satisfy requirements relating to radiation hardness and manufacturability while still delivering reasonably high performance at relatively low cost.

Looking ahead to the future, the use of silicon epitaxy on SIMOX (and SOS) should be able to satisfy the requirements for bipolar processing, but it may require use of a triple-implant technique to handle the carbon impurity problem. Silicon thickness will continue to be adjustable by conventional epitaxial means. Meanwhile, high-quality thin films (80 to 100 nm thick silicon films on the insulator) should be able to provide fully depleted MOS device structures.

SIMOX material is currently commercially available in the U.S. from IBIS Technology Corp. (Danvers, MA), with TI readying a major capability as well. Harris Semiconductor and Honeywell also have projects under way. In addition, Japanese and European commercial suppliers are entering the field.

## 6. Bonded Wafers

In the bonded-wafer (or bond-and-etch) process, two Si slices are bonded together by a high-temperature furnace cycle. One of the slices is an  $n^+$  substrate on which an Si epilayer is grown. The other slice is oxidized and used as the mechanical support for the joined SOI structure. After the two slices are bonded together at high temperature in an oxidizing ambient, the  $n^+$  layer is etched away and the epilayer is then polished to the desired thickness.

The bonded-wafer process allows a wide choice of oxide layer thicknesses, ranging from about 0.4 to 4.0  $\mu\text{m}$ . In contrast, oxide thicknesses achievable with the SIMOX process are typically limited to a narrow 0.3 to 0.5  $\mu\text{m}$  range. The thicker oxide layer available with bonded wafers suggests the possibility of a significant reduction in parasitic effects, compared to the SIMOX process.

Bonded wafers also exhibit relatively low leakage currents, suggesting suitability for advanced bipolar applications and potential attractiveness for some CMOS applications, such as very low-power or high-voltage circuits.

### 7. ZMR/ISE Material

Two new SOI processes, offshoots of the zone-melt-recrystallization (ZMR) technique, have been attracting a good deal of industry attention. One uses strip heaters, the other an electron gun, to recrystallize a layer of polysilicon atop a  $\text{SiO}_2/\text{Si}$  substrate.

Kopin Corp. (Taunton, MA) calls its proprietary strip-heater-based process Isolated Silicon Epitaxy (ISE). The process begins with a bulk Si wafer over which an oxide layer is thermally grown. The wafers then go into another furnace where a polysilicon layer is deposited, followed by a protective capping layer of deposited  $\text{SiO}_2$ . The movable strip heater is then passed slowly over the wafer surface to locally melt the polysilicon layer. The initially melted portion of the layer is held in contact with a single crystal seed so that the subsequent recrystallization results in a single crystal layer of silicon between the two oxide layers. The seed crystal can be the substrate itself if a small opening is made in the thermal oxide before the polysilicon deposition step. Finally, the top oxide layer is etched away, leaving a three-level structure: a Si epilayer atop  $\text{SiO}_2$  atop the Si substrate.

Applied Electron Corp. (Santa Clara, CA) has developed a proprietary high-current e-beam technology to produce SOI wafers. The process is similar to Kopin's ISE process, except that a high-power line-source electron beam, not a movable strip heater, is used to heat and crystallize the polysilicon film.

Both Kopin and AEC expect to be able to handle 8-inch wafers, produce Si layers as thin as 0.5  $\mu\text{m}$  and easily vary the thickness of the oxide layer. According to AEC, producing device-quality wafers with Si layers thinner than 0.5  $\mu\text{m}$  would require elimination of grain boundaries and marked reduction of defect density (to below  $10^6 \text{ cm}^{-2}$ ).

According to Kopin, both fast CMOS and rad-hard devices will probably require a 0.3  $\mu\text{m}$  Si epilayer atop a 1  $\mu\text{m}$  oxide; high voltage (up to 5 kV) devices will require a 2-3  $\mu\text{m}$  epilayer atop a 1-2  $\mu\text{m}$  oxide; and bipolar circuits might require 1.5-2  $\mu\text{m}$  epilayers atop a 1  $\mu\text{m}$  oxide. The company has reported relatively low defect densities on the surface ( $10^5$ - $10^6 \text{ cm}^{-2}$ ).

8. Examples of Current SOI/SOS Device Activity

a. 64K Static RAMs

64K static RAMs (SRAMs) have been built in SOS (0.4  $\mu\text{m}$  thick Si films) at GE/Harris and in SIMOX at TI and Harris (see Table 6). Honeywell, TI and Harris are also working under contract on 256K versions in SIMOX exclusively.

For example, in late 1989 Harris Semiconductor Corp. (Melbourne, FL) announced that it had built 64K SRAMs in SIMOX and SOS meeting SDIO Level I rad-hard conditions and was seeking next to meet Level II requirements. Harris is now building a 256K version and developing a 0.8  $\mu\text{m}$  rad-hard CMOS SOI process for high-density memories. Harris has been buying 4-inch and 5-inch SIMOX wafers from IBIS Technology and evaluating Kopin Corp.'s ZMR/ISE wafers.

**Table 6. Demonstrated SOI Circuit Capability**  
(64K Static RAM at TI, Honeywell, and Harris)

Total Dose	$> 1 \times 10^6$ Rads
Transient Upset	$> 5 \times 10^{11}$ Rads/sec
Single Event Upset	$< 1 \times 10^{-10}$ Errors/Bit Day
Access Time	$< 40$ nsec Post Rad
Static $I_{DD}$	$< 10$ nA, $V_{DD} = 5\text{V}$
Active Power	$< 150$ mW @ 25 MHz

b. Bipolar Devices

Bipolar transistors have been demonstrated in epitaxially deposited silicon layers on improved SOS materials under a cooperative program between the Navy and the Lawrence Livermore Laboratory.

c. Higher-Frequency Silicon Devices

In work performed at the Westinghouse Science & Technology Center (Pittsburgh), SIMOX technology has been combined with high resistivity FZ silicon substrates to extend the frequency range of silicon devices to 5 GHz, currently the lower limit of GaAs microwave device technology (see Fig. 9). Building on its initial SIMOX activity in the logic area, Westinghouse has moved from the development of a 16K SIMOX SRAM with 1.25  $\mu\text{m}$  gates (and current extension of that to 0.25  $\mu\text{m}$  gates) to the development of a silicon-based microwave device capability based on its so-called "MICROX" technology (see Fig. 10). According to Westinghouse, the use of MICROX technology in UHF-through-10 GHz applications could exceed its potential digital application by some 60% over the next 10 years.

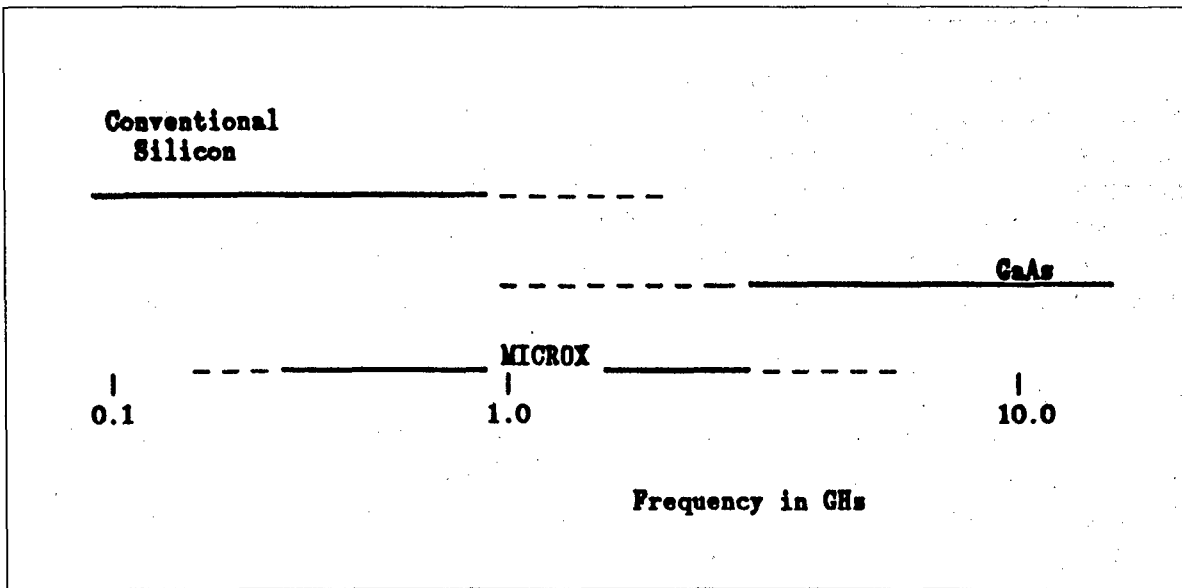


Fig. 9. Frequency range of present Si and GaAs technologies.

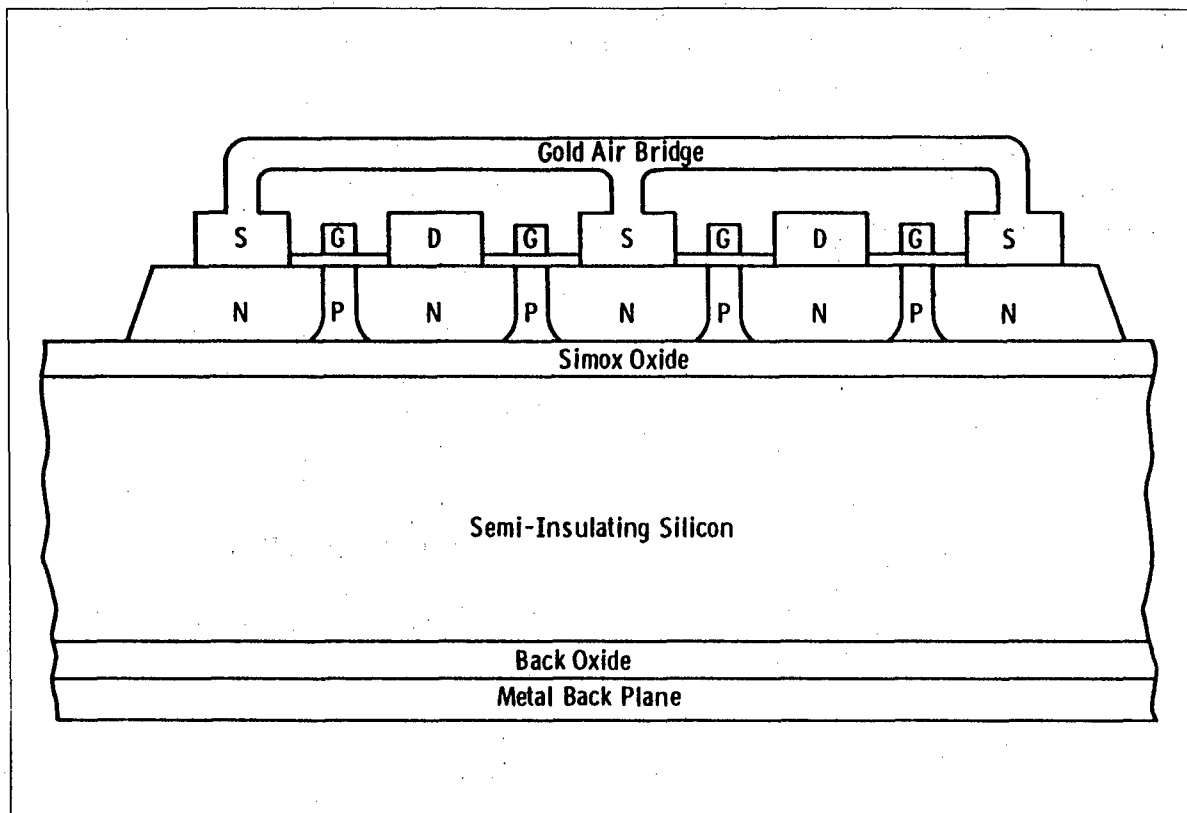


Fig. 10. Cross-section of Westinghouse "MICROX" transistor structure.



d. "Title 3" SOS Program

The U.S. Air Force and Army are collaborating on a Title 3 (critical material) program which was awarded competitively to Union Carbide. The objective of the program is to improve the manufacturability of radiation-hardened substrates (from Saphikon) for SOS device applications. The \$20M program, covering a period of five years, requires delivery of 5000 wafers per year. The David Sarnoff Research Center (Princeton, NJ) will evaluate the quality of the silicon films, which will be supplied in various silicon thicknesses (200, 300, and 400 nm). Both SDIO and DNA are closely monitoring the progress of this program.

e. Radiation-Hardened Power Integrated Circuits

Another possibility is the monolithic integration of SOI and bulk silicon technology to provide a radiation-hardened power integrated circuit (see Fig. 11). In this structure, the control circuitry is dielectrically isolated from the power structure, which is fabricated in the adjacent bulk silicon and capable of supporting up to 1000 V.

f. SOI and GaAs

SOI has potentially important implications for GaAs as well. On one hand, fully depleted SOI devices may eventually be able to compete effectively with GaAs devices in terms of speed and other factors. This was recently demonstrated by experiments with 500 angstrom devices at Toshiba, where a fourfold increase in speed was observed relative to that obtainable from an equivalent device in bulk silicon.

On the other hand, SOI can itself act as a substrate for GaAs heterostructures, as was demonstrated recently at Kopin Corp. Using an MOCVD process, the company fabricated n-channel GaAs-on-SOI MESFETs which exhibited a measured transconductance of 68 mS/mm for a 3  $\mu\text{m}$  gate length and 9  $\mu\text{m}$  source-to-drain spacing.

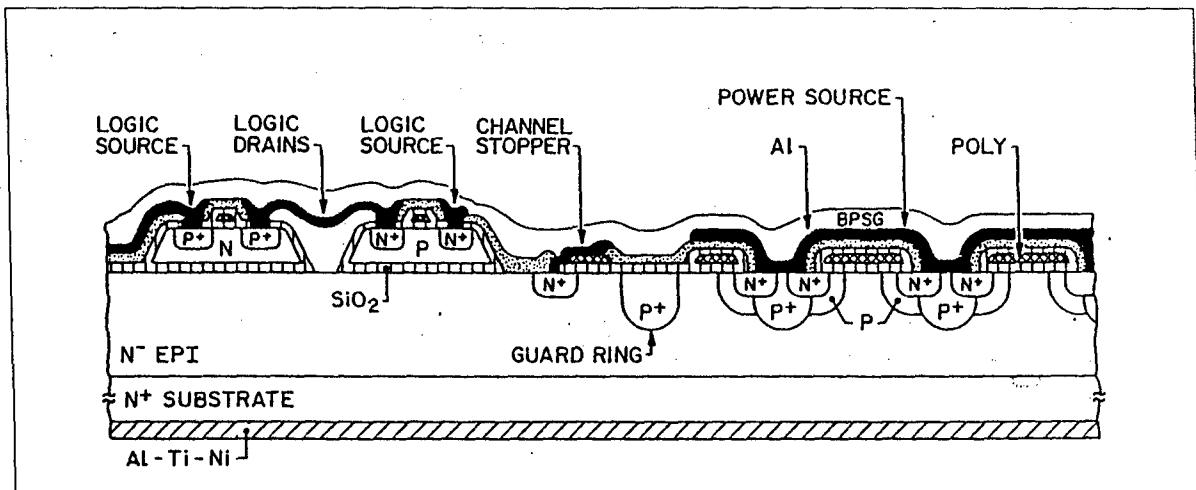


Fig. 11. Example of an SOI-based power IC co-integrated with logic circuitry.

9. Government-Sponsored SOI/SOS Program

As indicated in Table 7, the government has a fairly extensive program in SOI/SOS technology. It is important to recognize, however, that not all of the funding shown in that table supports materials work; a large percentage of the Honeywell 64K static RAM program (SDC/S081), for example, concerns device development. A more targeted summary of current government-funded SOI/SOS support, dealing mainly with materials and processing issues, is given in Table 8.

**Table 7. SOI Programs**  
(Funds in \$thousands)

<u>PROGRAM</u>	<u>AGENCY</u>	<u>FY90</u>	<u>FY91</u>	<u>FY92</u>
DSRC Mat'ls Characterization Methods	RADC/S081	250	200	250
IBIS/Honeywell SIMOX Process Dev't	RADC/S081	250	200	225
Allied Thin Film Bond and Etch SOI	RADC/S081	150	125	125
Spire SIMOX Process Development	RADC/S081	200	200	200
TI 64/256K Static RAM	DNA/S081	2,150	400	
Honeywell 64K Static RAM	SDC/S081	2,900	2,700	
Harris 64K CMOS/SOS Static RAM	SDC/S081	1,400		
TI 1M CMOS/SOI Static RAM	DNA/S081	1,750	1,750	1,750
TI/Spire SIMOX Mfg. Technology	WRDC/TEM	2,600	2,600	2,600

**Table 8. DoD Funding for SOI/SOS Materials Research**  
(6.1 funds unless otherwise noted; in \$thousands)

	<u>FY90</u>	<u>FY91</u>
N(ONR)	*100	*150
N(NOSC)	**750	**750
NRL Internal	600	600
A(ARO)	0	0
AF(OSR)	0	0
AF(RADC)	850	725
AF(WRDC)	†1300	†1300
Miscellaneous	††950	††950
Totals	4,550	4,475

\*Includes funds from DARPA, SDIO and DNA

\*\*6.2 funds

†Manufacturing Technology (7.8) funds

††6.4 funds

## 10. Worldwide Activity

Table 9 provides a rough estimate of the level and distribution of worldwide activity in SOI. Note that the Europeans are quite active in SOI technology even though radiation hardening is not a driving issue there. It is Marconi's view, for example, that one can get the same performance from an SOI device with 0.8  $\mu\text{m}$  critical spacings as from a 0.5  $\mu\text{m}$  bulk silicon device. This, it is argued, promises great advantages in terms of scaling limitations, equipment costs, manufacturability and first-pass yield.

**Table 9. Level of Activity in SOI/SOS**

- **Distribution of High Current Oxygen Implanters (as of Oct. 1989)**
  - 2 - United States
  - 2 - Japan
  - 1 - France
  - 1 - Germany
  
- **1989 SOS/SOI Technology Conference**  
(108 papers submitted, 77 presented)
  - 30 U.S. Industry
  - 10 U.S. University
  - 9 U.S. Government
  - 23 Europe
  - 5 Japan
  
- **Vendors Involved**
  - Potential circuit producers - TI, Honeywell, Harris, Marconi
  - IR&D - UTMC, Allied, IBM, Aracor
  - Material Development - IBIS, Spire

## 11. Summary

In order to remain competitive in SOI technology, the U.S. semiconductor community will need to develop a much fuller understanding of the SOI materials themselves—in terms of their basic properties, applicable processes and the relationship of those properties and processes to device performance. Although there appear to be no showstoppers looming, there are still some tough problems that need to be solved, relating to:

- Radiation hardness of edge devices without substrate bias. (This remains one of the advantages of the SOS approach.)
- Processing of very thin (< 0.10  $\mu\text{m}$ ) silicon for fully depleted devices.

- Materials microstructure/impurity control for deep-submicron devices.
- Development of needed diagnostic and quality control technology, capable of detecting low levels of carbon and heavy metals, defect levels, and small ( $< 1 \mu\text{m}$ ) surface particles in SIMOX.
- Determining the fundamental relationships between synthesis (production) variables, microstructure and impurity content, and device performance.
- Determining the material requirements—as well as optimum and lowest-cost materials—for  $0.5 \mu\text{m}$  feature-size devices, fully depleted devices, etc.
- Developing a mechanism for obtaining rapid feedback on the relationships between material properties and device performance.

#### D. Fluorides

##### 1. Introduction

Research over the last few years has shown that fluorides combined epitaxially with silicon and other semiconductor materials could well play an important role in future microelectronic devices. Potential applications include insulators in three-dimensional (3-D) or SOI devices, gate dielectrics in FETs, passivating layers in semiconductors lacking a native oxide, lattice-matching buffer layers, and electron beam resists that can be directly incorporated into a device structure. As a gate insulator, for example, epitaxial fluorides appear to offer atomically smooth interfaces, low interface state density, improved defect control and radiation hardness, and greater resistance to hot electron effects.

##### 2. Background

Because of their superior crystalline quality and close structural match to most of the important semiconductor materials, fluorides—particularly the Group IIA fluorides (see Table 10)—have been studied more extensively than any other potential epitaxial insulator. Epitaxial fluorides such as  $\text{CaF}_2$  could potentially provide:

- The possibility of new device structures
- Insulators in SOI or 3-D ICs
- Structurally characterizable interfaces
- 3-D heterostructures
- Buffer layers
- Dielectric isolation
- Semiconductor passivation
- Electron-beam resists

**Table 10. Fluorides and Associated Compatible Semiconductors**

<u>Fluoride</u>	<u>Semiconductor Substrate</u>
CaF <sub>2</sub>	Si, GaAs, Ge, InP
SrF <sub>2</sub>	Si, GaAs, Ge, InP
BaF <sub>2</sub>	Si, Ge, InP, CdTe, PbSe
Ca <sub>x</sub> Sr <sub>1-x</sub> F <sub>2</sub>	Si, Ge, GaAs
Ca <sub>x</sub> Ba <sub>1-x</sub> F <sub>2</sub>	Si, Ge, GaAs
Sr <sub>x</sub> Ba <sub>1-x</sub> F <sub>2</sub>	Si, InP, InAs
LaF <sub>3</sub>	Si, GaAs
CeF <sub>3</sub>	Si
NdF <sub>3</sub>	Si
PrF <sub>3</sub>	Si

However, before fluorides find widespread practical use in semiconductor devices, the following basic problems and physical limitations will have to be overcome:

a. Lattice Mismatch

CaF<sub>2</sub> has a lattice constant that is 0.6% larger than that of Si, and there are no fluorides that are more closely matched. As is the case with other heteromaterials, this lattice mismatch produces misfit dislocations in the resulting fluoride layers. In an attempt to deal with that problem, AT&T/Bell Labs has substituted some MgF<sub>2</sub> into the CaF<sub>2</sub> lattice to effectively reduce its mismatch relative to Si. However, because of the crystalline incompatibilities of the two fluorides and other problems, all such attempts to date have been unsuccessful. On GaAs, however, researchers have successfully grown mixed compounds since it is possible to provide exact lattice matching in that case—but only at a particular temperature because of the thermal expansion differences of the materials (see below).

Although the critical pseudomorphic thickness of CaF<sub>2</sub> on Si has not been measured directly, it is believed to lie somewhere below 100 angstroms. Films grown thicker than that tend to generate a considerable number of misfit dislocations, but it is still not clear whether those defect sites are electrically active.

b. Chemical Mismatch

Because of a chemical mismatch problem, it has not been possible to grow CaF<sub>2</sub> on conventional Si <100>. It turns out that the <100> fluoride does not like to grow with its <100> face exposed, so CaF<sub>2</sub> tends to grow three-dimensionally on Si <100>. On Si <111>, it will grow two-dimensionally fairly readily, however.

c. Thermal Expansion Mismatch

Another problem is the very large thermal expansion mismatch between these fluorides and most common semiconductors, particularly Si (see Table 11).

**Table 11. Linear Expansion Coefficients**  
( $\times 10^{-6}/K$ ; 270K)

CaF <sub>2</sub>	18.2	Si	2.5
SrF <sub>2</sub>	17.5	GaAs	6.9
BaF <sub>2</sub>	17.9	InP	5.6
		InSb	5.2
		CdTe	5

d. Ionicity Problem

The combining of epitaxial insulators, metals and semiconductors (for example, CaF<sub>2</sub>, CoSi<sub>2</sub>, and Si) into 3-D structures could provide major advantages in terms of ease of growth and low temperature growth. However, this use of epitaxial fluorides is likely to be seriously limited by their large ionicity and consequent susceptibility to ionic impurities.

e. Growth Asymmetry

It turns out that the crystallinity of Si grown on CaF<sub>2</sub> is not nearly as good as CaF<sub>2</sub> grown on Si. This is consistent with the general "rule" in heteroepitaxy that if it is easy to grow A on B, it will be difficult to grow B on A.

3. Potential Applications

a. Buffer Layers

This is perhaps the most immediately promising application area—that is, the use of epitaxial fluorides to provide either stress relief or grading between lattice constants. For example, in providing stress relief, one can either leave the fluoride layer strained and grow an unstrained semiconductor on top, or grow the fluoride thick enough so that the stress relieves itself. Through appropriate stoichiometry and the use of mixed fluorides, one could in principle combine semiconductors with widely differing lattice constants, including the III-V compounds (GaAs, InP, etc.) and Column IV semiconductors (silicon and germanium).

In addition, fluoride layers may also be used to separate chemically incompatible layers, although the practicability of that particular application is still unknown. Also unknown are

the effects of different crystal symmetries, the extent of interdiffusion effects, and the long-term stability of these layers in active devices.

b. 3-D Epitaxial Heterostructures

As stated previously, the integration of epitaxial insulators, metals, and semiconductors—such as  $\text{CaF}_2$ ,  $\text{CoSi}_2$ , and Si—has only begun to be explored. Although offering the advantages of easy, low temperature growth, the use of epitaxial fluorides in such structures is likely to be seriously limited by their high degree of ionicity, growth asymmetry, and different crystal symmetry, resulting in multiple epitaxial orientations. Clearly, if they are ever to be used as active elements, epitaxial insulators exhibiting far less ionicity will have to be developed. There is some hope that the work now under way in the area of high-temperature superconductors (see below) may accelerate the discovery of suitable materials. The ideal material would be some robust, single-crystal equivalent of  $\text{SiO}_2$ .

c. Other New Multimaterial Device Structures

The compatibility of epitaxial fluorides with both Si and GaAs could facilitate monolithic integration of GaAs and Si devices (see Section A). Here, electrical isolation would be provided by low-dielectric-constant epitaxial fluoride instead of a layer of undoped GaAs. Moreover, an epitaxial fluoride buffer layer could be inserted to localize and reduce the dislocations in the GaAs overlayer, which at present are too numerous ( $10^7 \text{ cm}^{-2}$ ) to permit fabrication of reliable minority carrier devices.

d. Dielectric Isolation

Interestingly, the original motivation for pursuing epitaxial insulators was mainly generated by interest in SOI applications. It was felt that epitaxial fluorides could be used to provide effective dielectric isolation of an SOI substrate because of their easy, low temperature growth. However, results were disappointing because of the poor quality of the semiconductor layer that could then be grown on them and because of the limited dielectric isolation actually achievable—owing to the sensitivity of fluorides to ionic impurities. Although the growth of semiconductor layers on epitaxial fluorides is still far from optimized, it remains doubtful that fluoride-isolated SOI devices will ever be as good as SIMOX devices.

e. Semiconductor Passivation

Because of their ease of growth and simplicity, epitaxial fluorides have been considered for passivation applications in semiconductor devices. However, the uncertain stability of these materials and their high sensitivity to ionic impurities have cooled interest in this particular application.

f. Electron Beam Resists

The use of fluorides as electron beam resists has been studied by several groups. The hope is to be able to combine the two steps, insulator and resist, into one, and through epitaxy

obtain good resolution. Thus far, resolutions of a few hundred angstroms have been demonstrated. However, developing these resists may prove to be difficult, and their sensitivity is likely to be inferior to other e-beam resists.

g. Superconductor Applications

BaF<sub>2</sub> has been used as both a substrate and buffer layer for high-temperature superconductor films. In 1989, improved transition characteristics were reported using MOCVD-grown BaF<sub>2</sub> as a buffer layer between MOCVD-grown YBCO films and a YSZ substrate. More recently, bulk BaF<sub>2</sub> was used as a high-T<sub>c</sub> substrate with very promising results. Several labs are now conducting research in these areas.

4. Review of Recent Activity

a. Fluorides as Buffer Layers

Besides grading mismatched lattice constants, fluoride buffer layers can be used either to provide strain relief or possibly act as diffusion barriers to effectively separate chemically incompatible layers. In the area of strain relief, research performed at SUNY-Albany, in collaboration with RPI and GE, has shown that a 2000 angstrom buffer layer of CaF<sub>2</sub> placed between a 7000 angstrom epilayer of GaAs and a Si substrate could essentially eliminate all strain from the GaAs layer.

As for using fluorides as diffusion barriers, not much work has been done in that area. However, promising research at AT&T/Bell Labs reportedly made use of a 600 angstrom mixed buffer layer of CaF<sub>2</sub> and SrF<sub>2</sub> to successfully block the cross-contamination that normally occurs in GaAs/Ge heterojunctions. The GaAs layer was 5000 angstroms thick.

b. Si Grown on CaF<sub>2</sub>

Despite the fact that it is more difficult to grow Si on CaF<sub>2</sub> than the other way around, the Tokyo Institute of Technology managed to achieve surprisingly good mobilities in a Si/CaF<sub>2</sub>/Si FET it recently built (see Fig. 12). Room temperature mobilities of 580 cm<sup>2</sup>/V-sec were measured, as compared to 700 for an all-Si control device. The main problem with this Si/CaF<sub>2</sub>/Si FET was its high leakage current, about 10 times greater than in the control device. Other problems included the nucleation of a large number of defects, having to deal with competing epitaxial orientations, and the need for high temperatures and acidic solutions in processing these devices.

It seems fairly certain that future progress in growing Si on CaF<sub>2</sub> will depend on the ability of researchers to improve the crystallinity of the Si epilayer. According to AT&T/Bell Labs, rapid thermal annealing of the CaF<sub>2</sub> before growing the Si may help, as may the use of ion beam deposition to get around the nucleation problem.



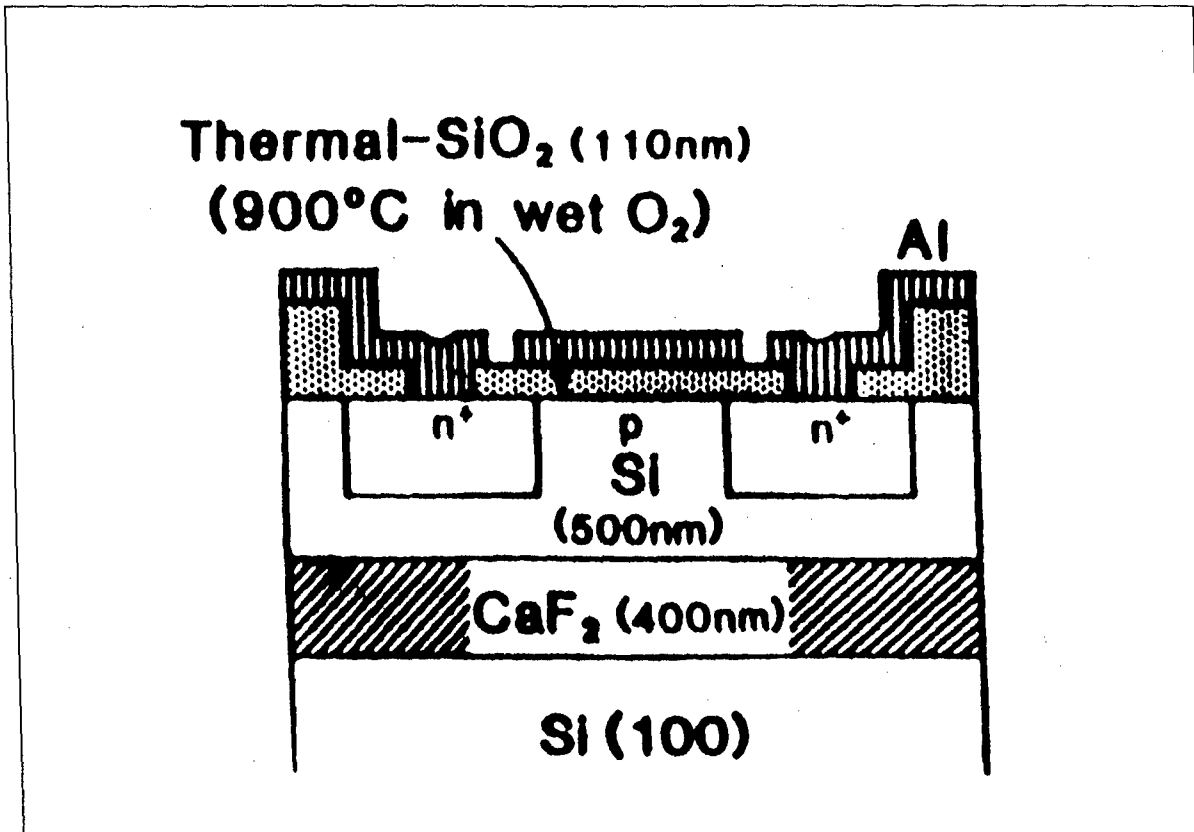


Fig. 12. Si/CaF<sub>2</sub>/Si FET built by Tokyo Institute of Technology.

c. Growth of Other Semiconductors on F/Si Layers

There have been attempts to grow other semiconductor materials on top of F/Si layers. For example, Ge and GaAs have both been grown on CaF<sub>2</sub>/Si and SrF<sub>2</sub>/Si structures, but there has tended to be problems with the crystallinity of the semiconductor overlayer. In attempting to overcome that problem, researchers at the Tokyo Institute of Technology found that electron beam exposure (at approximately 3 kV) of the fluoride prior to Ge or GaAs growth could dramatically improve the epitaxial quality of the semiconductor overlayer. It turns out, however, that even at small glancing angles the electron beam seriously damages the fluoride. In growing GaAs on CaF<sub>2</sub>/Si structures, that same group found that the growth was most successful when done on oblique surfaces such as <511>.

In growing GaAs or Ge on F/Si or Si/F surfaces, clearly something better than e-beam exposure is needed to improve the epitaxial quality of the top semiconductor layer. One possibility is rapid thermal annealing (RTA). It has been found that RTA performed at temperatures very close to the evaporation temperature of CaF<sub>2</sub> can significantly improve the structural and electrical properties of CaF<sub>2</sub>/Si systems.

In any case, much more work needs to be done in terms of electrically characterizing these semiconductor layers. For example, although Ge/CaF<sub>2</sub>/Si has much better crystallinity than Si/CaF<sub>2</sub>/Si, Ge has not been characterized electrically. The only thing known is that the Hall mobility is about 95% of the bulk Hall mobility. Moreover, Ge has not yet been grown on a lattice-matched fluoride; until that is accomplished it will not be possible to optimize the quality of Ge. Finally, work should be extended to SiGe, since by grading the lattice constant using combinations of Sr and Ca, one should be able to exactly lattice-match to whatever combinations of Si and Ge are desired. There has been no work reported on this anywhere.

5. Size and Distribution of Current Effort

Although encouraging results have been obtained in co-integrating fluorides and semiconductors, the electrical properties of CaF<sub>2</sub>/Si are still far from optimized. Moreover, there has been little organized effort to do so, at least not in the U.S. Most research projects here have been little more than existence proofs, with no serious effort made to coordinate, reproduce, or optimize the results. Consequently, despite the large number of research groups working in this area throughout the world (see Tables 12, 13 and 14), the possibility of combining epitaxial insulators, metals and semiconductors has only begun to be explored.

Table 12. U.S. Effort in Epitaxial Fluorides

INSTITUTION	SYSTEM	WORK	YEAR OF LAST PUBLICATION
AT&T Bell Labs	CaF <sub>2</sub> /Si	structure; electrical	1989
AT&T Bell Labs	F/GaAs	structure	1989
AT&T Bell Labs	F/GaAs	UV mirrors	1987
AT&T Bell Labs	F/InP	structure; electrical	1984
Case-Western Reserve U	CaF <sub>2</sub> /Si	theory	1988
IBM	CaF <sub>2</sub> /Si	structure	1989
Princeton	F/GaAs	structure	1989
RPI(GE)	CaF <sub>2</sub> /Si	structure	1989
SUNY-Albany	CaF <sub>2</sub> /Si	structure	1988
U. of CA-Berkeley	F/Si	structure	1989
U. of Oklahoma	F/Various	electrical; MOCVD	1989
Xerox PARC	CaF <sub>2</sub> /Si	theory	1989
Xerox Webster	CaF <sub>2</sub> /CdSe	structure	1986
Westinghouse	F/GaAs	structure	1988
U. of Texas-Austin	CaF <sub>2</sub> /Si	structure; MOCVD	1989

**Table 13. Japanese Effort in Epitaxial Fluorides**

INSTITUTION	SYSTEM	WORK	YEAR OF LAST PUBLICATION
Fujitsu	CaF <sub>2</sub> /Si	theory	1989
Kyoto U.	CaF <sub>2</sub> /Si	structure	1986
Mie U.	F/InAs	structure	1987
Nippondenso	CaF <sub>2</sub> /Si	pressure sensor	1986
OKI Electric	CaF <sub>2</sub> /Si	CMOS	1987
Optoelect. Int. Res. Lab	F/GaAs	structure	1987
Sanyo	CaF <sub>2</sub> /Si	structure; electrical	1988
*Tokyo Institute of Tech.	F/GaAs, Si	structure; electrical	1989

\* Largest effort anywhere (nine investigators). Fluoride on silicon work phasing out in favor of F/GaAs work.

**Table 14. European Effort in Epitaxial Fluorides**

INSTITUTION	SYSTEM	WORK	YEAR OF LAST PUBLICATION
CNRS-Grenoble	CaF <sub>2</sub> CoSi <sub>2</sub> /Si	structure	1989
CNRS-Toulouse	F/GaAs	structure; electrical	1988
* ETH-Zurich	II-VI, IV-VI/F/Si	structure; electrical	1989
Karl Marx U, Leipzig	F/GaAs	structure	1987
RSRE	F/Si	structure	1989
Tel Aviv. U.	CaF <sub>2</sub> /Si, Ge	structure	1986
U. of Manchester	BaF <sub>2</sub> (Ga,In)(As,Sb)	structure; electrical	1987

\* Most impressive work in Europe. Using fluorides as buffer layers to overcome very large lattice mismatches.

Most surprising has been the apparent lack of interest in this area on the part of DoD. Even though this technology could eventually have a major impact on the future performance of military devices and systems, there has been almost no DoD support of epitaxial fluoride research (see Table 15).

**Table 15. DoD Funding of Fluoride Research  
(in \$thousands)**

	<u>FY90</u>	<u>FY91</u>
N(ONR)	*150	*150
A(ARO)	50	50
Totals	200	200

\* Includes funds from SDIO.

#### 6. Summary

In summary, it is not yet known what the ultimate capabilities of fluorides in semiconductor structures may be, but it is fairly certain that they are more likely to be useful as relatively passive layers (buffers, for example) rather than as active layers. However, because of the potential usefulness of robust epitaxial insulators and metals, continued research is needed—both on fluorides and on less ionic epitaxial insulators. Specifically, work is needed in improving the quality of the semiconductor overlayers and in gaining a better understanding of the stress and aging properties of these structures.

According to AT&T/Bell Labs, where some of the most advanced  $\text{CaF}_2/\text{Si}$  work has been performed in this country, the following steps will need to be taken if further significant progress is to be made in establishing the electrical properties of these systems:

- Introduce clean room conditions during wafer cleaning and between growth and metallization. (The Japanese are well ahead in this area.)
- Institute in-situ metallization.
- Purify the fluoride sources.

#### **IV. CONCLUSIONS AND RECOMMENDATIONS**

The following are the conclusions and recommendations\* of the Advisory Group on Electron Devices—more specifically, AGED's Working Group B (Microelectronics)—based on the information gathered during the course of this study:

1. GaAs/Si structures may provide a critical element in future optoelectronic and electronic systems. Devices made using such heterogeneous structures may open the way to faster circuit switching times, forms of integration not achievable by other, more conventional means, and new device functions. To realize these advances, research and exploratory development efforts must emphasize a variety of approaches for improving the materials properties of GaAs films grown on Si. Full exploitation of GaAs/Si technology requires discovery of means for reducing the density of dislocations produced as a result of the inherent lattice mismatch at the GaAs/Si interface from approximately  $10^6$  to  $10^4$  defects/cm<sup>2</sup>. In short, GaAs/Si structures may open the way to enormous payoffs in electronics and optoelectronics integration if improved materials properties can be realized. The findings of this study indicate that progress is being made, as measured in terms of laser device performance. Other data presented indicate that selective deposition of GaAs islands on Si may be a more likely choice for deposited devices. Work on this technology is showing promising results and should be continued at current levels of effort (approximately \$1.6M per year).
2. High performance silicon-germanium (Column IV) devices are possible using heterostructures to modify band structures (for lower effective mass, improved mobility, etc.) or abrupt heterojunction interface structures (useful in heterojunction bipolar transistors) that have properties similar to those previously available only in compound semiconductor materials. The possibility of using Column IV technology to replace devices made using more exotic compound materials can ease processing problems in fabricating compatible microwave and optical devices (such as high efficiency photodetectors) on the same chip with conventional integrated circuit devices. Logic devices constructed from these heterostructured materials have speed-power performance beyond that attainable with conventional silicon devices. One heterojunction transistor development project has already demonstrated Si-Ge HBT's with cutoff frequencies of 75 GHz. Development of Si-Ge technology for fabrication of strained-layer quantum-well and other superlattice devices also looks promising. Increased research in this area should be encouraged—that is, the current rate of approximately \$3.5M per year should be raised to \$4.5M.
3. The study produced no clear resolution among the primary developmental SOI activities: BE (bond and etch), ZMR and SIMOX. SOS technology is still the best available radiation-hardened integrated circuit technology for many critical military applications; however, SOS remains more expensive than conventional (bulk silicon) processes—a

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\* Note that no attempt has been made to prioritize these conclusions and recommendations.

barrier to its attracting wide commercial interest. The successful completion of any of alternative SOI developments considered during this study would likely result in alternative device technologies to replace SOS technology in the long run for cost and flexibility reasons. Work in SOI technologies should continue at present levels—that is, at approximately \$4.5M per year.

4. The full potential of fluoride-on-silicon semiconductor technology is unknown but studies to date indicate that fluorides are more likely to be useful as relative passive layers than as active layers. Deposited fluoride materials together with metals and semiconductors may provide performance and density improvement alternatives to simple device shrinking (through nanolithography) and avoid voltage scaling problems. As these fluoride materials are at a primitive state of development, work should be continued at a modest level—approximately \$500K, up from the current \$200K per year—to sustain further development for evaluation.
5. Deposition technology is undergoing substantial improvements with the development of low-temperature epitaxy and remote plasma technologies. The potential impact of these developments on low-temperature processing of integrated circuits is substantial, as it would allow use of material combinations not now possible with processes requiring higher temperatures. In addition, defects induced by thermal cycling during fabrication can be substantially reduced. Work in this area is making good progress and should be continued.
6. The study did not cover alternative insulator materials or deposited ferroelectric and ferromagnetic materials (covered in an earlier Nonvolatile Memory STAR). New dielectric materials for denser DRAMs were also not considered, nor were materials treated in earlier STARs such as SiC and deposited diamond films. The recommendations of earlier STARs stand.
7. Multimaterial research can be advanced more rapidly through synergistic combination of both laboratory experiments and simulation techniques. Existing computer simulation is sufficiently well developed to predict characteristics of many heterostructures before they are fabricated.
8. Manufacturability of the deposition technologies being developed must be kept in mind early in the development activity—and certainly must be addressed before the technology is committed to high volume applications. Research activities in this process development area should look forward to equipment development options necessary to carry out the materials deposition processes with production process controls. Attention should especially be focused on process margins, throughput, impurity control and general compatibility with other process steps.
9. In order to ensure the most effective possible transfer of these new materials technologies, a strong effort should be made to disseminate the results of DoD-supported research—as well as an appreciation of the application potential of those results—to commercial and defense device producers. The Advisory Group recommends that, in addition to reliance

on the open literature and regular conferences, there be a series of research technology transfer conferences put on by DoD or an independent organization, such as SRC, to allow open discussion of the results of these Si-based multimaterial research efforts.

10. Stability of funding is a critical issue. A sustained, high-quality effort of modest size in these mixed material technologies, given their fabrication-intensive nature, will bear better results than research at a higher funding level that is periodically stopped and restarted. It is essential that planners of future development programs keep this in mind.

SPECIAL TECHNOLOGY AREA REVIEW (STAR)  
on  
MULTI-MATERIAL (SILICON-BASED) TECHNOLOGY

11-12 October 1989

AGENDA

11 Oct 89 at 1:00 pm

Keynote Speaker: Prof. James Harris, Stanford University 1hr15min

"Multi-Material Electronic Structures"

"GaAs-on-Si Lasers"	Prof. N. Holonyak University of Illinois	1hr
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"Co-Integration of GaAs and Si Circuits"	Dr. S. Shichijo Texas Instruments	35min
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"Challenges in GaAs/Si Integration"	Dr. Don Shaw Texas Instruments	35min
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12 Oct 89 at 8:30 am

"Fluorides on GaAs and on Si: U.S., Japan and Germany"	Dr. Julia Phillips AT&T Bell Labs.	1hr
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"Si/Ge Electronic Structures: Overview of Present and Potential Devices"	Dr. Kang L. Wang UCLA	1hr
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"SOI Technologies: Materials Issues and Military Applications"	PART I: Dr. Glenn Cullen David Sarnoff Research Center	45min
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PART II: Dr. Walter Shedd AF(RADC)	15min
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"SIMOX for Multi-Function Capabilities"	Dr. John Szedon Westinghouse Science and Technology Center	30min
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**SPECIAL TECHNOLOGY AREA REVIEW (STAR)  
on  
MULTI-MATERIAL ELECTRONIC STRUCTURES**

**11-12 October 1989**

**GOALS AND GUIDELINES**

Working Group B (Microelectronics) has been asked by DoD to recommend an investment strategy relative to multi-material (silicon-based) technology. Supportive of that undertaking, this STAR will seek answers to the following specific questions:

1. How critical is the systems need? Can it be satisfied by other means?
2. What critical components will this technology make possible? Are they achievable by other means/competing technologies?
3. What compromises in performance will accrue to the use of the technology?
4. What is the total amount of R&D activity in the field in terms of dollars, people and locations -- Government/Service, industry, academia? What is the level of activity in other countries?
5. What are the specific critical-path R&D and manufacturability problems that need to be solved? Are there any showstoppers?
6. What is the probability that solutions will be found? What will it cost?
7. What industry infrastructure needs to be created to make this a mature, manufacturable technology?
8. Is it likely that this will become a commercial technology? Why?
9. What, specifically, should be the role of SOI in DoD applications -- and the role of SOS?
10. Is there a commercial role foreseen for SOI?