REPORT OF
DEPARTMENT OF DEFENSE
ADVISORY GROUP ON ELECTRON DEVICES

SPECIAL TECHNOLOGY AREA REVIEW ON ELECTRONICS PACKAGING

JULY 1993

OFFICE OF THE UNDER SECRETARY OF DEFENSE FOR ACQUISITION
WASHINGTON, D.C. 20301-3140

THIS REPORT IS A PRODUCT OF THE DEFENSE ADVISORY GROUP ON ELECTRON DEVICES (AGED). THE AGED IS A FEDERAL ADVISORY COMMITTEE ESTABLISHED TO PROVIDE INDEPENDENT ADVICE TO THE OFFICE OF THE DIRECTOR OF DEFENSE RESEARCH AND ENGINEERING. STATEMENTS, OPINIONS, RECOMMENDATIONS, AND CONCLUSIONS IN THIS REPORT DO NOT NECESSARILY REPRESENT THE OFFICIAL POSITION OF THE DEPARTMENT OF DEFENSE.

CONTENTS

I. EXECUTIVE SUMMARY 1

II. INTRODUCTION 1

III. TECHNOLOGY PERSPECTIVE 2

IV. FINDINGS AND RECOMMENDATIONS 4

V. TECHNOLOGY STATUS, ISSUES, AND PROBLEMS 8

- DESIGN 8
- DEVICE PROTECTION 10
- INTERCONNECT 10
- SUBSTRATES 11
- TEST 11
- QUALIFICATION AND RELIABILITY 12
- STANDARDS 13

VI. CURRENT PROGRAMS SUMMARY 14

VII. CONTRIBUTORS AND PARTICIPANTS 19

VIII. REFERENCES 21

I. EXECUTIVE SUMMARY

Electronic packaging technology dictates the cost, performance and reliability of almost all future commercial and military electronics equipment. These equipments will be the marketable products of an electronics industry which is projected to grow to 2.0 trillion dollars by the year 2000. A strong and growing dependency exists between our national defense capability and this electronics industry.

Electronic packaging has traditionally been a shared responsibility of several industry sectors and specialty vendors. The packaging of integrated circuits constitutes a significant fraction of the product value provided by the device manufacturer, and additional value is added by circuit board specialists, frame manufacturers, subsystem and system assemblers, cable and connector companies and others involved in packaging the electronic equipments.

New packaging technologies, which utilize minimally protected die of increasing complexity and fine line integrating substrates to achieve higher packaging densities, are reshaping the contributions of the various industry sectors. Each involved industry sector, including defense electronics, recognizes these changes and is adjusting to retain a significant future packaging role.

However, the resulting plans and investments of both industry and government are unbalanced and lack coherence. DoD, with its strong and growing dependence on electronics, should, in its planning, coordination, and cooperative efforts, undertake to unify the various defense and industry efforts into a coherent plan that responds efficiently to the defined needs for electronic packaging.

This report makes specific recommendations for (1) a coordinated plan for industry and defense, (2) significant augmentation of specific packaging technologies, (3) market initiative assistance, and (4) a timely response.

The Advisory Group recommends that the DoD initiate a major effort to implement the recommendations of this report. In size and duration, it should be on the order of the VHSIC and MIMIC programs, managed in much the same fashion, with strong involvement of the military departments. It should encompass the related elements of computer-aided design, as well as packaging, with a clear emphasis on rapid insertion.

II. INTRODUCTION

Electronic packaging is the means by which components are housed, interconnected, and assembled to form useful systems. Packaging has traditionally been associated with the materials and joining technologies required to provide components, such as transistors, integrated circuits, resistors, inductors, and capacitors, with the physical protection and electronic connections that permit their assembly on printed circuit boards and into systems.

A modern definition of packaging requires consideration of not only the traditional packaging agenda but also input/output interfaces, data flow and timing, power and thermal management, advanced assembly concepts, and system architecture and partitioning issues associated with algorithm implementations.

Included within the scope of modern electronics packaging, as with all of electronics technology today, is a strong software element. Indeed, the success of any electronic packaging strategy will be vitally dependent on such software intensive items as design tools, modeling, simulation, test, compilers, language enhancements, data flow, and interface standards.

Modern electronics packaging also encompasses, at the highest level, the means by which the system interacts with users and with other systems, and with the platform on which it operates, while performing the signal or data acquisition, dispensing, processing, or actuation functions that electronics makes possible. For defense systems, these functions support communications, intelligence, weapons delivery, electronics warfare, surveillance, platform control, logistics, and management requirements associated with modern military forces and their missions.

Electronic packaging can be the major cost factor in a system. At the component level, the package cost often exceeds the cost of the integrated circuit itself. Moreover, the interconnections[1] which are an inseparable part of electronic packaging constitute the largest source of failures in electronic systems and are primary determinants of system cost and performance.

The advanced packaging technology that is the focus of this report centers around the assembly of a number of integrated circuits into one package instead of individual packages. This permits many chips to be interconnected into larger functional groups whose performance approaches the speed, reliability, and functional density of integrated circuits themselves. Concurrent important benefits, such as cost, reliability per interconnection, and improved availability, are associated with the advanced packaging technologies considered in this report.

The importance of electronic packaging for performance, cost, and reliability enhancement of all types of electronic systems was an underlying premise of the Special Technical Area Review on Electronic Packaging Technology. A wide range of industry and government initiatives directed to advanced packaging technology were reviewed and discussed. These included major programs in the military departments, investments by the DoD agencies, major packaging investments by the electronics industry and university programs. In addition, information from the activities of industry committees[2] and ad hoc groups was considered.

The STAR had excellent participation[3] from the technology community and from the electronics industry and provided a rich perspective on the technology for this report.

III. TECHNOLOGY PERSPECTIVE

Electronic component density improvements have driven progress in the electronics equipment industry. Density increases simultaneously improve performance, cost and reliability, and the integrated circuit industry has demonstrated this repeatedly as it evolved from a few gates per

---

[1] "Interconnection Technology," AT&T Technical Journal, July/August 1987

[2] Packaging & Interconnect Groups, see reference for complete listing

[3] Special Technical Area Review on Electronic Packaging Technology Summary, March 1992

integrated circuit to the millions of devices in today's complex products. Each evolutionary step in circuit density was accomplished at a constant cost and reliability per part and with a resultant improvement in the cost and reliability per unit electronic function. This has been sustained over five orders of magnitude improvement in integrated circuit density. This incredible progress has been the result of technological advances in shrinking the physical dimensions of the transistor and the interconnections between devices.

The increased complexity of integrated circuits and their fabrication processes necessitated the development of design tools for modeling, simulation and physical layout. Resulting design systems not only solved the complexity challenges, but also held non-recurring engineering costs in check.

Until the mid-80s, integrated circuit density improvements, coupled with conventional printed circuit board technology, met all the performance, cost and reliability needs of the electronic equipment industry. In 1985, the high performance computer industry had reached a state with its products where newer, high density packaging techniques, electrical interconnect external to the chip, thermal design, and electrical power and ground management had reached parity in importance with the individual integrated circuits in meeting market needs. Japanese and European mainframe computer companies emulated these high density packaging advances and quickly developed and marketed similar products. The rest of the electronic equipment industry essentially dismissed this technological advancement on the basis that it was unaffordable except for high performance mainframe computers. The military electronic equipment industry, whose products are characterized by performance and costs, similar to mainframe products, also dismissed the technological advancement, but for a very different reason. The infrastructure was not available to support its adoption.

For some seven years since that computer mainframe demonstration of advanced packaging technology, the electronic equipment industry has continued to improve conventional packaging technology and to hold off user adoption of packaging advances for reasons of risk and cost. While this strategy has met their on-going needs, the electronic equipment industry now recognizes the necessity of utilizing advanced packaging in its products or risking future markets.

The semiconductor industry, on the other hand, has reached the point where integrated circuit products have become too large or complex to support constant cost and reliability per product. The density driver paradigm is in jeopardy of breaking down at the integrated circuit level. Device density still enjoys a strong growth curve; however, the ability to interconnect, power up, and thermally manage these devices in integrated circuit product form has become a potential barrier. This was clearly brought into focus in the November 1992 Semiconductor Industry Association (SIA) Technology Workshop. The semiconductor industry must address the need to depend on advanced packaging technologies to provide an increasing part of the interconnect, power and thermal management functions. This prospect will be exacerbated by the fact that, because of their complexity, such future products will become much more user specific and therefore must face smaller market volumes.

This cursory description of the industry's evolution clearly highlights the merging, in a product sense, of two facets: (1) the interconnect external to the integrated circuit and (2) the next generation integrated circuits. It also points to potential changes in who will produce and market tomorrow's advanced electronics products. However the industry may evolve, the following is clear. Components, assemblies of components, and product level support for these assemblies have reached

a level of complexity, performance, reliability, cost and competition that demands heretofore unheard of user-supplier cooperation.

The current users of advanced packaging technology are vertically integrated in that they are both supplier and user, or that they have in place strategic alliances with suppliers. They have developed their own infrastructure to design, develop, manufacture and market their electronic equipments. This user vertical integration, represented by the computer mainframe industry, is extremely expensive.

Recent strategic changes within major corporations demonstrate this very clearly. In essence, they are disseminating advanced packaging technology to recover the cost of the supporting infrastructure. In related activities which reflect the need to spread supporting costs across a broad spectrum of users, the Electronic Industry Association has established a formal packaging interconnect industry subgroup with the primary goal to develop the infrastructure for advanced packaging technology for a broad class of users. Also, the European community, in conjunction with U.S. industries, has established a High Density Packaging Users Group.

It seems clear from the foregoing perspective that the continued advancement and employment of the technology, for both military and commercial purposes, requires the national orchestration of a range of users and suppliers, particularly in regard to their interfaces and standards required to facilitate the development and introduction of the technology. This is especially true in light of the fact that continuing advances in design, modeling and simulation will decrease the need for prototyping and allow the selection of individual hardware technologies from the world-wide marketplace of suppliers.

IV. FINDINGS AND RECOMMENDATIONS

A strong and growing dependency exists between our national defense capability and the electronics industry. Military electronic equipments which rely[4] exclusively on this industrial base not only provide defense capabilities, but also pace the high performance aspects of the electronic equipment marketplace. Today electronic packaging, particularly for silicon integrated circuits, is identified as an area of great opportunity for system performance enhancement for both defense and commercial applications and will determine the competitive posture of both military systems and the U.S. electronics industry in the next decade. The close linkage between U.S. commercial and defense interests was identified by government and industry leaders on the National Advisory Committee on Semiconductors in their third annual report.[5] The committee stated that "In view of the critical linkages that tie semiconductors to electronic systems (and) to high-technology industries...the Nation must move decisively to maintain a robust future for semiconductors...." *High-performance, low-cost packaging was identified as a highest priority area in their report.*

---

[4] Defense Science Board Report, Defense Semiconductor Dependency (Feb. 1987).

[5] The National Advisory Committee Report on Semiconductors, Attaining Preeminence in Semiconductors, Third Annual Report to the President and Congress (Feb. 1992).

Similarly, the Advisory Group on Electron Devices, in its deliberations on technologies of strategic importance to the military departments, has identified electronics packaging and interconnect technology and the interdependent field of design to be of paramount importance to future military systems and, therefore, to command special consideration in technology investment strategies. The Advisory Group also recognizes the existence of many complicated business and market issues associated with this technology and its pivotal role in an electronics industry which is projected[5] [6] [7] to grow to 2.0 trillion dollars by the year 2000. While it is not a purpose of this report to deal with such issues, they are a necessary part of the perspective and in some respects are inseparable from the technology development itself.

This report makes recommendations in four areas: (1) planning and coordination; (2) specific technologies; (3) market development; and (4) timeliness. It also suggests a management structure.

PLANNING AND COORDINATION

Electronic packaging has traditionally been a shared responsibility of several industry sectors as well as specialty vendors. New packaging technologies are reshaping the contributions of the various industry sectors, and as these industries respond to change and maneuver to retain a significant future packaging role, they create uncoordinated and often overlapping technology plans and roadmaps. DoD, in its planning, coordination, and cooperative efforts, must undertake to unify these various defense and industry efforts into a coherent planning structure.

The need for defense electronics packaging capabilities that are derived from a leading commercial U.S. industry, the diversity of packaging interests and activities, and the recommendations of related studies all indicate that coordination of the investments and technical directions of DoD and industry is a necessity. This is a major finding of this report. The need is for a coordinated plan for both industry and defense.

The most significant goal for the DoD is to foster jointness through:

- joint planning and coordination of electronic packaging investments within the DoD and other government agencies
- formulation of a coordinated strategy with the U.S. electronics industry
- increased DoD participation in cooperative efforts with the industry in a broad range of hardware, software, standards, specifications, and testing activities.

SPECIFIC TECHNOLOGIES

Investments in selected areas are required to assure the timely availability of leading packaging technologies to U.S. defense and commercial systems. Priority areas requiring investment to obtain advanced packaging and interconnection capabilities include:

---

[6] G. Heilmeier, "The Microelectronics Age: End of the Beginning or Beginning of the End," keynote address presented at the Plenary Session of the Government Microcircuits Conference (GOMAC), Orlando, FL, Nov. 91.

[7] MCM Technology - A Critical National Issue, unpublished report, Aug. 92.

- hardware and device technologies with emphasis on digital multichip assemblies (MCA)*
- software tools that support rapid design, simulation, test and acquisition of electronic assemblies
- system level interface tools
- manufacturing tools
- technology and production demonstrations

Observations relating to the need for specific investments in these areas were developed during the review and are listed here. No priority should be attached to the order.

- The availability of protected and functional bare die (unpackaged integrated circuits) will drive the cost and acceptance of multichip assemblies.
- Test standards, procedures, and strategies for die, multichip assemblies, and other higher order assemblies have failed to keep pace and inhibit the introduction and use of new technology.
- Packaging CAD is an urgent need for managing advanced packaging technology and to accelerate its development and use.
- Core packaging infrastructure technologies in substrates, mechanical and electrical interconnect, assembly, and the like, are either weak or non-existent.
- Quality assurance specifications and standards must be restructured and industry-wide test methods developed to foster the introduction and use of advanced packaging technologies.
- The range of existing U.S. commercial advanced packaging capabilities must be made available to all potential users through a software design interface capability that protects proprietary interests.
- New and innovative technology developments in special substrates, 3-D interconnects, and collateral optical and microwave technologies are required to maintain a leading-edge capability.

MARKET DEVELOPMENT

A packaging strategy must take into account the changes taking place in industry as well as the development of technology. These factors will have a large influence on the probability of success of any investment strategy. Chief among them are:

- Remaking of traditional user-supplier relationships
- Market development

Since all levels of packaging, from component through equipment, add significant value, and hence revenue, and since the thrust of advanced technology will force some combination of the traditionally separate functions of semiconductor manufacturing, board suppliers, system/equipment

* MCA is used here as a more general expression of the common term MCM, multichip module.

assemblers, the uncertainty in what market strategy the various companies will adopt will be an impediment to attempts to build a coherent investment strategy.

Further, the high volume markets to which a "reordered" industry must look do not exist. The investment in design systems and specially prepared integrated circuits required to take full advantage of advanced packaging can only be justified by high volume markets, and this may constitute a barrier that is difficult to cross.

The DoD must serve as a prime mover in this area. Future military systems capability is critically dependent upon high speed signal processing for the majority of its system needs. The performance, affordability and timeliness of these advanced signal processors will be determined primarily by advanced electronics packaging and interconnect technology.

- A series of advanced technology demonstration vehicles is necessary to collect, demonstrate and validate the technology at sequential stages and to provide future development guidelines.
- A target high volume system must be selected for production as a "market ice-breaker" to ignite the commercial industry, much as the Minute Man program in the early 60's provided the same function for the fledgling IC industry.[8]

TIMELINESS

It has been asserted in discussions by senior industry and government technologists throughout the background development and preparation of this report that the time in which the U.S. must act to establish and maintain a superior market position is limited. One estimate places this time at three years.[9] The consequences of the U.S. not being a major developer and supplier of this technology have not been quantitatively assessed; however, examples[10] from other areas indicate that it is reasonable to conclude that the U.S. would lose direct and timely access to state-of-the-art electronics technology. There is a consensus of the participants that the recommendations in this report should be implemented as soon as possible.

MANAGEMENT

The Advisory Group recommends that the DOD initiate a major effort[11] to implement the recommendations of this report. In size and duration, it should be on the order of the VHSIC and MIMIC programs, managed[12] in much the same fashion, with strong involvement of the military departments. It should encompass the related elements of computer aided design, as well as

---

[8] The Institute for Defense Analysis, The Role of the Department of Defense in the Development of Integrated Circuits, IDA Report, P-1271 (May 1977)

[9] MCM Technology - A Critical National Issue, unpublished report, Aug. 1992

[10] The General Accounting Office, "Review of Allegations that U.S. Firms Are Being Denied Advanced Technology From Foreign Suppliers," GAO Report #NSIAD91-278.

[11] Existing contributing programs are summarized in Section VI of this report.

[12] The Office of the Under Secretary of Defense Acquisition, VHSIC Management Plan (DoD Letter)

packaging, with a clear emphasis on rapid insertion. Such an effort would be a logical progression from the VHSIC and MIMIC programs, and in the view of the Advisory Group, will have a more significant impact.

V. TECHNOLOGY STATUS, ISSUES AND PROBLEMS

Packaging serves a broad spectrum of user products that have diverse cost-performance needs. Some needs are common to all users, while other needs are representative of a smaller group of users. A recurring theme throughout the STAR and this section is that users must drive the process and that superior user-supplier relationships are critical.

The notion of "user groups" which appears in this section is a mechanism to facilitate the description, to define the nature and importance of the interactions between particular segments of the technology, and to stimulate thought on the need for such a mechanism to enhance the development and use of packaging technology.

This section provides a summary of the information developed during the Special Technical Area review. It also draws on related reports (references 13-28).

DESIGN

Elements of a structured, hierarchial design process are essential to advanced packaging. They are: identification and formal description of product constraint/attribute requirements that drive the design process; trade-offs in key product parameters at a high level of abstraction; and the simulation of all product components at appropriate levels of detail to ensure successful manufacture.

The elements of packaging relevant to computer aided manufacturing are: automated transfer of information between design, manufacturing, test and inspection; marketing and product support; provisions for coordination of engineering changes with all affected activities prior to release to determine the impacts of engineering changes on schedules, risk and cost; provision of transferable, simulatable, unambiguous descriptions of the products in standard formats; and the ability to easily incorporate new manufacturing and device technology into the production of new or established products.

Automated integration of the design and manufacturing processes must be accomplished. The electronics community is well on its way to implementing the design process using the VHSIC Hardware Description Language, VHDL. However, it is relatively new and practices and procedures must be standardized and linked to manufacturing, product support and marketing. The computer and information system industry is working on UNIX operating systems and open systems framework standards as well as windowing and graphics standards that will allow heterogeneous hardware and software to communicate efficiently. These various elements need to be integrated, demonstrated and analyzed to develop guidelines for their use and to identify enhancements/requirements for subsequent integrations and demonstrations.

Engineering information system requirements for an open, object-oriented data management system, reference 22, were developed as early as 1986 and are in prototype development by all of the

major CAD/CAE vendors. Significantly more interchange of information between tools is necessary. The major CAD/CAE vendors are rewriting their existing tool sets so that they will be more interactive; however, system requirement synthesis/partitioning tools and manufacturing interface tools are not being developed by the CAD/CAE vendors.

Synthesis/partitioning tools range in scope from the current commercial offerings known as "silicon" and "HDL" compilers to tools that could compile an MCA design to a number of MCA vendor's technologies "packaging compilers", synthesize processor architectures from behavior or algorithm specifications, synthesize integrated circuits from behavior specifications, and synthesize designs across multiple integrated circuits. All such tools eventually need to be integrated into a readily available commercial CAD/CAE framework.

Tool and methodology developments are needed for synthesis of components from behavioral specifications in the form of VHDL. The behavioral specifications designate the function and timing of the object being designed. The output of the tools should be VHDL descriptions of the synthesized components including timing attributes. The synthesis tool should support physical design, creation of manufacturing art work, either directly or through a bidirectional interface to/from a separate physical design tool. In other words, the Packaging Compiler interface to the manufacturing line. The tool should adjust the synthesized design's characteristics to account for the entity's final packaging format, that is, various types of single or multiple chip packages or board level wiring assemblies. The tools should either automatically or interactively partition the design across multiple components. Synthesized components must include automatically generated test structures and interfaces to the IEEE 1149.1 specification, "Standard Test Port and Boundary Scan Architecture." Test vectors and test waveforms should be automatically generated for each component. Formal methods are needed to verify that a completed design does indeed comply faithfully to its specification.

Packaging compiler tools automatically design and document the package for the multiple components identified. It takes in the component and packaging technology information from the manufacturers and generates the total aggregate of information to build the multi-chip assemblies and/or the board level package to integrate MCAs/components. It generates all information needed to analyze the package and to differentiate between, and even competitively assess, vendors/-manufacturers using various advanced packaging and interconnect technologies. As such, it can trade-off attributes such as performance, size, weight, strength, reliability, manufacturability, thermal management and cost. Properly structured, the packaging compiler interface to the manufacturing lines can provide the user competitive bid access to virtually any packaging technology, and at the same time protect the proprietary aspects of the manufacturer. Note that the interface can be established now, and the analysis, trade-off tools can be added later. This packaging compiler also supports the development of "MOSIS-like" capability which would significantly enhance the university, low cost, rapid prototyping research contribution to advanced packaging.

DEVICE PROTECTION

Benefits of MCAs come from the increased silicon volumetric efficiencies (throughput per unit volume) and the preservation of device speed throughout the packaging hierarchy. Techniques are being explored and products offered which mount devices on edge and even mount devices on top of each other. These approaches use minimally packaged, protected devices and many use bare, almost totally unprotected, devices. Minimally protected devices are integrated into MCAs which are difficult to test and rework. Finally, test and assembly equipments for minimally protected, small devices induce failures and yield loss and increase costs. All of these issues have been dealt with under the descriptor, Known Good Die (KGD). Although much progress has been made, many problems still remain to be solved, particularly if advanced packaging technology is to be cost effective (reference 19). Currently, the consensus approach to solving the KGD issues is to develop a series of negotiated user-supplier specifications for minimally packaged semiconductor die. This endeavor is being undertaken by the SEMATECH Task Force on Known Good Die.

Both organic and inorganic surface protective coatings are being developed to provide protection for bare die, to enhance the environmental protection of plastic encapsulated devices and to replace classical hermetic packages for MCAs. The inorganic silicon dioxide, silicon nitride, silicon carbide and amorphous silicon coatings applied directly to the semiconductor wafers may well have their maximum payoff as solutions to the KGD problems. Plastic packaging continues to improve and the general conclusion is that reliability concerns, associated with these plastic encapsulants, can be met with properly designed packages. A focussed effort to evaluate reliability, thermal management, and the benefits of emerging plastic packaging, like TSOPs and PTSPs from Japan, pre/post molded MCAs and chip-on-board (COB) is required. TSOP and PTSP types of minimal packaging may significantly impact KGD problems. A number of bare die and/or wafer level test and burn-in approaches are being explored (reference 19). It is necessary that one or more of these techniques become a commercial reality. There is a great need for new approaches since each of the approaches under development has disadvantages.

INTERCONNECT

Pin-in-hole and pin-grid-array interconnect provides both mechanical and electrical connection, but places unacceptable area penalties on the integrating substrate due to the large size of the holes. These approaches have limitations on the amount of heat that can be conducted through the interconnect to the integrating substrate. Area array interconnect provides maximum interconnect density at relaxed design rules. A robust technology base requires its further development, especially to provide the high I/O requirements of the future for both the signal interconnect, but perhaps more importantly the large number of power and ground interconnects to control noise and high speed "shielded" interconnect.

Area array interconnect also provides the highest density of interconnect, the lowest electrical parasitics, and the highest assembly yields. It is becoming recognized by, and available to, all users. Stress relief by underfill epoxies and compliant high aspect ratio solder columns and Coefficient of Thermal Expansion (CTE) matched packaging structures, assembly and test technology are, or have, removed most objections to accepting the technology. Third-party solder bump and TAB services

are increasing availability. Even printed wiring boards with improved via and interconnect densities are becoming available. Anisotropic conductive adhesives, elastomers, and epoxies are receiving increased research.

Advances in wire-bonding and TAB should not be ignored. Most advanced structures will be a mix of wire-bonded, TAB, and area array interconnection.

Mechanical interconnect approaches such as elastomers, "fuzz buttons" and interposers/sockets offer alternatives for device to MCA and MCA to board interconnect. Elastomers and "fuzz buttons" are particularly attractive in conjunction with land grid array, pad array carriers and C-4 structures. They also offer temporary interconnect for die burn in and test approaches. Their low impedance and ease of rework are major advantages. Industry and government applications should be identified and cost/benefit analyses and reliability data must be developed.

There is a need to focus on requirements and prioritization for optical interconnects. Clearly, optical interconnect has a role in high speed, wide bandwidth large area networks down to the backplane and even to the card level. Requirements below the card level are unclear. Requirements and priorities must be established in relation to the best area array electrical interconnect performance.

SUBSTRATES

Substrates to interconnect components within an MCA, and to interconnect MCAs, in the worst-case, need to meet three competing requirements: interconnect density, thermal and power management, and mechanical integrity. The user must trade-off these requirements against his point design product performance, reliability, and cost. Low and medium performance products allow multiple solutions which are ultimately driven by cost and reliability. High performance and high thermal flux products are best served by removing the heat directly from the devices, thereby requiring the integrating substrate to provide only the mechanical integrity and the interconnect density. Typically, substrates with 3-5 mil lines and spaces and blind and buried vias satisfy high performance requirements.

A choice of robust substrate technologies is extremely desirable to meet the varied user needs. For cost driven applications, an aggressive PWB and large area medium to high resolution lithography is warranted. Large panel, wet chemical plating of fine lines on PWBs is a very attractive concept. Substrate testing techniques and equipment also deserve consideration to reduce costs. For performance driven requirements, ceramic systems appear to be the substrates of choice for the future, particularly those compatible with MCM-D, high density interconnect, and the ability to support power and thermal management and mixed digital, analog and microwave designs. These ceramic substrate efforts should receive aggressive support, particularly since such support will help to develop the U.S. industry as a major world-wide supplier.

TEST

Judicious testing is important to the economic production of MCAs and the use of other advanced packaging technologies and yet there still does not exist a "turnkey" testing methodology. Given the increasing complexity of electronics designs, products and associated manufacturing

processes, thought must be given to overall Design for Testability, DFT, strategies and manufacturing cost including test, debug and repair during the initial stages of product definition. Without a coherent testing strategy, it is doubtful that advanced packaging technology will be fully utilized in future equipments/products. A common DFT strategy and capability is needed that addresses the entire product life cycle with a focus on: development of a "Best Practices" DFT requirements document; expansion of current industry boundary scan test vector generation product capabilities to include "partial" DFT designs; cooperation with established industry groups to expand the IEEE 1149.1 standard to support analog circuitry and at-speed testing requirements; and development of a minimum built-in-test specification at both the IC and MCA levels. Substrate testing needs include developing "true" four point resistance testing and non-contact test technology. Finally, MCA test alternatives, specifically in the areas of burn-in and complete at-speed electrical testing require definition and development.

QUALIFICATION AND RELIABILITY

Advanced packaging technology not only provides performance but it also provides enhanced reliability. The vision is the upward migration of silicon technology interconnect practices to engulf the entire electronic assembly. In principle, what has been done on the individual integrated circuit level can be extended to complete signal processors. As with integrated circuits, qualification and certification of manufacturing lines, rather than products, will reduce impediments to the adoption of commercial manufacturing practices for military equipments.

If the military is to become an attractive customer for commercial vendors, it must fully develop its endeavor toward the QML, Qualified Manufacturers List. Commercial and military users must also develop a position regarding the EIA 599 standard and international standards such as ISO 9000. The newly formed Electronic Industry Quality Council (EIQC) is leading the development of such a position. It will have the full support of the DoD, NASA, DLA, DOC, and ARPA.

Presently, a significant number of military microcircuits are acquired under the Qualified Parts List (QPL) Program. Part qualification requires testing large sample sizes to stringent, nonflexible requirements and extensive end-of-line testing to screen out defective devices. End-of-line screens provide a standard series of reliability tests for the industry. Although manufacturers continue to use these screens, many of the screens are impractical or need modifications for new technologies, and add little or no value for mature technologies. Also, the high cost and low volume of complex microcircuits being used by the military today prohibit testing large sample sizes required by the QPL system. Manufacturers have developed alternative ways of assuring the reliability of devices. The most important of these are Statistical Process Control (SPC) and in-line process monitoring. These alternative methods may address the same reliability concerns as the screens, but they are not properly assessed under the QPL system. This inflexibility in the QPL system resulted in the merger of the QPL, MIL-M-38510, into the Qualified Manufacturer's List (QML), MIL-I-38535. The QPL product in existence today will be supported, but all new product must be qualified under the QML system. Existing QPL product will be listed in a separate QPL section of the QML 38535 listing.

The QML Program provides assurance to the DOD user that the manufacturer has control of the entire manufacturing process, from design through final test. QML endorses use of best

commercial practices while still ensuring a product is capable of performing in harsh military environments.

In the QML approach, the manufacturer demonstrates to a validation team sufficient competence to generate effective tests to assure product quality and reliability for their baseline technology. After this validation, the manufacturer's test approach is documented in his Quality Manual (QM) and concurrent government approval of manufacturing and/or test changes is not required. MIL-I-38535, "General Specification for Integrated Circuits (Microcircuits) Manufacturing," and the proposed Option 4 of MIL-H-38534, "General Specification for Hybrid Microcircuits," have been created to define the criteria for this QML approach. These specifications will also be merged within the year resulting in a single approach for qualifying chips through multichip modules. The validation team is led by the Defense Electronics Supply Center (DESC) with support from other Government agencies and industry. Periodic verification of the QML operation is accomplished through review of the minutes and actions of the manufacturer's Technology Review Board which controls the technical operations. Presently, more than 50 manufacturers' processes (both hybrid and monolithic) are qualified under the QML program, and it now allows offshore assembly and test of fully qualified military monolithic microcircuits.

The DoD and the electronics industry are coordinating the efforts of several programs in order to create the framework necessary for the selection, procurement, availability, and use of plastic packages. These efforts include procurement mechanisms which allow the selection of reliable products from the commercial market, characterization of use environments, evaluation and transfer of technologies, and the coordination of these efforts with electronics manufacturers and customers.

Procurement is being addressed through the merger of MIL-M-38510 (QPL) into MIL-I-38535 (QML), and through the modification of MIL-HDBK-217 to provide reliability values for qualified PEDs. The specification merger will be completed by May 1993, and new values will be implemented as soon as qualification levels for PEDs are established. These will be updated as new data is generated.

The sponsorship and coordination of these activities is taking place through the combined efforts of the Services, DLA, DESC, OEMs and the component manufacturers.

STANDARDS

It is important to recognize the need to identify and develop industry standards which will facilitate the development and use of packaging technologies. For instance, the IEEE Computer Society provided JEDEC with a candidate set of MCA substrate sizes that were keyed to IC processing equipment. Such standards can have substrate processing cost advantages and, in turn, reduce the number of toolings required by, for example, the package suppliers, which would result in additional cost savings. The potential also exists for standardizing on area array interconnect grids with similar cost benefits. There are many other possible standardization areas such as voltage, I/O drive power, pad size, and pad metalization, to name a few. Specific steps should be taken for the early identification and adoption of standards.

VI. CURRENT PROGRAMS SUMMARY

This summary focuses on government-supported efforts. Industrial efforts are included by exception since much information is not available. It does not attempt to be comprehensive or include every current program. Major current programs are discussed individually or collectively, as appropriate. Broadly based programs, such as the ARPA Application-Specific Electronic Modules (ASEM) program, are not treated as entities; rather, they are referred to at the individual effort level within the functional categories. It should be understood that most programs span a range of technologies and may not be neatly categorized by technology and, further, that a number of programs are dynamic in terms of both funding and content. The figures herein are the best estimates that could be made at the time. Key application area demonstration efforts are included for completeness.

COMPONENT PROTECTION

Single chip or component packaging by plastic encapsulation or classical hermetic packaging is being aggressively pursued by the industry at large. Plastic encapsulation continually improves toward meeting harsher environmental needs, encapsulating MCAs, and reduced footprints with higher I/Os. Minimally packaged components, such as TAB and thin-small outline packages are being developed commercially and will impact the density and performance capabilities of higher level assemblies.

The Defense Logistics Agency initiated a new effort to enhance the utilization of advanced plastic encapsulation at about $0.5M/year.

The government is spending about $1.5M/year to develop surface protective coatings for components and MCAs and the Known Good Die Task Force to develop standard specifications for the procurement of KGDs.

Individual tasks within larger efforts are developing and demonstrating the merits of aluminum nitride hermetic packaging versus the classical alumina hermetic packages.

- ESTIMATED LEVEL OF EFFORT: $3M/Year

SIGNAL DISTRIBUTION

This area broadly includes interconnect, substrate, fidelity of signals, design, modeling, and test. By far, the most active developments are the adoption of commercial area array interconnect and printed wiring board technologies and the development of computer-aided design tools and frameworks.

A flip-chip solder bumping service is being supported at about $2-3M/year to supply bumped ICs in wafer or die form for flip chip bonding and/or for die burn-in.

A cooperative venture is supported by the Department of Commerce to develop and make available printed wiring boards. With industry matching funds, this effort is about $10M/year.

Both the DARPA ASEM and the Rapid Acquisition of Application Specific Signal Processors (RASSP) programs are aggressively supporting CAD and test. The ASEM CAD and test primarily supports advanced packaging at about $4M/year. The RASSP design effort is focused on the design,

simulation and modeling of signal processors which includes much more than advanced packaging; however, many aspects, such as the design framework, are directly applicable. The RASSP efforts are still being implemented.

A number of university centered efforts are modeling high speed interconnect. Some efforts are including the modeling of the power distribution system as well to account for its influence on noise and signal fidelity.

ARPA is supporting superconducting interconnect at about $5M/year that would allow the lossless routing of gigahertz signals at the board level.

A minimal amount of funds are applied to advanced interconnect technology, such as elastomers and other mechanical interconnect.

- ESTIMATED LEVEL OF EFFORT: $20/Year

POWER DISTRIBUTION

The 5-volt CMOS standard has already been replaced by 3.3 volts in commercial laptop computers. The semiconductor industry is rapidly moving to nominal 2-volt operation which will impact power and heat dissipation problems. The simultaneous switching of many devices requires the use of many I/O pads for good ground contact and to supply the large current surges and their associated noise. Decoupling capacitators are being designed and fabricated in the substrate for noise control. Fifty-volt backplanes are being explored for military equipments, making them compatible with commercial practices. High efficiency 50- to 5-volt DC-to-DC power conditioning modules are being developed as MCAs.

The government is only spending about $2M/year on power distribution. The commercial laptop computer industry will spend many millions over the next two to three years to develop two-volt power distribution.

HEAT DISSIPATION

With the advent of 20-watt ICs and the projection of 200-watt ICs, heat dissipation is seen as a formidable problem. The Semiconductor Industry Association has projected a maximum IC power of 40 watts, provided about 2-volt operation is available. There are two heat dissipation needs: the elimination of hot spots via good heat spreaders and the dissipation of high average thermal fluxes.

The government is spending about $2M/year on the development of diamond substrates which promises to help the elimination of hot spots. Other substrate approaches, such as silicon carbide, receive very little support in spite of their very low cost and immediate availability. Approximately $5M/year supports the development of Metal Matrix Composites (MMCs) for in-plane heat conduction and control of thermal expansion. About $1M developed the liquid flow-through card for the military, and it has been adopted by major systems program offices.

The commercial work station industry will enhance its thermal management tools. Closed cycle refrigeration may be necessary to avoid the inclusion of a liquid cooling input/output system.

- ESTIMATED LEVEL OF EFFORT: $7M/Year

APPLICATIONS/COST

The major programs attacking cost are focused on design and the utilization of commercial and/or multi-user MCA and board manufacturing facilities.

The design tools were discussed under Signal Distribution. The interfacing of these design tools to manufacturing centers is seen as a cost control approach wherein a design can be competed by several manufacturers to increase competition and to access commercial manufacturing lines. Approximately $1M/year is being provided to establish these design interfaces. Additionally, an Application-Specific IC (ASIC), MOSIS-like capability for MCAs, is being supported at about $2M/year to make MCAs affordable and widely available, particularly for the university research community.

Some five MCA foundries are being supported at a total funding level of $10-12M/year. These foundries are predominately commercial vendors which should provide lower cost MCAs. A very large commercial effort is being planned (reference 25) wherein processing and assembly equipment will be developed specifically for advanced packaging in contrast to the current practice of adapting obsolete IC processing and assembly equipment. The ASEM program is supporting the feasibility of a large area, medium to high resolution optical lithography approach.

The design tools, particularly the focus of the RASSP effort, should allow for the simulation and modeling of electronic equipments, greatly reducing, and ultimately precluding, the need to prototype [new and upgrade equipment designs]. This approach is seen primarily as an attempt to control costs and provide advanced performance through the cost effective and low risk insertion of state-of-the-art technologies.

- ESTIMATED LEVEL OF EFFORT: $20M/Year

APPLICATIONS/PERFORMANCE

Both the ASEM and RASSP programs have the objective of enhancing performance by providing the design access to advanced packaging technology and the rapid insertion of other system level technologies.

- ESTIMATED LEVEL OF EFFORT: $7M/Year

APPLICATIONS/RELIABILITY

Advanced packaging and interconnect technology has been proven to be more reliable. The focus of these programs is on the acceptance of advanced technologies by the users. Hence, the key objective of the Advanced Assembly and Packaging Technology (AAPT) and the RELTECH, government efforts are to develop the failure modes and test methods for advanced packaging and interconnect technologies. Once these are understood, then military specifications and standards can be altered to make them as compatible as possible with best commercial practices. These programs are only funded at about $0.4M/year.

Finite element and fracture mechanics analytical techniques are being supported by the government at about $1M/year. The success of these tools is dependent upon the characterization of

many materials and processes in their thin film state. Such materials work is woefully underfunded at about $0.5M/year.

- ESTIMATED LEVEL OF EFFORT: $2M/Year

DEMONSTRATION

Application-driven demonstrations of advanced packaging technology have been funded at about $10-20M/year depending on how the resources are prorated to packaging versus other development tasks. These efforts are represented by: Aladdin, ATCURE, SPPD and ASCM. Two are focused on smart munitions, ATCURE and SPPD, while Aladdin is viewed as a general purpose three-dimensional signal processor and ASCM is directed at space applications. These efforts have served to demonstrate to the users the performance enhancements available through the utilization of advanced packaging technology.

VII. CONTRIBUTORS AND PARTICIPANTS

M. Adler
General Electric Co.

James Armstrong
Virginia Tech

James H. Aylor
University of Virginia

John P. Beccone
AT&T Bell Labs

John Bedinger
Texas Instruments

Anthony F. Bernhardt
Lawrence Livermore National Lab.

Eugene C. Blackburn
Rome Laboratory

Robert Byrne
National Semiconductor Corp.

Robert C. Camilletti
Dow Corning Corp.

Grish Chandra
Dow Corning Corp.

Grover Coors
Adolph Coors

Gary L. Denman
DARPA

James DiNitto
Certification/Qualification Assoc.

Stan Drobac
nCHIP, Inc.

William Edwards
Wright Laboratory

John W. Evans
NASA HQ

Ron Evans
Nat'l Ctr. for Manufacturing Science

Martin G. Freedman
AMP, Inc.

Philip Garrou
Dow Chemical U.S.A.

Lance Glasser
DARPA

Simon E. Goldman
AT&T

John Gulick
Hughes Aircraft Company

Peter Hansen
Teradyne, Inc.

Frank L. Howland
Sematech

John Jackson
National Semiconductor Corp.

Linda L. Johnson
Defense Electronics Supply Ctr.

Robert T. Kemerley
Wright Laboratory

Joseph Key
U.S. Army Research Lab

William R. Lambert
AT&T Bell Labs

Christina N. Le
US Army NVEOD

Harry Lockwood
GTE Laboratories, Inc.

Capt. Jim Lyke
Philips Laboratory

Ingham Mack
ONT

Paul McCarley
Wright Laboratory

Archie Mones
Dupont Electronics

Ronald Naster
General Electric Co.

Chong Park
Kyocera America Inc.

Michael Pecht
CALCE Center
Univ. of Maryland

Rick Perko
M/A-COM

Gregg Pitts
MCC

David Polak
IBM-FSD

John L. Prince
University of Arizona

Jon Prokop
MCC

Pat H. Reaves
NCCOSC

William Riley
Research Opportunities, Inc.

Terry Ritter
nCHIP, Inc.

Bill Robinette
Digital Equipment Corp.

William E. Russell, Jr.
Wright Laboratory

Dean A. Schaefer
E-Systems

Dennis Seals
AT&T Bell Labs

John Shea
Shea Technology Group

John M. Segelken
AT&T Bell Laboratories

Robert W. Techentin
Mayo Clinic

Alan Tewksbury
Wright Laboratory

Clare Thornton
US Army Research Laboratory

Rao Tummala
IBM

Iwona Turlik
MCNC

Ranga Vemuri
University of Cincinnati

Stanley Wagner*
Wright Laboratory

Mauro Walker
Motorola, Inc.

Michael A. Zimmerman
AT&T Bell Labs

Chuck Zyetz
Aerospace Corp.

Jack Kilby
Chairman
Advisory Group on Electron Devices

John M. MacCallum, Jr.
Executive Director
Advisory Group on Electron Devices

* STAR organization and report preparation

VIII. REFERENCES

1. "Interconnection Technology," AT&T Technical Journal. July/August 1987.
2. Packaging & Interconnect Groups: EIA Subgroup on Packaging & Interconnect; High Density Packaging Users Group (HDPUG); RWOH Group; KGD Task Force; RELTECH; Advanced Assembly & Packaging Technology (AAPT) Group; National Strategic Research Planning Group; IEEE Computer Society, and MCM Size Task Force.
3. Advisory Group on Electron Devices. "Preliminary Summary of the Special Technical Area Review (STAR) on Electronic Packaging Technology." March 1992.
4. Defense Science Board. "Defense Semiconductor Dependency." February 1987.
5. National Advisory Committee on Semiconductors. "Third Annual Report to the President and Congress—Attaining Preeminence in Semiconductors." February 1992.
6. Heilmeier, George. "The Microelectronics Age: End of the Beginning or Beginning of the End?" Keynote Address, GOMAC Plenary Session. November 1991.
7. "MCM Technology - A Critical National Issue." Unpublished report. August 1992.
8. Asher, N.J. and L.D. Strom. "The Role of the Department of Defense in the Development of Integrated Circuits." IDA Report, P-1271. May 1977.
9. General Accounting Office. "Review of Allegations that U.S. Firms Are Being Denied Advanced Technology from Foreign Suppliers." GAO Report #NSIAD91-278. September, 12, 1991.
10. VHSIC Management Plan, DoD Ltr, January 1982.
11. Defense Science Board. "Use of Commercial Components in Military Equipment." June 1989.
12. SIA Technology Workshop, November 1992.
13. Seraphim, Donald P. and Donald E. Barr. Interconnect and Packaging Technology in the 90's.
14. Tummala, Rao (editor) et.al. Microelectronics Packaging Handbook. Van Nostrand Reinhold, New York (1988).
15. Seraphim, D.P., R. Lasky, and C. Yl Li (editors). Principles of Electronic Packaging. McGraw Hill. New York (1989).
16. Materials for High-Density Electronic Packaging and Interconnect. National Academy Press (NMAB-449) (1990).
17. Prince, John L. III. Packaging Strategic Research Plan Workshop Report (P92001). Semiconductor Research Corporation. January 1992.
18. Kurtz, B. "Electronics Packaging/Interconnect, The Next Crisis for Cost-Effective Military Electronics." HMRC Spring 1990 Meeting.
19. Hagge, J. K. "State-of-the-Art Multichip Modules for Avionics." SPIE/OPTCON-90, Boston.

REFERENCES, Continued

20. Messner, G. and J. Blade, I. Turlik and P. Garrou (edited by). Thin Film Multichip Modules. Electrochemical Press (1992).

21. "Multichip Integration, A Briefing Hosted by Industry." Senate Caucus Room, April 1992.

22. Linn, J.L. and R.E. Winner (Editors). "The Department of Defense Requirements for Engineering Information System (EIS), Volume II: Requirements." Institute for Defense Analyses. IDA Paper P-1953. July 1986.

23. Advisory Group on Electron Devices. "Special Technology Area Review (STAR) on Computer-Aided Design." (March 1993).

24. "International Quality Assessment Systems." HMRC Conference, December 1990.

25. Summerford, J. "MCM Development Roadmap—The EIA Perspective." Proceedings International Conference on Multichip Modules (April 1993).

26. Bergman, D. (editor). "Technology Roadmap Workshop for the Future of the Electronic Interconnection Industry." IPC, 5-7 April, 1993.

27. Electronic Industries Quality Council, North American, EIA Engineering News, January/February 1993.

28. Bergman, R. "Transformation of High Density Packaging Infrastructure." Proceedings International Conference on Multichip Modules (April 1993).