NAVAL POSTGRADUATE SCHOOL

MONTEREY, CALIFORNIA

THESIS

A GALVANICALLY ISOLATED POWER CONVERTER MODULE FOR DC ZONAL ELECTRIC DISTRIBUTION SYSTEMS

by

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March 2006

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REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503.			
1. AGENCY USE ONLY *(Leave blank)*	**2. REPORT DATE** March 2006	**3. REPORT TYPE AND DATES COVERED** Master's Thesis	
4. TITLE AND SUBTITLE: A Galvanically Isolated Power Converter Module for DC Zonal Electric Distribution Systems			**5. FUNDING NUMBERS**
6. AUTHOR(S) Stephen F. Sarar			
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey, CA 93943-5000			**8. PERFORMING ORGANIZATION REPORT NUMBER**
9. SPONSORING /MONITORING AGENCY NAME(S) AND ADDRESS(ES) N/A			**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**
11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.			
12a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release: distribution is unlimited			**12b. DISTRIBUTION CODE**

13. ABSTRACT (maximum 200 words)

The United States Navy is currently in a state of transition from mechanical to electric propulsion. Future warships, such as the new destroyer class, will contain an Integrated Power System (IPS) that provides power to all propulsion and ship service loads. These warships will likely have a dramatic increase in the number of power electronic loads, both AC and DC. For ship service loads, a DC Zonal Electric Distribution System (DCZEDS) will likely be used. DCZEDS requires a device that provides galvanic isolation between the feeder buses and the zones to prevent fault propagation between zones. For DCZEDS to be practical, DC-DC converters that provide galvanic isolation with an efficiency and reliability approaching that of existing low frequency AC isolation transformers must be placed between the feeder buses and the zones. This thesis examines the construction and operation of a prototype galvanically isolated DC-DC converter using commercial-off-the-shelf parts. The converter uses a single-phase high-frequency transformer link to provide galvanic isolation. This work shows that this converter topology is reliable enough to be used in an IPS. A three-phase solution using this topology can provide sufficient power density at the megawatt level, necessary for an interface converter in DCZEDS.

14. SUBJECT TERMS DC-DC Converter, Integrated Power System, Galvanic Isolation			**15. NUMBER OF PAGES** 93
			16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT Unclassified	**18. SECURITY CLASSIFICATION OF THIS PAGE** Unclassified	**19. SECURITY CLASSIFICATION OF ABSTRACT** Unclassified	**20. LIMITATION OF ABSTRACT** UL

NSN 7540-01-280-5500 Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18

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A GALVANICALLY ISOLATED POWER CONVERTER MODULE FOR DC ZONAL ELECTRIC DISTRIBUTION SYSTEMS

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March 2006

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ABSTRACT

The United States Navy is currently in a state of transition from mechanical to electric propulsion. Future warships, such as the new destroyer class, will contain an Integrated Power System (IPS) that provides power to all propulsion and ship service loads. These warships will likely have a dramatic increase in the number of power electronic loads, both AC and DC. For ship service loads, a DC Zonal Electric Distribution System (DCZEDS) will likely be used. DCZEDS requires a device that provides galvanic isolation between the feeder buses and the zones to prevent fault propagation between zones. For DCZEDS to be practical, DC-DC converters that provide galvanic isolation with an efficiency and reliability approaching that of existing low frequency AC isolation transformers must be placed between the feeder buses and the zones. This thesis examines the construction and operation of a prototype galvanically isolated DC-DC converter using commercial-off-the-shelf parts. The converter uses a single-phase high-frequency transformer link to provide galvanic isolation. This work shows that this converter topology is reliable enough to be used in an IPS. A three-phase solution using this topology can provide sufficient power density at the megawatt level, necessary for an interface converter in DCZEDS.

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LISTS OF SYMBOLS, ACRONYMS, AND ABBREVIATIONS

ABT	Automatic Bus Transfer
AC	Alternating Current
COTS	Commercial-off-the-Shelf
DC	Direct Current
DDX	Newest Destroyer Class
DSP	Digital Signal Processing
EDS	Electrical Distribution System
EM	Electromagnetic
EMALS	Electromagnetic Aircraft Launch System
FBC	Full Bridge Converter
FBI	Full Bridge Inverter
GIBB	Galvanically Isolated Building Block
GIFB	Galvanically Isolated Full Bridge
HFHE	High Frequency High Efficiency
IGBT	Insulated Gate Bipolar Transistor
IPS	Integrated Power System
NPS	Naval Postgraduate School
OP-AMP	Operational Amplifier
PCB	Printed Circuit Board
PID	Proportional, Integrative, and Derivative
PWM	Pulse Width Modulation

SSA	State Space Averaging
U.S.	United States
ZEDS	Zonal Electrical Distribution System

ACKNOWLEDGMENTS

This thesis would not have been possible without all of the support given to me by faculty, friends, and family. In particular, many thanks to Professors Ashton and Parker, for their invaluable help and support in writing this thesis.

To both Warren Rogers and Jeff Knight, those underappreciated NPS lab staff; I am deeply indebted to you both for all the practical hands on assistance you have provided me for the last two years.

The Physics department provided great help by providing thermal imaging during troubleshooting. Professor Walters was especially helpful in this area.

And lastly, my deepest appreciations to my wife Ellen, without whose support this thesis would not have been able to be completed.

EXECUTIVE SUMMARY

The United States Navy has concluded that future warships will become all electric. These warships will utilize an Integrated Power System with electric drive. The ship service distribution system will be a DC Zonal, which differs markedly from today's radial system. In order to achieve maximum survivability it is critical that electric loads be galvanically isolated from their common zone feed busses. Although transformers can be used for this purpose, they are inherently AC devices, and thus, not suitable for standard DC operation. This is a serious issue, as electric warships will utilize an increasing number of DC loads.

A DC-DC converter with galvanic isolation has been modeled, assembled and tested. This chosen topology, referred to as a Galvanically Isolated Full Bridge (GIFB), has been constructed as a prototype for use in the ship service distribution system of an all-electric warship. The GIFB is, first and foremost, a device that mimics the operation of an AC transformer for use by DC systems.

The GIFB consists of three main power components: a Full Bridge Inverter (FBI), a High Frequency High Efficiency (HFHE) transformer, and a Full-Wave Bridge Rectifier. The FBI utilizes Insulated Gate Bipolar Transistors (IGBT) and associated control circuitry to convert a DC supply voltage into a three step 20kHz AC waveform suitable of the HFHE transformer. The HFHE transformer is optimized for 20kHz and provides the desired galvanic isolation. The HFHE's primary windings are connected to the FBI and its secondary windings are connected to the Full-Wave Bridge Rectifier. The Full-Wave Bridge Rectifier converts the three step AC waveform back into DC for use by the load. A block diagram of the power section of the GIFB is shown below in Figure 1.

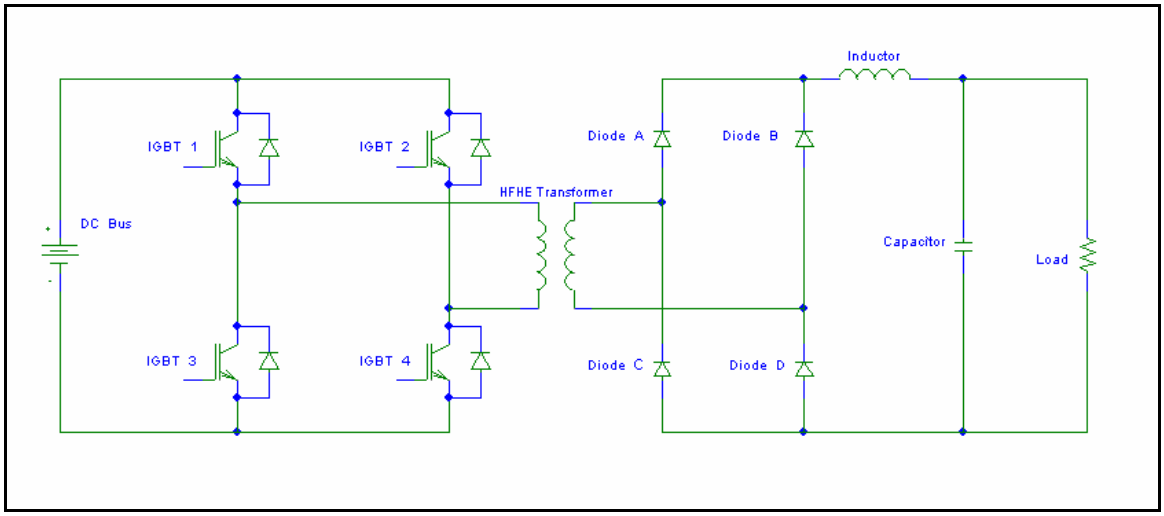

Figure 1. Diagram of the GIFB

The GIFB actually operates very similarly to that of a buck-chopper. The buck chopper equations were therefore utilized in determining the control scheme of the GIFB. A multi-loop control method previously designed for buck choppers at the Naval Postgraduate School (NPS) was utilized to control the output voltage of the GIFB. MATLAB was used to calculate the output response of the controller. Suitable gains were calculated for the controller along with an additional control element for future use.

The input and output voltages for the GIFB were both specified as 300V. The duty cycle of the GIFB was designed for approximately 80%, which is considered a maximum efficiency point for a buck chopper while still maintaining sufficient control 'headroom'. Although a buck-chopper results in a lower output voltage than input voltage, unity gain was achieved in this case due to the primary to secondary turns-ratio (3:4) of the HFHE transformer. Testing was discontinued at an input/output voltage ratio of 240V/240V respectively; the goal of 300V could not be reached with the existing breadboard prototype due to noise disrupting the IGBT gating signals.

This research examines how a GIFB can be used to create a more fault tolerant and reliable DC ship service system. A GIFB can be seen as a replacement for an AC transformer in a DC system. Further research on this concept can be used to turn the GIFB into a true Power Electronics Building Block (PEBB) by making the converter

capable of bi-directional operation. This Galvanically Isolated Building Block (GIBB) would allow a fuel cell, micro-turbine or other power source on the load side to assist in 'dark-ship' startup, power the resident zone or power a longitudinal feeder bus in the event of an interruption of main power. In addition, it may be possible to increase power density through the use of a three-phase GIBB. This may prove to be useful in powering large DC loads found on future electric warships, such as homopolar motors.

I. BACKGROUND AND INTRODUCTION

A. CHAPTER INTRODUCTION

This chapter presents an overview of the Navy's decision to pursue all electric warships utilizing electric drive. Following this, the Zonal Electrical Distribution System (ZEDS) proposed for new warships will be discussed. The ZEDS will need to reliably and efficiently change DC voltage levels while providing galvanic isolation. Finally, it will be detailed how a DC-DC converter that behaves similar to a classic AC transformer meets all of these requirements.

B. AN ALL ELECTRIC NAVY

The United States Navy has committed itself to the development and deployment of electric warships with an Integrated Power System (IPS). In January 2000, the Secretary of the Navy, Richard Danzig, announced that the DD-21 (now changed to DDX) was to be built with an IPS. [1] The Secretary's announcement was reaffirmed by a CNO Executive Board in March 2001 stating, "The Navy is committed to fielding Electric Warships". [2] There is a large effort involved in the transition to electric warships, which are sharply different from those warships currently in service today. Service warships currently utilize segregated propulsion and electric plants. In some cases over ninety percent of the ship's power is dedicated solely to propulsion. Because these warships very seldom travel at top speed, this is a tremendous reserve of thermal power that is not capable of being utilized for electrical purposes. This is an issue with large ramifications, as electrical demands have grown dramatically in the past hundred years and now will include electric weapons and launchers. Figure 2 illustrates this trend with respect to destroyers. The solution that the Navy has decided upon is an electric warship utilizing an IPS.

An IPS differs from a segregated power system in that a common set of prime movers is used to generate all onboard power. This power is applied to the IPS, from which all loads, both propulsion and ship's service, receive their power. The IPS allows the warship commander a much larger degree of flexibility when executing combat roles. It also allows for the installation of weapons and other equipment that can be powered by

the IPS when the ship is not operating at high speed. Examples of this include such weapons as a long range electromagnetic (EM) "Railgun" for the shore bombardment role, and the use of an Electromagnetic Aircraft Launch System (EMALS) for use in launching fixed wing aircraft. Figure 3 shows a comparison between an IPS and a traditional segregated power system.

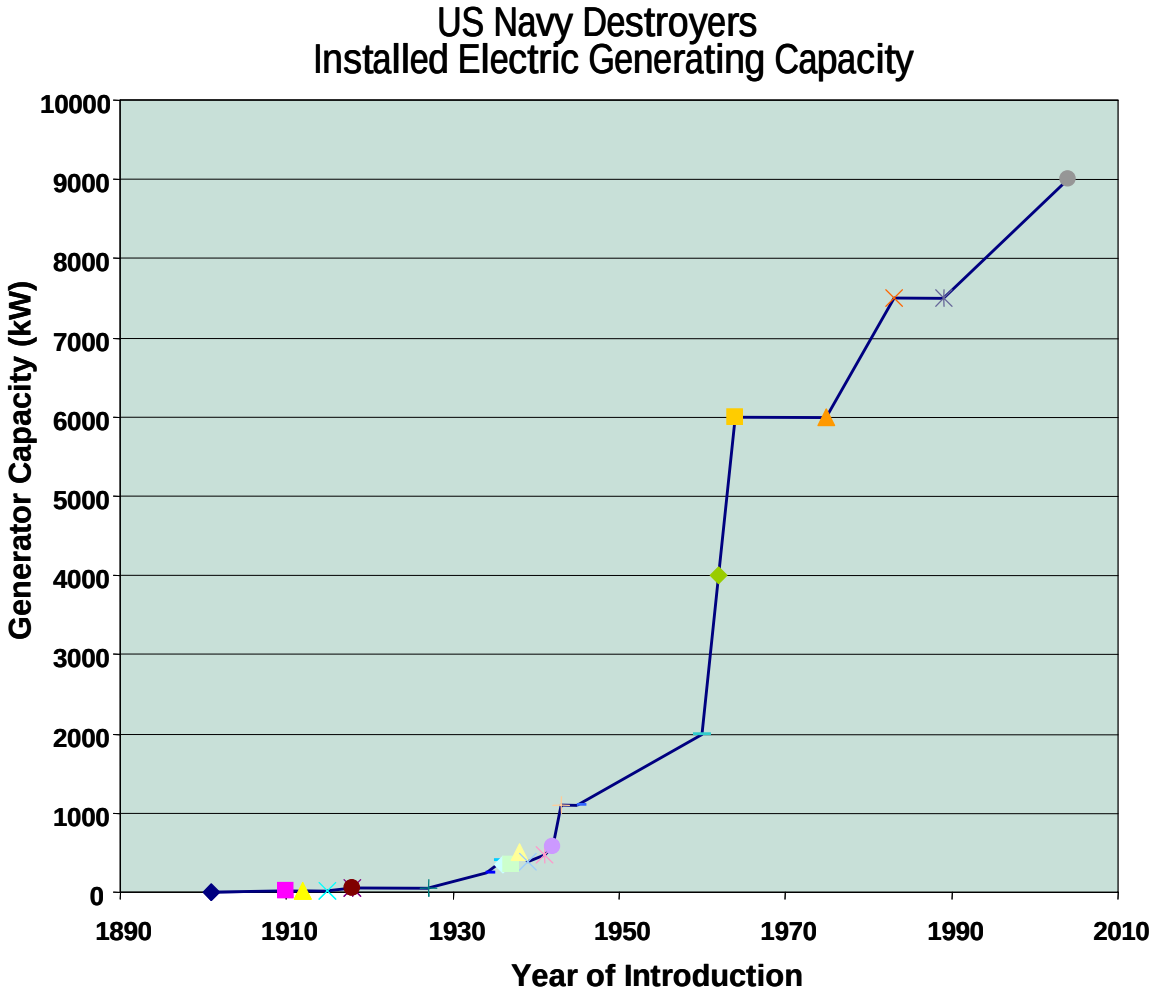

Figure 2. US Navy Destroyers Installed Electrical Generating Capacity (From Ref. 1)

The replacement of the segregated power plant by an IPS is not the only change that the shift to an electric warship will entail. The Electrical Distribution System (EDS) will undergo radical changes as well. The current EDS that is installed on virtually all

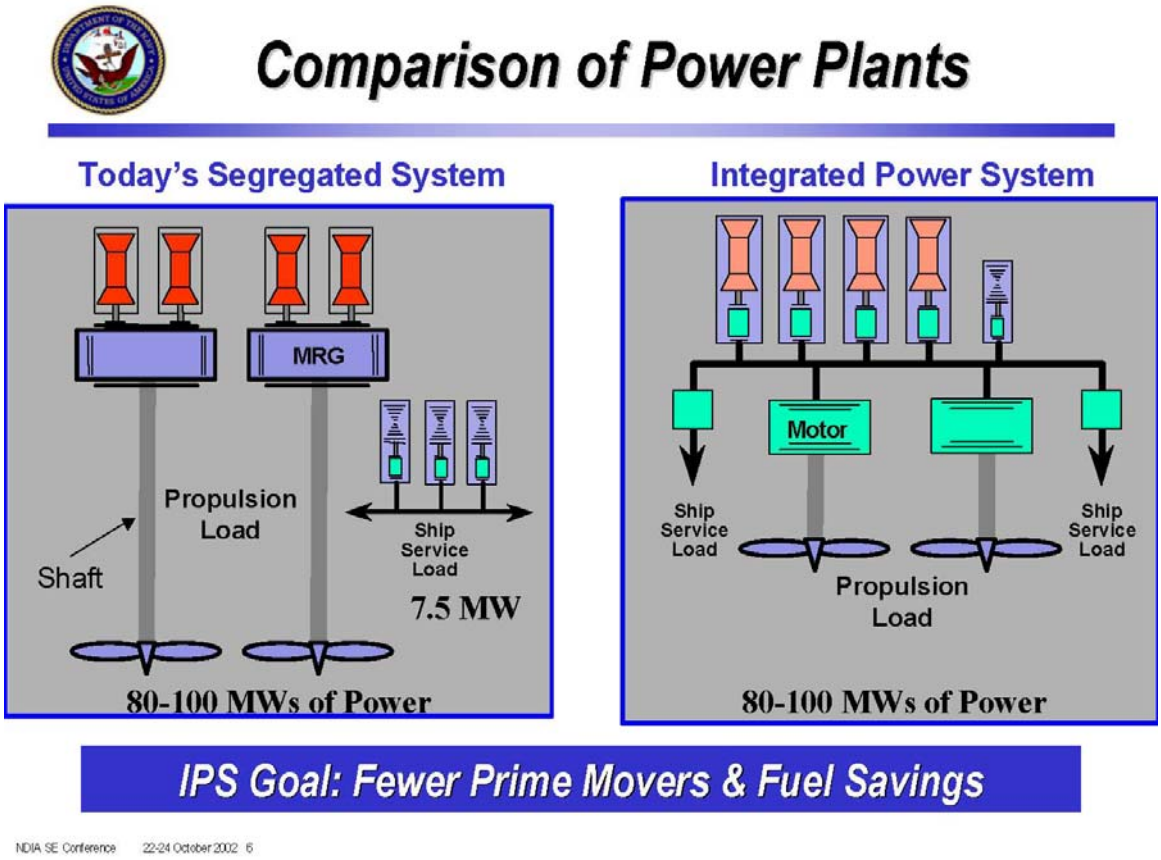

Figure 3. A Comparison of a Segregated Power Plant versus an IPS (From Ref. 3)

warships is termed a radial. The basic concept was developed during the 1940s and remains relatively unchanged today. Ship Service Turbine Generators provide 450V 60Hz AC as the primary power source. This power is applied to distribution switchboards, from which all vital and non-vital electrical loads draw their power. In the example shown in Figure 4, vital loads are connected to backup power sources via Automatic Bus Transfers (ABTs). Backup power sources exist in either the form of Diesel Engines on surface ships, and a diesel generator and batteries on submarines. Additional backup is provided to switchboards in the form of load circuit breakers and fuses which offer protection from any faults on individual loads.

Although the radial EDS offers significant protection and redundancies, it has problems of its own as well. A radial EDS employs a huge amount of cables to connect its loads to the various busses. These cables often penetrate watertight bulkheads. Any penetration through a watertight bulkhead lowers the survivability of the ship. This cable

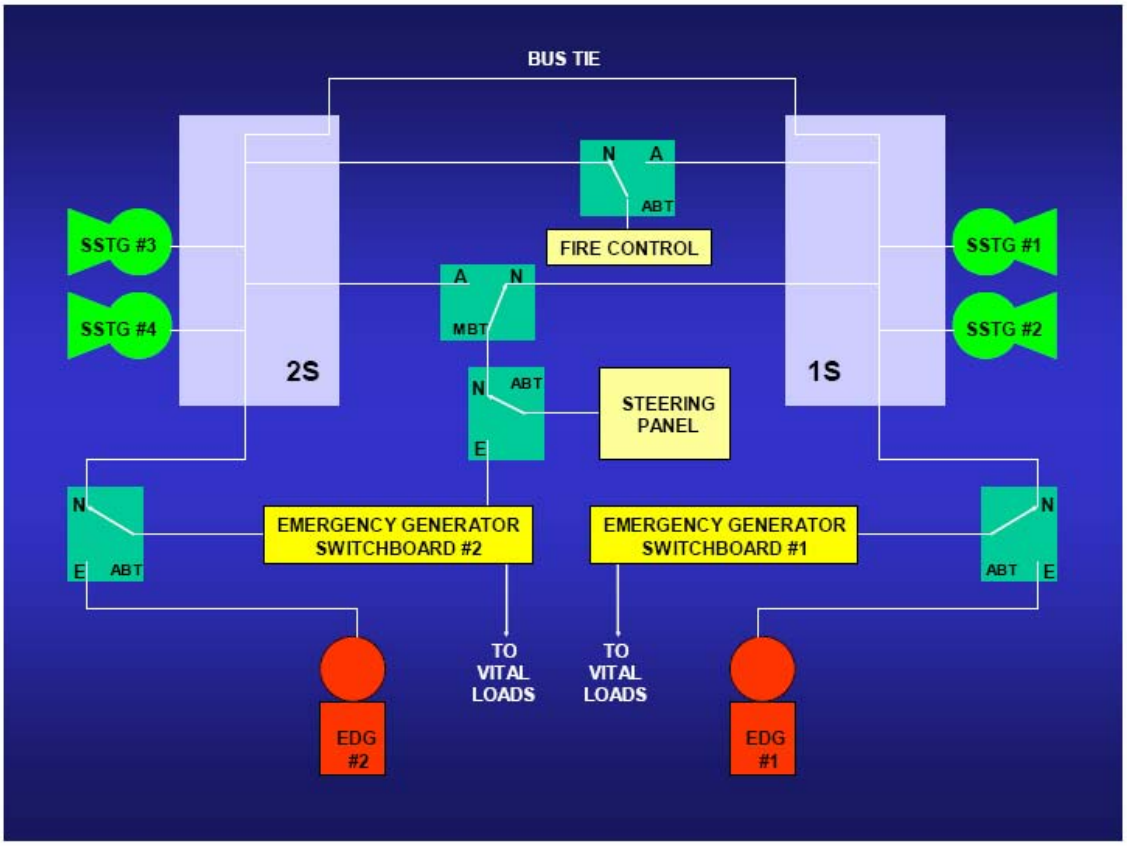

Figure 4. A Simplified Schematic of a Radial EDS (From Ref. 4)

layout also adds complexity to the ship's design, making construction and maintenance more costly and time intensive.

C. THE ZONAL EDS

The wave of the future with respect to the EDS appears to be the DC ZEDS. A DC ZEDS is planned for DDX, a comparison of the Radial and DC ZEDS is shown in Figure 5. All power is generated in the ship by gas turbines. Each main bus has two gas turbines associated with it, providing redundancy. These gas turbines provide 3 phase 13.8kV AC. The ships electric drive will be supplied power by this bus. Any ship's service loads requiring AC will utilize 450V AC that is "stepped down" from the main busses. A rectifier such as a Ship's Service Converter Module will be utilized to rectify 450V AC into 375V DC. If this DC voltage is inappropriate for a DC load, the voltage will have to be stepped up or down by a DC-DC Converter.

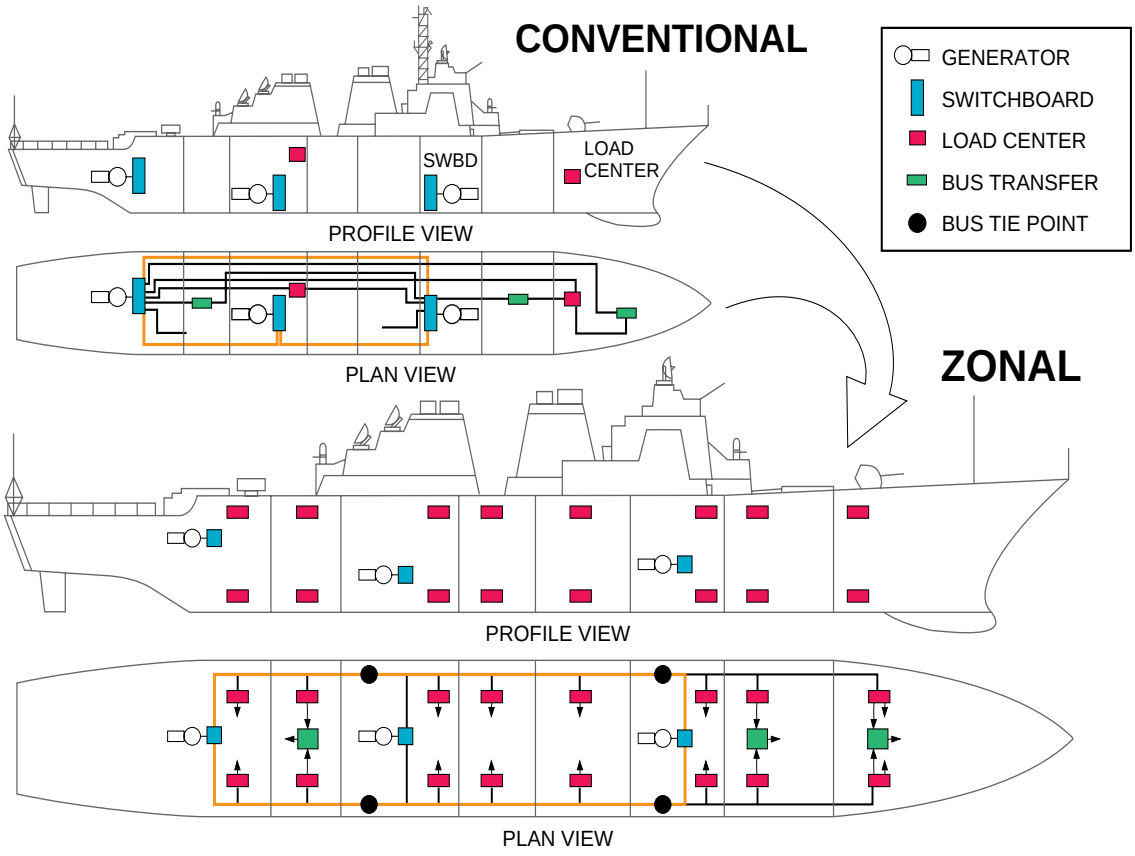

Figure 5. Radial versus DC ZEDS

The ZEDS provides a significant advantage over the radial with respect to layout. In the ZEDS the port and starboard busses run the entire length of the ship, one on each side of the ship. All loads in a compartment receive power from a "zone" of one or both of the buses directly in that compartment. This has the effect of limiting bulkhead penetrations to a minimum. Additionally both the cost and complexity of installation and maintenance is minimized. Circuit breakers and fuses will supply additional protection, just as in the radial.

D. THE NEED FOR GALVANIC ISOLATION

Galvanic isolation refers to a case where there is no direct current path between the load and its source. In a naval EDS, survivability is of the utmost concern. If there is a direct current path between the load and the source, a single ground fault anywhere on the entire zone has the potential to damage the entire zone. If another fault develops *anywhere* on the zone, a current path will exist between the two faults. This has two

main implications. The first is that power to the whole zone may be interrupted due to protective functions. The second is that the current due to the faults may be severe enough to damage components before the protective functions can activate. If galvanic isolation is employed, a single fault on the load side of the isolation and a fault anywhere else in the zone will not cause a current path to be formed. Thus, the zone will remain powered and undamaged. A current path only has the potential to exist if multiple faults occur on the same side of the isolation. It is therefore very advantageous to find a means of providing galvanic isolation for all loads. Figure 6 shows these affects on a DC bus with the green X's indicating faults and the red line indicating the current path available due to the faults.

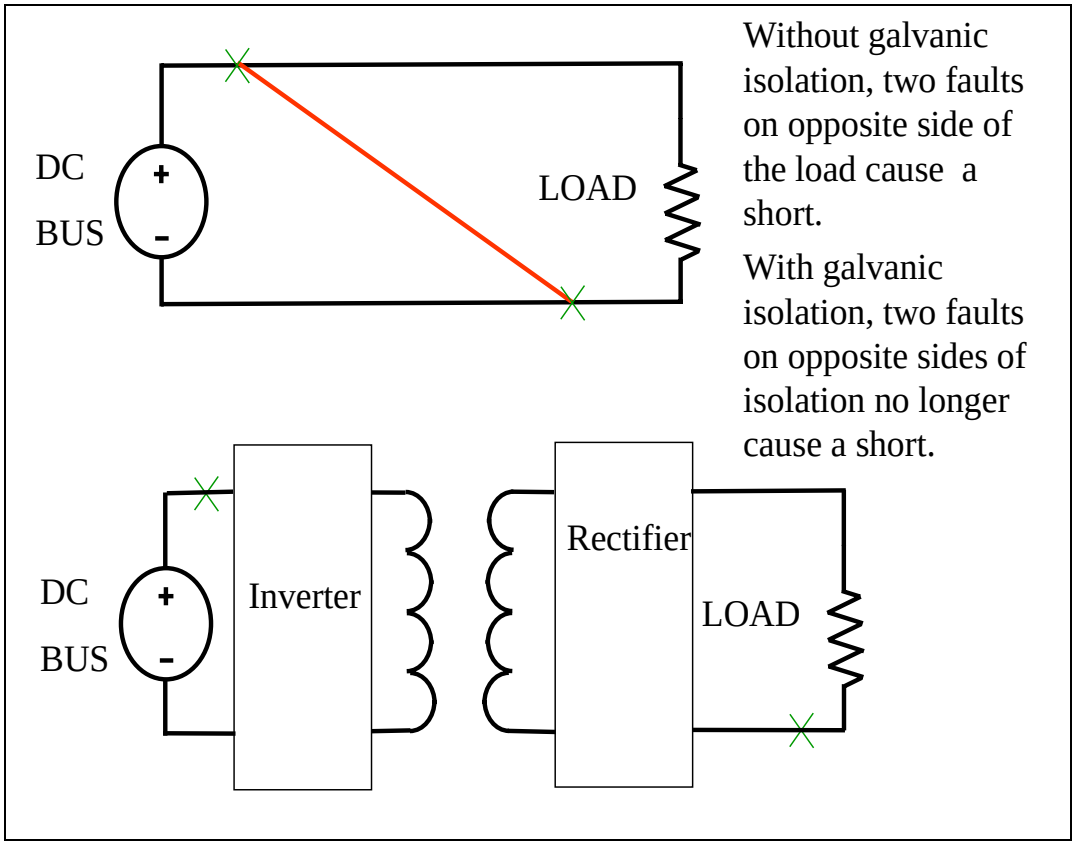

Figure 6. The Effect of Galvanic Isolation on a DC Load with Multiple Faults

In an AC system, galvanic isolation is easily provided by the use of a transformer. Since transformers are inherently an AC component, they are not suitable for use with

DC voltages. Hence, another method must be employed to provide galvanic isolation for DC systems. It would be advantageous to incorporate the galvanic isolation into a converter, which can reliably alter the DC voltage levels as necessary.

E. THESIS STRUCTURE

This thesis examines the construction of a prototype DC-DC converter with galvanic isolation. The converter was built using Commercial-off-the-Shelf (COTS) parts. A transformer is utilized in order to provide the galvanic isolation. In order to be compatible with the transformer, the DC voltage must first be transformed into AC voltage to be passed along the transformer. This AC voltage must be rectified back into DC voltage for use by the load.

The operation of the converter with a description of its major components is detailed in Chapter II. Chapter III derives the State Space Modeling of the converter, and the scheme that is utilized to control it. The controller components are described in detail in Chapter IV. Chapter V will discuss the conclusions reached during the construction of this converter, with recommendations on how it can be improved for bi-directional operation. A three-phase topology will also be discussed, the greater power density of which will be useful for loads such as homopolar motors.

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II. GALVANICALLY ISOLATED CONVERTER DESCRIPTION

A. CHAPTER OVERVIEW

This chapter will discuss the operation of the Galvanically Isolated Full Bridge (GIFB) as a DC-DC converter. The converter has three main stages: a Full Bridge Inverter (FBI), High Frequency High Efficiency (HFHE) transformer, and a single-phase Full-Wave Bridge Rectifier. The FBI and Full-Wave Bridge Rectifier perform the actual power conversion functions, while the transformer provides added reliability in the form of galvanic isolation. Each of these stages will be examined and their operation discussed in detail.

B. OVERALL VIEW

1. Topology

This thesis used a GIFB for its chosen topology. Previous research at NPS in LT Zengle's thesis identified this as a topology suitable for large power operations and was able to recommend a workable control scheme. [4] An example of this topology (with the galvanically isolating HFHE transformer) is shown in Figure 7. The main purpose of this topology is to mimic a classic AC transformer for use by DC systems.

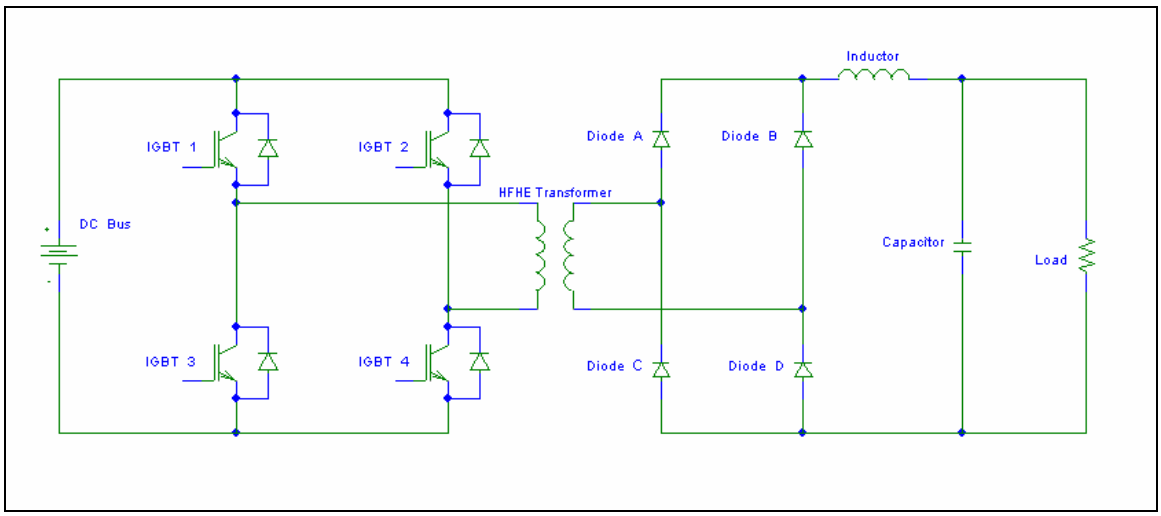

Figure 7. Diagram of the GIFB

This converter used a FBI in order to drop the DC bus voltage into a 3-level AC voltage. A HFHE transformer was utilized to provide galvanic isolation between the load and the DC bus. Due to the high switching frequency of the GIFB (20kHz) a standard 60Hz transformer was deemed insufficient. The 3-level AC voltage from the secondary of the HFHE transformer was then applied to a Full-Wave Bridge Rectifier to produce the appropriate DC voltage for the load. The inverter switching operation was monitored and modified as necessary by a controller, which will be discussed in greater detail in Chapters III and IV.

2. Specifications

The NPS GIFB was designed specifically to provide the Navy with a DC-transformer that mimics its classical AC counterpart. A bus voltage of 300V was selected for the DC supply bus. The GIFB behaves identically to a buck chopper, with the exception of the effect of the HFHE transformer. A duty cycle of 80% has become the standard for the buck chopper. A 75% duty cycle was utilized in this thesis, yielding an output voltage of approximately 300V when the turns ratio of the HFHE transformer was taken into account. The switching frequency of the converter was chosen to be 20kHz. 20kHz has become the Navy standard for switching frequency, due to its being well above the audio spectrum. Finally, an initial load was selected to be 20Ω. The limitations on bus voltage were the result of component selection and available laboratory equipment.

C. FULL BRIDGE INVERTER

1. Purpose

The Full Bridge Inverter is fundamental to the operation of the GIFB. It consists of four power switches, connected in an "H" pattern. Insulated Gate Bipolar Transistors (IGBT) were chosen as the power switch. IGBTs are currently the device of choice for medium power and low voltage applications. The input terminals of the inverter are connected to the DC supply bus, while the output terminals are connected to the HFHE transformer. The Full Bridge is responsible for transforming DC supply voltage into a 3-level AC waveform suitable for the HFHE. The FBI is highlighted in Figure 8.

2. Operation

A DC voltage on the FBI is transformed into a 3–level AC waveform, similar to that shown in Figure 9. A controller monitors both the output voltage and current flowing through the capacitor. The controller then sends output signals which gate the

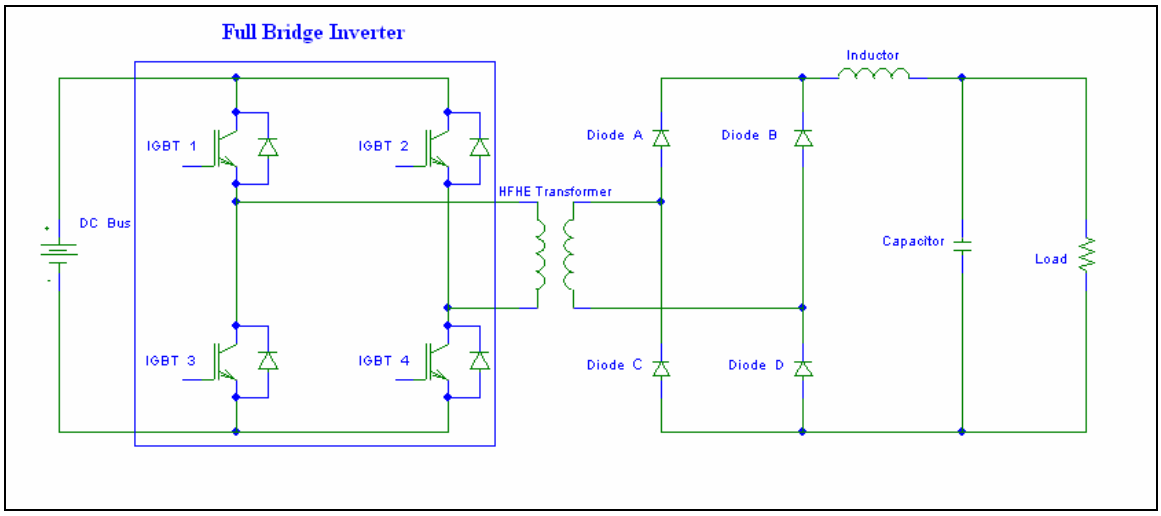

Figure 8. Full Bridge Inverter, Highlighted

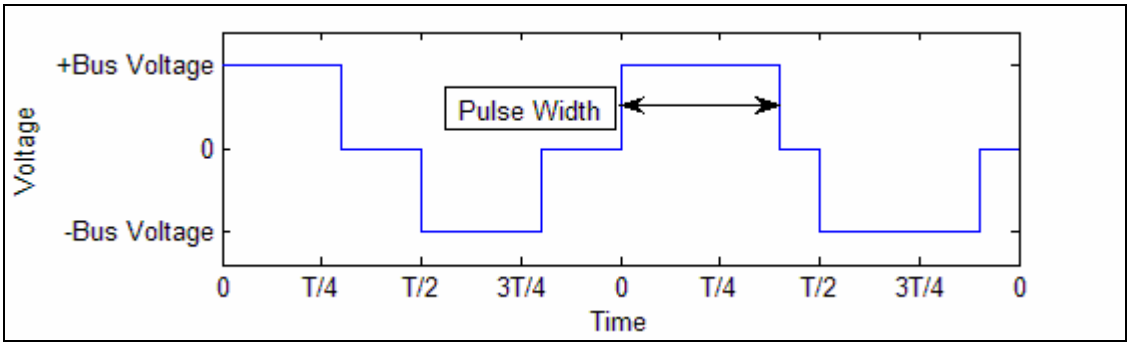

Figure 9. An Example of a 3-Level Voltage with Varying Pulse Widths

IGBTs. When IGBTs 1 and 4 are gated, a positive level of voltage is produced. IGBTs 2 and 3 produce a negative value of voltage. A complete cycle of the system consists of both a positive voltage pulse and a negative voltage pulse, both separated by periods when no IGBT is conducting and hence no voltage is produced. The pulse widths of the

3-level AC voltage are varied in order to change the overall output voltage of the GIFB. Figure 9 shows the 3-level AC voltage waveform with varying pulse widths while Figure 10 shows a block diagram of the controller.

3. Component Selection

Initially, the FBI was constructed utilizing two Toshiba© MG50Q2YS9 dual IGBT packs, configured as half-bridges. A NPS developed optically isolated gate driver card was utilized to make each individual IGBT a floating switch. The controller is completely isolated from the high voltage collectors and emitters of all IGBTS. Once the initial operation of the GIFB was verified, it was decided to procure an integrated COTS component for the FBI.

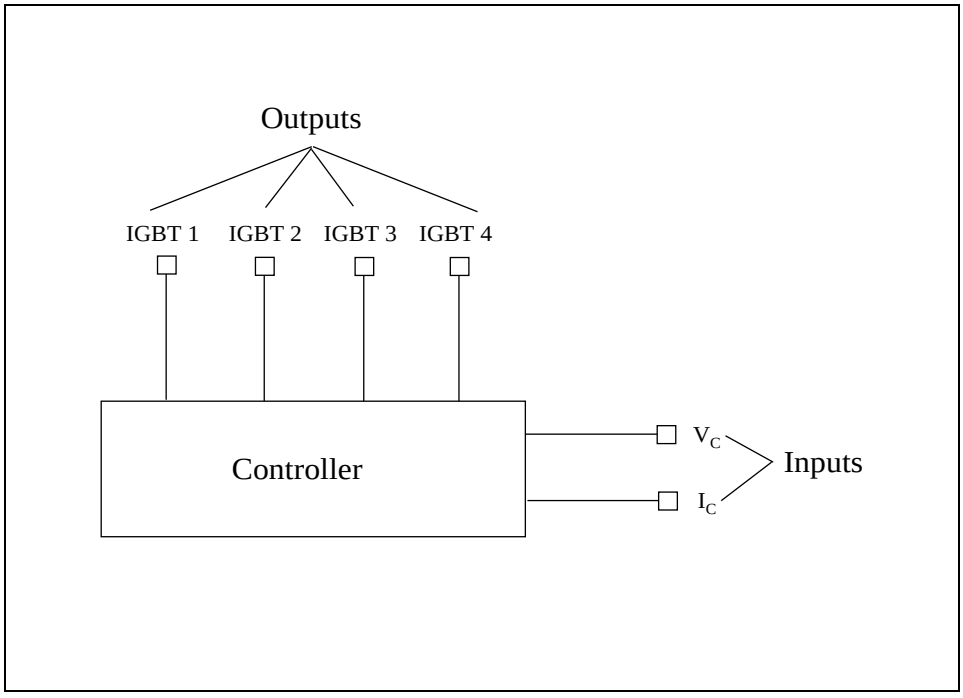

Figure 10. Simplified Controller Input/Output Diagram

The final component selected for the FBI is the PowerEX© POW-R-PAK 150A/1200V 3 phase IGBT Assembly. The complete description of this component is found in Appendix A. The converter is capable of being operated in a variety of configurations, including that of a FBI. It is also capable of being operated as a three-phase inverter, which will be potentially useful in other power electronics thesis applications, and a follow on three-phase GIBB. The POW-R-PAK is a true PEBB that

includes an optically isolated gate driver card. Unfortunately, time did not allow for the installation of the POW-R-PAK, and this thesis was completed with the Toshiba MG50Q2YS9's. A picture of the FBI is shown in Figure 11.

D. HFHE TRANSFORMER

1. Purpose

The HFHE transformer utilized in this design has two main effects. The first, and most important, is to provide galvanic isolation from the source to the load. This is extremely useful in that it protects the ZEDS from any damage caused to the load. The second effect is that the transformer will alter the voltage and current levels supplied from the inverter. The HFHE transformer's position in this design is highlighted in Figure 12.

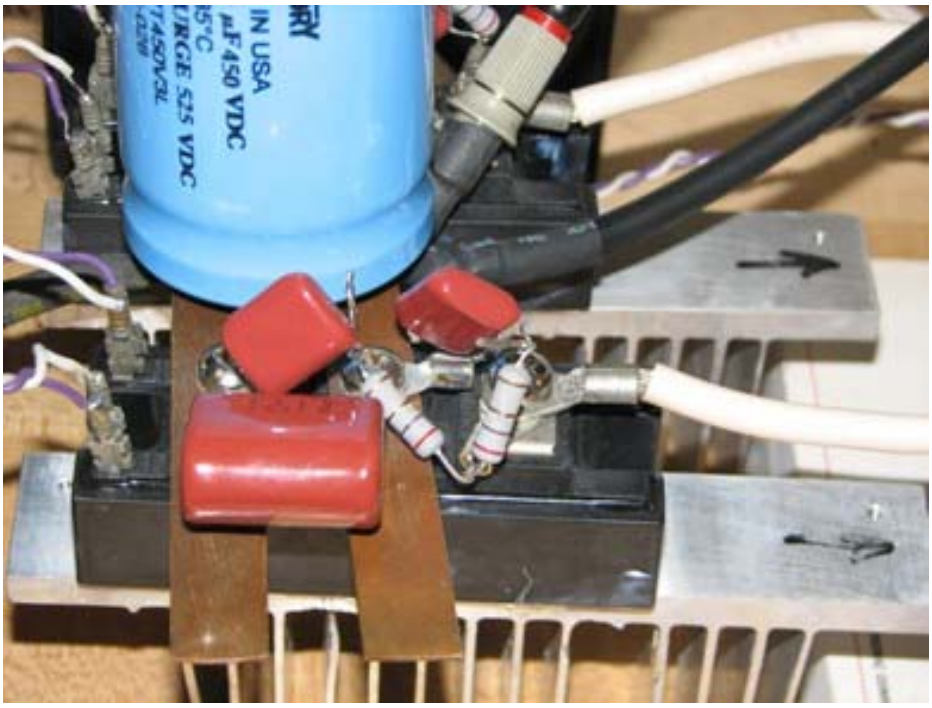

Figure 11. Actual FBI

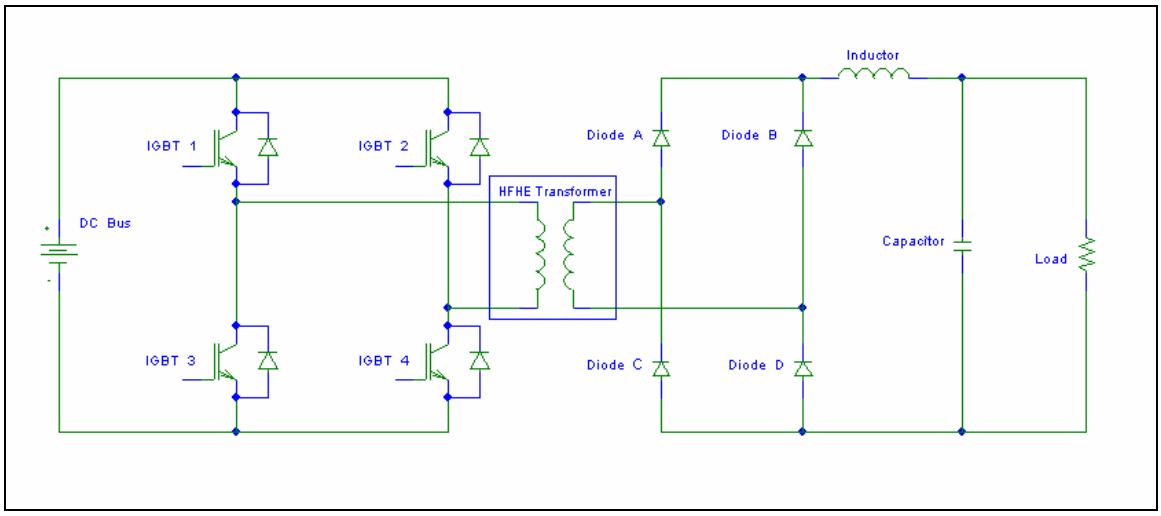

Figure 12. HFHE Transformer, Highlighted

2. HFHE versus Classical Transformer

HFHE transformers share certain characteristics with classical 60Hz transformers. Both types contain a core that magnetically couples two sets of windings (the primary and the secondary) together. Voltage and current levels in both types are altered according to the below formulas where 'a' is the ratio of turns of the primary windings to the secondary windings. In terms of actual construction, however, HFHE transformers are radically different.

$$\text{Voltage}_{\text{primary}} = a \times \text{Voltage}_{\text{secondary}} \tag{2.1}$$

$$\text{Current}_{\text{primary}} = \frac{\text{Current}_{\text{secondary}}}{a} \tag{2.2}$$

The type of HFHE transformer used in this thesis utilizes planar magnetics [5]. Planar magnetics refers to a practice of building magnetic components (transformers and inductors) to mimic a more two-dimensional structure. The two-dimensional structure results in fewer losses at switching frequencies such as those found in the GIFB. Different structural materials will further minimize the losses as well.

a. Core Construction

Major core losses offset by planar magnetics include eddy currents and hysterisis losses. Eddy currents are small currents that are induced in a conductive material (such as the core) due to changing magnetic fields. These currents will produce power loss in the form of heat. In planar magnetics eddy currents are minimized by the selection of a core material with high resistivity, such as a ferrite structure.

Hysteresis refers to the non-reversible effect when the magnetic core is continually magnetized and demagnetized. The core resists changing as fast as the magnetic field and hence some of the magnetic energy is absorbed into the core material as heat. Hysteresis losses per unit volume can be shown to be directly proportional to the magnetic flux swing [5], which is inversely related to the core's cross sectional area. By maximizing the core's cross sectional area while minimizing its volume, planar magnetics significantly lowers hysteresis losses.

b. Windings Construction

Winding losses which are minimized by planar magnetics can be classified under two headings, copper losses and inductance leakage. Copper losses can be further subdivided into two categories, the "skin effect" and the "proximity effect". Both become larger as the switching frequency is increased. The skin effect refers to the action that occurs when the magnetic field generated by a current carrying conductor acts upon itself. The proximity effect is due to the mutual induction between two nearby conductors. Both effects tend to drive current towards the outside of the conductor, which will increase the impedance of the conductor, and hence the losses. Planar magnetics tends to increase the area of the conductor relative to its width, which in turn reduces these losses.

The imperfect coupling between the primary and secondary transformer windings results in leakage inductance losses. These losses can be reduced by minimizing the distance between the two sets of windings. Due to the higher effective cross section made available by planar magnetics, a fewer number of windings is required on both the primary and secondary side. The reduction of windings allows them to be placed closer together and hence lowers the leakage inductance losses.

3. Component Selection

The transformer chosen for this application was the Payton© Size 5000 Transformer by Payton Electronics. Its specifications can be found in Appendix B. The core is constructed out of Ferrite and is E shaped. The windings are made of copper with kapton insulators. This transformer was chosen because of its operating frequency range of 20kHz to 300kHz. The actual HFHE transformer is shown in Figure 13.

E. FULL-WAVE BRIDGE RECTIFIER

1. Operation

A Full-Wave Bridge Rectifier consists of four diodes and converts AC to pulsating DC power. Figure 14 highlights a Full-Wave Bridge Rectifier. When the positive portion of an AC signal is applied to the rectifier, diodes A and D will conduct.

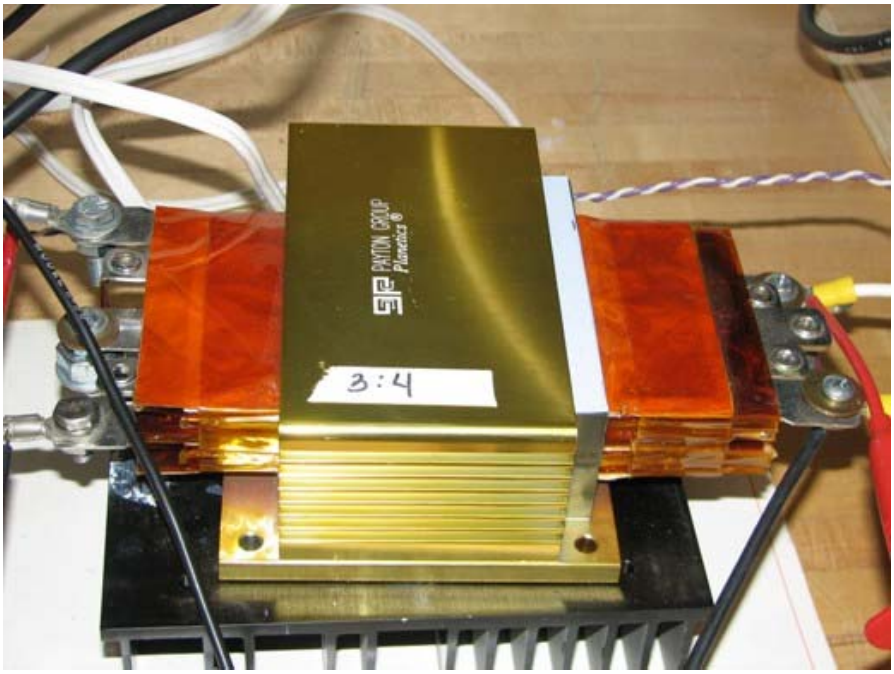

Figure 13. Actual HFHE Transformer

When the negative portion of an AC signal is applied, diodes B and C will conduct. As a result, all current that flows out of the rectifier will be positive. The output waveform is now the absolute value of the input waveform. Figure 15 shows both the input waveform and the output waveform of the Full-Wave Bridge Rectifier.

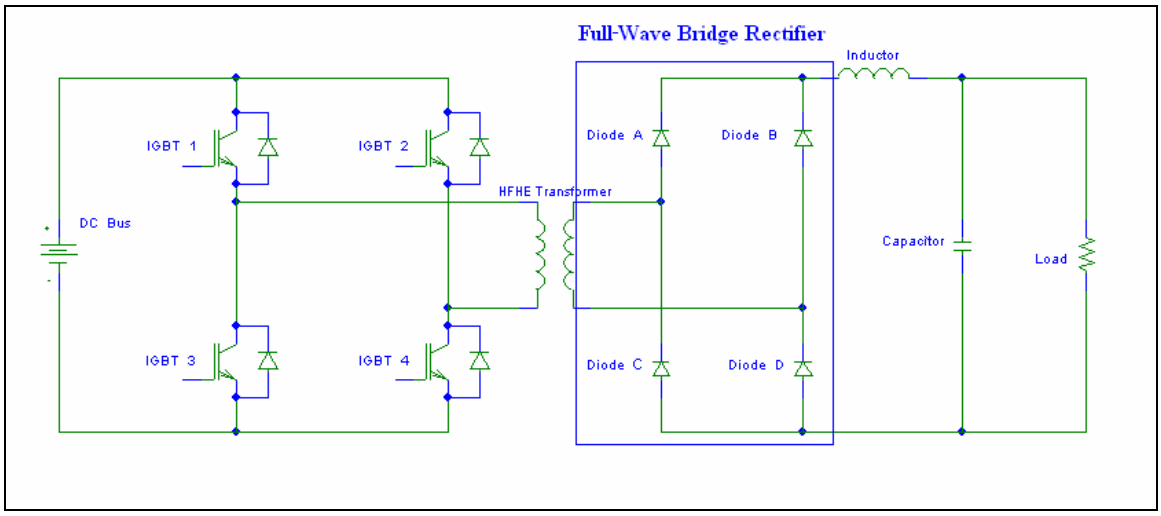

Figure 14. The Full-Wave Bridge Rectifier, Highlighted

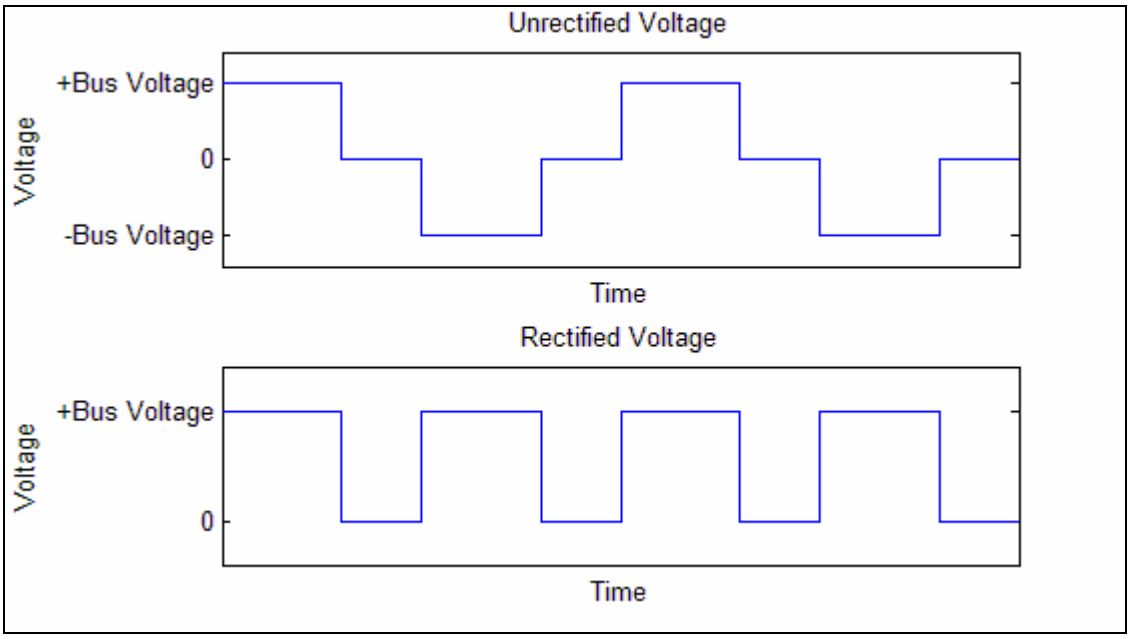

Figure 15. A Comparison of the Unrectified Voltage versus the Rectified Voltage

The output waveform contains a significant amount of ripple that must be filtered out prior to being applied to a load. An inductor-capacitor circuit is used to produce a much smoother waveform. The inductor acts to smooth the current, while the capacitor acts to smooth the voltage.

2. Component Details

Initially the Full-Wave Bridge rectifier was constructed out of four HFA 16PB 120 type diodes. These diodes provided a workable design during the initial phase. However, these diodes experienced significant power losses due to the high switching frequency of 20kHz. A decision was made to acquire an integrated Full-Wave Bridge Rectifier with fast switching diodes which would result in lower losses.

The full bridge rectifier chosen for this application was an ECO-PAK Single-phase Rectifier Bridge with Fast Recovery Epitaxial Diodes, model VBE 55-12NO7, manufactured by IXYS. Specification sheets on this device are included as Appendix C. This device is rated for 1200V @ 59 amps. Most importantly, the diode reverse recovery time is 40ns, which is 1250 times less than the period of the 20kHz switching frequency. A picture of this component is shown in Figure 16.

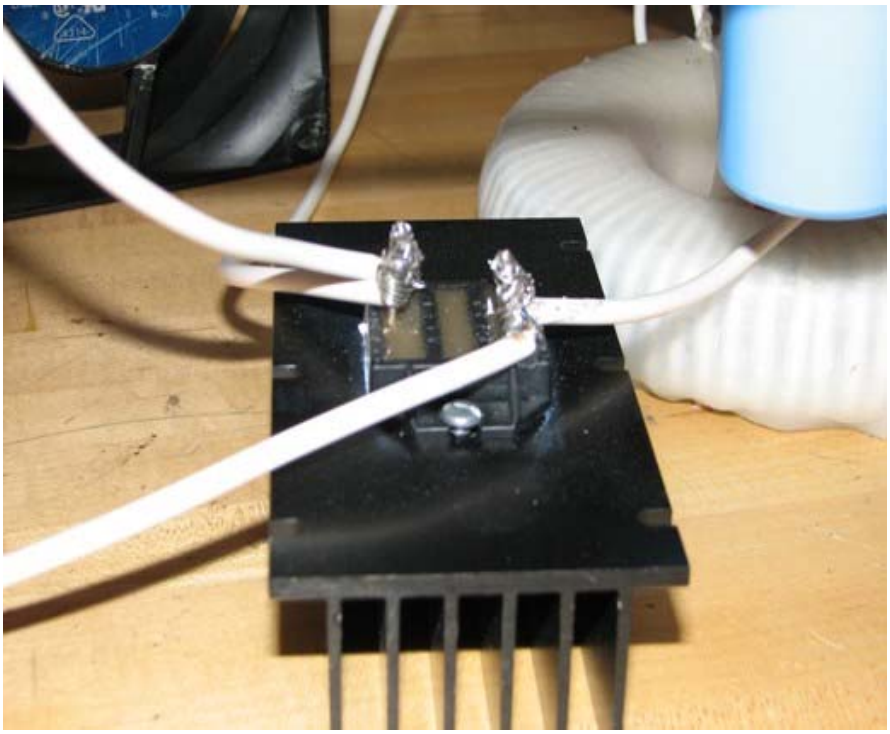

Figure 16. Full-Wave Bridge Rectifier

3. Inductor and Capacitor Sizing

The GIFB is a type of buck chopper, and hence, buck chopper equations apply. Equations governing the response of a buck chopper can found in Reference 6. It is

necessary to modify these equations to account for the turns ratio of the HFHE transformer. These modified equations will be used to determine the size of the filter inductor and capacitor.

One of the key concerns is the amount of the current flowing through the inductor. Specifically, is the inductor large enough to ensure that the inductor current remains continuous, that is, greater than zero? In order for a buck chopper to be controlled properly, it is necessary to maintain continuous inductor current. The Navy generally requires buck choppers to maintain a continuous inductor current down to 10% load. Figure 17 shows an example of continuous current operation versus discontinuous operation.

In the following equations, the variable 'a' refers to the turns ratio of the primary side of the HFHE transformer to the secondary side. The 'E' refers to the input bus voltage, V_c to the output voltage, and D represents the time that the switch is closed. In

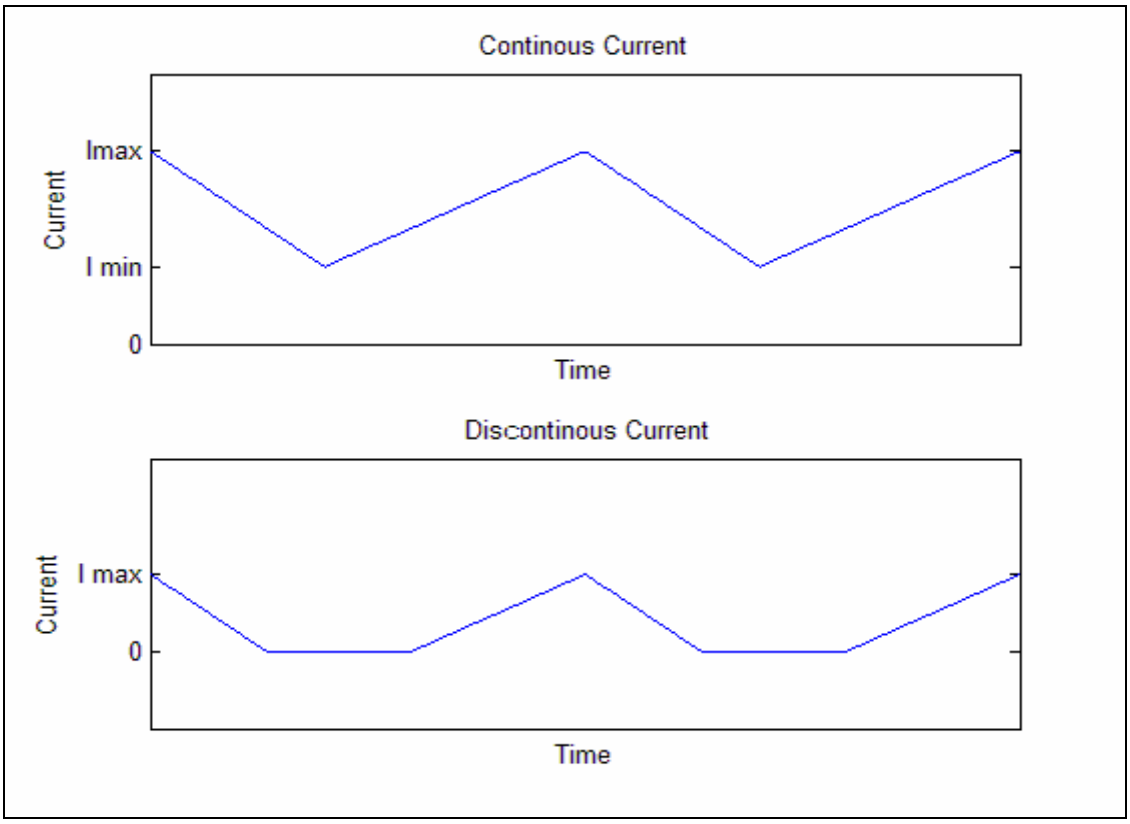

Figure 17. A Comparison of Continuous versus Discontinuous Current

the second equation, L represents the size of the filter inductor, T the period of the overall switching frequency, and R is the size of the load. Lcrit refers to the inductance necessary to maintain continuous current operation.

$$\boxed{V_c = aDE} \tag{2.3}$$

$$\boxed{L_{crit} = \left(\frac{TR}{2}\right)(1-D)} \tag{2.4}$$

Substituting equation 2.1 into 2.2 yields:

$$\boxed{L_{crit} = \left(\frac{TR}{2}\right)\left(1-\frac{V_c}{Ea}\right)} \tag{2.5}$$

When the appropriate values are inserted into equation 2.3, the resulting critical inductance is 1.25mH. For the actual GFBB, an inductor of size 2.14mH was selected, easily guaranteeing enough inductance to sustain continuous current operation.

The key factor in determining the size of the capacitor is the amount of ripple voltage desired. Specifically, it is preferable to minimize ripple voltage. A larger capacitor leads to smaller ripple voltage. It was decided for this thesis that the ripple voltage, defined as $\Delta V_C / V_C$, be less than one percent. Equation 3.4 represents the peak-to-peak ripple voltage for continuous operation. The variable f refers to the switching frequency, C is the size of the capacitor.

$$\boxed{\frac{\Delta V_c}{V_c} = \frac{(1-D)}{f^2}\left(\frac{1}{8LC}\right)} \tag{2.6}$$

Solving for the capacitor size yields the equation:

$$\boxed{C = \frac{V_c}{\Delta V_c}\frac{(1-D)}{f^2}\left(\frac{1}{8L}\right)} \tag{2.7}$$

This yields a capacitor value of 3.7uF. The actual capacitor chosen for this thesis was 144uF. When substituted into equation 2.7 this value yields a peak-to-peak ripple voltage of 0.025 %.

III. STATE SPACE MODELING AND CONTROL

A. CHAPTER OVERVIEW

The purpose of this chapter is threefold. First, a model of the converter will be derived using State-Space-Averaging (SSA). Following this, a multi-loop controller scheme will be described in detail. Finally, the advantage of adding a fourth gain in a future controller will be described.

B. STATE-SPACE MODELING

1. Background and Initial Conditions

SSA is a mathematical tool for constructing a linear model of a power converter. It is based on determining the circuit equations of the power converter for each switch configuration (hereafter referred to as mode of operation.) Once these equations have been obtained, they are "weighted", that is, they are multiplied by the fraction of time that the converter operates in that cycle. In the case of the GIFB, the variable 'd' will refer to the time when IGBTs are conducting (modes 1 and 3); while the term '1-d' refers to the time the IGBTs are not conducting (modes 2 and 4).

Two main initial conditions were assumed in this analysis. First, all components were modeled as ideal components with no losses. Second, SSA requires that the GIFB be operating in a continuous mode. Continuous in this case refers to the fact that the inductor current always remains greater than zero and flowing in the direction shown in Figure 14.

2. Mode 1 Operation

The first mode of operation involves the converter powering the load from the DC supply bus. Current flows from the DC supply bus, through IGBT 1, into the dotted side of the primary coil of the transformer, through IGBT4, and back to the DC supply bus. Even if we assume that the transformer is ideal, the turns ratio will introduce voltage or current magnification if it is not unity. The current in the primary winding of the transformer magnetizes the core, and induces current in the secondary winding. Current flows out of the dotted side of the secondary coil, through diode A and across the inductor, into the load and finally back to the transformer through diode D. Initially, the

capacitor is also supplying current to the load as well. (Figure 18, between points A and B.) As the inductor current continues to build up, it will eventually begin to charge the capacitor. (Figure 18, between points B and C.) Figure 19 depicts the current flow in the GIFB. Neglecting voltage drops across the IGBTs and the diodes yields the resulting equivalent circuit shown in Figure 20. Note that voltage source in the equivalent circuit must be scaled by the variable 'a', to account for the primary to secondary turns ratio.

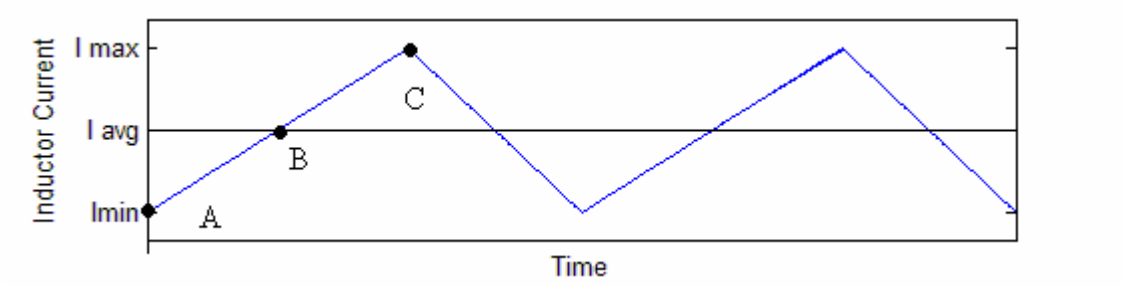

Figure 18. Mode 1 Inductor Current

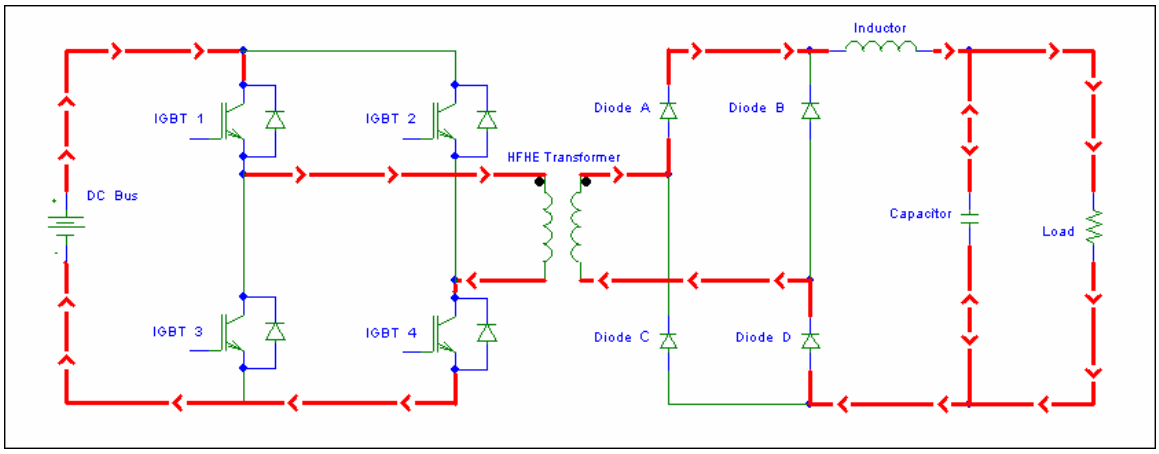

Figure 19. Mode 1 Operation of the FBC

The following equations describe the operation of the converter during mode 1. The lowercase terms include both the steady state and small signal components and are thus time varying, (i.e. e=e(t).) The capital letter refers to the steady state value, while the lowercase letter with hat refers to the small signal component.

$$\boxed{\frac{e}{a} = v_L + v_C} \tag{3.1}$$

$$\boxed{i_L = i_C + i_R} \tag{3.2}$$

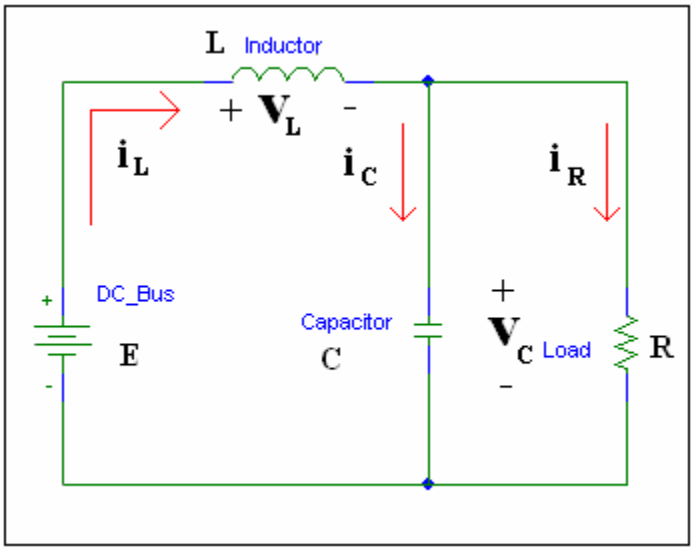

Figure 20. Simplified Circuit of Mode 1 Operation

$$\boxed{i_R = \frac{v_C}{R}} \tag{3.3}$$

$$\boxed{i_C = C\frac{dv_C}{dt}} \tag{3.4}$$

$$\boxed{v_L = L\frac{di_L}{dt}} \tag{3.5}$$

Substituting equations 3.3 and 3.4 into 3.2 and rearranging yields:

$$\boxed{\frac{dv_C}{dt} = \frac{1}{C}\left[i_L - \frac{v_C}{R}\right]} \tag{3.6}$$

Substituting equation 3.5 into 3.1 and rearranging yields:

$$\boxed{\frac{di_L}{dt} = \frac{1}{L}\left[\frac{e}{a} - v_C\right]} \tag{3.7}$$

Equations 3.6 and 3.7 are the defining state equations for mode 1.

3. Mode 2 Operation

Mode 2 involves the converter powering the load from the energy stored in the capacitor and the inductor with all IGBTs off. At first the inductor current is sufficient to supply current to both the capacitor and the load. (Figure 21, time between points C and D) However, as the inductor current decays, a point exists at which both the inductor and capacitor are utilized to supply energy to the load (Figure 21 time between points D and E). Due to the back electromotive force produced by the IGBT's anti-parallel diodes, no current may flow through the transformer. Rather current is split among both diode paths. Figure 22 shows the actual current flow paths while Figure 23 shows the simplified circuit.

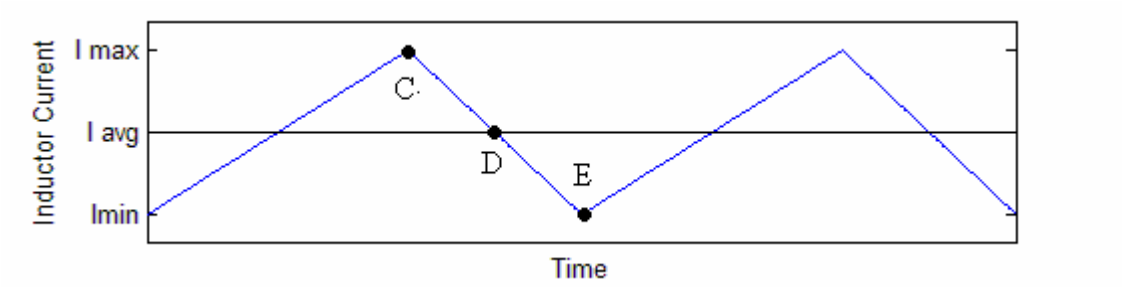

Figure 21. Mode 2 Inductor Current

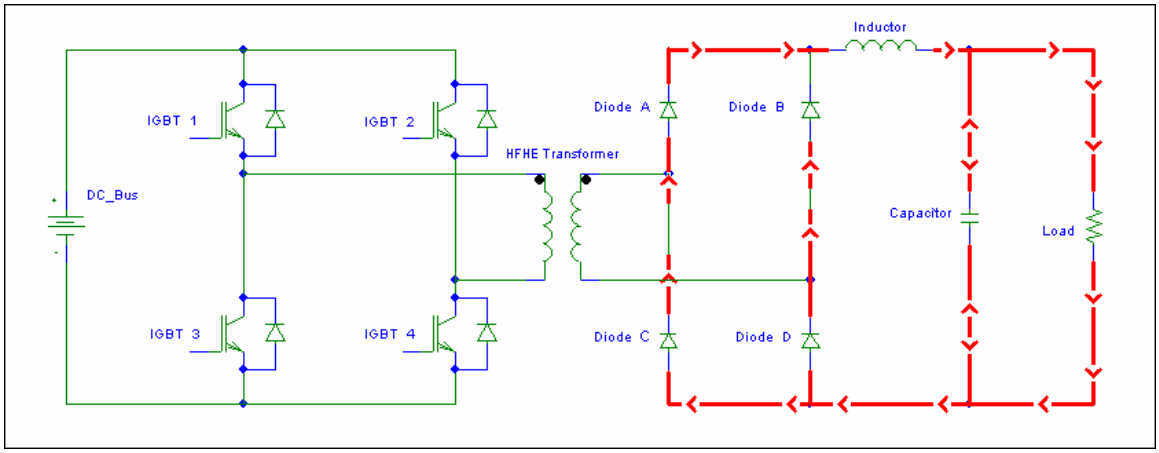

Figure 22. Mode 2 Operation of the FBC

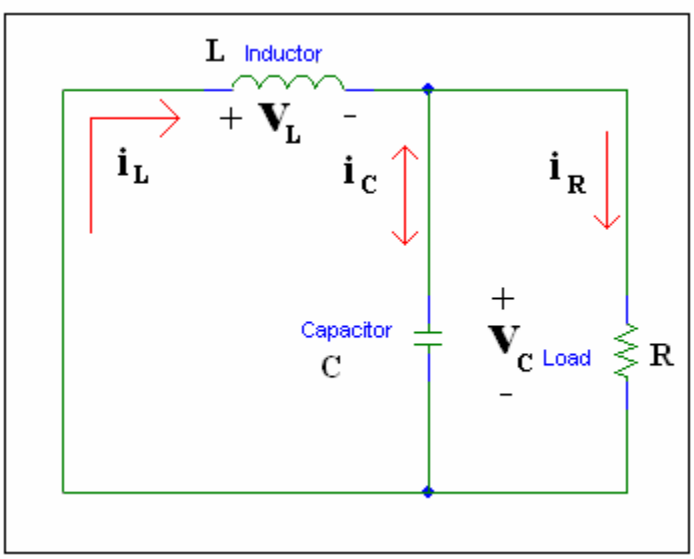

Figure 23. Simplified Circuit of Mode 2

The following equations describe the operation of the converter during mode 2.

$$\boxed{i_L = i_C + i_R} \tag{3.8}$$

$$\boxed{0 = v_L + v_C} \tag{3.9}$$

$$\boxed{i_R = \frac{v_C}{R}} \tag{3.10}$$

$$\boxed{i_C = C\frac{dv_C}{dt}} \tag{3.11}$$

$$\boxed{v_L = L\frac{di_L}{dt}} \tag{3.12}$$

Substituting equations 3.10 and 3.11 into 3.08 and rearranging yields:

$$\boxed{\frac{dv_C}{dt} = \frac{1}{C}\left[i_L - \frac{v_C}{R}\right]} \tag{3.13}$$

Substituting equation 3.12 into 3.9 and rearranging yields:

$$\boxed{\frac{di_L}{dt} = \frac{1}{L}\left[-v_C\right]} \tag{3.14}$$

Equations 3.13 and 3.14 are the defining state equations for mode 2.

4. Mode 3 and Mode 4 Operation

Mode 3 works very similar to Mode 1 in that the load is being powered from the DC bus. The only difference is that current flow is through IGBTs 2 and 3 on the converter side and through diodes B and D on the load side. The equations are identical to those of mode 1. Mode 4 operation and equations are identical to those of mode 2.

5. Weighting and Combining the Equations

The time has now come to weigh and combine the equations. The symbol d will denote the time that the one of the IGBT switching pairs (either 1 and 4 or 2 and 3) are closed.

If we weight equations 3.6 and 3.13 together and also weight 3.7 and 3.14 together this yields:

$$\boxed{\frac{dv_C}{dt} = \frac{1}{C}\left[i_L - \frac{v_C}{R}\right]} \tag{3.15}$$

and

$$\boxed{\frac{di_L}{dt} = \frac{1}{L}\left[\frac{de}{a} - v_C\right]} \tag{3.16}$$

The astute power engineer with recognize equations 3.15 and 3.16 as buck chopper equations modified with a transformer turns ratio.

6. Adding Small Signal Elements

The time has come to separate the small signal components from the average portion of each equation. The capital letter stands for the DC or steady state portion of the signal, while the lowercase letter with the ^ represents the small signal, or “ripple” portion of the signal. The following signals are thus defined.

$$\boxed{d = D + \hat{d}} \tag{3.17}$$

$$\boxed{e = E + \hat{e}} \tag{3.18}$$

$$\boxed{i_L = I_L + \hat{i}_L} \tag{3.19}$$

$$\boxed{v_C = V_C + \hat{v}_C} \tag{3.20}$$

$$\boxed{\frac{di_L}{dt} = \frac{d\hat{i}_L}{dt}} \tag{3.21}$$

$$\boxed{\frac{dv_C}{dt} = \frac{d\hat{v}_C}{dt}} \tag{3.22}$$

Now that the small signal terms are introduced, two new state equations will be derived. Any multiplication of two small signal terms was considered negligible and hence discarded. In addition, a smooth DC bus was assumed and therefore the small signal portion of the DC bus (the variable ‘ $\hat{e}$ ’) was dropped as well.

$$\boxed{\frac{d\hat{v}_C}{dt} = \frac{1}{C}\left[I_L + \hat{i}_L - \frac{V_C}{R} - \frac{\hat{v}_C}{R} \right]} \tag{3.23}$$

$$\boxed{\frac{d\hat{i}_L}{dt} = \frac{1}{L}\left[\frac{\hat{d}E}{a} + \frac{DE}{a} - \hat{v}_C - V_C \right]} \tag{3.24}$$

Using the concept of superposition equations 3.23 and 3.24 can be broken down into DC equations and ripple equations. The DC equations are the following:

$$\boxed{I_L = \frac{V_C}{R}} \tag{3.25}$$

$$\boxed{V_C = \frac{DE}{a}} \tag{3.26}$$

The ripple equations are the following:

$$\boxed{\frac{d\hat{v}_C}{dt} = \frac{1}{C}\left[\hat{i}_L - \frac{\hat{v}_C}{R}\right]} \tag{3.27}$$

$$\boxed{\frac{d\hat{i}_L}{dt} = \frac{1}{L}\left[\frac{\hat{d}E}{a} - \hat{v}_C\right]} \tag{3.28}$$

Substituting equation 3.28 into 3.27 yields the second order differential equation:

$$\boxed{CL\frac{d^2 v_C}{dt} + \frac{Ldv_C}{Rdt} + \hat{v}_C = \frac{\hat{d}E}{a}} \tag{3.29}$$

Taking the Laplace transform of equation 3.29 yields:

$$\boxed{\frac{v_c}{\hat{d}} = \frac{E}{LCa\left(s^2 + s\frac{1}{CR} + \frac{1}{LC}\right)}} \tag{3.30}$$

Equation 3.30 is the open loop transfer function of the system. In the open loop system, the output voltage is controlled by the duty cycle as expected. By setting s equal to a frequency of zero, equation 3.30 reduces to:

$$\boxed{\hat{v}_c = \frac{\hat{d}E}{a}} \tag{3.31}$$

This is similar to a buck chopper equation, modified by the transformer turns ratio.

C. CLOSED LOOP DESIGN

1. Closed Loop Theory

The time has come to add a controller and to create a closed loop system. The controller will be of a multi-loop type, utilizing a proportional and integrative gain on the output voltage, and a proportional gain on the capacitor current. Previous research at NPS has concluded that this is the best type of controller for converters such as buck choppers. [4] Figure 24 shows an example of this type of controller. [7]

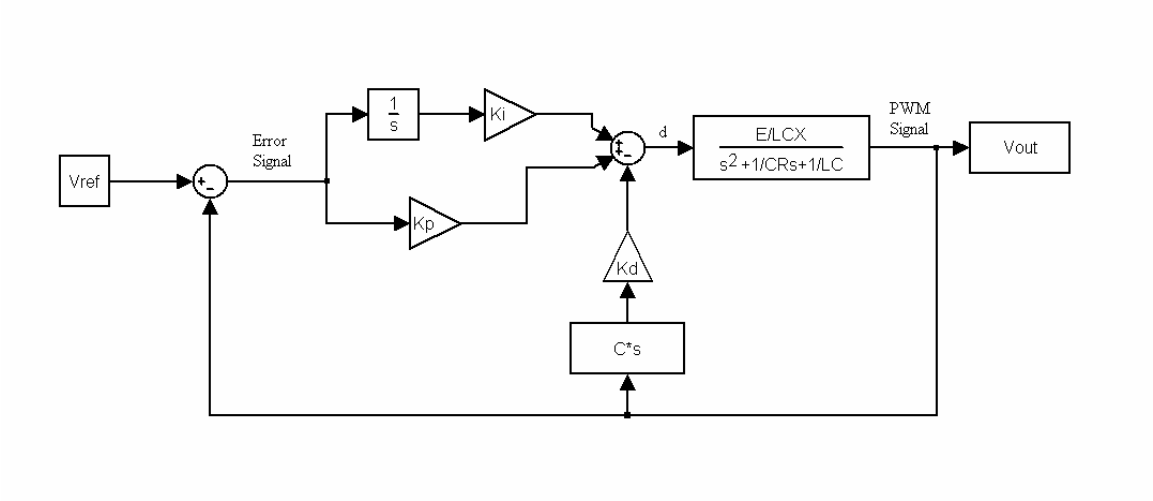

Figure 24. A Modified Multi-Loop Controller

The controller is controlling three different elements. In order to control the output voltage level, a reference level is established. The difference between the output level and this reference level is referred too as the error signal, and is multiplied by the proportional gain, k_p. This error is what the controller actually uses to set the proper duty cycle of the IGBTs so as to properly change the output voltage level. The error signal is also integrated and multiplied by the integrative gain k_i. The integrative gain serves to eliminate the inherent steady state error present by using proportional gain alone.

The last gain to be addressed is the proportional capacitive current gain. Here a derivative element of the output voltage is obtained by the sampling of the capacitor current. This derivative gain k_d gain serves to give the system speed in achieving its desired output. The resulting equation to describe the interaction of these gains is as follows:

$$\boxed{d(t) = k_p(v_{ref} - v_C) + k_i\left(\int (v_{ref} - v_C)\right) + k_d(-\frac{dv_C}{dt})} \qquad (3.32)$$

There remain two practical controller implementation issues that have yet to been discussed. These issues involve the scaling output voltage V_c, and the scaling of the capacitor current, i_c. The output voltage V_c is specified at 300V. The actual control circuit, described in more intimate detail in section 4, has a dynamic input range of ±15V.

A circuit to step down the output voltage is required. For our purposes, we will consider this voltage scaling factor to be called k_{vout}. This scaling factor must be applied to the proportional and integrative gains portion of the controller. The derivative function of the capacitor current also has a similar scaling factor applied to it as well. This factor will be called k_{ic}. Equation 3.31 is thus modified into:

$$\boxed{d(t) = k_p k_{vout}(v_{ref} - v_C) + k_i k_{vout}\left(\int (v_{ref} - v_C)\right) + k_d k_{ic}(-\frac{dv_C}{dt})} \tag{3.33}$$

The closed loop transfer function becomes:

$$\boxed{\frac{v_C}{v_{ref}} = \frac{\frac{E}{aCL} k_{vout}\left[sk_p + k_i\right]}{s^3 + s^2\left[\frac{Ek_d k_{ic}}{aL} + \frac{1}{CR}\right] + s\left[\frac{Ek_p k_{vout}}{aCL} + \frac{1}{LC}\right] + \frac{Ek_i k_{vout}}{aCL}}} \tag{3.34}$$

2. Closed Loop Implementation

The closed loop transfer function shown in equation 3.34 contains one zero and three poles. With a transfer function of this type, it is normally preferred to have a closed loop pole-zero location similar to that shown in Figure 25.

The closed loop transfer function represented by the closed loop root locus above is dominated by a pair of complex poles located at a 45 degree angle to the origin. The zero and remaining pole are far to the left of the complex poles, having little result on the systems performance. The resulting response to a step input for a function of this type is shown in Figure 26.

Unfortunately, with the components specified in the GIFB closed loop transfer function it was impossible to achieve the pole/zero condition of Figure 25. The single pole and single zero were always to the right of the complex poles. It was therefore necessary to undertake a different approach. The gains could be manipulated so that a pole cancelled out the zero and both remaining poles were real, not complex. If enough space existed between the two remaining poles, one pole would dominate the response. This approach was used in the design of the GIFB controller.

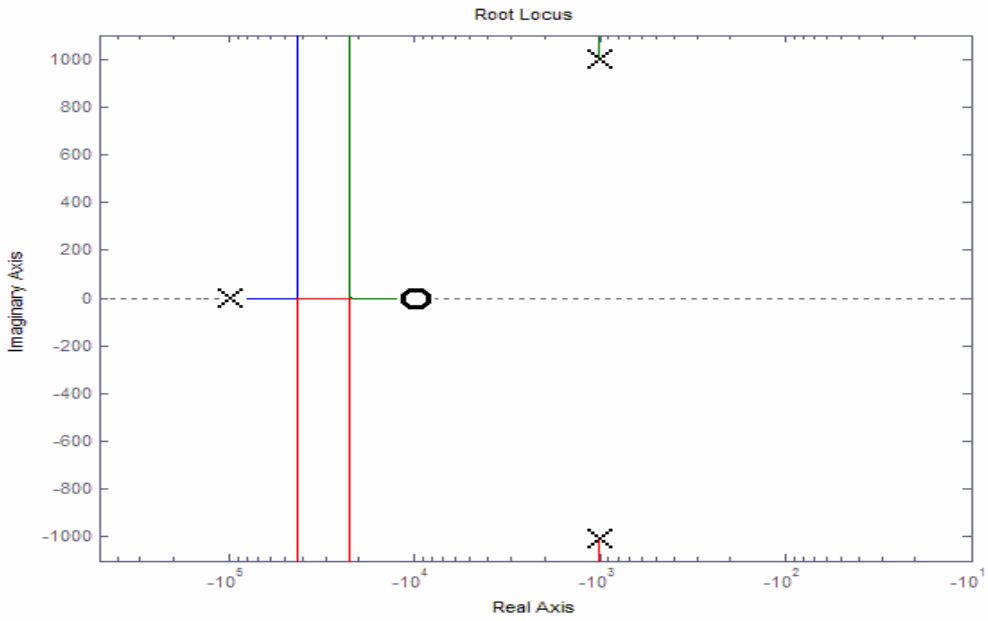

Figure 25. Preferred Closed Loop Pole/Zero Location

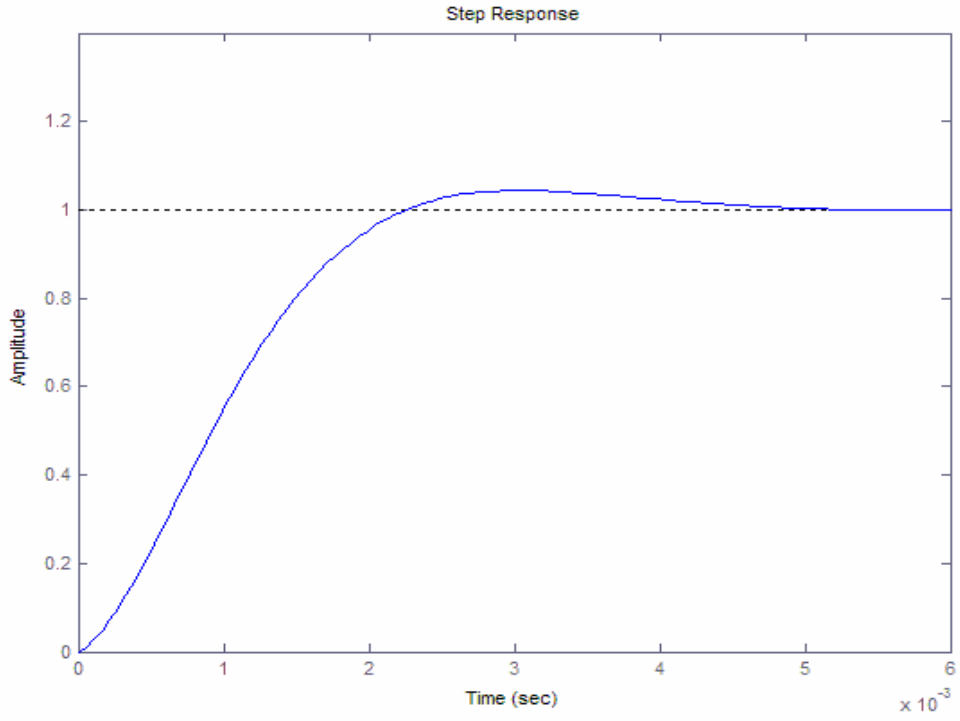

Figure 26. Ideal Step Response

The Matlab© code used to calculate the gains is contained in appendix A. Gains of k_i=2241.8, k_p=64.7, k_d=15, k_{vout}=.033, and k_{ic}=0.075 yielded a step response of approximately 0.4 ms, shown in Figure 27. Figure 28 contains the pole zero locations. This response was deemed suitable for the GIFB. This step response was only possible over a very narrow range of gains, however. This was primarily due to two reasons. First, in order to reduce the amount of noise present, it was decided to only utilize gain resistors with values between 5.1kΩ and 330kΩ and to use only single stages in determining these gains. This limited the upper bound of k_p to a value of 64.7, which drove the value of k_i to be approximately 2200 to remove steady state error. Second, the system was quite variable with respect to bus voltage and the gain k_d=15. A value k_d=7.5 provided a stable response at a bus voltage of 300V but produced a response with 30% overshoot at a bus voltage of 30V.

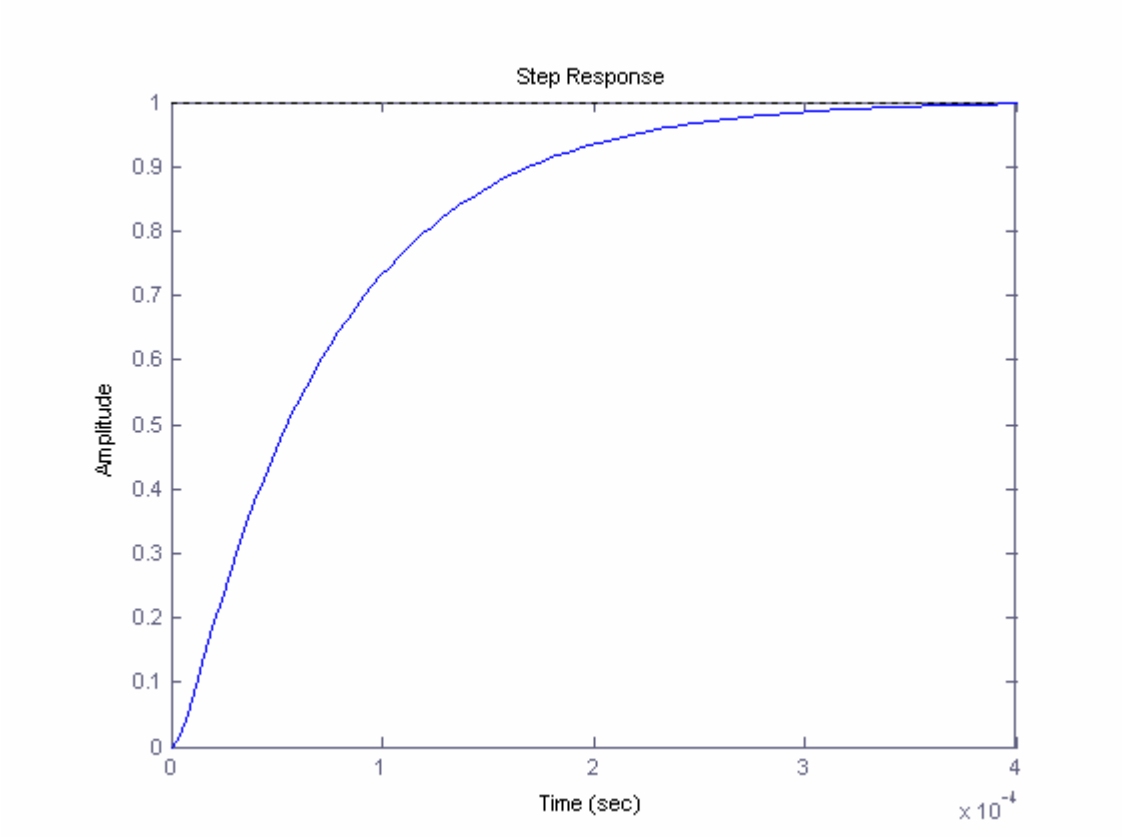

Figure 27. Final GIFB Step Response

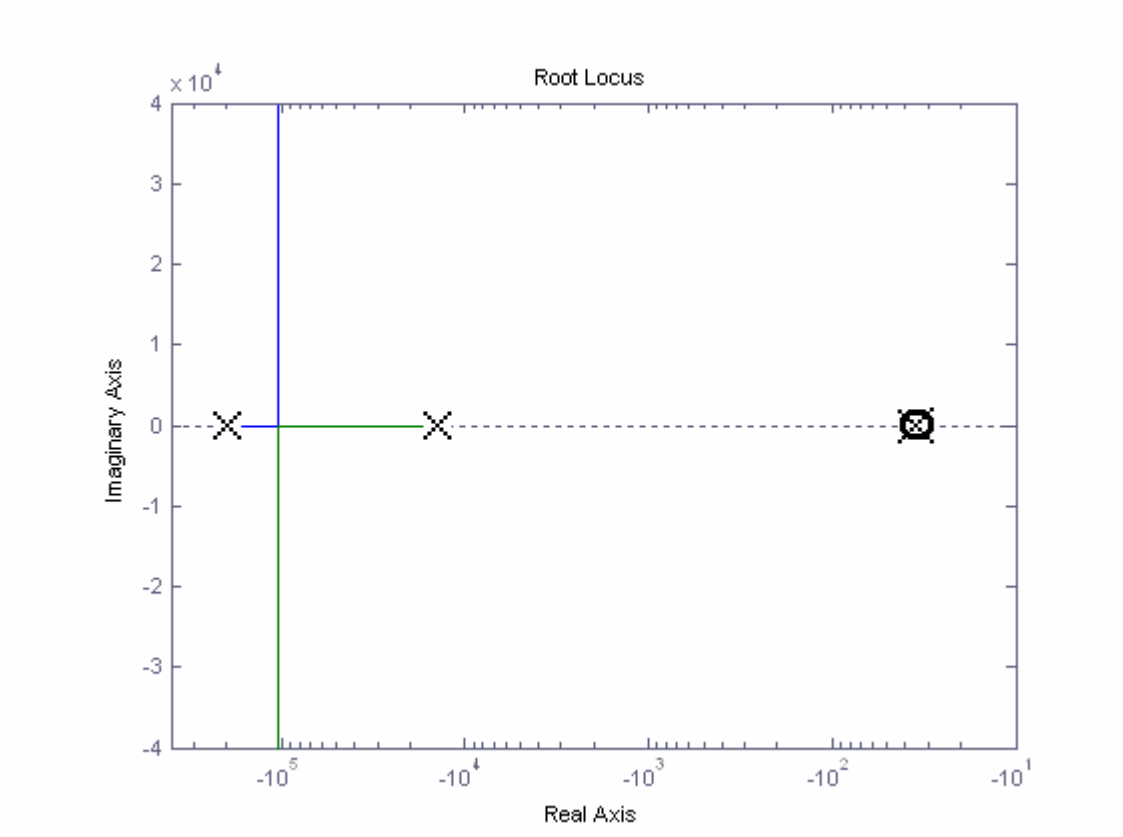

Figure 28. Final Closed Loop Pole/Zero Location

For future applications such as this, it would be appropriate to introduce another gain to rectify the situation. This gain would be called k_c and would be applied to a sampling of the output current. (It would also have the same scaling value as the capacitor current, k_c.) The resulting system is shown in Figure 29.

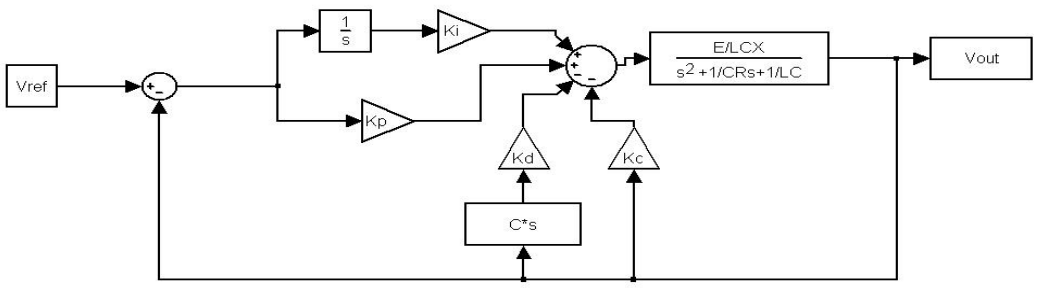

Figure 29. PID Controller with Proportional Current Gain Added.

The resulting closed loop transfer function is contained below:

$$\frac{v_C}{v_{ref}} = \frac{\frac{E}{aCL} k_{vout}\left[s k_p + k_i \right]}{s^3 + s^2\left[\frac{E k_d k_{ic}}{aL} + \frac{1}{CR}\right] + s\left[\frac{E k_p k_{vout}}{aCL} + \frac{1}{LC} + \frac{E k_{ic} k_c}{XCLR}\right] + \frac{E k_i k_{vout}}{aCL}} \tag{3.35}$$

The need for a fourth gain can better be described by simplifying the transfer function. Consider the following transfer function below. (Here the variables A, B, C, D, and Z represent merely the polynomial coefficients and do not correspond to actual values of the converter.)

$$\frac{v_C}{v_{ref}} = \frac{Z\left[s + A\right]}{s^3 + Bs^2 + Cs + D} \tag{3.36}$$

If the zero were to cancel a pole, the following two equations must be true:

$$\frac{v_C}{v_{ref}} = \frac{Z\left[s + A\right]}{\left(s + A\right)\left(s^2 + \left(-A + B\right)s + \frac{D}{A}\right)} \tag{3.37}$$

$$C = A\left(B - A\right) + \frac{D}{A} \tag{3.38}$$

Previous research on buck choppers at NPS has identified that the total integrative gain $k_i k_{vout}$, should be at least a decade greater than $k_p k_{vout}$. [8] This proportion essentially defines the variable A in equations 3.35 through 3.37. The gain $k_p k_{vout}$ must also be greater than the combined gain $k_d k_{ic}$. These gains will usually result in an acceptable response. The variable D is determined by the total integrative gain, $k_i k_{vout}$, the variable B is determined by the total derivative gain, $k_d k_{ic}$, while the variable Z is defined by the total voltage proportional gain, $k_p k_{vout}$. These values should be selected so as to determine a two pole response, as shown in equation 3.9. In order to achieve the desired over-damped response, the values should be chosen to place at least a decades distance between the two poles.

$$\boxed{\frac{v_C}{v_{ref}} = \frac{Z}{\left(s^2 + (-A + B)s + \frac{D}{A}\right)}} \tag{3.39}$$

Without the new proportional current gain, $k_c k_{ic}$, the variable C is solely determined by the proportional voltage gain, $k_p k_{vout}$. However, $k_p k_{vout}$ has already been locked into place upon the selection of $k_i k_{vout}$. By adding the proportional current gain $k_c k_{ic}$, the variable C may be altered without changing any other variables. This gives much more flexibility when trying to cancel the zero.

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IV. CONTROLLER ASSEMBLY

A. CHAPTER OVERVIEW

This chapter describes the physical construction of the controller assembly. As stated in Chapter III, the controller is a multi-loop type. The output voltage and capacitor current are compared against a reference signal to produce a duty cycle signal. This duty cycle signal is then fed into the Pulse Width Modulation (PWM) section where it is converted into four separate signals for use by the IGBT gate drivers. The IGBT gate drivers in turn determine which IGBT pair is conducting. Figure 30 shows an overall diagram of the controller sections. The remaining portions of this chapter discuss the controller and PWM section in greater detail.

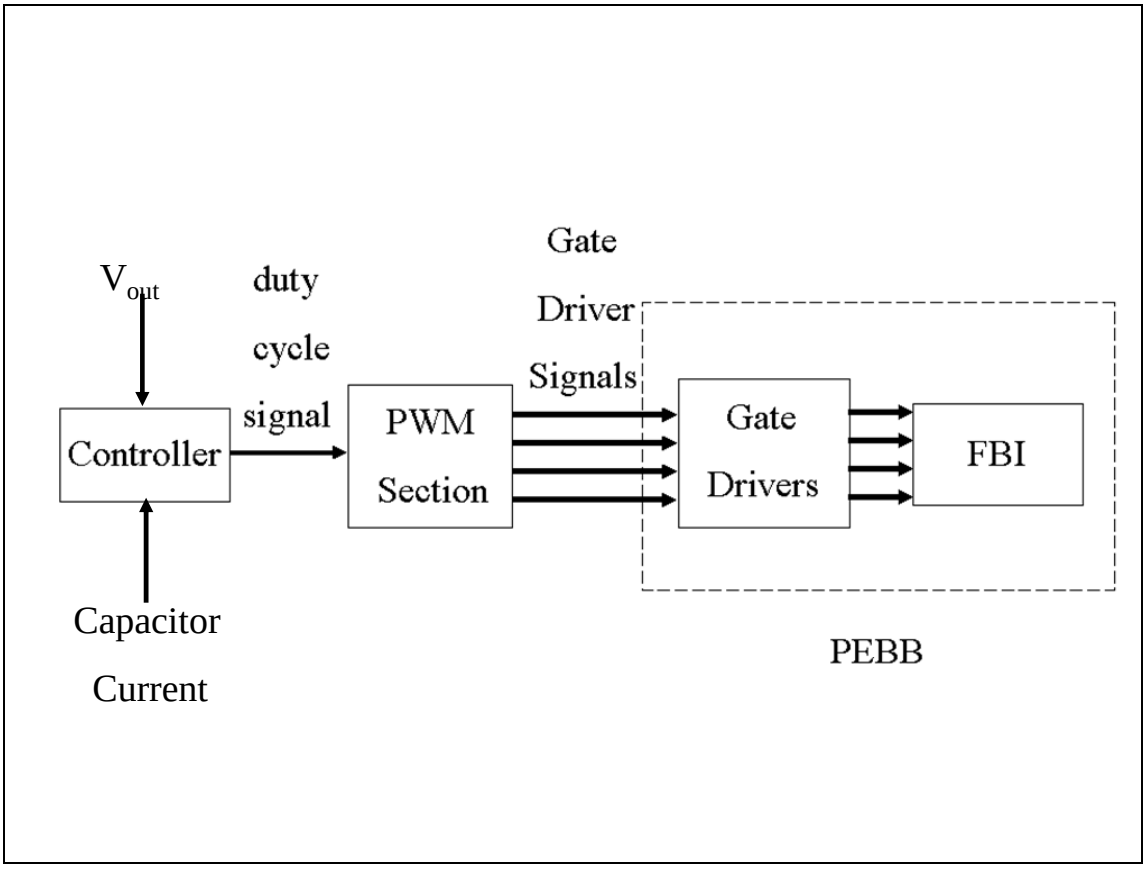

Figure 30. Controller Block Diagram

B. CONTROLLER

The purpose of the Controller is to generate a duty cycle signal that will be passed on to the PWM Section. The duty cycle signal is determined the output voltage, a reference voltage, and the capacitor current. The output voltage is first scaled down by the controller, which also generates the reference signal. These two functions will be discussed before describing the rest of the controller operation.

1. Output Voltage Scaling

In this subsection the output voltage is scaled down to an appropriate value that may be utilized by the rest of the controller. This gain, k_{vout}, is performed by a simple resistor network, shown in Figure 31. Utilizing the resistor values shown yields a k_{vout} of .0326, or 1/30. For an output voltage of 300V, this yields a value of approximately 10V. Since the controller utilizes power supplies of ± 15V, the sensed output voltage $\frac{V_{out}}{30}$ is well within the dynamic range of the controller.

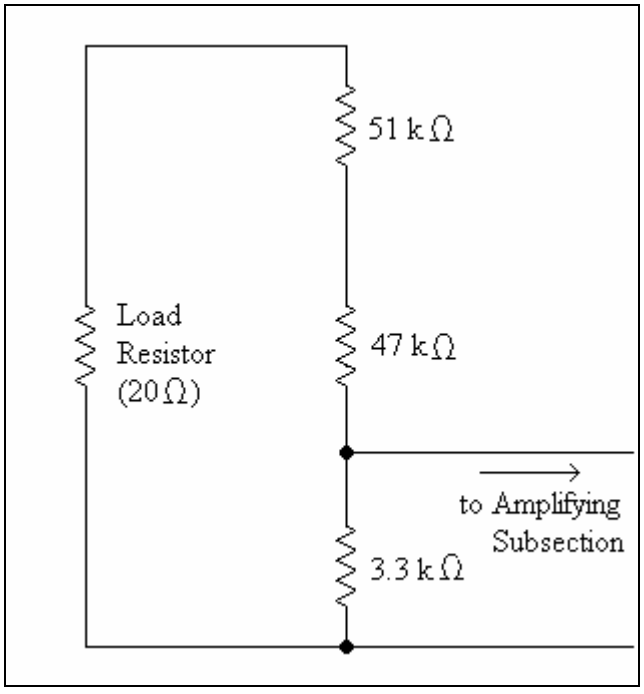

Figure 31. A Diagram of the Output Sampling Subsection

2. Reference Signal Generation

The generation of the reference signal is accomplished by a LM 317 Three Terminal Regulator. [9] This device develops a 1.25V difference between the terminals labeled Vout and Adj, as shown in Figure 32. The 2kΩ potentiometer R1 allows the reference voltage to be adjusted according to equation 4.1.

$$\left(\frac{1.25}{100}\right)\left(\frac{2000\times R1}{2000+R1}\right)+1.25 \tag{4.1}$$

The circuit allows a reference voltage of between 1.25V and 13.75V. 1.25V corresponds to an output voltage of 38V, 13.75V to an output voltage of 422V.

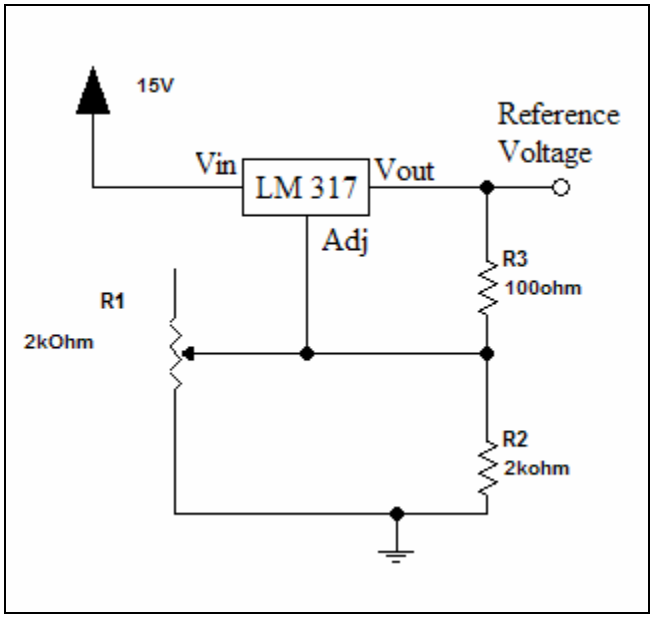

Figure 32. A Simplified Reference Signal Generator Schematic

3. Controller Operation

The Controller's main component is a LF 347 two input Quad Operational Amplifier (OP-AMP). [10]. All four OP-AMPS were utilized to provide the appropriate gains. Resistors with values between 5.1kΩ and 330kΩ were chosen to determine the

OP-AMP gains. These maximum and minimum values were chosen to ensure a stable, noise-free signal. Figure 33 shows a symbolic representation of the controller's operation.

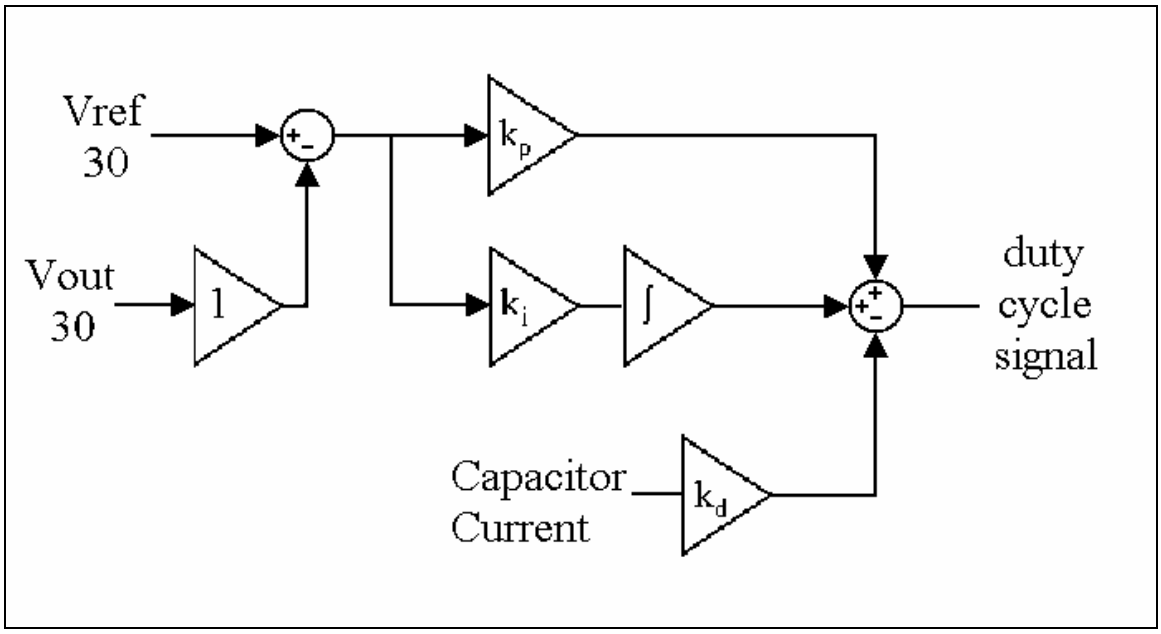

Figure 33. A Diagram of the Controller's Operation

The signal from the Output Sampling Subsection is sent to the first OP-Amp where it is buffered. In the second OP-AMP the buffered signal is subtracted from the reference signal to form an error signal. This resultant error signal is sent to both OP-AMPs three and four. In OP-AMP three the error signal is integrated and sent to OP-AMP four. OP-AMP then four amplifies the error signal, the integrated error signal, and the capacitive current signal. These three signals have the gains $k_p k_{out}$, $k_i k_{out}$, and $k_d k_c$ respectively. These three signals are combined to form a single duty cycle signal that is sent to the PWM Section.

C. PWM SECTION

The PWM Section is where the shape of the IGBT Gate Driver signals are formed. It consists of a UC 3637 PWM chip [11] and a logic subsection. The UC 3637

converts the duty cycle signal into a series of pulses; the logic section converts this pulsed signal into four distinct signals for use by the IGBT drivers. A diagram of this relationship is shown in Figure 34.

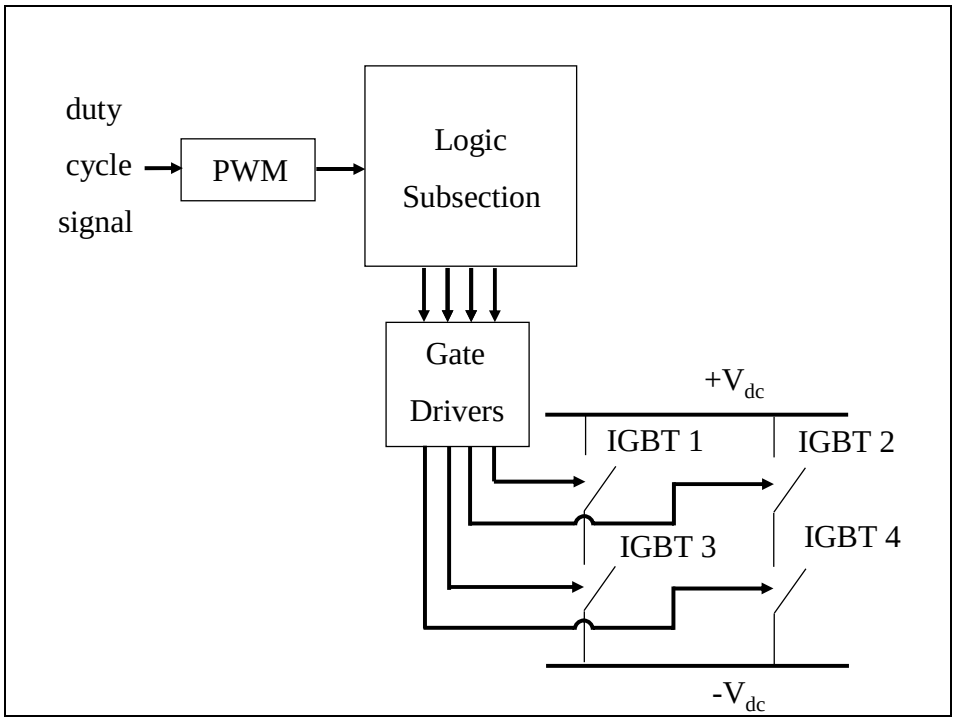

Figure 34. Diagram of PWM Section

1. PWM

The UC 3637 compares the duty cycle signal against an internally generated saw tooth oscillation signal with values of 9V and -3V. The output voltage pulse has a positive level of 13V and negative level of -13V. The pulse achieves its positive value when the output signal is greater than the saw tooth isolation and its negative value when the comparator signal is less than the isolation. This output pulse is then sent to the Logic subsection. Figure 35 shows an example of the Controller signal (brown), the saw tooth oscillation signal (aqua), and the output pulse (deep blue).

2. Logic Subsection

The Logic subsection utilizes a series of AND gates and a J-$\overline{K}$ flip flop to form the signals that will be sent to the individual IGBT gate drivers. The AND gates can be further subdivided into a delay element, and four gate elements. A diagram of the logic section is shown in Figure 36.

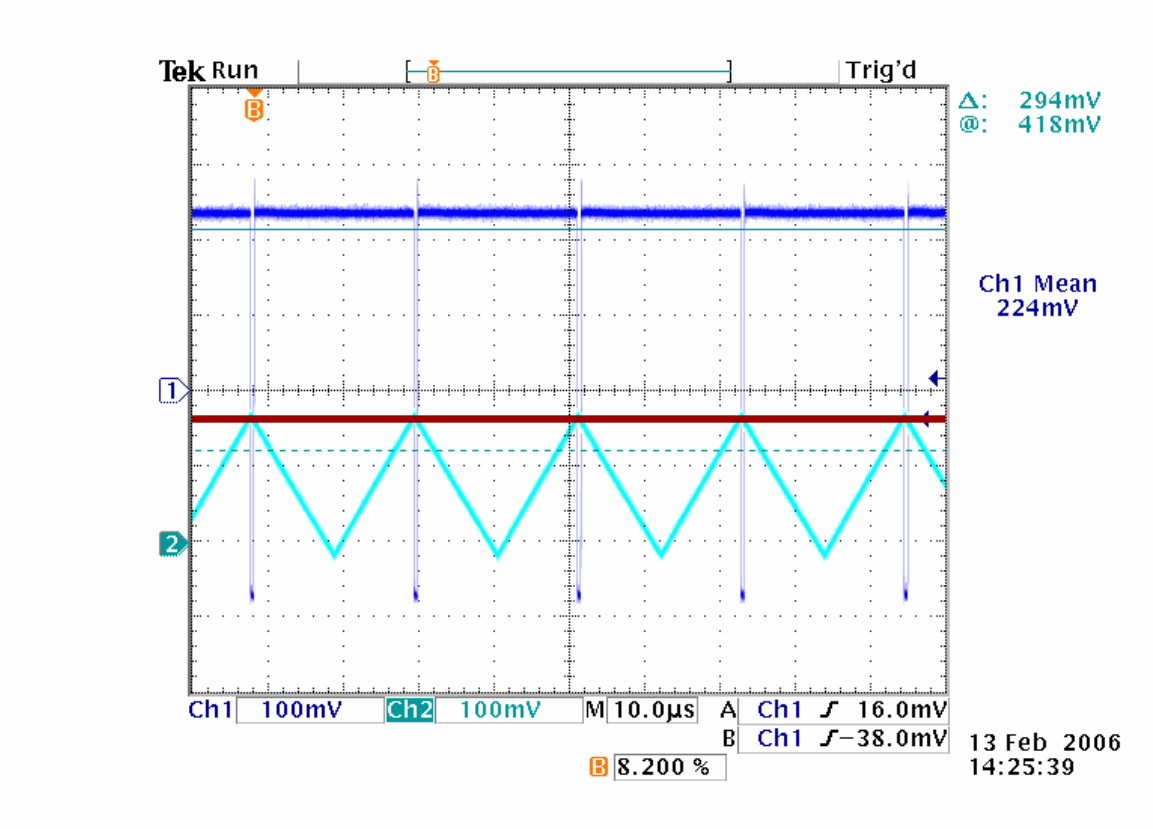

Figure 35. Duty Cycle versus Oscillation Signal versus PWM Output Voltage

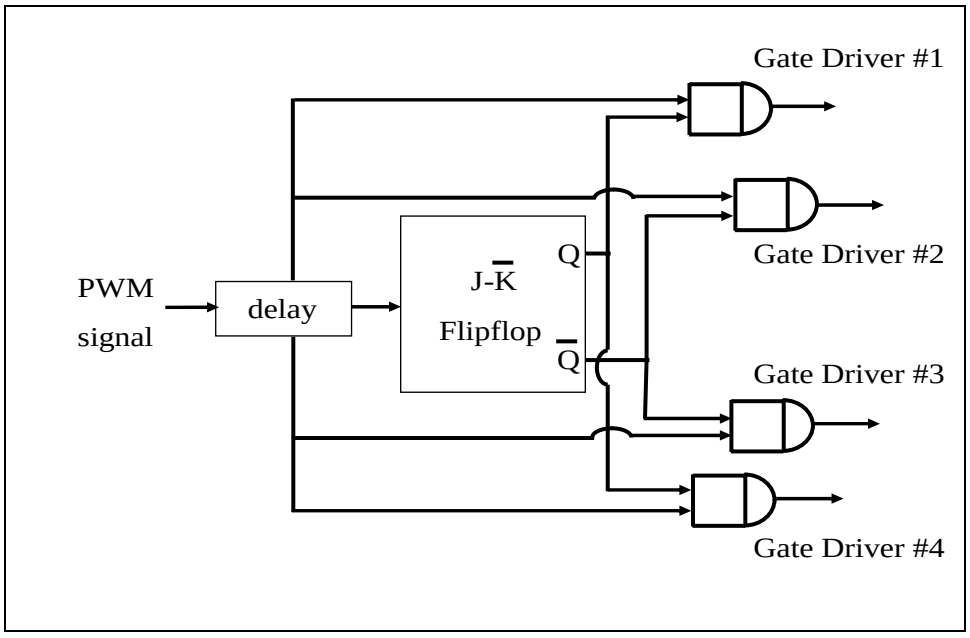

Figure 36. Logic Subsection

The first stage in the logic subsection is a delay element. The delay element is based on a DM74SL08 which is a microchip containing dual input quad AND gates. [12] All four AND gates are cascaded together, delaying the PWM signal by about 40ns.

The output of the delay element is then sent to a SN74109, which is a dual J-$\overline{K}$ Positive Edge Triggered Flip Flop with Preset and Clear Functions. [13] In the GIFB, the SN 74109 is wired to perform as a toggle flip flop. Whenever a positive pulse is received from the output of the delay element, the J-$\overline{K}$ Flip Flop will change states. This signal will serve to switch between Mode 1 and Mode 3 operation. This switching philosophy ensures the IGBTs can never cycle shut at the same time and short out the system. The output of the SN74109 is routed to the gate elements.

The gate elements consist of more DM74SL08 AND gates. These AND gates utilize input from both the J-$\overline{K}$ Flip Flop and the delay element. A display of gate signals contrasting Mode 1 and Mode 3 operation is shown in Figure 37.

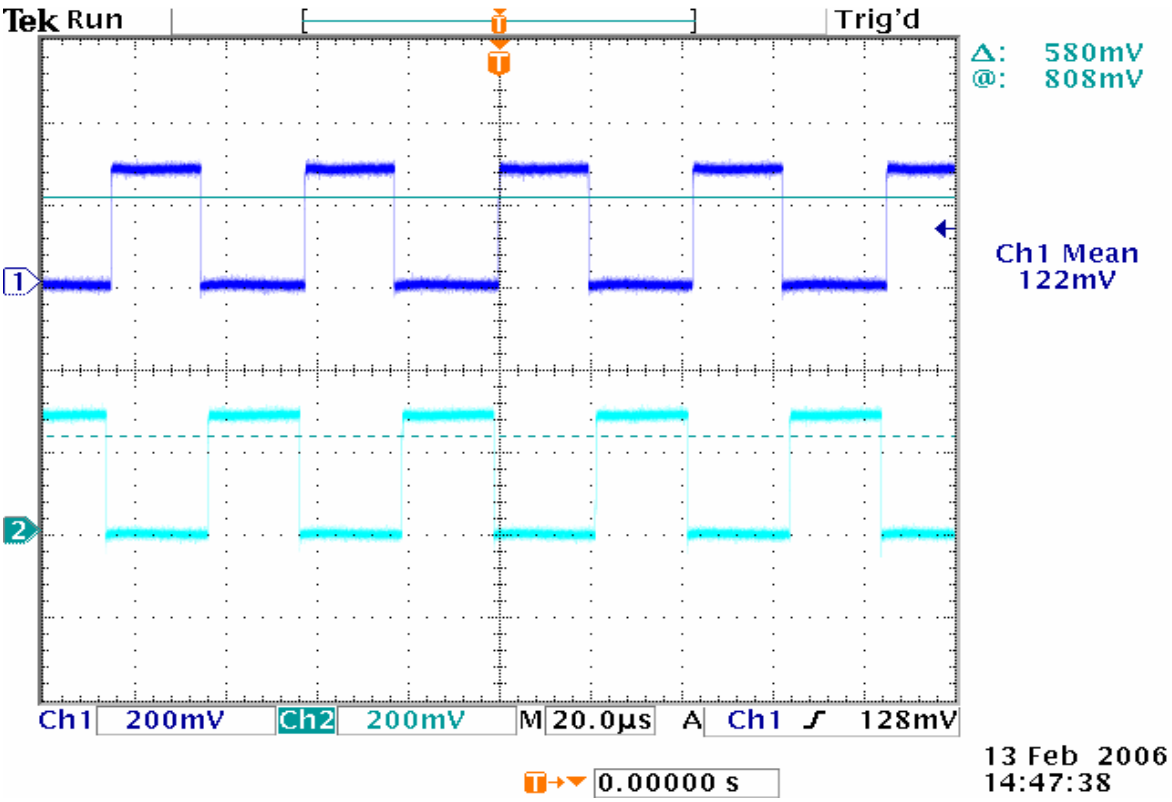

Figure 37. Mode 1 Gate Signals versus Mode 3 Gate Signals

V. RESULTS AND RECOMMENDATIONS

A. RESULTS

The GIFB was designed to operate as a unity gain, DC-DC converter with an input and output voltage of 300V DC. A load was selected (20Ω) that would result in an output power of 4.5kW. From past NPS experience with buck choppers, it was estimated that an efficiency rating of 98% would be attainable at full power; however, a final efficiency of 91.9% at reduced load was obtained. Due to equipment limitations and the prototype nature of the control boards, the actual maximum power obtained was 3.2kW. This was the result of a 240V/240V input/output voltage ratio and an 18Ω load. Figure 38 illustrates the efficiencies obtained for various voltages and currents.

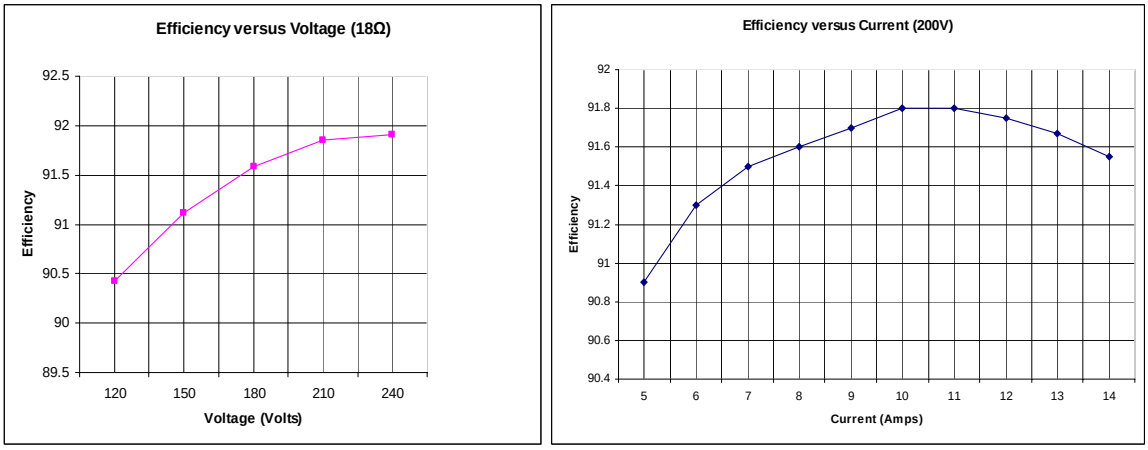

Figure 38. Efficiency for Various Input/Output Voltages

B. AREAS FOR FURTHER RESEARCH

1. Efficiency Improvements

As seen above, the GIFB has a maximum efficiency of approximately 92%. The power loss can be attributed to three areas of the power section: the FBI, the HFHE transformer and the Full-Wave Bridge Rectifier. In order to target the worst offender, thermal images were captured. These images are shown in Figures 39, 40, and 41. These

figures show quite clearly that the Full-Wave Bridge Rectifier is the largest heat source, and hence the portion of the GIFB that contributes to efficiency loss the most. In future endeavors with the GIFB, the rectifier should be replaced.

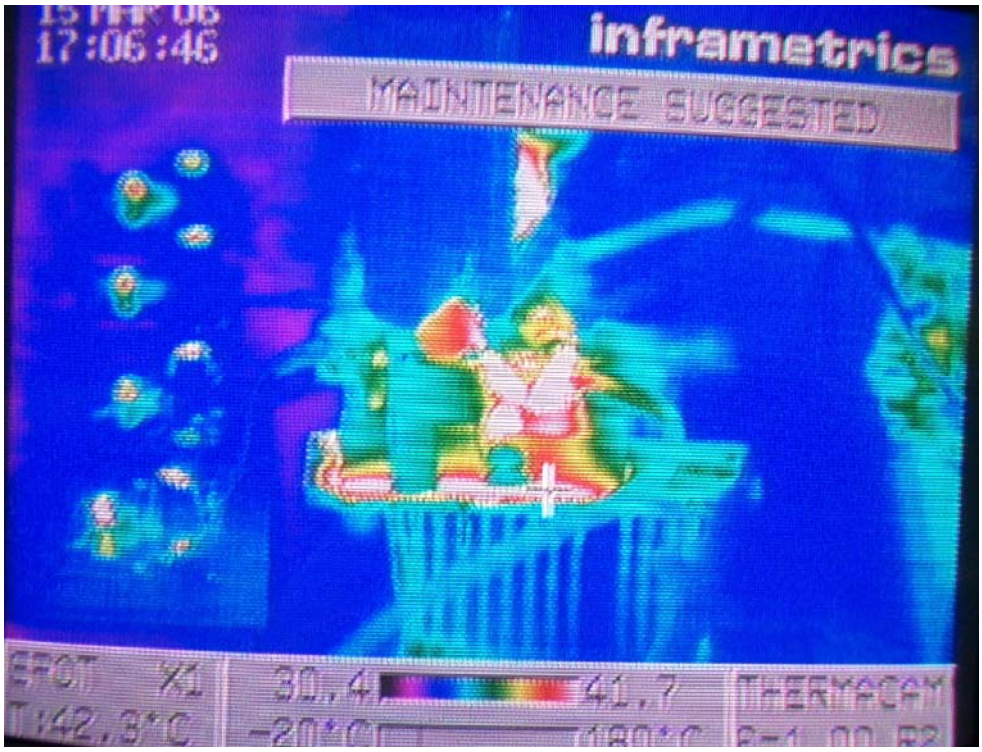

Figure 39. Thermal Image of FBI

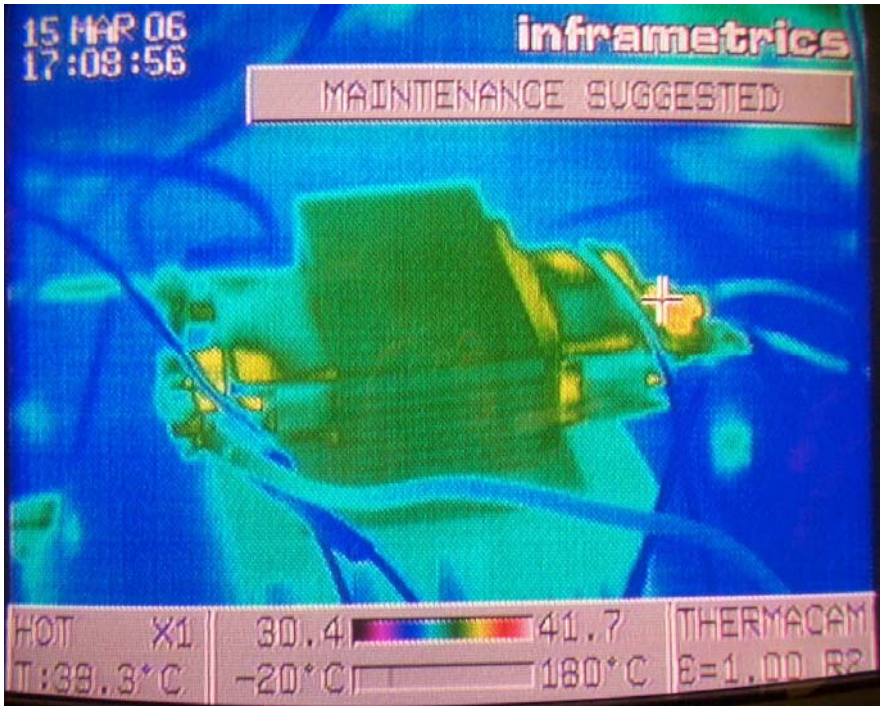

Figure 40. Thermal Image of HFHE Transformer

Figure 41. Thermal Image of Full-Wave Bridge Rectifier

2. Controller Improvements

The GIFB controller used in this thesis was built using copper boards and conventional wires to connect device pins. Although this allowed the controller to be modified as needed, component placement was somewhat haphazard due to these modifications. A future controller should be built on printed circuit boards (PCB) with a large ground plane to minimize the effects of noise.

Two options are easily available at NPS for controller digitalization: an NPS developed Xilinx based-controller and a dSPACE 1103 hardware-in-the-loop Digital Signal Processing (DSP) board. A DSP based solution is consistent with the Navy's desire for a programmable PEBB.

3. EM Interference Implications

There is currently no research regarding EM interference emanating from the GIFB. Future research should include possible effects upon a DCZEDS from the GIFB's 20kHz switching frequency.

4. Bi-Directional Galvanic Isolated Building Block (GIBB)

The GIFB is currently a unidirectional power converter; power only flows in a single direction from the DC bus to the load. The DCZEDS currently envisions the select placement of alternate power sources such as batteries, fuel cells, micro-turbines or diesel engines. Backup or distributed power sources would be housed within various zones. This power is trapped inside the resident zone unless the interface converter for the bus connection is bi-directional. Other zones could then be powered from a zone containing a source. Bi-directionality is a very useful attribute for 'dark-ship' startup. It is therefore useful to upgrade the existing GIFB into a bi-directional GIBB. In this sense, the GIBB could be said to simulate a true DC transformer. The modified topology is show in Figure 42. As can be seen the only major change is the swapping of the rectifier with a FBI which is identical to the input FBI.

As stated in Chapter II, the GIFB can be modeled as a modified buck converter. It was necessary to convert the DC voltage into a three step voltage for transmission over the HFHE transformer. Because the GIFB was modeled on a buck converter, the HFHE transformer was used to step up the voltage to achieve a unity gain. If the converter was

made bi-directional, the HFHE transformer would step down the voltage when the converter powers the main bus. By adding another FBI to the load side and a capacitor to the bus side, the converter can be altered to provide a boost capability when powering the bus. When coupled with the step down ability of the transformer, this provides a unity gain. The Full-Wave Bridge Rectifier is no longer required (on either side) because the IGBT anti-parallel diodes now provide this function.

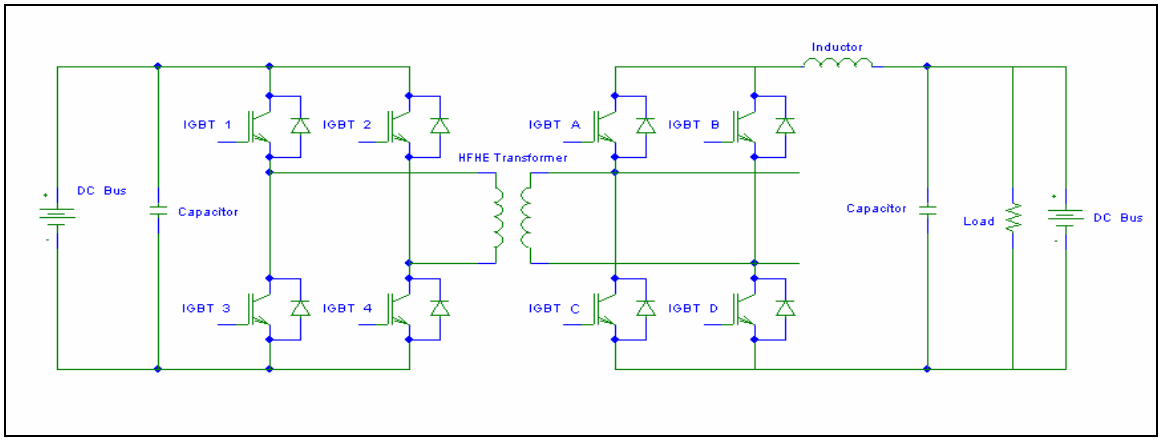

Figure 42. Diagram of the GIBB

The added components now resemble a boost chopper when the alternate power source is powering the DC Bus. In order to conform to industry standards, it is recommended that the GIBB be designed to operate at a supply and load voltage of 700V. This corresponds to the recommended bus voltage when using standard 1200V IGBTs.

5. Three-Phase GIBB

Another topology offers the potential for increased power density. This topology utilizes the basic topology of the GIBB, but upgrades the FBIs to three-phase FBIs. Three HFHE transformers connected in a delta-delta fashion are now required to magnetically couple all three phases. A diagram of the three-phase GIBB is shown in Figure 43.

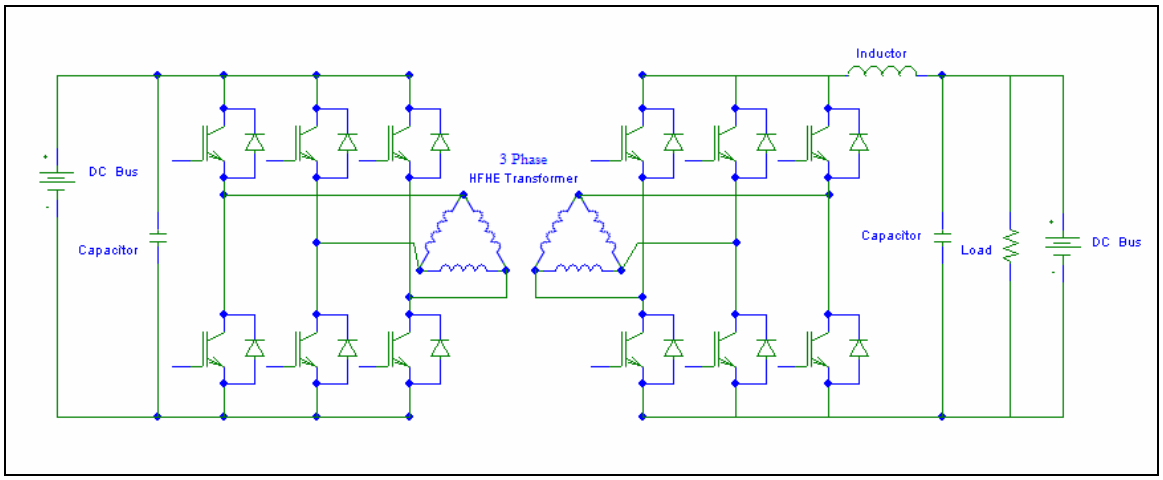

Figure 43. Diagram of the Three-Phase GIBB

The prime advantage of utilizing a three-phase GIBB lies in the reduced size of the filter components. Specifically the inductor and capacitor are dramatically reduced because of the higher frequency ripple inherent with a higher pulse-count. In addition, the switching frequency of the IGBTs is reduced. With a single-phase GIBB, each IGBT cycles at a frequency of 10kHz (resulting in an inverter frequency of 20kHz); each IGBT in the three-phase GIBB only has to cycle at a frequency of 6.6kHz.

The primary disadvantage of the three-phase GIBB is the addition of two more HFHE transformers. Furthermore, the extra IGBTs add to cost. At smaller powers, it is anticipated that the single-phase GIBB will have a higher power density than the three-phase GIBB. As power increases, eventually the three-phase GIBB will have a larger power density. Figure 44 depicts one possible relationship. Further research is required to ascertain the 'Breakpoint' between the single and three-phase units.

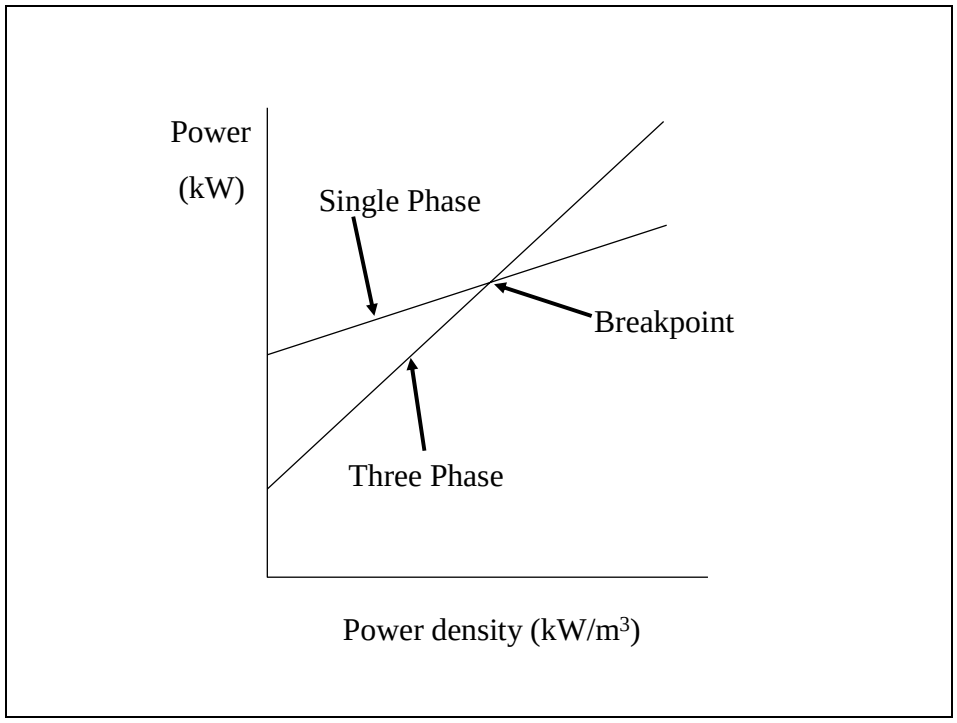

Figure 44. Relationship of Power Density to Number of Phases

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APPENDIX A. MATLAB CODE

A. MAIN CODE

```
%program for calculating Sarar thesis step response


clear all

format long

L=.00214;

R=20;

E=300;

C=.000144;


kic=.075;

kvout=(3.3/(3.3+98));


a=.75;%turns ratio of transformer, primary to secondary


%values from program gaincalcsfinal

ki=2241.8;

kp=64.7;

kd=15;


%calculates what gains would be without equipment limitations
```

```
gaini=ki*(kvout/a)

gainp=kp*(kvout/a)

gaind=kd*(kic/a)

%integrative gain is 97.4, proportional gain 2.8, capacitor current gain

%1.5




opentop=E;

openbottom=[(L*C*a) ((L*a)/R) a];

open=tf(opentop,openbottom);

%open is open loop transfer function



top=[((kp*E*kvout)/(L*C*a)) ((ki*E*kvout)/(L*C*a))];

bottom=[1  ((1/(R*C))+((E*kic*kd)/(L*a)))  ((1/(L*C))+((E*kvout*kp)/(L*a*C)))
*((E*kvout*ki)/(L*a*C))];


closed=tf(top,bottom);

%closed is closed loop transfer function

step(closed)


roots(bottom) %closed loop poles
```

roots(top) %closed loop zeros

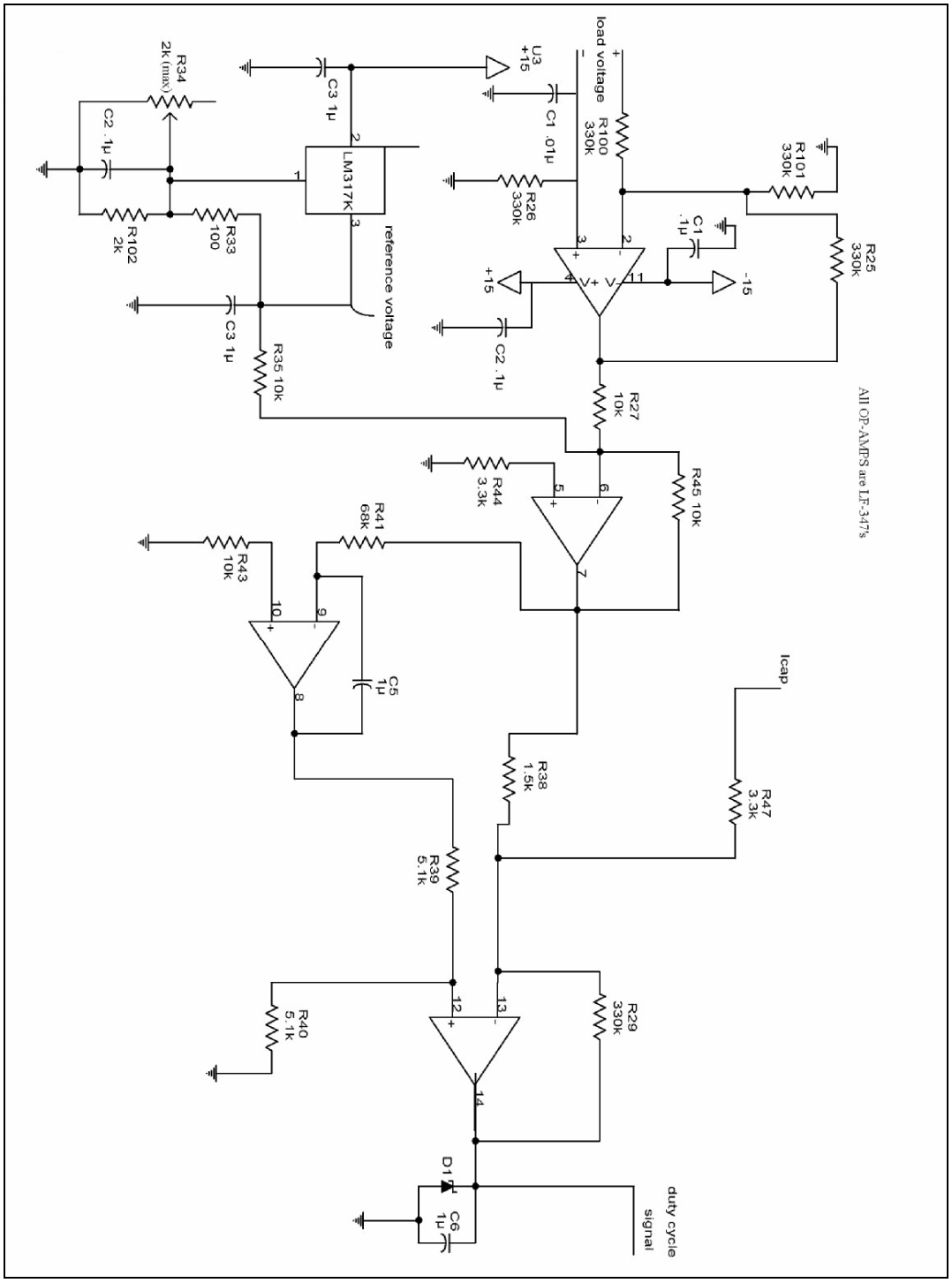
B. GAIN CALCULATION CODE

```
%program for calculating resistor and capacitor sizes to achieve
%gains required in program thesis final

format long

%note: all components referened occur in schematic 1

ca=.000001;
%refers to Capacitor C5

ra=18000;
%refers to Resistor R41

rb=5100;
%refers to Resistor R39

rc=5100;
%refers to Resistor R40

rd=5100;
%refers to Resistor R38
```

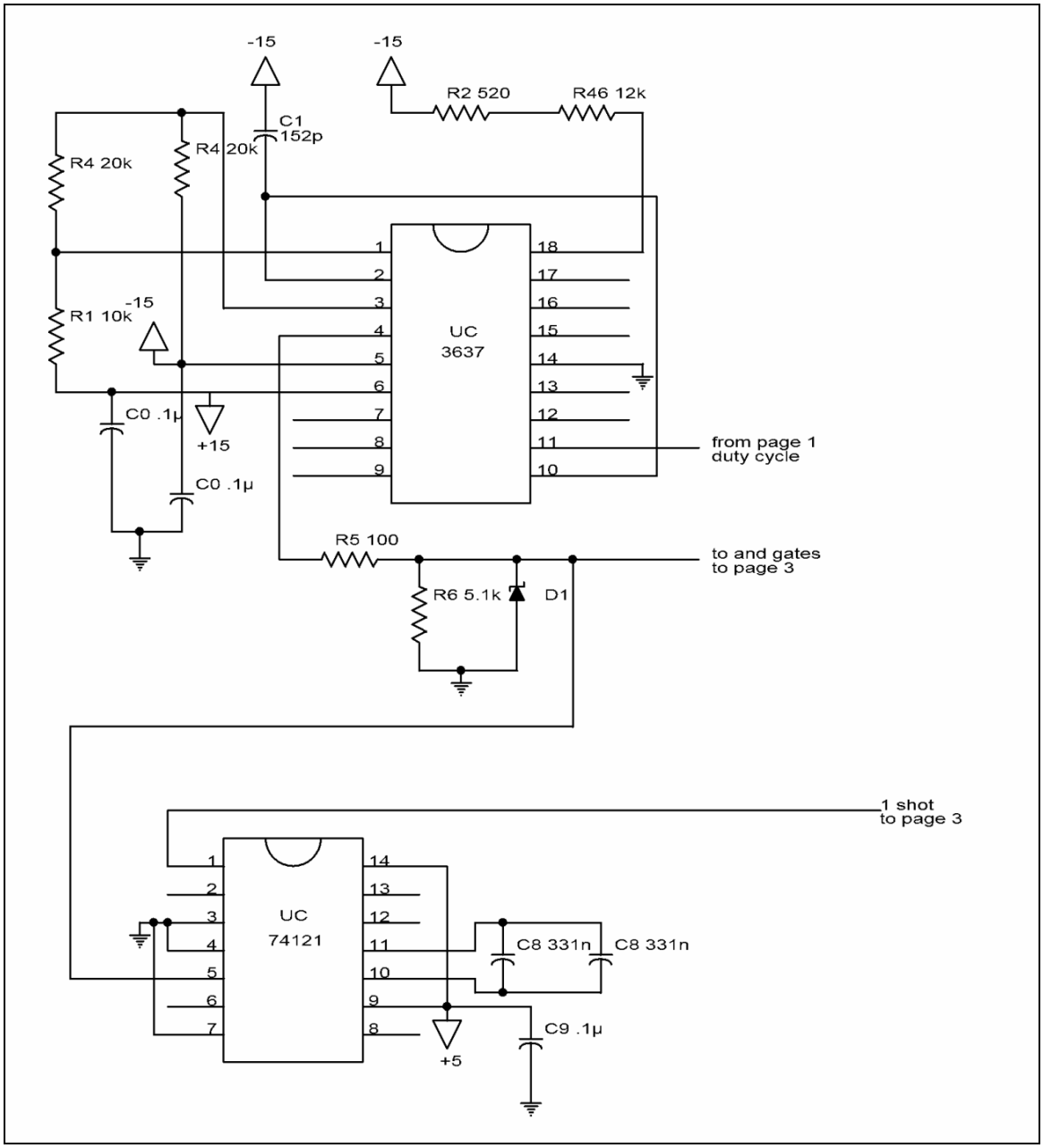
```
re=22000;
%refers to Resistor R47

rf=330000;
%refers to Resistor R29

kci=.075
%kci refers to the stepdown effect of the capacitor current probe


ki=((1/(ra*ca))*(rc/(rc+rb))*(1+(rf/re)+(rf/rd)))
kp=(rf/rd)
kd=(rf/re)
```

APPENDIX B. CONTROLLER SCHEMATICS

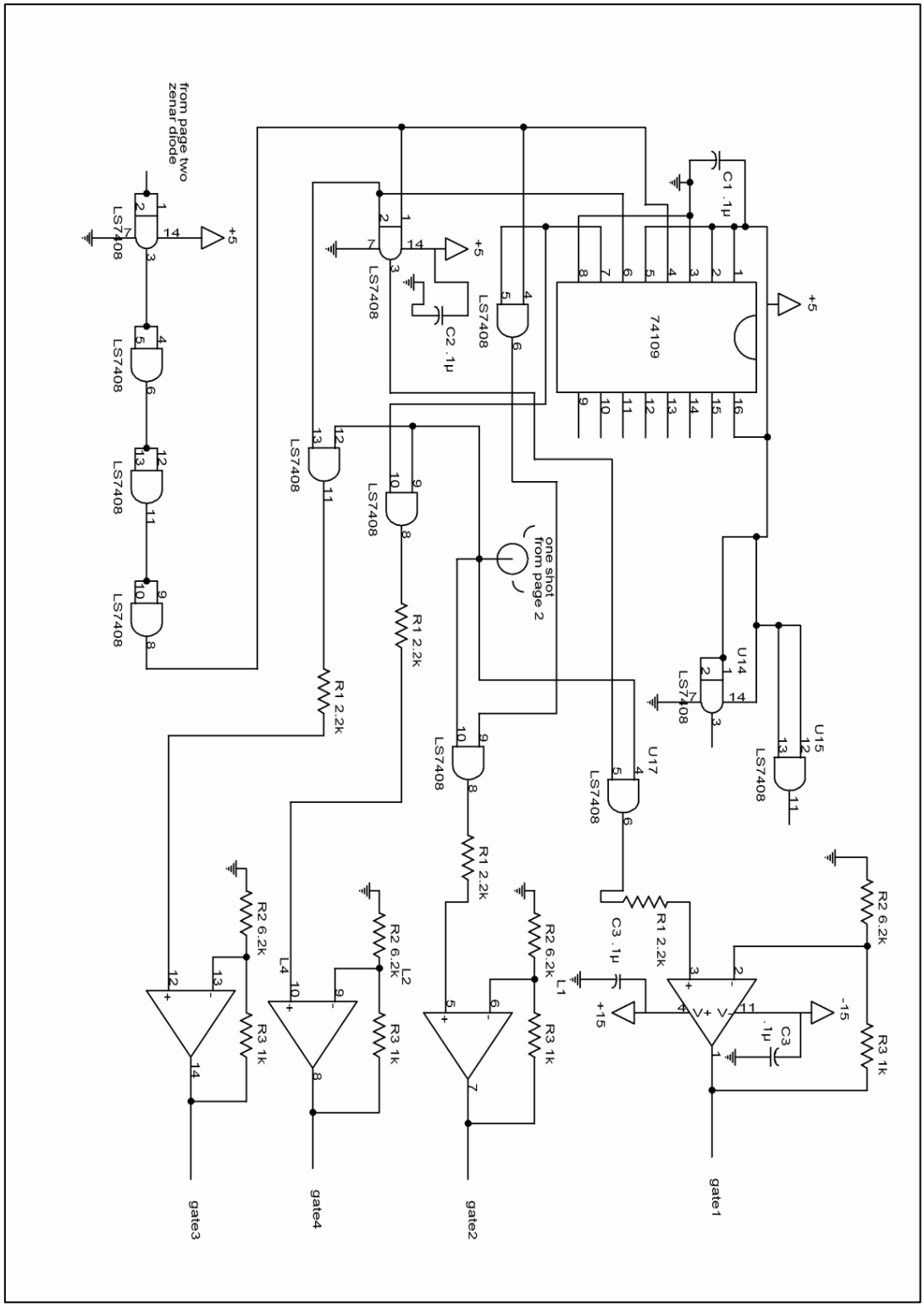
A. CONTROLLER SCHEMATIC #1



B. CONTROLLER SCHEMATIC #2



C. CONTROLLER SCHEMATIC #3



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APPENDIX C. DATA SHEETS

A. FBI

POWEREX TENTATIVE PP150T120

Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

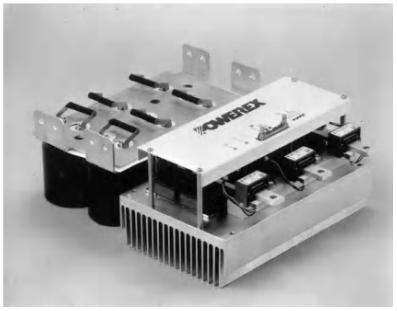
POW-R-PAK™
150A / 1200V
3 phase IGBT Assembly

Description:

The Powerex POW-R-PAK™ is a configurable IGBT based power assembly that may be used as a converter, chopper, half or full bridge, or three phase inverter for motor control, power supply, UPS or other power conversion applications.

The power assembly is mounted on a forced air-cooled heatsink and features state-of-the-art Powerex F-series trench gate IGBTs with low conduction and switching losses for high efficiency operation. The POW-R-PAK™ includes a low inductance laminated bus structure, optically isolated gate drive interfaces, isolated gate drive power supplies, and a DC-link capacitor bank. The control board provides a simple user interface along with built-in protection features including overvoltage, undervoltage lockout, overcurrent, overtemperature, and short circuit detection.

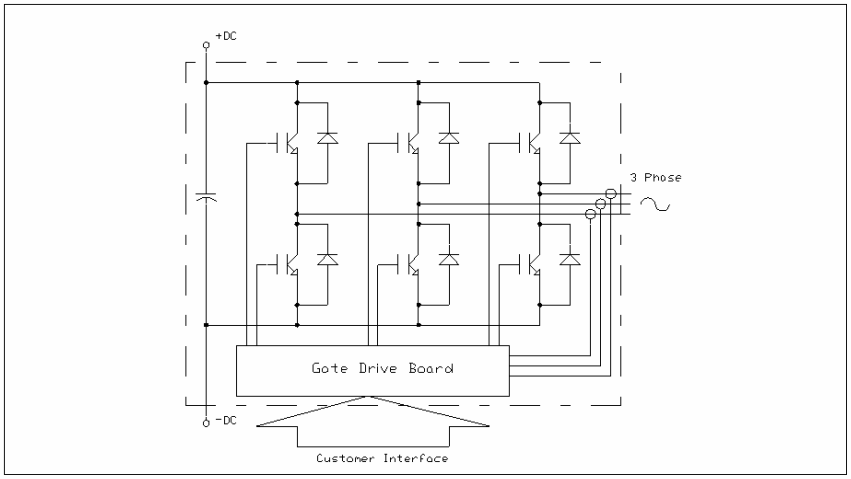
Depending on application characteristics the POW-R-PAK™ is suitable for operation with DC bus voltages up to 800VDC and switching frequencies above 20kHz.



Features:

- High performance IGBT inverter bridge
- Integrated gate drive with fault monitoring & protection
- System status / troubleshooting LEDs to verify or monitor proper operation
- Isolated gate drive power supplies
- Low inductance laminated bus
- Output current measurement & feedback
- Superior short circuit detection & shoot through prevention

Schematic



Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

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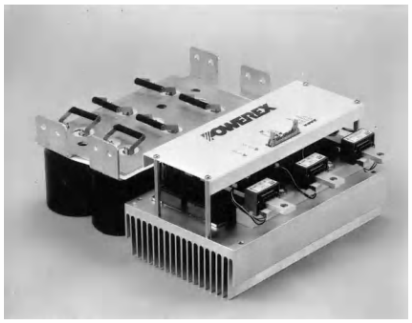

Features:

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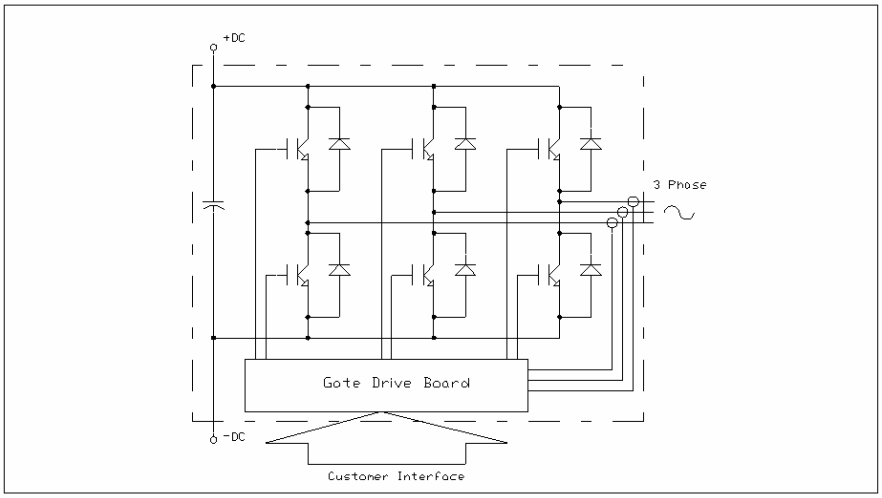
- System status / troubleshooting LEDs to verify or monitor proper operation
- Isolated gate drive power supplies
- Low inductance laminated bus
- Output current measurement & feedback
- Superior short circuit detection & shoot through prevention

Schematic



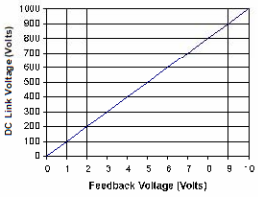
Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

POW-R-PAK™
150A / 1200V
3 phase IGBT Assembly

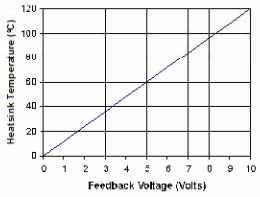
Gate Drive Board Electrical Characteristics

Characteristics	Min	Typ	Max	Units
Unregulated +24V Power Supply	20	24	30	Volts
Regulated +15V Power Supply	14.4	15	18	Volts
PWM Input On Threshold	12	15		Volts
PWM Input Off Threshold		0	2	Volts
Output Overcurrent Trip		225		Amperes
Overtemperature Trip	96	98	100	°C
Overvoltage Trip		920		Volts
DC Link Voltage Feedback		See Figure Below		Volts
Heatsink Temperature Feedback		See Figure Below		Volts
Output Current Feedback		See Figure Below		Volts

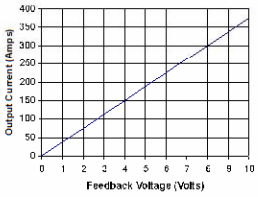
DC Link Feedback



Heatsink Temperature Feedback



Output Current Feedback



Thermal and Mechanical Characteristics

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Units
IGBT Thermal Resistance, Junction to Case	$R_{th(j\text{-}c)}Q$	Per IGBT ½ module	-	0.11	0.21	°C/W
FWD Thermal Resistance, Junction to Case	$R_{th(j\text{-}c)}D$	Per FWD ½ module			0.24	°C/W
Contact Thermal Resistance	$R_{th(c\text{-}f)}$		-	0.020	-	°C/W
Heatsink Thermal Resistance	$R_{th(f\text{-}a)}$	1500 LFM airflow		0.040		°C/W
Mounting Torque, AC terminals				75	90	in-lb
Mounting Torque, DC terminals				130	150	in-lb
Mounting Torque, Mounting plate				130	150	in-lb
Weight				21		lb

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Gate Drive Board Interface Signal Definitions

Pin	Signal Name	Description
1	Shield	Connected to circuit ground
2	PWM A-	0-15 V signal controlling the duty cycle of A- IGBT
3	Phase A Error[1]	Open collector output, external pull-up resistor required LOW = No Error; Floating = Phase A overcurrent or short circuit
4	PWM A+	0-15 V signal controlling the duty cycle of A+ IGBT
5	PWM B-	0-15 V signal controlling the duty cycle of B- IGBT
6	Phase B Error[1]	Open collector output, external pull-up resistor required LOW = No Error; Floating = Phase B overcurrent or short circuit
7	PWM B+	0-15 V signal controlling the duty cycle of B+ IGBT
8	PWM C-	0-15 V signal controlling the duty cycle of C- IGBT
9	Phase C Error[1]	Open collector output, external pull-up resistor required LOW = No Error; Floating = Phase C overcurrent or short circuit
10	PWM C+	0-15 V signal controlling the duty cycle of C+ IGBT
11	Overtemp[1]	Open collector output, external pull-up resistor required LOW = No Error; Floating = heatsink overtemp
12	Not Connected	
13	DC Link Voltage	Analog voltage representation of DC link voltage
14	24 VDC input power[2]	20 – 30 VDC input voltage range
15	24 VDC input power[2]	20 – 30 VDC input voltage range
16	15 VDC input power[2]	14.4 – 18 VDC input voltage range
17	15 VDC input power[2]	14.4 – 18 VDC input voltage range
18	GND	Ground reference for 15 and 24 VDC inputs
19	GND	Ground reference for 15 and 24 VDC inputs
20	Heatsink Temperature	Analog voltage representation of heatsink temperature
21	GND[3]	Tied to pins 18 and 19
22	I_{out} Phase A	Analog voltage representation of phase A output current
23	GND[3]	Tied to pins 18 and 19
24	I_{out} Phase B	Analog voltage representation of phase B output current
25	GND[3]	Tied to pins 18 and 19
26	I_{out} Phase C	Analog voltage representation of phase C output current

Notes:
1. Open collectors can be pulled up to 30 V max and sink 50mA continuous.
2. Do not connect a 15 VDC and 24 VDC source to the unit at the same time, use one or the other.
3. GND signals to be used for analog feedback signals, i.e. twisted pair with I_{out} Phase A.

Gate Drive Board Interface Connector

Description	Symbol	Type	Manufacturer
Gate Drive Board Interface Header	J1	0.100" x 0.100" latching header, 26 pin	3M# 3429-6002 or equivalent
Recommended Mating Socket	-	0.100" x 0.100" IDC socket, 26 pin	3M# 3399-7600 or equivalent
Recommended Strain Relief	-	Plastic strain relief	3M# 3448-3026 or equivalent

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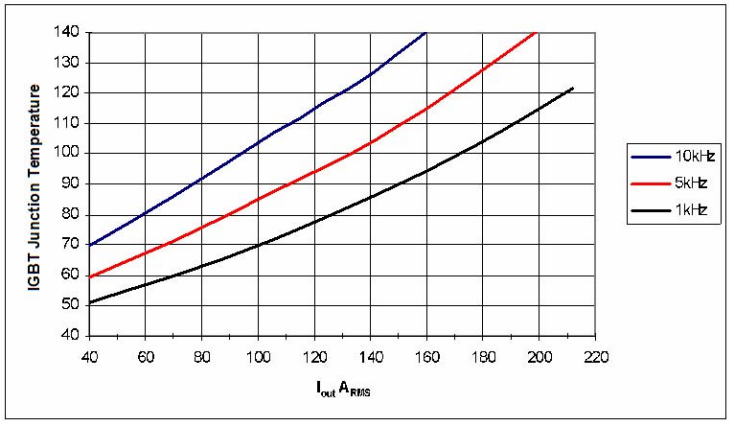
POW-R-PAK™
150A / 1200V
3 phase IGBT Assembly

Performance Curves

Effective Output Current vs. Carrier Frequency (Typical)



Condition	Symbol	Value	Units
Ambient Temperature	T_A	40	°C
DC Bus Voltage	V_{CC}	600	Volts
Load Power Factor	cos ϕ	0.8	
IGBT Saturation Voltage	$V_{CE(sat)}$	Typical @ T_J = 125°C	Volts
IGBT Switching Loss	E_{SW}	Typical @ T_J = 125°C	mJ
Airflow	-	1500	LFM
Switching Conditions	3 phase PWM, 60Hz sinusoidal output		

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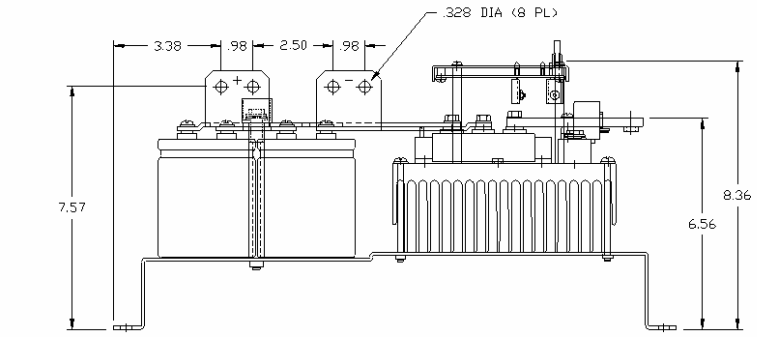
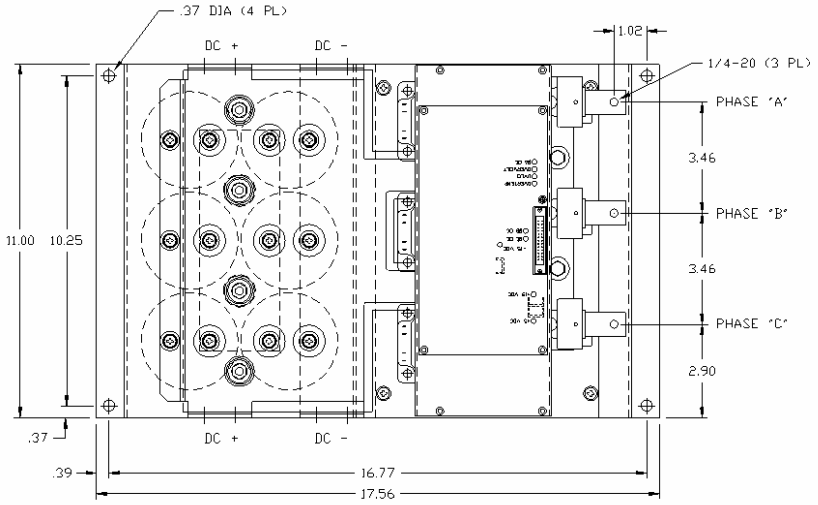
POW-R-PAK™
150A / 1200V
3 phase IGBT Assembly

Mechanical Drawing





B. HFHE TRANSFORMER

TRANSFORMERS AND INDUCTORS

SIZE 5000 Power Capacity 5 to 20kW

Description

The Payton **SIZE 5000** provides a planar solution for high power applications (such as traction, induction heating etc.) providing high efficiency, low EMI, excellent repeatability, low profile and weight with an operating temperature range of -40°C to +130°C.

1. Transformer Application

POWER CAPACITY	DIMENSIONS (mm)	TYPICAL WEIGHT	DIELECTRIC ISOLATION	OPERATING VOLTAGE	OPERATING CURRENT (RMS)
5kW, forward at 50 kHz 20kW, full bridge at 100 kHz	L = 180-230 W = 104-145 H = 20-60	2-3 kg.	500 Vdc- 4k Vrms	1000 Vpeak max.	1000 A max.

Typical efficiency: 97-99%

Recommended frequency range: 20 kHz – 300 kHz.

Topologies:

Full bridge; Half bridge; Push-Pull; Forward;
Resonant topologies (in order of preference).

Mounting Options: a. Horizontal b. Vertical

2. Inductor Application

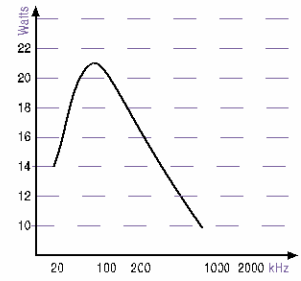
STANDARD A_L (nH/t²)	1600	1000	630	400	315	250	160
TYPICAL VALUE OF MAX. Amper Turns	190	310	490	790	950	1202	1500

A_L values not listed are available upon request.

3. Typical Thermal Impedance For Different Cooling Conditions

NATURAL COOLING (Hot Spot - Air)	BLOWING AIR 3m/sec (Hot Spot - Air)	ONE SIDE HEATSINK (Hot Spot - Heatsink)	TWO SIDE HEATSINK (Hot Spot - Heatsink)
1.7°/W	1.3°/W	1.6°/W	0.8°/W

Power Capacity vs. Frequency*



*For single output AC to DC full bridge power supply transformer with turns ratio of 6.

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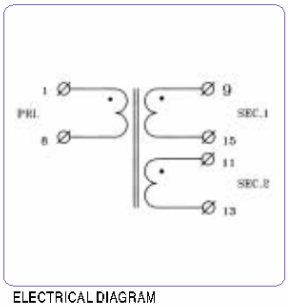
EXAMPLE

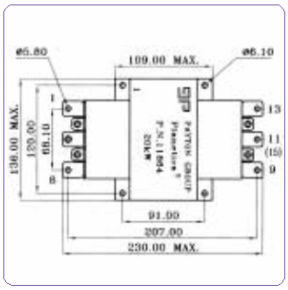
Transformer Type T5000 AC P.N. 11864

This T5000-16-6-6, super high power, high input voltage, high frequency, small dimensional planar transformer is developed for a high power density AC-DC converter and may be used in high power applications, providing the following specifications:

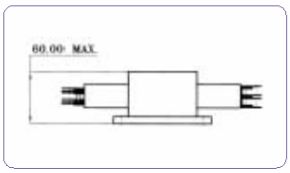
Transformer Specifications	
Total output power	20kW (590 Vdc@34 Adc)
Operating frequency	100 kHz
Input voltage range	815 - 900 Vdc
Topology	Full bridge, resonant
Max. Volt-Sec. product	8.15 V-msec
Duty cycle	2 x 0.5 max.
Primary current Secondary 1,2 output current	27 Arms max. 30 Arms max.
Primary to Sec. 1,2 ratio	16 : 6
Dielectric strength pri. to sec.1+sec.2+core sec.1, sec.2 to core	 3750 Vrms 1500 Vrms
Ambient temperature	-20°C to +50°C
Total losses (With 45°C heat sink)	95W
Hotspot temperature (With 45 °C heat sink)	120°C max.
Weight	3000 gr.



ELECTRICAL DIAGRAM



TOP VIEW



SIDE VIEW

(All dimensions are given in mm.)

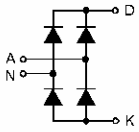
C. FULL-WAVE BRIDGE RECTIFIER

IXYS **VBE 55-12NO7**

ECO-PAC™
Single Phase Rectifier Bridge
with Fast Recovery Epitaxial Diodes (FRED)

I_{dAV} = 59 A
V_{RRM} = 1200 V
t_{rr} = 40 ns

V_{RSM} V	V_{RRM} V	Typ
1200	1200	VBE 55-12NO7



Symbol	Conditions		Maximum Ratings	
I_{dAV} ①	T_C = 85°C, module		59	A
I_{dAVM}			90	A
I_{FSM}	T_{VJ} = 45°C	t = 10 ms (50 Hz), sine	200	A
	V_R = 0	t = 8.3 ms (60 Hz), sine	220	A
	T_{VJ} = T_{VJM}	t = 10 ms (50 Hz), sine	170	A
	V_R = 0	t = 8.3 ms (60 Hz), sine	190	A
I^2t	T_{VJ} = 45°C	t = 10 ms (50 Hz), sine	200	A^2s
	V_R = 0	t = 8.3 ms (60 Hz), sine	205	A^2s
	T_{VJ} = T_{VJM}	t = 10 ms (50 Hz), sine	145	A^2s
	V_R = 0	t = 8.3 ms (60 Hz), sine	150	A^2s
T_{VJ}			-40...+150	°C
T_{VJM}			150	°C
T_{stg}			-40...+125	°C
V_{ISOL}	50/60 Hz, RMS	t = 1 min	3000	V~
	I_{ISOL} ≤ 1 mA	t = 1 s	3600	V~
M_d	Mounting torque (M4)		1.5-2/14-18	Nm/lb.in.
Weight	typ.		19	g

Features

- Package with DCB ceramic base plate in low profile
- Isolation voltage 3000 V~
- Planar passivated chips
- Low forward voltage drop
- Leads suitable for PC board soldering

Applications

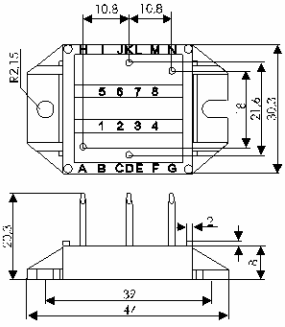
- Supplies for DC power equipment
- Input and output rectifiers for high frequency
- Battery DC power supplies
- Field supply for DC motors

Advantages

- Space and weight savings
- Improved temperature and power cycling capability
- Small and light weight
- Low noise switching

Symbol	Conditions		Characteristic Values typ.	max.	
I_R	V_R = V_{RRM}	T_{VJ} = 25°C		0.25	mA
	V_R = V_{RRM}	T_{VJ} = T_{VJM}		1.0	mA
V_F	I_F = 30 A	T_{VJ} = 25°C		2.71	V
V_{T0}	for power-loss calculations only			1.31	V
r_T				15	mΩ
R_{thJC}	per diode; DC current			0.9	K/W
R_{thCH}	per diode, DC current, typ.			0.3	K/W
I_{RM}	I_F = 50 A, -diF/dt = 100 A/µs		6	11.4	A
	V_R = 100 V, L = 0.05 mH, T_{VJ} = 100°C				
t_{rr}	I_F = 1 A; -di/dt = 200 A/µs; V_R = 30 V, T_{VJ} = 25°C		40	tbd	ns
a	Max. allowable acceleration			50	m/s^2
d_S	creeping distance on surface			11.2	mm
d_A	creepage distance in air			9.7	mm

Dimensions in mm (1 mm = 0.0394")



Data according to IEC 60747 refer to a single diode unless otherwise stated
① for resistive load at bridge output.

IXYS reserves the right to change limits, test conditions and dimensions.

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1 - 2

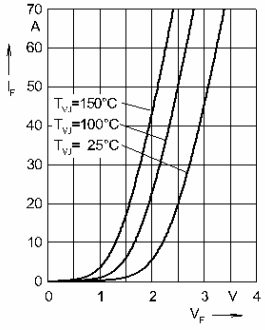

Fig. 1 Forward current I_F versus V_F

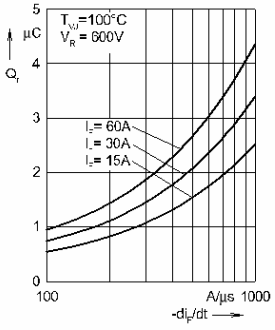

Fig. 2 Reverse recovery charge Q_r versus $-di_F/dt$

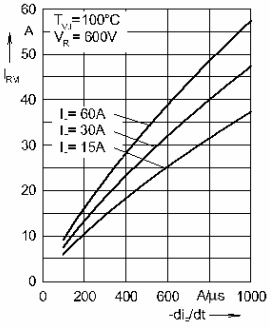

Fig. 3 Peak reverse current I_{RM} versus $-di_F/dt$

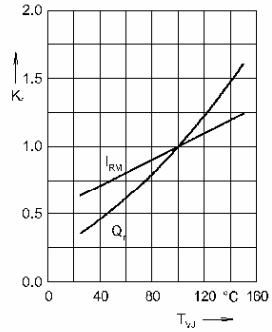

Fig. 4 Dynamic parameters Q_r, I_{RM} versus T_{VJ}

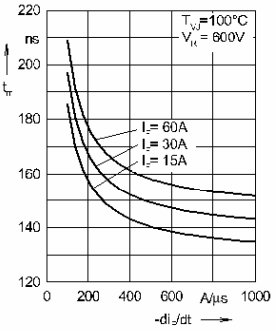

Fig. 5 Recovery time t_{rr} versus $-di_F/dt$

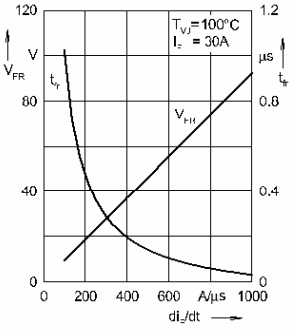

Fig. 6 Peak forward voltage V_{FR} and t_{fr} versus di_F/dt

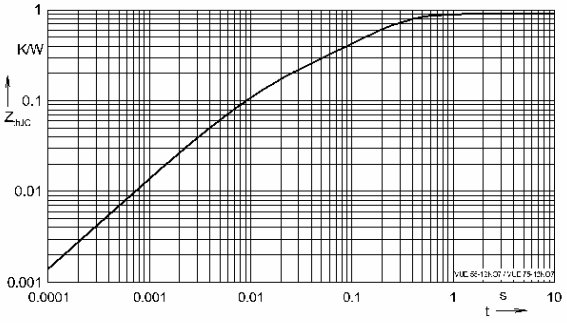

Fig. 7 Transient thermal resistance junction to case

Constants for Z_{thJC} calculation:

i	R_{thi} (K/W)	t_i (s)
1	0.3012	0.0052
2	0.116	0.0003
3	0.0241	0.0004
4	0.4586	0.0092

NOTE. Fig. 2 to Fig. 6 shows typical values

APPENDIX D. RAW EFFICIENCY DATA

Input Voltage (V)	Input Current (A)	Input Power (W)	Output Voltage (V)	Output Current (A)	Output Power (W)	Efficiency
121.2	7.50	903	121.2	6.74	817	90.4%
151.6	9.27	1396	151.3	8.41	1272	91.1%
182.3	10.95	1984	181.0	10.04	1817	91.6%
213.1	12.69	2688	211.2	11.69	2469	91.9%
240.3	14.60	3487	240.6	13.32	3205	91.9%

Input Voltage (V)	Input Current (A)	Input Power (W)	Output Voltage (V)	Output Current (A)	Output Power (W)	Efficiency
201.4	5.58	1121	201.8	5.05	1019	90.9%
200.5	6.74	1347	201.9	6.09	1230	91.3%
200.6	7.85	1569	201.9	7.11	1436	91.5%
202.3	8.71	1754	201.7	7.97	1608	91.6%
201.8	9.95	1998	200.5	9.14	1833	91.7%
201.7	11.04	2215	200.5	10.14	2033	91.8%
202.1	11.95	2401	200.4	11.00	2204	91.8%
202.2	13.16	2643	200.8	12.08	2426	91.8%
201.5	14.45	2891	200.6	13.21	2650	91.7%
203.7	15.17	3067	200.3	14.02	2808	91.6%

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