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DEVELOPMENT OF HIGH-TEMPERATURE, HIGH-POWER, HIGH-EFFICIENCY, HIGH-VOLTAGE CONVERTERS USING SILICON CARBIDE (SiC)

Delivery Order Delivery Order 0002: Critical Analysis of SiC VJFET Design and Performance Based Upon Material and Device Properties

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14. ABSTRACT

Silicon carbide as a semiconductor material possesses several significant physical properties which make it superior for applications to high power devices. This report documents the efforts to develop, demonstrate, and optimize the design and fabrication methodologies for the realization of power vertical junction field effect transistors in the 4H-polytype of silicon carbide. Theoretical prediction and modeling simulation, incorporating all the significant SiC specific device physics, are utilized to develop a design methodology which is to ultimately be used for device fabrication. The results illustrate that good agreement between theoretical prediction and accurately modeled simulations can be achieved and enable the forecasting of device performance as a function of temperature, design modification, and variations in material transport characteristics.

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EXECUTIVE SUMMARY

Contract F33615-01-D-2103 was awarded on 19 April 2001 as an Indefinite Delivery, Indefinite Quantity (IDIQ) contract with a ceiling of $13,553,119 and an anticipated expiration date of 31 October 2004 or as extended. Multiple delivery orders were expected to be awarded under the contract. Delivery Order no. 2, the subject of this final report, was awarded on September 24, 2001 and eventually funded to April 30, 2003 with amendments.

The effort funded by this contract encompassed two principal objectives:

1. The continuation of a project funded by Contract F33615-00-C-2030, which created a silicon carbide semiconductor device prototyping capability at Mississippi State University known as the Mississippi Center for Advanced Semiconductor Prototyping (MCASP).
2. The extension of the earlier work, which demonstrated a power Schottky barrier diode (SBD) prototyped in pre-production lot size (i.e., many more parts than is typical of research), to a unipolar silicon carbide semiconductor power switch, the Vertical Junction Field Effect Transistor (VJFET).
3. The continued involvement by a direct commercialization partner, namely SemiSouth Laboratories, Inc., in the development of a realistic path to system insertion for the technology funded by this contract and its predecessor (F33615-00-C-2030), via a public/private partnership involving technology licensing and subcontracting.

The two larger objectives, the development of a viable power semiconductor switch and the creation of a realistic commercial path to DoD system integrators (the large defense prime contractors) cannot be accomplished in one delivery order. This Delivery Order no. 2 final report examines another aspect of the project, namely, the design of a viable power vertical junction field effect transistor. A design based on a self-aligned, gate-implanted, trenched source-gate junction FET was selected for its near term technological readiness and it long term manufacturability. Delivery Order no. 2 concentrated on several key aspects:

- Optimized design of the fundamental static induction transistor that is the heart of the power VJFET. This includes critical dimensions of the gate and the channel fingers.
- Optimized design of an appropriate edge termination suitable for scaling the gate-drain diode of the VJFET, where the drain potential is blocked, to high voltages in excess of 1.2 kV.

This final report will focus on the design of the critical static induction transistor. An appendix has been added that documents the edge termination design optimization effort in the form of a paper published at the International Conference on Silicon Carbide and Related Materials (ICSCRM) held in Lyon, France in 2003. However, that paper documents the first investigation. Continuing investigation in later delivery orders has led to further understanding of the issues, including a need to improve the edge termination and passivation approach applied to the power trench VJFET. It is now recognized that an integrated approach using features of the gate-drain pn diode lead to the best results, which will be documented in later reports.

The follow-on delivery orders (3-5) will report the performance of a critical transistor component (ohmic contacts – Delivery Order no. 3) and the performance of the numbered VJFET developmental lots (Delivery Order nos. 4 and 5). A single final report will be issued covering both of the later delivery orders. Delivery order 6 concludes the contract, and will summarize the final results of device development, applications development, and the initial reliability testing studies. A single report will be issued covering Delivery order 6, including the enhancement.

CHAPTER 1
INTRODUCTION

1. Background : Review

Silicon Carbide (SiC) as a semiconductor material is provided with several special properties. The primary research areas for SiC have been high power RF devices, high temperature electronics and radiation hard electronics (space electronics and nuclear reactor). This can be attributed to special material properties of SiC. The large bandgap of SiC (3.2*eV* for 4H polytype) and high electron field strength (3.0 *MV/cm*) allows for high voltage applications and reduces series resistance in the lightly-doped drift region. The high saturated drift velocity of SiC is also advantageous in the development of high speed devices such as high frequency amplifiers [1]. Table 1-1 shows a comparison of material parameters for various semiconductors.

SiC's Static Induction Transistor (SIT) is well-suited for high power and high frequency (71 kW demonstrated at UHF). The leading parameters for design are developed through careful modeling by means of simulations and inclusion of all significant device physics, this thesis demonstrates that good agreement is reached between theoretical prediction and results of various simulations , such as temperature, saturation drift velocity, and contact resistance.

The SiC Static Induction Transistor is based on the original SIT concepts developed in 1950 [2] by Nishizawa, which have received continued development for the past 5 decades [3-5]. As compared to a Si Bipolar Junction Transistor (BJT), the SIT has advantages in being a majority carrier device, voltage-controlled, and often higher breakdown voltage and input impedance. While most SIT development has occurred in Si, renewed interest in the use of SiC SIT's over the past 10 years has occurred because of SiC's ten-fold advantage (3 *MV/cm*) in critical field strength and nearly two-field advantage in saturated electron velocity $\left(1.6 \sim 2.2 \times 10^7 cm/s\right)$ [6-10]. Additionally, SiC has an extremely high thermal conductivity ($\theta_k = 3 \quad W/cm \cdot k$) which far surpasses that of Si and GaAs, and allows an increased junction operating temperature $\left(T_j\right)$to nearly $400°C$ because of the high θ_k and dramatically reduced pn junction leakage currents resulting from its wide ($E_g = 3.2\ eV$ for the 4H-SiC polytype) bandgap. By use of SiC, it is thus possible to increase the voltage (power) rating of high-frequency amplifiers, and also increase the power density by a factor of 4 to 10 in UHF to S-band transistors. Parasitic capacitances are reduced by shrinking the device area while maintaining the power level and higher input/output impedance of the devices often requires little or no impedance matching. Limitations, which have slowed commercial insertion of SiC devices to date, include wafer size (75 *mm* maximum diameter available in 2002), wafer cost, device/epitaxy processing, and wafer defects. Currently, solid state devices are available provide a total power of tens of watts at 1 *GHz*, such as the silicon based bipolar transistor, and a few watts at 10 *GHz*, like GaAs based MESFET. When higher power is needed, one needs to either combine the output power of multiple devices or use vacuum tubes, which are still uncontested at very high power levels, capable of up to a few hundred kilowatts at 5 *GHz* [11]. High total power for a single device means that a smaller number of devices are needed to build a high power amplifier. This should lead to higher reliability, easier circuit design and lower cost.

2. Properties of SiC

2.1 Crystal Structure

SiC exhibit a one-dimensional polymorphism called polytypism. An almost infinite number of SiC polytypes are possible, and approximately 200 polytypes have already been discovered. [12] SiC polytypes differentiated by the stacking sequence of each tetrahedrally bonded Si-C bilayer. With the exception of 2H and 3C, all of the polytypes form 1-D superlattice structure [13]. The polytypes are divided into three basic crystallographic categories; cubic (C), hexagonal (H), and rhombohedral (R). Cubic SiC has only one possible polytype, and is referred to as 3C-SiC or β-SiC. Each SiC bilayer can be oriented into only three possible positions with respect to the lattice while the tetrahedral bonding is maintained. If these three layers are arbitrarily denoted *A, B,* and *C*, and the stacking sequence is *ABC/ABC…* then the crystallographic structure is cubic zinc blende and referred to as 3C-SiC. It possesses the smallest bandgap (~2.4eV) [14], and one of the largest electron mobility of all the SiC polytypes, and has been grown on 6H-SiC substrate. If the stacking of the bilayers is *ABC/ABC…,* then referred to as 2H-SiC, stacking sequence with *ABC/ABCB…*and *ABCACB/ABCACB…*, is referred to as 4H-SiC and 6H-SiC. 4H-SiC consists of equal number of cubic and hexagonal bonds. 6H-SiC is composed of two-thirds cubic bonds and one-third hexagonal bonds.

These SiC polytypes have substantially different thermal, optical, and electrical properties due to their different crystal structure. The properties of the commonly used SiC polytypes, which are most important for device applications, are comparing with the similar properties of silicon and gallium arsenide in Table 1.1.

The properties of SiC, such as wide band gap, excellent thermal conductivity, high breakdown field, high saturation drift velocity, provide a great deal of attractiveness in high speed, high power devices working at elevated temperatures and radiation, such as high power switch and high power amplifier. Also, SiC's properties of high chemical stability and radiation tolerance have attraction for aviation, nuclear, and space applications.

Table 1.1 Properties of SiC polytypes

Property	Si	GaAs	4H-SiC	6H-SiC	3C-SiC
Band Gap(eV)	1.12	1.42	3.2	3	3.2
Breakdown Field (MV/cm)	0.6	0.6	3.0	3.0	3.0
Saturated Drift Velocity (cm/s)	10^7	10^7	$2.2\times10^{7‡}$	$1.9\times10^{7‡}$	2.5×10^7
Thermal Conductivity (w/cm °C)	1.5	0.5	4.9	4.9	5
Electron Mobility (cm^2/Vs)†	1100	6000	900	370	750
Hole Mobility (cm^2/Vs)†	420	320	115	90	40

†: at doped concentration of 10^{17} cm^{-3}
‡: [15]

2.2 Energy Band Structure

The energy band structure of SiC strongly depends on the polytypes. Both experimental and theoretical results show that the valence band maxima for all common polytypes are located at the center of the Brillouin zone (Γ point). For all polytypes but 2H-SiC the conduction band minimum of 4H-SiC is found to be at the M point of the Brillouin zone. The indirect gap varies with the polytype reaching values between $E_g = 2.3\ eV$ for 3C-SiC and $E_g = 3.2\ eV$ for 4H-SiC has the largest energy band gap among all common SiC polytypes.

The temperature dependent energy band gap is not known for 4H-SiC. Experiment results Ref. in [16] show that the temperature coefficients of energy band gap for 6H-SiC and 3C-SiC are $-3.3\times10^{-4}\ eV/K$ and $-5.8\times10^{-4}\ eV/K$, respectively, Since crystal structure of 4H-SiC is closer to 6H-SiC than to 3C-SiC, following the same approach as in Ref. [17] and using the temperature coefficient of the energy band gap of 4H-SiC, the following temperature dependent band gap of 4H-SiC is obtained

$$E_g = 3.19 - 3.3\times10^{-4}\left(T - 300K\right)\ eV \tag{1.1}$$

2.3 Intrinsic carrier concentration

In semiconductor 4H-SiC, effective densities of states in the conduction and valence bands can be expressed as

$$N_c = \left(\frac{4\pi m_c kt}{h^2}\right) \tag{1.2}$$

$$N_v = \left(\frac{4\pi m_v kt}{h^2}\right) \tag{1.3}$$

where *k* is the Boltzman constant. For 4H-SiC $m_c(300k) = 0.76m_{0,}\, m_v(300k) \approx 1.2m_0$ in room temperature. The intrinsic carrier concentration at thermal equilibrium is given by

$$n_i = \sqrt{N_c N_v}\,\exp\left(\frac{-E_g(T)}{2kT}\right) \tag{1.4}$$

The temperature dependent intrinsic carrier concentrations of 4H-SiC, Si, and GaAs are shown in Figure 1.1.

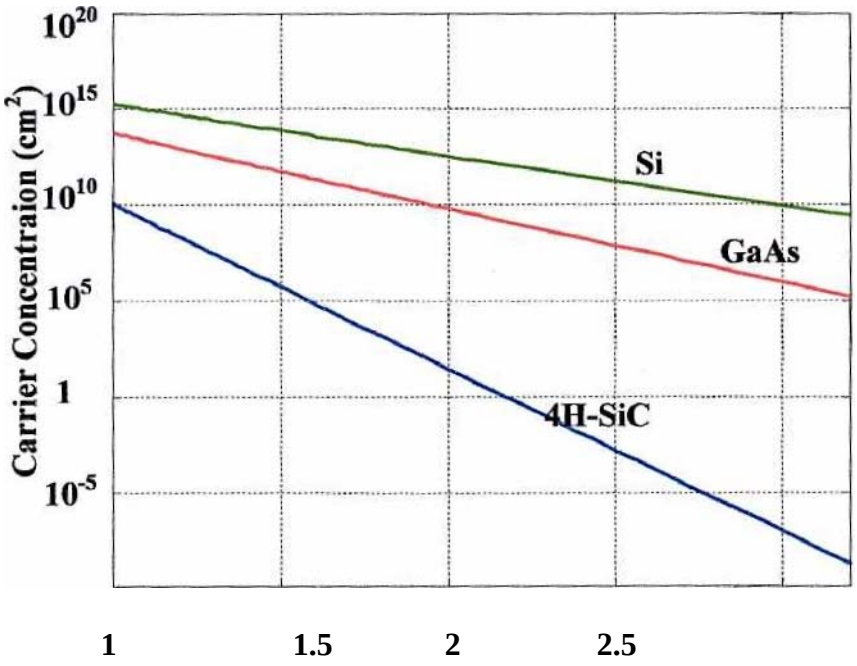

Figure 1.1 Intrinsic carrier concentrations *vs* temperature of 4H-SiC, Si and GaAs. (calculated from Eq. 1.4)

2.4 Low field mobility

The low field mobility model for 4H-SiC can be expressed as

$$\mu_{n,p} = \mu_{n,p}^{\min} + \frac{\mu_{n,p}^{delta}}{1+\left(\frac{N_D + N_A}{N_{n,p}^{\mu}}\right)^{\gamma_{n,p}}}\left(\frac{T}{300K}\right)^{\alpha_{n,p}} \tag{1.5}$$

where the electron set of data are $\mu_n^{\min} = 0\ \ cm^2/(V\sec)$, $\mu_n^{delta} = 947\ \ cm^2/(V\sec)$, $N_n^{\mu} = 1.94\times10^{17}\ cm^2/(V\sec)$, $\gamma_n = 0.61$ and $\alpha_n = -2.15$; the hole set of data are

$\mu_p^{\min} = 15.9\ cm^2/(V\sec)$, $\mu_n^{delta} = 108.1\ cm^2/(V\sec)$, $N_p^{\mu} = 1.76\times10^{19}\ cm^2/(V\sec)$, $\gamma_p = 0.34$ and $\alpha_p = -2.15$.

Note: this mobility model does not contain the effects of electron-hole scattering, which may be important in power devices and operating under high-injection conditions [17].

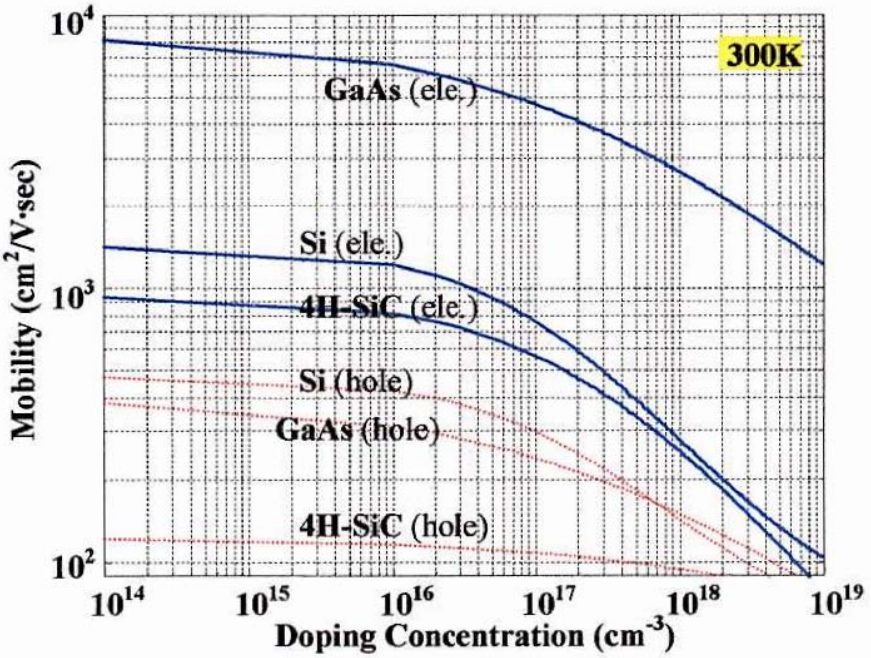

Figure 1.2 Low field electron and hole mobility of 4H-SiC, Si, and GaAs at room temperature

The low field mobility of 4H-SiC higher than those of 6H-SiC for both electrons and holes; the mobility of Si is higher than that of 4H-SiC, and that of GaAs is highest. Thus GaAs has tremendous advantage in high speed application field over both Si and 4H-SiC at low fields. The low field mobility of 4H-SiC, Si, and GaAs at room temperature increases, the lattice atoms vibrate more about their mean position, thus effectively increasing in "size" and thereby increasing the chance of collisions. The mobility therefore decreases with increase *T*. The theoretical dependence is $\mu \infty T^{\frac{-3}{2}}$ [18] and it's shown in Figure 1.3.

2.5 Thermal conductivity

The other important physical property of SiC is its high thermal conductivity. Typically, the thermal conductivity depends on polytypes and doping but the thermal conductivity of SiC exceeds that of copper $\left(4.01 W cm^{-1} K^{-1}\right)$, silver $\left(\left(4.29 W cm^{-1} K^{-1}\right)\right)$, Al_2O_3, and is about 5 times higher than that of Si. This is mainly due to the phonon dispersion relation distribution. Also, this property leads to a single design of heat dissipation of the device and the circuit even in high temperature and high power [19].

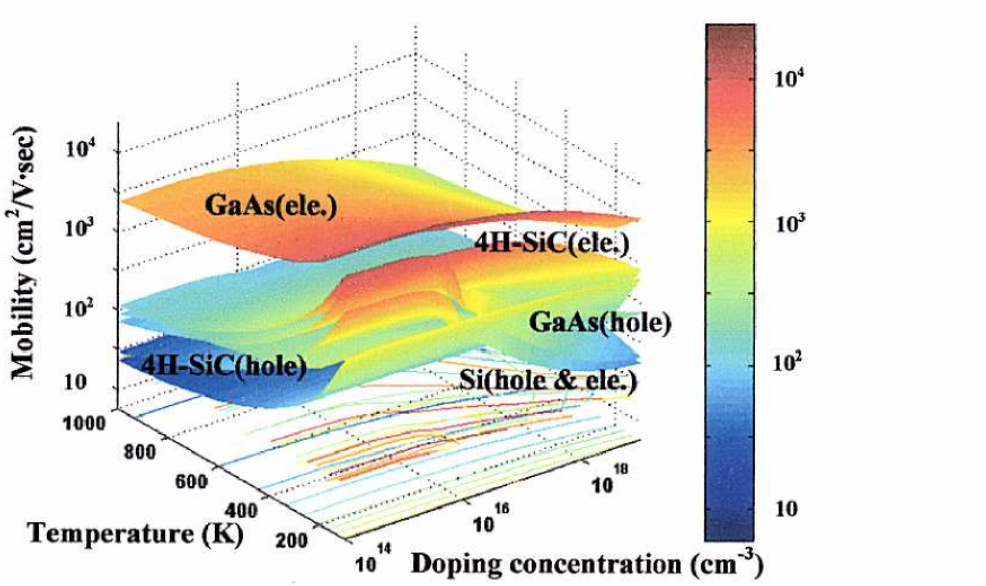

Figure 1.3 Mobility *vs* doping and temperature for electron and holes 4H-SiC, GaAS, Si.

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CHAPTER II
STATIC INDUCTION TRANSISTOR

1. Device Structure

Both recessed gate and planar gate SIT's have been fabricated in Si and SiC. However because of difficulty in deep ion implantation (p-type dopant Al implanted at energy of 380 *keV* has a peak range of only 0.42μ*m* into SiC) and the lack of diffusion at temperatures below 1800 °C, the recessed gate structure has been favored in SiC. Typical recessed gate SIT structures are shown in Fig. 2.1, with primary differences found in the gates. The gate may be a Recessed Gate - Bottom contact (RG-B), as shown in Fig. 2.1, or a RG with Sidewall and Bottom contact (RG-SF3), as shown in Fig. 2.2 which provides a longer gate length (L_g). Increasing L_g improves gate control, voltage gain (μ), and transconductance (g_m), while reducing the output resistance (r_{DS}). The gate material may be formed from either a Schottky metal or a pn junction, and can be thought of as analogous to a vertical dual-gate MESFET or JFET structure, respectively. The gate depletes the channel from each side a distance (x_d) into the channel. The total channel thickness ($2a$), trench width (t), and drift region length (L_{gd}) are illustrated in Fig. 2.1. Planar gates can also be fashioned in SiC [1], but the recessed gate with a Schottky barrier offers the lowest parasitics and most efficient gating [2]. A PN junction gate can be used with higher gate resistance (R_g), but offers less gate-to-source leakage at a higher maximum junction temperature $(T_{j\max})$ and potentially higher power density. The PN gate leakage at high temperatures in SiC devices is substantially reduced (proportional to the intrinsic carrier concentration of ni or ni^2) compared to Si or GaAs devices, and degradation of the Schottky contact is not limiting reliability if one uses a PN gate, as shown in Fig.2.3. PN gate adds some cost to processing since additional p-type implant and activation anneal are required.

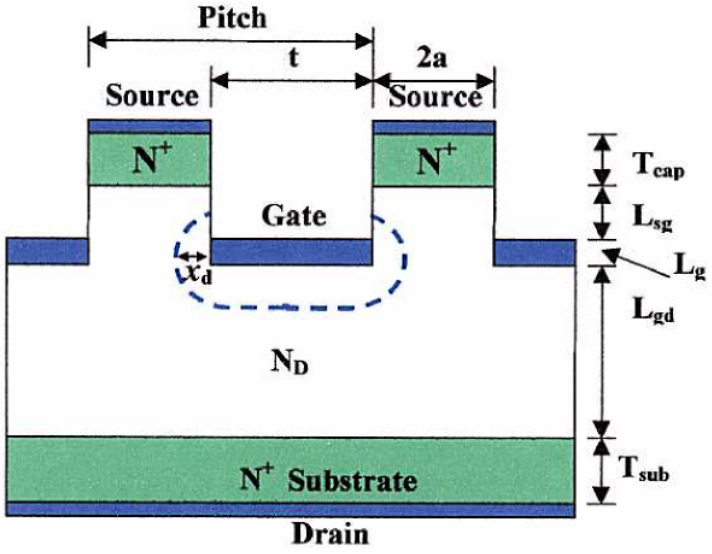

Figure 2.1 Structure of recessed gate static induction transistor.

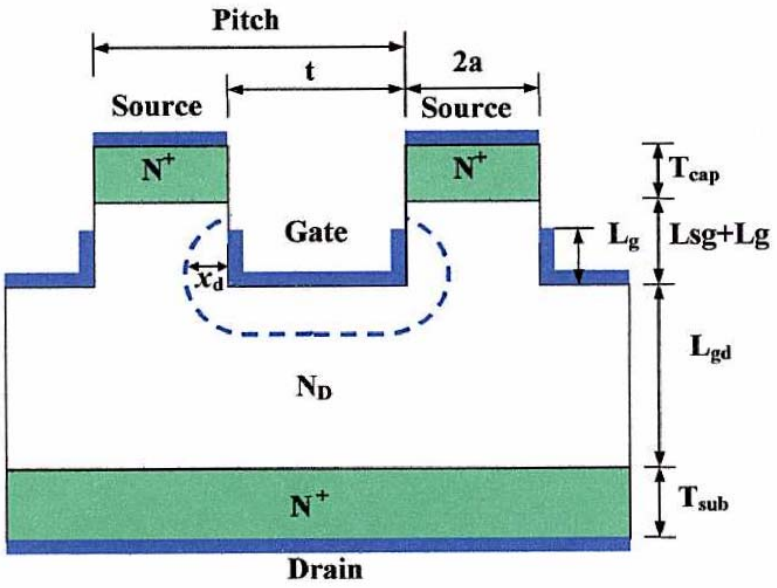

Figure 2.2 Structure of well-suited recessed gate static induction transistor

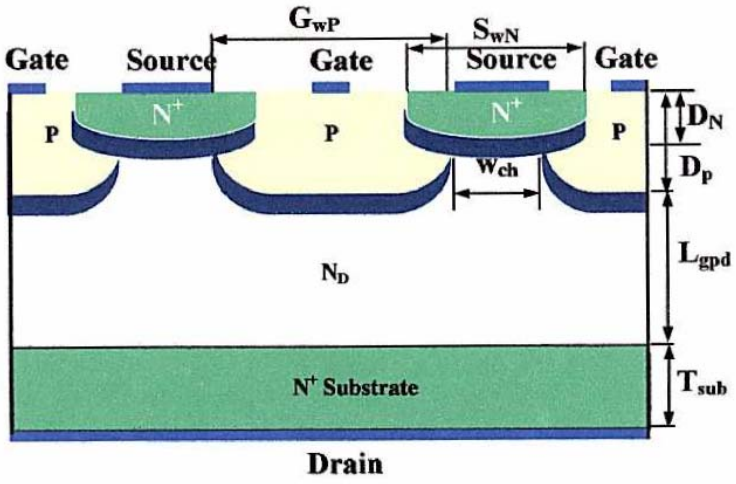

Figure 2.3 Structure of surface gate static induction transistor.

2. Operation

With $V_g = V_s = 0\,V$, the conventional SIT has its channel completely depleted $(x_d > a)$. If $x_d > a$, which often is done to increase maximum total current and power, then the SIT is referred to as mixed-mode [4]. Other terms for the SIT include gridstor, VFET (Vertical FET), or Permeable Base Transistor (PBT) [15]. PBT's often have extremely short gates $(L_g < a < x_d)$. The VFET nomenclature is generally reserved for devices with saturated drain-source output curves, unlike the triode characteristics of the SIT. The SIT name itself refers to the fact that the output characteristics are modified by static induction and not just the input

(gate) voltage, as is the case for conventional FET's in the saturation mode. There are three basic conduction mechanisms possible when the SIT is on, known as the ohmic, exponential, and Space Charge Limited Current (SCLC) regions, which are identified in Fig. 2.4 for a typical RG-SB SIT in SiC with a channel and drift region doped at $5\times10^{15}cm^{-3}$. (One may increase the channel doping to increase the total maximum current.) The transistor conduction mechanisms are two-dimensional, and a short basic description of the various regimes is given. Current flow is modified by gate, drain, and source potentials, through a saddle point minima between the gate electrodes, as shown in Fig. 2.5. where the minima is located at the mid-point of the channel.

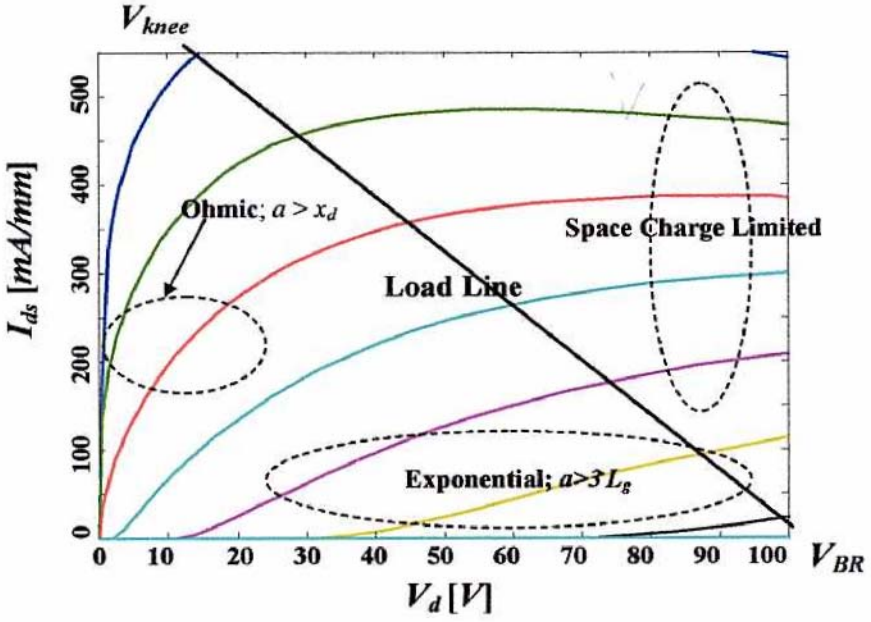

Figure 2.4 SIT's three regions of current flow.

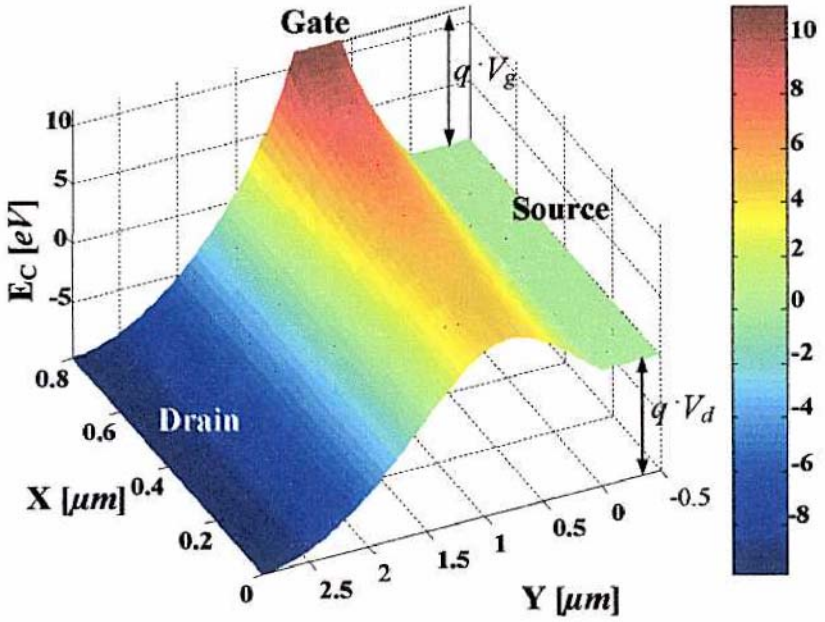

Figure 2.5 Conduction Band Energy of one half drift channel.

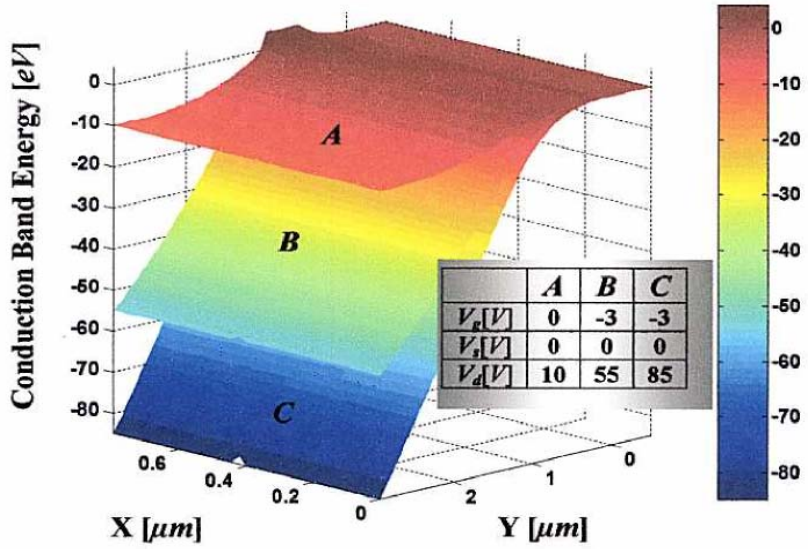

Figure 2.6 Conduction Band Energy in some bias.

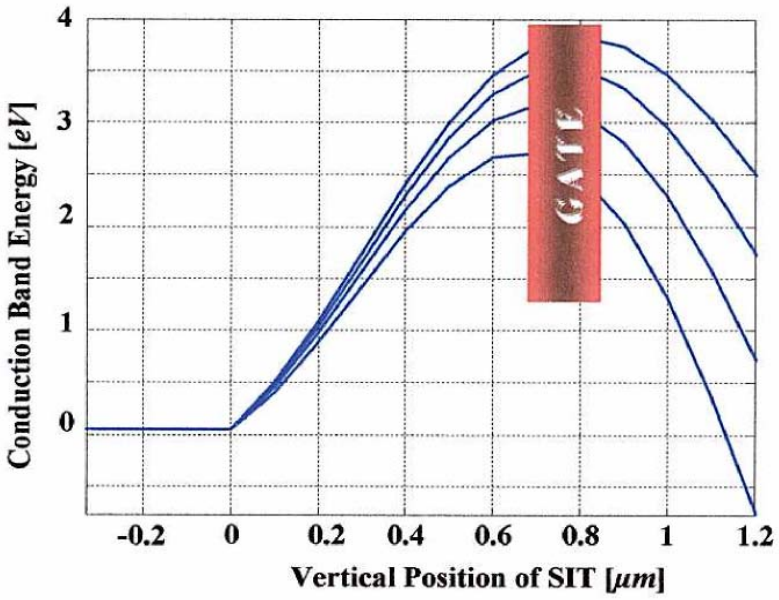

Figure 2.7 Conduction Band Energy in the center of channel (X=0) for different drain voltages.

2.1 Ohmic region

In the ohmic (linear) region, the channel is not completely pinched off by the depletion regions under fairly low gate and drain bias (see Fig. 2.5, Fig. 2.6, and Fig. 2.7). The current from drain-to-source (I_{ds}) is controlled by ohmic resistances found between the depletion regions under (beside) the gate, undepleted portions of the drift region, and the partially depleted portion of the channel immediately above the gate. The limiting portion is of course the region between gate depletion regions, which is often very narrow. Each channel is depleted from the gate on both sides by x_d which is given by *Eqn. (2.1)*, where $\varepsilon_s = 10.0$ for

SiC, $\varepsilon_0 = 8.854 \times 10^{-14}\ F/cm^2$ and N_D is the channel doping. V_{bi} and V_g represent the built-in potential and gate voltage, respectively. ε

$$x_d = \sqrt{\frac{2\varepsilon_s \varepsilon_0 (V_{bi} - V_g)}{qN_D}}$$

where: $V_{bi} = \phi_B - \frac{1}{q}\left[\frac{E_g}{2} - kT\ln\left(\frac{N_d}{n_i}\right)\right]$

The quantity ϕ_B is the Schottky barrier height (typically 1.1 *eV* for Ni on SiC) at the metal-SiC junction. The current density in this region can be given by $J_D = q \cdot v n_D \cdot N_D$, and the area is simply $A=2.A_{eff}$. Z per finger. The quantities A_{eff} and Z are the undepleted channel width and channel depth, respectively. In this low-field region, the current is not limited by v_{sat}, but rather proportional to the effective open area, channel doping, and low-field electron velocity (v_{nD}). For this reason, the 4H polytype of SiC is the commercially-available preferred polytype because it has the highest electron mobility.

2.2 Exponential region

In the exponential region, even though the channel is depleted with a low gate bias, a high drain bias influences conduction over the potential barrier in the channel from drain to source. The potential barrier in the channel (as shown in Fig. 2.5 and 2.6 for half of a 1.2 μ*m* channel thickness) between the two gate electrodes has barrier lowering in the mid-point region exponentially dependent upon the high drain bias. Since the exponential relationship exists, the current in this region can be described below in *Eqn. (2.2)* as exponentially dependent upon the amount of barrier lowering in the channel (ΔΦ), which is a function of the drain and gate bias [6].

$$I = I_0 e^{\frac{q\Delta\Phi}{kT}} \qquad (2.2)$$

where q is the electron charge, k is Boltzman's constant, T is the absolute temperature, and I^0 is a constant that depends on the channel geometry.

2.3 Space Charge Limited Conduction region

When the current density becomes high, a large drain voltage induces a large number of carriers into the gated and drift region. Also, when the carrier concentration becomes higher than the doping, the current becomes space charge limited. One can modify the treatment by Mott and Gurney [7,8] and arrive at

$$J_D = 2\varepsilon_s \varepsilon_0 v_{SAT} \frac{V}{L^2} \qquad (2.3)$$

where, *V* is the voltage drop from the contact (drain terminal) to the saddle point minima and *L* is the distance from the drain to the saddle point minima ($\approx L_{sg} + L_g + L_{gd}$). v_{SAT} *is* the saturated electron drift velocity. *Eqn. (2.3)* can be expressed in terms of total current [2] as shown in *Eqn. (2.4).* Note that total current for similar voltage and frequency rated Si and SiC devices will be quite different as L_{gd} would be an order of magnitude thinner and v_{SAT} would be 1.5 to 2X higher in the case of SiC. However, in using these equations, there is

an intrinsic assumption made regarding the SIT operation, which is explicitly that the electric field remains high enough ($\square 1\times 10^5\ V/cm$ in SiC) throughout the device, so that the electron velocity remains in saturation. While this is a simplifying assumption, which makes analysis easier, it can easily be violated, and can have significant impact on device operation (see discussion regarding temperature limits below for example).

$$I_d = 2\varepsilon_s \varepsilon_0 v_{sat} \frac{V_d}{\left(L_{sg} + L_g + L_{gd}\right)^2} A_{eff} \tag{2.4}$$

3. Limitations for Design

3.1 Thermal Limit on Total Power

Most power devices have a heat sink that is usually attached to the backside of the wafer. The generated heat must be transferred to it. Assuming a 45° spreading angle, the associated thermal resistance can be computed by

$$R_{TH} = \frac{1}{\sigma_{TH}\left|W - Z\right|}\left|\ln\frac{\left(T_{sub} + W\right)Z\right)}{\left(T_{sub} + Z\right)W\right)}\right| \tag{2.5}$$

where, W and Z are width and depth of device. and, for a given power density per area P" we find the rise in device temperature ΔT for steady state conditions.

$$\Delta T = R_{TH} P'' \tag{2.6}$$

The thermal resistance R_{TH} has a sizable spreading part that scales sublinearly with an increase of the device area, $A=WZ$ This means an increase in internal device temperature for larger area devices and a give temperature of the heat sink. Typically, the pitch between adjacent mesas, $t+2a$, affects the thermal resistance as well as the thermal power density generated on the top side of the wafer. A larger pitch makes it easier to dissipate the heat from the device. Additionally possibilities to improve the heat dissipation are a reduction of the generated thermal power by a high efficiency, and reducing the thermal resistance by thinning the substrate. However, a thinner substrate may in practice not improve the heat dissipation much because the thermal conductivity of the SiC substrate is comparable to the thermal conductivity of the metals that one would use for a heat sink attached to the backside of the wafer.

3.2 Impedance and Area Limit on Total Power

The output and input impedances can use in a microwave system have a lower limit that is fixed by circuit considerations and rarely be influence by the device designer. The impedance at the input and output of a device decreases with increasing device periphery, thus impedance imposes a limit on the total device size. The input impedance of a typical SIT is mainly capacitive. For example, the input capacitance with the output shorted is C_{in}^{S}, the input impedance with output connected to load is C_{in}^{L}. For all cases of interest C_{in}^{S} is larger than C_{in}^{L} due to the Miller effect [9]. In Power microwave, the loaded input capacitance; C_{in}^{L} must be small enough so that the desired bandwidth can be achieved. The input impedance of the device is realized by synthesizing a transmission line such that the input capacitance of each transistor stage is absorbed into the line impedance. This transmission line will have a cut-off frequency given by [10]

$$\omega_c = \frac{2}{\sqrt{C_{in}^L L_{in}}} \tag{2.7}$$

and,

$$Z_{in} = \sqrt{\frac{L_{in}}{C_{in}^L}} \tag{2.8}$$

Eqn. (2.7) and Eqn. (2.8) lead to the frequency limit for the amplifier given by

$$f_c \left\langle \frac{1}{\pi Z_{in} C_{in}^L} \right. \tag{2.9}$$

The load line is given in Fig. 2.4 between $V_{BR}(I_{ds}=0)$ to $I_{\max}(V_{ds}=V_{knee})$, where V_{BR} is the static breakdown voltage between drain and source. $I_{\max}$ is the maximum total current in the ohmic region at $V_8 = 0$ before conduction begins to be affected by SCLC and series resistance denoted at $V_{ds} = V_{knee}$. The very high V_{BR} of SiC SIT's (up to 450 V for S-band parts has been demonstrated) allows the theoretical power density *(P_D)* described in *Eqn. (2.10)* to be much higher than in Si. Since P_D is proportional to V_{BR}^2, and SiC's V_{BR} is nominally 10X that of Si for similar-rated parts, this translates to a 100X higher theoretical power density advantage for SiC SIT's over Si. Achieving those advantages will also require exceptional packaging technology to be implemented for SiC parts.

$$P_D = \frac{1}{8} I_{\max}(V_{BR} - V_{knee}) = \frac{(V_{BR} - V_{knee})^2}{8R_L} \tag{2.10}$$

Using SiC provides another advantage in broadband amplifiers, which require minimum output impedance from the transistor. Since scaling the area up in a device decreases both input and output impedance, the area of the device can be constrained by this requirement. SiC's ability to operate at higher voltages can increase the total output power while still maintaining some required output impedance.

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CHAPTER III
STATIC CHRACTERISTICS

1. Device Physics

The static I-V characteristics of the basic SIT were computed with the three partial differential equations *(Eqn. (3-1), (3-2),* and (3-3)) self-consistently for the electrostatic potential Ψ and for the electron concentrations *n,* respectively. In the SIT, the electrical behavior is governed by Poisson's equation.

$$\nabla^2 \Psi = -\frac{q}{\varepsilon}\left(-n + N_D^+\right) \tag{3-1}$$

and Continuity equation for electrons.

$$\nabla \cdot \vec{J} = U_n \tag{3-2}$$

where ψ, ε, and *n* are the electrostatic potential, dielectric constant, and electron density, respectively. N_D^+, $\vec{J}$, U_n are the concentration of ionized donors, current density, and net rate of electron recombination. Since the SIT is a majority carrier device and SiC is large bandgap material, the effect of holes has been omitted in this analysis. The whole concentration will be smaller that the numerical limit of the simulation tools. Carrier transport is given by the drift diffusion equation

$$\overrightarrow{J} = q\mu_n \overrightarrow{E_n} n + qD_n \vec{\nabla} n \tag{3-3}$$

where μ_n, $\overrightarrow{E_n}$, and D_n are the electron mobility, the electric field, and electron diffusivities, respectively.

2. Voltage Gain and Maximum Current Physics

The voltage gain μ is a measure for the possible large signal gain. It changes considerably with drain voltage, but for the scope of this work μ is defined for a drain voltage of 100*V*. For practical devices the voltage gain should be at around 10, which would correspond to a device that required –10*V* on the gate terminal to keep the device off at 100*V* on the drain. A graphical interpretation of these parameters is shown in Fig. 3.1.

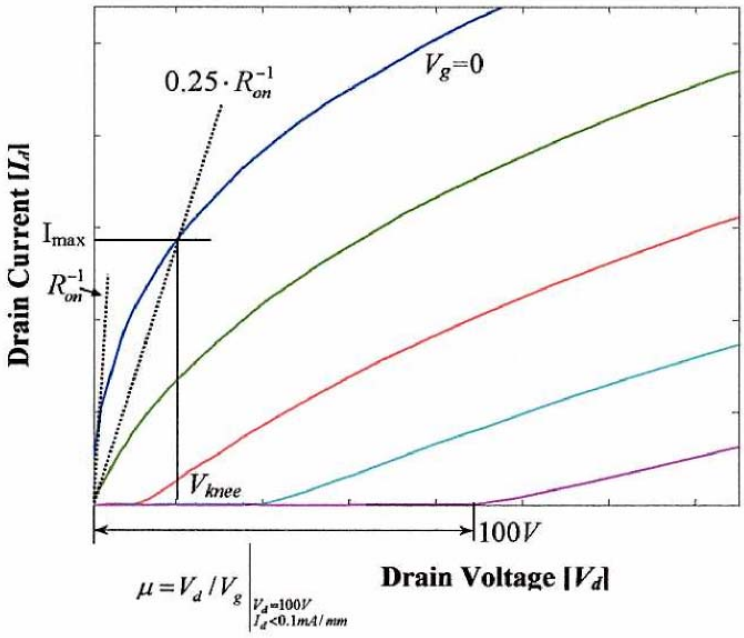

Figure 3.1 On resistance, voltage gain, maximum current and knee voltage.

The zero bias on-resistance, R_{on} is simply the initial slope of the drain current versus drain voltage curve for zero gate voltage

$$R_{on} = \left(\frac{\partial V_d}{\partial I_d} \right) \Bigg|_{\substack{v_{d=0} \\ v_{g=0}}} \tag{3-4}$$

In Eqn. (3-4), a small R_{on} is desirable for higher total current and smaller knee voltage. The definition illustrated in Fig. 3.1 places the point of maximum current where the straight line through the origin given by $I_{\max} = \frac{V_d}{4R_{on}}$ intersects with the drain current curve for $V_g = 0$. Since the SIT shows non-saturating I-V curves, $I_{\max}$ is not as obvious as for MESFET type device. Also, should mention that V_g can be up to +2.5V in wide bandgap (3.2 *eV)* SiC pn-gate SIT's without getting forward bias injection from the gate. But higher $I_{\max}$ will allow for a higher power density per unit width for a given breakdown voltage. The knee voltage V_{knee} is the drain voltage that corresponds to the point of maximum current. The knee voltage is important because it is the main factor that degrades the drain efficiency, which is given by [1]

$$\eta_D = \frac{P_{out}}{P_{DC}} = \frac{0.5}{1 + 2\left(\frac{V_{knee}}{I_{\max} R_L} \right)} \tag{3-6}$$

where P_{DC} is the DC power dissipated in the device, P_{out} is AC output power which is given by $P_{out} = \frac{R_L V_{\max}^2}{8(R_{on} + R_L)^2}$, and R_L is a load impedance. For class *A* operation, and reaches a maximum of 50% for the case V_{knee}=0.

3. Basic Dimension parameters for SIT Design

We have seen the SIT in Fig. 2.1 and Fig. 2.2, it is defined by four geometry parameters *(*$2a$, L_g, L_{sg}, and L_{gd}*)* and one doping parameter *(*N_D*).* Theoretically, the source gate distance L_{sg} should be as small as possible to minimize the source resistance. However L_{sg} is limited by the requirement that a low leakage path with sufficient breakdown voltage must exist between the gate and source. A nominal distance of L_{sg} = 0.5 μ*m* works well and this value was also adopted for all simulations. As a side note we mention that the voltage gain improves when L_{sg} increases for fixed L_g, because for increasing drain bias the saddle point tends to move toward and eventually reach the source, as was shown in Fig. 2.7. An increased L_{sg} allows the saddle point to move further behind the gate and increase the screening of the drain induced field by the gate, thereby increasing the blocking gain. The trench width (*t*) was fixed at one half of mesa width (2*a*), and except for a small change in spreading resistance of the drain drift region, it had relatively little effect on the static characteristic.

One of the most significant parameters for design is the doping value, N_D. In these simulations, we used four different values, $5 \cdot 10^{15} cm^{-3}$, $1 \cdot 10^{16} cm^{-3}$, $5 \cdot 10^{16}$ cm^{-3}, and $2 \cdot 10^{17} cm^{-3}$, spanning a range of nearly two orders of magnitude. Two lower doping values correspond to devices used by Northrop Grumman for their pioneering work [2] whereas the two higher doping values were used by Purdue University [3]. The gate-drain length (L_{gd}) needs to be tailored to each doping, and is determined by the two conflicting requirements of low drain resistance and a large breakdown voltage. In lower doping levels, the gate-drain length *(*L_{gd}*)* is limited by the requirements for *a* low drain resistance, due to the low doping and resulting in high bulk resistivity. On other hand, in high doping, the bulk resistivity is low enough that the gate-drain distance can be chosen to be comparable to the punch-through depletion depth for maximum drain voltage. We investigate the effect of varying two design parameters, gate length (L_g) and mesa width (2*a*) on the static I-V curve by keeping all other parameter constant. The computed static I-V curve for SIT with a doping value of $N_D = 5 \cdot 10^{15}$ cm^{-3} are shown Fig. 3.2 for five different gate lengths (0.05, 0.1, 0.2, 0.3, and 0.5 μ*m)* and five different mesa width (0.4, 0.5, 0.6, 0.7, and 0.8 μ*m)*. Other plots for different doping values can be found in appendix C. For the case of a large mesa width and very short gate, as shown in the lower left hand corner of Fig. 3.2, it is difficult to pinch off the drain current at high gate voltages, which corresponds to a low voltage gain μ. The other extreme case of a long gate length and a narrow mesa width, is the device characteristic in the upper right hand corner of Fig.3.2. This device is pinched off for all drain voltage with a relatively small gate voltage at the expense of having only a very small maximum current $I_{\max}$.

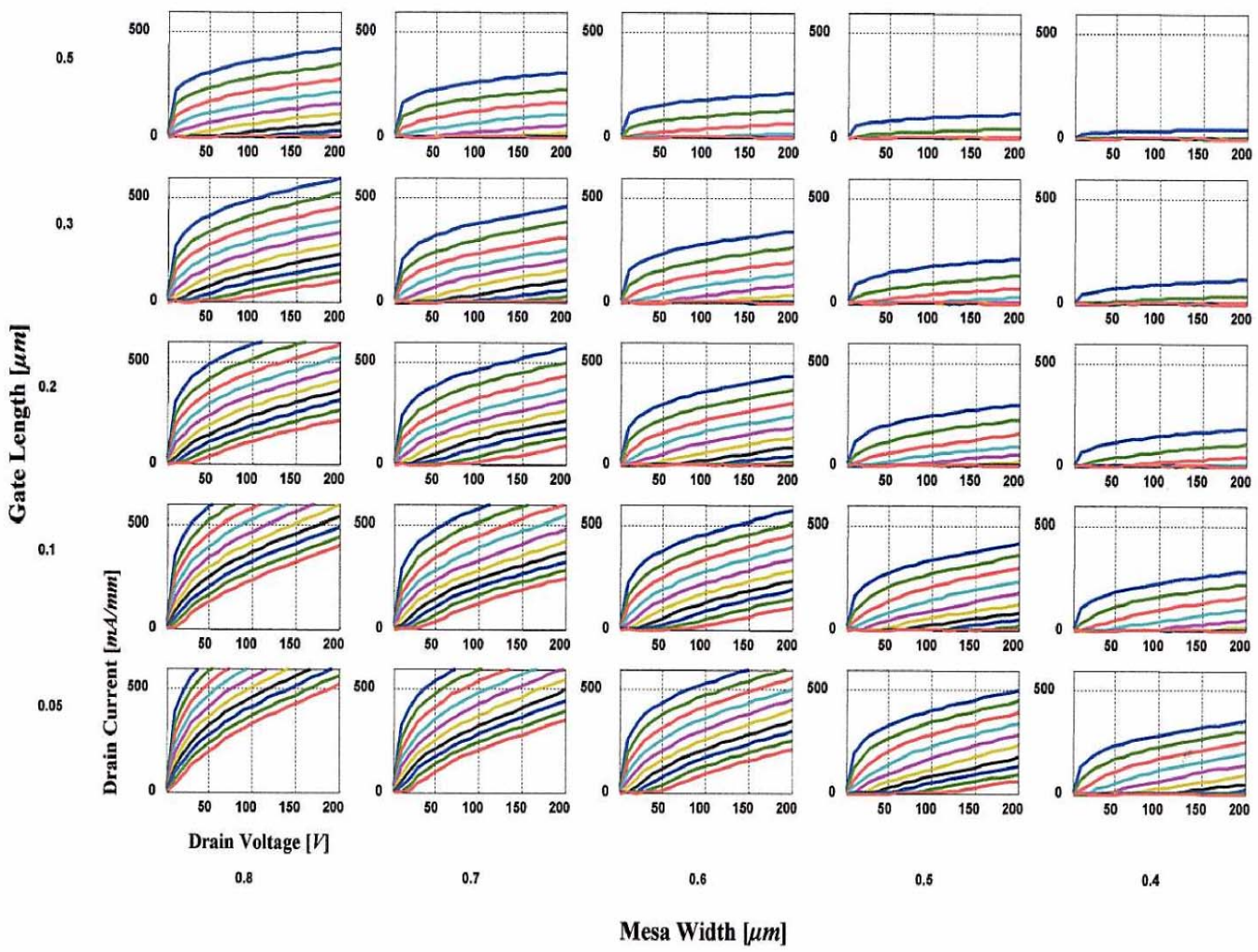

Figure 3.2. I-V curves for various gate length and mesa widths with $N_D = 5 \cdot 10^{15}\ cm^{-3}$, L_{sg}=0.5 μm and $t=2a$. Curve start at a gate voltage Vg=0 and progress in -2V steps.

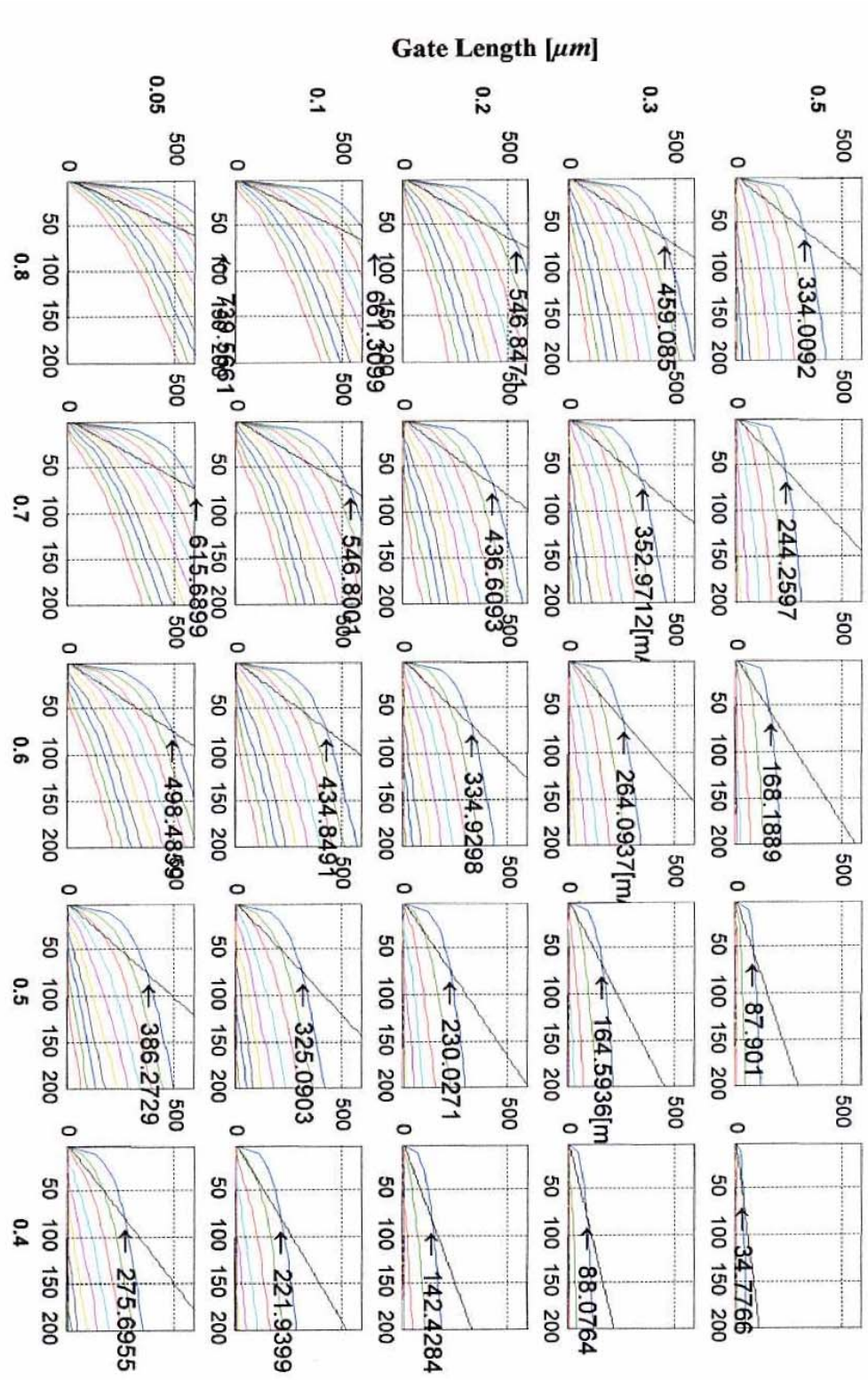

Figure 3.3 Maximum Current for various gate lengths and mesa widths on the IV curves.

Fig. 3.5 shows that maximum current, $I_{\max}$, depends on the gate length, L_g, *along* with mesa width *2a* as a parameter. In Fig. 3.5, the effect of an increased L_g is a reduction in $I_{\max}$, as a result of the increased channel resistance. The part of the channel between the gates that is partially depleted and which forms the bottleneck for current flow simply becomes longer. The increase of the channel resistance follows nearly linearly with L_g, and we can see an inverse

proportional effect on the maximum current. On other hand, maximum current is proportional to mesa width and it increases with mesa width in a nearly linear fashion, because the bottleneck between gate electrodes becomes narrower. The blocking gain, μ, is a stronger function of mesa width and gate length than the maximum current, unless the mesa width becomes very narrow, as shown Fig. 3.6. The physical reason is that the current changes linearly with channel dimension whereas the blocking gain to first order depends exponentially on the channel dimension [5], because of high voltages and low current in exponentially related to the saddle point potential. As a result, the blocking gain increases and the maximum current decreases, when the ratio between gate length and mesa width is increased.

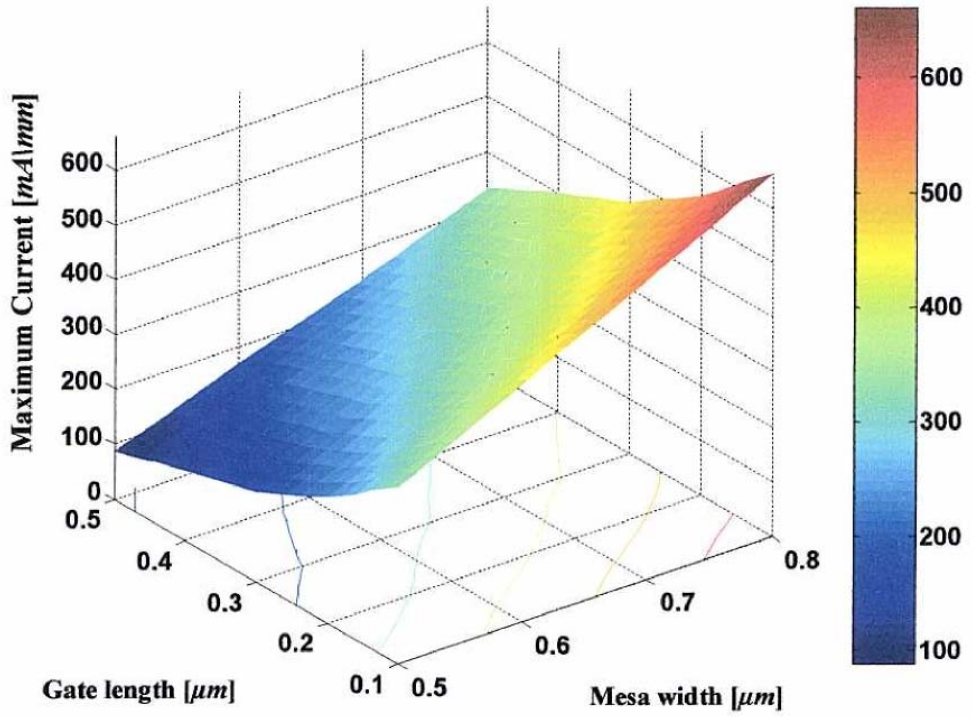

Figure 3.4 Maximum Current for various gate lengths and mesa widths.

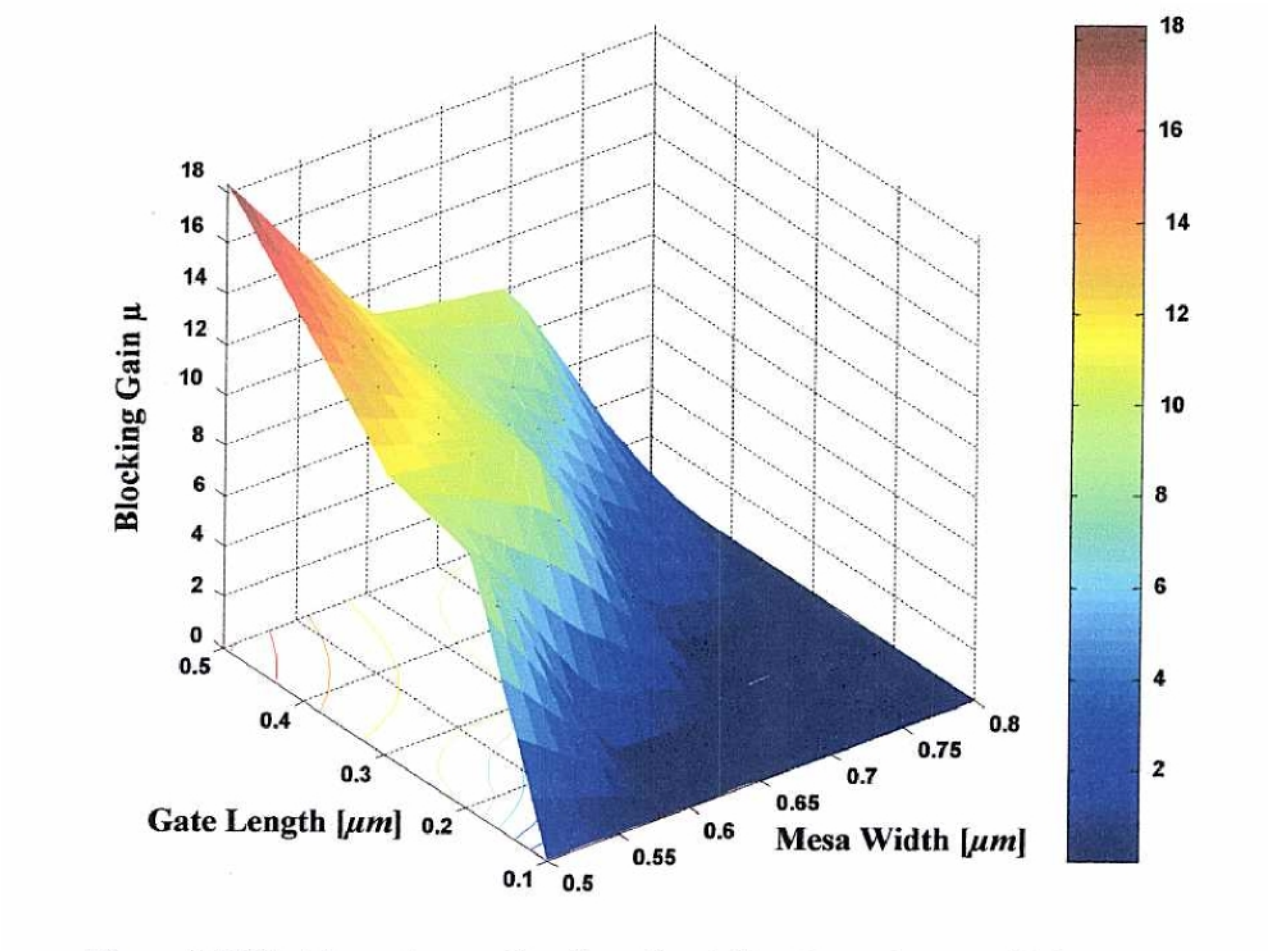

Figure 3.5 Blocking gain as a function of gate lengths and mesa widths.

4. Drain and Source Resistance

The parasitic resistances in the SIT are the resistance of the source (R_S), Drain (R_D) and the bulk resistance of the substrate (R_{sub}). The substrate resistance can only be meaningfully defined for a complete device, and by assuming current spreading angle of 45 degrees can be computed by

$$R_{sub} = \rho_{sub} \frac{1}{|W - Z|} \left| \ln \frac{(T_{sub} + W)Z}{(T_{sub} + Z)W} \right| \tag{3.7}$$

which is similar to the equation for the thermal resistance (see Eqn. (2.5)), expect that now the resistivity of the substrate, ρ_{sub}, appears. The resistance of the drain and source contact for a complete device can be estimated by

$$R_D = \frac{\rho_d}{(W + 2 \cdot T_{sub})(Z + 2 \cdot T_{sub})} \tag{3.8}$$

$$R_S = \frac{\rho_D}{2a \cdot W \cdot N_m} \tag{3.9}$$

Typical values are $T_{sub} = 300\mu m$, $\rho_{sub} = 15m\Omega \cdot cm$, and $\rho_{D,S} = 1 \cdot 10^{-5}\Omega \cdot cm^2$. When we assume a small area test device with 1 mm periphery with 20 fingers, Z=40 μm and W=50 μm, the substrate contribution would be $R_{sub} = 2.9\Omega \cdot mm$ by Eqn. (3.7), nearly order of magnitude smaller than the large area limit. Similarly, we find $R_D = 0.5\Omega \cdot mm$ and $R_S = 0.0024\Omega \cdot cm$ for the large area and small area device respectively. From this follows immediately that the resistance due to the drain contact can be neglected; this would still be true for even a poor contact of $\rho = 1 \cdot 10^{-4}\Omega \cdot cm^2$. The source resistance depends on the particular design because the area of the contact is determined by the mesa width.

5. Basic considerations of Power and frequency performance

In previous definition of maximum current $I_{\max}$, a large maximum current can be obtained for larger channel dimensions. Shown in Fig. 3.7 is the effect of varying gate length on frequency performance. It should be understood that f_T is a function of zero bias. The use of smaller dimensions allows for higher frequency performance, but comes at the expense of a slightly lower maximum current. Therefore, to maximize frequency performance, a short gate length should be selected.

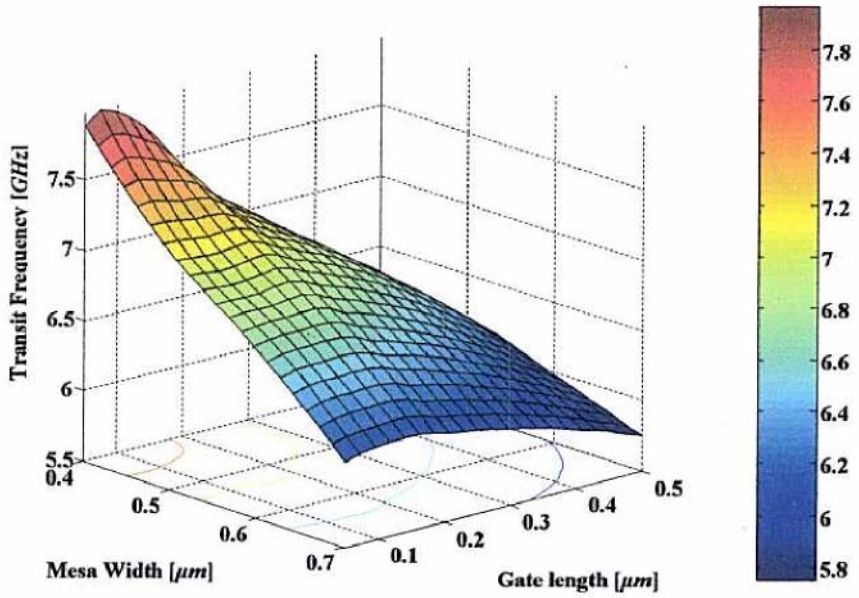

Figure 3.6 Frequency as function of gate lengths and mesa widths for fixed voltage gain 10 dB

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CHAPTER IV
HIGH FREQUENCY CHARATERISTICS

I. Small Signal Equivalent Circuit of SIT

The SIT is usually used as a small signal amplifier. Small signal analysis is as important as DC analysis for semiconductor device, especially for high frequency operation of the SIT. There are three types of techniques for small signal analysis of a semiconductor device [1]. The first technique is transient excitation followed by Fourier decomposition, second is incremental charge partitioning, and third is small-signal AC steady state frequency domain analysis. The small-signal AC steady state frequency domain analysis is a superior approach comparing to the other methods [1]. This technique is easy to be incorporated into a device simulator. In this chapter, the small-signal AC steady state frequency domain analysis technique is applied on the frequency performance of the SIT.

For an assessment of the frequency performance of the SIT, the small signals Y-parameters have been computed by MEDICI over the anticipated operation frequency range from 500 *MHz* to 10 *GHz*. The Y-parameters as a function of frequency, as obtained from MEDICI simulation, were fit to the pi-equivalent circuit shown in Fig. 4.1. The gate-drain capacitance is occasionally referred to as the feedback capacitance because it couples the output and input of the device. The model the frequency behavior of the input impedance the gate-source resistance R_{gs} is connected in series with C_{gs}. The gate-source resistance represents the resistance of the undepleted part of the mesa on the source side of the gate.

The magnitude of the transconductance, g_m, is equal to the DC transconductance. The transit time, τ, accounts for the delay due to the finite time that a carrier needs to travel from the source to the drain. The output conductance is denoted by G_{ds}. The procedure of finding the equivalent circuit elements from the simulated data is identical to determining these elements from a measured data set, with the exception that measured data are obscured by unwanted effects such as noise, imperfect calibration and unaccounted parasitics because the exact details of a physical structure are only known within certain limits, whereas the simulated structure is known precisely. At circuit level, input current I_i is equal to the magnitude of ideal output current $g_m \cdot V_{gs}$, of the intrinsic transistor. When the output is short-circuit [2],

$$I_i = jw\left(C_{gs} + C_{gd}\right)V_{gs} \tag{4-1}$$

if let $C_g = C_{gs} + C_{gd}$, then at the cutoff frequency

$$\left|I_i\right| = 2\pi f_T C_g V_{gs} = g_m V_{gs} \tag{4-2}$$

in Eqn. (4-2),

$$f_T = \frac{g_m}{2\pi C_g} \tag{4-3}$$

or,

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{4-4}$$

The four elements of the general pi-circuit, Y_i, Y_0, Y_r and Y_f, can be obtained easily from the Y-parameters [3] that one has available either from simulations or from measured S-parameters that were transformed to Y-parameters (see App. D).

$$Y_i = Y_{11} - Y_{12} \tag{4-5}$$

$$Y_o = Y_{22} - Y_{12} \tag{4-6}$$

$$Y_r = -Y_{12} \tag{4-7}$$

$$Y_f = Y_{21} - Y_{12} \tag{4-8}$$

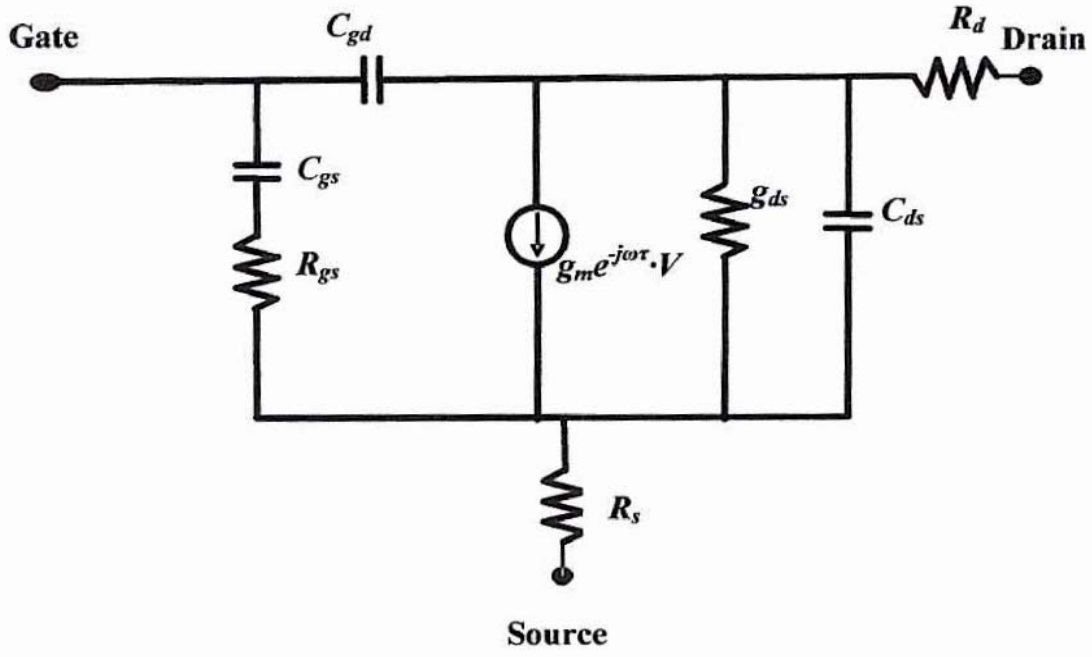

Figure 4.1 Pi-equivalent circuit for small signal modeling.

From these, the reactive components of the intrinsic device may be determined. MEDICI will be able to create the Y-parameters directly from the small signal simulation. Using circuit model for the SIT, the value of the components can be determined by the simulations. Applying the small signal simulations to the circuit models, from Eqn. (4-5) through (4-8) the Y-parameters are related by [3]:

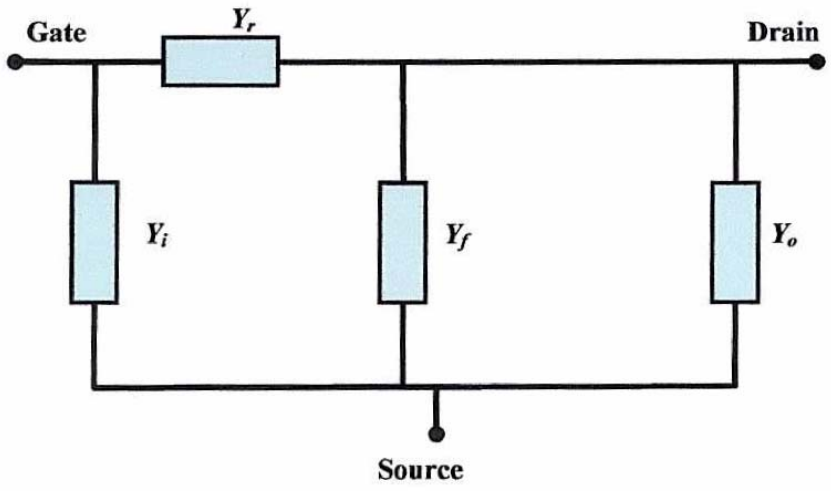

Figure 4.2 General Hybrid-Pi equivalent circuit.

$$Y_{11} = j\omega(C_{gs} + C_{gd}) \tag{4-9}$$

$$Y_{12} = -j\omega \cdot C_{gd} \tag{4-10}$$

$$Y_{21} = g_m \cdot e^{-jw\tau} - j\omega C_{gd} \tag{4-11}$$

$$Y_{22} = g_{ds} + j\omega(C_{ds} + Cgd) \tag{4-12}$$

The Y-parameters used for the following discussion are for a bias point with $V_d = 10V$ and $V_g = 0$. Plotting the magnitude of Y_f as a function of frequency, as shown in Fig. 4.3, we can obtain values for g_m, and τ. By Eqn. (4-11), (4-10), and (4-8), the magnitude of $|Y_f|$ is almost independent of frequency, and we obtain g_m by forming the average over the lower frequency part of the plot. The phase plot linearly decreases over frequency, and τ can be obtained from the slope of the line by fitting the plot using the equation $\Delta Y_f = 2\pi f\tau$. Also shown in Fig. 4.3 is the magnitude of Y_0 that Gate-Drain and Gate-Source Capacitance from which we obtain a value for g_{ds}. The feedback capacitance C_{gd} is obtained by averaging the data of a plot of $\Im(-Y_{12}/\omega)$over frequency by Eqn. (4-10), which should be independent of frequency. Here $\Im(-Y_{12}/\omega)$ means that the imaginary part is taken of $-Y_{12}/\omega$ expression in brackets. Similarly, C_{gs} is found by averaging $\Im((Y_{11}+Y_{12})/\omega)$over frequency by Eqn. (4-9), (4-10), as shown in Fig. 4.4.

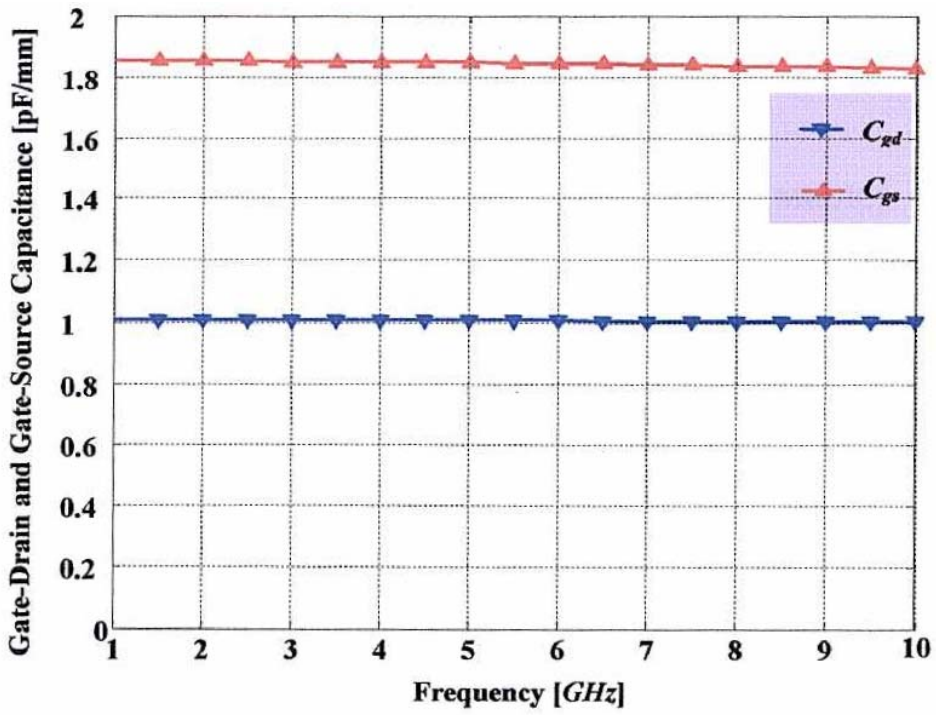

Figure 4.3 Magnitude of Y_f and Y_o as function of frequency at bias point $V_d = 10V$, $V_g = 0V$.

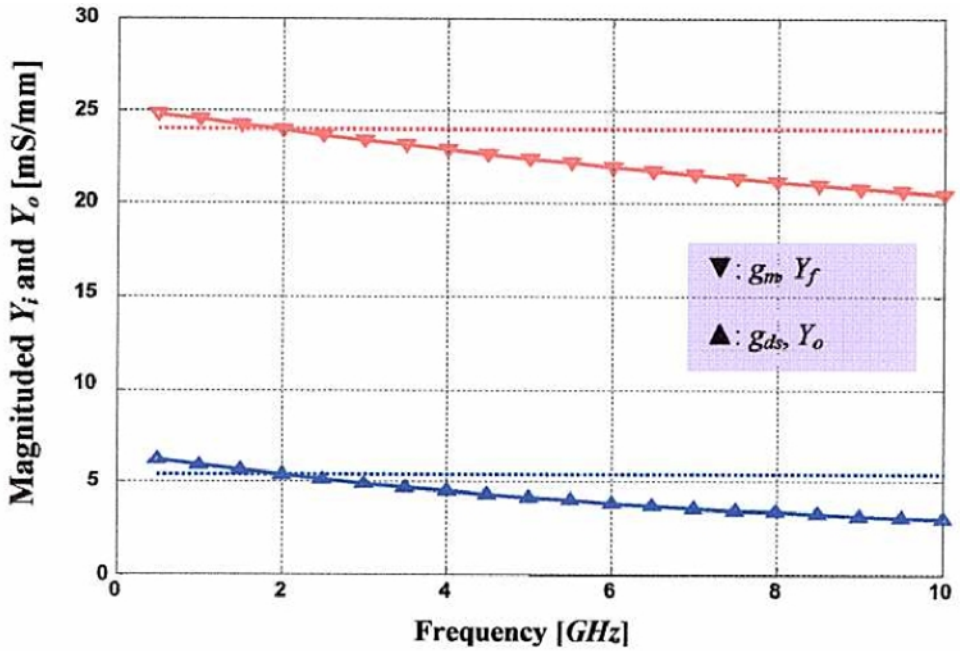

Figure 4.4 Gate-Drain and Gate-Source Capacitance as function of frequency for bias point $V_d = 10V$, $V_g = 0V$.

If one tried to find a value for C_{ds} by simulation from MEDICI, the resulting values seem randomly jump between positive and negative numbers with an absolute value that is at least an order of magnitude smaller than either of the values found for C_{gs} or C_{gd}. Therefore, let $C_{gd} = 0$. This is physically meaningful if one considers the vertical arrangement of the

device that essentially places the gate electrode as a grid between the drain and source electrode, electrostatically shielding the two from each other. This also agrees with the usual interpretation of the drain source capacitance in lateral devices, such as MESFET, where it is due to fringing effects between the source and drain electrode through the substrate under the active device [4]. There is no equivalence to the substrate fringing effect in a SIT due to the vertical channel, which is similar to two MESFET channel in a mirror image like arrangement.

2. Effect of contact Resistance

The contract resistivity of R_s and drain contact R_d can be described by lumped resistances that are in series with the source and drain terminal, respectively. A finite source resistance R_s affects the transconductance as well as the short circuit input capacitance. For the special case that R_d =0 we find for the transconductance [5]

$$g_{m,ext} \approx \frac{g_m}{1+g_m R_s} \qquad \text{when } R_d = 0 \tag{4-13}$$

and for the short circuit input capacitance

$$C_{in} \approx C_{gs}\frac{1}{1+g_m R_s} + C_{gd} \qquad \text{when } R_d = 0 \tag{4-14}$$

The drain resistance, Rd acts like a built in load resistance and therefore increase the input capacitance according to the Miller effect. When we assume in any special case that $R_s = 0$, the Miller effect can be theoretically expressed by the following approximation [5]

$$C_{in} \approx C_{gs} + C_{gd}\left(1+\frac{g_m}{g_{ds}+1/R_d}\right) \quad \text{assumed } R_s = 0 \tag{4-15}$$

In the general case, when both R_s and R_d are unequal to zero, the expression for the input capacitance becomes more complicated. However, we conclude that an increase in R_d and R_s leads to an overall degradation in frequency performance, namely the cut-off frequency, because the contribution of C_{gd} is significant for the SIT and tends not to decrease when a source resistance is introduced, Eqn. (4-14). Note that for a device with a very small feedback capacitance, the cut-off frequency does not change notably with increasing source resistance. Such as, MESFET and HEMT, where the overall contribution of C_{gd} to the total input capacitance is typically less than 10% [6]. The source resistance is also increases the total resistance of the device between source and drain, and therefore the maximum current reduced. The effect of the specific contact resistivity ρc is illustrated from Fig. 4.5 to Fig. 4.15.

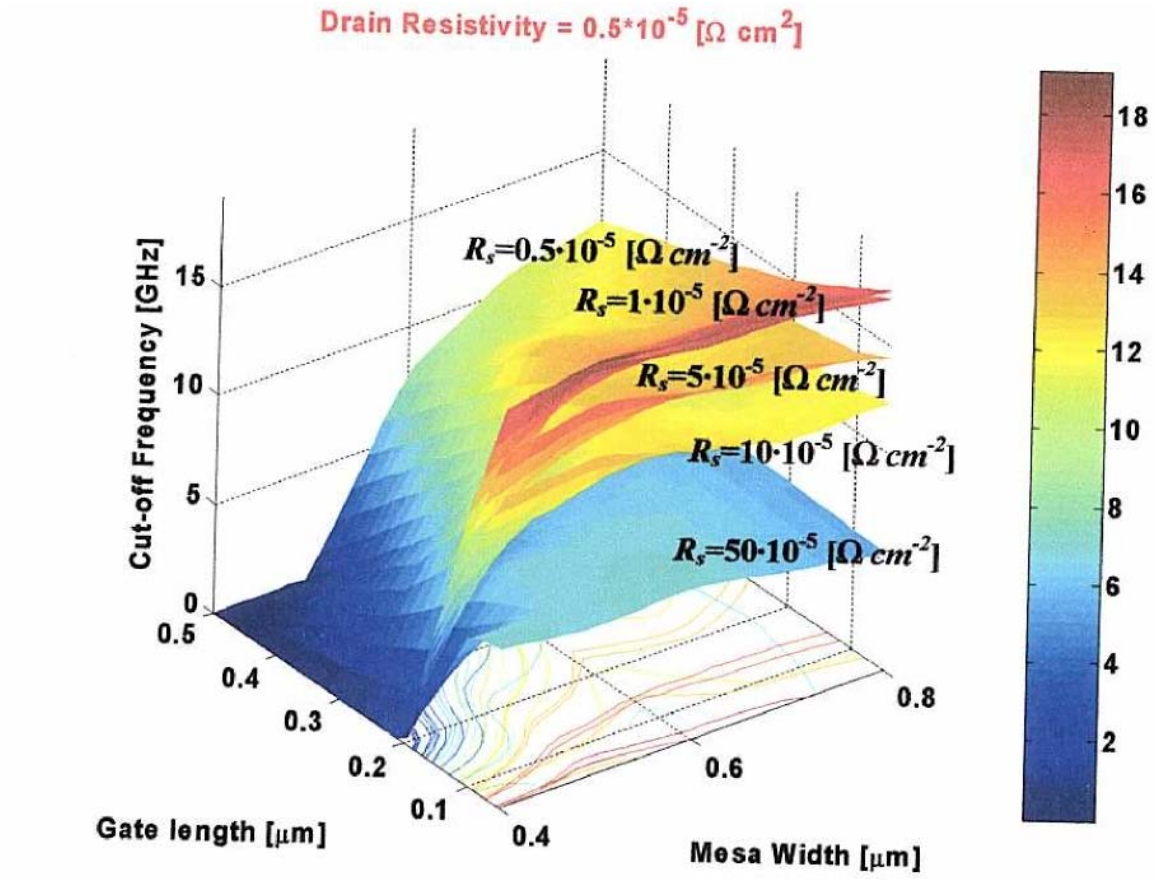

Figure 4.5 Cut-off Frequency as a function of gate length and mesa width with drain contact resistivity $0.5 \cdot 10^{-5}$ [Ω cm^2].

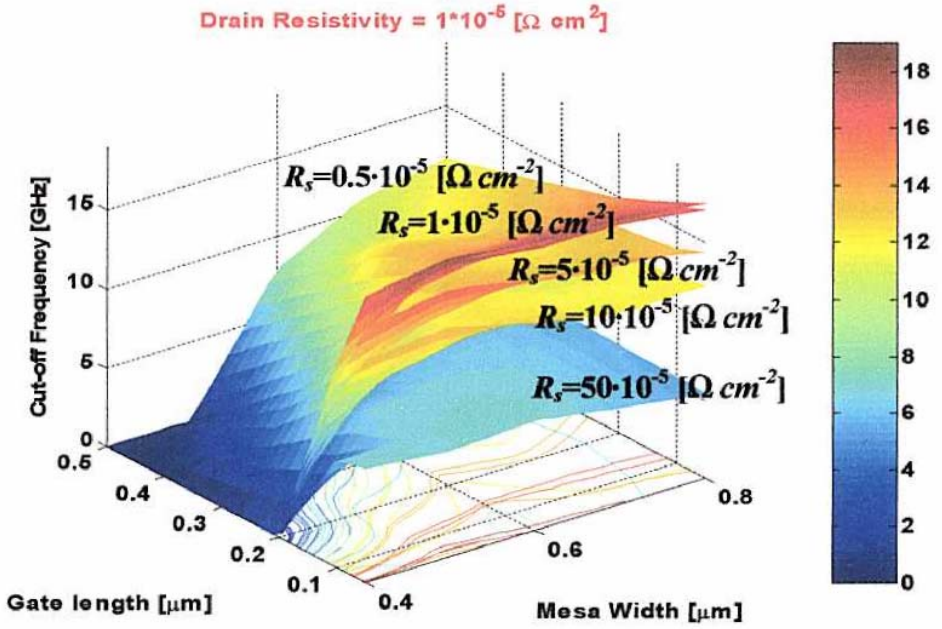

Figure 4.6 Cut-off Frequency as a function of gate length and mesa width with drain contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2].

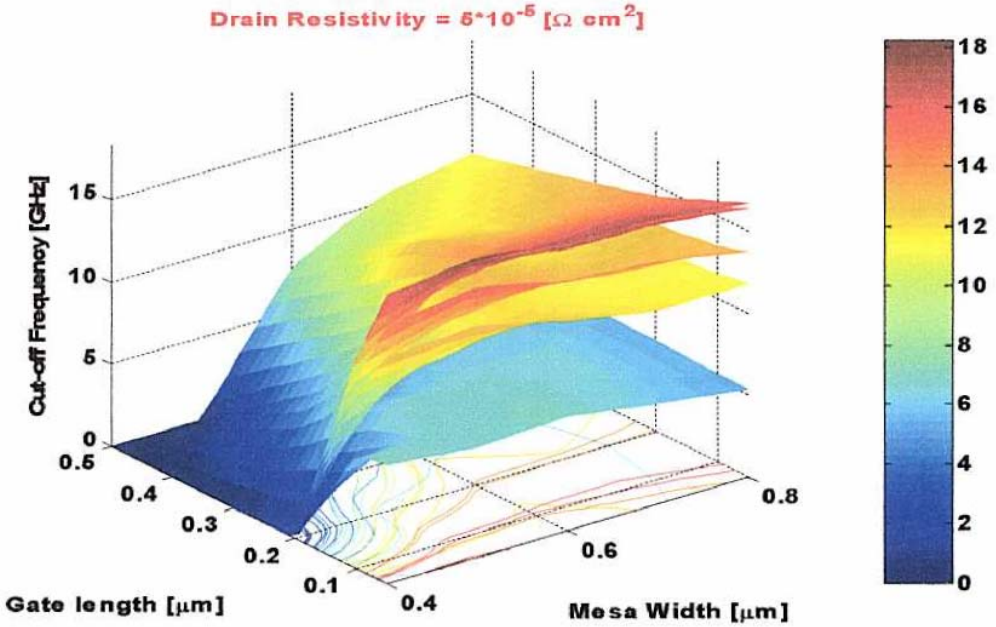

Figure 4.7 Cut-off Frequency as a function of gate length and mesa width with drain contact resistivity $5 \cdot 10^{-5}$ [Ω cm^2].

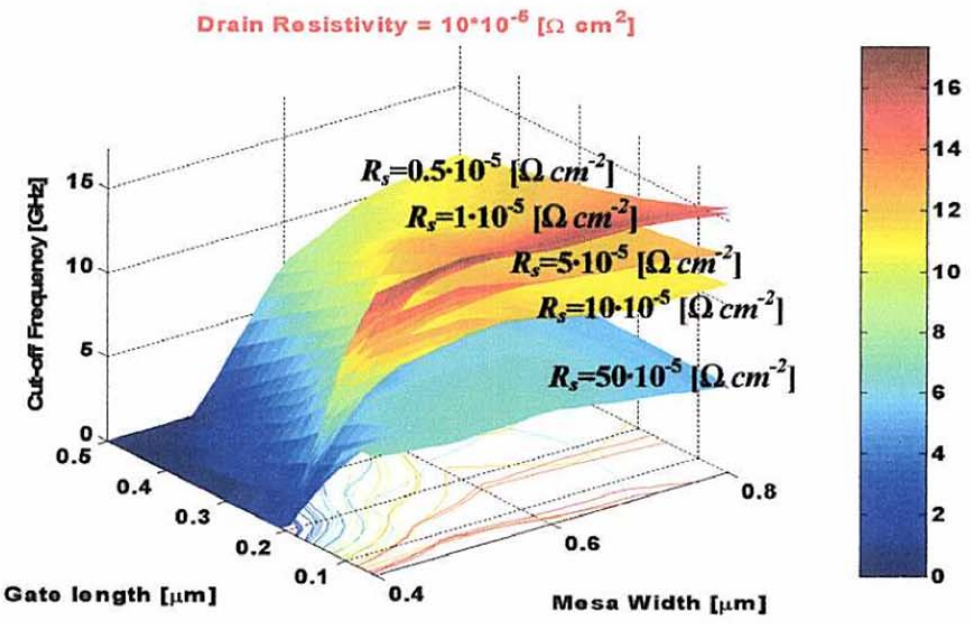

Figure 4.8 Cut-off Frequency as a function of gate length and mesa width with drain contact resistivity $10 \cdot 10^{-5}$ [Ω cm^2].

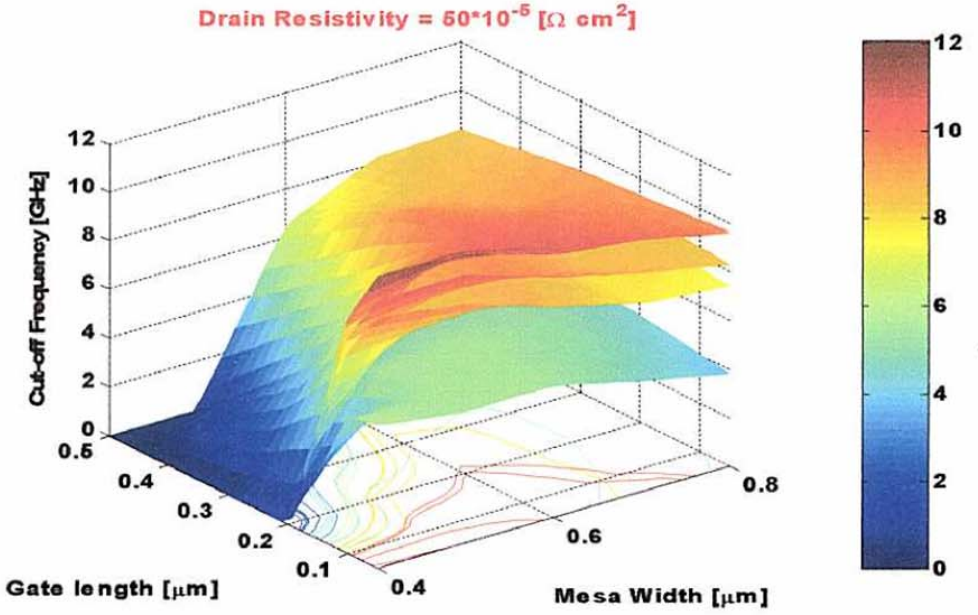

Figure 4.9 Cut-off Frequency as a function of gate length and mesa width with drain contact resistivity $50 \cdot 10^{-5}$ [Ω cm^2].

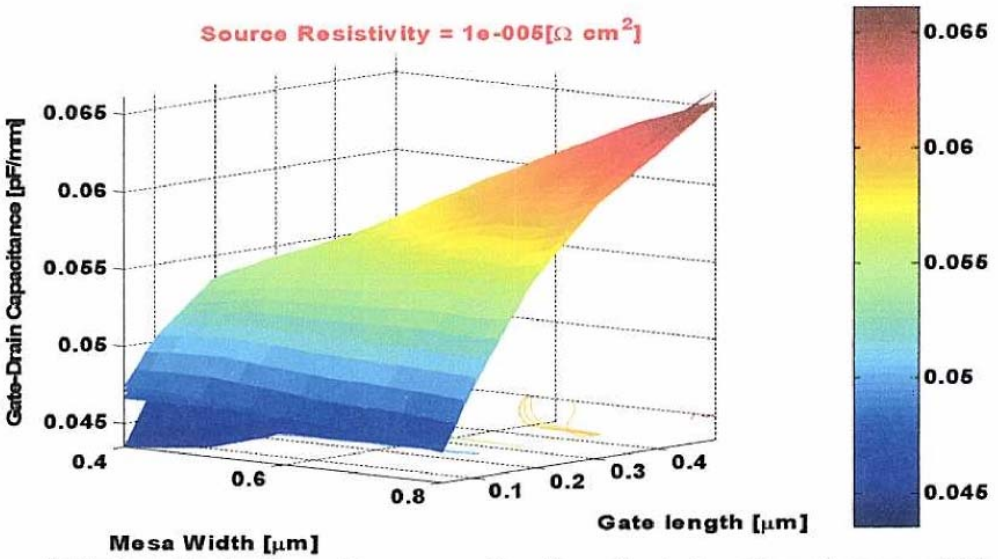

Figure 4.10 Gate-Drain Capacitance as a function of gate length and mesa width at source contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], from top drain contact resistivity $50 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $0.5 \cdot 10^{-5}$ [Ω cm^2], respectively.

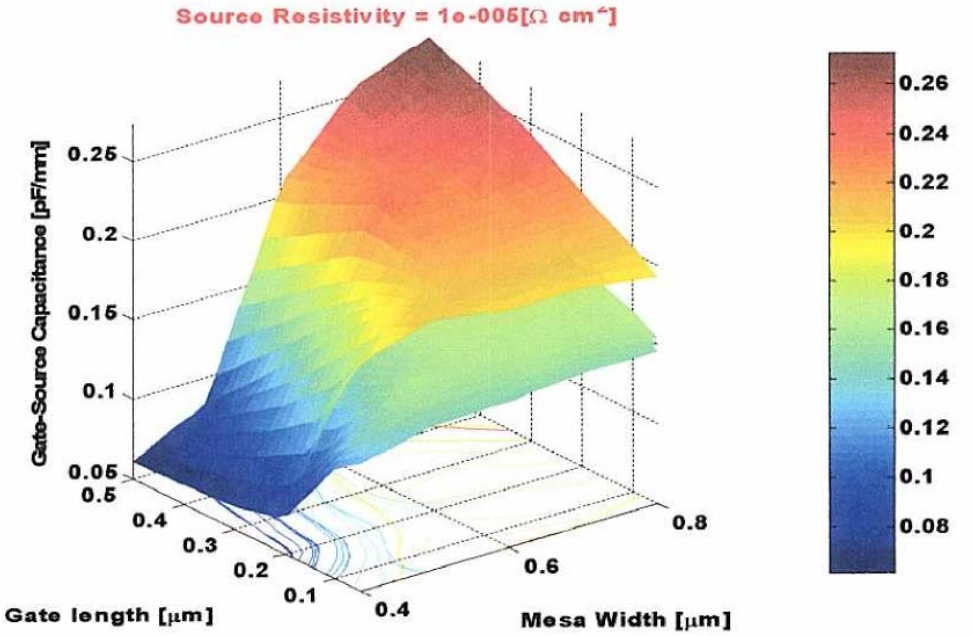

Figure 4.11 Gate-source Capacitance as a function of gate length and mesa width at source contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], from top drain contact resistivity $50 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $0.5 \cdot 10^{-5}$ [Ω cm^2], respectively.

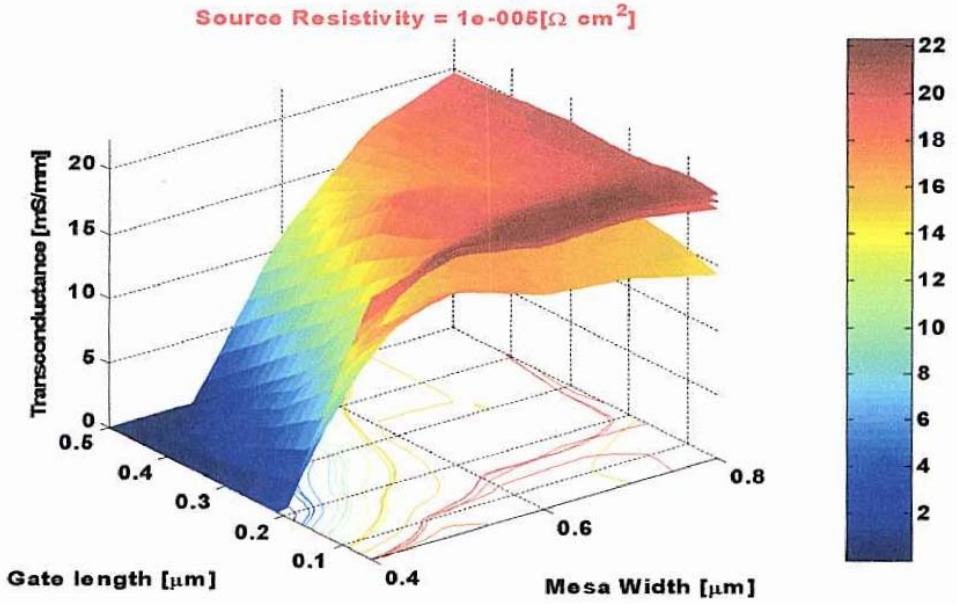

Figure 4.12 Transconductance as a function of gate length and mesa width at source contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], from top drain contact resistivity $0.5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $50 \cdot 10^{-5}$ [Ω cm^2], respectively.

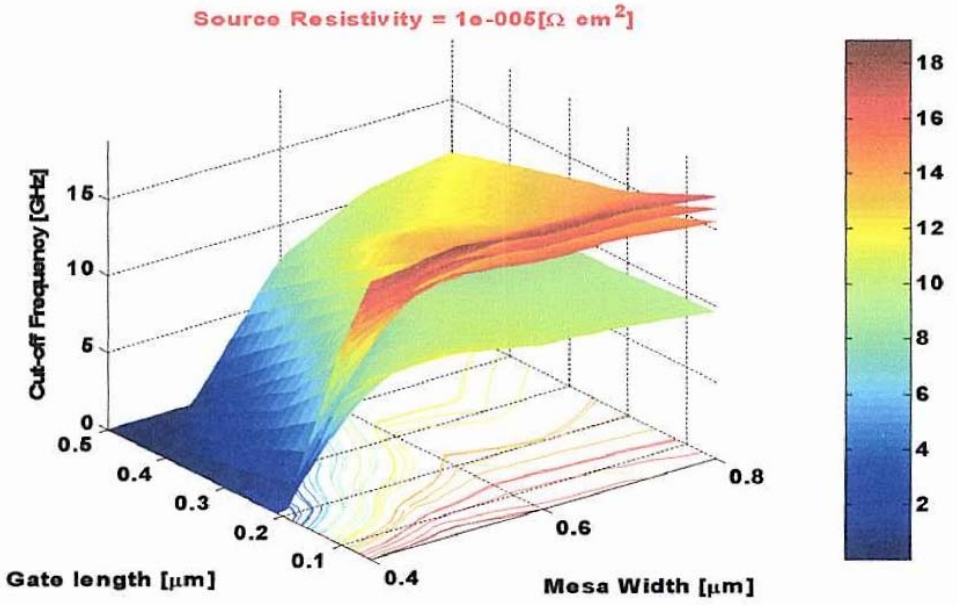

Figure 4.13 Cut-off Frequency as a function of gate length and mesa width at source contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], from top drain contact resistivity $0.5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $50 \cdot 10^{-5}$ [Ω cm^2], respectively.

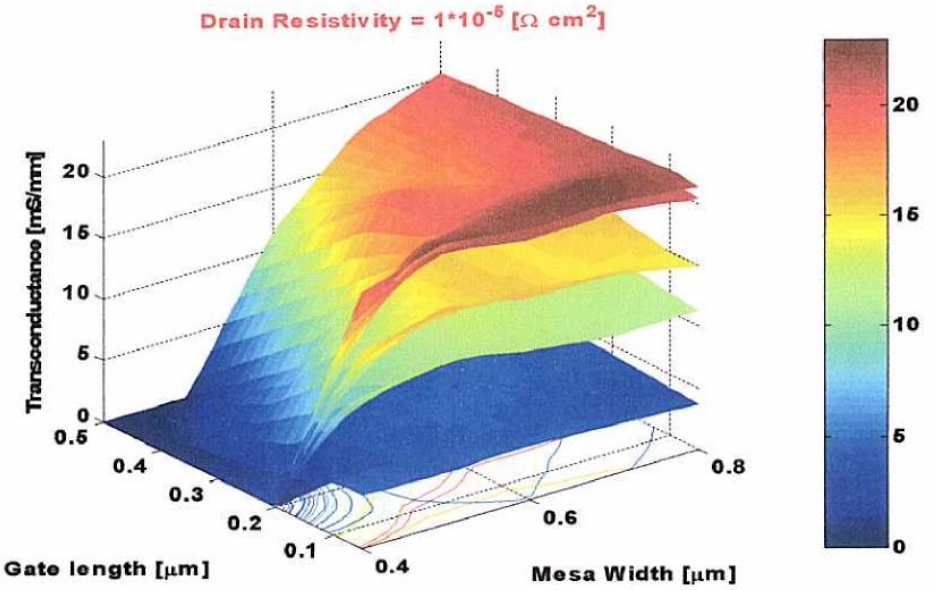

Figure 4.14 Transconductance as a function of gate length and mesa width at drain contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], source contact resistivity $0.5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $50 \cdot 10^{-5}$ [Ω cm^2], from top to bottom, respectively.

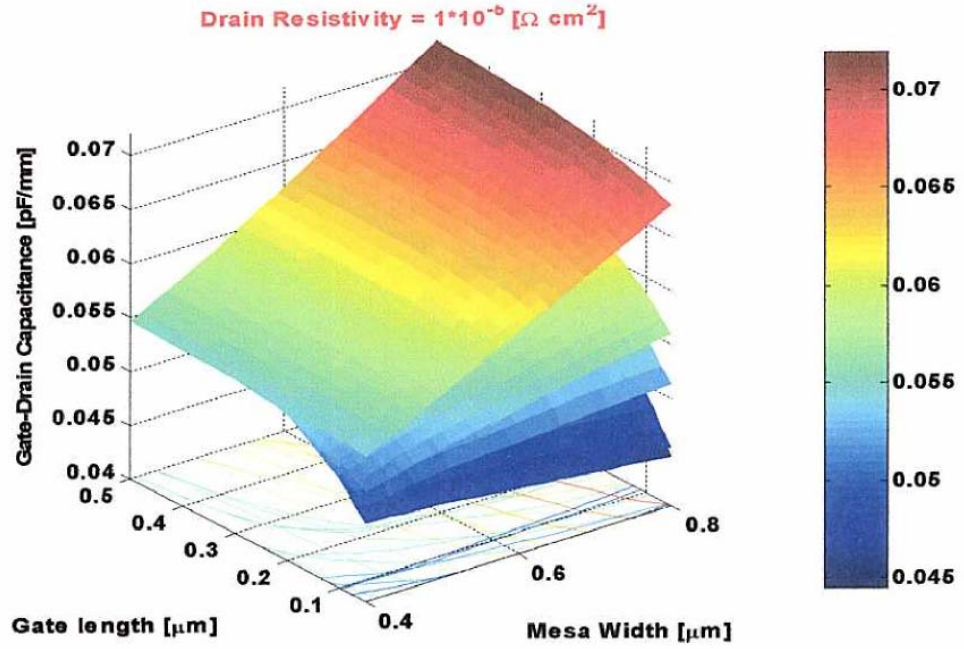

Figure 4.15 Gate-drain capacitance as a function of gate length and mesa width at drain contact resistivity $1 \cdot 10^{-5}$ [Ω·cm^2], source contact resistivity $50 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $0.5 \cdot 10^{-5}$ [Ω cm^2], from top to bottom, respectively.

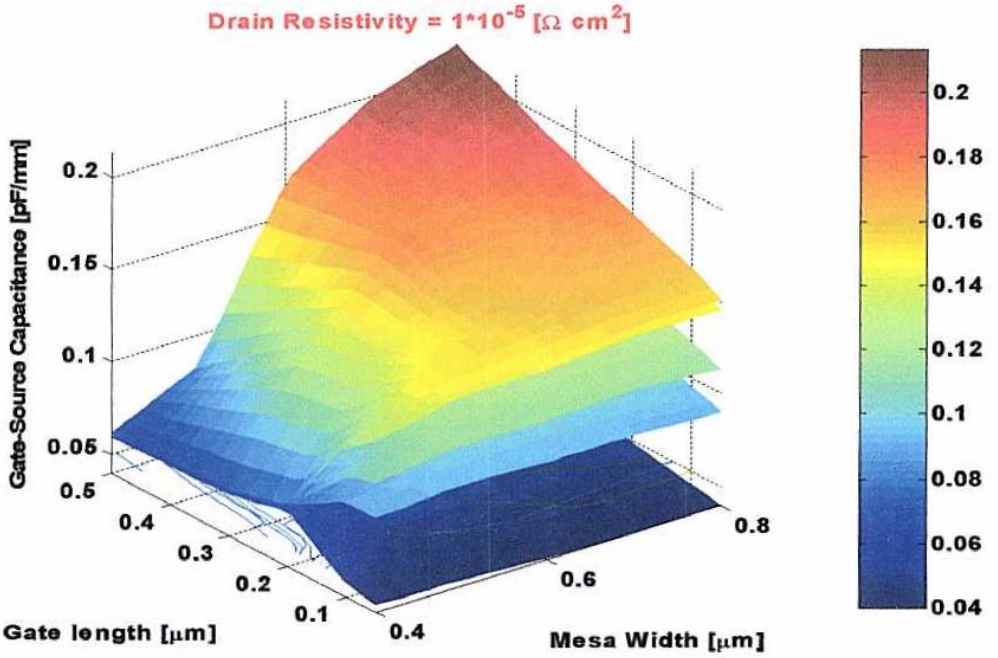

Figure 4.16 Gate-source capacitance as a function of gate length and mesa width at drain contact resistivity $1 \cdot 10^{-5}$ [$\Omega \cdot cm^2$], source contact resistivity $0.5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $50 \cdot 10^{-5}$ [$\Omega\ cm^2$], from top to bottom, respectively.

3. Effect of Mobility

The carrier mobilities and account for scattering mechanisms in electrical transport. MEDICI provides several mobility model choices.

As an alternative to the concentration-dependent mobility, this mobility is concentration- and temperature-dependent empirical mobility function. These are given by the expressions [7]

$$\mu_{n,p} = \mu_{\min} + \frac{\mu_{\max}\left(\frac{T}{300}\right)^{N^{\mu}_{n,p}} - \mu_{\min}}{1+\left(\frac{T}{300}\right)^{xin,p}\left(\frac{N_{total}(x,y)}{N_{refn,p}}\right)^{\alpha_{n,p}}} \qquad (4\text{-}16)$$

In most case, this mobility model use in semiconductor device simulation.

3.1 Perpendicular Electric Mobility Model

This model is applied at every position in the device and not just at interfaces or in the inversion layer and is described by modified version of Analytic Mobility Eqn. (4-16).

$$\mu_{S,n,p} = G_{surfacn,p} \cdot \frac{\mu_{n,p}}{\sqrt{1 + \frac{E_{\perp,n,p}}{E^{\mu}_{cn,p}}}} \tag{4-17}$$

where $E_{\perp,n}$, and $E_{\perp,p}$ are the components of electric that are perpendicular to the side of an element (the default) or the components of electric perpendicular to the current direction. The factors $G_{surfacn}$ and $G_{surfacp}$ are only applied at interfaces between semiconductor and insulator.

3.2 Surface Mobility Model

Along insulator-semiconductor interface, the carrier mobilities can be substantially lower than in the bulk of the semiconductor due to surface scattering. This model is only applied at the interface because it assumes that the carrier inversion layer width is smaller than the grid spacing used at the interface. With this assumption, all the inversion charge effectively occurs at the interface, and it is appropriate to use this model. This model calculates effective mobilities at the interfaces using the expressions

$$\mu_{S,n,p(Surface)} = G_{surfan,p} \left(\frac{E_{eff\perp,n,p}}{E_{refn,p}} \right)^{-exn,p} \mu_{refn,p} \tag{4-18}$$

Also, and enhanced surface mobility model has been included in MEDICI that takes into account phonon scattering, surface roughness scattering, and charges impurity scattering.

The Hewlett-Packard Mobility model takes account dependence on electric s both parallel and perpendicular to the direction of current flow. The expressions for mobility used by this model are

$$\mu_{n,p} = \frac{\mu_{\perp,n,p}}{\sqrt{1 + \frac{\left(\frac{\mu_{\perp,n,p} E_{\square,n,p}}{V_{cn}^{HP}}\right)^2}{\frac{\mu_{\perp,n,p} E_{\square,n,p}}{V_{cn}^{HP}} + G_{n,p}^{HP}} + \left(\frac{\mu_{\perp,n,p} E_{\square,n,p}}{V_{sn,p}^{HP}}\right)^2}} \qquad (4\text{-}19)$$

The expressions for $\mu_{\perp,n,p}$ are given by

$$\mu_{\perp,n,p} = \frac{\mu_0^{HP}}{1 + \frac{E_{\perp,n,p}}{E_{cn,p}^{HP}}} \qquad \text{if } N_{total}(x,y) < N_{ref}^{Hp} \qquad (4\text{-}20)$$

the default value for N_{ref}^{Hp} is $5 \cdot 10^{17}$. if above condition is not satisfied, then $\mu_{\perp,n,p} = \mu_{n,p}$, where $\mu_{n,p}$ are low mobility values described in 4.3.1 Analytic Mobility.

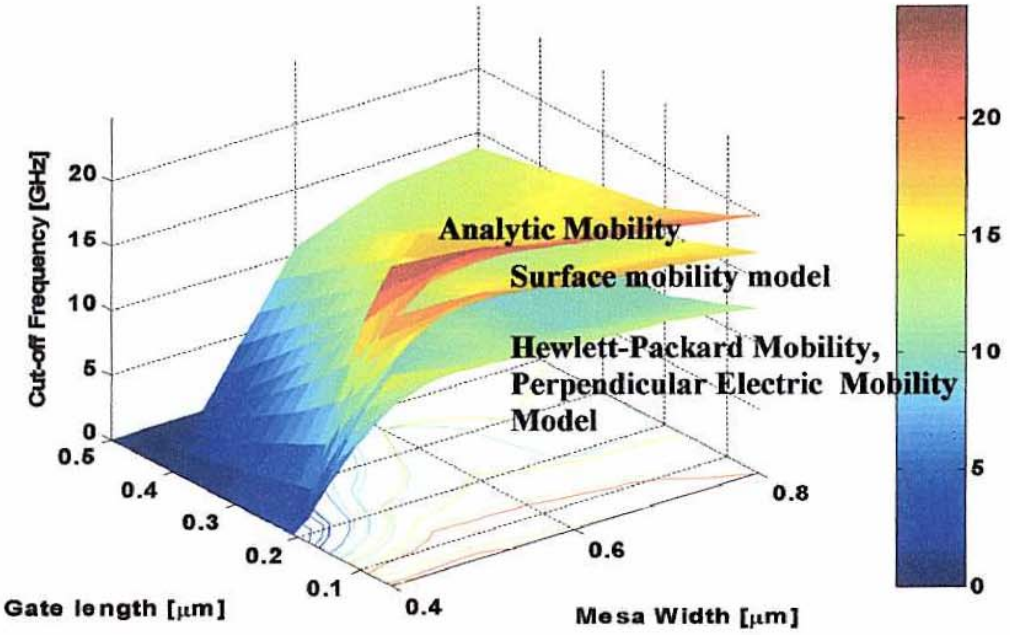

Figure 4.17 Cut-off Frequency depend on mobility model

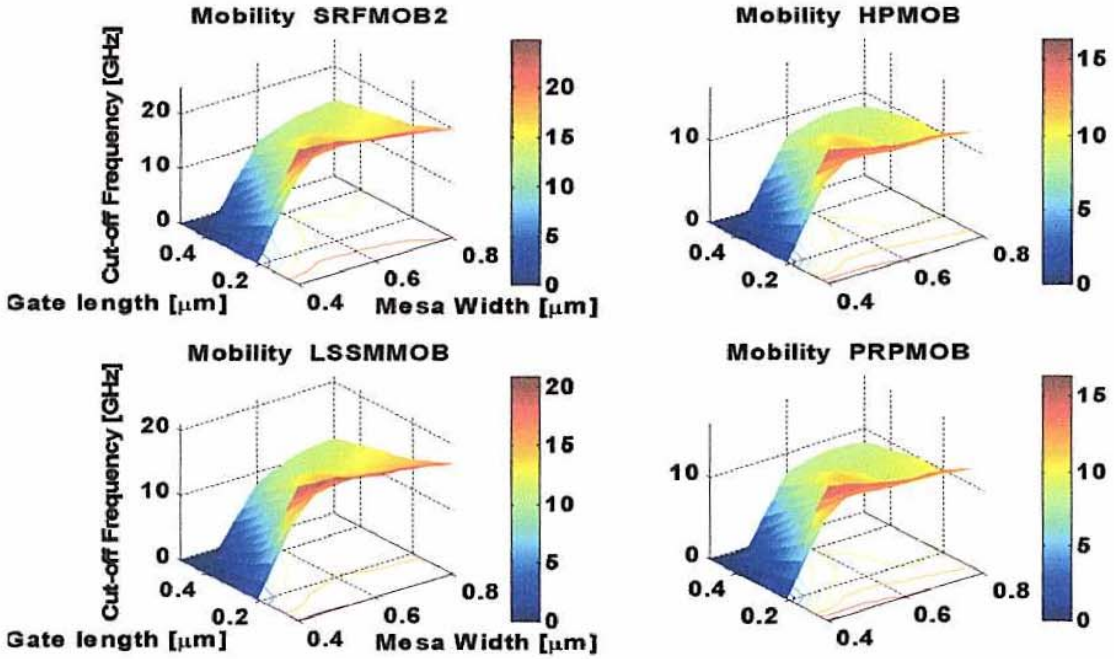

Figure 4.18 Cut-off Frequency in several mobility models

4. Effects of Saturation Drift velocity

In semiconductor device design, one of the most important parameters is a saturated drift velocity that the relationship between the drift velocity of electrons and applied electric field. The first measurements of the high-field drift velocity of electrons in SiC were performed by von Muench and Pettenpaul in 1977 on Lely crystals of 6H-SiC. They reported an electron saturation velocity of $2\times10^{7} cm/s$ parallel to the basal plane at room temperature. But recently, the drift saturation velocity reported to $1.9\times10^{7} cm/s$ in 6H-SiC and $2.2\times10^{7} cm/s$ in 4H-SiC, with data at both room temperatures [8]. Therefore, in this work, we simulated device behavior with different saturated drift velocity, respectively. Shown in Fig. 4.19.

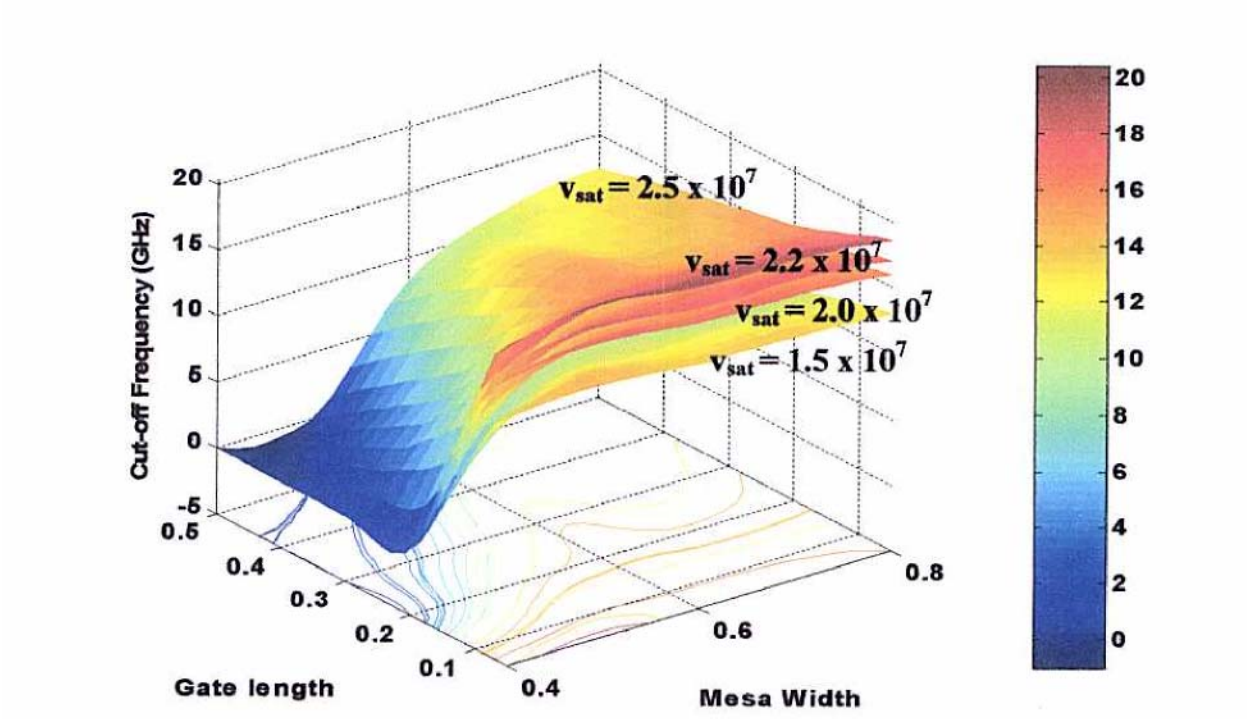

Figure 4.19 Cut-off Frequency depend on Saturation Drift velocity.

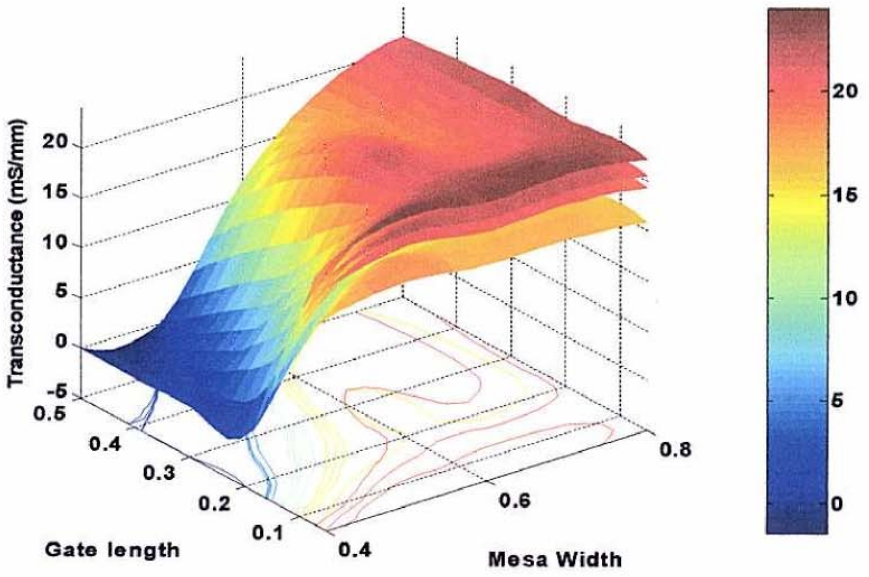

Figure 4.20 Transconductors depend on Saturation Drift velocity, from top v_{sat} is 2.5×10^7, 2.2×10^7, 2.0×10^7 and 1.5×10^7[*cm/s*].

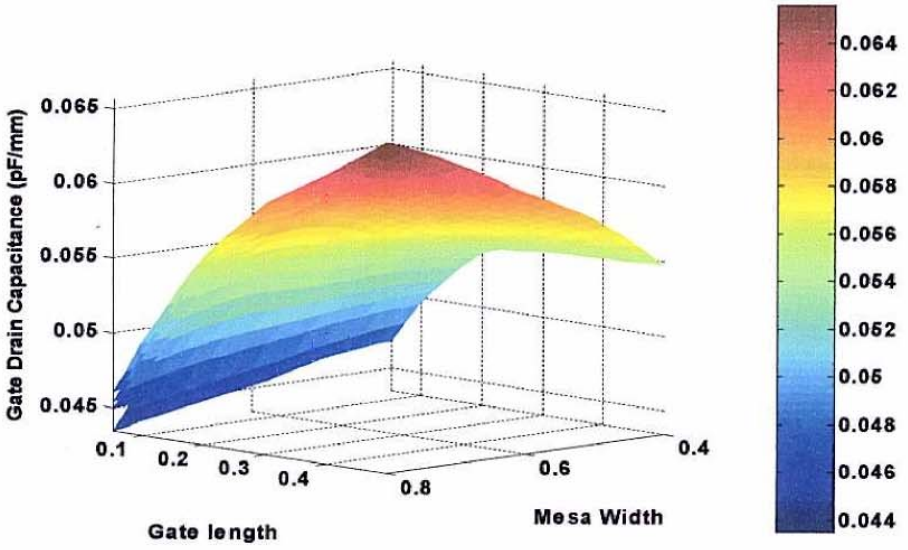

Figure 4.21 Gate-drain capacitances in other saturation drift velocity, from top v_{sat} is 2.5×10^7, 2.2×10^7, 2.0×10^7, and 1.5×10^7[*cm/s*].

5. Considerations for higher frequency SIT Design

In order to design SITs with higher frequency, scaling of the device doping and mesa with has the biggest effect. The transconductance increase faster with doping, roughly linearly, than the input capacitance. The cut-off frequencies as a function of doping and for gate length, assuming ideal contacts, shown in Fig 4.22, cut-off frequencies in excess of 20 *GHz* can be obtained for doping $2 \cdot 10^7 cm^{-3}$. However, reduction of trench width is also important because the value of C_{gd}, which contributes to the input capacitance $C_{in} = C_{gd} + C_{gs}$ of device, essentially scales with the trench width *t*. The effect of C_{gd} gains its importance when the doping is increased because C_{gd} can be approximated by the depletion capacitance under the gate electrode. Also, the reduction in depletion width with increasing doping for a given bias point results in an increase value for C_{gd}. For a scaled trench, the effect of C_{gd} eventually becomes so pronounced that the rise in cut-off frequency for increasing doping levels off. Therefore, it is important to scale the trench together with the mesa width. However, other considerations besides maximizing the frequency response affect the choice of the trench width, such as device heating due to excessive power density.

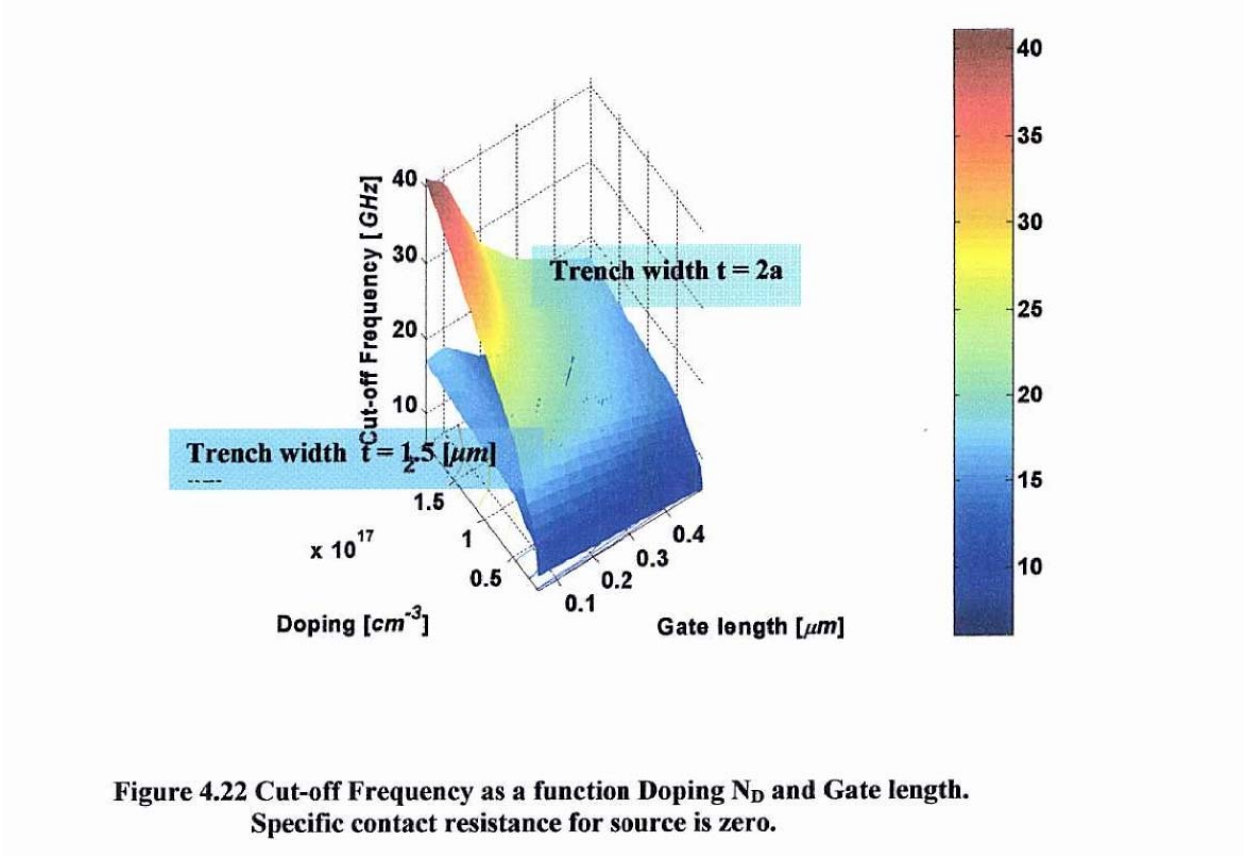

Figure 4.22 Cut-off Frequency as a function Doping N_D and Gate length. Specific contact resistance for source is zero.

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CHAPTER V
TEMPERATURE SIMULATIONS

1. Theoretical Considerations

Silicon Carbide (SiC) is a semiconductor material combining several unique features such as high breakdown field, high electron saturation velocity, and high thermal conductivity. These properties make it a promising candidate for RF power transistors. RF Power transistors are commonly operated at high voltage and high current levels leading to considerable self-heating. Thus, the operating temperature can be much higher than room temperature. To simulate power transistors under these conditions properly, the temperature dependence of the electron mobility in the both the low-field and high-field region must be also taken into account in the mobility models. Recently, the electron mobility in 4H, 6H, and, 3C SiC has been investigated both experimentally and theoretically by Monte Carlo(MC) simulations by several authors, and models for the electron mobility have been proposed. Unfortunately, none of these models includes detailed temperature dependence for both the low-field and high-field mobilities [1]. In this works, we will use the electron mobility model for SiC RF device simulation. The models are based on reported mobility data and include the dependence of the mobility on doping concentration, temperature, and electric field. The following 4H-SiC temperature dependant parameters have been determined by [1]

$$\mu_{\max} = 950 \times \left(\frac{T}{300K}\right)^{-2.4} \tag{5-1}$$

$$\mu_{\min} = 40 \times \left(\frac{T}{300K}\right)^{-0.5} \tag{5-2}$$

$$N_{ref} = 2 \times 10^{17} \times \left(\frac{T}{300K}\right) \tag{5-3}$$

$$\alpha = 0.76 \tag{5-4}$$

$$\beta = \beta_0 + a \times \exp\left(\frac{T - T_0}{b}\right) \tag{5-5}$$

2. Gate-Drain Breakdown Voltage

Silicon Carbide (SiC) has received increasing attention for power switching, microwave and high temperature applications due to its high breakdown electric field, thermal conductivity and electron saturation drift velocity. One of the most important parameters of SiC power device is its breakdown voltage. Also, one of the advantages of the static induction transistor is its high output impedance which results from the high breakdown voltage between the gate and drain terminals. This is expected because of the vertical arrangement of the device channels. The gate electrode, in effect, looks like a finely meshed grid such that the overall field distribution approaches that of a parallel plate capacitor. The local field at the very corner of the gate is expected to approach arbitrarily high values, depending on how sharp the corner will be in practice, as shown in Fig. 5.1 through Fig. 5.3. However, this field spike does not mean that the breakdown

due to avalanche will occur at much lower voltages than predicted by calculation. The avalanche breakdown process occurs when electrons and/or holes, moving across the space charge region, acquire sufficient energy from the electric field to create electron-hole pairs by colliding with atomic electrons within the depletion region. Thus, for avalanche to occur, a high enough electrical field must be supplied to the charge carriers in order to produce electron-hole pairs, and a certain extent of the avalanche region is needed to obtain a round trip gain of unity in order to sustain the avalanche. In this work, because of the importance of the gate-drain breakdown voltage, the maximum obtainable output voltage for a SIT was investigated by means of simulations with several temperatures and doping, respectively.

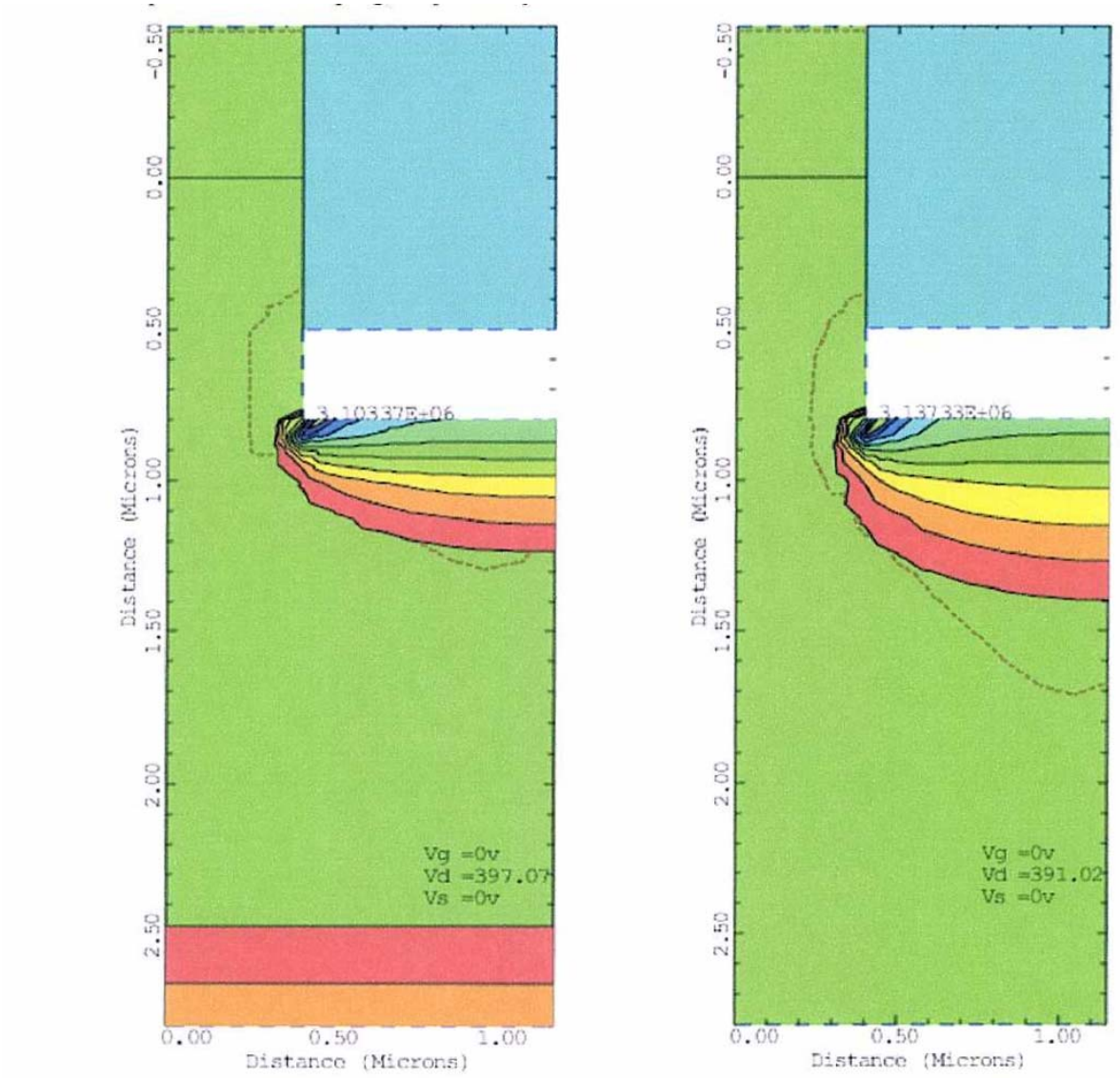


Figure 5.1 Avalanche Breakdown voltage and Electric Field at Impact Ionization integral reaches unity for 300K and 400K.

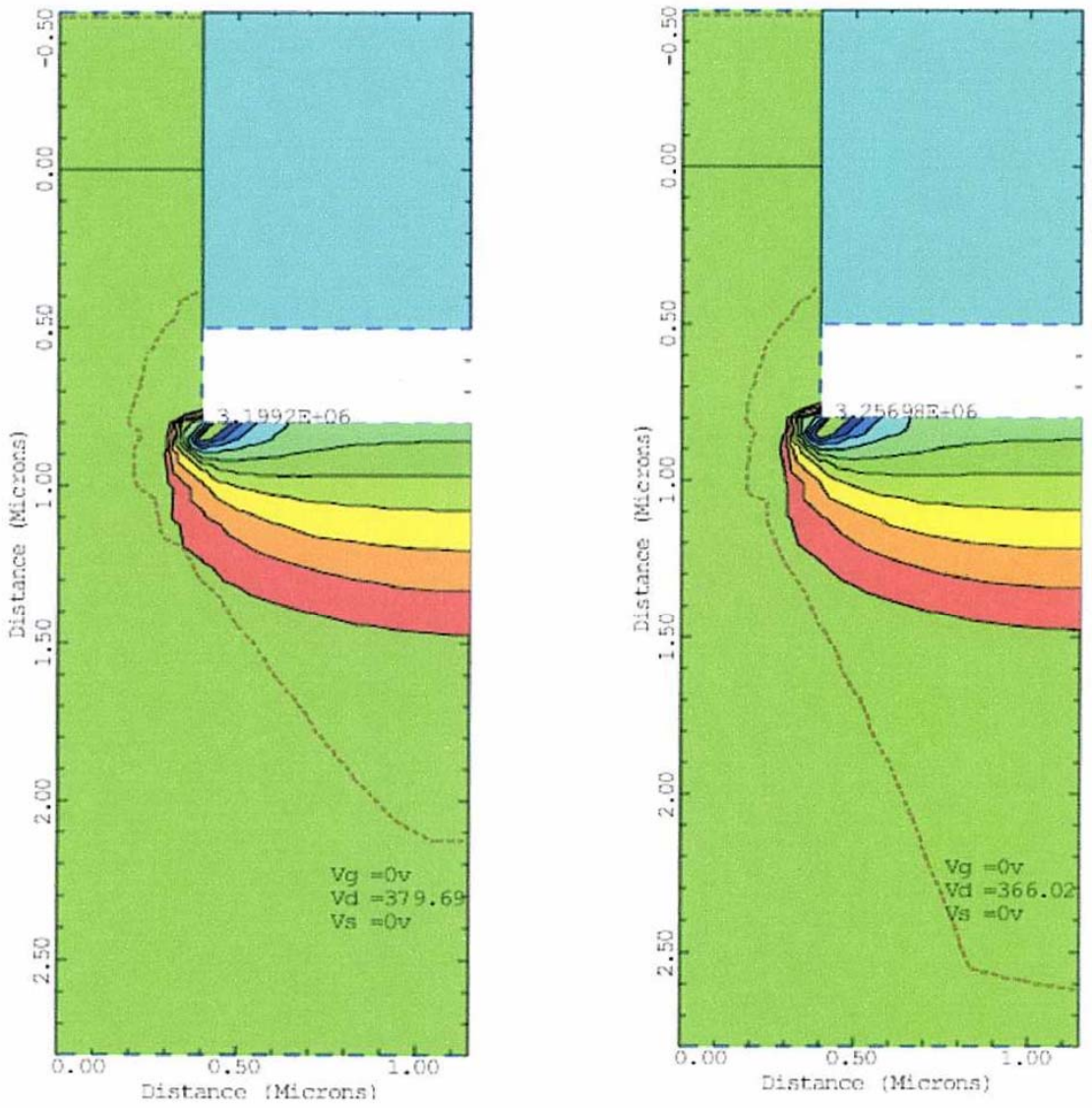


Figure 5.2 Avalanche Breakdown voltage and Electric Field at Impact Ionization integral reaches unity for 500K and 600K.

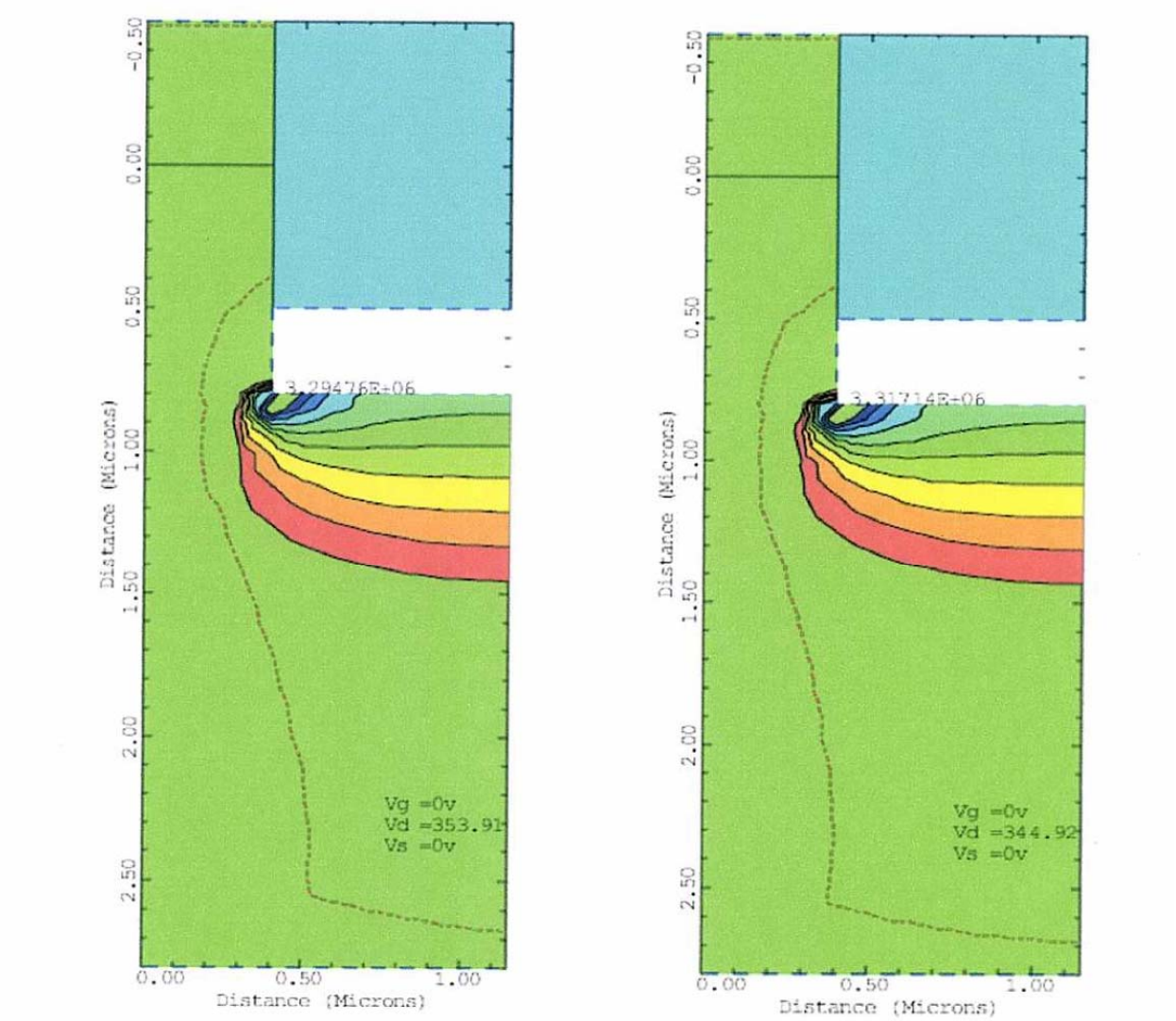


Figure 5.3 Avalanche Breakdown voltage and Electric Field at Impact Ionization integral reaches unity for 700K and 800K.

In Fig. 5.1 to Fig. 5.3, we can see that avalanche breakdown voltages decrease, maximum electric field increase, and depletion region increase. The breakdown voltage due to avalanche breakdown predicted by the ionization integral is usually lower for the SIT because it does not take into account that a carrier can escape from the path along the highest field either by diffusion or scattering due to the curvature of the electric field line, thereby decrease the multiplication factor of carriers in the avalanche region. In Fig. 5.4 through Fig. 5.7, four different drain regions are considered with doping concentrations of $5\cdot10^{15}cm^{-3}$, $1\cdot10^{16}cm^{-3}$, $5\cdot10^{16}cm^{-3}$, and $2\cdot10^{17}cm^{-3}$ that have a thickness of gate-drain, L_{gd} =4μm, 3μm, 2μm, and 1.3μm, respectively. When the gate-drain voltage is not limited by the gate edge, the device will break down intrinsically at the corner of the gates facing the mesa center. The simulated breakdown due to avalanche of the device 668V, 473V, 382V, and 174V for the two considered drain regions, and the avalanche breakdown voltage is roughly 25% lower than one would obtain from a parallel plate calculation.

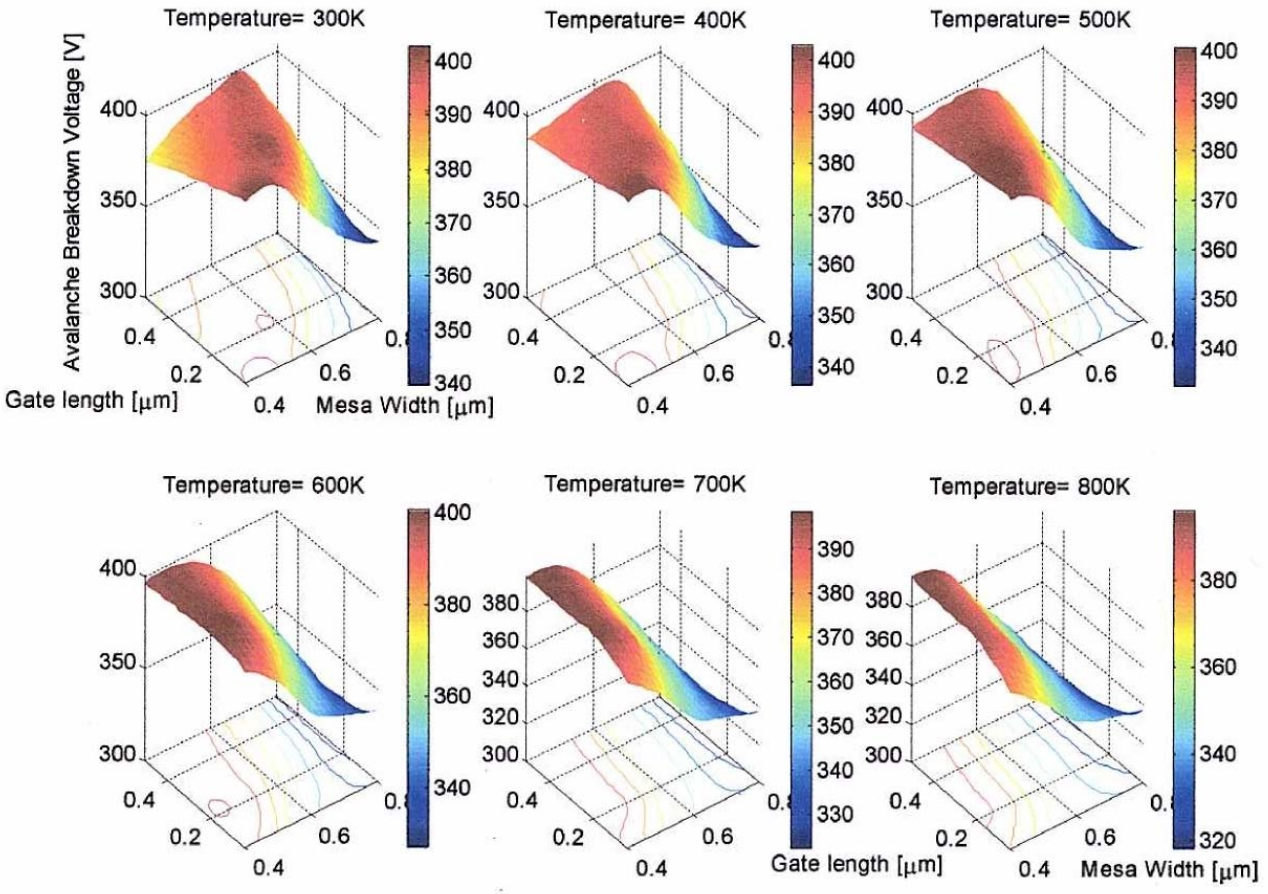


Figure 5.4 Avalanche Breakdown voltage with temperature increasing for the doping $5 \cdot 10^{16}$ [cm^{-3}].

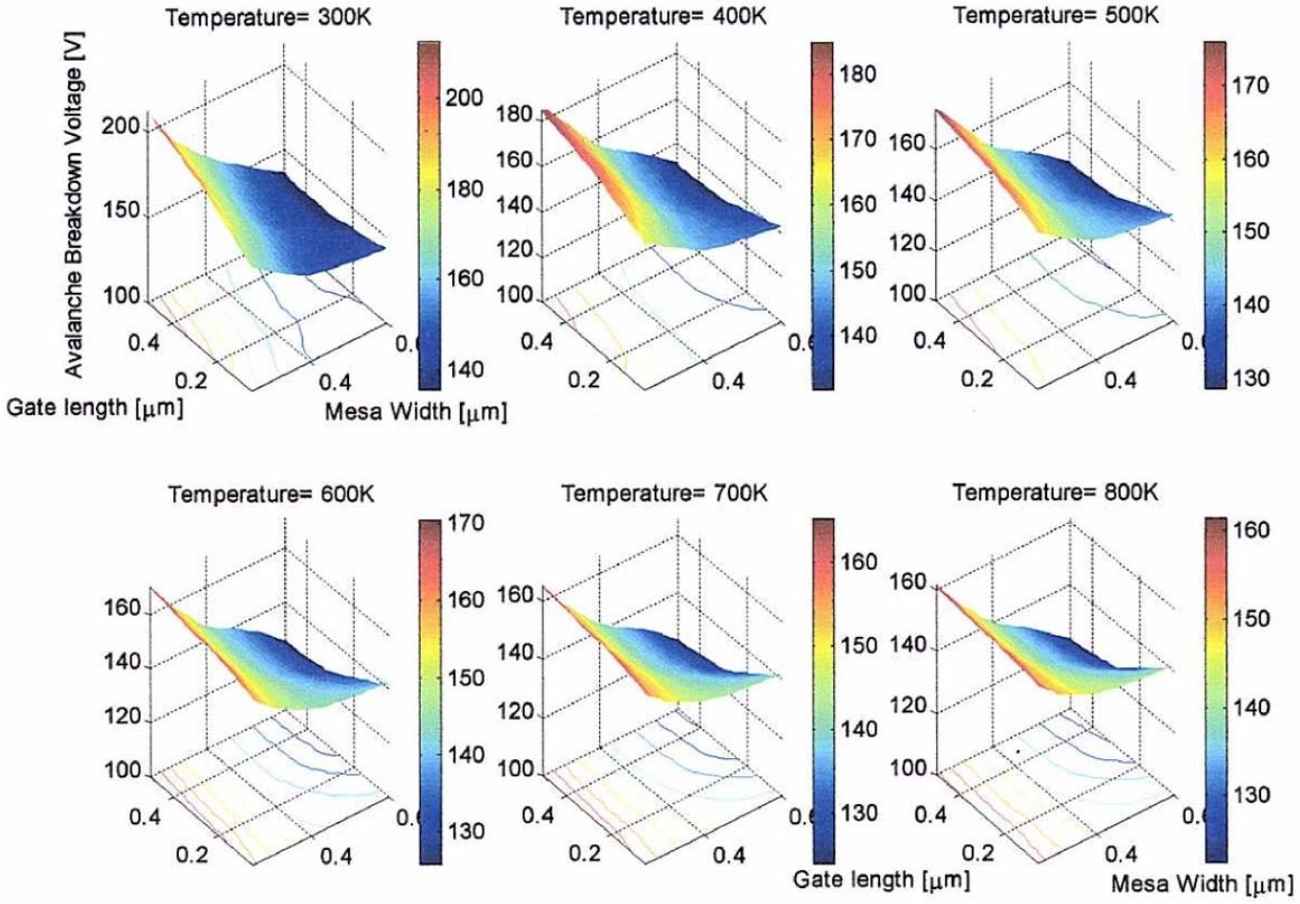


Figure 5.5 Avalanche Breakdown voltage with temperature increasing for the doping $2 \cdot 10^{17}$ [cm^{-3}].

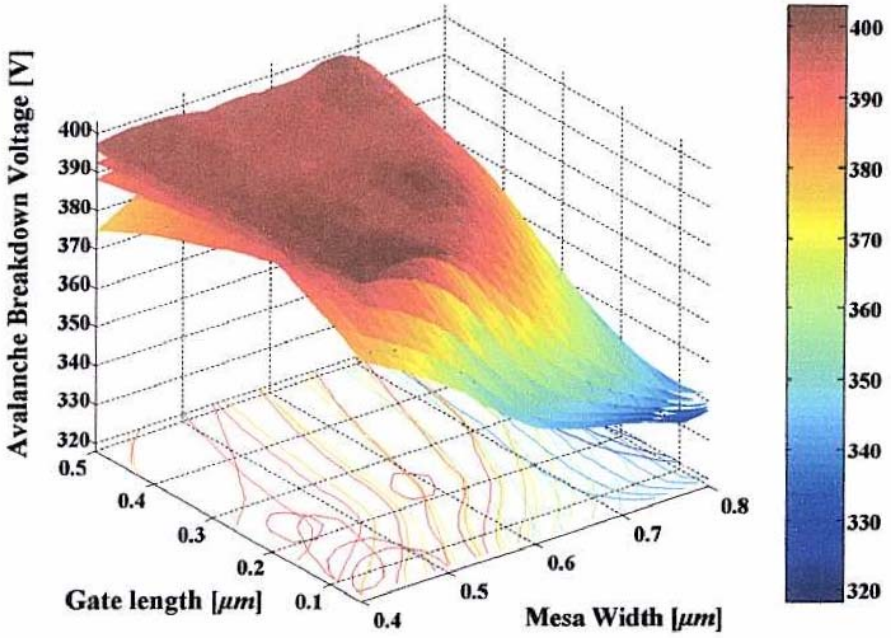


Figure 5.6 Avalanche Breakdown voltage with temperature increasing for the doping $5 \cdot 10^{16}$ [cm^{-3}], from top 300K, 400K, 500K 600K 700K, 800.

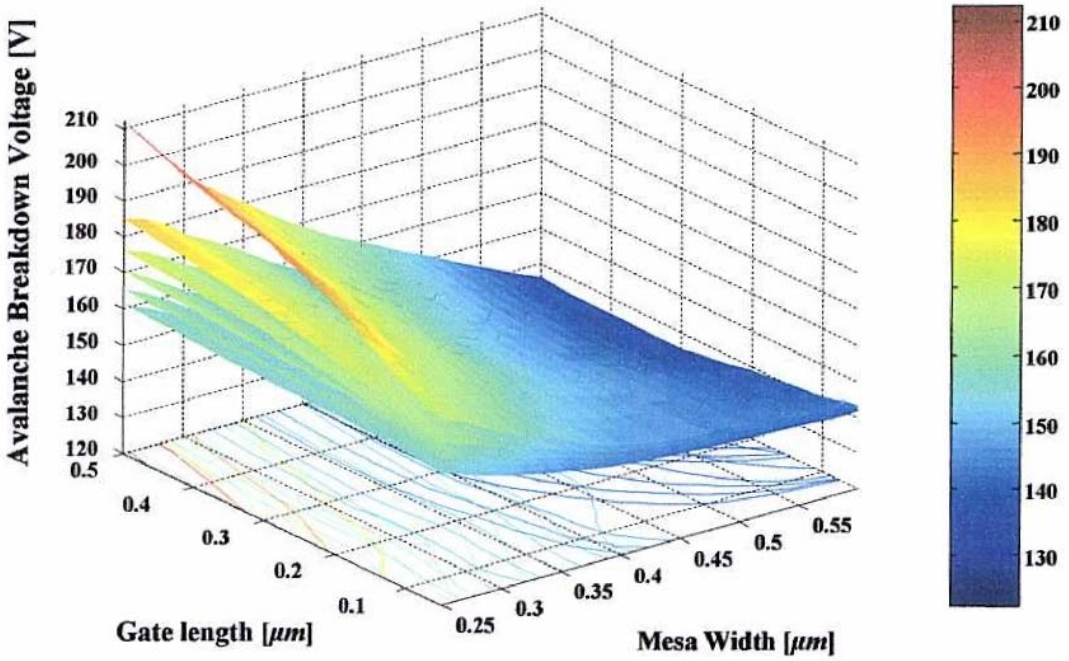
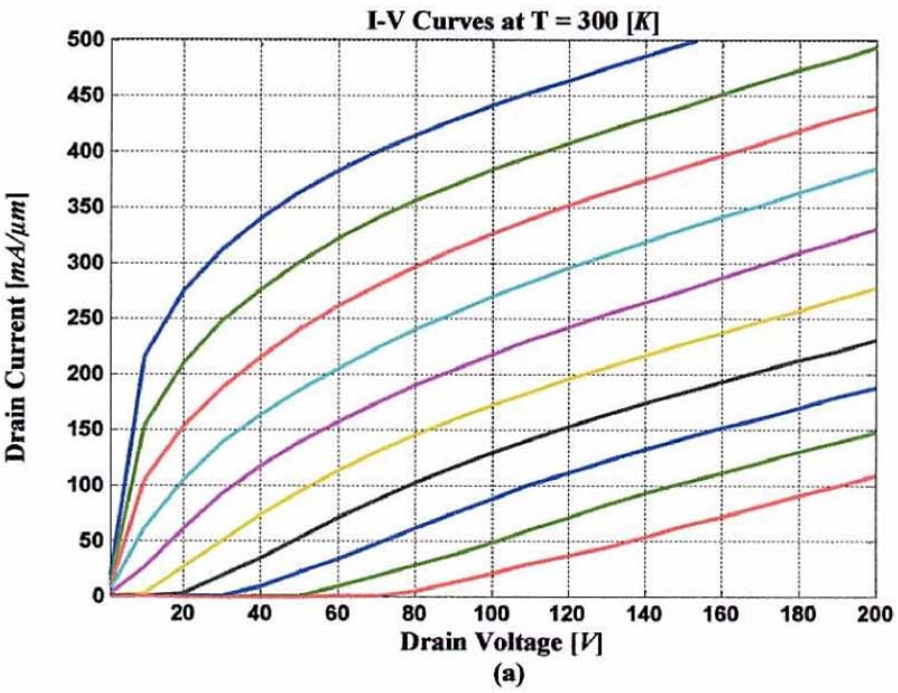


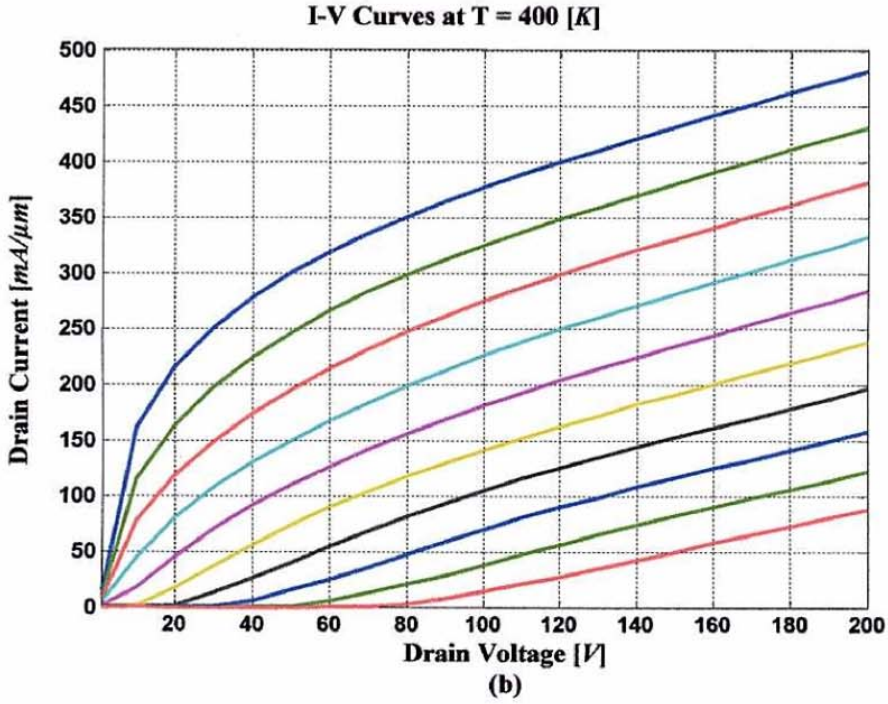
Figure 5.7 Avalanche Breakdown voltage with temperature increasing for the doping $2 \cdot 10^{17}$ [cm^{-3}], from top to bottom 300K, 400K, 500K 600K 700K, 800K.

3. Temperature Dependent DC performances

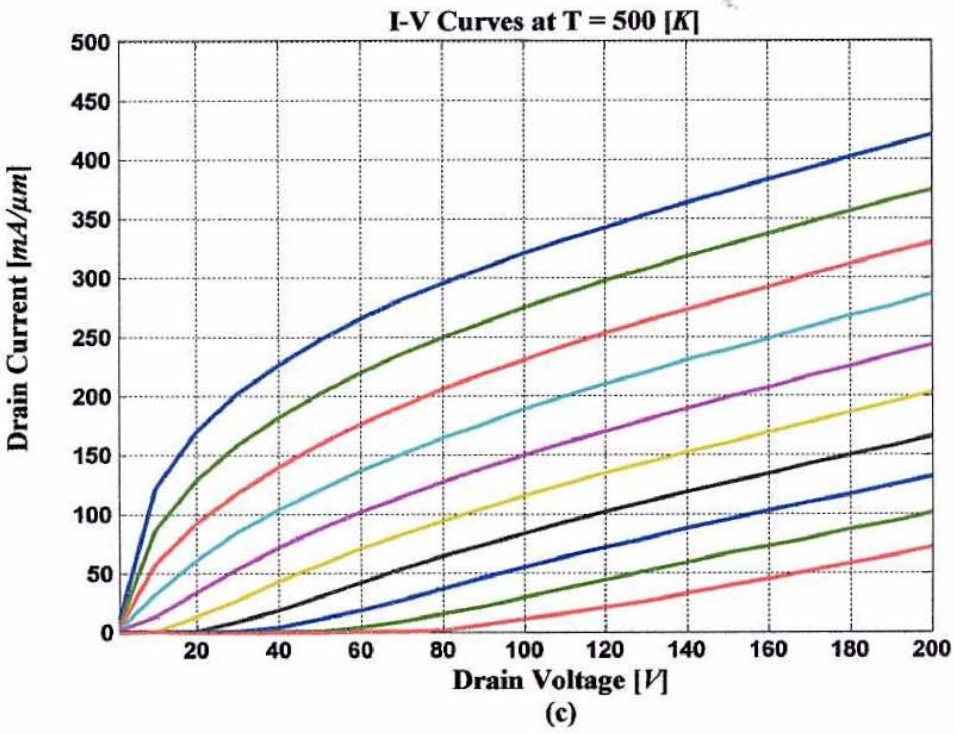
DC performances at the room temperature have been described in chapter 3. Fig 5.6 shows the I-V curves from 300K to 800K. As the operating temperature increases, I_{ds} decrease monotonically for $V_g = 0V$. At 700K, the saturation current it almost 50% of the 300K. This is quite good comparison with Si device, which is completely useless at such temperature. The temperature dependent characteristics can be explained as follows. As temperatures increase, more donors are ionized; the depletion width decreases, and the effective channel thickness increase. Thus, the total number of mobile carriers increases. On the other hand, the carrier mobilitizes decreases. The maximum current is shown in Fig. 5.7. As temperature increases, the maximum current decreases.


I-V Curves at T = 300 [K]
Drain Current [mA/μm]
Drain Voltage [V]
0
50
100
150
200
250
300
350
400
450
500
20
40
60
80
100
120
140
160
180
200

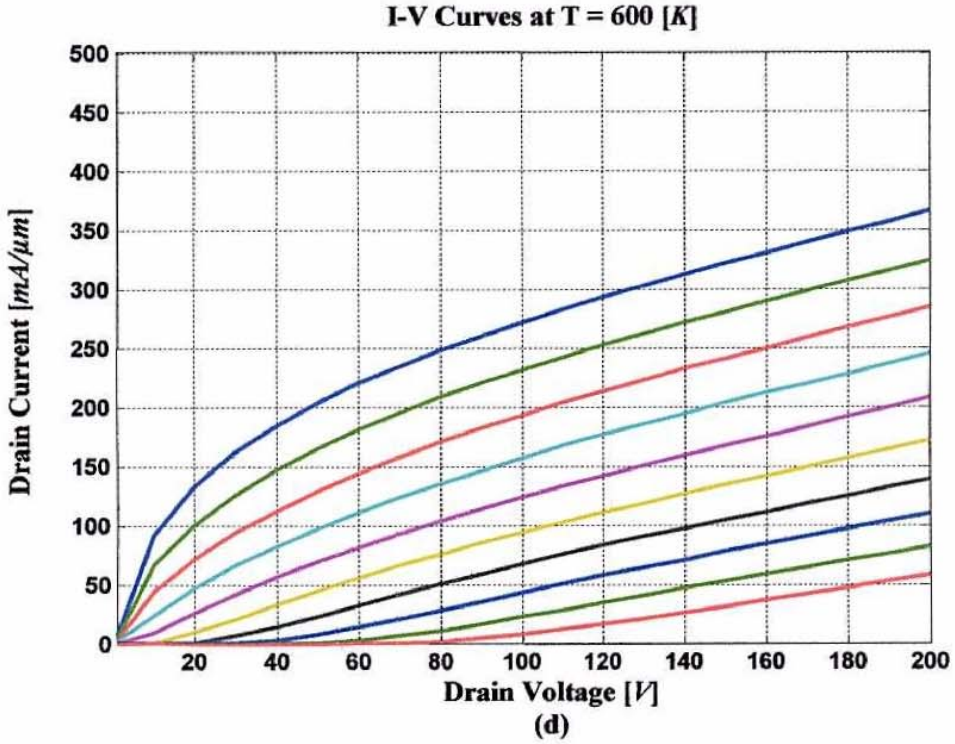
(a)


I-V Curves at T = 400 [K]
Drain Current [mA/μm]
Drain Voltage [V]
0
50
100
150
200
250
300
350
400
450
500
20
40
60
80
100
120
140
160
180
200

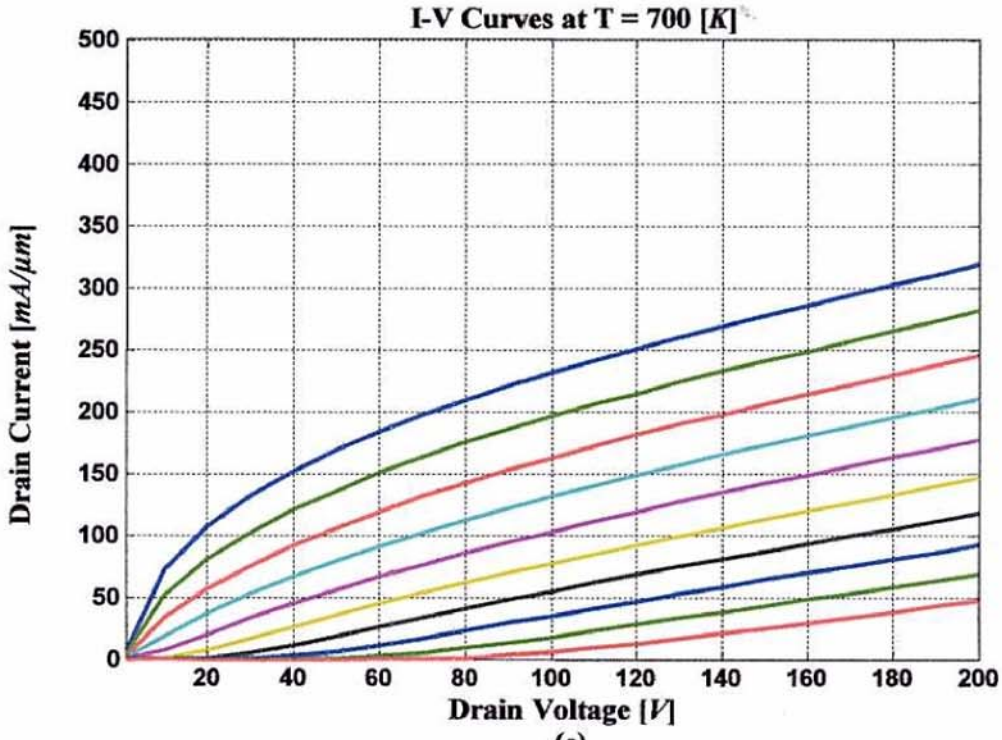
(b)


I-V Curves at T = 500 [K]
Drain Current [mA/μm]
Drain Voltage [V]
0
50
100
150
200
250
300
350
400
450
500
20
40
60
80
100
120
140
160
180
200

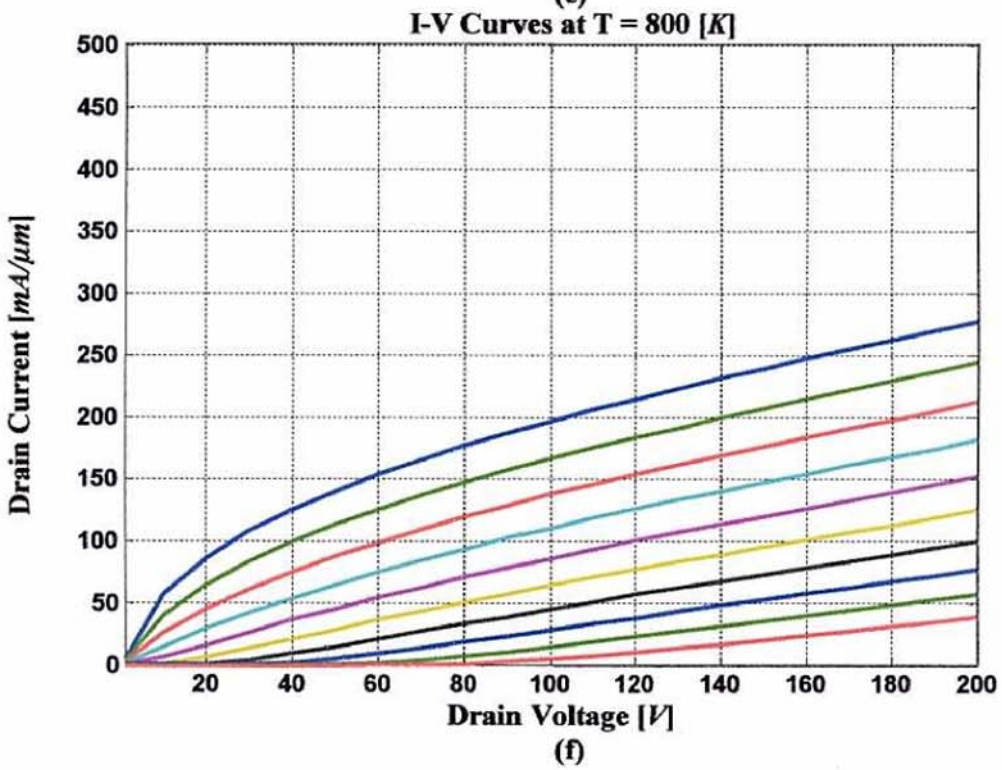
(c)


I-V Curves at T = 600 [K]
Drain Current [mA/μm]
Drain Voltage [V]
0
50
100
150
200
250
300
350
400
450
500
20
40
60
80
100
120
140
160
180
200

(d)



(e)



(f)

Figure 5.8 I-V Curves at (a) T=300*K*, (b) T=400*K*, (c) T=500*K*, (d) T=600*K*, (e) T=700*K*, (f) T=800*K*, respectively. From the top to the bottom, the five curves in each figure correspond to V_g=0*V*, -2*V*, -4*V*, -6*V*, -8*V*, -10*V*, -12*V*, -14*V*, -16*V*, -18*V*.

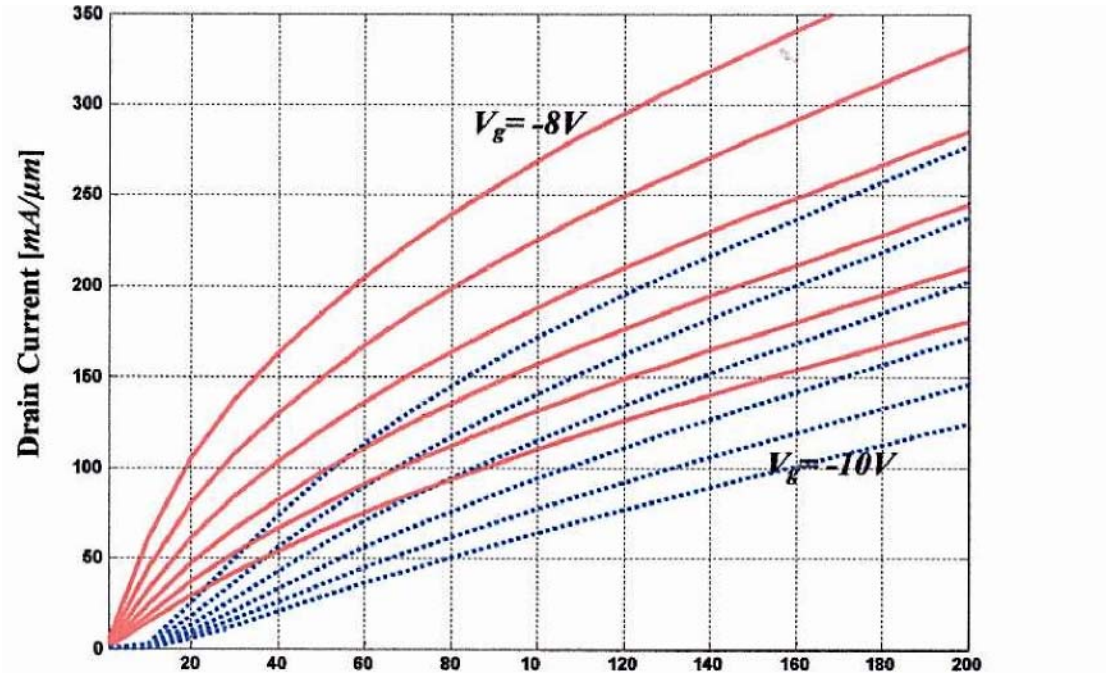
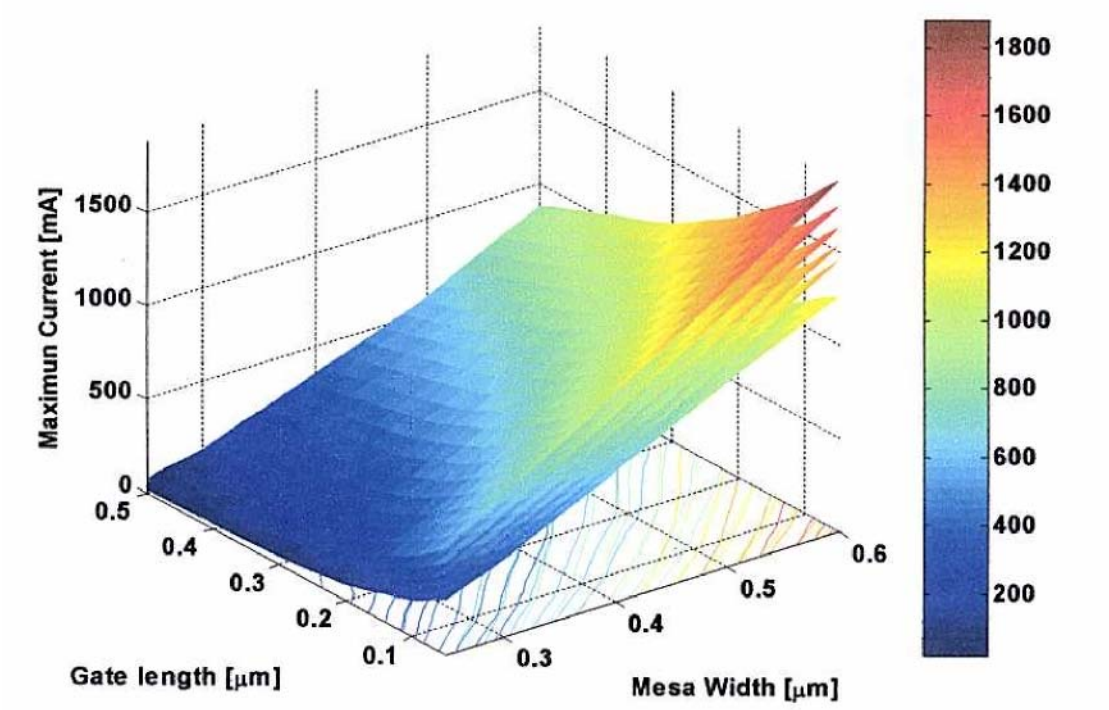


Figure 5.9 I-V Curves at T=300K, 400K, 500K, 600K, 700K, 800K for $V_g = 8V$, 10*V*, from the top to the bottom, respectively.



'igure 5.10 Maximum Current at T=300*K*, 400*K*, 500*K*, 600*K*, 700*K*, 800*K* for $2 \cdot 10^{17} cm^{-3}$, from the top to the bottom, respectively.

4. Temperature Dependent Frequency performances

Since the system input and output impedance are variables, we are interested in the maximum frequency that the device can operate The definition of this maximum frequency becomes ambiguous. These are two standard measures of this maximum frequency; f_T and $f_{\max}$. The f_T, or the frequency bandwidth is the frequency that the transistor has unity current gain while driving a short circuit load. This is equal to the $h_{21}=1$ frequency. The $f_{\max}$ is the maximum frequency of oscillation. In order to have oscillation, the gain of the device must be equal to, or above unity. Therefore $f_{\max}$ is the highest frequency unity gain can be obtained for any load condition. This is obtained under the maximum available gain condition; ($G_{\max}$) which occur when the device is conjugate matched.

Y or *S*-parameters can be extracted from MEDICI simulation and h_{21}, $G_{\max}$ can be obtained by calculation. The h_{21} can be calculated by

$$h_{21}=\frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{21}S_{12}}=\frac{Y_{21}}{Y_{11}} \tag{5-6}$$

This is using standard parameter transformations. From this f_T is obtained. The maximum available power gain can also be calculated from *Y* or *S*-parameters.

$$G_{\max}=\left|\frac{S_{21}}{S_{12}}\right|\left(K-\sqrt{K^2-1}\right) \tag{5-7}$$

where K is the stability factor, which is given by

$$K=\frac{1+\left|S_{11}S_{21}-S_{12}S_{21}\right|^2-\left|S_{11}\right|^2-\left|S_{22}\right|^2}{2\left|S_{12}\right|\left|S_{21}\right|} \tag{5-8}$$

The stability factor will predict the stability of the device against oscillation. For a *K* greater than unity and positive, the device will be unconditionally stable for any impedance presented to it. Oscillations are possible whenever an $|S_{11}|$ or $|S_{22}|$ greater than unity. The device is unconditionally stable if the input and output impedances are greater than zero for any source or load impedance presented. The calculation of $G_{\max}$ is only valid when the device is unconditionally stable. From Eqn. (5-6) the gain bandwidth f_T can be calculated directly from the simulated Y-parameters. Fig. 5.8 shows h_{21} verses frequency. The extrapolated intercept of h_{21}= unity (0 dB) can be found f_T. For this SIT, 0.5 μ*m* mesa width and gate length 0.3 μ*m* with $V_g=-4V$, $V_d=50V$, f_T is 9.6 *GHz* at 600 [K].

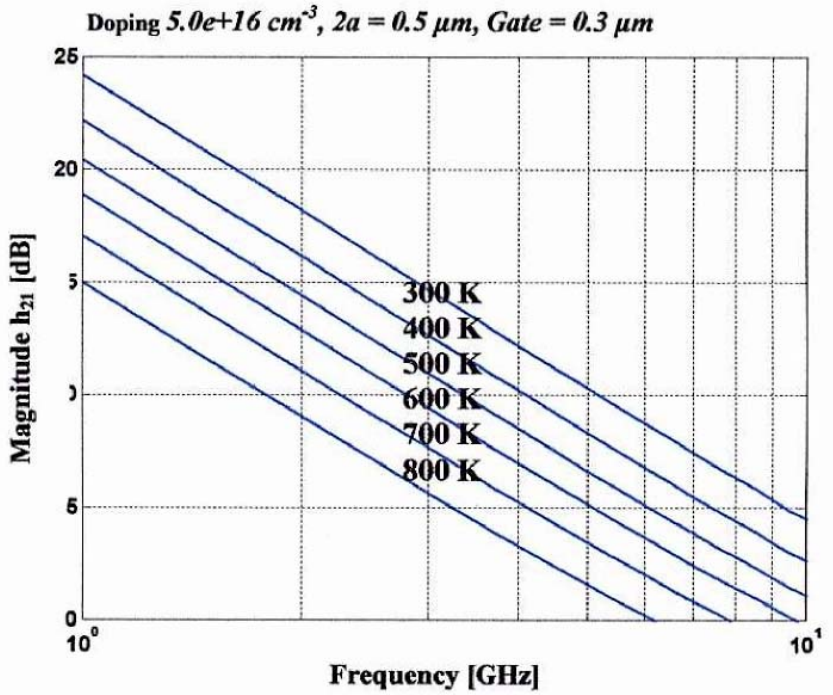


Figure 5.11 h_{21} parameter from simulated Y-parameter showing the bandwidth-gain product (f_T) of 9.6 *GHz* at 600 [K]. Bias point is $V_d = 50$ *V*, $V_g = -4$ *V*.

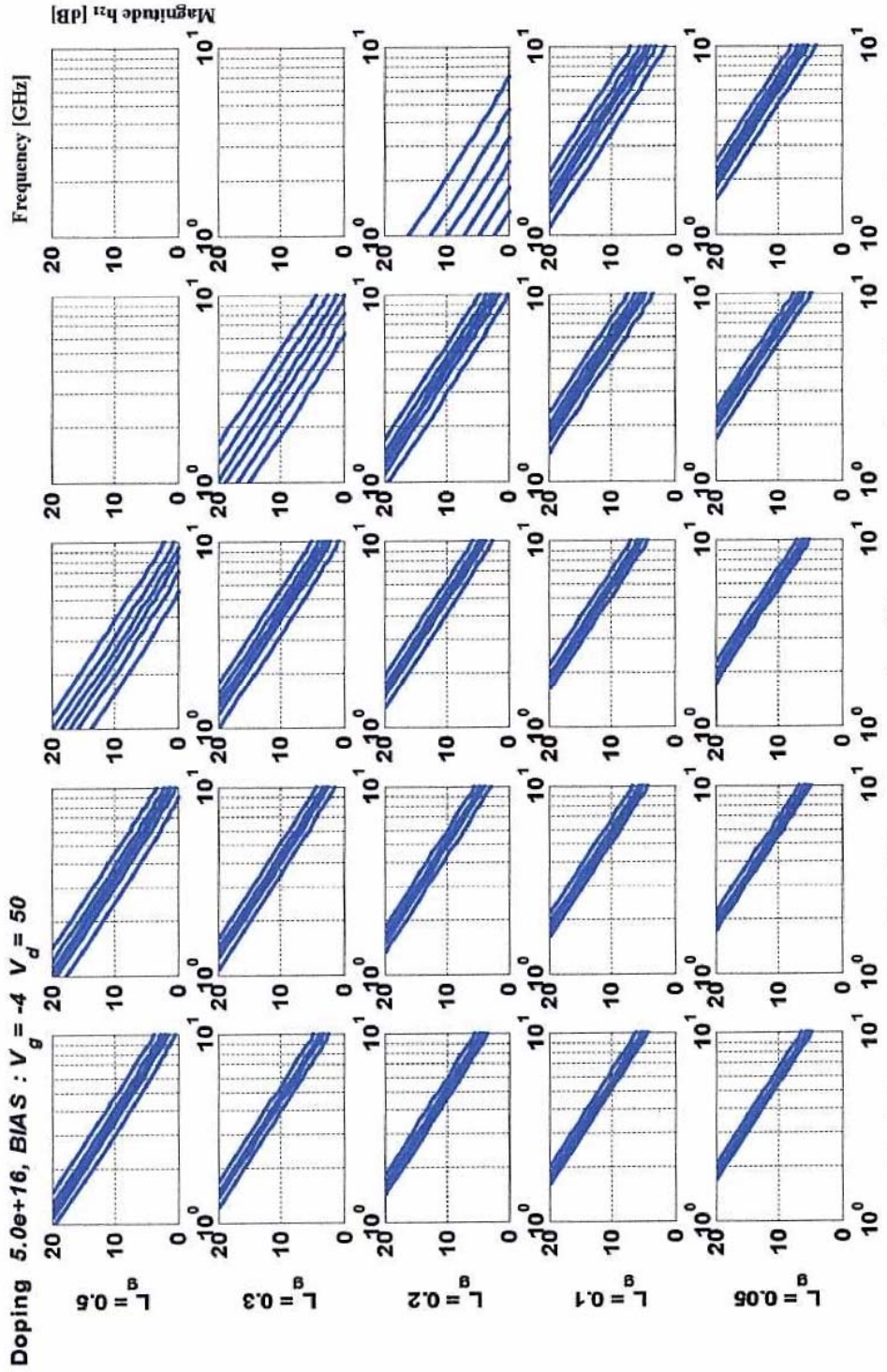


Figure 5.12 h_{21} parameter from simulated Y-parameter with bas point is V_d = 50 *V*, V_g = -4 *V*, Doping value *5.0e+16 cm*$^{-3}$, from top to bottom curves, 300, 400 500, 600, 700, 800 [K], respectively.

Additionally from the Y-parameters obtained by MEDICI Simulations, the data can be converted into S-parameters, and using information from Eqn. (4-9) through (4-12), the circuit model capacitance can be determined. Also, we can obtain cut-off frequency from the capacitance. Fig. 5.10 thorough Fig. 5.20 show cut-off frequency, transconductance, gate-source capacitance and gate-drain capacitance for a bias point of V_d = 10, 50, 75,

[V] and $V_g = 0$, -4 [V] with doping value 5.0e + 16, 2.0e + 17 [cm^{-3}]. As temperature increases, frequency decreases. Mainly, transconductance affect the frequency. The other side, gate-drain capacitance is an inversely proportional temperature increase.

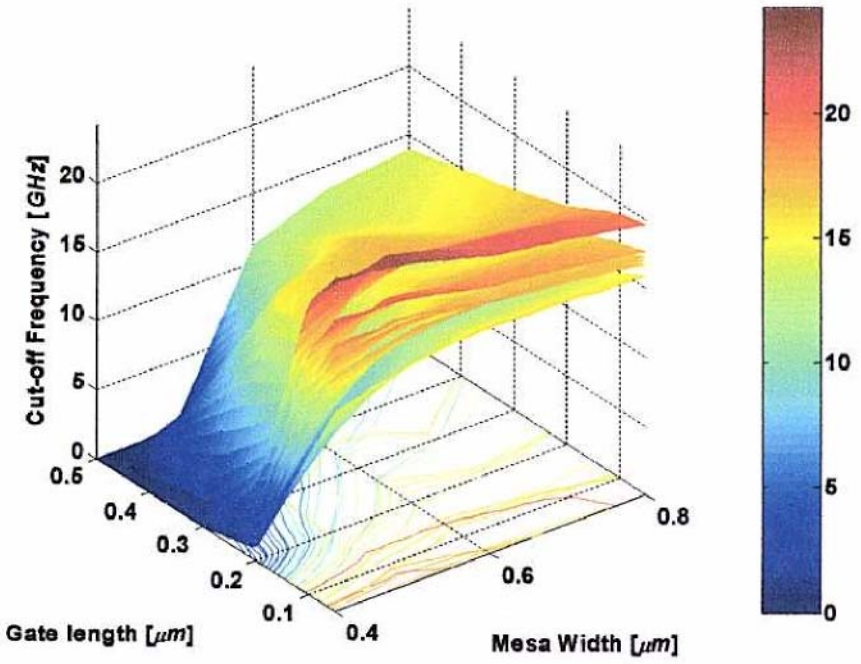


Figure 5.13 Cut-off frequency plotted as a function of gate length and mesa width for a bias point of V_d = 50*V*, V_g = -4 *V*, Doping value $5.0e+16cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

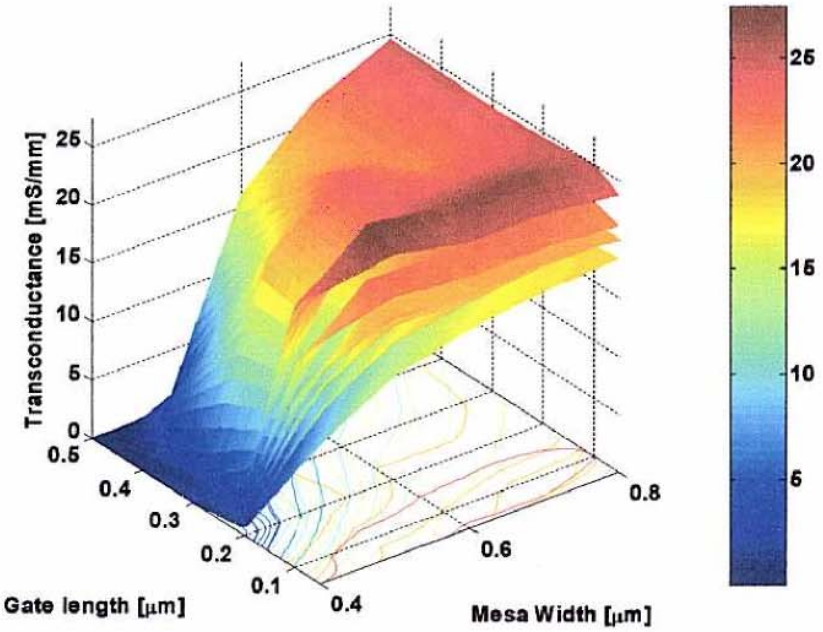


Figure 5.14 Transconductance plotted as a function of gate length and mesa width for a bias point of V_d = 50 V, V_g = -4 V, Doping value *5.0e+16* cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K],

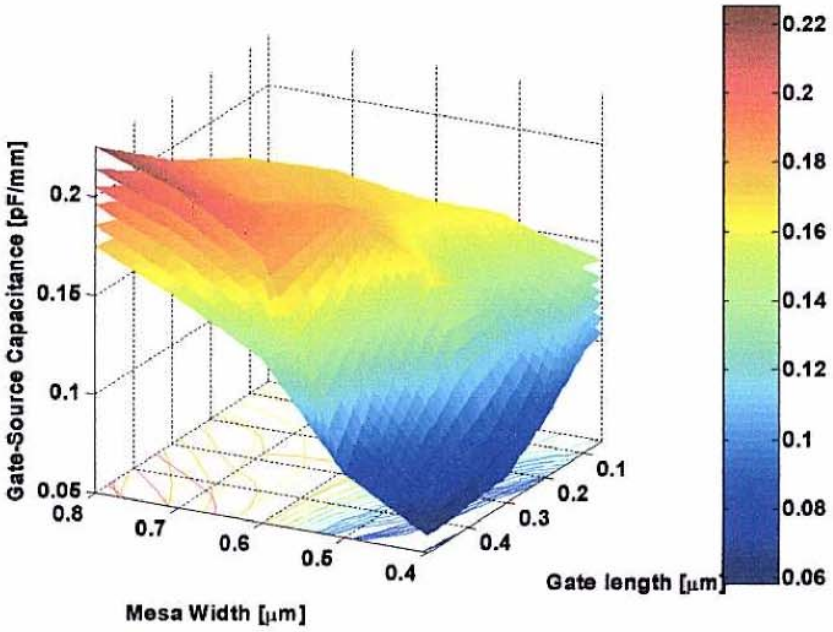


Figure 5.15 Gate-Source capacitance plotted as a function of gate length and mesa width for a bias point of V_d = 50 V, V_g = -4 V, Doping value *5.0e+16* cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

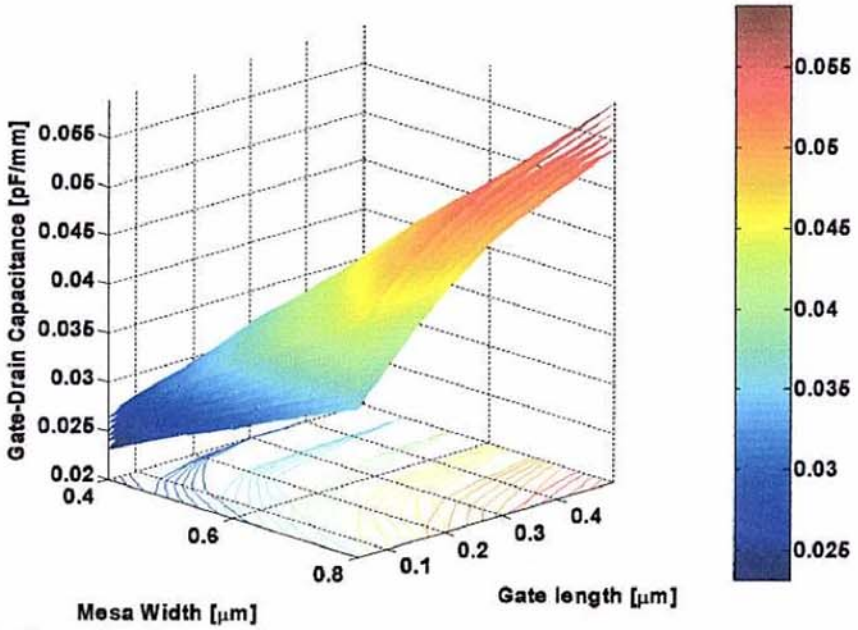


Figure 5.16 Gate-Drain capacitance plotted as a function of gate length and mesa width for a bias point of $V_d = 50$ V, $V_g = -4$ V, Doping value *5.0e+16* cm^{-3}, from top to bottom curves, 800, 700, 600, 500, 400, 300 [K], respectively.

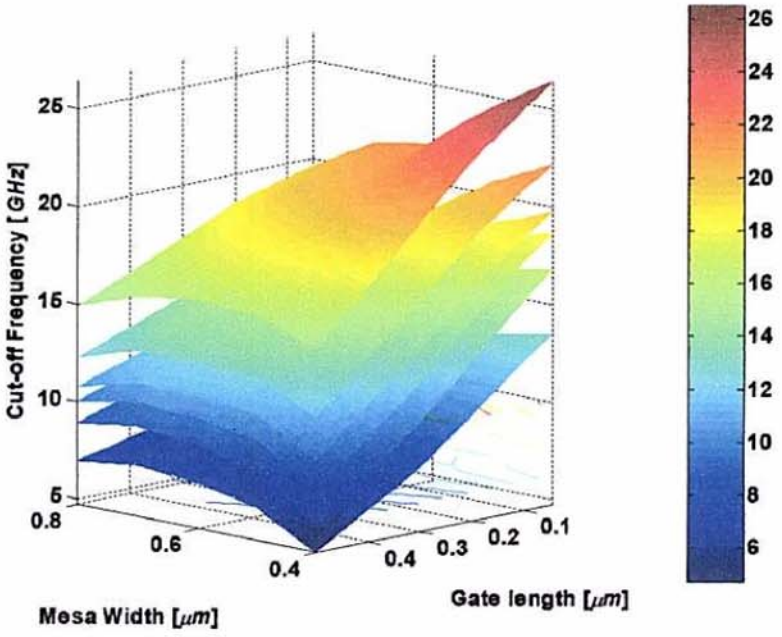


Figure 5.17 Cut-off frequency plotted as a function of gate length and mesa width for a bias point of $V_d = 25$ V, $V_g = 0$ V, Doping value *5.0e+16* cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

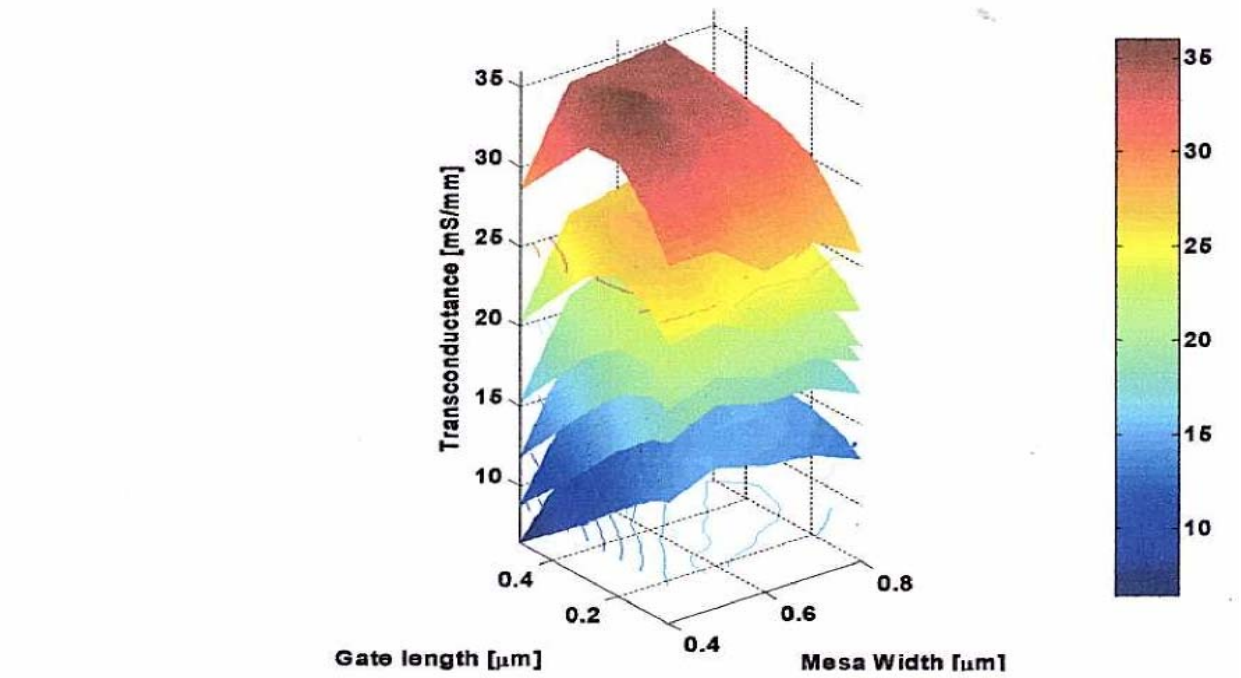


Figure 5.18 Transconductance plotted as a function of gate length and mesa width for a bias point of V_d = 25 V, V_g= 0 V, Doping value $5.0e+16\ cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

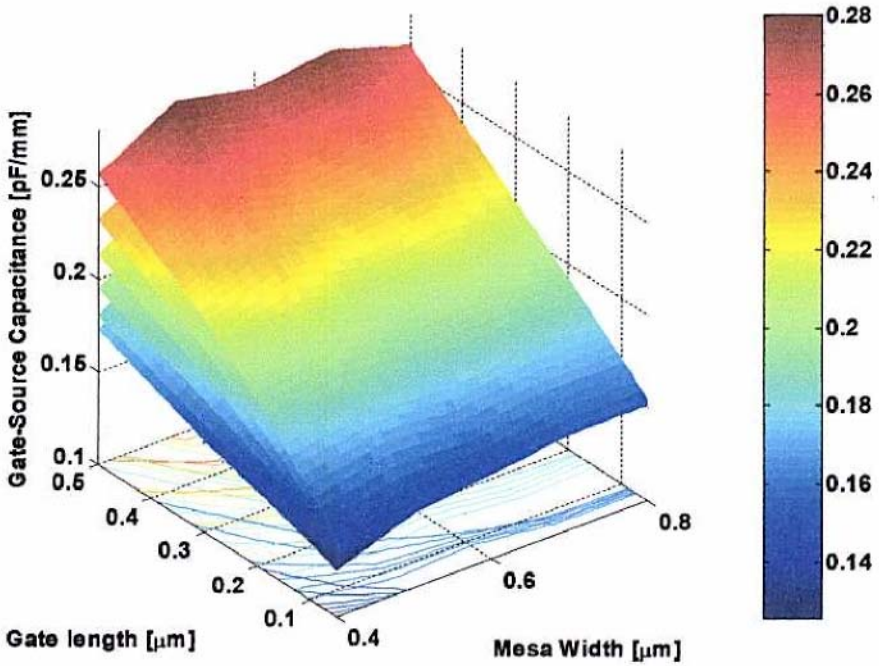


Figure 5.19 Gate-Source capacitance plotted as a function of gate length and mesa width for a bias point of V_d = 25 V, V_g = 0 V, Doping value $5.0e+16\ cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

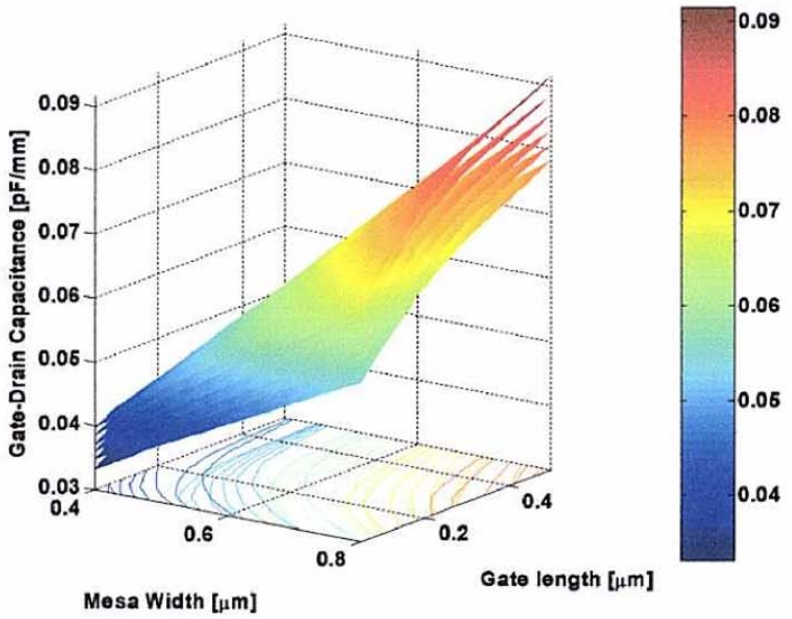


Figure 5.20Gate-Drain capacitance plotted as a function of gate length and mesa width for a bias point of $V_d = 25$ V, $V_g = 0$ V, Doping value *5.0e+16* cm^{-3}, from top to bottom curves, 800, 700, 600, 500, 400, 300 [K], respectively.

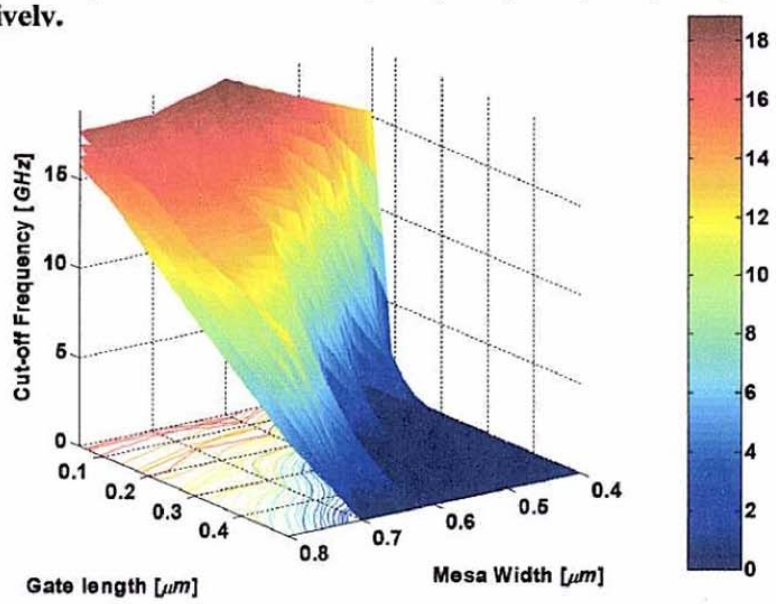


Figure 5.21Cut-off frequency plotted as a function of gate length and mesa width for a bias point of $V_d = 75$ V, $V_g = -10$ V, Doping value *5.0e+16* cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

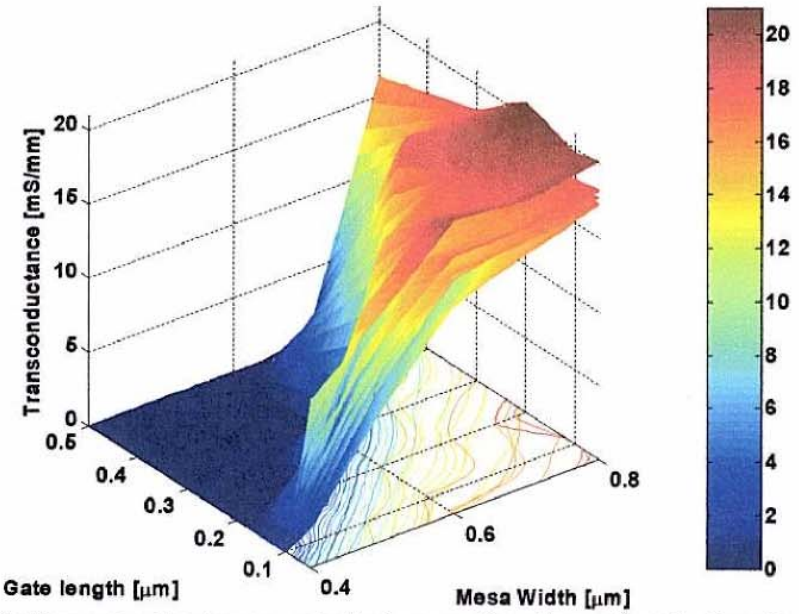


Figure 5.22 Transconductance plotted as a function of gate length and mesa width for a bias point of V_d = 75 V, V_g = -10 V, Doping value *5.0e+16* cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

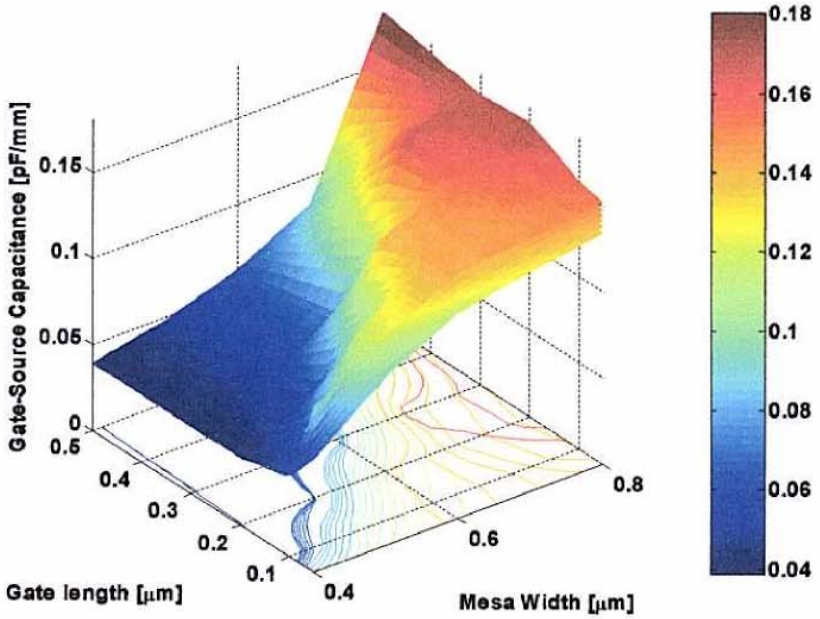


Figure 5.23 Gate-Source capacitance plotted as a function of gate length and mesa width for a bias point of V_d = 75 V, V_g = -10 V, Doping value *5.0e+16* cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

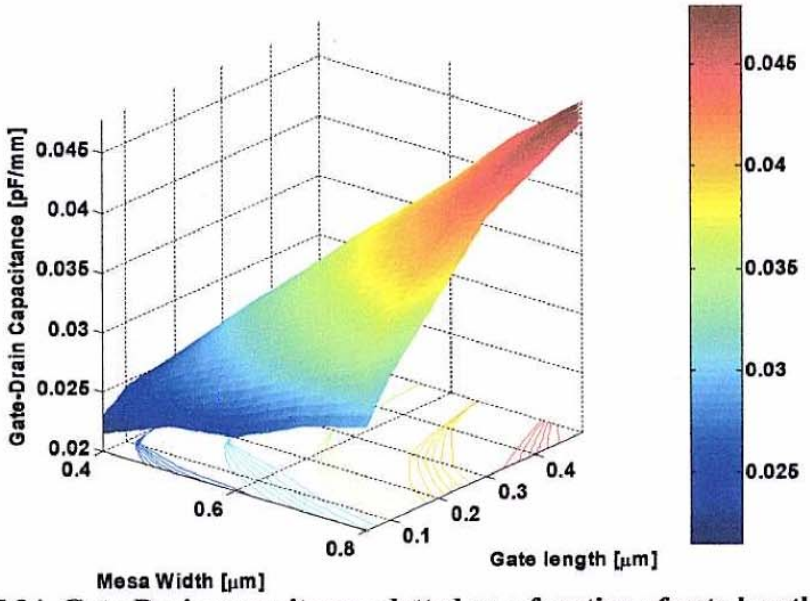


Figure 5.24 Gate-Drain capacitance plotted as a function of gate length and mesa width for a bias point of $V_d = 75$ V, $V_g = -10$ V, Doping value *5.0e+16 cm*$^{-3}$, from top to bottom curves, 800, 700, 600, 500, 400, 300 [K], respectively.

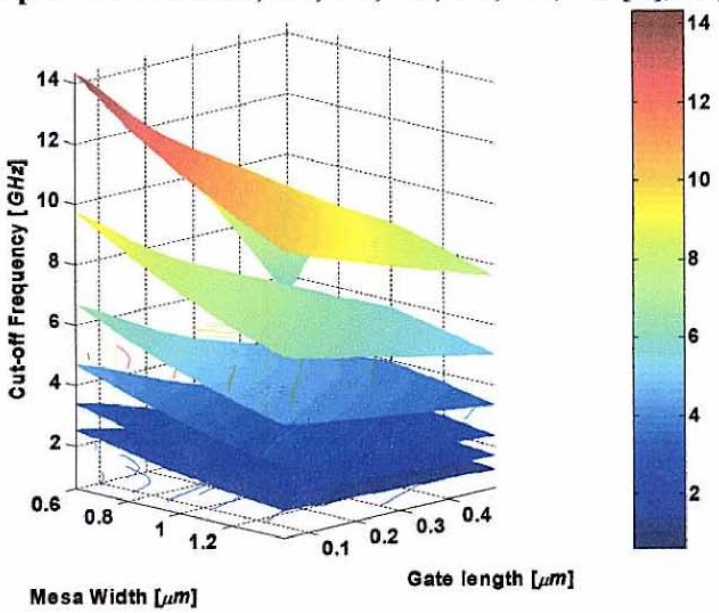


Figure 5.25 Cut-off frequency plotted as a function of gate length and mesa width for a bias point of $V_d = 10$ V, $V_g = 0$ V, Doping value *1.0e+16 cm*$^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

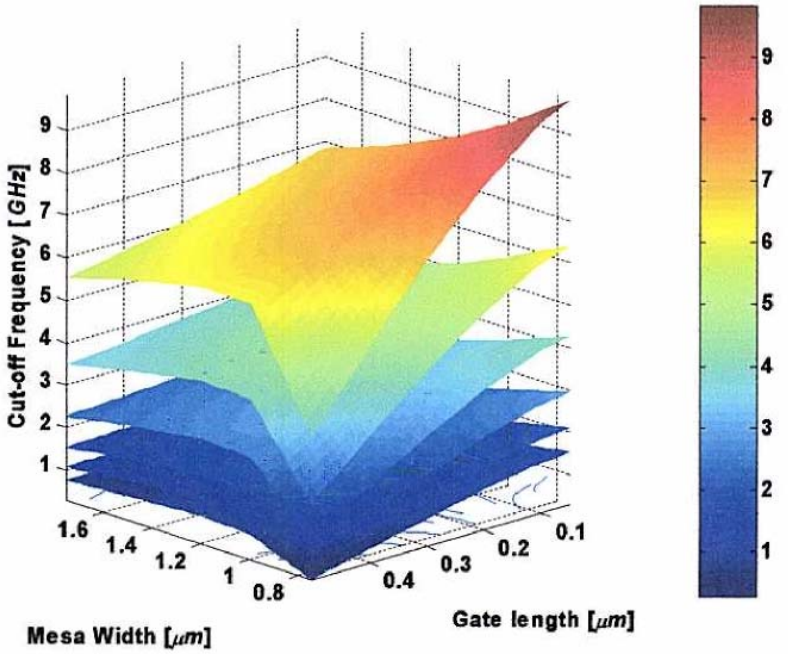


Figure 5.26 Cut-off frequency plotted as a function of gate length and mesa width for a bias point of $V_d = 10\ V$, $V_g = 0\ V$, Doping value $5.0e{+}15\ cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

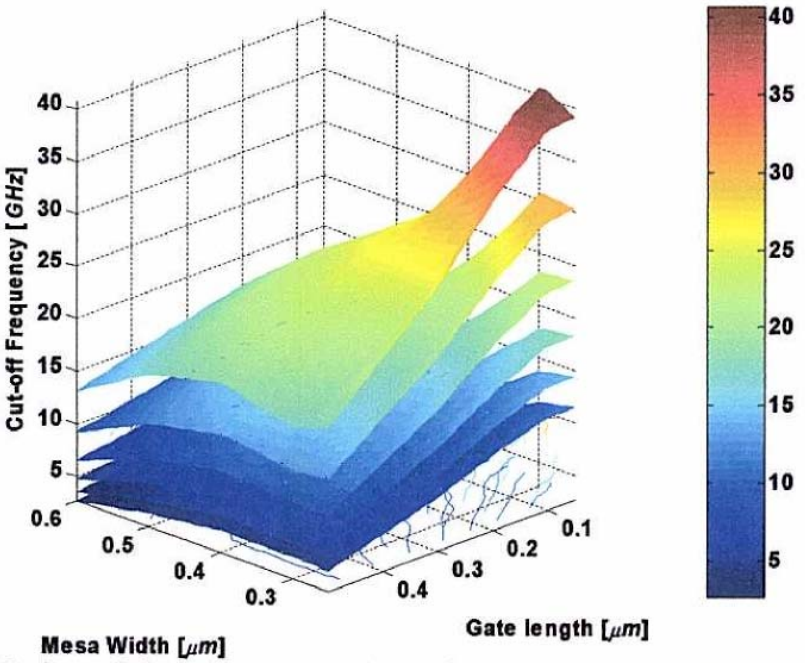


Figure 5.27 Cut-off frequency plotted as a function of gate length and mesa width for a bias point of $V_d = 10\ V$, $V_g = 0\ V$, Doping value $2.0e{+}17\ cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

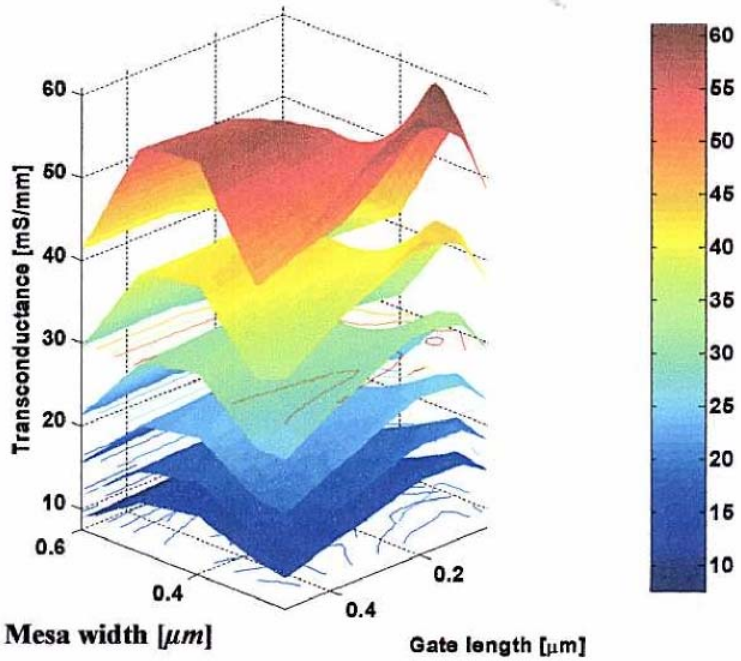


Figure 5.28 Transconductance plotted as a function of gate length and mesa width for a bias point of V_d = 10 V, V_g = 0 V, Doping value *2.0e+17* cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

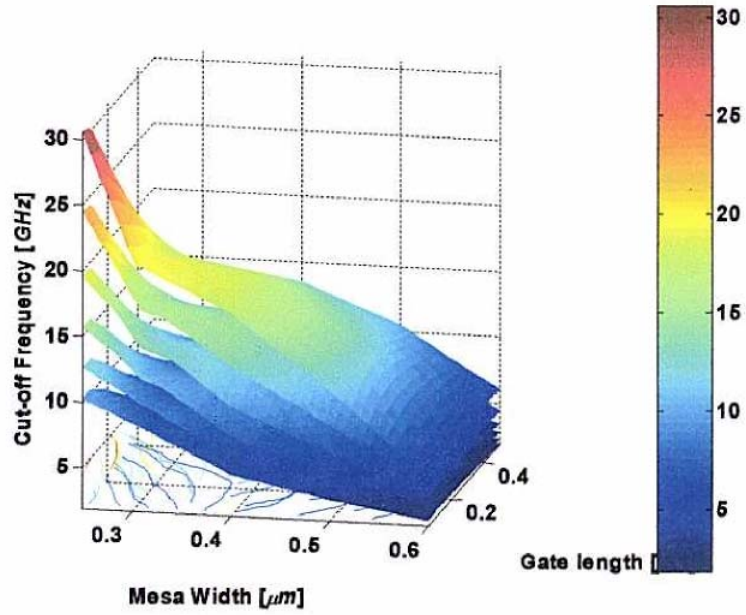


Figure 5.29 Cut-off frequency plotted as a function of gate length and mesa width for a bias point of V_d = 10 V, V_g = 0 V, Doping value *2.0e+17* cm^{-3}, with Source contact 5e-5 [Ωcm^2], from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

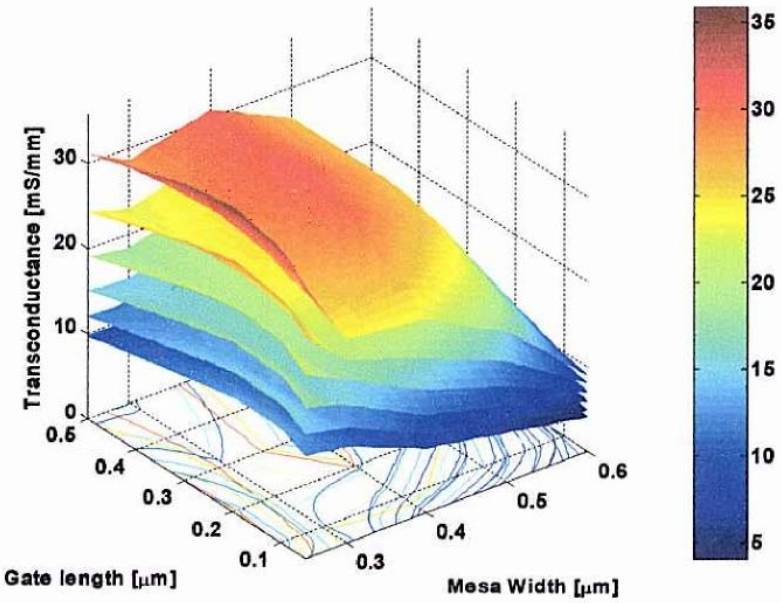


Figure 5.30 Transconductance plotted as a function of gate length and mesa width for a bias point of V_d = 10 V, V_g = 0 V, Doping value *2.0e+17* cm^{-3}, with source contact, 5e-5 [Ωcm^2], from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

In above results, as temperature is increased, f_T and g_m are decreased. At 800 K, g_m is about 20% of its value at 300 K. The monotonic decrease of transconductance is due to the decrease of the saturation current which is mainly a result of mobility degradation. At 800 K with doping *2.0e+17* cm^{-3}, f_T is about 13 *GHz* which is about 20% of its value at 300 K. Thus, f_T and g_m decrease to almost same rate.

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CHAPTER VI
CONCLUSION AND FUTURE WORK

1. Conclusion

The superior physical properties of SiC, such as wide band gap, high saturation electron velocity, low impact ionization rates, and high thermal conductivity, provide very promising candidates for high temperature, high power, high frequency, and radiation hard applications. The high blocking voltage, the low harmonics and the low internal modulation distortion (IMD) are the excellent features of SIT compared to those of BJT and FET. The current-voltage (I-*V*) transfer function (I_b to I_c) of BJT is the exponential, and the square law (V_g to I_d) of the conventional FET. In contrast to those of the BJT and FET, the low distortion amplifier was reported by virtue of its linear V_g - I_d characteristics of SIT. In this work, the static induction transistor (SIT) in SiC was investigated as a possible microwave device for high breakdown voltage and large bandwidth of operation. A large number of device structures were considered by means of simulations. The key design parameters are the mesa width 2*a* and L_g while maintaining adequate blocking gain. It is also shown that short gate lengths are needed for a high cut-off frequency and that a trade-off exists between frequency performance and current density.

The main approach to get higher cut-off frequency is to increase the doping in channel, and adjust the mesa width and gate length accordingly. Also, trench width is made very narrow. For the highest doping values, the smallest trench width is considered; a cut-off frequency of up to 42 *GHz* is predicted.

Actually, current high cut-off frequency devices do not reach theoretical best performance because of the source contact resistivity and the shrink source contact area with reduced mesa width. Contacts better than $1.5^{-5}\Omega cm^2$ are needed to reduce the effect of the source resistance. The large gate-drain capacitance of the SIT does not only reduce the cut-off frequency but more importantly, the input capacitance under realistic operating conditions is further increased due to the Miller effect.

The equivalent circuit was extracted from simulated Y-parameter as a function of bias, and it can be expanded to a large signal equivalent circuit. This circuit model was imported into a circuit simulation program to simulate load-pull results, and could also be used for circuit design.

The drain-gate breakdown voltage is limited by breakdown at the edge of the gate metal, unless an edge termination is employed. The edge termination of the gate seems to be of limited use because the drain-gate breakdown merely shifts to the inner trench corners, and the ultimate breakdown voltage is only slightly higher than in the unterminated device. However, it is still useful to terminate the gate edge, especially because the added processing is minimal and easy to perform. The breakdown with terminated gate is less abrupt, because a large leakage current signals that the maximum operating voltage is approached and the failure may be thermal an therefore time dependant. This made devices with termination more rebust during operation and testing.

The presented results demonstrate that simulations are accurate enough to be used as a design tool, and to establish a reference line against which measured device performance can be compared. It needs to be understood that the results for absolute numbers need to be interpreted with care, because the material parameters of SiC are not known well enough. They may even vary from lot to lot, to vendor to vendor, particularly when being compared with the control available in more mature material systems. A better knowledge base will emerge, once the commercialization of SiC based devices progresses further.

The two key advantages of the SIT are the high breakdown voltage and the high power density per area. Both of these advantages allow the SIT with large periphery for large output power. However, with increasing doping the advantages of a high breakdown voltage diminishes, the large breakdown voltage only helps on the output of the device. The bandwidth is limited by the large input capacitance due to C_{gd} and C_{gs}. Also, the inability to scale the device to large periphery at high frequencies diminishes the advantages of a large power per unit area. Therefore, a trade-off exists between high breakdown voltage and high frequency.

The SIT is the suitable device for the recent digital RF systems such as $\pi/4$ shifted quadric phase shift keying (QPSK) and quadric amplitude modulation (QAM) and broadband amplifier such as for the CATV.

2. Future Work

The neural networks have recently been introduced to the microwave area as a fast and flexible vehicle to microwave modeling, simulation and optimization. Also, in recent years, a new CAD approach based on neural network models has been introduced for microwave device design. It has been applied to the efficient modeling of devices, circuit and device optimization.

Even if today's simulations are powerful tools, they can only be as accurate as the mathematical models that are used. As a consequence, constructing good model for device used in circuits for circuits used in systems in a basic task.

There are three main factors that make the SIT devices less attractive in RF mobile applications. First, it is on normally-on characteristics, second, the large on-state voltage drop, and third, the need of using relatively high gate bias voltage [1]. To overcome this problem, neural network can be used. We obtain much SiC SIT data of properties and can be used for training neural network to it.

In neural network, adequate modeling of nonlinear RF devices still remains a complex but an avoidable step toward the achievement of a good design. And simulation boundary is very flexible.

Reference

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APPENDIX

A. MEDICI Programming Source Examples.

```
ASSIGN        NAME=vgmin      C.VAL=0.0
ASSIGN        NAME=vgstep     C.VAL=-2
ASSIGN        NAME=nvg        C.VAL=11
ASSIGN              NAME=vdmax      C.VAL=200
ASSIGN        NAME=Lsg        N.VALUE=0.5
ASSIGN        NAME=RDTH       N.VALUE=50
ASSIGN        NAME=MYSAT      N.VALUE=2.2E7
ASSIGN        NAME=RS       N.VALUE=1
ASSIGN        NAME=RD         N.VALUE=1

LOOP STEPS=6
   $ASSIGN  NAME=MYSAT N.VALUE=(1.5E7  2.0e7 2.2e7 2.5e7 )
   ASSIGN  NAME=TMP1 N.VALUE=(800 700 600 500 400 300)

 LOOP STEPS=5
     ASSIGN        NAME=Lgate      N.VALUE=(0.05 0.1 0.2 0.3 0.5)
$       ASSIGN        NAME=Lgate        N.VALUE=0.2

    LOOP STEPS=5
         ASSIGN   NAME=RS          N.VALUE=(0.5 1 5 10 50)

\       LOOP STEPS=5
          ASSIGN   NAME=RD          N.VALUE=(0.5 1 5 10 50)

         LOOP STEPS=5
          ASSIGN              NAME=d     N.VALUE=(1.75 1.5 1.2 1.0 0.75)
            ASSIGN            NAME=d     N.VALUE=1.2
            ASSIGN       NAME=T          N.VALUE= 1.5
            ASSIGN       NAME=t          N.VALUE= @d
            ASSIGN       NAME=pitch      N.VALUE= @d+@t
             CALL FILE="acNd3_The_elec_RSRD_1.md"

      L.END
    L.END
  L.END
  L.END
  L.END

STOP
```

```
<<acNd3_The_elec_RSRD_1>>

TITLE     SIC SIT Temperature Simulation
COMMENT   finds the DC and small signal AC parameters

CALL FILE="Mobn.md"

ASSIGN        NAME=MYMAX     N.VALUE=@Mumax
ASSIGN        NAME=MYMIN     N.VALUE=@Mumin
ASSIGN        NAME=MYCON     N.VALUE=@NNref

MESH    OUT.FILE="../../../Mesh/break_"@Str".mesh"

X.MESH          X.MIN = 0.0       WIDTH=@d/2     H1=0.1
X.MESH          X.MIN = @d/2      WIDTH=@t/2              H1=0.1
Y.MESH          Y.MIN=-0.5        DEPTH=0.5      H1=0.1   H2=0.05
Y.MESH          DEPTH=@Lsg        H1=0.1    H2=0.025
Y.MESH          DEPTH=@Lgate      H1=0.025
Y.MESH          DEPTH=@Ld1        H1=0.1    H2=0.25


REGION          NAME=SiC SIC
REGION          NAME=n_plus_SiC          SIC       Y.MAX=0.0
REGION          NAME=air INSULATO
+         X.MIN=@d/2      X.MAX=@pitch/2 Y.MIN=-0.5 Y.MAX=@Lsg+@Lgate/2


ELECTR    NAME=source  X.MAX=@d/2      TOP
ELECTR    NAME=gate     VOID X.MIN=@d/2          X.MAX=@pitch/2
+                       Y.MIN=@Lsg Y.MAX=@Lsg+@Lgate
ELECTR    NAME=drain    BOTTOM
ELECTR    NAME=drainth BOTTOM          THERMAL

PROFILE   N-TYPE        UNIFORM        N.PEAK=@ND  OUT.FILE="../../../Mesh/break_"@Str".pro"
PROFILE   N-TYPE        UNIFORM        N.PEAK=1.2E19
+          Y.MAX=0.0

CONTACT    NAME=gate   WORKFUNC=5.2          BARRIERL
CONTACT    NAME=source    CON.RESI=@RS*(@d*1E-5)
CONTACT    NAME=drain           CON.RESI=(@pitch/2)*(@RD*1E-5)
CONTACT    NAME=drainth         R.THERMA=@RDTH*1E3

CALL FILE="4h-SiC_pur_my.md"

MATERIAL        INSULATO        PERMITTI=1.0


MODEL   FERMIDIR INCOMPLE ANALYTIC  FLDMOB TEMPERAT=300
SYMBOL     CARRIERS=1
METHOD    CONT.STK
SOLVE   INI

REGRID   POTEN IGNORE=air RATIO=.1 MAX=1 SMOOTH=1
+ IN.FILE="../../../Mesh/break_"@Str".pro"
+ OUT.FILE="../../../Mesh/break_"@Str".mesh"

REGRID    DOPING LOG IGNORE=air RATIO=2
+ IN.FILE="../../../Mesh/break_"@Str".pro"
+ OUT.FILE="../../../Mesh/break_"@Str".mesh"
```

```
PLOT.2D  GRID TITLE="Lg="@Lgate",d="@d",Ld1="@Ld1",Nd="@ND
+        BOUNDARY DEPLETIO FILL SCALE T.SIZE=0.15
$ +        DEVICE=CP  PLOT.OUT="psfiles/"@device".ps"
PLOT.1D  DOPING TITLE="Doping at x=0 "@device"  "
+        X.START=0.0 X.END=0.0 Y.START=-0.5   Y.END=@Lsg+@Lgate+@Ld1
+        LOGARITH  T.SIZE=0.2

COMMENT    Compute equilibrium solution as initial guess
LOG                OUT.FILE="../../../temp/"@device".log"
SYMBOL     CARRIERS=1 NEWTON
METHOD   STACKS=20  CONT.STK
SOLVE      V(gate)=0.0    V(source)=0.0  V(drain)=0.0

REGRID   POTEN  IGNORE=air  RATIO=.05  MAX=1  SMOOTH=1
+ IN.FILE="../../../Mesh/break_"@Str".pro"
+ OUT.FILE="../../../Mesh/break_"@Str".mesh"


SYMBOL    CARRIERS=1 NEWTON   ELECTRONS  COUP.LAT

METHOD   STACKS=20  CONT.STK
SOLVE      V(gate)=0.0    V(source)=0.0  V(drain)=0.0

LOG                OUT.FILE="../../../log/"@device".log"

SOLVE      V(gate)=@vgmin  ELECTROD=gate VSTEP=@vgstep NSTEP=@nvg-1
+          OUT.FILE="../../../Gate_Sol/"@Str"_00"  SAVE.BIA


CALL FILE="biaspoint_Temp_AC_anal.md"
```

```
<< Mobn.md>>
COMMENT  Mobility Caculation -- Depend on Temperature.

ASSIGN NAME=Mumax  N.VALUE=950*(@TMP1/300)**(-2.4)
ASSIGN NAME=Mumin  N.VALUE=40*(@TMP1/300)**(-0.5)
ASSIGN NAME=NNref   N.VALUE=2E17*(@TMP1/300)
ASSIGN NAME=alpha   N.VALUE=0.76
ASSIGN NAME=Tbeta   N.VALUE=0.816
ASSIGN NAME=aa    N.VALUE=4.27E-2
ASSIGN NAME=bb    N.VALUE=98.4
ASSIGN NAME=tt    N.VALUE=327
ASSIGN NAME=beta    N.VALUE=@Tbeta+@aa*exp((@TMP1-@tt)/@bb)


<< biaspoint_Temp_AC_anal.md>>

TITLE Bias point

ASSIGN   NAME=vgac   C.VAL=-0.0
ASSIGN   NAME=vdac   C.VAL=10
ASSIGN   NAME=startsol C.VAL=00
CALL FILE="biasplot_Temp_AC_anal_RSRD.md"

ASSIGN   NAME=vgac   C.VAL=0.0
ASSIGN   NAME=vdac   C.VAL=25
ASSIGN   NAME=startsol C.VAL=00
CALL FILE="biasplot_Temp_AC_anal_RSRD.md"

ASSIGN   NAME=vgac   C.VAL=-4.0
ASSIGN   NAME=vdac   C.VAL=50
ASSIGN   NAME=startsol C.VAL=02
CALL FILE="biasplot_Temp_AC_anal_RSRD.md"

ASSIGN   NAME=vgac   C.VAL=-6.0
ASSIGN   NAME=vdac   C.VAL=75
ASSIGN   NAME=startsol C.VAL=03
CALL FILE="biasplot_Temp_AC_anal_RSRD.md"

ASSIGN   NAME=vgac   C.VAL=-10.0
ASSIGN   NAME=vdac   C.VAL=75
ASSIGN   NAME=startsol C.VAL=05
CALL FILE="biasplot_Temp_AC_anal_RSRD.md"

ASSIGN   NAME=vgac   C.VAL=-4.0
ASSIGN   NAME=vdac   C.VAL=35
ASSIGN   NAME=startsol C.VAL=03
CALL FILE="biasplot_Temp_AC_anal_RSRD.md"
```

```
<< biasplot_Temp_AC_anal_RSRD.md>>

COMMENT Small signal parameters for Vd=vdac , Vg=vgac

TITLE "VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d" Temp="@TMP1 T.SIZE=0.2

LOAD   IN.FILE="../../../Gate_Sol/"@Str"_"@startsol

METHOD STACK=20 CONT.STK

LOG   OUT.FILE="../../../temp/"@device".log_NC"

SOLVE  V(source)=0  V(gate)=@vgac  V(drain)=@vdac

PLOT.2D TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1""
T.SIZE=0.2
+ BOUNDARY DEPLETIO FILL
$+  DEVICE=CP
PLOT.OUT="../../../psfiles/Temp_"@Str"_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@RS"_"@RD".ps"

SOLVE V(source)=0.0 V(drain)=@vdac  V(gate)=@vgac
+     AC.ANALY FREQUENC=0.5E9  HI.FREQ  FSTEP=0.5E9 NFSTEP=20

PLOT.1D  IN.FILE="../../../temp/"@device".log_NC"  X.AXIS=freq
+ Y.AXIS="G(gate,gate)"  X.LOG Y.LOG TITLE="VD="@vdac"[V],  VG="@vgac"[v] Str="@Str" Lg="@Lgate"
d="@d" Temp="@TMP1"" T.SIZE=0.2
+OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".ggg"
$ PLOT.OUT="../../../psfiles/Temp_"@Str"_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_NoContator.ps"

PLOT.1D  IN.FILE="../../../temp/"@device".log_NC"        X.AXIS=freq
+ Y.AXIS="G(drain,drain)"  X.LOG Y.LOG TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate"
d="@d"Temp="@TMP1"" T.SIZE=0.2
+
OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".gdd"

PLOT.1D            IN.FILE="../../../temp/"@device".log_NC"          X.AXIS=freq
+ Y.AXIS="G(drain,gate)"  X.LOG Y.LOG TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate"
d="@d"Temp="@TMP1"" T.SIZE=0.2
+
OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".gdg"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"         X.AXIS=freq
+ Y.AXIS="G(gate,drain)" X.LOG Y.LOG TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate"
d="@d"Temp="@TMP1"" T.SIZE=0.2
+
OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".ggd"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"         X.AXIS=freq
+ Y.AXIS="G(drain,source)"  X.LOG Y.LOG TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate"
d="@d"Temp="@TMP1"" T.SIZE=0.2
+
OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".gds"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"         X.AXIS=freq
+ Y.AXIS="G(source,drain)"  X.LOG Y.LOG
+ TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1"" T.SIZE=0.2
+OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".gsd"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"         X.AXIS=freq
```

```
+            Y.AXIS="C(gate,drain)" X.LOG
+ TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1"" T.SIZE=0.2
+OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".cgd"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"        X.AXIS=freq
+            Y.AXIS="C(gate,source)" X.LOG
+ TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1"" T.SIZE=0.2
+ OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".cgs"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"        X.AXIS=freq
+            Y.AXIS="C(drain,source)" X.LOG
+ TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1"" T.SIZE=0.2
+ OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".cds"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"        X.AXIS=freq
+            Y.AXIS="C(gate,gate)" X.LOG
+ TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1"" T.SIZE=0.2
+
OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".cgg"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"        X.AXIS=freq
+            Y.AXIS="C(source,drain)"  X.LOG
+ TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1"" T.SIZE=0.2
+ OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".csd"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"        X.AXIS=freq
+            Y.AXIS="C(gate,source)"  X.LOG Y.LOG ABSOLUTE
+OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".cgs1
"
PLOT.1D IN.FILE="../../../temp/"@device".log_NC"        X.AXIS=freq
+            Y.AXIS="Y(gate,drain)" X.LOG Y.LOG ABSOLUTE
+ TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1"" T.SIZE=0.2
+
OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".y12"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"        X.AXIS=freq
+            Y.AXIS="Y(drain,drain)" X.LOG Y.LOG ABSOLUTE
+ TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1"" T.SIZE=0.2
+
OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".y22"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"        X.AXIS=freq
+            Y.AXIS="Y(gate,gate)" X.LOG Y.LOG ABSOLUTE
+ TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1"" T.SIZE=0.2
+
OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".y11"
PLOT.1D IN.FILE="../../../temp/"@device".log_NC"        X.AXIS=freq
+            Y.AXIS="Y(drain,gate)" X.LOG Y.LOG ABSOLUTE
+ TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1"" T.SIZE=0.2
+
OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".y21"

PLOT.1D IN.FILE="../../../temp/"@device".log_NC"        X.AXIS=freq
+            Y.AXIS="Y(source,drain)"  X.LOG Y.LOG ABSOLUTE
+ TITLE="VD="@vdac"V,  VG="@vgac"v Str="@Str" Lg="@Lgate" d="@d"Temp="@TMP1"" T.SIZE=0.2
+
OUT.FILE="../../../Results_ac_"@Str"/Temp_"@TMP1"_"@MYSAT"_"@Lgate"_"@d"_"@startsol"_"@vdac".ysd"

STOP
```

B. MATLAB Example Sources

```
<<Temp_freq_Str_all_cal.m>>
close all
clear all
format long g

% Structure type
%for Str=1:4
Str=1;
   LLg = zeros(6,4,4);
   DDl = zeros(6,4,4);
   CCgs = zeros(6,4,4);
   CCgd = zeros(6,4,4);
   FFt = zeros(6,4,4);

% Concentration Nd
o=Str;

% Velocity drift saturation
p=5;
rs=2;rd=2;
%m=1;
%for rs=1:4

if Str==1
   d= [1.75 1.5 1.2 1.0];
   elseif Str==2
      d=[1.2 1 0.8 0.6];
   elseif Str==3
         d= [0.8 0.7 0.6 0.5 0.4];
   else
         d= [0.6 0.5 0.4 0.3 0.25];
 end

 Vsat=['1.0E+07'; '1.5E+07';'2.0E+07';'2.2E+07';'2.5E+07'];
 L=['0.50000'; '0.20000'; '0.10000'; '5.0e-02'];
 Tempr=['300';'400';'500';'600';'700';'800'];
 Nd=['5.0e+15'; '1.0e+16'; '5.0e+16';'2.0e+17'];

 RS=[0.5 1 5 10];
 RD=[0.5 1 5 10];

 for tt=1:6
    i=0;
   for n=1:5
      for m=1:5
        i=i+1;

if n==5
   F1=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' L(n,:) '_' num2str(d(m))
'_NoContator_' num2str(RS(rs)) '.y11']);
          F2=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' L(n,:) '_' num2str(d(m))
'_NoContator_' num2str(RS(rs)) '.y12']);
          F3=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' L(n,:) '_' num2str(d(m))
'_NoContator_' num2str(RS(rs)) '.y21']);
          F4=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' L(n,:) '_' num2str(d(m))
'_NoContator_' num2str(RS(rs)) '.y22']);
```

```
        F5=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' L(n,:) '_' num2str(d(m))
'_NoContator_' num2str(RS(rs)) '.cgd']);
        F6=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' L(n,:) '_' num2str(d(m))
'_NoContator_' num2str(RS(rs)) '.cgs']);
        F7=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' L(n,:) '_' num2str(d(m))
'_NoContator_' num2str(RS(rs)) '.gds']);
else
  F1=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' num2str(str2num(L(n,:))) '_'
num2str(d(m)) '_NoContator_' num2str(RS(rs)) '.y11']);
        F2=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' num2str(str2num(L(n,:))) '_'
num2str(d(m)) '_NoContator_' num2str(RS(rs)) '.y12']);
        F3=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' num2str(str2num(L(n,:))) '_'
num2str(d(m)) '_NoContator_' num2str(RS(rs)) '.y21']);
        F4=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' num2str(str2num(L(n,:))) '_'
num2str(d(m)) '_NoContator_' num2str(RS(rs)) '.y22']);
        F5=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' num2str(str2num(L(n,:))) '_'
num2str(d(m)) '_NoContator_' num2str(RS(rs)) '.cgd']);
        F6=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' num2str(str2num(L(n,:))) '_'
num2str(d(m)) '_NoContator_' num2str(RS(rs)) '.cgs']);
        F7=(['../../Tempr/Results_ac_' num2str(Str) '/Temp_' Tempr(tt,:) '_' Vsat(p,:) '_' num2str(str2num(L(n,:))) '_'
num2str(d(m)) '_NoContator_' num2str(RS(rs)) '.gds']);
end

[fid1,err1]=fopen(F1,'r');
[fid2,err1]=fopen(F2,'r');
[fid3,err1]=fopen(F3,'r');
[fid4,err1]=fopen(F4,'r');
[fid5,err1]=fopen(F5,'r');
[fid6,err1]=fopen(F6,'r');
[fid7,err1]=fopen(F7,'r');

S11 = fscanf(fid1,'%s',15);
S12 = fscanf(fid2,'%s',15);
S13 = fscanf(fid3,'%s',15);
S14 = fscanf(fid4,'%s',15);
S15 = fscanf(fid5,'%s',15);
S16 = fscanf(fid6,'%s',15);
S17 = fscanf(fid7,'%s',15);

S41 = fscanf(fid1, '%16e',[2 inf]);
S42 = fscanf(fid2, '%16e',[2 inf]);
S43 = fscanf(fid3, '%16e',[2 inf]);
S44 = fscanf(fid4, '%16e',[2 inf]);
S45 = fscanf(fid5, '%16e',[2 inf]);
S46 = fscanf(fid6, '%16e',[2 inf]);
S47 = fscanf(fid7, '%16e',[2 inf]);

fclose(fid1);fclose(fid2);fclose(fid3);fclose(fid4);fclose(fid5);
fclose(fid6);fclose(fid7);

S21=('Frequency GHz');
S31=('Conductance(pF/mm)');

y1 = S41(2,:);
y2 = S42(2,:);
y3 = S43(2,:);
y4 = S44(2,:);
y5 = S45(2,:);
y6 = S46(2,:);
```

```
y7 = S47(2,:);

x1 = (S41(1,:));
x2 = (S42(1,:));
x3 = (S43(1,:));
x4 = (S44(1,:));
x5 = (S45(1,:));
x6 = (S46(1,:));
x7 = (S47(1,:));

f=x1;
w=f.*2*pi;

yi=y1-y2;
yo=y3-y2;
yr=-y2;
yf=y3-y2;

Cgd=yr./w;
Cgs=-yi./w;
Y12=complex(0,-w.*y5);
gm1=y3+w.*y5;
gm2=abs(yf);
gds=abs(yo);
n5=length(y5);

Lg=str2num(L(n,:));Lg;
DD=num2str(d(m));DD;
nn=length(gm1);
gm11=(sum(gm1)/nn)*1e6;
gm22=(sum(gm2)/nn)*1e6;
n5=length(y5);
Cgd11 =(sum(abs(y5(2:n5)))/(nn-1)).*1e15;
Cgd22 =(sum(abs(Cgd(2:n5)))/(nn-1)).*1e15;
Cgs11 =(sum(abs(y6(2:n5)))/(nn-1)).*1e15;
Cgs22 =(sum(abs(Cgs(2:n5)))/(nn-1)).*1e15;
Ft1=gm11/(2*pi*(Cgs11+Cgd11));
Ft2=gm22/(2*pi*(Cgs22+Cgd22));
LLg1(tt,n,m) = Lg;
DDl1(tt,n,m) = str2num(DD);
GGm1(tt,n,m) = gm22;
CCgs1(tt,n,m) = Cgs22;
CCgd1(tt,n,m) = Cgd22;
FFt1(tt,n,m) = Ft1;
VVsat(tt,n,m) = str2num(Vsat(p,:));
%disp('=============================================');
end
end
end

fclose all;
Filename = (['d:/Research/DaTa/Frequency/NoContact/freq_Str_' num2str(Str) '.mat']);
save(Filename, 'VVsat', 'LLg1', 'DDl1', 'GGm1', 'CCgs1', 'CCgd1', 'FFt1','RS');

%end
%end
disp('=============================================');
disp('==============Str_all_Cal==============');
```

```
<< Temp_freq_Str.m>>

%
% Include contact Resistor
%

close all
clear all
format long g


% d is 3 steps

Lg=zeros(1,5);
Tempr=['300';'400';'500';'600';'700';'800'];
 Vsat=['1.0E+07';'1.5E+07';'2.0E+07';'2.2E+07';'2.5E+07'];
 RS=[0.5 1 5 10 50];
 RD=[0.5 1 5 10 50];
 Nd=['5.0e+15'; '1.0e+16'; '5.0e+16';'2.0e+17'];
 Bias=[.0, 10; 0.0, 25; -4, 50; -6.0, 75; -10.0, 75; -4.0, 35];
 vgac=Bias(:,1)';
 vdac=Bias(:,2)';

 Str=4;
BA=1;
rs=2;rd=2;

 if Str==1
   d= [1.75 1.5 1.2 1.0 0.75];
  elseif Str==2
      d=[1.4 1.2 1 0.8 0.6];
  elseif Str==3
        d= [0.8 0.7 0.6 0.5 0.4];
  else
        d= [0.6 0.5 0.4 0.3 0.25];
     end

     fi=1;
     ii=1;

 for tt=1:6

     Filename = (['g:\Tempr\\Data\freq_Str_' num2str(Str) '_' num2str(Tempr(tt,:)) '_' num2str(BA) '-' num2str(RS(rs))
'_' num2str(RD(rd)) '.mat']);
     load(Filename, '-mat');

     Lg =LLg(:,1)';
     d =DDl(1,:);
     evalc(['Ft_' num2str(Tempr(tt,:)) '=FFt']);
     evalc(['Gm1_' num2str(Tempr(tt,:)) ' =GGm']);
     evalc(['Cgs1_' num2str(Tempr(tt,:)) ' =CCgs']);
     evalc(['Cgd1_' num2str(Tempr(tt,:)) ' =CCgd']);
     evalc(['Vsat =VVsat']);


%RS = RS.*10^-5;

N=40;
```

```
N1=40;
nx1=(d(1) - d(5))/N;
ny1=(Lg(1) - Lg(5))/N;
ny2 = (RS(1,5) - RS(1,1))/N1;


[x1,y1] = meshgrid( d(1):-nx1:d(5), Lg(1):-ny1:Lg(5));
[x2,y2] = meshgrid( Lg(1):-ny1:Lg(5), RS(1,1):ny2:RS(1,5));
[x3,y3] = meshgrid( d(1):-nx1:d(5), RS(1,1):ny2:RS(1,5));

evalc(['zi1_' num2str(Tempr(tt,:)) ' = interp2(d, Lg, Ft_' num2str(Tempr(tt,:)) ', x1, y1)' ]);

% change data structure
% evalc(['Ft1_' num2str(m) '_RS(:,rs) = Ft_' num2str(m) '_T_' num2str(rs) '(:,3)']);
% evalc(['Ft2_' num2str(m) '_RS(rs,:) = Ft_' num2str(m) '_T_' num2str(rs) '(3,:)']);


figure(1);

evalc(['surfc(x1, y1, zi1_' num2str(Tempr(tt,:)) ')']);
% evalc(['[XX11, YY11] = max(zi1' num2str(rs) ')']);
% evalc(['ZZi=zi1' num2str(rs)]);
% text(XX11,YY11, ZZi, ['Maxf_t=', num2str(RS(rs)) ]);
hold on
xlabel('Mesa Width [{\it\mum}]');
ylabel('Gate length [{\it\mum}]');
zlabel(' Cut-off Frequency [{\itGHz}]');

colorbar
axis tight
axis vis3d
shading interp

figure(300);
subplot(2,3,fi)
evalc(['surfc(x1, y1, zi1_' num2str(Tempr(tt,:)) ')']);
hold on

if fi==1
xlabel('Mesa Width [{\it\mum}]');
ylabel('Gate length [{\it\mum}]');
zlabel(' Cut-off Frequency [{\itGHz}]');
title([' Temperature = ' num2str(Tempr(tt,:)) ',[{\itK}]'],'Color','r')
end
if fi ==2
   title([ num2str(Tempr(tt,:)) ',[{\itK}]'],'Color','r')
end
if fi ==3
   title([ num2str(Tempr(tt,:)) ',[{\itK}]'],'Color','r')
end
if fi ==4
   title([ num2str(Tempr(tt,:)) ',[{\itK}]'],'Color','r')
end
if fi ==5
   title([ num2str(Tempr(tt,:)) ',[{\itK}]'],'Color','r')
end
colorbar
axis tight
axis vis3d
```

```
shading interp
fi=fi+1;
evalc(['zi4' num2str(Tempr(tt,:)) ' = interp2(d, Lg, Ft_' num2str(Tempr(tt,:)) ', x1, y1)' ]);
evalc(['zi5' num2str(Tempr(tt,:)) ' = interp2(d , Lg, Gm1_' num2str(Tempr(tt,:)) ', x1, y1)' ]);
evalc(['zi6' num2str(Tempr(tt,:)) ' = interp2(d, Lg, Cgs1_' num2str(Tempr(tt,:)) ', x1, y1)' ]);
evalc(['zi7' num2str(Tempr(tt,:)) ' = interp2(d, Lg, Cgd1_' num2str(Tempr(tt,:)) ', x1, y1)' ]);

figure(60);
evalc(['surfc(x1, y1, zi7' num2str(Tempr(tt,:)) ')']);
hold on
xlabel('Mesa Width [\mum]');
ylabel('Gate length [\mum]');
zlabel(' Gate-Drain Capacitance [pF/mm]');
%title([' Temperature = ' num2str(Tempr(tt,:)) '[K]'],'Color','r');
colorbar
axis tight
%axis([0.05 0.5 (0.5*10^-5) (10*10^-5) 6 14]);
axis vis3d
shading interp

figure(70);
evalc(['surfc(x1, y1, zi6' num2str(Tempr(tt,:)) ')']);
hold on
xlabel('Mesa Width [\mum]');
ylabel('Gate length [\mum]');
zlabel(' Gate-Source Capacitance [pF/mm]');
%title([' Temperature = ' num2str(Tempr(tt,:)) '[K]'],'Color','r');
colorbar
axis tight
%axis([0.05 0.5 (0.5*10^-5) (10*10^-5) 6 14]);
axis vis3d
shading interp

figure(71);
subplot(2,3,ii)
evalc(['surfc(x1, y1, zi6' num2str(Tempr(tt,:)) ')']);
hold on
xlabel('Mesa Width [\mum]');
ylabel('Gate length [\mum]');
zlabel(' Gate-Source Capacitance [pF/mm]');
%title([' Temperature = ' num2str(Tempr(tt,:)) '[K]'],'Color','r');
colorbar
axis tight
%axis([0.05 0.5 (0.5*10^-5) (10*10^-5) 6 14]);
axis vis3d
shading interp


figure(75);
evalc(['surfc(x1, y1, zi7' num2str(Tempr(tt,:)) ')']);
hold on
xlabel('Mesa Width [\mum]');
ylabel('Gate length [\mum]');
zlabel(' Gate-Drain Capacitance [pF/mm]');
%title([' Temperature = ' num2str(Tempr(tt,:)) '[K]'],'Color','r');
colorbar
axis tight
%axis([0.05 0.5 (0.5*10^-5) (10*10^-5) 6 14]);
axis vis3d
```

```
shading interp

figure(76);
subplot(2,3,ii)
evalc(['surfc(x1, y1, zi7' num2str(Tempr(tt,:)) ')']);
hold on
xlabel('Mesa Width [\mum]');
ylabel('Gate length [\mum]');
zlabel(' Gate-Drain Capacitance [pF/mm]');
%title([' Temperature = ' num2str(Tempr(tt,:)) '[K]'],'Color','r');
colorbar
axis tight
%axis([0.05 0.5 (0.5*10^-5) (10*10^-5) 6 14]);
axis vis3d
shading interp

figure(80);
evalc(['surfc(x1, y1, zi5' num2str(Tempr(tt,:)) ')']);
hold on
xlabel('Mesa Width [\mum]');
ylabel('Gate length [\mum]');
zlabel(' Transconductance [mS/mm]');
%title([' Temperature = ' num2str(Tempr(tt,:)) '[K]'],'Color','r');
colorbar
axis tight
axis vis3d
shading interp

figure(81);
subplot(2,3,ii)
evalc(['surfc(x1, y1, zi5' num2str(Tempr(tt,:)) ')']);

if ii==1
xlabel('Mesa Width [\mum]');
ylabel('Gate length [\mum]');
zlabel(' Transconductance [mS/mm]');

title([' Temperature = ' num2str(Tempr(tt,:)) ',[K]'],'Color','r')

else
   title([ num2str(Tempr(tt,:)) ',[K]'],'Color','r')
end

%title([' Temperature = ' num2str(Tempr(tt,:)) '[K]'],'Color','r');
colorbar
axis tight
axis vis3d
shading interp

figure(90+ii);
evalc(['surfc(x1, y1, zi4' num2str(Tempr(tt,:)) ')']);
xlabel('Mesa Width [\mum]');
ylabel('Gate length [\mum]');
zlabel(' Cut-off Frequency [GHz]');
title([' Temperature = ' num2str(Tempr(tt,:)) '[K]'],'Color','r');
colorbar
axis tight
%axis([0.05 0.5 (0.5*10^-5) (10*10^-5) 6 14]);
axis vis3d
```

```
shading interp
ii=ii+1;
end

fclose all;
 hold off;
disp('=========================================');
disp('=========================================');
```

C. Simulation Results for I-V Characteristics

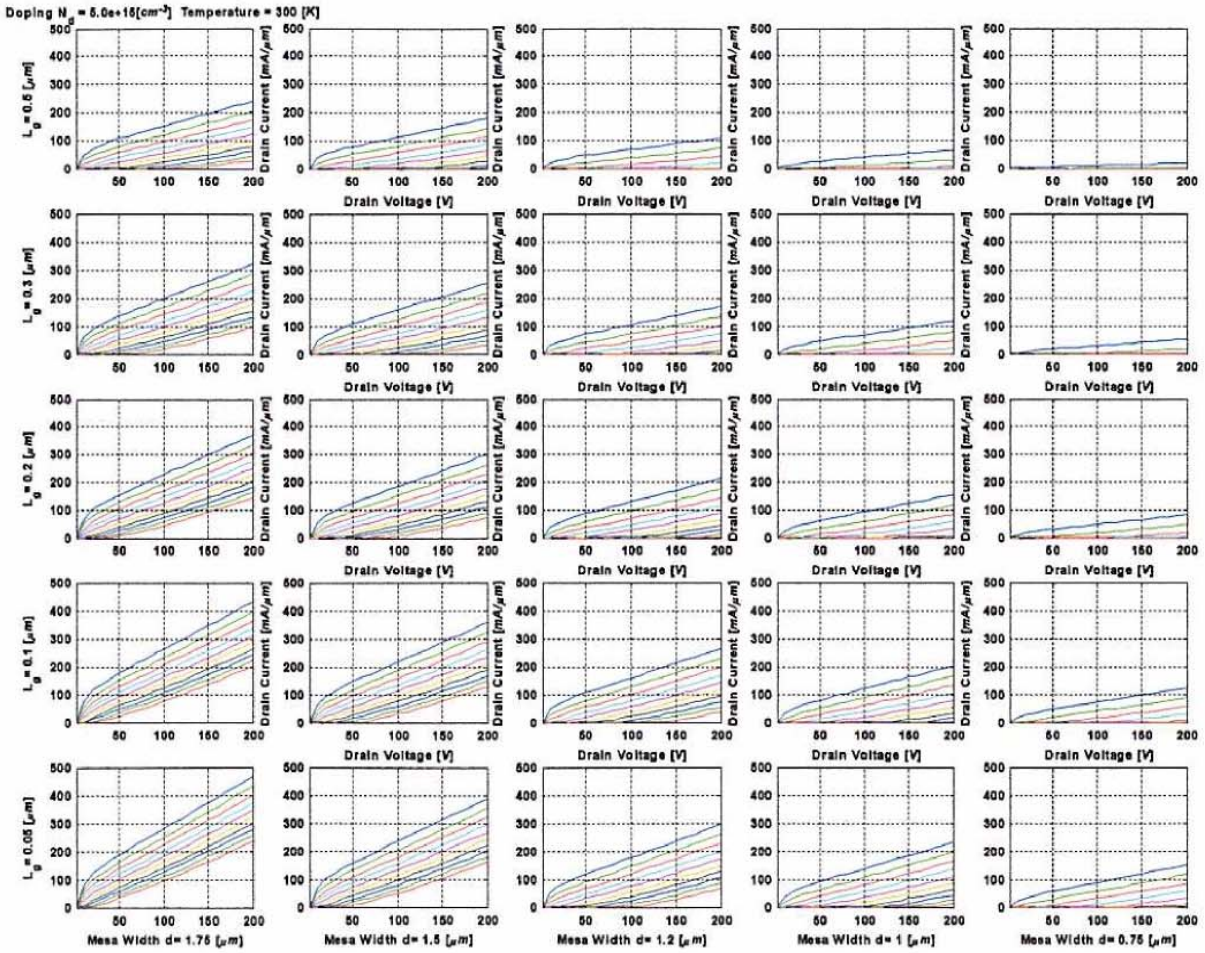

Figure C.1 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}] and 300 [K].

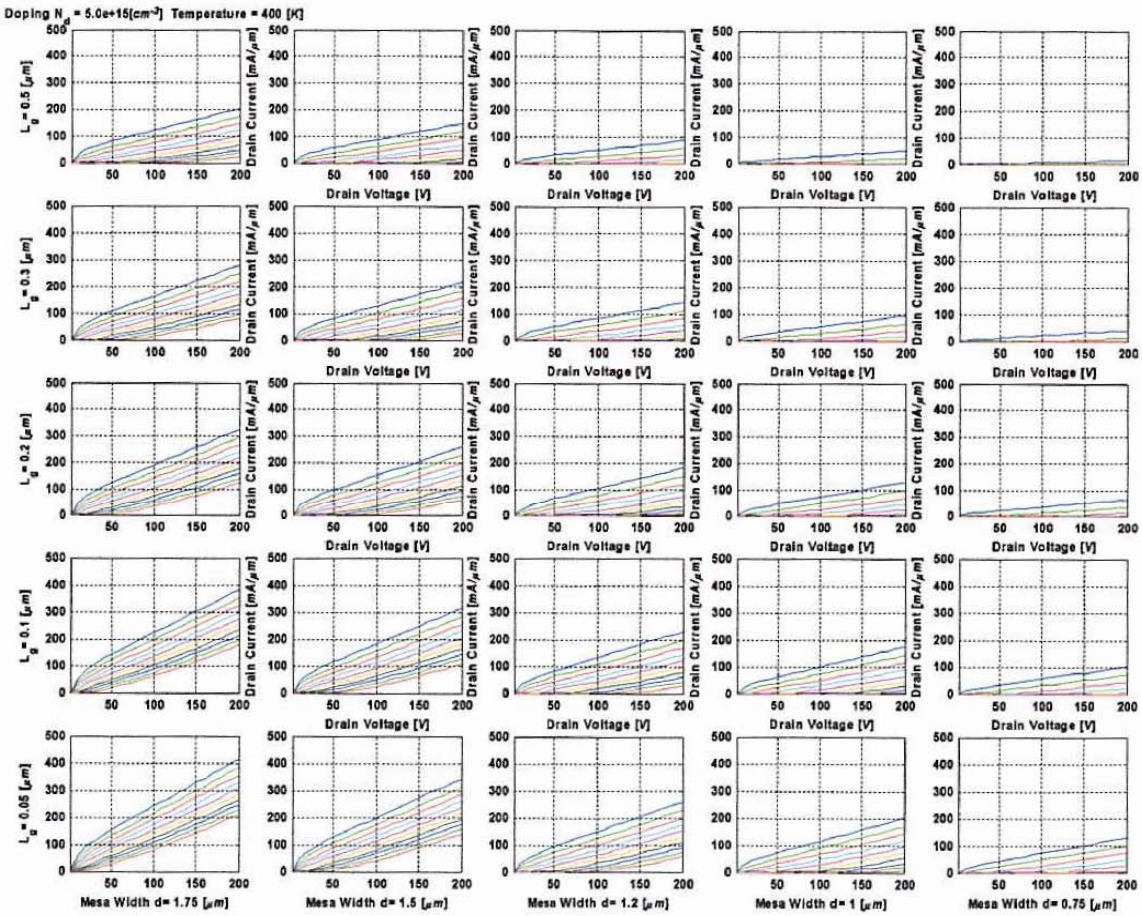

Figure C.2 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}] and 400 [K].

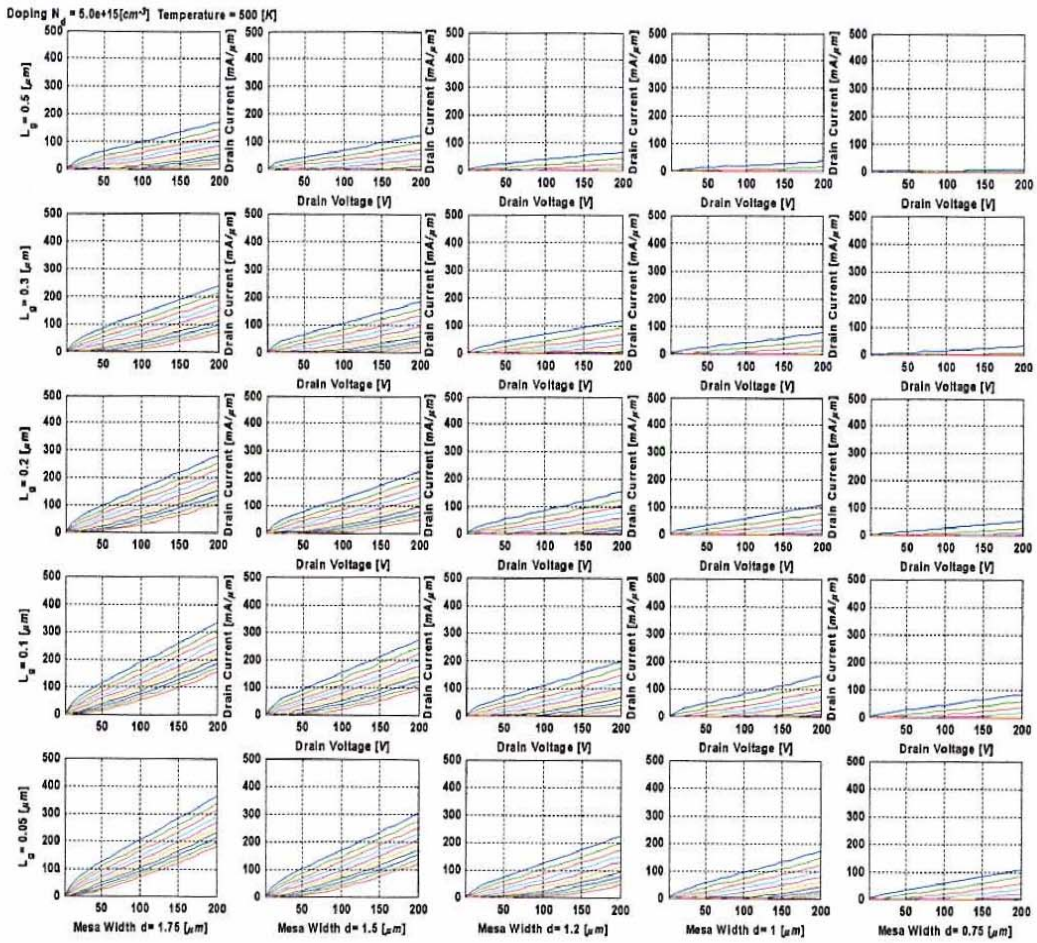

Figure C.3 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}] and 500 [K].

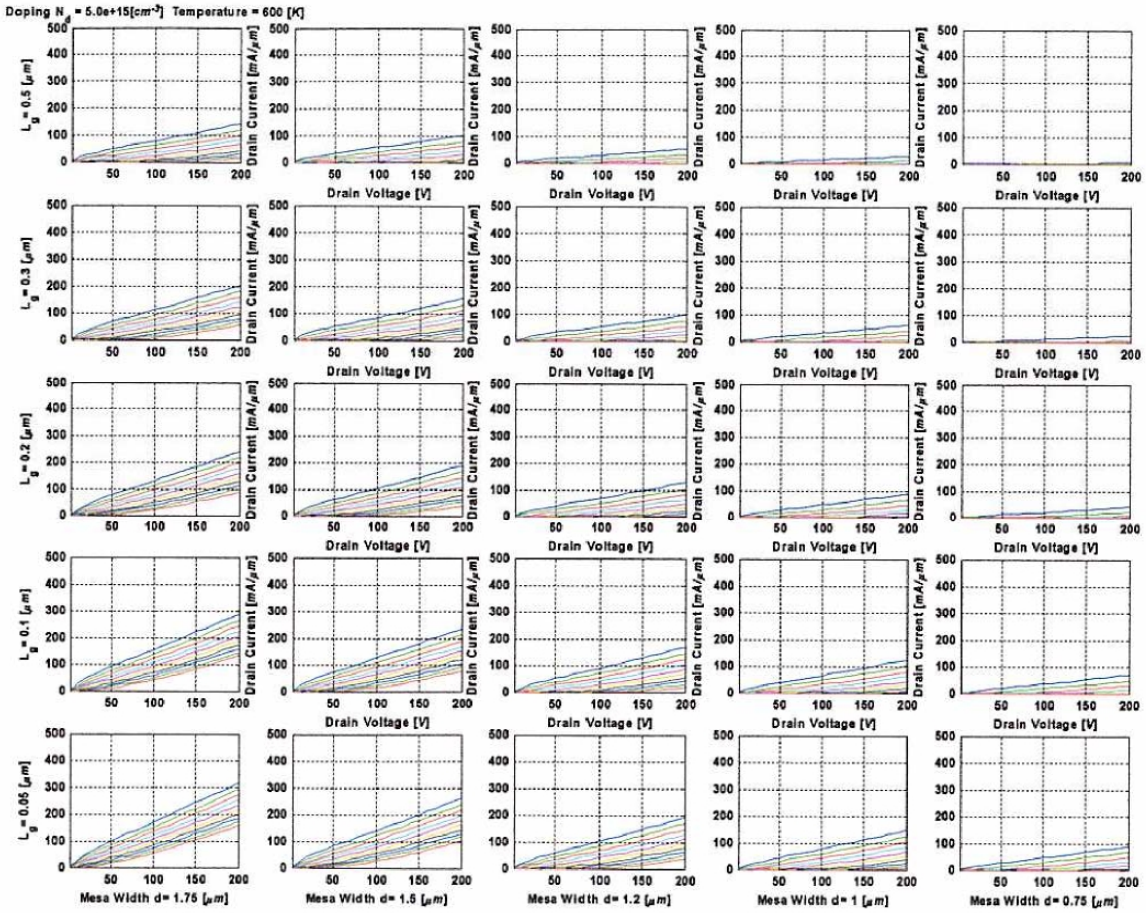

Figure C.4 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}] and 600 [K].

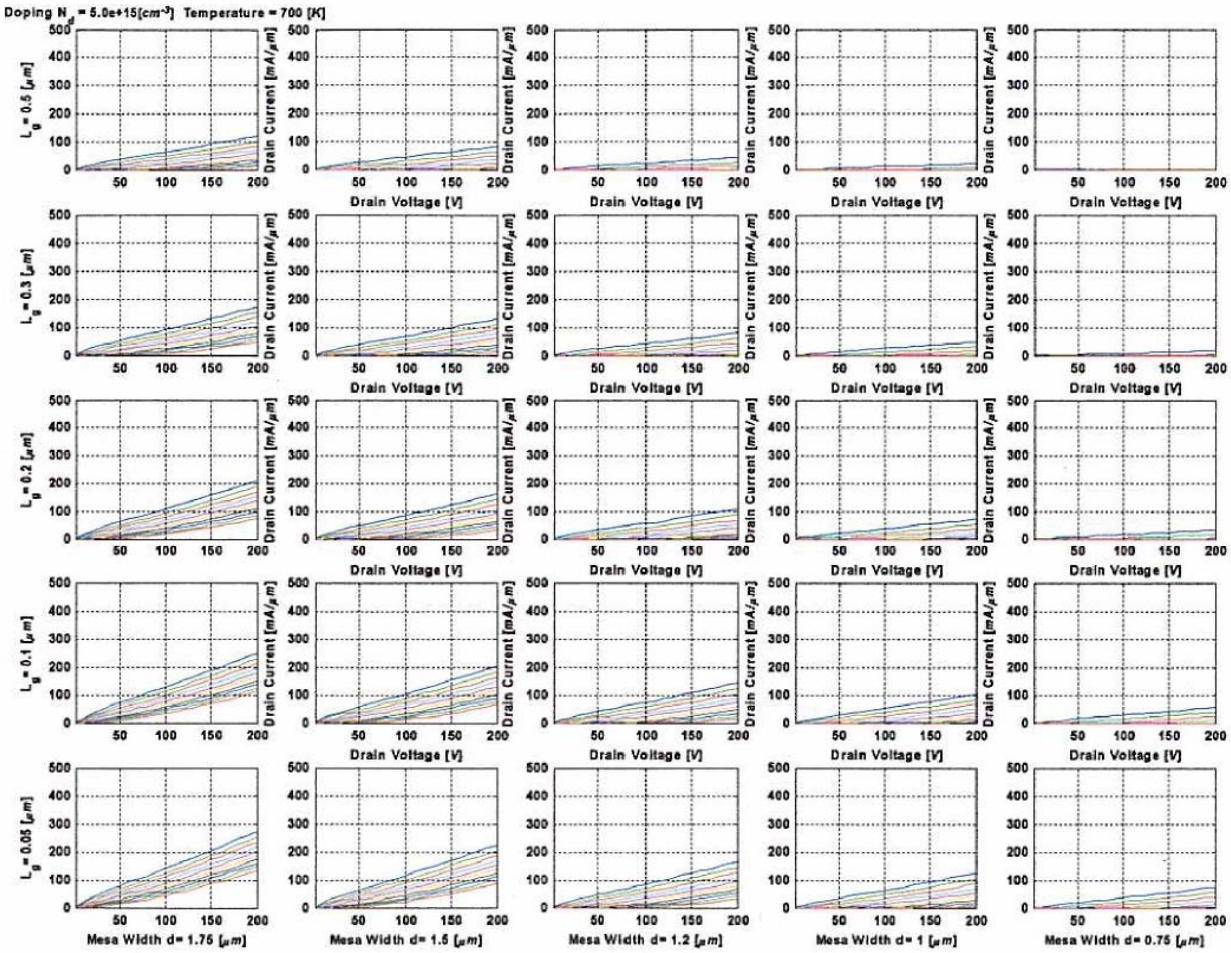

Figure C.5 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}] and 700 [K].

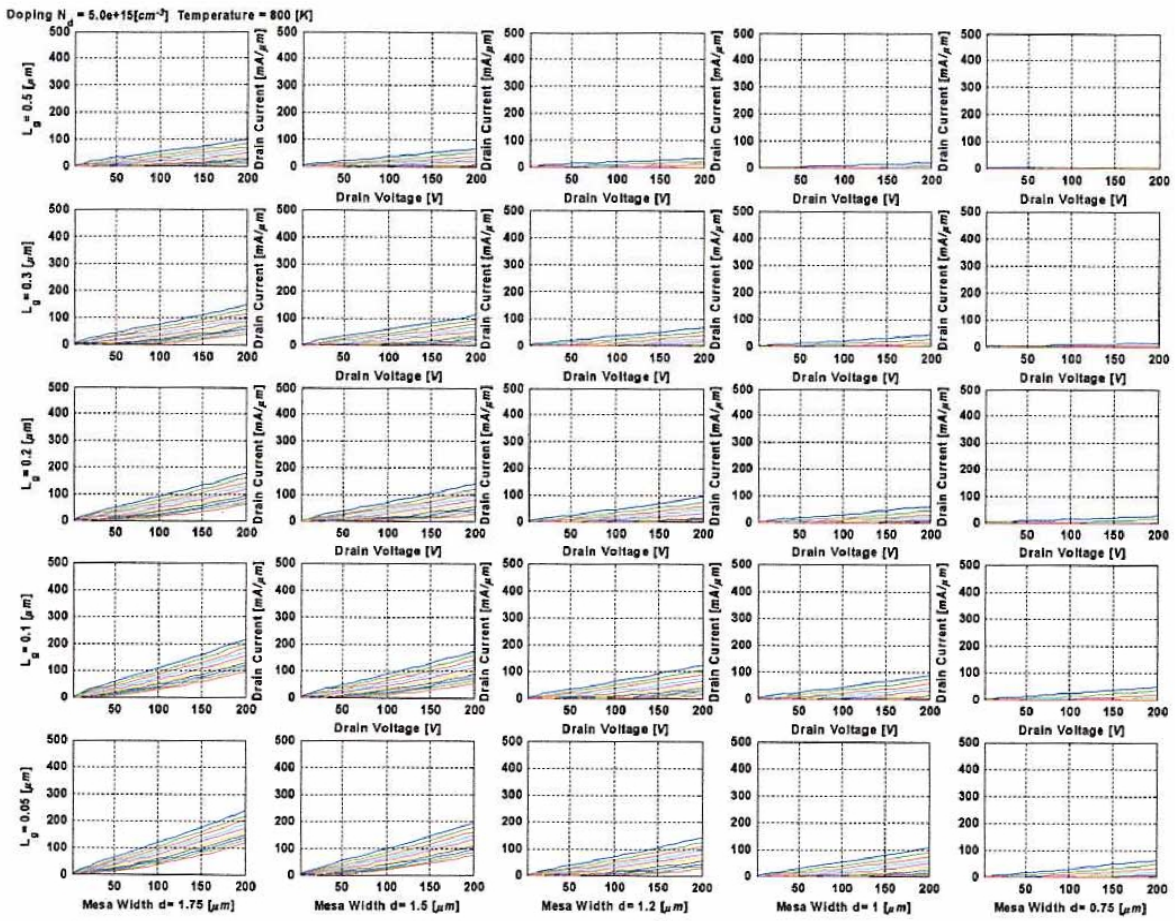

Figure C.6 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}] and 800 [K].

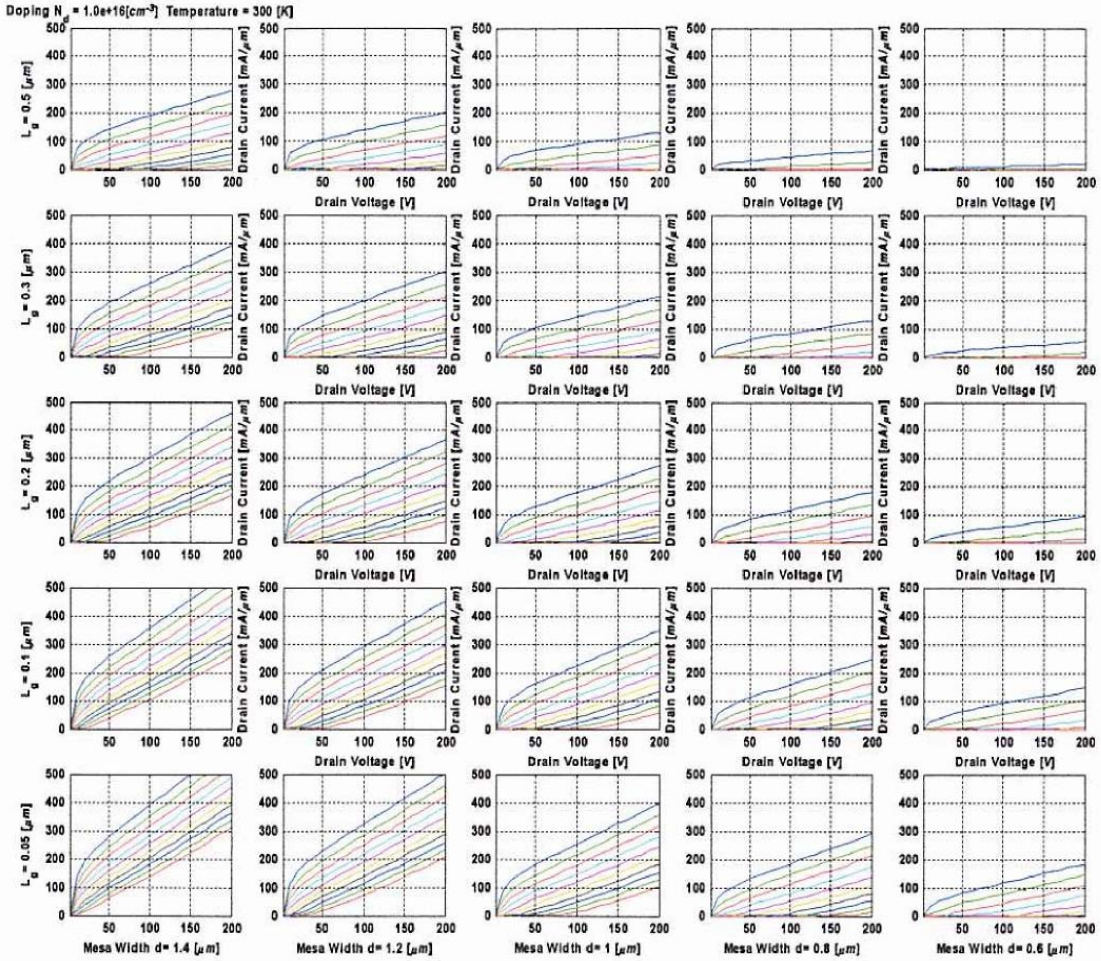

Figure C.7 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 300 [K].

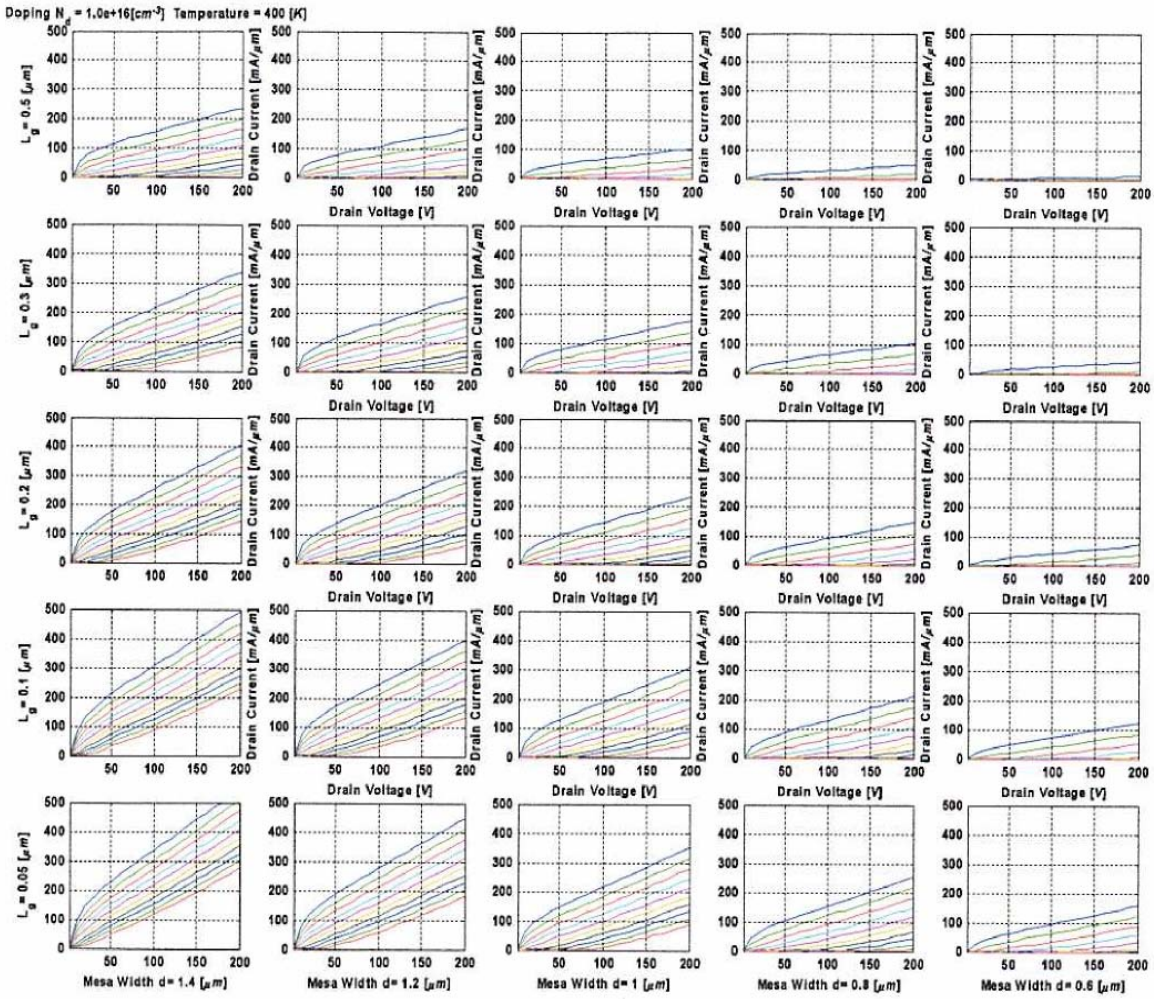

Figure C.8 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 400 [K].

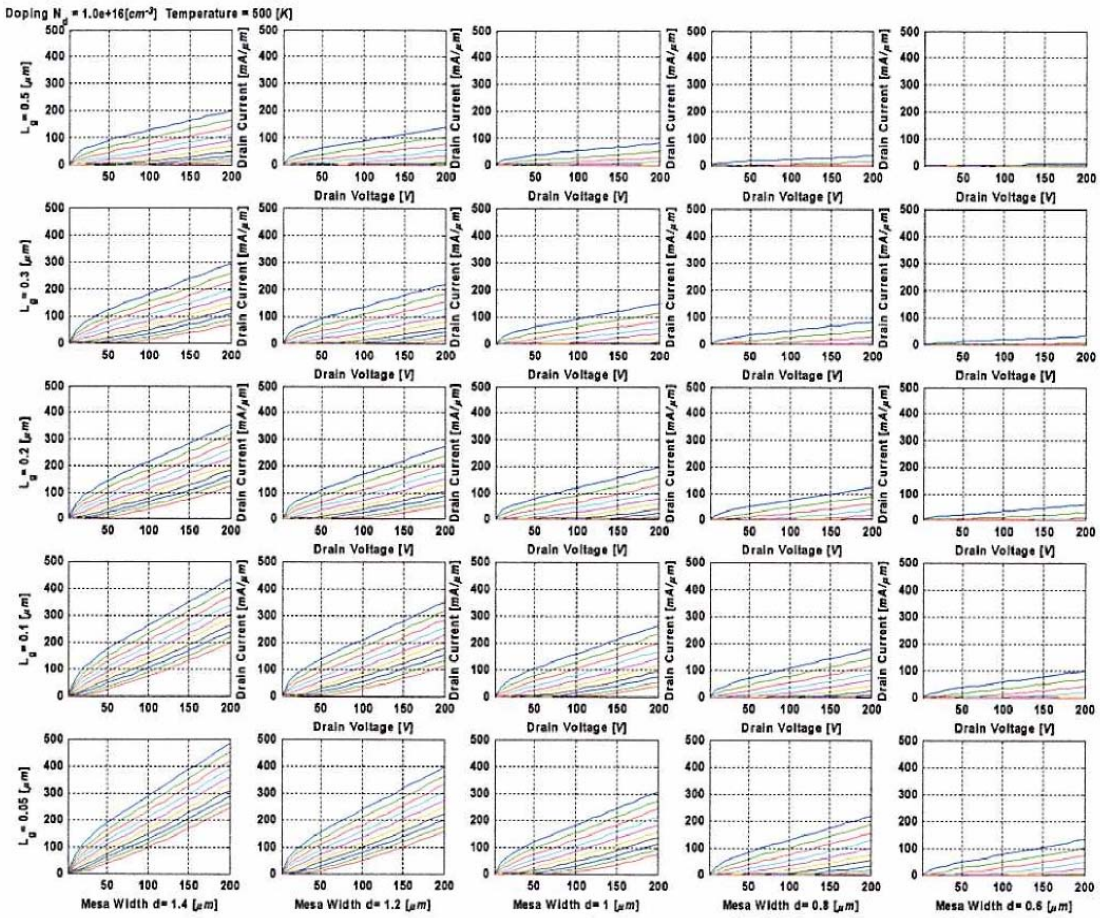

Figure C.9 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 500 [K].

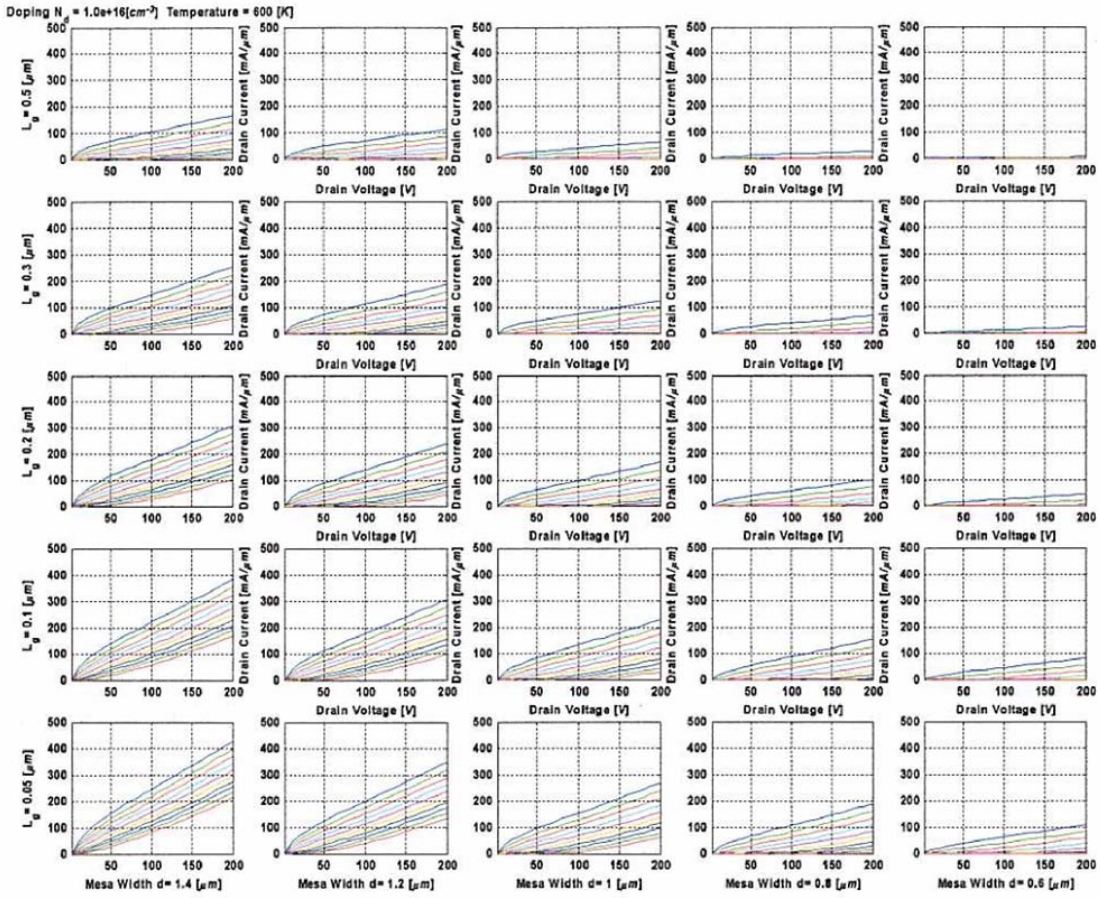

Figure C.10 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 600 [K].

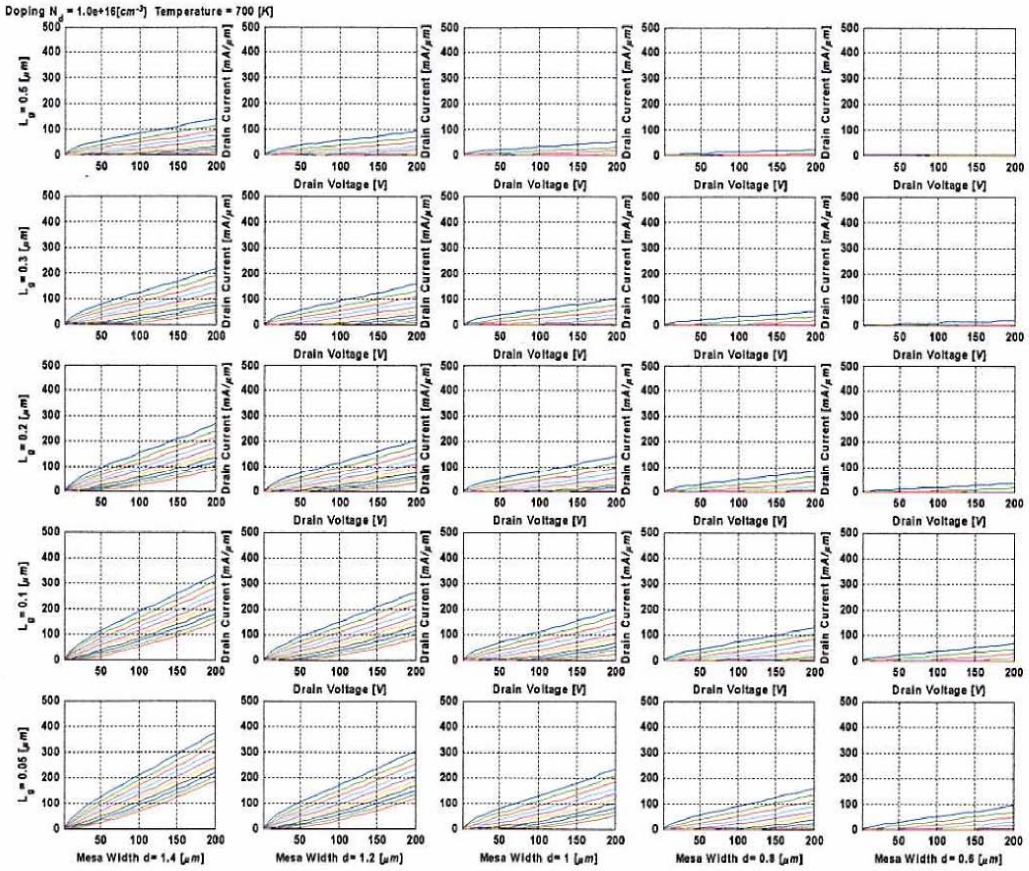

Figure C.11 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 700 [K].

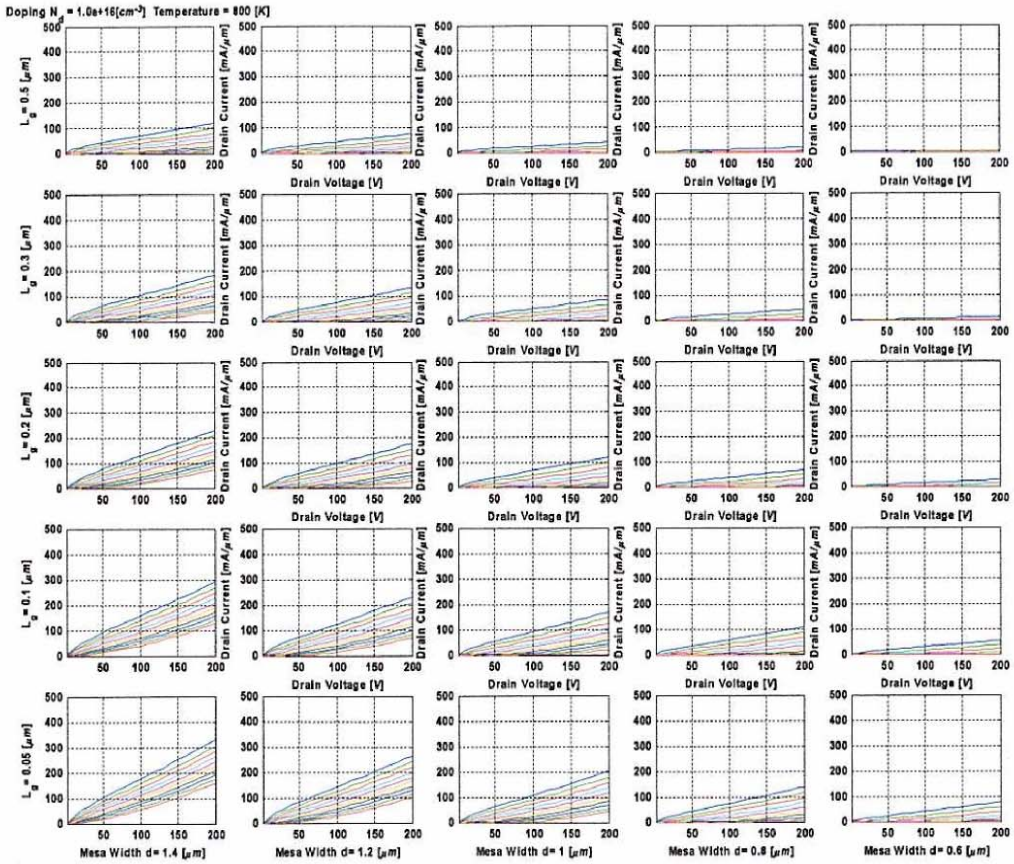

Figure C.12 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 800 [K].

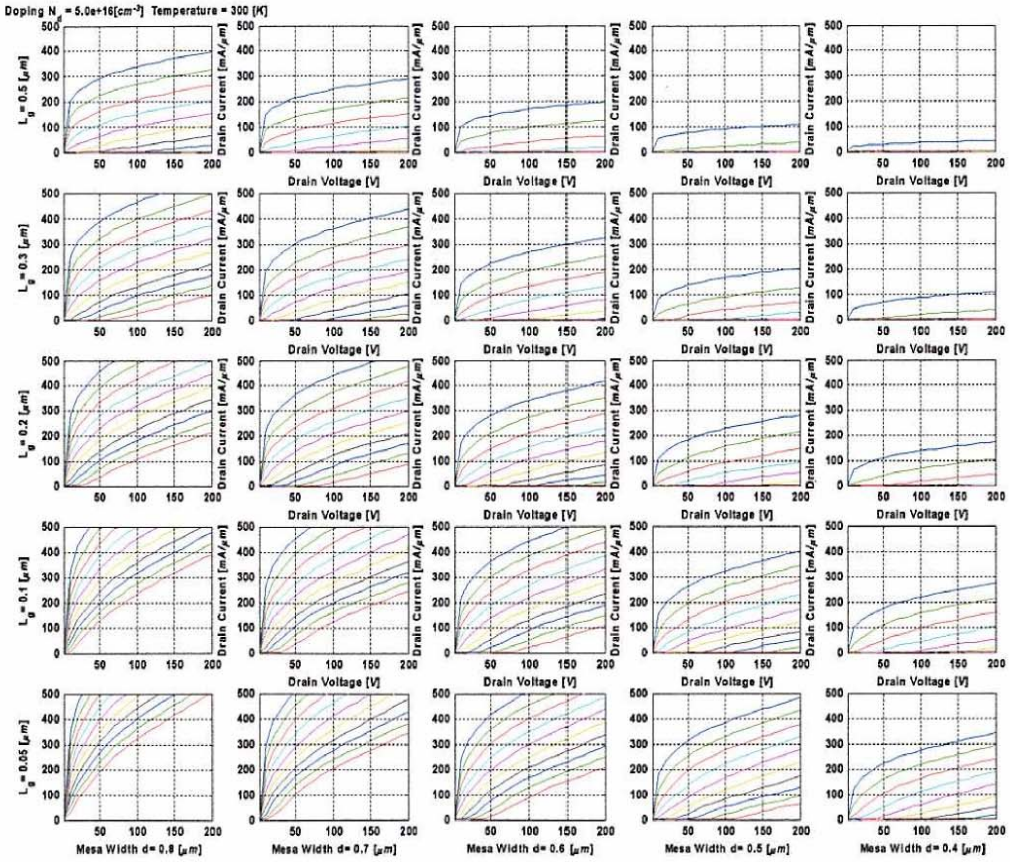

Figure C.13 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ $[cm^{-3}]$ and 300 $[K]$.

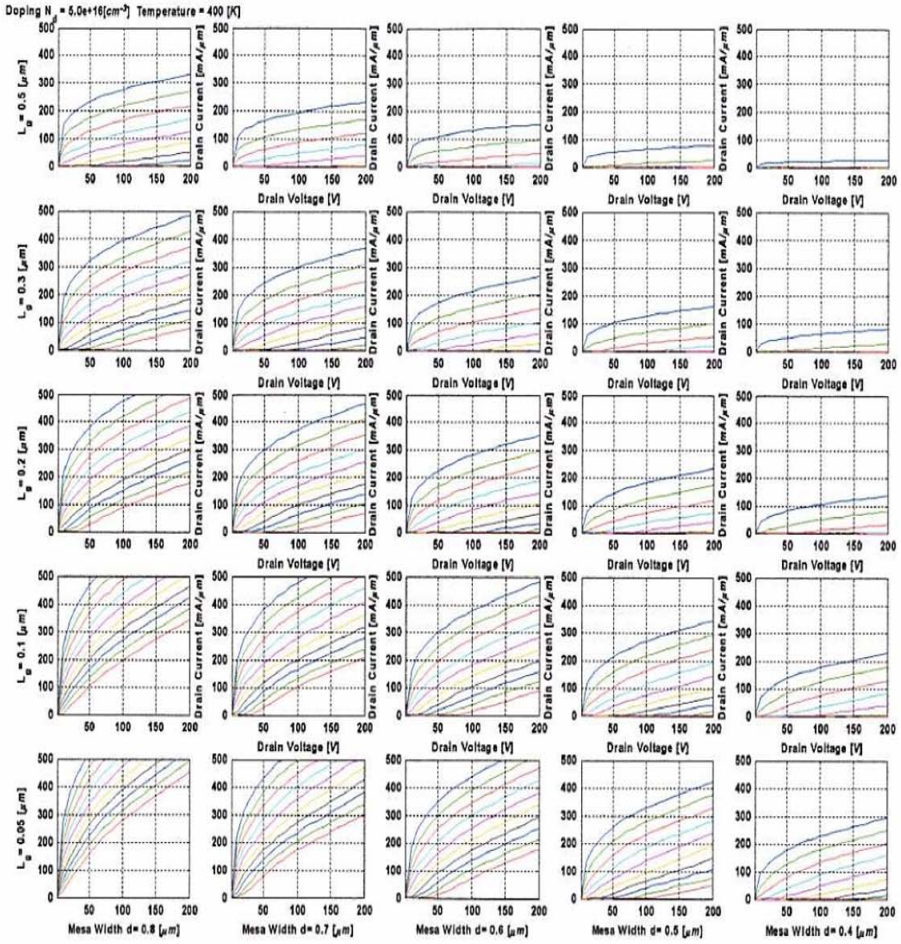

Figure C.14 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ $[cm^{-3}]$ and 400 $[K]$.

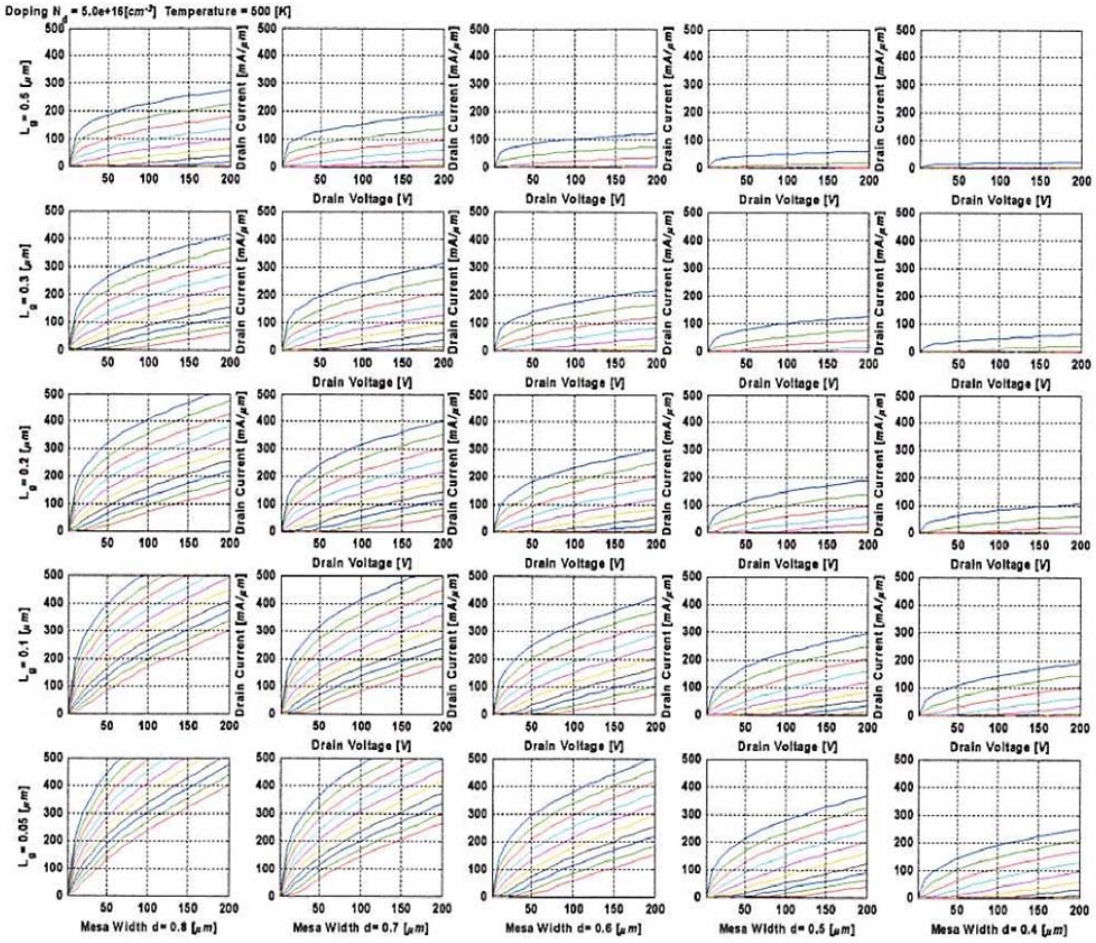

Figure C.15 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 500 [K].

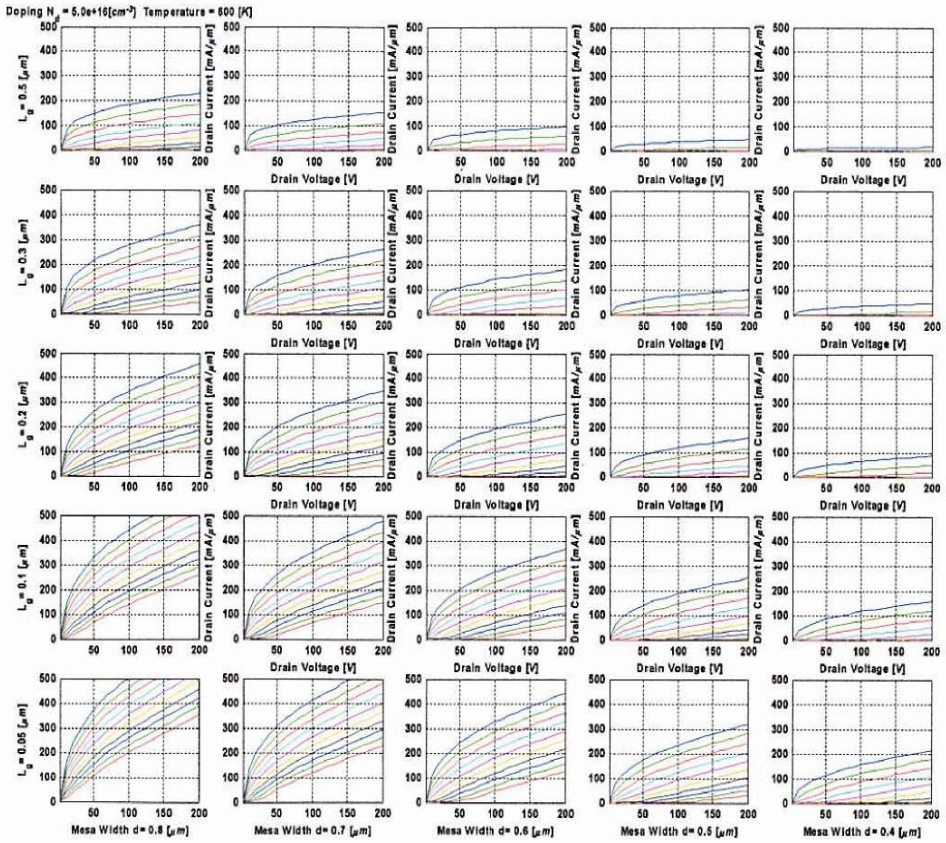

Figure C.16 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 600 [K].

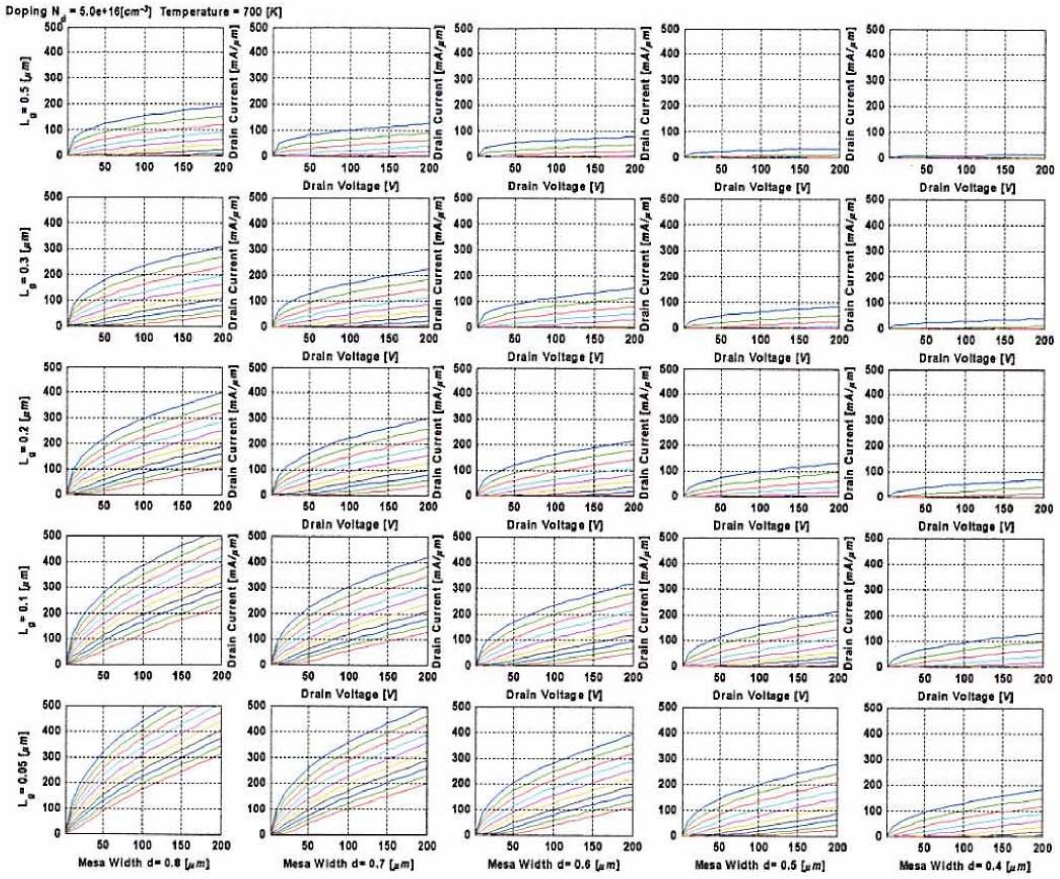

Figure C.17 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 700 [K].

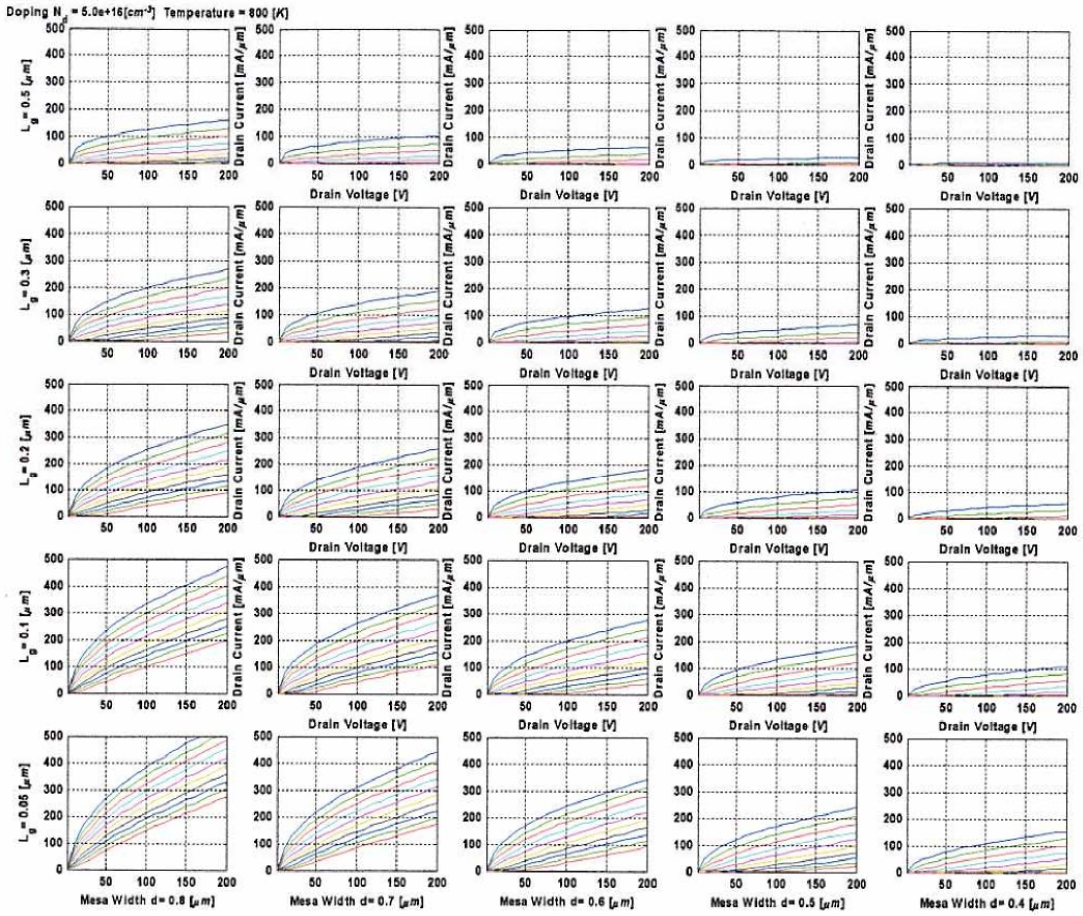

Figure C.18 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 800 [K].

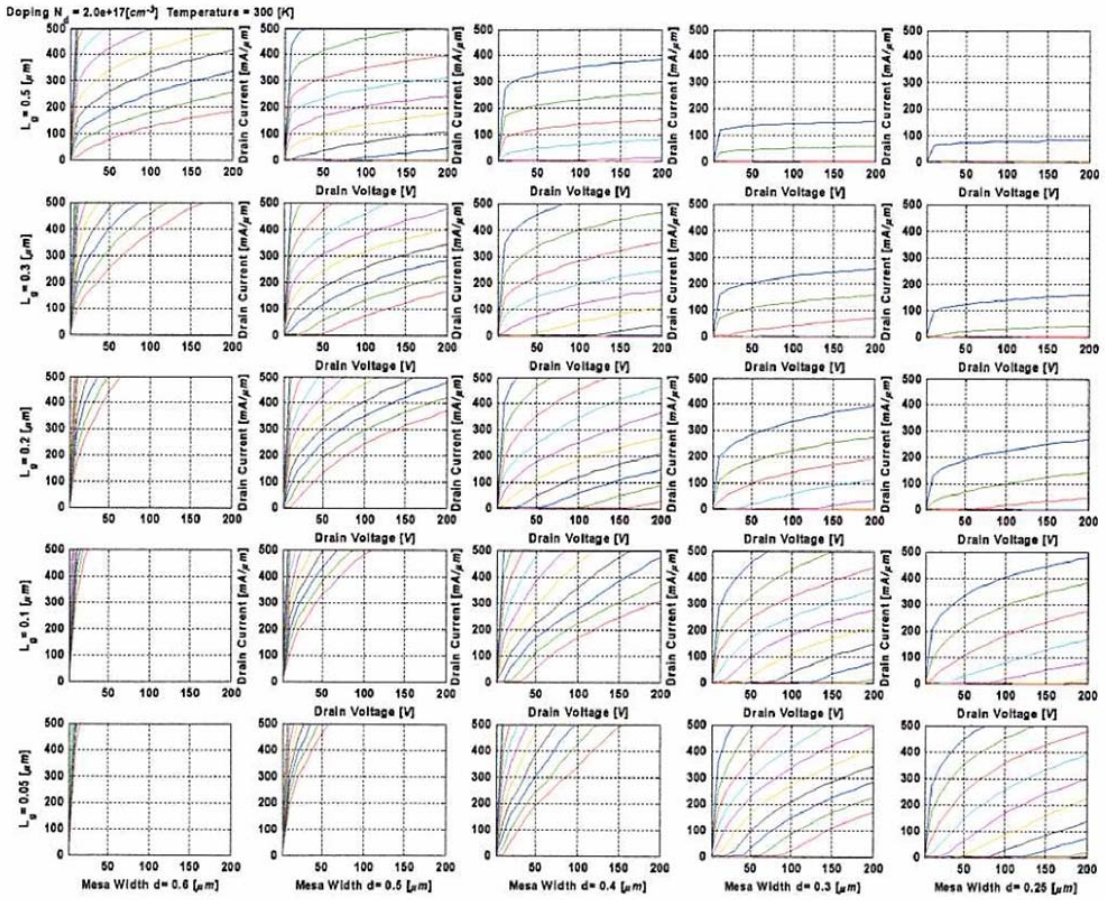

Figure C.19 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 300 [K].

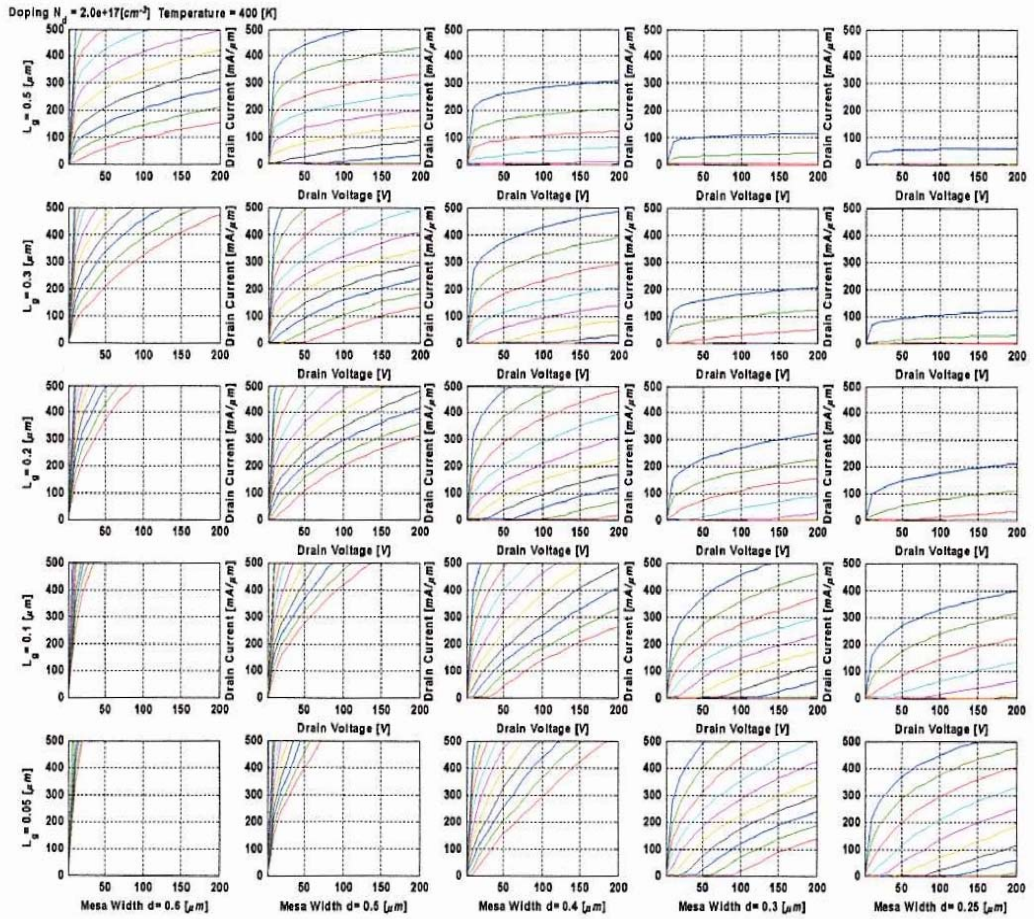

Figure C.20 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 400 [K].

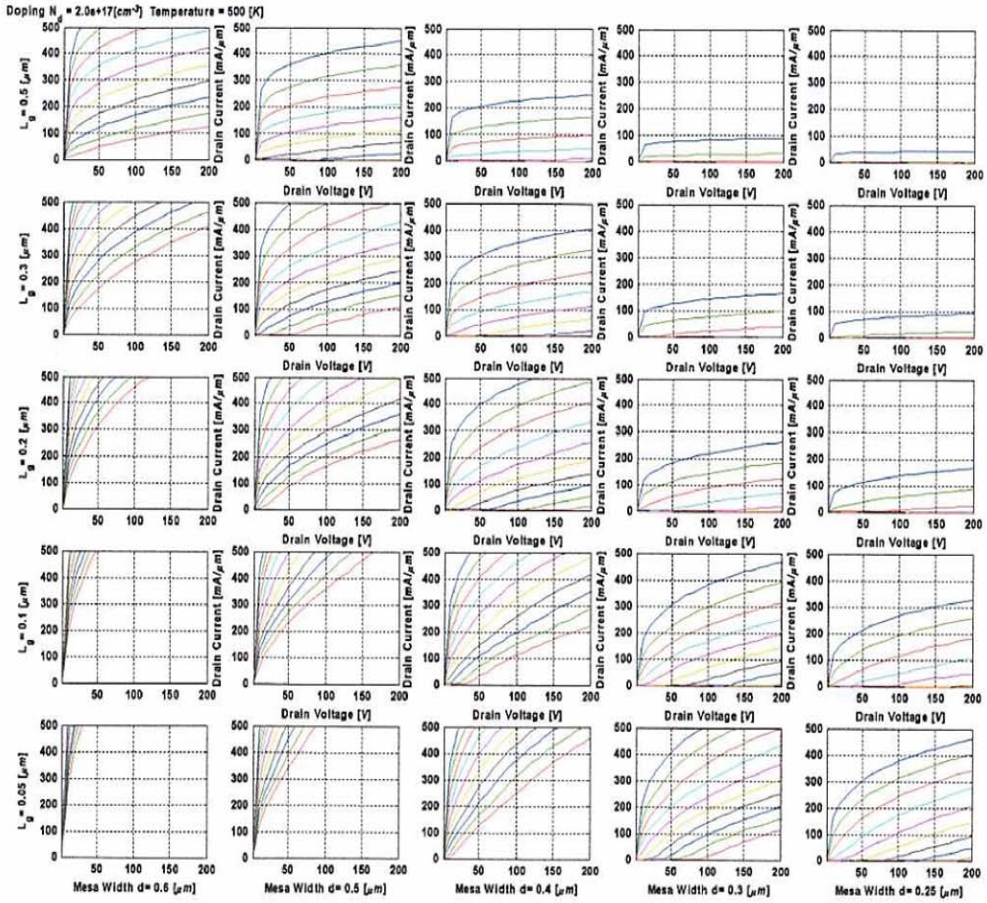

Figure C.21 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 500 [K].

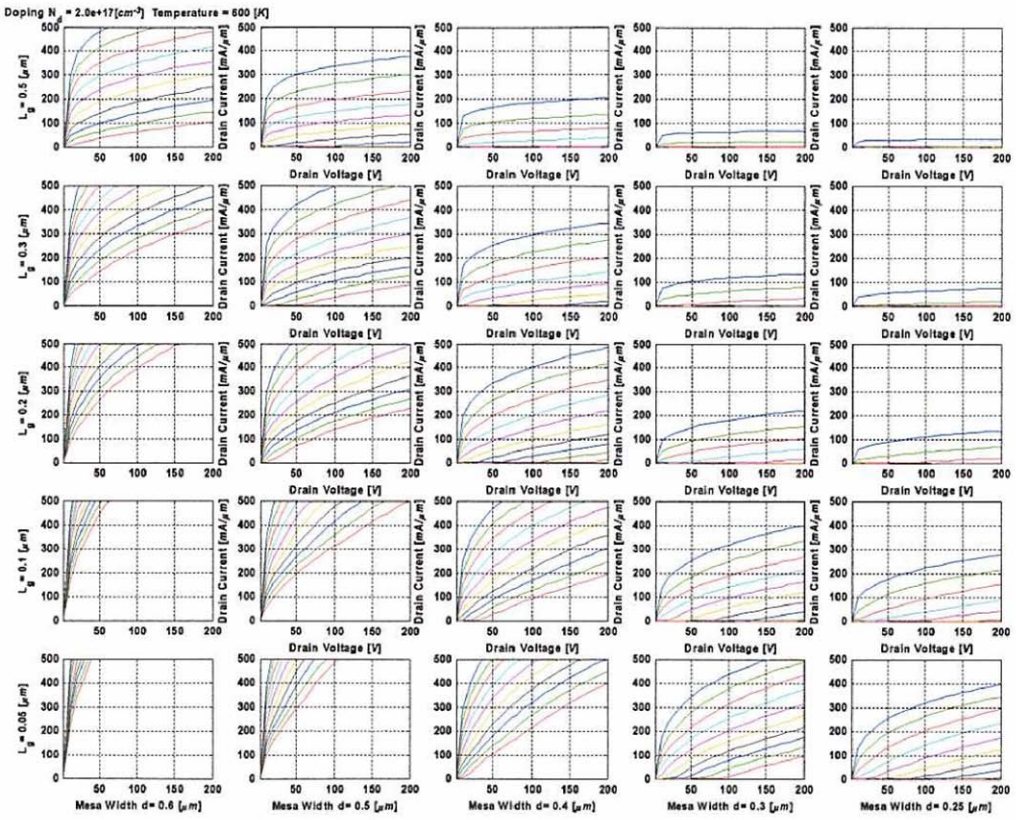

Figure C.22 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 600 [K].

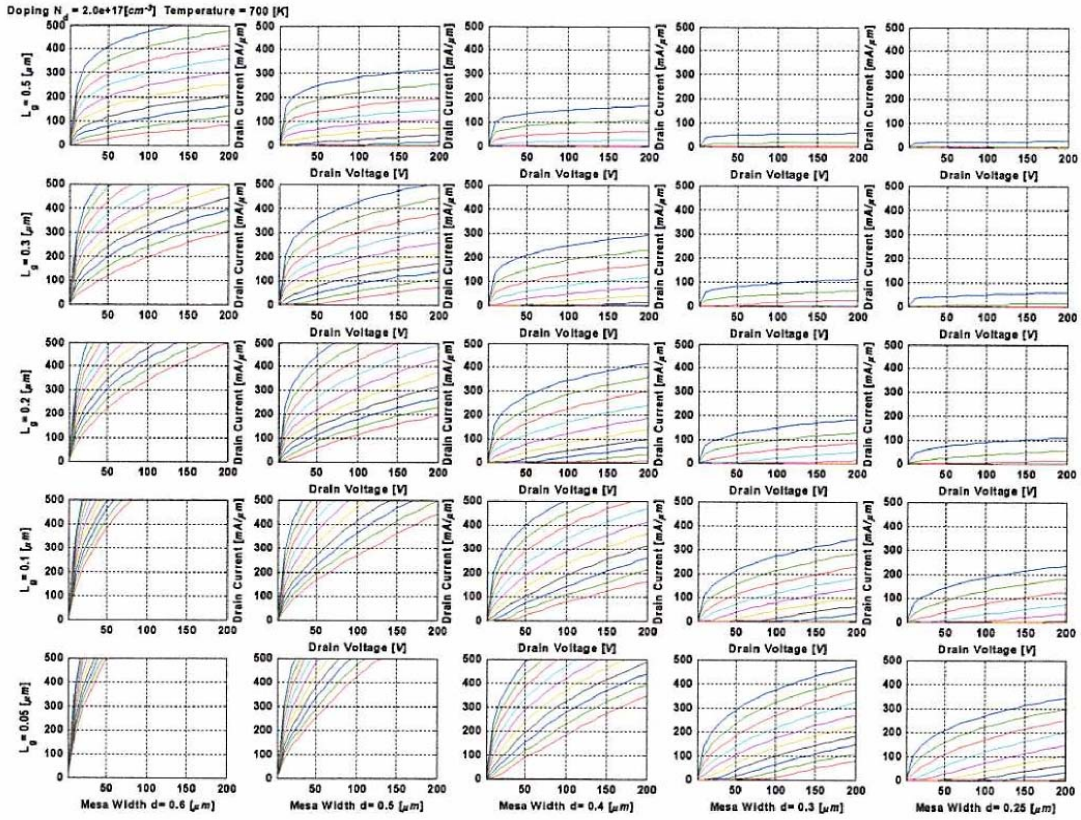

Figure C.23 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 700 [K].

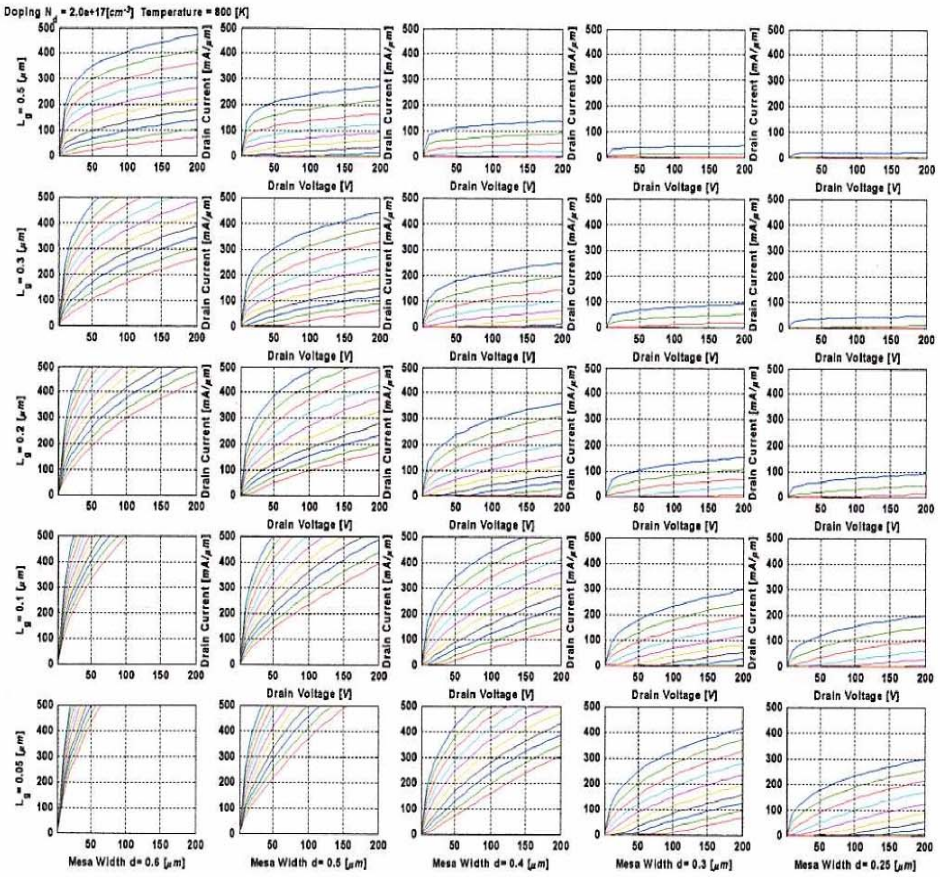

Figure C.24 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 800 [K].

D. Conversion from Y-parameter to S-parameter

$$Y_{11} = \frac{(1-S_{11})(1+S_{22})+S_{12}\cdot S_{21}}{(1+S_{11})(1+S_{22})-S_{12}\cdot S_{21}} = \frac{1}{h_{11}} \tag{D-1}$$

$$Y_{12} = \frac{-2\cdot S_{12}}{(1+S_{11})(1+S_{22})-S_{12}\cdot S_{21}} = \frac{-h_{12}}{h_{11}} \tag{D-2}$$

$$Y_{21} = \frac{-2\cdot S_{21}}{(1+S_{11})(1+S_{22})-S_{12}\cdot S_{21}} = \frac{h_{12}}{h_{11}} \tag{D-3}$$

$$Y_{22} = \frac{(1+S_{11})\cdot(1-S_{22})+S_{12}\cdot S_{21}}{(1+S_{11})\cdot(1+S_{22})-S_{12}\cdot S_{21}} = \frac{h_{11}\cdot h_{22}-h_{12}\cdot h_{21}}{h_{11}} \tag{D-4}$$

E. Simulation Results for Frequency and Transconductance Characteristics

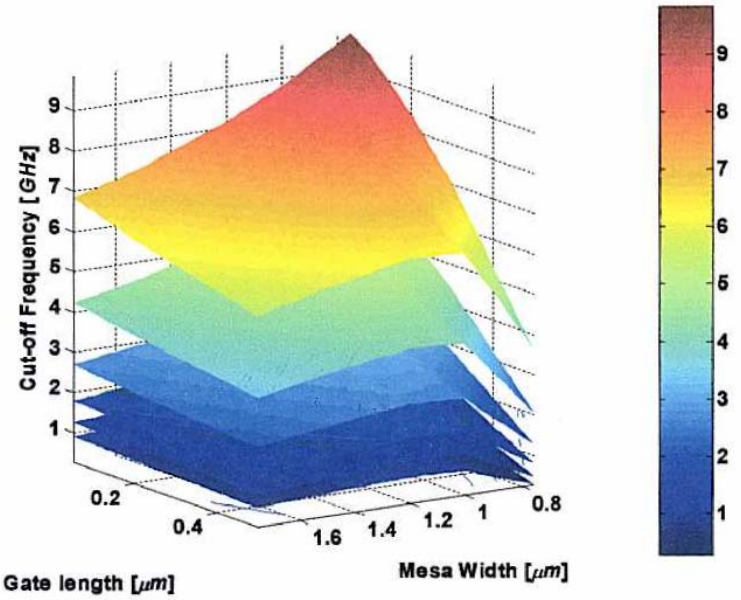

Figure E.1 Cut-off frequency for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.

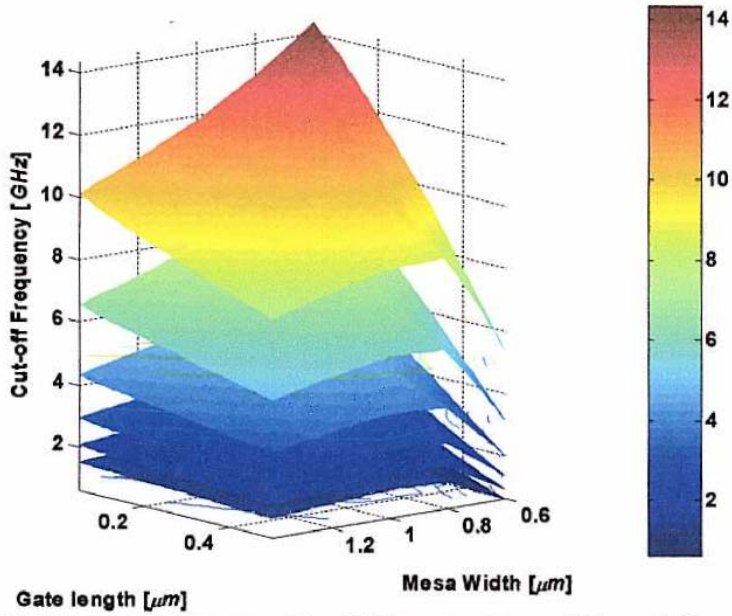

Figure E.2 Cut-off frequency for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.

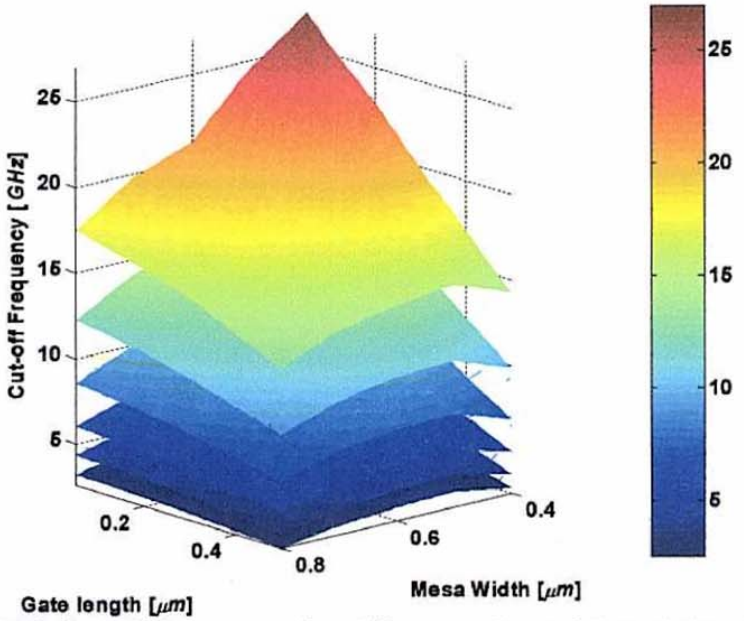

Figure E.3 Cut-off frequency for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.

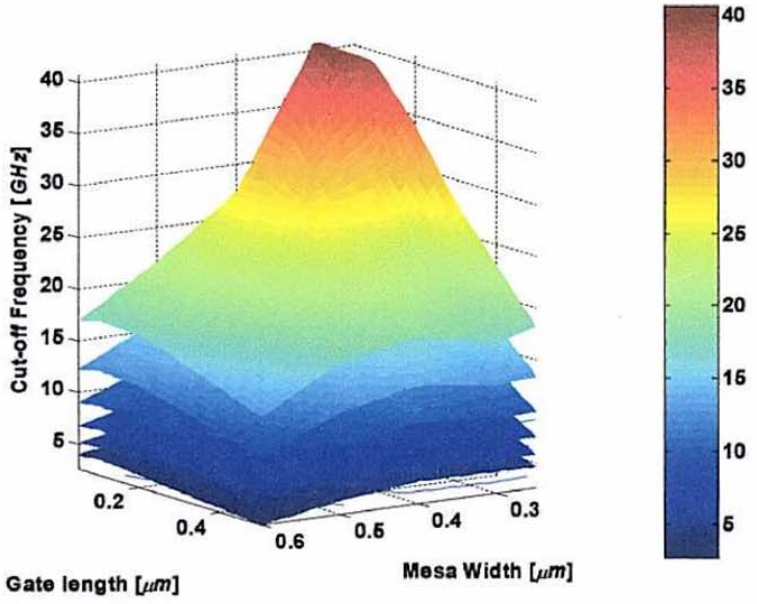

Figure E.4 Cut-off frequency for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.

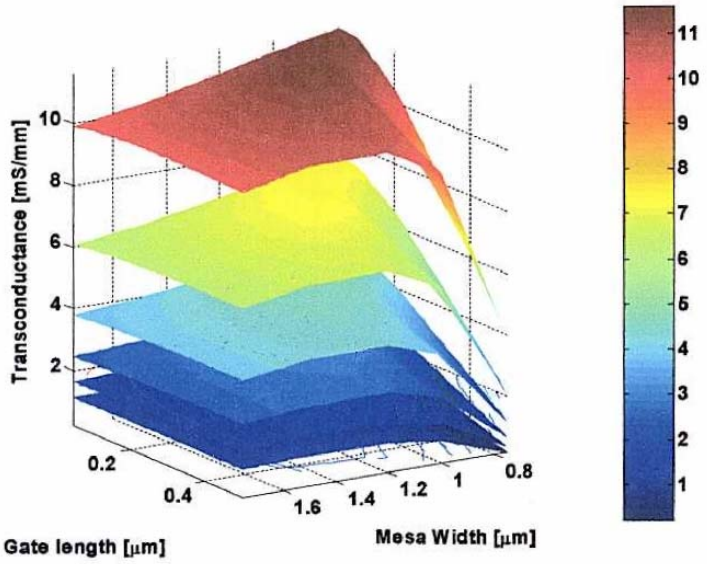

Figure E.5 Transconductance for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ $[cm^{-3}]$, from top to bottom, 300, 400, 500, 600, 700, 800 $[K]$, respectively.

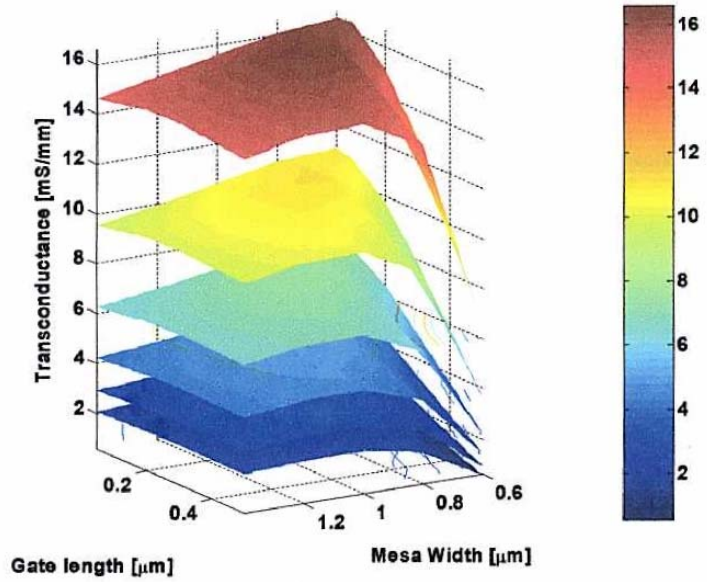

Figure E.6 Transconductance for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ $[cm^{-3}]$, from top to bottom, 300, 400, 500, 600, 700, 800 $[K]$, respectively.

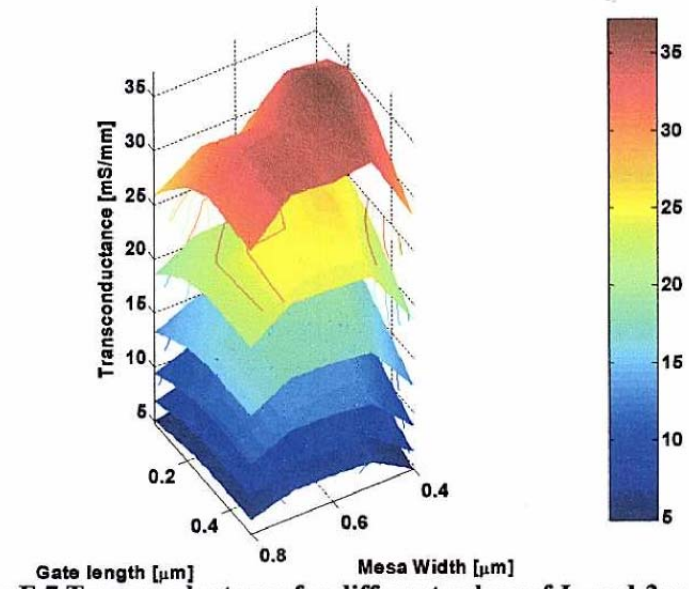

Figure E.7 Transconductance for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ $[cm^{-3}]$, from top to bottom, 300, 400, 500, 600, 700, 800 $[K]$, respectively.

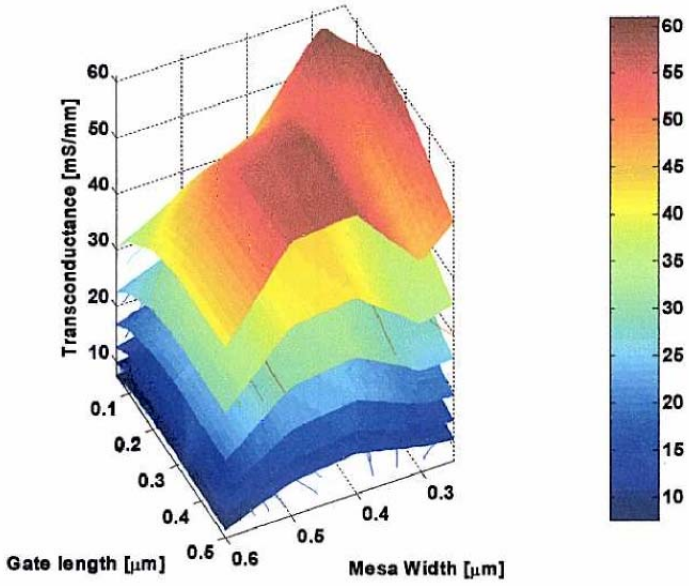

Figure E.8 Transconductance for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ $[cm^{-3}]$, from top to bottom, 300, 400, 500, 600, 700, 800 $[K]$, respectively.