HIGH PERFORMANCE NANO-CONSTITUENT BUFFER LAYER THIN FILMS TO ENABLE LOW COST INTEGRATED ON-THE-MOVE COMMUNICATIONS SYSTEMS

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ABSTRACT

Successful integration of paraelectric $Ba_{1-x}Sr_xTiO_3$ (BST) based thin films with affordable Si substrates has a potential significant commercial impact as the demand for high-frequency tunable devices intensifies. Utilizing a co-planar device design we have successfully designed, fabricated, characterized, and optimized a high performance Ta_2O_5 thin film passive buffer layer on Si substrates, which will allow the integration of BST films with large area affordable Si substrates. This passive buffer layer thin film was fabricated via the industry standard metalorganic solution decomposition technique. The anneal optimized Ta_2O_5 based thin film possessed excellent material properties. Specifically, these material properties include an enhanced dielectric constant (ε_r =45.6), low dielectric loss (tan δ=0.006), low leakage current or high film resistivity (ρ=10^{12} Ω-cm at E=1 MV/cm), excellent temperature stability (temperature coefficient of capacitance of 52 ppm/^{o}C), and excellent bias stability of capacitance (~1.41% at 1 MV/cm). Additionally, the permittivity and dissipation factor exhibited minimal dielectric dispersion with frequency. The dielectric passive buffer layer film was typified by a uniform dense microstructure with minimal defects, and a smooth, nano-scale fine grain, crack/pinhole free surface morphology. This work also demonstrated that the coefficient of thermal expansion (CTE) mismatch between the Ta_2O_5 buffer and BST active thin films in the coplanar device design serves to enhance the dielectric tunability of the device. The development of this passive buffer layer thin film materials technology will enable the direct integration of paraelectric active thin films (BST) with silicon substrates. The impact of this materials technology is paramount, as this phase shifter materials technology design will promote broad scale implementation of affordable On The Move (OTM) phased array antenna systems across a variety of DoD platforms.

1. INTRODUCTION

The Army is actively pursuing technologies to meet transformation goals of a lighter, faster, more lethal force via "*Integrated On-The-Move (OTM) Communications*" from sensor to shooter. Affordable electronically scanned phased array antennas (ESA's) provide the means for achieving this high data rate, beyond line of sight, OTM communications. Unfortunately, costly phase shifter elements (essential active components in the ESA's); with prices of ~ $100.00 per element, are the primary obstacle inhibiting the "*broad scale*" adaptation of ESA's within the DoD (Coryell, L., 2003). In order to accomplish broad scale implementation of ESA's, a shift in design strategy is required with emphasis on the fabrication of affordable phase shifters. Specifically, the cost of the phase shifter must be reduced to ~$5 per element. The recent advancements in material design and process science suggests paraelectric electroceramic BST based thin films to be the prime candidate "*active*" material for achieving such affordable phase shifter circuits (Wolf and Treger, 2002). However, a major caveat in using such active thin films hinges on the integration this active material with large area, low cost, microwave friendly substrates. Phase shifter device fabrication utilizing paraelectric active thin films requires appropriate substrates for both mechanical support and device integration. To date, paraelectric active BST based thin films, compositionally designed for tunable microwave applications, have been deposited on ceramic (MgO, $LaAlO_3$, $SrTiO_3$, Al_2O_3) substrates. The major drawback of such substrates is their high cost ($50-$100 for ~1x1 in^2 pieces). Aside from the direct substrate cost, the affordability criteria is further compromised by (1) the small substrate size (MgO, $LaAlO_3$ and $SrTiO_3$ are only available in small size geometries, ~1x1 in^2) which translates to fewer devices per wafer, and (2) the inherent brittleness of all ceramic substrates which manifests into wafer dicing issues (i.e., device breakage) which lowers the device yield per substrate. An additional cost driver ramification of utilizing thin film/ceramic substrate phase shifter components is that such device components are considered "*discrete devices*" and require mounting in a "*hybrid*" microwave integrated circuit (MIC) type construction. The fabrication and tuning of MIC's is labor intensive and expensive. Additionally, this configuration is not considered a "*direct*" monolithic integration process and therefore poses reliability issues via component mount-bond failure.

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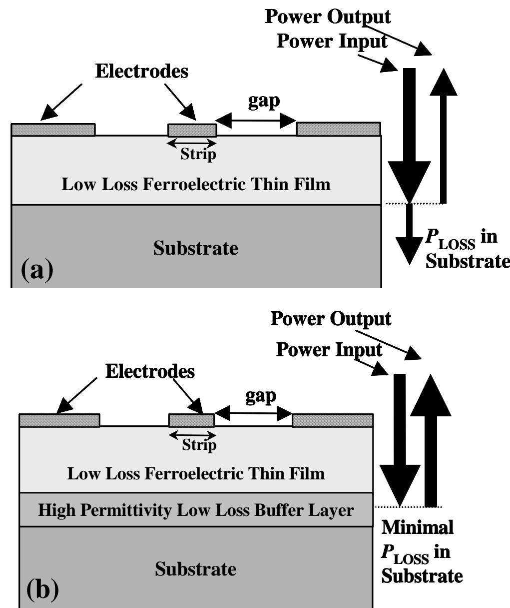


Figure 1. Coplanar device design; (a) tunable low loss active thin film deposited on lossy substrate and (b) tunable low loss active thin film integrated with the same lossy substrate utilizing a "*microwave friendly*" buffer layer.

OTM antenna performance specifications (e.g., low insertion loss), requires the phase shifter substrate to be "*microwave friendly*", that is, one which does not attenuate the microwave energy of the actual device material and structure. Additionally, the substrate must be large area (≥ 6 inch diameter), low cost, thermally stable, chemically resistant, structurally suitable with good mechanical integrity, and must not perturb the performance of the active layer(s) constituents of the phase shifter device. Since most electronic systems, military and commercial, are built as integrated circuits, ensembles of both active and passive devices on Si substrates linked via metal interconnects, it is of significant interest to integrate these active thin films with Si substrates. This interest is driven by the affordability and large size availability of Si wafers and the widespread industrial/commercial use of Si based processing technology. However, for microwave device applications, such integration precludes the use of bare Si substrates since Si is not a "*microwave friendly*" material, i.e., at microwave frequencies Si becomes less resistive, and consequently is too lossy for use in microwave devices. Therefore, Si is not the semiconductor of choice for microwave components. Figure 1a depicts a standard coplanar microwave phase shifter design whereby a microwave friendly, low loss tunable paraelectric active thin film is deposited on a "non-microwave friendly" substrate such as Si. This configuration is performance limiting since there is considerable attenuation of the microwave energy by the substrate, i.e., significant power loss in substrate. However, in theory, silicon substrates can be utilized if "*microwave friendly*" passive buffer layers can be sandwiched between the Si substrate and the active paraelectric thin film. Figure 1b is representative of the configuration where a "*microwave friendly*" passive (non-tunable) buffer layer is sandwiched between the Si substrate and the low loss active (tunable) thin film. In this case there is negligible attenuation of the microwave energy by the substrate.

In this work we demonstrate that silicon substrates can be utilized in phase shifter devices if a "*microwave friendly*" passive buffer layer can be sandwiched between the Si substrate and the low loss active paraelectric BST based thin film. In this heterostructure configuration there is negligible attenuation of the microwave energy by the substrate. In addition, if the buffer layer is designed to promote a tensile stress in the active thin film, the tunability of the device will be enhanced to levels comparable to that of varactor device design.

2. EXPERIMENTAL

The Ta_2O_5 buffer layer thin films were fabricated via the metalorganic solution deposition (MOSD) technique. Tantalum ethoxide was used as the precursor to form the film and acetic acid and 2-methoxyethanol were used as solvents and for viscosity adjustment. The precursor films were spin coated onto Pt-coated silicon and bare n^+-silicon substrates. Prior to film deposition, the silicon substrates were cleaned by spin etching (Kim et al., 1994). This cleaning allowed for the removal of the native silicon oxide and hydrogen termination of the Si dangling bonds. Particulates were removed from the solution by filtering through 0.2 μm syringe filters. Subsequent to coating, the films were pyrolyzed at 350 ^oC for 10 min. in order to evaporate solvents and organic addenda to form an inorganic amorphous film. The spin coat pyrolyzation process was repeated until a nominal film thickness of ~100 nm was achieved. Optimized film crystallinity was achieved via post-deposition annealing in an oxygen ambience at 750 ^oC for 1 hour.

The coplanar device heterostructure configuration, depicted in Figure. 1b, was achieved by depositing a 200 nm 5 mol-% Mg doped BST paraelectric film, over the optimized Ta_2O_5 buffer layer. The experimental details of details of the Mg doped BST film fabrication have presented elsewhere (Cole et al., 2003). Two heterostructure processing protocols were evaluated for integration integrity, namely, (1) a single anneal and (2) a dual anneal process protocol. The single anneal protocol consisted of depositing a 100 nm layer of Ta_2O_5 on a silicon substrate and pyrolyzing at 350 ^oC. Subsequent to film pyrolyzation, a 200 nm 5 mol-% Mg doped BST film was deposited and pryroyzed at 350 ^oC. The composite film heteroestucture (BST/Ta_2O_5) fabricated on the Si substrate was then annealed for 60 min. at 750 ^oC in an

oxygen ambiance. Alternatively, the dual anneal process protocol consisted of depositing a 100 nm layer of Ta_2O_5 on a Si substrate, pyrolyzing (350 ^oC), and annealing at 750 ^oC for 60 minutes. Subsequent to the Ta_2O_5 film anneal a 200 nm of Mg doped BST film was deposited and pryrolyzed at 350 ^oC. The composite heterostructure was then annealed for 60 min. at 750 ^oC in an oxygen ambiance.

The dispersion of dielectric response (capacitance and loss tangent) of the of the Ta_2O_5 thin films was measured as a function of frequency (1 kHz to 1 MHz), temperature (25-125 ^oC) and applied bias (-15 to +15 V) in the metal-insulator-metal (MIM) device configuration using Pt as the bottom and top electrodes. The film capacitance (C_p) and dissipation factor ($\tan\delta$) were measured with an HP 4194A impedance/gain analyzer. The insulating properties of the films were evaluated via I-V measurements using a HP 4140B semiconductor test system from 0.1-1.0 MV/cm.

Both the buffer layer (Ta_2O_5/Si) and coplanar heterostructure device configuration (BST/Ta_2O_5/Si) were characterized for integration integrity via structural, microstructural and interfacial characterization techniques. Specifically, film crystallinity was assessed via glancing angle x-ray diffraction (GAXRD) using a Rigaku diffractometer with CuKa radiation at 40 kV. Cross-sectional film microstructure was examined using a Hitachi S4500 field emission scanning electron microscope (FESEM). The surface morphology of the constituent films and the composite heterostructure was assessed by a Digital Instrument's Dimension 3000 atomic force microscope (AFM) using tapping mode. Film residual stress was characterized via laser reflection curvature technique using a Tencor system. Rutherford backscattering spectrometry (RBS) was employed to assess film elemental composition, areal thickness, and film-substrate interface quality. The RBS measurements were obtained using 2 MeV He^+ ion beams from an NEC 5SDH-2 tandem positive ion accelerator. All spectra were fit and interpreted using the program RUMP (Doolittle, 1985).

3. RESULTS AND DISCUSSION

The Ta_2O_5 films were fabricated by the MOSD technique using carboxylate-alkoxide precursors. The as-pyrolyzed films (at 350 ^oC) were amorphous in nature and post-deposition annealing was required to obtain fully developed crystalline films, increase the overall grain size of the film, and to remove film strain by filling oxygen vacancies. GAXRD analysis of the films annealed at temperatures ranging from 600 to 750 ^oC, in 50° increments, for 1 hour determined the optimum annealing temperature to be 750 ^oC. At this temperature the films were well-crystallized, single phase, orthorhombic in structure with a preferential (200) orientation. The anneal optimized Ta_2O_5 thin films were characterized for dielectric and insulating properties in the metal-insulator-metal MIM configuration. Figure 2 shows the dielectric permittivity and dissipation factor of the 100 nm thick Ta_2O_5 thin film as a function of frequency. The small signal dielectric constant and dissipation factor at a frequency of 100 kHz were 51.8 and 0.008, respectively. The permittivity and loss factor showed no appreciable dispersion with frequency up to about 1 MHz indicating that the values were not masked by any surface layer effects or electrode barrier effects in this frequency range.

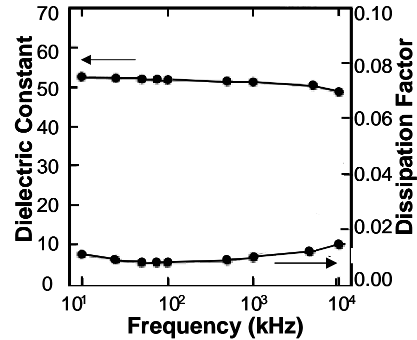


Figure 2. Dielectric constant and dissipation factor as a function of frequency for the 750 ^oC annealed Ta_2O_5 thin film.

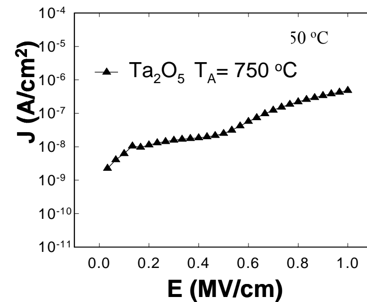


Figure 3. Leakage current density as a function of applied electric field for the 750 ^oC annealed Ta_2O_5 thin films.

Figure 3 displays the leakage current density for the anneal optimized Ta_2O_5 thin film as a function of applied electric field. Leakage current is one of the limiting characteristics of a dielectric material for tunable device applications. The leakage current density of the thin film as a function of applied electric field is an electrical measure of the quality and reliability of a dielectric film (Cole et al., 2000; Saha and Krupanidhi, 2000). Elevated leakage current/low resistivity values suggest poor device reliability and ultimate device failure/breakdown. The low leakage current or enhanced film resistivity value (2.0×10^{12} Ω-cm at 1MV/cm) observed in the present films demonstrates the completeness of phase formation and oxidation of the Ta_2O_5 MOSD fabricated thin films. The

leakage current was observed to increase with applied electric field (Figure 3). It has been suggested that at high fields, grain boundary conduction may be larger than the grain conductivity setting large tunneling currents through these grain boundary layers. However even at these large field strengths the MOSD fabricated Ta_2O_5 films possessed excellent leakage characteristics.

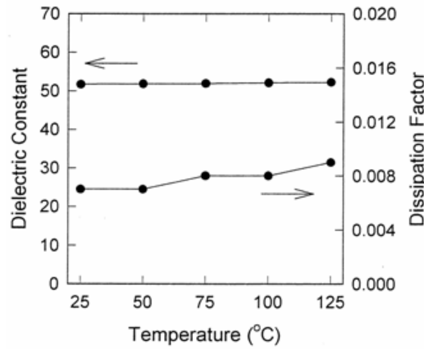


Figure 4. Permittivity and dissipation factor of the Ta_2O_5 thin film buffer layer as a function of measurement temperature from 25 to 125 °C.

In view of the fact that the Ta_2O_5 thin film will serve as an integration layer within the phase shifting element of the antenna its performance must not to perturb the phase shifter's in-service device operation. Thus, for Ta_2O_5 to be of practical use as an integration buffer layer in phase shifting device elements it must possess minimal dielectric dispersion with both temperature and applied bias. For example, an antenna/communication system must perform equally as well in the frigid temperatures of Russia as it does in the deserts of Kuwait, i.e. the antenna performance must not be modified/degraded by environmental ambient conditions such as temperature. It is well established that temperature sensitivity of the phase shifter's tunable (BST film) and/or passive (Ta_2O_5) constituents results in severe performance shortfalls (Wolf and Treger, 2002; Coryell, L., 2003). Such performance shortfalls, namely beam pointing errors and device-to-device phase shift and/or insertion loss variations, are resultant of the highly non-linear temperature response of the constituent dielectric film(s), which make up the phase shifter. Figure 4 displays the dielectric dispersion of the anneal optimized Ta_2O_5 thin films as a function of temperature from 25-125 °C. Both the permittivity and dissipation factor were relatively unchanged with measurement temperature in the range of 25 to 125 °C indicating excellent temperature stability of the buffer layer films. The temperature coefficient of capacitance (TCK) was calculated using the equation $\Delta C/(C_o \Delta T)$, where ΔC is the change in capacitance relative to capacitance C_o at 25 °C and ΔT is the change in temperature relative to 25 °C. The 750 °C anneal optimized films exhibited a low TCK of +114 ppm/°C confirming good reliability and integration integrity of the MOSD fabricated Ta_2O_5 films for buffer layers in phase shifting device elements.

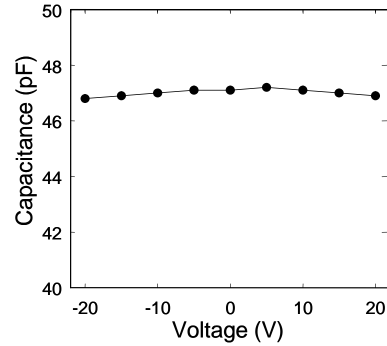
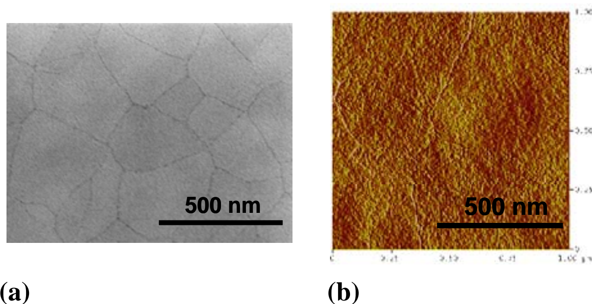


Figure 5. C-V characteristics of 750 °C annealed Ta_2O_5 thin films.

In addition to temperature stability, the buffer layer must not be tunable, i.e. it should be passive and exhibit good bias stability characteristics. Poor bias stability of the buffer layer would interfere with the tunability of the active material in the device and in turn would result in extreme unpredictable and uncorrectable errors in antenna phase shift. Such unexpected phase shift modifications would disable the antenna's ability to receive and/or transmit the information and ultimately result in communication failure. Therefore, it is necessary for the passive buffer layer component (Ta_2O_5) of the phase shifting element to be bias insensitive. The bias stability of the buffer layer film was determined via C-V measurements (Figure 5). The C-V measurements were obtained by applying a small ac signal of 10 mV amplitude and 100 kHz V across a Pt/ Ta_2O_5/Pt capacitor device structure, while the direct current electric field was swept from negative bias to positive bias. The change in film capacitance was determined to be 1.41% for the anneal optimized Ta_2O_5 films at an applied electric field of 1 MV/cm. The loss factor (not shown in Figure 5) also showed excellent bias stability, and was determined to be less than 1% up to 1 MV/cm.

In conjunction with the dielectric properties discussed above there are other materials properties, which must be satisfied for Ta_2O_5 to be a successful candidate as a buffer layer in phase shifting devices. For a buffer layer film to be monolithically integrated between the Si substrate and the overlying active thin film to create a bilayer heterostructure, the underling film (Ta_2O_5) must possess a pristine, surface morphology. In other words, a smooth, continuous, uniform, defect free surface morphology of the Ta_2O_5 film is critical if it is to serve as the "pseudo-substrate" for the growth of the overlying active layer, BST based thin film, in a heterostructure coplanar device configuration. If the Ta_2O_5 film surface is not smooth a rough BST film-Ta_2O_5 interface will result, and this interfacial roughness will in turn promote a rough BST

film surface. In a coplanar microwave device design the top surface of the BST film must be metallized in order to fabricate the electrodes, i.e., the ground and center conductors of the device (Figure 1). There are losses associated with the electrode metallization and the quality of the film-metal electrode interface, which augment to the overall loss of the device. Minimization of film-metal interfacial roughness serves to reduce the conductor loss and improves the overall device loss for microwave frequency operation. Thus, the quality of the conductor-BST film interface is critical, and is strongly dependent on the nature of the buffer layer's surface morphology. Plan-view FESEM and AFM analyses were utilized to evaluate the 750 ^{o}C annealed Ta_2O_5 film surface for feasibility of promoting the growth of a continuous BST film with a uniform/smooth defect free surface morphology. The plan-view FESEM and AFM images of the 750 ^{o}C annealed Ta_2O_5 films on n^+-Si substrates are displayed in Figure 6. The micrographs show that the Ta_2O_5 films exhibited a smooth uniform microstructure with no cracks or defects observed. Furthermore, the microscopy results demonstrate that the Ta_2O_5 films possessed a dense microstructure composed of 200 nm domains, which encase a fine grain nano-crystallite microstructure or subgrains, with a grain size on the order of 25 nm. This domain-type microstructure is more pronounced/visible in the plan-view FESEM micrographs of the film surfaces (Figure 6a). The average surface roughness of the 750 ^{o}C post-deposition annealed films, as quantified by AFM, was found to be <1 nm. Thus, the Ta_2O_5 film surface properties, i.e., extreme uniformity, smoothness, and defect free nature, appear to be well suited for the BST overgrowth.



(a) **(b)**

Figure 6. Surface morphology of the 750 ^{o}C annealed Ta_2O_5 thin films; (a) plan-view FESEM and (b) plan view AFM images.

Subsequent to the optimization of the Ta_2O_5 buffer layer film the challenge of integrating the buffer layer with the active BST thin film was addressed. To accomplish the integration task two different heterostructure processing protocols were evaluated, namely, (1) single anneal protocol and (2) dual anneal protocol. The single anneal process protocol consisted of depositing the Mg doped BST film over a pyrolyzed Ta_2O_5 film and performing a single anneal at 750 ^{o}C to attain crystallization of the heterostructure. The underlying premise of the single anneal protocol was to limit the number of device processing steps by performing the two material depositions sequentially without employing separate crystallization steps for each film. Figure 7 shows the x-ray diffraction patterns of the annealed BST/Ta_2O_5 heterostructure on n^+-Si substrate. From the x-ray spectrum the diffraction peaks form each layer of the heterostructure were easily delineated, that is, the (001), (1,11,0), (201), (002) (1,11,2) peaks were indicative of the Ta_2O_5 layer while the (110), (111), 200) and (211) peaks were attributed to the BST film. The x-ray diffraction results demonstrate that is possible to obtain a well-crystallized bi-layer film heterostructure, i.e., adequate crystallization of the respective thin films, with no evidence of secondary phase formation, via a single anneal process protocol at 750 ^{o}C.

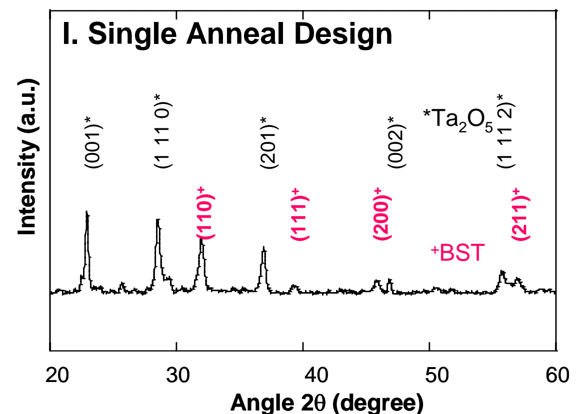


Figure 7. X-ray diffraction pattern from the BST/Ta_2O_5 bi-layer heterostructure on Si fabricated via the single anneal process protocol. The Ta_2O_5 x-ray peaks are denoted with stars (*) and the peaks from the BST are denoted by crosses (+).

Besides the ability to generate the appropriate crystalline phases of each material, it is also necessary that the buffer layer-active layer film interface, (interface between the constituent films) be abrupt/smooth and defect free. The quality of this interface directly influences the surface morphology of the heterostructure, which, in turn, influences the magnitude of conductor loss associated with the metal contacts of the coplanar device. The surface morphology of the integrated heterostructure must be continuous, smooth, uniform, and crack/defect free. The plan-view surface morphology and cross-sectional film microstructure of the single anneal process protocol integrated heterostructure are displayed in Figures 8 and 9, respectively. From figure 8 it is evident that the films surface is neither uniform nor continuous, but instead is heterogeneous or mottled in appearance. The mottled nature of the films surface is most likely due to out-gassing of the organic addenda from the MOSD precursors used to synthesize the Ta_2O_5 film. In other

words the organic addenda was not effectively removed from the film during the pyrolyzation process step, which preceded the deposition of the BST film over-layer.

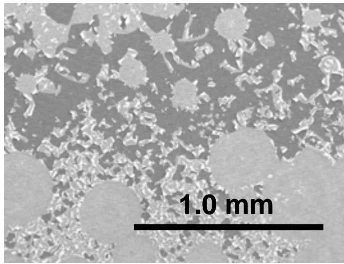


Figure 8. Optical micrograph of the single anneal process protocol bilayer heterostructure surface.

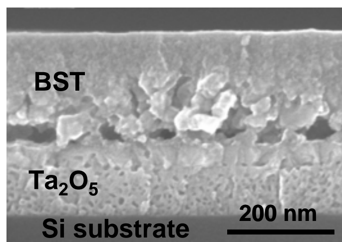


Figure 9. FESEM micrograph showing the cross-sectional microstructure and interface of the BST/Ta_2O_5 heterostructure fabricated via the single anneal process protocol.

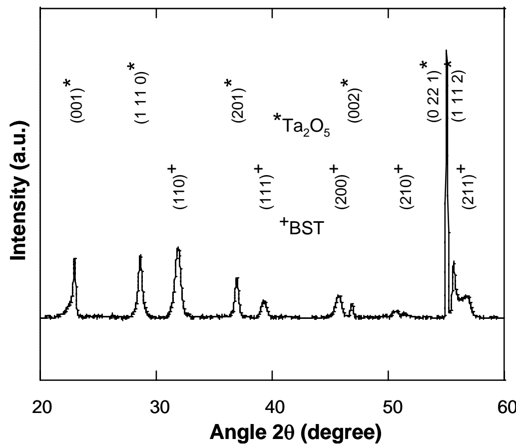


Figure 10. X-ray diffraction pattern from the BST/Ta_2O_5 bi-layer hetrostructure on Si fabricated via the dual anneal process protocol. The Ta_2O_5 x-ray peaks are denoted with stars (*) and the x-ray peaks from the BST are denoted by crosses (+)

Figure 9 displays the cross sectional FESEM micrograph of the bilayer film heterostrurcture. Figure 9 clearly demonstrates that the BST/Ta_2O_5 bilayer does not possess an abrupt defect free interface. In fact, in some areas, the interfacial region possess a roughness on the order of ~50 nm which violates the integration criteria. Due to the irregular interface and non-uniform surface morphology it was determined that the single anneal process protocol is not appropriate for fabricating the monolithic film integration design as shown in Figure 1b.

As an alternative to the single anneal process protocol, the dual anneal process protocol was fabricated and evaluated for integration criteria. Figure 10 displays the x-ray diffraction pattern of the dual anneal process protocol for the BST/Ta_2O_5 heterostructure on n^+-Si substrate. The x-ray diffraction results demonstrated that the films were well crystallized and that the appropriate crystalline phases of each material were present within the heterostructure. As such, the diffraction peaks form each layer of the heterostructure were easily identified and attributed to each of the constituent layers of the heterostructure with no evidence of secondary phases.

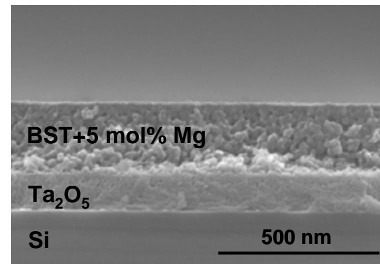


Figure 11. FESEM micrograph showing the cross-sectional microstructure and interface of the BST/Ta_2O_5 bi-layer film heterostructure fabricated via the dual anneal process protocol.

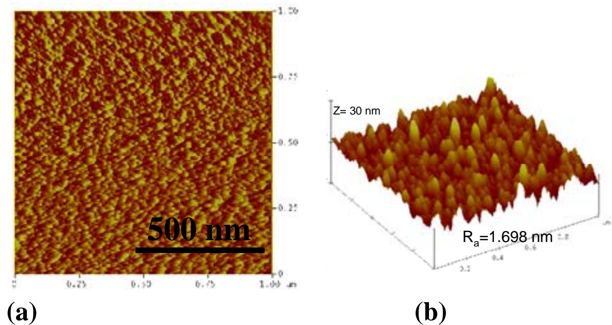


Figure 12. AFM data for the BST/Ta_2O_5 bi-layer film heterostructure fabricated via the dual anneal process protocol: (a) plan view and (b) three dimensional AFM images.

The cross-sectional FESEM micrograph of the dual anneal heterostructure, displayed in Figure 11, demonstrated that the constituent films possessed a dense well-crystallized microstructure with uniform thickness. The FESEM micrograph shows a distinct structural delineation between the bilayer films and between the buffer layer film and the Si substrate. No amorphous layer or voiding/defects were observed at the interfaces. In addition, the surface morphology (Figure 12) of this heterostructure exhibited a dense microstructure with no cracks or defects observed. The surface roughness (Figure 12 b) as quantified by AFM, was ~ 1.7 nm. The excellent crystallinity, defect free structurally abrupt interface in concert with an extremely smooth, uniform and defect free surface morphology bodes well for the

integration suitability of this heterostructure fabricated via the dual anneal process protocol.

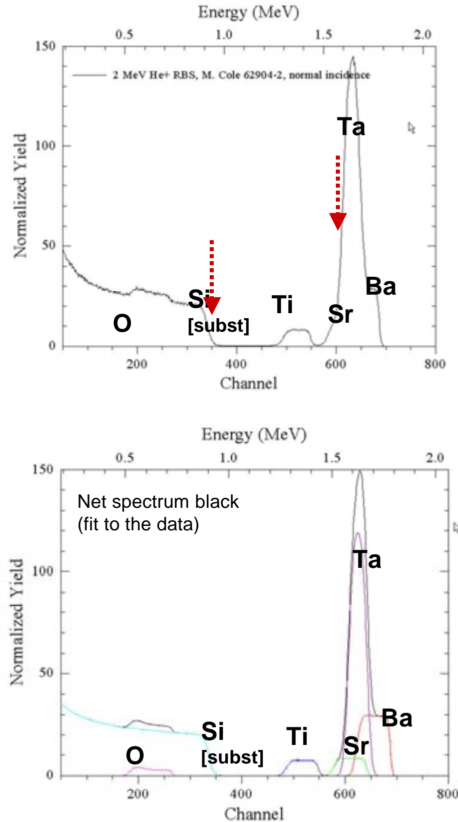
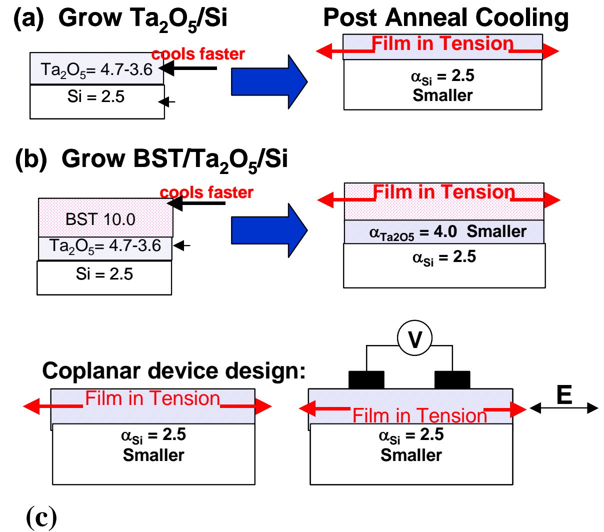


Figure 14. The RBS spectra of the dual anneal process protocol heterostructure: (a) the BST/Ta_2O_5/Si heterostructure data and (b) the BST/Ta_2O_5/Si simulation via RUMP.

For integrated thin-film device applications ideal performance of a coplanar heterosturctural design is best achieved by minimizing chemical imperfections such as variations in stoichiometry of the material. Such stoichiometric variations arise from elemental interdiffusion between the bilayer films and/or between the films and Si substrate. Rutherford backscatter spectroscopy (RBS) analysis was employed to access the prospect of elemental diffusion, and the interfacial quality of the dual anneal process protocol fabricated heterostructure. Specifically, composition, thickness, and interface quality of the constituent bilayer films were determined by comparing the experimental data to a simulation generated by the RUMP RBS analysis package (Doolittle, 1985). The simulated spectrum was derived for an idealized BST/Ta_2O_5/Si heterostructure with no occurrence of elemental interdiffusion within the device structure. Figure 14 displays the RBS spectra for both the experimental data and RUMP simulation. A quantitative comparison of the experimental data with the simulated RBS results revealed no measurable deviation in peak shape and position between the two spectra. From the experimental RBS data (Figure 14a) it was observed that the low energy (back edges) edges of the Ba, Sr, Ti, and Ta peaks (from the bilayer film), and the high energy (front edge) edge of the Si signal from the substrate were sharp/abrupt. The fact that the experimental data is virtually identical to that of the simulation, combined with the peak edge sharpness, indicates that there was negligible interdiffusion within the heterostructrure fabricated via the dual anneal process protocol. The RBS analyses confirmed the BST active thin film to be stoichiometric, i.e. the Ba:Sr ratio was confirmed to be 61.5:38.5. However, the stoichiometry of the Ta_2O_5 buffer layer was found to be $Ta_2O_{5.5}$, that is, the film contained about 10% excess oxygen. This excess oxygen may be due to absorbed water or contamination by low–Z oxides. The film thickness of the Ta_2O_5 and BST layers were determined to be ~100 and 200 nm, respectively, which is in agreement with the cross-sectional FESEM studies.



(c)

Figure 15. Schematic illustrating (a & b) the resultant residual stress due to the effect of CTE mismatch between integrated materials and post-anneal cooling, and (c) the films residual stress depicted in the coplanar device configuration under bias.

Our experimental results suggest that BST can be successfully integrated with affordable Si substrates utilizing a Ta_2O_5 buffer layer and a dual anneal process protocol. However, a major drawback of this device configuration, i.e. coplanar device design, is its lower tunability with respect to that of a parallel plate/vatactor device design (Geyer and Cole, 2004, Wolf and Treger, 2002, Horwitz et al., 1998). We suggest that this device design performance short fall is mitigated by residual stress modification, which is inherent to our BST/Ta_2O_5/Si heterostructure design. Figure 15 (a & b) illustrates this residual stress modification which is resultant from the film CTE integration-mismatch and post-anneal cooling. Since the CTE of Si (2.5×10^{-6} $^{o}C^{-1}$) is much less than that of the Ta_2O_5 buffer layer (4.7×10^{-6} $^{o}C^{-1}$), subsequent to annealing the film will cool such that the Ta_2O_5 is in tension (Tien et al., 2000). The residual

stress of the 750 °C annealed Ta_2O_5 film on Si, measured via laser reflective curvature analysis, and was observed to be 21.9 MPa. The tensile nature of the Ta_2O_5 film is due to the CTE mismatch, post-anneal cooling, and the substrate effect. Specifically, as the Ta_2O_5/Si cools the film shrinks slower than the substrate thus an external force (CTE mismatch-substrate effect) causes the film to be in tension. Similarly, after the BST is deposited over the annealed Ta_2O_5 buffer layer and post-anneal cooled, it too will be in tension. In other words, the fact that the CTE of Ta_2O_5 (4.7 x10^{-6} °C^{-1}) and the Si substrate (2.5x10^{-6} °C^{-1}) are significantly smaller than that of the BST film (10.5 x10^{-6} °C^{-1}), upon cooling the BST film will shrink slower than that of both the buffer layer and the substrate leaving the BST film in tension. The measured residual stress of the heterostructure bilayer (237.4 MPa) strongly supported this assertion. We suggest that this stress modification of the active material, via the integration with the Ta_2O_5 buffer layer and Si substrate, promotes enhanced tunability in the coplanar device design. In theory, in a coplanar device design, if the active thin film (BST) is under tension it is aligned parallel with the applied electric field and this configuration serves to promote the polarization of the electric dipoles (Figure 15c). In contract, an active film in compression constrains the polarization. Thus, this enhanced polarization results in a high capacitance density, which in turn promotes enhanced device tunability.

4. CONCLUSIONS

This investigation demonstrated the feasibility of utilizing MOSD fabricated Ta_2O_5 as a buffer layer film to promote the integration of BST with affordable large area silicon substrates for tunable device applications. The anneal optimized Ta_2O_5 based thin film possessed excellent material properties, namely, an enhanced dielectric constant (ε_r =45.6), low dielectric loss (tan δ=0.006), high film resistivity ($\rho=10^{12}$ Ω-cm at E=1 MV/cm), excellent temperature stability (TCK of 52 ppm/°C), and excellent bias stability of capacitance (~1.41% at 1 MV/cm). The integration of the BST/Ta_2O_5 bilayer heterostructure on Si substrate (in the coplanar device configuration), was demonstrated via two fabrication process methods; (1) the single anneal and (2) the dual anneal process protocols. The non-uniform surface morphology and interfacial roughness associated with the single anneal process protocol deemed this fabrication method inappropriate for monolithic integration of BST and Ta_2O_5 films with Si substrates. In contrast, the defect free, structurally abrupt bilayer and bilayer film-substrate interface; combined with the smooth, uniform and defect free surface morphology of the dual anneal fabricated heterostructure suggest this process protocol to be an excellent method for realizing the successful monolithic integration of BST with affordable Si substrates in a coplanar device design. Our results suggest that it is the combination of material design and anneal process protocol, which promoted enhanced device tunability comparable to that of varactor devices.

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