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12 a. DISTRIBUTION / AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

12 b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

The goal of this project was to develop a complete system for droplet chemistry and biowarfare detection applications based on a programmable dielectrophoretic array concept. In this final reporting period design and testing of the 4th and 5th generation SOI chip was completed. A silicon and glass solid-state microfluidics system was designed at M. D. Anderson and successfully fabricated and integrated with the SOI chip at AppliedMEMS. Simultaneously, cost savings in foundry work permitted an additional iteration in the final design of the integrated electrode array. Identifying and implementing the new microfluidics technology and developing the technique to bond it to the revised SOI chip imposed a delay of some 11 months on the project completion which will was used to integrate the new microfluidics with the revised chip. With the accomplishment of these steps, all of the major aims of the project have been successfully completed. Thus, a programmable fluidic processor platform capable of on-the-fly adaptation to multiple testing challenges and based on dielectrophoretic manipulation of microdroplets has been successfully developed and demonstrated. A complete software solution for programming the system has also been provided. Finally, this new technology has been licensed for commercial development.

14. SUBJECT TERMS

Bioflips; Microfluidics; Biowarfare detection; Lab-on-a-chip; dielectrophoresis; droplet chemistry

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Statement of Problem Studied

To realize the vision of a miniature integrated system adaptable to a broad range of analysis problems, it is important to consider that many problems demand a sequence of disparate preparation operations and perhaps multiple assays. Only after an aggregate of indicators have been assayed in host-based detection, for example, can response to a biowarfare agent be confirmed. To eliminate false alarms, the ability of a detection system to navigate adaptively a sequence of tests would be of advantage. Biowarfare agent detection is the subject of ongoing research and it is also desirable that a detection system developed now should be able to accommodate new assay types, as they are developed, through user-transparent evolutionary upgrades such as the addition of improved software or a new reagent cartridge. Indeed, it would be ideal if detection systems were reprogrammable and could be used quickly to fulfil new or multiple detection needs on the fly, even for agents that are presently unknown. This study was aimed at the realization of a novel, dielectrically-actuated, programmable system for droplet chemistry, appropriate control and programming software, and proof of principle demonstrations of these new technologies.

Scope of Report

This is the fifth and final progress report for this DARPA project that is supported and administered under Army Research Office contract DAAD19-00-1-0515. It covers the period from 1 August 2000 through the end of the contract on 30 September 2004.

Administrative Issues

Subcontracts with Coventor, Inc., Lynntech, Inc., Lawrence Livermore National Laboratory (LLNL), and AppliedMEMS, Inc. were in place as described in our DARPA proposal that forms the basis for this ARO contract. The agreement reached with LLNL for their subcontract was based on a Cooperative Research and Development Agreement (CRADA) between LLNL and UTMDACC for execution of the work planned in this project.

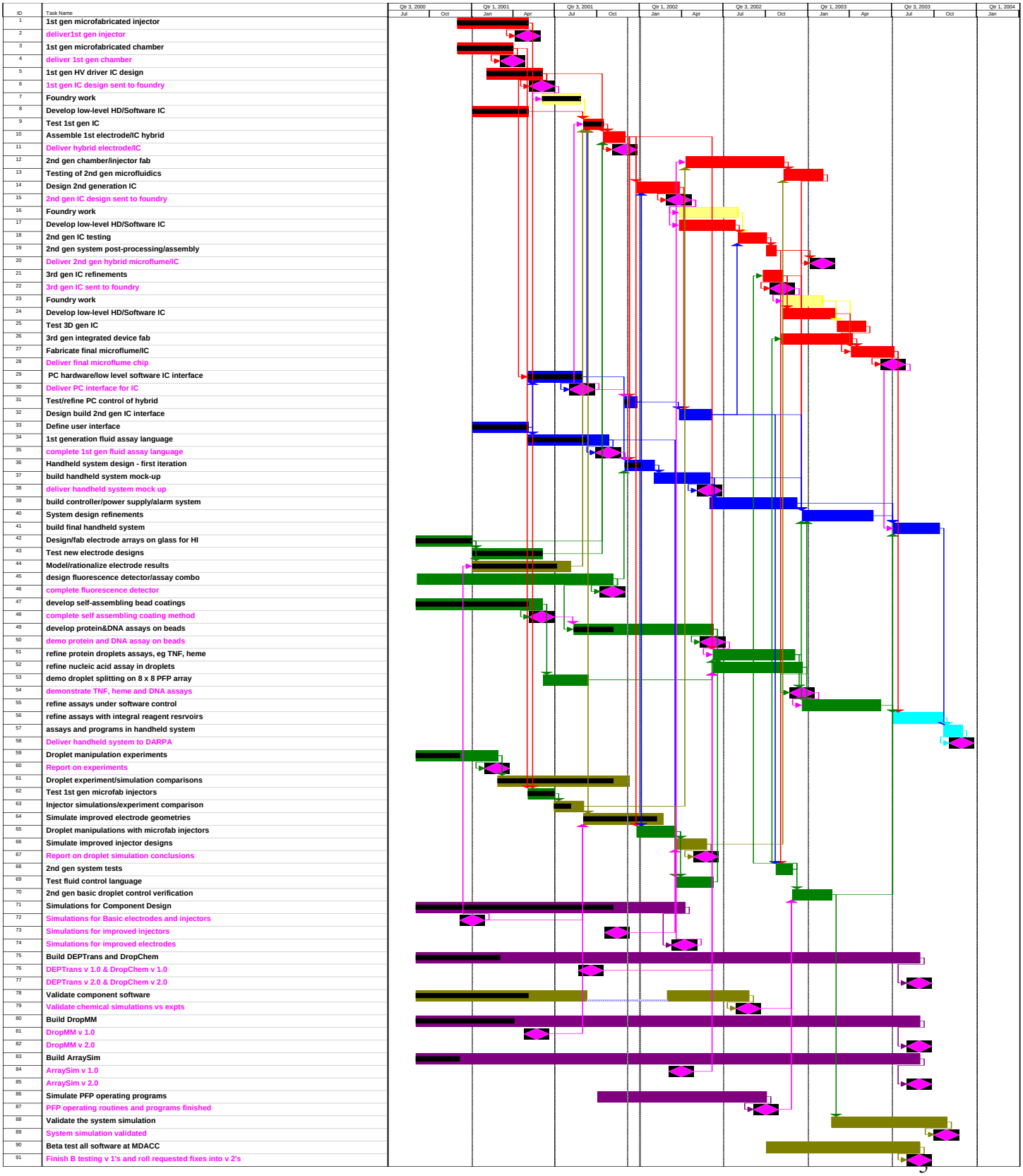
DARPA and ARO agreed to a completion date of September 2004 to accommodate the change from microfluidics components fabricated in PDMS to components fabricated in silicon. The budget for the contract remained unchanged. MDACC adjusted the subcontract completion dates with Lawrence Livermore National Lab, Lynntech, Coventor, and AppliedMEMS Inc. accordingly.

Report on Research

The planned schedule for execution of research tasks, as proposed for DARPA and encompassed in our ARO contract, are delineated in the Gantt chart shown later in this section. This chart shows the originally forecast duration of tasks, their interrelationships and dependencies, and the organizations within our teams responsible for their execution. Apart from stretching out the timeline to August 2004, no significant change in tasks is occurred. Following the Gantt chart is a list of the deliverables for the project, followed by a list of the Publications and Patents derived from this work, and detailed descriptions of work undertaken on various tasks during the period covered by this report. To allow easy cross-reference, the same numbers in the Gantt chart, List of Deliverables, and Progress Details identifies specific tasks.

Gantt Chart of Project

The task and deliverable numbers are used for reference throughout this report



List of Deliverables

Gantt #	Tasks	Corresponding deliverables
1	1st gen microfabricated injector	
2		deliver1st gen injector
3	1st gen microfabricated chamber	
4		deliver 1st gen chamber
5	1st gen HV driver IC design	
6		1st gen IC design sent to foundry
7	Foundry work	
8	Develop low-level HD/Software IC	
9	Test 1st gen IC	
10	Assemble 1st electrode/IC hybrid	
11		Deliver hybrid electrode/IC
12	2nd gen chamber/injector fab	
13	Testing of 2nd gen microfluidics	
14	Design 2nd generation IC	
15		2nd gen IC design sent to foundry
16	Foundry work	
17	Develop low-level HD/Software IC	
18	2nd gen IC testing	
19	2nd gen system post-processing/assembly	
20		Deliver 2nd gen hybrid microflume/IC
21	3rd gen IC refinements	
22		3rd gen IC sent to foundry
23	Foundry work	
24	Develop low-level HD/Software IC	
25	Test 3D gen IC	
26	3rd gen integrated device fab	
27	Fabricate final microflume/IC	
28		Deliver final microflume chip
29	PC hardware/low level software IC interface	
30		Deliver PC interface for IC
31	Test/refine PC control of hybrid	
32	Design build 2nd gen IC interface	
33	Define user interface	
34	1st generation fluid assay language	
35		complete 1st gen fluid assay language
36	Handheld system design - first iteration	
37	build handheld system mock-up	
38		deliver handheld system mock up
39	build controller/power supply/alarm system	
40	System design refinements	
41	build final handheld system	
42	Design/fab electrode arrays on glass for HI	
43	Test new electrode designs	
44	Model/rationalize electrode results	
45	design fluorescence detector/assay combo	
46		complete fluorescence detector
47	develop self-assembling bead coatings	
48		complete self assembling coating method
49	develop protein&DNA assays on beads	
50		demo protein and DNA assay on beads
51	refine protein droplets assays, eg TNF, heme	
52	refine nucleic acid assay in droplets	
53	demo droplet splitting on 8 x 8 PFP array	
54		demonstrate TNF, heme and DNA assays
55	refine assays under software control	
56	refine assays with integral reagent resrvoirs	
57	assays and programs in handheld system	
58		Deliver handheld system to DARPA
59	Droplet manipulation experiments	
60		Report on experiments
61	Droplet experiment/simulation comparisons	
62	Test 1st gen microfab injectors	
63	Injector simulations/experiment comparison	
64	Simulate improved electrode geometries	
65	Droplet manipulations with microfab injectors	
66	Simulate improved injector designs	
67		Report on droplet simulation conclusions
68	2nd gen system tests	

List of Deliverables (cont'd)

69	Test fluid control language	
70	2nd gen basic droplet control verification	
71	Simulations for Component Design	
72		Simulations for Basic electrodes and injectors
73		Simulations for improved injectors
74		Simulations for improved electrodes
75	Build DEPTrans and DropChem	
76		DEPTrans v 1.0 & DropChem v 1.0
77		DEPTrans v 2.0 & DropChem v 2.0
78	Validate component software	
79		Validate chemical simulations vs expts
80	Build DropMM	
81		DropMM v 1.0
82		DropMM v 2.0
83	Build ArraySim	
84		ArraySim v 1.0
85		ArraySim v 2.0
86	Simulate PFP operating programs	(now 50% Lynntech task)
87		PFP operating routines and programs finished
88	Validate the system simulation	
89		System simulation validated
90	Beta test all software at MDACC	

Publications – peer-reviewed

1. Vykoukal, Jody V., "Dielectrophoresis-Based Analyte Separation and Analysis", Doctoral Dissertation, University of Texas Graduate School of Biomedical Sciences, 2001.

2. Schwartz, Jon A., "Dielectrophoretic Approaches to Sample Preparation and Analysis", Doctoral Dissertation, University of Texas Graduate School of Biomedical Sciences, 2001.

3. Vykoukal, J., Schwartz, J., Becker, F. and Gascoyne, P. "A programmable dielectrophoretic fluid processor for droplet-based chemistry" in in *Micro Total Analysis Systems 2001*, J. M. Ramsey and A. van den Berg (eds) (Kluwer Academic Publishers, The Netherlands, 2001), pp 72-74.

4. Vykoukal, J., Sharma, S., Mannering-Vykoukal, D., and Gascoyne, P.R.C. Engineered Dielectric Microspheres for use in Microsystems, in Micro Total Analysis Systems 2002: Vol I, Y. Baba et al.(eds) (Kluwer Academic Publishers, The Netherlands, 2002), 335-337.

5. Wang, X-J., Becker, F.F. and Gascoyne, P.R.C., Membrane dielectric responses indicate induced apoptosis in HL-60 cells more sensitively than surface phosphatidylserine expression or DNA fragmentation, Biochim. Biophys. Acta, 1564:412-420, 2002.

6. Ratanachoo, K., Gascoyne, P.R.C., and Ruchirawat, M., Detection of cellular responses to toxicants by dielectrophoresis, Biochim. Biophys. Acta , 1564:449-458, 2002.

7. Gascoyne, P.R.C., Cell Dielectric Properties as Diagnostic Markers for Tumor Cell Isolation, in Tumor Markers — Physiology, Pathobiology, Technology, and Clinical Applications, E.P. Diamandis, editor, (AACC press, New York, 2002), Chapter 53.

8. Gascoyne, P.R.C., Ruchirawat, M., Satayvivad, J., Ratanachoo, K., and Becker, F.F., in The Fourth Princess Chulabhorn International Science Congress: Chemicals in the 21st Century, Trinity Publishing Co, Bangkok, pp. 495-504 (copyright 1999 publ. 2002).

9. Vykoukal, J. and Gascoyne, P.R.C. Invited review: Particle separation by dielectrophoresis, Electrophoresis, 23:1973-1983 (2002).

10. Cristofanelli, M., De Gasperis, G., Zhang, L., Hung, M-C., Gascoyne, P.R.C., and Hortobagyi, G.N. Automated electrorotation to reveal dielectric variations related to HER2/neu overexpression in MCF-7 sublines, Clin. Cancer Res., 8:615-619, 2002.

11. Gascoyne, P., Mahidol, C., Ruchirawat, M., Satayavivad J., Watcharasit, P., and Becker, F. Microsample preparation by dielectrophoresis: isolation of malaria, Lab on a Chip, 1:(in press), 2002.

12. Gascoyne, P., Mahidol, C., Ruchirawat, M., Satayavivad, J., Watcharasit, P., Becker, F., Microsample preparation by dielectrophoresis: isolation of malaria, 2002, Lab on a Chip, 2002, 70-75.

13. Gascoyne, P., Satayavivad, J., and Ruchirawat, M., Microfluidic approaches to malaria detection, 2004, Acta Tropica, 89:357-369.

14. Vykoukal, J., Vykoukal, D., Sharma, S., Becker, F. F., and Gascoyne, P. R. C., Dielectrically Addressable Microspheres Engineered Using Self-Assembled Monolayers, 2003, Langmuir, 19: 2425-2433.

15. Schwartz, J., Vykoukal, J., Gascoyne, P. R. C., Droplet-based chemistry on a programmable micro-chip, 2004, Lab on a Chip, 4:11-17.

16. Gascoyne, P. R. C., Vykoukal, J. V., Schwartz, J. A., Anderson, T. J., Vykoukal, D. M., Current, K. W., McConaghy, C., Becker, F. F., and Andrews, C., Dielectrophoresis-based Programmable fluidic processors , lab-on-a-chip (invited), 2004, Lab on a Chip 4(4):299-309.

17. Zeng, J., Korsmeyer, F. T., Liquid Disintegration: Investigation of Physics by Simulation, 2004, to appear at Nanotech 2004, Boston, Massachusetts, March 7-11, 2004.

18. Zeng, J., Korsmeyer, F. T., Principles of droplet electrohydrodynamics for lab-on-a-chip (invited), 2004, Lab on a Chip, June 2004.

Publications – non peer-reviewed

1. Korsmeyer, F. T., Zeng, J., The Computational Challenges of Microsystem Simulation, 2003, SIAM News, 36(4) 3, published by Society for Industrial and Applied Mathematics (SIAM), May 2003.

Presentations

1. Vykoukal, J., Schwartz, J., Becker, F. F., Gascoyne, P. R. C., "A Programmable Dielectrophoretic Fluid Processor for Droplet-Based Chemistry", MicroTAS 2001, Monterey, CA, 21-25 October 2001.

2. Zeng, J., Sobek, D., Korsmeyer, F. T., Electro-Hydrodynamic Modeling of Electrospray Ionization: CAD for a μFluidic Device – Mass Spectrometer Interface, 2003, Transduers'03 Digest of Technical Papers, pp.1275-1278, the 12th Int. Conf. on Solid-State Sensors, Actuators and Microsystems, Boston, MA, June 8-12, 2003.

3. Zeng, J. and Korsmeyer, F. T., (2003) "Computational Prototyping of the Programmable Fluid Processor", 5th Annual BioMEMS - Analytical Devices and Applications, San Jose, CA, June 15-17, 2003.

4. Zeng, J., Computational Prototyping for Bio-MEMS (invited), 2003, 5th Annual BioMEMS - Analytical Devices and Applications, San Jose, CA, June 15-17, 2003.

New Patents

Granted

"Microfluidic DNA sample preparation method and device", US patent # 6,352,838, issued 5 March 2002.

"Microfabricated AC impedance sensor", US patent # 6,437,551, issued 20 August 2002.

"Methods and apparatus for programmable fluid processing". U.S. Patent No. 6,294,063, awarded September 25, 2001.

Pending

"Dielectrically-engineered microspheres", World Intellectual Property Organization #WO 10/96023A2, published 20 December 2001.

"Apparatus and method for fluid injection", World Intellectual Property Organization #WO 10/96024A2, published 20 December 2001.

"Forming and modifying dielectrically engineered microparticles", U.S. patent application #10/027,782, filed 20 December 2001.

"Dielectric gate and method for fluid injection and control", U.S. patent application #10/028,945, filed 18 May 2002.

"Systems and Methods for Cell Subpopulation Analysis," U.S. Patent Application Serial No. 09/883,110, [MDA00-036], filed June 14, 2001.

"Apparatus and Method for Fluid Injection," Serial No. 60/211,516, U.S. Patent Application Serial No. 09/883,109, [MDA00-037], filed June 14, 2001.

"Dielectrically-Engineered Microparticles," U.S. Patent Application Serial No. 09/883,112, [MDA99-043], filed June 14, 2001.

"Method and Apparatus for Combined Magnetophoretic and Dielectrophoretic Manipulation of Analyte Mixtures," Serial No. 60/211,757, filed June 14, 2001.

"Particle Impedance Sensor Based on a Multi-Electrode, Inline Design,"[MDA01-047], invention disclosure, filed March 8, 2001.

"Droplet-based microfluidic oligonucleotide synthesis engine", United States Patent Application #20030170698, published September 11, 2003.

"Wall-less channels for fluidic routing and confinement", United States Patent Application #20030173223, published September 18, 2003.

Advanced Degrees Earned by Project Personnel

1. Jody V. Vykoukal, Ph. D. in Biophysics, University of Texas Graduate School of Biomedical Sciences, Oct. 2001. Thesis entitled: "Dielectrophoresis-Based Analyte Separation and Analysis".

2. Jon A. Schwartz, Ph. D. in Biophysics, University of Texas Graduate School of Biomedical Sciences, Oct. 2001. Thesis entitled: "Dielectrophoretic Approaches to Sample Preparation and Analysis".

Summary of Most Important Results
Tasks 21-25. 3rd Generation IC

Programmable Fluidics Processor ver. 5 (PFP5)
High Voltage SOI CMOS 32x32 Electrode Array Driver Chip
Description

Wayne Current, Kelvin Yuk
ECE Dept
UCD

General Description

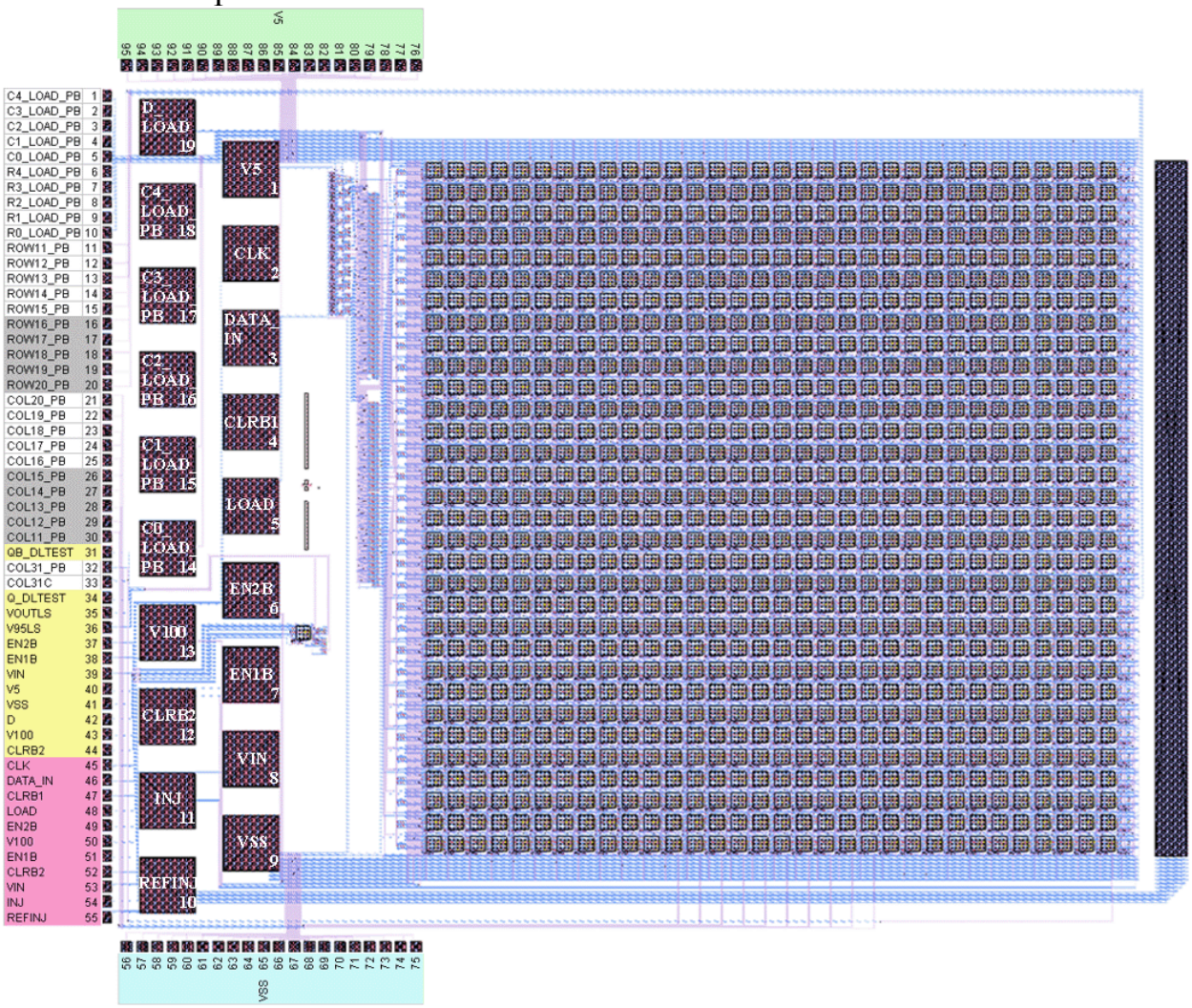


Figure 1. PFP5 Electrode Driver Chip Layout with labeled bond pads and pogo pads. The color coding of the bond pads categorizes them by type according to the color coding chart in Table 5.

The PFP5 chip will be bonded to the MEMs fluidics chamber to create the prototype integrated PFP5 system. The layout of the PFP5 chip is shown in Figure 1. The chip has a 32x32 array of electrode/electrode-driver-electronics cells (or pixels). The chip is approximately 8210 μm high and

10010μm wide. The chip will be bonded to the MEMs fluidic structure such that the fluidic chamber is on top of the 32x32 array of electrodes. Each pixel area is a 200μm square area that contains the electrode driver electronics and the pixel electrode. The electrodes are 133μm square areas of Metal 3 that lie 67μm apart from each other. Each electrode rests on top of its driver circuitry. The electrodes also have a pitch of 200μm in both directions. A 300μm-wide injection reference electrode spans the height of the array and is located 400μm to the right of the right-most column's (column 31) cells' electrodes. The injection reference electrode is composed of all the conducting layers found in a bonding pad and is independently controlled externally to support droplet injections. The fluid injectors' tips within the MEMs structure will lie over column-31-electrodes and the injector reference electrode will provide a reference electric field to the injector fluid reservoir chambers. A serial communications shift register receives the pixel data and addresses one frame at a time. Injection reference electrode signal and additional injection data are provided independently of the serial register.

The PFP5 chip is fabricated by Xfab in 1-micron SOI CMOS technology. The PFP system found on the chip is composed of the electrode array, an 11-bit serial communication shift register, two array address decoders, injection circuitry for realizing a third electrode output state, an injection reference electrode and appropriate signal buffers. The test cells on PFP5 comprise of a single driver test cell, a revised version of the D latch without a metal 3 jumper and a high voltage level shifter circuit. Signals to the PFP system are routed to nineteen large "pogo" pin interconnection pads and 95 standard bonding pads. Originally, the nineteen large pogo pads were to be used for external interfacing of the PFP5 chip as a part of the prototype test device. However, they are not to be used in the new prototype version and kept for possible bonding. The pogo pad signal descriptions are shown in Table 3. The PFP5 signals are primarily routed to the bonding pads and are comprised of control signals for the PFP system and test structures. The bonding pad signal descriptions are shown in Table 4.

Operation of the PFP5 System

The PFP5 System consists of the 11-bit serial input communications shift register (SR), the row- and column-decoders, the 32x32 electrode and digital driver array, signal buffers for largely loaded cells, the injection column of circuitry and the injection reference electrode. During the data load of programming cycle, the communications shift register receives first the 5-bit column-address, next the 5-bit row-address and finally the new phase data bit. Once the data is completely loaded into the shift register, a LOAD signal is enabled, allowing the addresses to pass to the address decoders and the new phase data bit to pass to the input latch of every array cell. The row and column decoders decode the row and column address data and enable the corresponding ROW and COL lines. This allows the memory of the targeted cell to latch in the new phase data. Once the EN1B signal is enabled, the data is then latched into the input latch of the dual latch memory of the targeted driver cell. The programming process is repeated for the desired number of cells, and after the desired pixel updates loaded, the data in the pixel memories are simultaneously transferred to the electrode drivers by the signal EN2B. The new phase data determines the phase of the output at that cell. All electrode memories are updated simultaneously so that all electrodes that change states do so at the same time. Data in the electrode memories direct the electrode driver circuits to output a signal with a phase corresponding to the data bit. A set of three programming cycles followed by a simultaneous output update of the driver array is shown in Figure 2. The cells are first addressed and programmed sequentially with the new desired phase output state and then the entire array outputs are updated simultaneously.

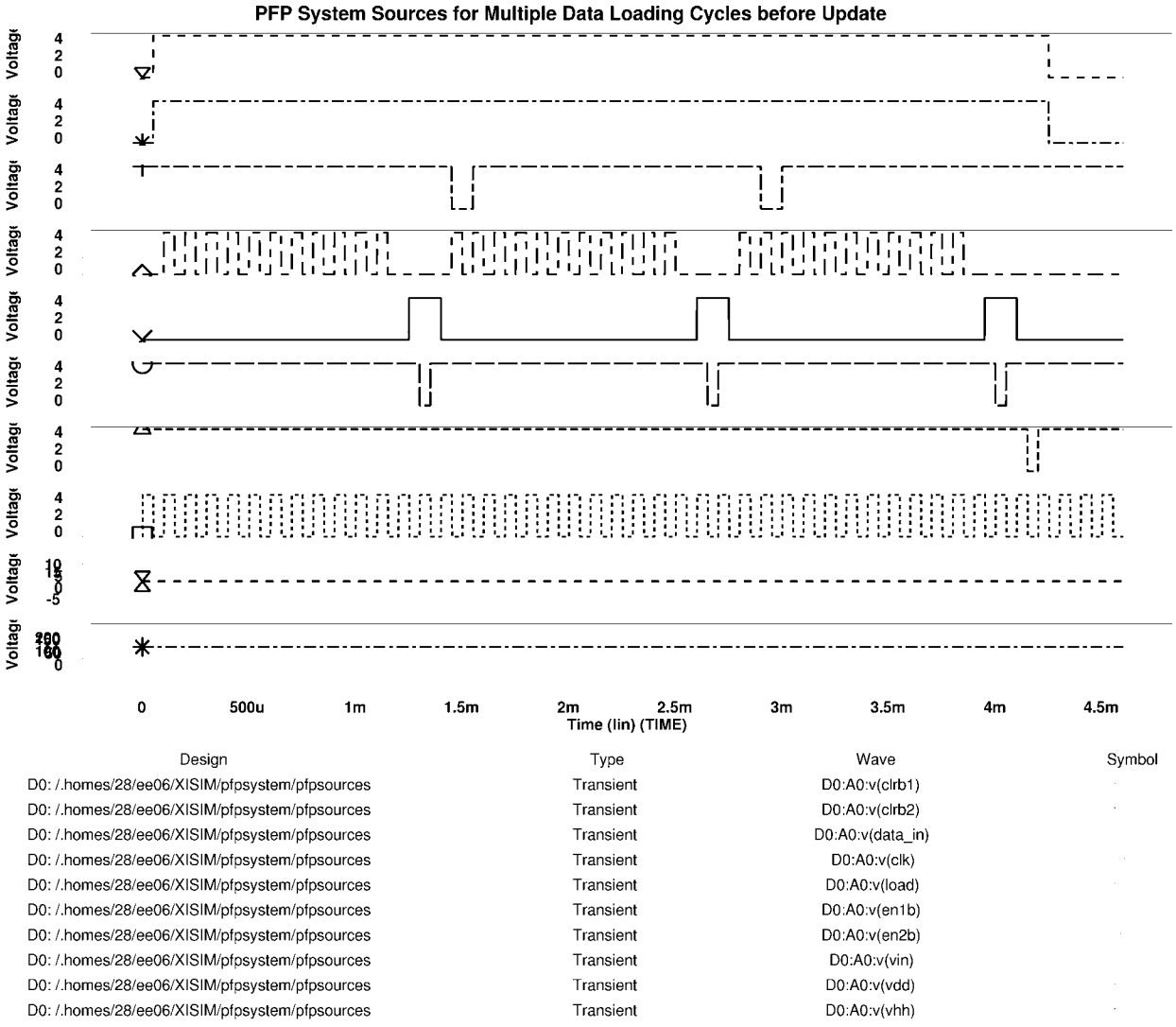


Figure 2. Timing diagram for the operation of PFP showing three programming cycles and a simultaneous output update

A single programming cycle for the driver cell at location (row 10, column 21) is shown in Figure 3. Here, the address and phases data are first loaded into the shift register. Once all the shift register data is loaded in, the CLK enable on the shift register is stopped and the LOAD signal passes the addresses to the decoders. The decoders decode the address and enable the 10^{th} row and the 21^{st} column lines as shown in the figure. The EN1B signal is enabled followed by the EN2B to update the output of (10,21). When EN2B is enabled, the output changes phases by 180 degrees as expected.

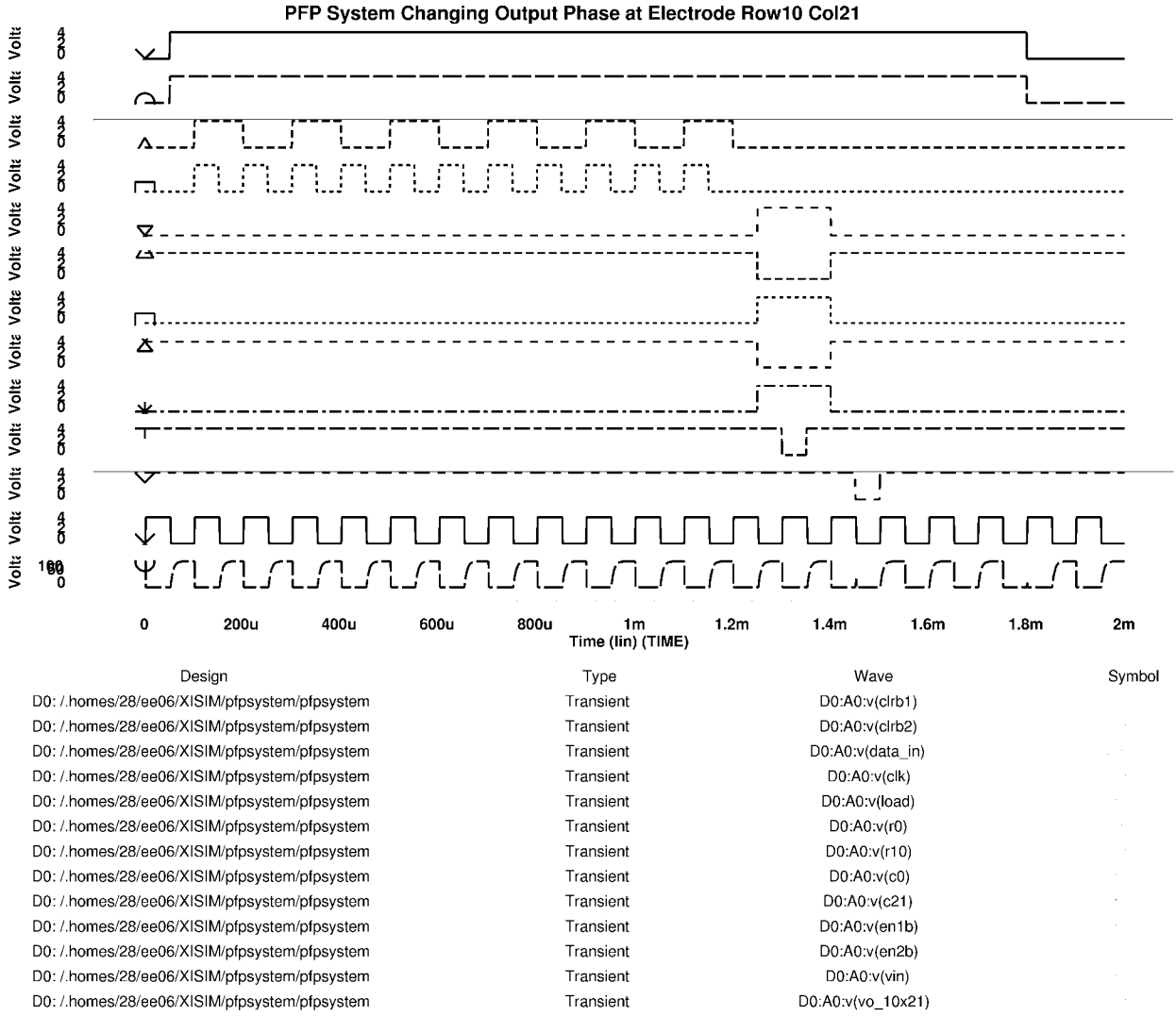


Figure 3. Timing diagram for the programming cycle of the PFP

Loading the Shift Register

The 11-bit communications shift register, its output enabling circuitry and data buffers are shown in detail in Figure 4. Data comes on chip through a bonding pad or a pogo pin pad at the input DATA_IN. CLRB1 is an asynchronous active-low reset that forces the SR outputs to logical ZERO. The signal names used on the chip are shown in Figure 4. The shift register uses a dual latch for each register element, each of which is composed of two active-low D latches cascaded in a master-slave configuration. The first latch (input latch) is enabled by the CLKB signal generated from the CLK signal through an inverter, and the second latch (output latch) is enabled by the CLK signal. When CLK is high, CLKB is low and the input latch latches the data at its input. Then when CLK goes low, the second latch latches the output of the input latch and outputs that data. Therefore, the dual latch system requires that CLK first rise to a logic high level and then fall to a logic low level before the data is output from the shift register to the parallel LOAD gates.

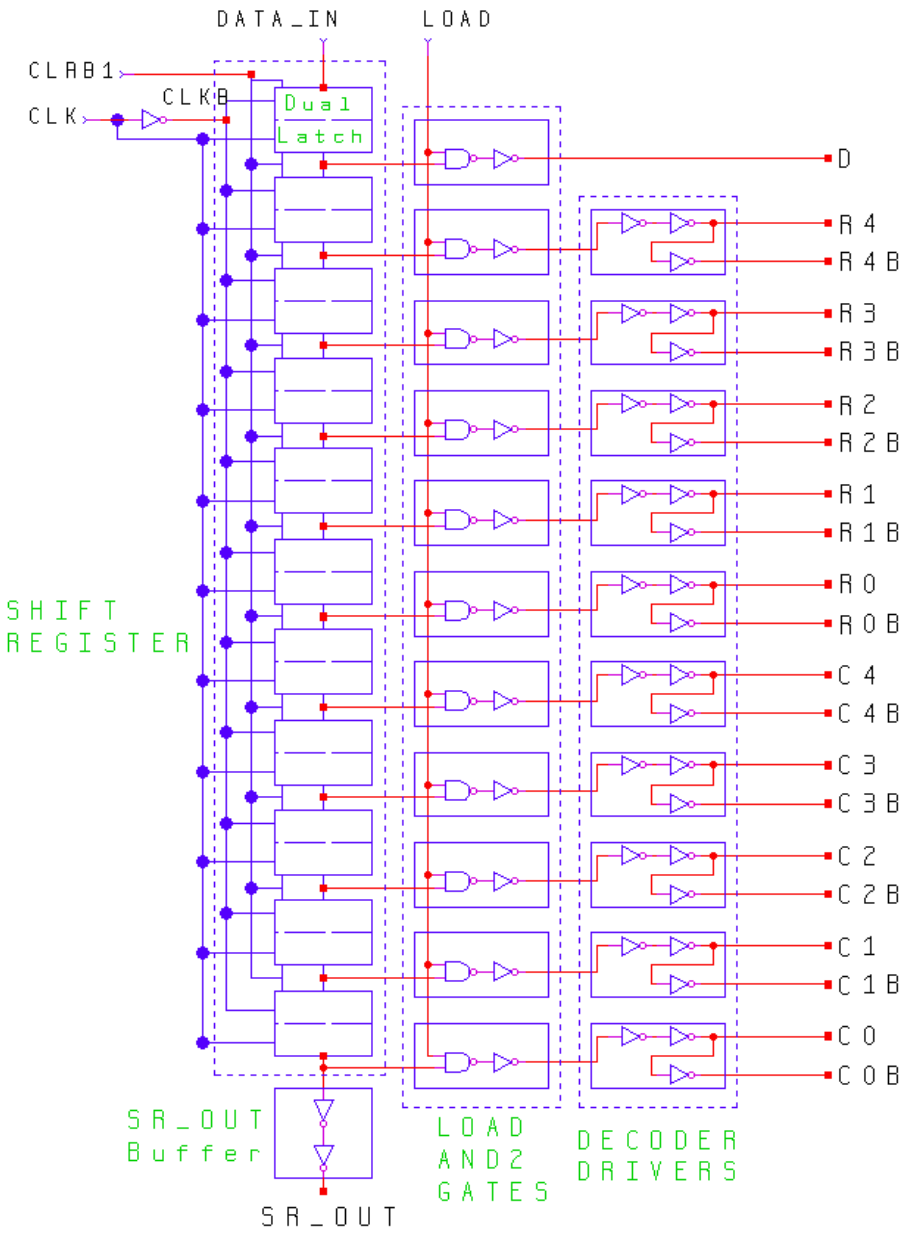
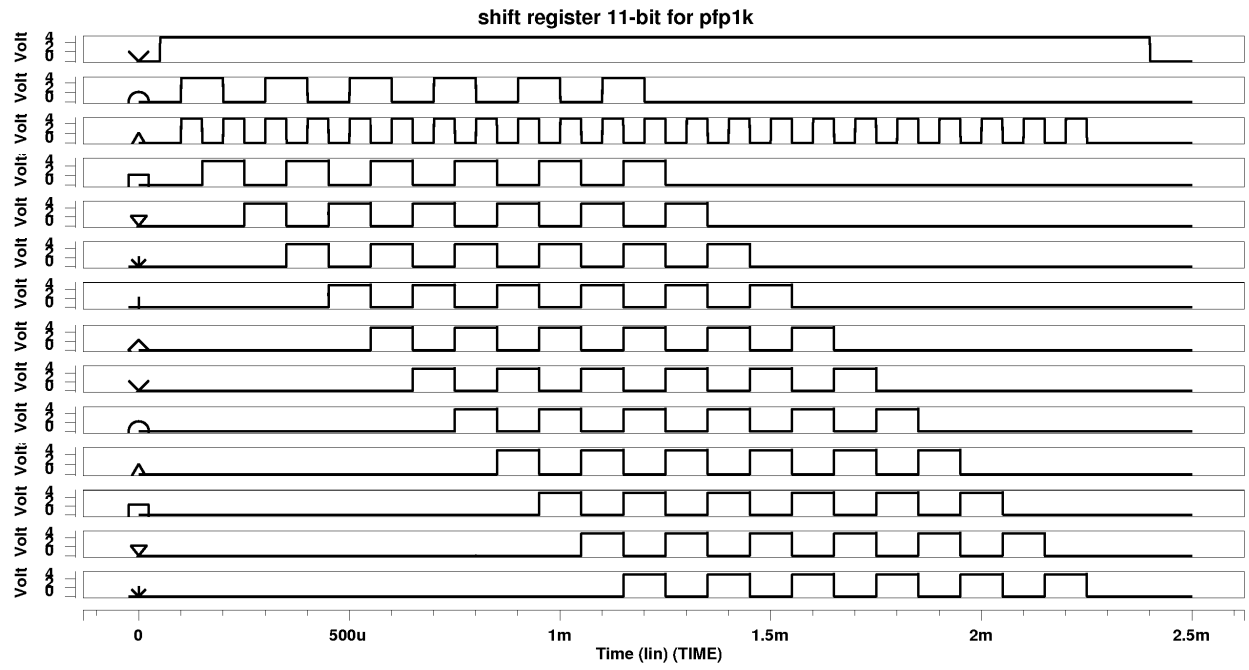


Figure 4. Schematic of 11-bit serial communications shift register with 11 2-input AND gates controlling the parallel outputs of the shift register and decoder driving buffers
NOTE: The signal names in Figure 4 have "_LOAD_PB", "_LOAD" or "_PB" appended to them in Tables 4, 5, and 7. The "_LOAD" indicates that the data is valid only after LOAD is logical 1. The "PB" indicates that the signal is the output of the buffer (post-buffered).

A timing diagram showing the operation of the shift register is given in Figure 5. In the simulation, an alternating series of logic low and logic high data are sent into the DATA_IN input and clocked into the shift register. Each of the shift register's eleven outputs are shown copying the same pattern of bits but in the proper delayed sequence.



Design	Type	Wave	Symbol
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(clrb1)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(data_in)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(clk)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(sr10)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(sr9)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(sr8)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(sr7)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(sr6)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(sr5)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(sr4)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(sr3)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(sr2)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(sr1)	
D0: /.homes/28/ee06/XISIM/pfpsystem/sr11	Transient	D0:A0:v(sr0)	

Figure 5. Timing diagram for the operation of the shift register

Decoding the Pixel Address

Figure 4 shows the communication SR's 11 parallel output signals going to 11 2-input AND (AND2) gates that allow the 11 bits of SR signals to propagate into the 32x32 array only after the LOAD signal is enabled high. The outputs of the 11 AND2 gates for the row- and column-addresses and the input data D are shown in Figure 4. When LOAD is asserted, the row- and column-addresses are passed to the respective row- and column-decoders, which produce a logic high value at the row and column line corresponding to the address loaded into the shift register. The driver cell at row 0 and column 0 is the lower leftmost cell in the 32x32 array. The row number increases from the bottom to the top while the column number increases from the left to the right of the array. Each pixel in the 32x32 electrode array must be addressed individually to write data into that pixel.

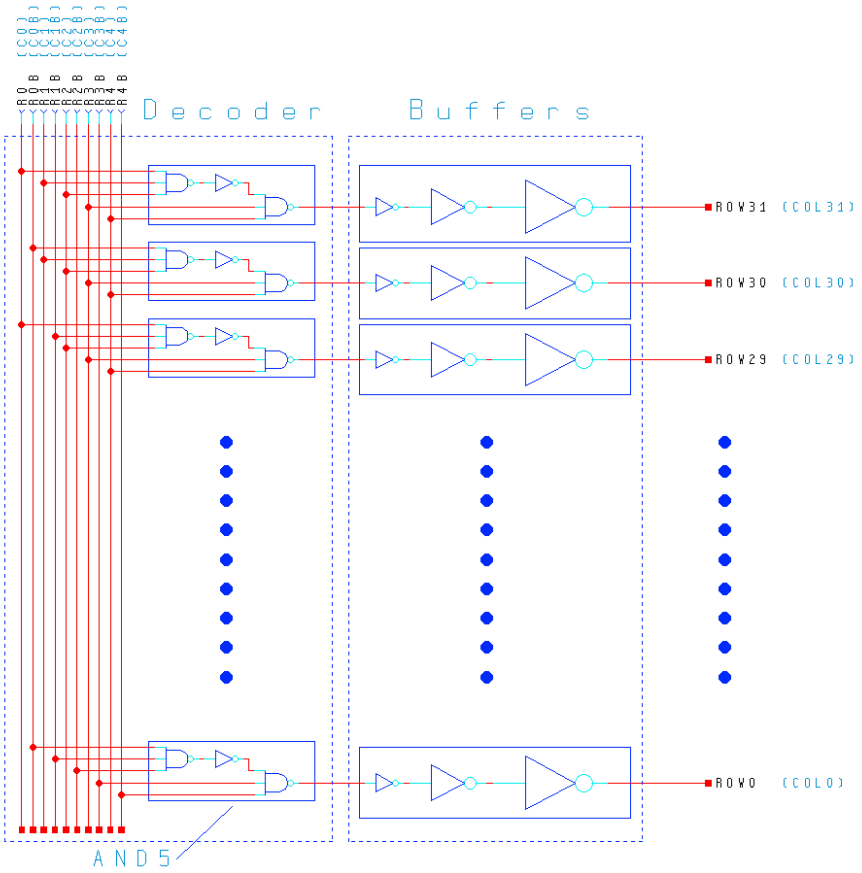


Figure 6: Gate-level schematic of the 5-bit address decoder and output buffers configured for the ROW address. NOTE: The signal names in Figure 5 have "_LOAD_PB", "_LOAD" or "_PB" appended to them in Tables 4, 5, and 7. The "_LOAD" indicates that the data is valid only after LOAD is logical 1. The "PB" indicates that the signal is the output of the buffer (post-buffered).

The gate-level decoders are shown in Figure 6. The decoder has 32 elements, each corresponding to a single permutation of the 5-bit address. Each of the decoder element is composed of a 5-bit NAND gate (NAND5) and an three-inverter output buffer for driver the large loads of each row or column line. The decoders used for the row and column addresses are identical

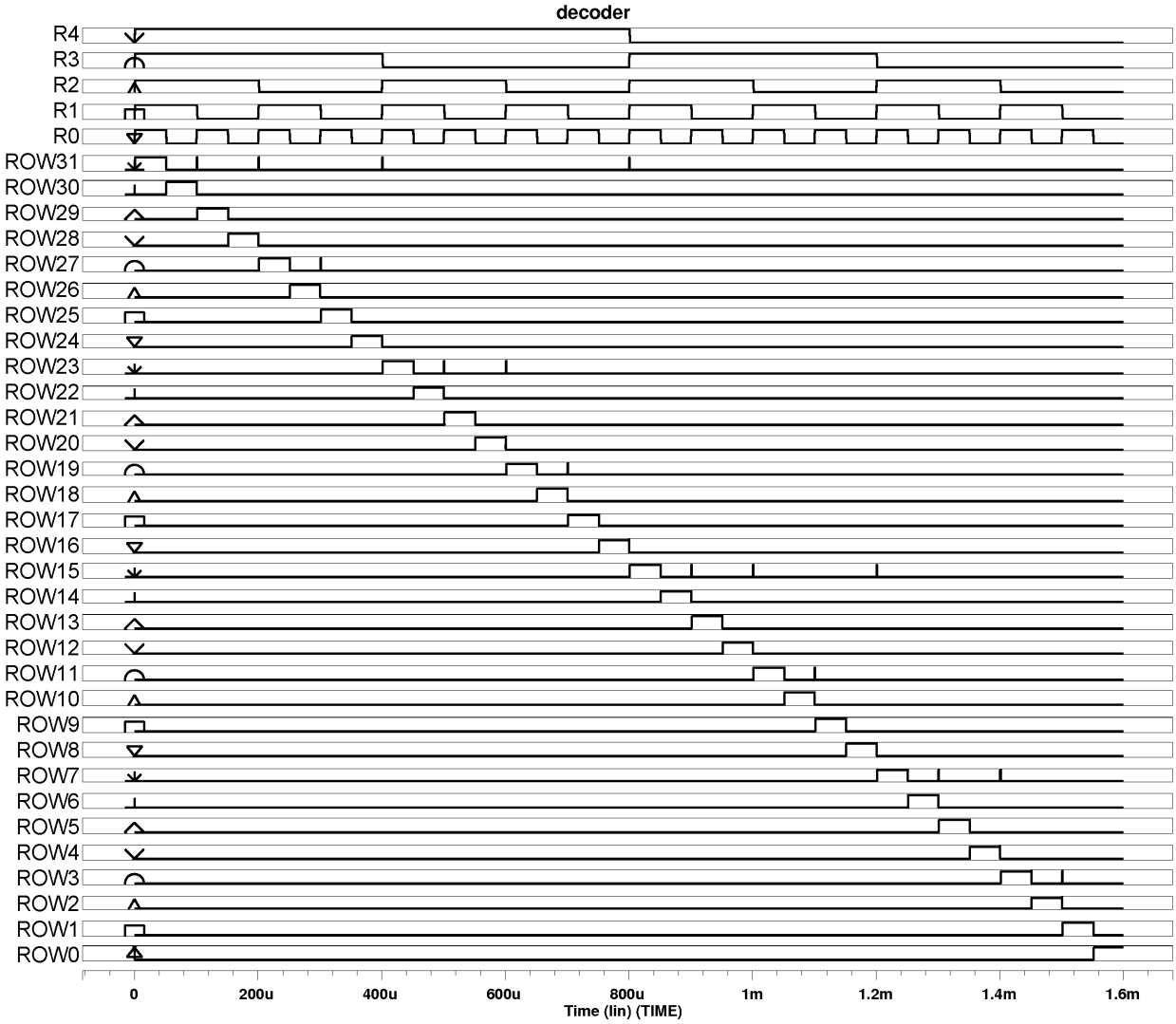


Figure 7. Decoder timing diagram configured for the ROW address bits and enable signals

The operation of the decoder is shown in Figure 7 configured for the ROW address. The simulation shows all the possible combinations of the the 5-bit address as the input to the decoder, and the decoder enabling the corresponding output for every one of those addresses. There are 32 possible combinations and therefore 32 rows and 32 columns of the PFP5 array.

Dual Latching Data into Pixel-Electrode Memory

The memory and enable circuitry or the driver cell is shown in Figure 8. Each driver cell has a dual latch memory, with each latch independently enabled. The input latch records the new phase data assigned to that pixel, and the output latch holds the old latch data and controls the phase of the electrode output through the electrode driver circuit. The asynchronous clear signal CLRB2 will reset every latch in the array. The new phase data from the shift register is passed to every pixel's input latch at the input D_DD as shown in Figure 8. When the row (ROW1 in the figure) and column (COL2 in the figure) line for a particular pixel are enabled and the EN1B signal is also pulsed, the data at D_DD is stored into the input latch of the pixel memory. If all 32x32 pixels are to be updated with new phase data, then 1024 frames must be loaded into the communications register, and 1024 bits of data must be written to the pixel input memory. When all of the new phase data have been loaded in each cell's pixel memory, then all the electrode memory latches are updated with EN2B and all the electrode outputs are updated simultaneously. In Figure 8 the signals C and CB of the latch are used to control the phase of the signal generated by the digital driver amplifier.

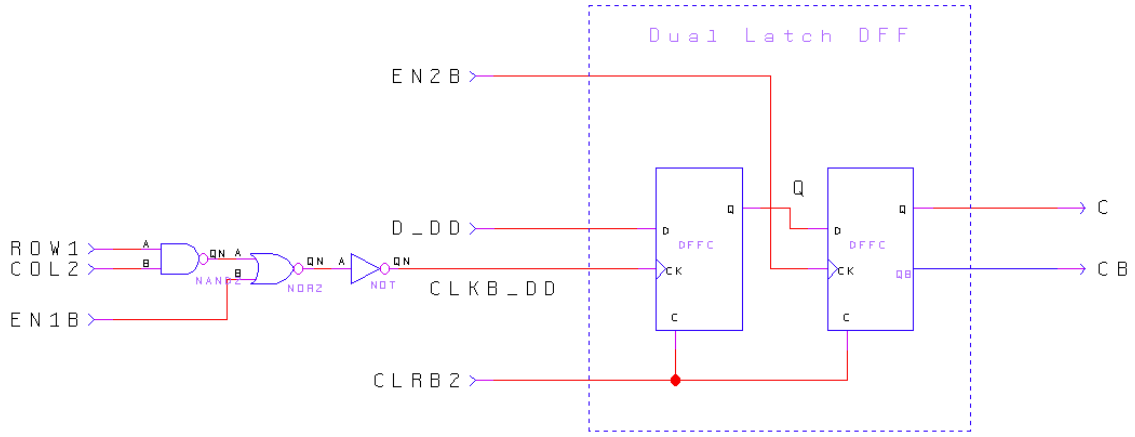


Figure 8. Schematic of the driver cell memory connected to the memory enable logic

Changing the Output Phase of the Electrode

The high voltage digital driver circuit is shown in Figure 9. The inputs are VIN, the 5V square wave reference signal, C and CB, which are taken from the output of the driver cell memory and control the phase of the output. The output of this circuit a square-wave with peak voltage determined by the VHH supply. The target peak output is a 100V. The reference signal VIN is a 5V square-wave that is sent to every driver cell as a reference for the output signal. Signals C and CB determine whether the output of the driver cell is in phase with VIN or 180 degrees out of phase with VIN. When C is low (and CB is high), HVIN is in phase with VIN and the output of the driver, HVOUT, is 180 degrees out-of-phase with VIN. When C is high (and CB is low), HVIN is 180 degrees out-of-phase with VIN and the output HVOUT is in-phase with VIN. In the digital driver circuit, the standard 5V CMOS logic input signal drives a high voltage NMOS with 5Megohm resistor load (or resistor load binary inverter) that creates a 100V peak-to-peak drain swing that drives the electrode.

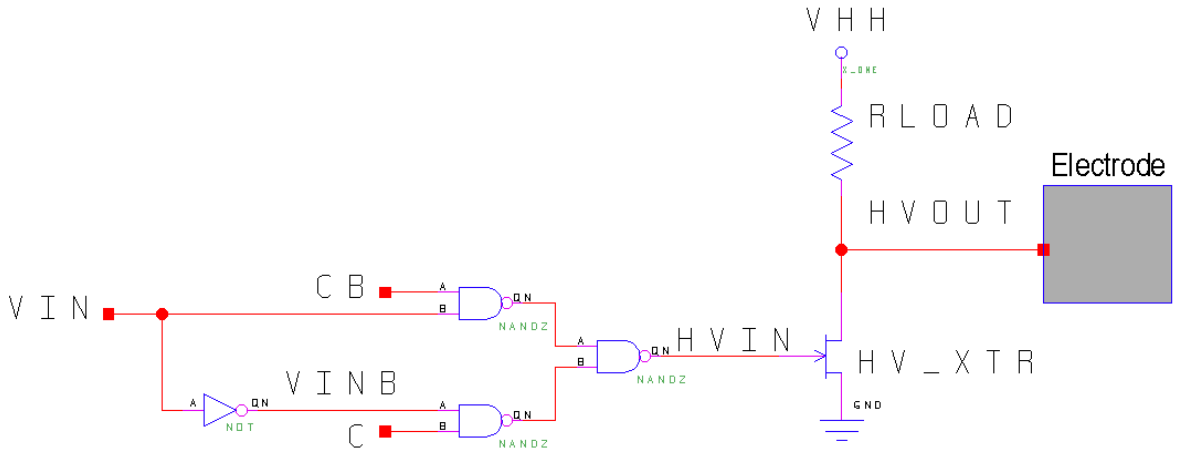
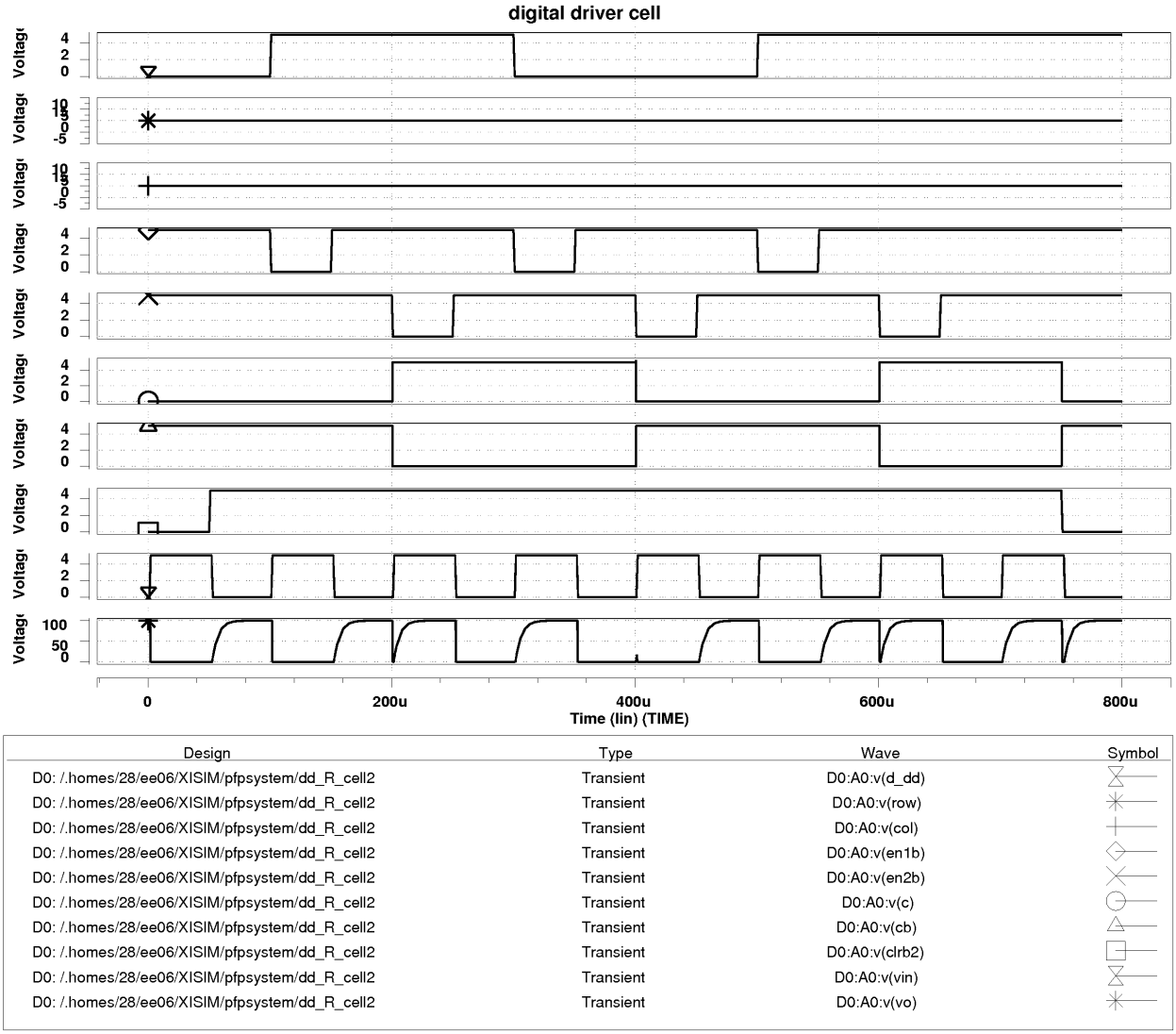


Figure 9. Schematic of high voltage digital electrode driver

A simulation of the driver cell changing phases is shown in Figure 10. With a logic high ROW and logic high COL signal, a logic high data D_DD is first latched into the driver cell memory when the EN1B signal is enabled at t=100us. Then, EN2B is enabled at t=200us and the output changes phases from out-of-phase with VIN to out-of-phase with VIN. At t=300us, EN1B goes low again and a logic low D_DD is latched into the driver cell. EN2B is enabled again at t=400us and the output changes back to out-of-phase with the input VIN. Following that, the output is again programmed to in-phase to illustrate the reset when CLRB2 is enabled at t=160us.



Design	Type	Wave	Symbol
D0: /.homes/28/ee06/XISIM/pfpsystem/dd_R_cell2	Transient	D0:A0:v(d_dd)	
D0: /.homes/28/ee06/XISIM/pfpsystem/dd_R_cell2	Transient	D0:A0:v(row)	
D0: /.homes/28/ee06/XISIM/pfpsystem/dd_R_cell2	Transient	D0:A0:v(col)	
D0: /.homes/28/ee06/XISIM/pfpsystem/dd_R_cell2	Transient	D0:A0:v(en1b)	
D0: /.homes/28/ee06/XISIM/pfpsystem/dd_R_cell2	Transient	D0:A0:v(en2b)	
D0: /.homes/28/ee06/XISIM/pfpsystem/dd_R_cell2	Transient	D0:A0:v(c)	
D0: /.homes/28/ee06/XISIM/pfpsystem/dd_R_cell2	Transient	D0:A0:v(cb)	
D0: /.homes/28/ee06/XISIM/pfpsystem/dd_R_cell2	Transient	D0:A0:v(clrb2)	
D0: /.homes/28/ee06/XISIM/pfpsystem/dd_R_cell2	Transient	D0:A0:v(vin)	
D0: /.homes/28/ee06/XISIM/pfpsystem/dd_R_cell2	Transient	D0:A0:v(vo)	

Figure 10. Timing diagram for the digital driver cell

Droplet Injection Control

The voltage of the injection reference electrode is determined by the REFINJ signal, which is driven by either its pogo pin or bonding pad. The voltage applied to REFINJ is whatever is needed to support droplet injection and is still under study.

To support injection, the column 31 electrodes need the additional functionality of a 0V state. To generate this additional 0V state, a high-voltage pull down transistor with its own memory is included in the functionality of column 31. This additional memory and high-voltage driver transistor are called column COLINJ. The drain of the additional pull-down high voltage transistor is connected to the output of the electrode driver as shown in Figure 11 and will force the electrode voltage to zero when activated. The high-voltage pull down transistor is controlled by its own data signal INJ. When a logic high INJ is latched into the COLINJ cell, the 0V electrode state will be initiated upon activation of the EN2B signal. When a logic low INJ is latched in the COLINJ memory, the electrode in column 31 will operate normally. The COLINJ memory is addressed whenever column 31 memory is addressed. Injection data INJ is an asynchronous signal brought in on its own pogo pin to all rows in COLINJ. The COLINJ memory is also reset by the CLRB2 signal. The INJ data will be stored in the memory of the COLINJ cell. To enable the memory of a particular COLINJ cell, the address of its corresponding COL31 cell is

loaded into the shift register and then passed through decoders to the array. When EN1B is clocked, the selected cell in COLINJ will store INJ into its own memory at the same time the corresponding COL31 cell will store D. Once programming of the third state COLINJ electronics is complete, EN2B will simultaneously update all signals in the array as well as the COLINJ memories. The INJOR signal at the output of the COLINJ memory will be logically OR'ed with the HVIN signals of column 31. The HVIN signal from schematic Figure 11 controls the gate of the high voltage NMOS in column 31. If INJ is asserted high, then INJ will control the addressed COL31 electrode and pull its voltage towards ground. Otherwise, the INJ is logic low (INJ = 0V). The INJ signal and COL31 pull down drivers add a third state to the COL31 cells and allow column 31 electrodes to either realize a zero volt output or operate normally with a 2-phase 100V peak-to-peak signal with the phase controlled by the standard data bit, D.

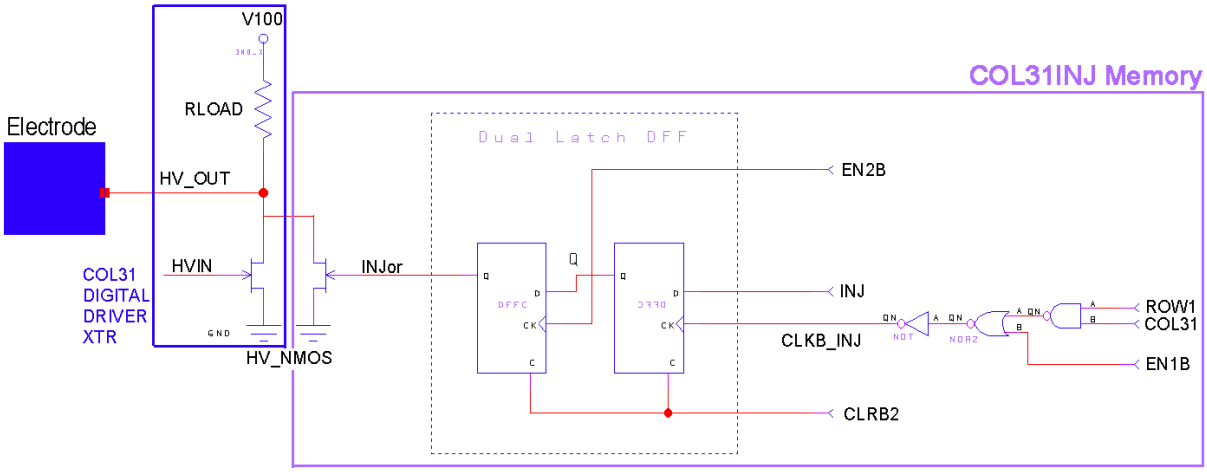
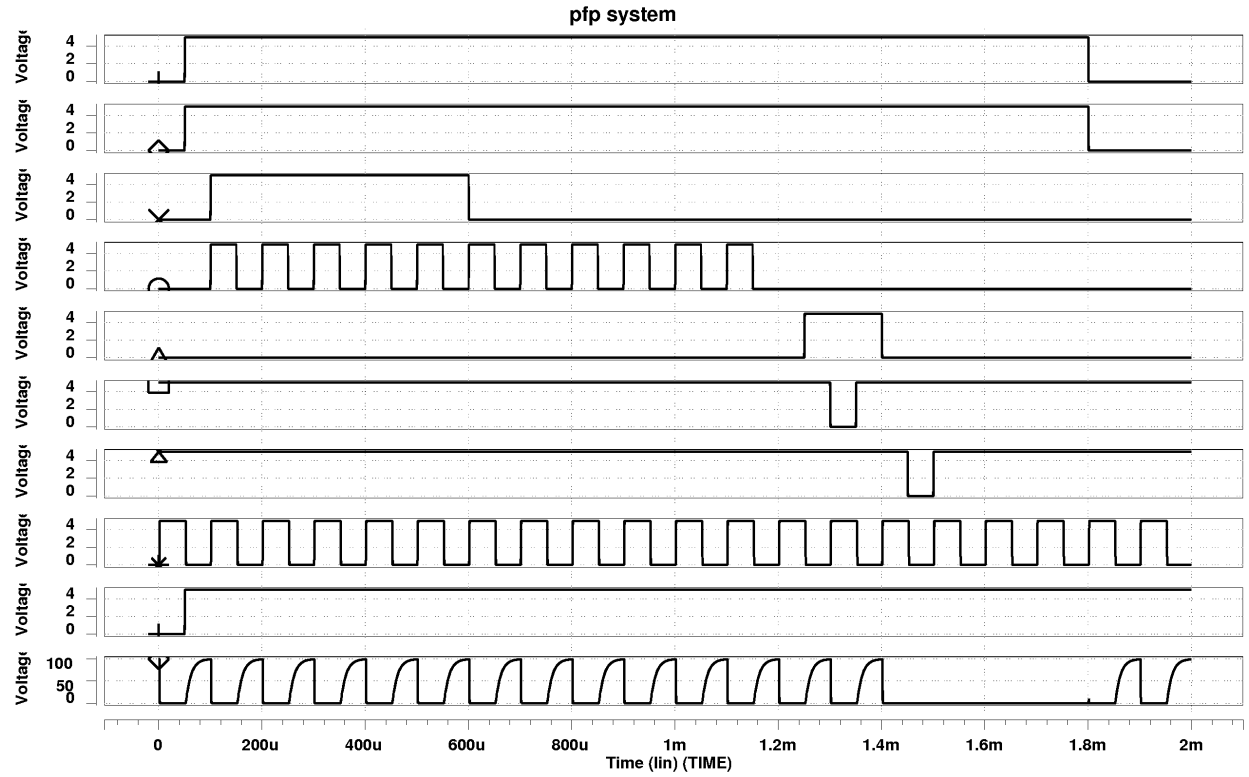


Figure 11. Schematic of the COLINJ cell connected to output of its corresponding COL31 electrode



Design	Type	Wave	Symbol
D0: /.homes/28/ee06/XISIM/pfpsystem/colinj_pfp1k	Transient	D0:A0:v(clrb1)	
D0: /.homes/28/ee06/XISIM/pfpsystem/colinj_pfp1k	Transient	D0:A0:v(clrb2)	
D0: /.homes/28/ee06/XISIM/pfpsystem/colinj_pfp1k	Transient	D0:A0:v(data_in)	
D0: /.homes/28/ee06/XISIM/pfpsystem/colinj_pfp1k	Transient	D0:A0:v(clk)	
D0: /.homes/28/ee06/XISIM/pfpsystem/colinj_pfp1k	Transient	D0:A0:v(load)	
D0: /.homes/28/ee06/XISIM/pfpsystem/colinj_pfp1k	Transient	D0:A0:v(en1b)	
D0: /.homes/28/ee06/XISIM/pfpsystem/colinj_pfp1k	Transient	D0:A0:v(en2b)	
D0: /.homes/28/ee06/XISIM/pfpsystem/colinj_pfp1k	Transient	D0:A0:v(vin)	
D0: /.homes/28/ee06/XISIM/pfpsystem/colinj_pfp1k	Transient	D0:A0:v(inj)	
D0: /.homes/28/ee06/XISIM/pfpsystem/colinj_pfp1k	Transient	D0:A0:v(vo_0x31)	

Figure 12. Timing diagram for the operation of the COLINJ injection circuitry creating a zero volt state

A programming cycle illustrating the operation of the COLINJ electronics is shown in Figure 12. The cell (0,31) is targeted for programming of the zero volt state and the address loaded into the shift register also enables the COLINJ cell corresponding to that location. INJ is logic high when EN1B is latched which causes the COLINJ cell to store a logic high memory. Once EN2B is enabled at t=1.45ms, instead of the output remaining a square wave, it is driven down towards ground by the COLINJ pull down high voltage NMOS. At t=1.8ms, the reset signal is activated and the output of phase square wave is restored.

Discussion of Issues Involving Power

In this section, the power dissipated by the PFP1K system is estimated and discussed. The simulations and estimation were performed on the PFP1K chip, but should be very similar to the PFP5 chip since the differences between the PFP1K and PFP5 chips are minor. These differences are described in following section entitled “Changes made to PFP1K to get PFP5”.

Estimation of power requirements is complicated because of the way the chip is to be operated. First, during a reset phase all the chip memory has to be reset. The low-voltage, 5-volt input signal Vin that drives the 1024 high-voltage electrode drivers circuits will probably be running continuously. Under

these conditions, all the data stored in the array will be logical ZERO and all the electrodes will be driven by the same phase of the bi-phase 100-volt electrode excitation. Thus, the current demand on the 100-volt power supply will be greatest when all high-voltage electrode signals are in-phase just after memory reset. After the memory is reset, the pixel array data may be stored. Each pixel's data must be loaded individually. To set all 1024 pixels to new data values, 1024 communications frames must be written. When the operator is ready for the stored pixel data to be transferred to the electrode drivers so that the new data appears on the electrodes, all electrodes are switched simultaneously. This transfers data from one pixel latch to another latch within the pixel and causes the phase of the high-voltage electrode voltage waveform to change if the data changed state. We envision the next step to be the loading of more pixel data to establish a new pattern in the pixel array. Thus, the reset operation is undertaken at start up and only occassionally as needed. The primary mode of operation is the transfer of pixel data with the communications SR and impressing the array data pattern on the high-voltage electrodes. This is repeated as often as needed to move the droplets as required. Thus, power required at reset and power required during the 2 parts of the primary operation mode should be estimated.

Since the high-voltage circuitry is the least complicated, we can start with it. The maximum current each of the 1024 high-voltage signal generation circuits uses is set by the 5MΩ resistor tied to the 100volt supply -- about 20μA. This current times 1024 pixels is a peak current of 20.48mA. This is a peak power for the 100volt supply of 2.048W. The bi-phase high-voltage waveforms are to be square waves with 180degree phase shift. If all pixels have the same phase, then over the period of the signal, the average power will be half the peak power. If N of the signals are switched to the other phase, the average power over a period will remain half the peak power. Thus, the average power required from the 100volt supply is expected to be just over 1W.

Estimating the power required during memory reset is more complicated. HSPICE simulation of the entire circuit indicated that the peak (worst-case) current needed from the 5-volt supply to be approximately 1.26A. This is a large current that would exist for a short time that is due to simultaneous reset of all the memory in the circuit. This can be reduced slightly by resetting the array memory (2048 latches + 64 injector latches) and the SR memory (22 latches) at different times. Thus, the peak estimated power from the 5-volt supply would be approximately 6.3W for a short time. If the time required is 1μs, the peak energy required would be approximately 6.3μJ. All the 5-volt logic circuitry and memory are standard CMOS logic and thus require nominally no power when they are idle (not switching).

The primary mode of operation will be the indefinate repetition of 1) the reception of data in the communications SR and placing that data in the specified pixel location and 2) driving the high-voltage electrodes with the new signals. Step 1 of this mode could be of variable duration depending upon how many pixels are to be updated between operations of step 2. We can break the power estimation into examining the communication frame power at a clock rate, the load and write data into a pixel, and the changing of the high-voltage signals.

The communications shift register clock will be run at a constant clock rate during any frame. The communications SR clock is stopped between frames. Each communications transaction or frame is 11 bits. After the 11 bits have been loaded into the communications SR, a "LOAD" signal places the 11 SR signals into the decoders and buffers that drive the array. After the data has had time to settle in the array, a memory control signal latches that new pixel data into the target pixel. When this is complete, the communications transaction is complete and new data can be loaded into the communications SR. Thus, to receive data for one pixel, we have to receive one data frame of 11-bits in the communications SR and load that data into the pixel location specified by the address. We can estimate peak power and average power during a frame. A frame has 2 phases: 1) during the operation of the communications SR (during which time the decoders, buffers, and array are static), and 2) during the load and write pixel operation (during which time the SR is static).

Power Simulations

The power dissipation of the 5V supply and the 100V supply used to operate PFP1K were simulated with HSPICE. The current demand of these two supplies were simulated separately.

5V Power Supply Simulation

Approximating the power consumption over an entire operational cycle

Measurement of the power dissipation in the PFP1K chip could easily be done by simulating an entire operating cycle. An entire operating cycle consists of loading new data into all 1024 of the array cells, and updating the electrode outputs. However, due to limitations set by computer system operation policy, we cannot simulate 1024 sequences nor can we simulate the entire array. Instead, we perform the memory loading and updating of a single cell, break that simulation into multiple stages that we can then repeat and project the power required for an entire cycle. Figure 13a and 13b show a schematic of the PFP1K system and how the power measurements are made in parts with respect to time. The first average power measurement taken is when the shift register is loaded with the addresses and data bit. This measured average power is called SR and is shown in Figure 13a. The next measurement is taken from the time the LOAD signal is set high to when the EN1B signal latches the data in the memory of the target cell. This measurement is called PM for Pixel Memory and can be traced from Figure 13a to Figure 13b. Finally, the high voltage transistor driver logic is updated, simulating a simultaneous update of all driver circuits. The power measured from this stage is called EAU for Electrode Array Update and is shown in Figure 13b. The high voltage transistors' gate terminals are grounded during the 5V power consumption measurements to set the 100V power supply power to zero.

We now extrapolate the power consumption of an entire 1024 cell operating cycle with the data calculated from the single cell simulation that is organized as illustated in Figure 14. To calculate average power, we calculate the total energy used in a time interval of interest and divide by the time interval of interest. In an entire operating cycle, the communication shift register is loaded and the data is sent to a pixel memory for each of the 1024 cells. Therefore, this data loading process is performed 1024 times. Once the new data has been loaded into the cells, the array update is performed. The average power data that we calculated during the simulation, SR, PM and EAU can be mapped across an entire 1024 cell operating cycle. Since we know that SR (taken over a time t_SR = 1.15ms) and PM (taken over a time t_PM=0.2ms) repeat 1024 times, the energy is calculated with 1024 x (t_SR + t_PM). We then add EAU (taken over a time t_EAU=0.1ms) to find the total energy. The average power of the 5V power supply can be calculated by as the total energy divided by the total time:

$$P_{avg\_5V} = \frac{N \times (SR \times t\_SR + PM \times t\_PM) + (EAU \times t\_EAU)}{N \times (t\_SR + t\_PM) + t\_EAU}$$

Predicting the effect of loading on the power sources from the 32x32 array

The above procedure is used to approximate the power consumption over a time larger than what was simulated. However, due to computer system administration policy, our computers cannot simulate the entire array of driver cells either. The size of the array and the number of untargeted cells in the array affect the power consumption of the circuit even though only one cell is being loaded with new data and only its electrode is being updated. This is because gates in the digital drivers of those untargeted cells are still being switched on and off by Vin. The signal Vin is passed into two gates of each driver: a 2-input NAND gate and an inverter followed by another 2-input NAND gate as shown in Figure 13b. The signal Vin will continuously switch two gates throughout all stages of operation regardless of the logic state and thus consume power throughout the circuit operation. Some of the additional power can also be attributed to the capacitances of the untargeted circuits that load the lines driving the array. As a

result, gates take longer to switch and more current is required. Parasitic currents also modeled in simulation will affect current drawn from the internal signals as well as the external signal sources.

Since we cannot simulate the circuit with an entire array of 1024 cells, we simulate the circuit multiple times with a smaller array and increase the size of it at each subsequent simulation. By doing this, we can establish the relationship between the power consumption at the three stages with the size of the array. It is possible then to predict the average power variables SR, PM and EAU for an entire array and time extend them to solve for the total average power. First, the simulation is executed with an array composed of only a single row of cells containing the target cell. That simulation gives the three power averages SR_1, PM_1 and EAU_1. The simulation is then repeated for an array of two rows from which we obtain SR_2, PM_2, EAU_2. The process can be repeated as many times as allowed. We simulated PFP1K with array sizes of 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 and 16 rows at a CLK and VIN frequency of 10kHz. The data from each stage were plotted and linearly interpolated and extrapolated as shown in Figure 15. From the plots, we predicted SR, PM and EAU for an entire array of 32 rows and used those values in the power computation. The interpolated data is plotted with the simulation data to show the consistency of the extrapolation.

From the extrapolation, we obtain SR = 3.4mW, PM = 3.6mW and EAU = 3.4mW. Solving for the total average power, the average power is P_{avg_5V} = 3.5mW. A summary of the variables used to calculate P_{avg_5V} is shown in Table 1. The interpolation and extrapolation were performed on the peak power that occurs during the circuit operation (not the CLRB1/CLRB2 case) and is estimated at P_{peak_5V} = 1.9878W. The peak power is consumed when the LOAD signal is triggered from low to high and data is passed from the shift register to the decoders. The plot for that data is also shown in Figure 15.

100V Power Supply Simulation

In our 5V power simulations, we grounded the gates of the HV transistors to set the 100V supply current to zero. Since only the high-voltage transistors operate on 100 volt supply, it is possible to estimate power by simulating 1024 high voltage transistors loaded with 5Megaohm resistors and 1pF capacitors each, excluding any 5V logic circuits. One simulation is sufficient.

The 100V power supply simulation consists of two major stages and the organization is shown in Figure 14. The first stage is the time before the HV transistor data is updated. During this time, the high voltage transistor is being switched on and off by a periodic square wave. In the second stage, the HV transistors change phase. To find the maximum average power, the signals CLK and Vin are set to 10kHz, all high-voltage outputs are initially in the same phase before the array update, and all electrodes change to the opposite phase after the array update. We simulated 1024 high-voltage transistors and loads with a phase '0' square-wave input for the duration t_BAU (= 1.35ms) during which time the 5V circuits are communicating data. At the time the array data is updated in the 5V simulation, we simultaneously change the phase of the 1024 high-voltage transistors inputs and measure the average power for the duration t_AAU (= 0.1ms). From the simulation we obtain the powers BAU (Before Array Update) and AAU (After Array Update). The simulation is extended in time using the same method shown in Figure 14. BAU is repeated for 1024 durations before AAU is averaged in. The average power consumption of the 100V supply can be solved:

$$P_{avg\_100V} = \frac{N \times (BAU \times t\_BAU) + (AAU \times t\_AAU)}{(N \times t\_BAU) + t\_AAU}$$

From the simulation, BAU = 1.1570W, AAU = 1.0904W and P_{avg_100V} = 1.1570W. The peak power from the 100V supply during normal operation is P_{peak_100V} = 2.0488W. The values used to compute the average power from the 100V supply is given in Table 2.

Table 3 below summarizes the power estimates performed.

Wiring the power lines on PFP1K

The pogo pins are rated at 3A continuous current and can handle the expected current. To ensure that current is supplied to different parts of the PFP1K chip without overloading the metal layers, a power grid was designed around the array to evenly distribute the current. Each column of the array has its own VDD and VSS line routed to the respective pogo pins through power and ground buses. The VDD bus is routed through the top of the array and to pogo pad 1 and the VSS bus is routed out through the bottom to pogo pad 9. VDD and VSS form their own grids within the array cell structures and have 37 wires at the connection to the pogo pad (33 for the array and 4 for the SR, decoders, and buffers). The power lines are also routed through bonding pads at the top and bottom of the chip. Twenty bonding pads at the top and bottom of the chip are dedicated to wiring VDD and VSS lines. The VDD power lines are connected together at the top of the array and the VSS power lines are connected together at the bottom of the array.

Table 1. Values used in 5V average power consumption calculation

Variable	Value	Description
N	1024	Number of cells
SR	3.4mW	Average power consumed during shift register loading stage
t_SR	1.15ms	Time duration of shift register loading stage
PM	3.6mW	Average power consumed during the pixel memory load stage
t_PM	0.2ms	Time duration of pixel memory load stage
EAU	3.4mW	Average power consumed during the electrode array update stage
t_EAU	0.1ms	Time duration of electrode array update stage
P_{avg_5V}	3.5mW	Total average power consumed from the 5V power supply

NOTE: SR and PM could have been combined, but we separate them for clarity

Table 2. Values used in 100V average power consumption calculation

Variable	Value	Description
N	1024	Number of cells
BAU	1.1570W	Average power consumed before electrode array update
t_BAU	1.35ms	Time duration before electrode array update
AAU	1.0904W	Average power consumed after electrode array update
t_AAU	0.1ms	Time duration after electrode array update
P_{avg_100V}	1.1570W	Total average power consumed from the 100V power supply

Table 3. Summary of Power Analysis

	5V Power Supply	100V Power Supply
Average Power	3.5mW	1.1570W
Peak Power during operation	1.9878W^{o}	2.0488W
Maximum Peak Power	6.3W^{+}	2.048W*

^{o}Occurs when LOAD signal is activated

$^{+}$Occurs during CLRB1/CLRB2 reset

*Hand estimated and occurs during operation. Simulated Peak Power during operation is slightly greater due to current spikes.

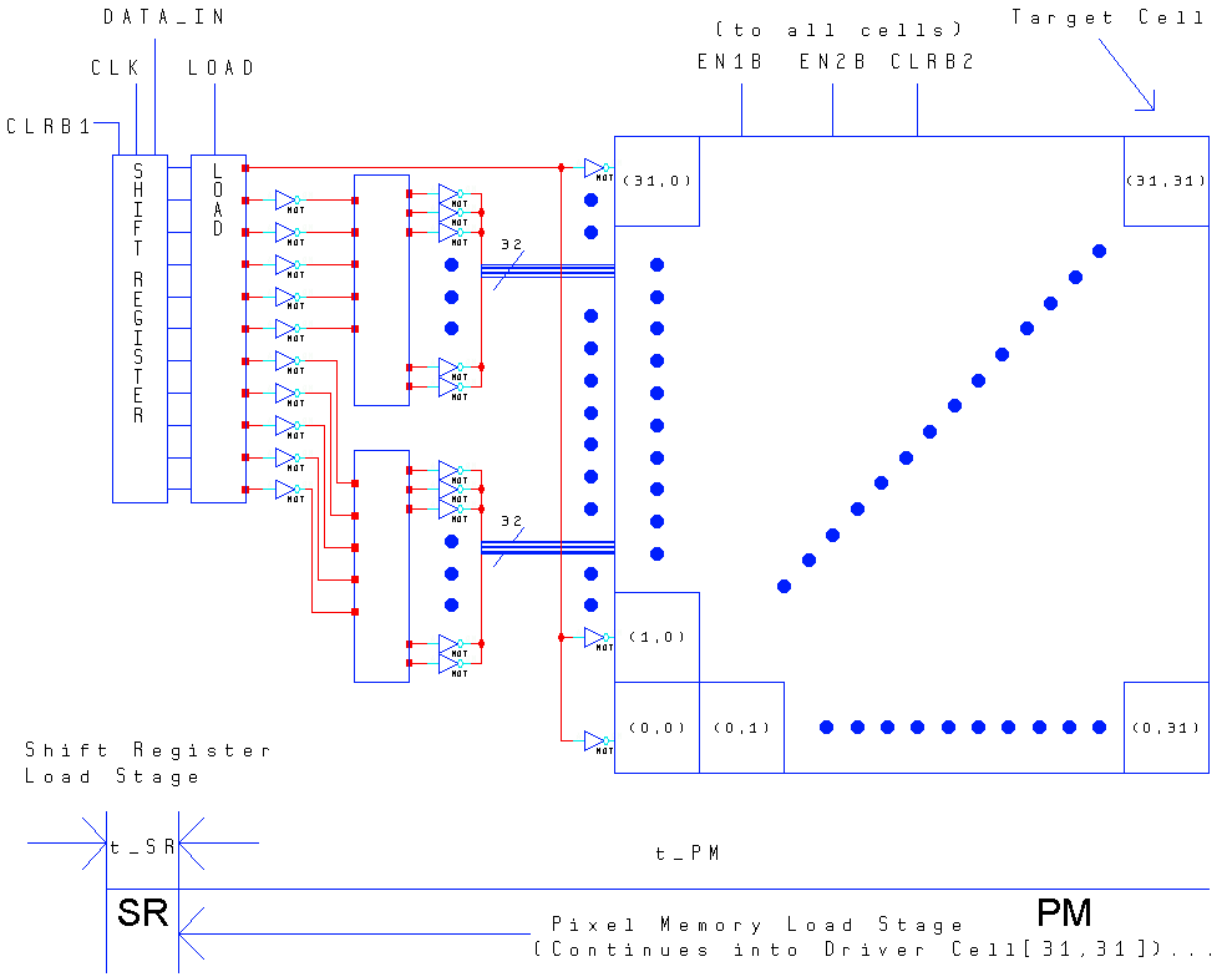


Figure 13a. Average Power Measurement Stages Shown Over the Circuit

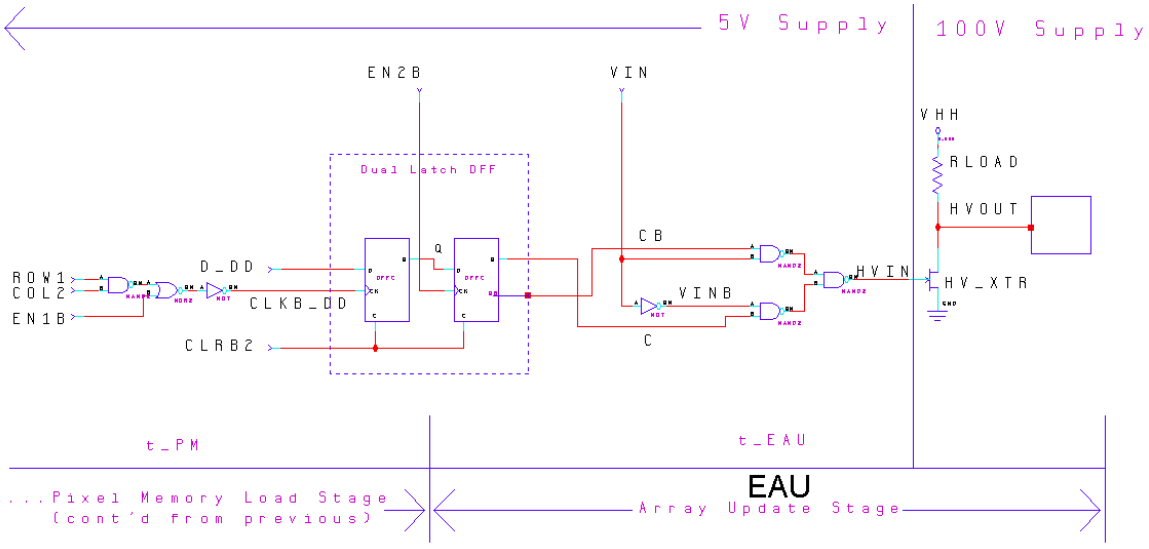


Figure 13b. Average Power Measurement Stages Shown Over the Digital Driver Cell.

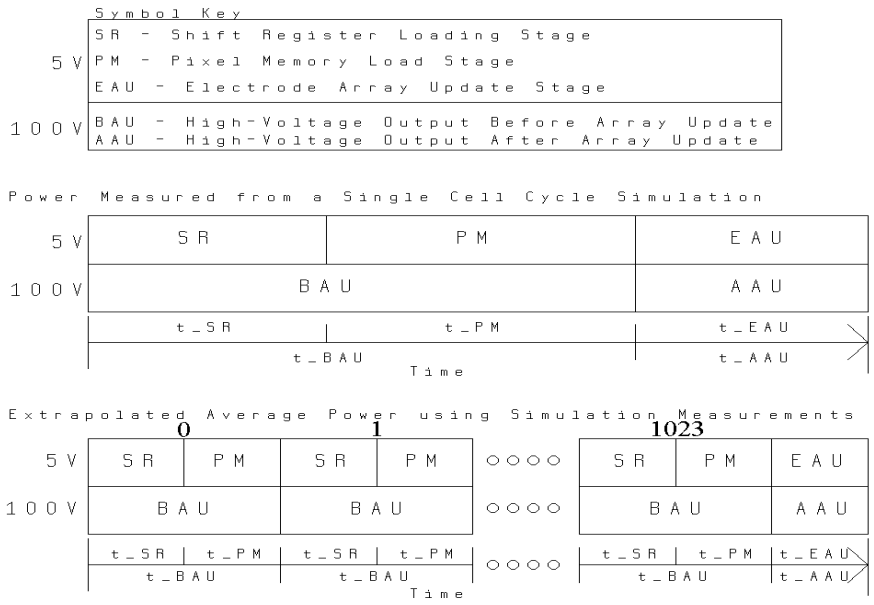


Figure 14. Mapping of the Power Simulation Measurements Over a Full Operating Cycle

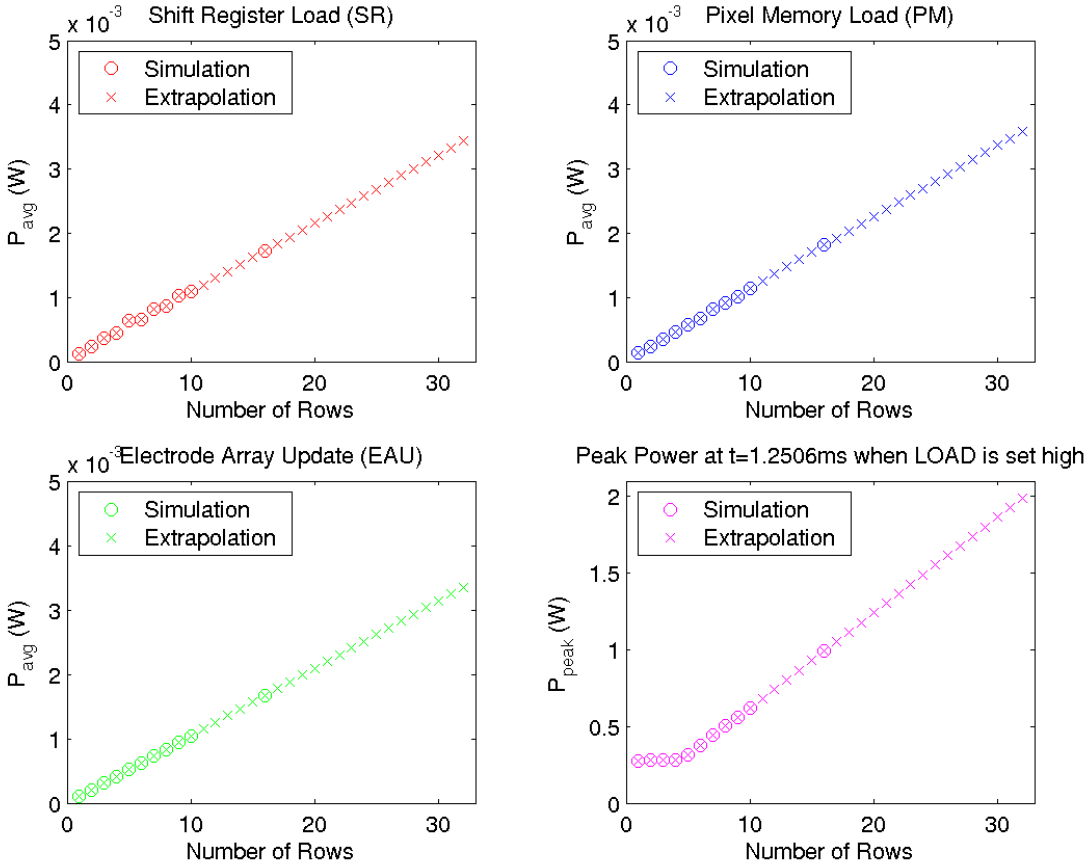


Figure 15. Data, interpolated and extrapolated plots used to predict: power averages of a 32-row driver array, and the peak power consumed during the operating cycle.

Results from testing

During testing of PFP1K, the large power numbers were not observed by either UC Davis (UCD) or Jon Schwartz at the University of Texas MD Andersen Cancer Center (UTMDACC) possibly due to the short duration of the signals switching or that the frequencies used for testing were much less than the desired 10kHz operating frequency. At UCD, a frequency of 100Hz was used while at UTMDACC, a frequency of 19Hz was used. The lower frequency results in less switching per second and therefore less average power dissipation.

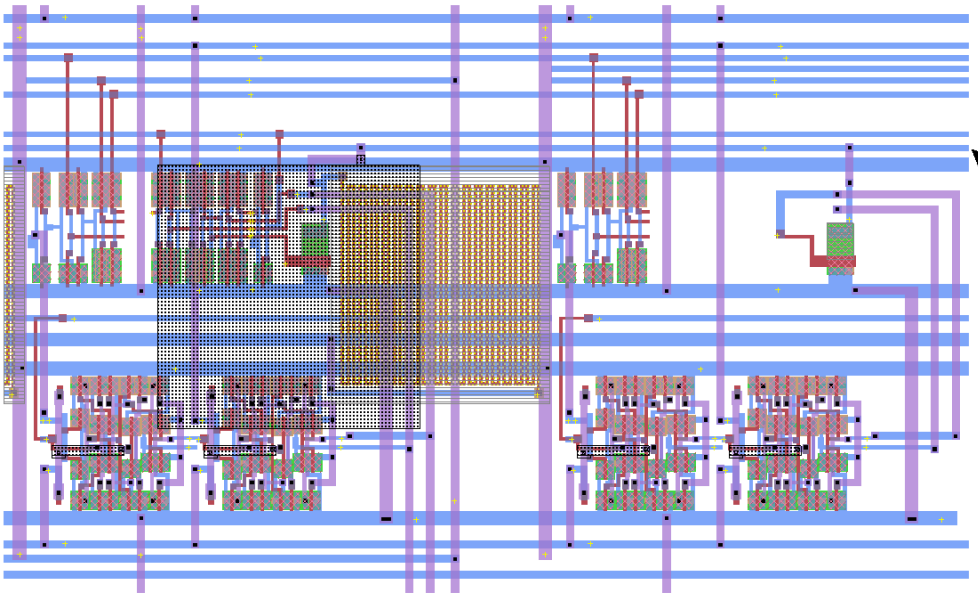


Figure 16. COL31 and COLINJ section of PFP1KV11 with the COL31 output error

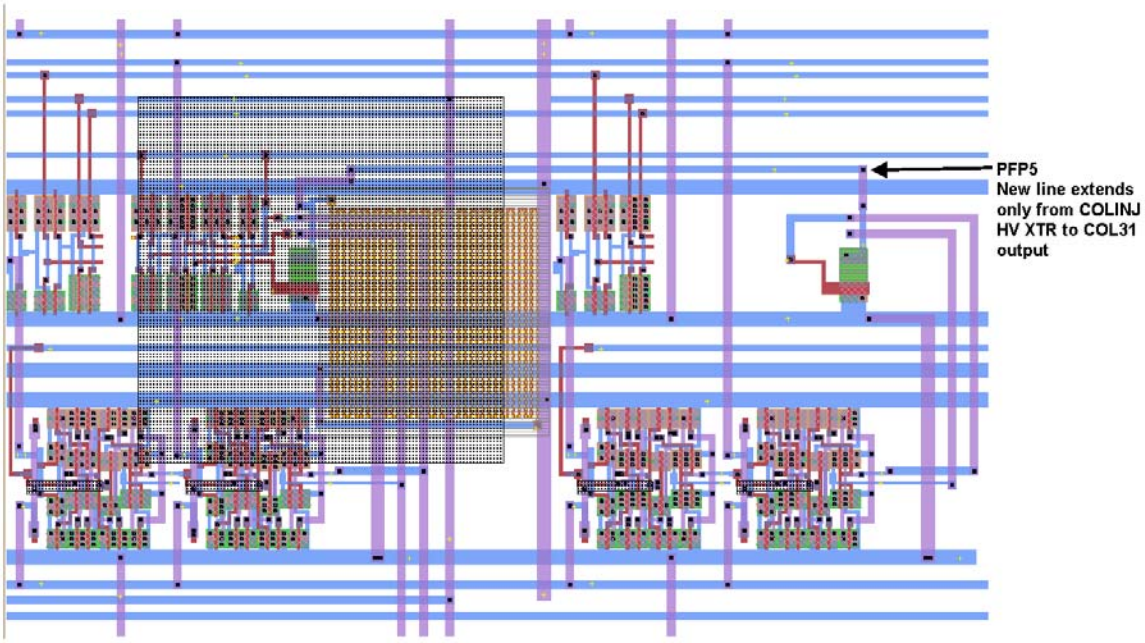


Figure 17. COL31 and COLINJ section of PFP5 with correction of the COLINJ error by a reduction of length of the M1 line connecting the COLINJ pull-down NMOS to the COL31 electrode output.

Enlargement of the high voltage electrode

The high voltage electrode for all cells has been enlarged from 100um square to 133um square. The lower left coordinates of the electrode have not been changed. The electrode are no longer centered within the cell but retain equal spacing between adjacent electrodes.. An example of the size of the enlarged electrode is shown in the digital driver test cell layout in Figure 18.

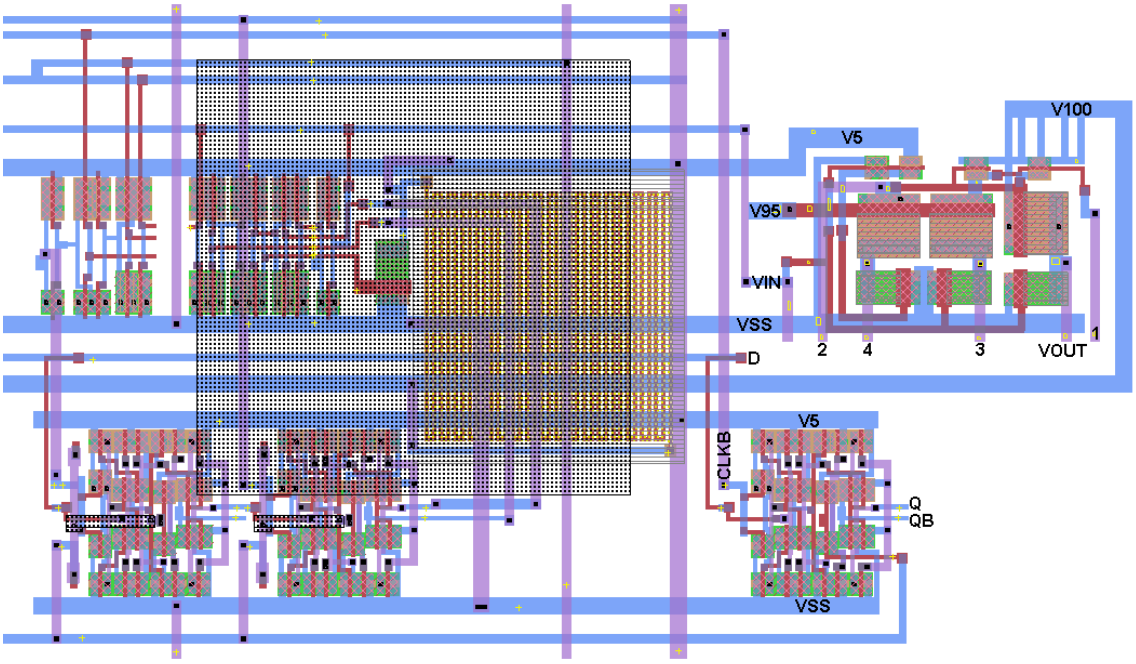


Figure 18. Test cell area of PFP chip showing the DD test cell, HVLS and D latch w/o M3

Addition of the DL without M3 test cell

The D latch w/o M3 jumper is connected at the right of the digital driver test cell in the layout and shares the signals VSS, V5, D CLKB and CLRB with the digital driver test cell's signals as shown in Figure 18. The output signals of the latch, Q and QB, are wired out to bond pads.

Addition of the high voltage level shifter (HVLS) test cell

The HVLS is placed on the right side of the digital driver test cell on the PFP5 chip as shown in Figure 18. The signals VSS, V5, V100 and VIN are shared with the digital driver test cell's signals. The signals V95 and VOUTLS cannot be shared and require two bond pads. The four intermediate nodes are not wired out on PFP5 because of the excessive loading that would result at those nodes.

Addition of fiducial marks

A fiducial mark has been added to the left of the array. The fiducial mark is composed of M3 and consists of a cross hair-like structure whose center sits vertically between the electrodes of rows 15 and 16 and horizontally 1109.5u to the left of the first column of electrodes, between the array and the pogo pads. Passivation holes have been placed above the fiducial marks above the larger four sections of the cross-hair and on the long M3 north and south of the cross hair. The fiducial mark can be seen in layout in Figure 1.

Chip Pad Numbering and Description

Overall description of PFP5 bond pad signals

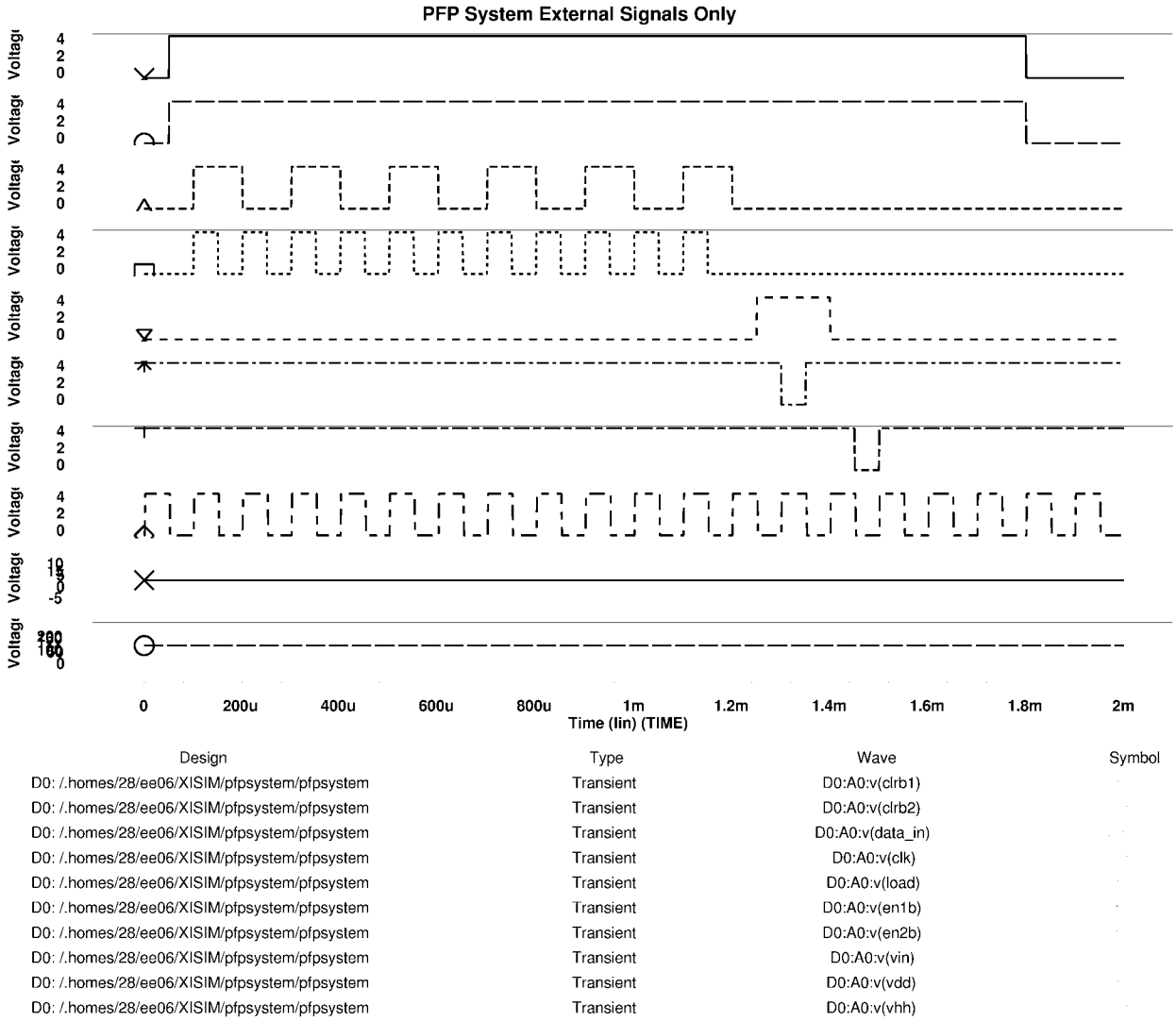


Figure 19. Timing diagram for the PFP system control signals.

The signals used for the control and monitoring of the PFP5 system are described here. A normal programming cycle employing the necessary control signals are shown in Figure 19. The description of the pogo pads and signals are given in Table 4. The bond pad signals are given in Table 5 and labeled on the PFP5 layout shown in Figure 1. The PFP5 system's signals grouped by input/supply are given in Table 6 while the monitor/overrides and outputs are given in Table 7.

Table 4: PFP5 Pogo Pin Pad Description

Pogo Pin Pad Number	Signal	Description
1	V5	5V power supply. Connected to BOND PADs 76-95
2	CLK	Clock signal governing the operation of the Communications Shift Register. When CLK is high, the first latch of each dual latch element

		stores the received data. When CLK is low, the second latch stores the data from the first latch and outputs it to the LOAD array. Connected to BOND PAD 45
3	DATA_IN	Data input to Communication Shift Register. The register has 11-bits. The data in the register are arranged $DR_4R_3R_2R_1R_0C_4C_3C_2C_1C_0$ where the first data bit shifted in time is C0 and the last data bit shifted in is D. Connected to BOND PAD 46
4	CLRB1	"0" = asynchronously resets all latches in Communication Shift Register. Connected to BOND PAD 47
5	LOAD	"1" = gates the data and target address from the output of the shift register into the decoders Connected to BOND PAD 48
6	EN2B	"0" = updates the electrode array memory by loading data from the first latch in every cell into the second latch. Connected to BOND PAD 49
7	EN1B	"0" = loads data into the first latch of the target cell of the array. The target cell is determined by the row and column addresses that activate the corresponding ROW and COL signals. Connected to BOND PAD 51
8	VIN	Input signal to all digital drivers. Generally a square-wave function from 0V to 5V and frequency up to 10kHz. Connected to BOND PAD 53
9	VSS	Ground. Connected to BOND PAD 56-75
10	REFINJ	Injection Reference electrode voltage for the injectors. Connected to BOND PAD 55
11	INJ	Data into the dual latches of COL31INJ cells that control injection. "0" will turn off HV xtr at COL31INJ and allow COL31 to output the normal 2-phase 100V square wave. "1" will turn on HV xtr at COL31INJ and pull the voltage at the electrode of COL31 to GND. Connected to BOND PAD 54
12	CLRB2	"0" = asynchronously resets the memory of all the array cells Connected to BOND PAD 52
13	V100	100 Volt power supply Connected to BOND PAD 50
14	C0_LOAD_PB	Valid post-buffered C0 address bit monitor and/or override. Valid C0 after LOAD = "1." Connected to BOND PAD 5 Corresponds to signal 'C0' in Figure 4.
15	C1_LOAD_PB	Valid post-buffered C1 address bit monitor and/or override. Valid C1 after LOAD = "1." Connected to BOND PAD 4 Corresponds to signal 'C1' in Figure 4.
16	C2_LOAD_PB	Valid post-buffered C2 address bit monitor and/or override. Valid C2 after LOAD = "1." Connected to BOND PAD 3 Corresponds to signal 'C2' in Figure 4.
17	C3_LOAD_PB	Valid post-buffered C3 address bit monitor and/or override. Valid C3 after LOAD = "1." Connected to BOND PAD 2 Corresponds to signal 'C3' in Figure 4.
18	C4_LOAD_PB	Valid post-buffered C4 address bit monitor and/or override. Valid C4 after LOAD = "1." Connected to BOND PAD 1 Corresponds to signal 'C4' in Figure 4.
19	D_LOAD_PB	Valid post buffered D data monitor and/or override. Valid D after LOAD = "1." Connected to BOND PAD 35 Corresponds to signal 'D' in Figure 4.

Table 5: Bonding Pad Description

Color	Signal Type
	Monitor/Override signal
	Not wired to pad
	Test cell input and control
	PFP System input and control
	Ground
	5V Supply

Bonding Pad Number	Signal	Description
1	C4_LOAD_PB	Valid post-buffered C4 address bit monitor and/or override. Valid C4 after LOAD = "1." Connected to POGO PAD 18. Corresponds to signal 'C4' in Figure 4.
2	C3_LOAD_PB	Valid post-buffered C3 address bit monitor and/or override. Valid C3 after LOAD = "1." Connected to POGO PAD 17. Corresponds to signal 'C3' in Figure 4.
3	C2_LOAD_PB	Valid post-buffered C2 address bit monitor and/or override. Valid C2 after LOAD = "1." Connected to POGO PAD 16. Corresponds to signal 'C2' in Figure 4.
4	C1_LOAD_PB	Valid post-buffered C1 address bit monitor and/or override. Valid C1 after LOAD = "1." Connected to POGO PAD 15. Corresponds to signal 'C1' in Figure 4.
5	C0_LOAD_PB	Valid post-buffered C0 address bit monitor and/or override. Valid C0 after LOAD = "1." Connected to POGO PAD 14. Corresponds to signal 'C0' in Figure 4.
6	R4_LOAD_PB	Valid post-buffered R4 address bit monitor and/or override. Valid R4 after LOAD = "1." Corresponds to signal 'R4' in Figure 4.
7	R3_LOAD_PB	Valid post-buffered R3 address bit monitor and/or override. Valid R3 after LOAD = "1." Corresponds to signal 'R3' in Figure 4.
8	R2_LOAD_PB	Valid post-buffered R2 address bit monitor and/or override. Valid R2 after LOAD = "1." Corresponds to signal 'R2' in Figure 4.
9	R1_LOAD_PB	Valid post-buffered R1 address bit monitor and/or override. Valid R1 after LOAD = "1." Corresponds to signal 'R1' in Figure 4.
10	R0_LOAD_PB	Valid post-buffered R0 address bit monitor and/or override. Valid R0 after LOAD = "1." Corresponds to signal 'R0' in figure 4.
11	ROW11_PB	Post-buffered ROW11 monitor and/or override.
12	ROW12_PB	Post-buffered ROW12 monitor and/or override.
13	ROW13_PB	Post-buffered ROW13 monitor and/or override.
14	ROW14_PB	Post-buffered ROW14 monitor and/or override.
15	ROW15_PB	Post-buffered ROW15 monitor and/or override.
16	ROW16_PB	Post-buffered ROW16 monitor and/or override.
17	ROW17_PB	Post-buffered ROW17 monitor and/or override.
18	ROW18_PB	Post-buffered ROW18 monitor and/or override.
19	ROW19_PB	Post-buffered ROW19 monitor and/or override.
20	ROW20_PB	Post-buffered ROW20 monitor and/or override.

21	COL20_PB	Post-buffered COL20 monitor and/or override.
22	COL19_PB	Post-buffered COL19 monitor and/or override.
23	COL18_PB	Post-buffered COL18 monitor and/or override.
24	COL17_PB	Post-buffered COL17 monitor and/or override.
25	COL16_PB	Post-buffered COL16 monitor and/or override.
26	COL15_PB	Post-buffered COL15 monitor and/or override.
27	COL14_PB	Post-buffered COL14 monitor and/or override.
28	COL13_PB	Post-buffered COL13 monitor and/or override.
29	COL12_PB	Post-buffered COL12 monitor and/or override.
30	COL11_PB	Post-buffered COL11 monitor and/or override.
31	QB_DLTEST	QB output of modified DL w/o M3 test cell.
32	COL31_PB	Post-buffered COL31 monitor and/or override.
33	COL31C	C monitor and/or override of cell (0,31)
34	Q_DLTEST	Q output of modified DL w/o M3 test cell.
35	VOUTLS	Output of HVLS test cell
36	V95LS	V95 supply of HVLS test cell
37	EN2B	"0" = updates the digital driver test cell (DD) electrode by loading data from the first latch into the second latch.
38	EN1B	"0" = loads data into the first latch of the test cell. ROW and COL must = "1" to activate the first latch of the DD test cell.
39	VIN	Input signal into the test cell's digital driver Generally a square-wave function from 0V to 5V and frequency up to 10kHz.
40	V5	5 Volt power supply of DD test cell. ROW & COL tied HIGH here
41	VSS	Ground of the DD test cell
42	D	Data into first latch of the DD test cell's logic
43	V100	100V supply of the DD test cell
44	CLRB2	"0" = asynchronously resets the memory of the DD test cell
45	CLK	Clock signal governing the operation of the Communication Shift Register. When CLK is high, the first latch of each dual latch element stores the received data. When CLK is low, the second latch stores the data from the first latch and outputs it to the LOAD array. (Corresponds to POGO PAD 2)
46	DATA_IN	Data input to Communications Shift Register. The register has 11-bits. The data in the register are arranged $DR_4R_3R_2R_1R_0C_4C_3C_2C_1C_0$ where the first data bit shifted in time is C0 and the last data bit shifted in is D. (Corresponds to POGO PAD 3)
47	CLRB1	"0" = asynchronously resets all latches in Shift Register (Corresponds to POGO PAD 4)
48	LOAD	"1" = gates the data and target address from the output of the shift register into the decoders (Corresponds to POGO PAD 5)
49	EN2B	"0" = updates the electrode array by loading data from the first latch in every cell into the second latch. (Corresponds to POGO PAD 15
50	V100	100 Volt power supply (Corresponds to POGO PAD 13)
51	EN1B	"0" = loads data into the first latch of the target cell in the array. The target cell is determined by the R and C addresses that activate the

		corresponding ROW and COL signals. (Corresponds to POGO PAD 7)
52	CLRB2	"0" = asynchronously resets the memory of all the array cells (Corresponds to POGO PAD 12)
53	VIN	Input signal to all digital drivers. Generally a square-wave function from 0V to 5V and frequency up to 10kHz. (Corresponds to POGO PAD 8)
54	INJ	Injection control Data into the dual latch of COL31INJ. "0" will turn off HV xtr at COL31INJ and allow COL31 to output the normal 2-phase 100V square wave. "1" will turn on HV xtr at COL31INJ and pull the voltage at the electrode of COL31 to GND. (Corresponds to POGO PAD 11)
55	REFINJ	Injector Reference electrode voltage (Corresponds to POGO PAD 10)
56-75	VSS	Ground (20 pads) (Corresponds to POGO PAD 9)
76-95	V5	5V power supply (20 pads) (Corresponds to POGO PAD 1)

Input/output signals arranged according to test circuits

PFP System

The signals for the PFP5 system are described here based on input or output. The inputs/supply lines are described in Table 6. The outputs/monitor lines are described in Table 7.

Table 6. PFP5 control and supply lines

45	CLK	Clock signal governing the operation of the Communication Shift Register. When CLK is high, the first latch of each dual latch element stores the received data. When CLK is low, the second latch stores the data from the first latch and outputs it to the LOAD array. (Corresponds to POGO PAD 2)
46	DATA_IN	Data input to Communications Shift Register. The register has 11-bits. The data in the register are arranged $DR_4R_3R_2R_1R_0C_4C_3C_2C_1C_0$ where the first data bit shifted in time is C0 and the last data bit shifted in is D. (Corresponds to POGO PAD 3)
47	CLRB1	"0" = asynchronously resets all latches in Shift Register (Corresponds to POGO PAD 4)
48	LOAD	"1" = gates the data and target address from the output of the shift register into the decoders (Corresponds to POGO PAD 5)
49	EN2B	"0" = updates the electrode array by loading data from the first latch in every cell into the second latch. (Corresponds to POGO PAD 6)
50	V100	100 Volt power supply (Corresponds to POGO PAD 13)
51	EN1B	"0" = loads data into the first latch of the target cell in the array. The target cell is determined by the R and C addresses that activate the corresponding ROW and COL signals. (Corresponds to POGO PAD 7)
52	CLRB2	"0" = asynchronously resets the memory of all the array cells (Corresponds to POGO PAD 12)
53	VIN	Input signal to all digital drivers. Generally a square-wave function from 0V to 5V and frequency up to 10kHz. (Corresponds to POGO PAD 8)

54	INJ	Injection control Data into the dual latch of COL31INJ. "0" will turn off HV xtr at COL31INJ and allow COL31 to output the normal 2-phase 100V square wave. "1" will turn on HV xtr at COL31INJ and pull the voltage at the electrode of COL31 to GND. (Corresponds to POGO PAD 11)
55	REFINJ	Injector Reference electrode voltage (Corresponds to POGO PAD 10)
56-75	VSS	Ground (20 pads) (Corresponds to POGO PAD 9)
76-95	V5	5V power supply (20 pads) (Corresponds to POGO PAD 1)

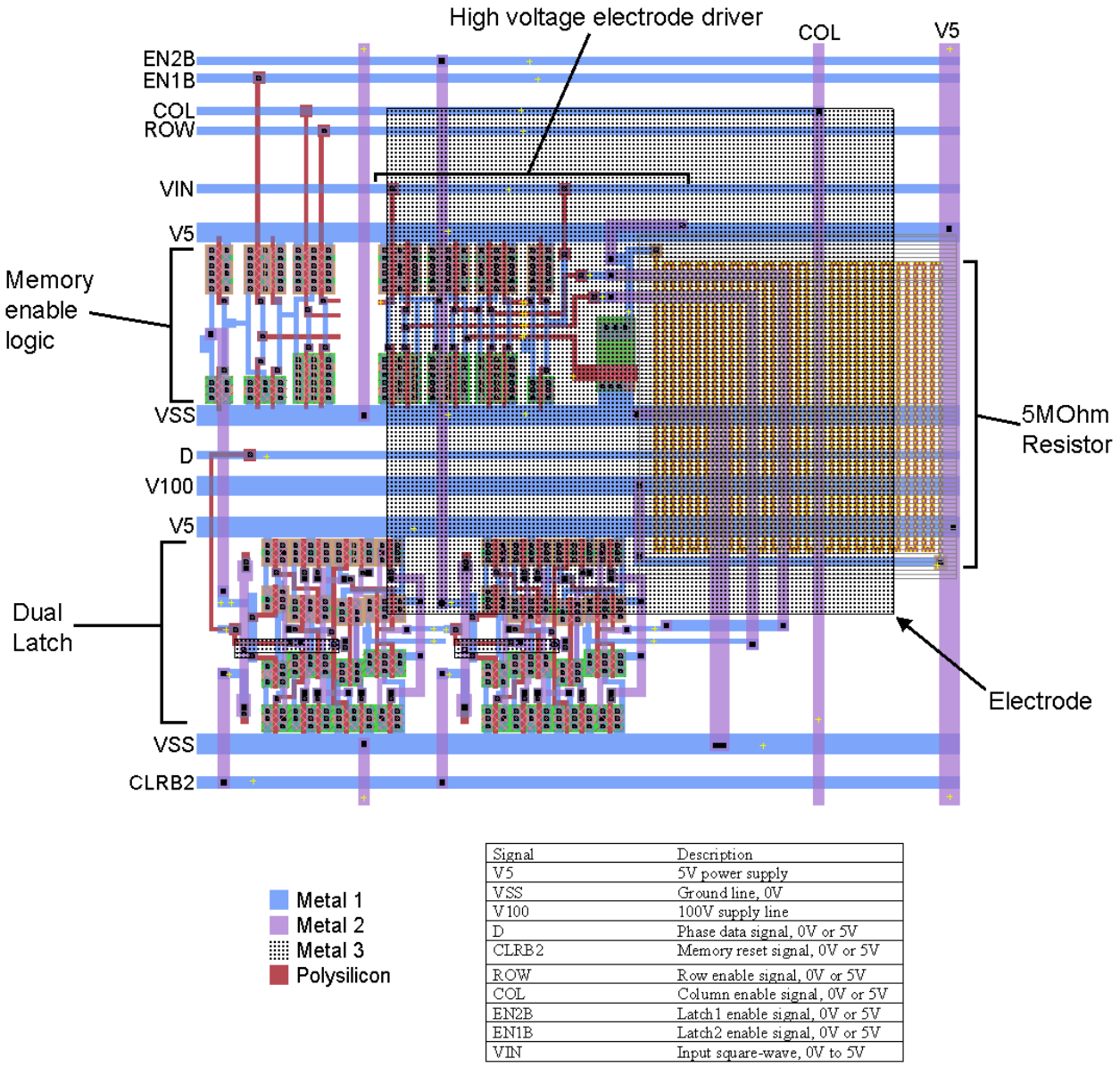
Table 7. PFP5 Monitor/Override lines

Bonding Pad Number	Signal	Description
1	C4_LOAD_PB	Valid post-buffered C4 address bit monitor and/or override. Valid C4 after LOAD = "1." Connected to POGO PAD 18. Corresponds to signal 'C4' in Figure 4.
2	C3_LOAD_PB	Valid post-buffered C3 address bit monitor and/or override. Valid C3 after LOAD = "1." Connected to POGO PAD 17. Corresponds to signal 'C3' in Figure 4.
3	C2_LOAD_PB	Valid post-buffered C2 address bit monitor and/or override. Valid C2 after LOAD = "1." Connected to POGO PAD 16. Corresponds to signal 'C2' in Figure 4.
4	C1_LOAD_PB	Valid post-buffered C1 address bit monitor and/or override. Valid C1 after LOAD = "1." Connected to POGO PAD 15. Corresponds to signal 'C1' in Figure 4.
5	C0_LOAD_PB	Valid post-buffered C0 address bit monitor and/or override. Valid C0 after LOAD = "1." Connected to POGO PAD 14. Corresponds to signal 'C0' in Figure 4.
6	R4_LOAD_PB	Valid post-buffered R4 address bit monitor and/or override. Valid R4 after LOAD = "1." Corresponds to signal 'R4' in Figure 4.
7	R3_LOAD_PB	Valid post-buffered R3 address bit monitor and/or override. Valid R3 after LOAD = "1." Corresponds to signal 'R3' in Figure 4.
8	R2_LOAD_PB	Valid post-buffered R2 address bit monitor and/or override. Valid R2 after LOAD = "1." Corresponds to signal 'R2' in Figure 4.
9	R1_LOAD_PB	Valid post-buffered R1 address bit monitor and/or override. Valid R1 after LOAD = "1." Corresponds to signal 'R1' in Figure 4.
10	R0_LOAD_PB	Valid post-buffered R0 address bit monitor and/or override. Valid R0 after LOAD = "1." Corresponds to signal 'R0' in Figure 4.
11	ROW11_PB	Post-buffered ROW11 monitor and/or override.
12	ROW12_PB	Post-buffered ROW12 monitor and/or override.
13	ROW13_PB	Post-buffered ROW13 monitor and/or override.
14	ROW14_PB	Post-buffered ROW14 monitor and/or override.
15	ROW15_PB	Post-buffered ROW15 monitor and/or override.
16	ROW16_PB	Post-buffered ROW16 monitor and/or override.
17	ROW17_PB	Post-buffered ROW17 monitor and/or override.
18	ROW18_PB	Post-buffered ROW18 monitor and/or override.
19	ROW19_PB	Post-buffered ROW19 monitor and/or override.

20	ROW20_PB	Post-buffered ROW20 monitor and/or override.
21	COL20_PB	Post-buffered COL20 monitor and/or override.
22	COL19_PB	Post-buffered COL19 monitor and/or override.
23	COL18_PB	Post-buffered COL18 monitor and/or override.
24	COL17_PB	Post-buffered COL17 monitor and/or override.
25	COL16_PB	Post-buffered COL16 monitor and/or override.
26	COL15_PB	Post-buffered COL15 monitor and/or override.
27	COL14_PB	Post-buffered COL14 monitor and/or override.
28	COL13_PB	Post-buffered COL13 monitor and/or override.
29	COL12_PB	Post-buffered COL12 monitor and/or override.
30	COL11_PB	Post-buffered COL11 monitor and/or override.
32	COL31_PB	Post-buffered COL31 monitor and/or override.
33	COL31C	C monitor and/or override of cell (0,31)

Digital driver test cell

The layout of the digital driver test cell in PFP5 is shown in Figure 17 with labels and legend on the different parts of the cells. The cell has the enlarged M3 electrode on it. The layout corresponds to the digital driver cell schematics shown in Figures 8 and 9 with the signals. The control signals for the test cell are described in Table 8.



Signal	Description
V5	5V power supply
VSS	Ground line, 0V
V100	100V supply line
D	Phase data signal, 0V or 5V
CLRB2	Memory reset signal, 0V or 5V
ROW	Row enable signal, 0V or 5V
COL	Column enable signal, 0V or 5V
EN2B	Latch1 enable signal, 0V or 5V
EN1B	Latch2 enable signal, 0V or 5V
VIN	Input square-wave, 0V to 5V

Figure 17. Layout of the digital driver test cell

Table 8. Signals for the digital driver test cell

Bonding Pad Number	Signal	Description
37	EN2B	"0" = updates the digital driver test cell (DD) electrode by loading data from the first latch into the second latch.
38	EN1B	"0" = loads data into the first latch of the test cell. ROW and COL must = "1" to activate the first latch of the DD test cell.
39	VIN	Input signal into the test cell's digital driver Generally a square-wave function from 0V to 5V and frequency up to 10kHz.
40	V5	5 Volt power supply of DD test cell. ROW & COL tied HIGH here

41	VSS	Ground of the DD test cell
42	D	Data into first latch of the DD test cell's logic
43	V100	100V supply of the DD test cell
44	CLRB2	"0" = asynchronously resets the memory of the DD test cell

High voltage level shifter (HVLS)

The high voltage level shifter (HVLS) test cell schematic is shown in Figure 18 and its signal descriptions and bond pads are given in Table 9. The supply V100 receives the high voltage supply, while V95 is 5V below V100, turning on M4 and M5. When VIN is high, M8 is on and the VOUT is driven to ground. When VIN is low, M6 is off, M7 is on and node 2 is pulled toward ground. When 2 is pulled toward ground, M1 turns on and pulls 1 toward V100 causing M2 to turn off. Since 2 is pulled towards ground, M3 is also turned on, which pulls VOUT to V100.

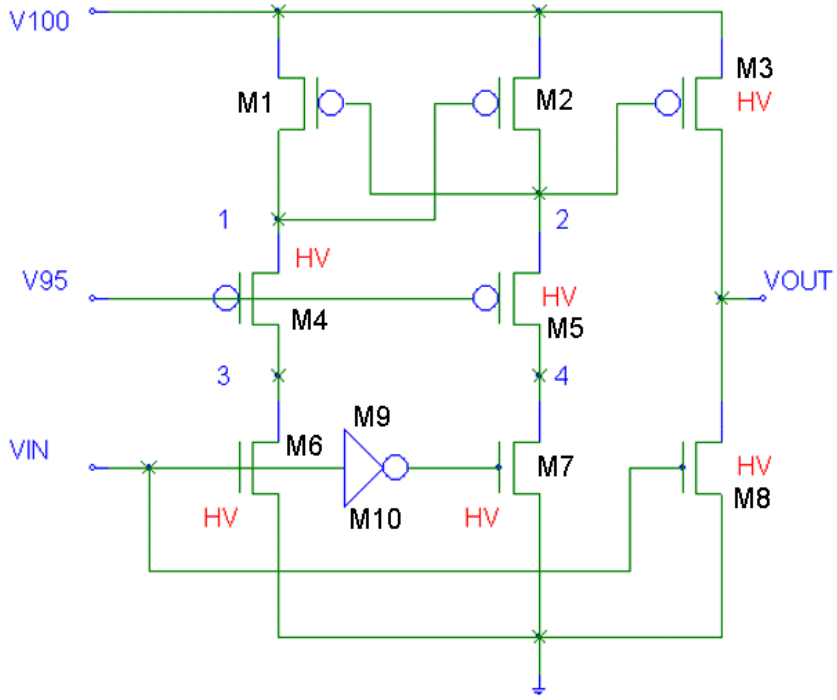


Figure 18. High voltage level shifter schematic

Table 9. Signals for the high voltage level shifter circuit

Bonding Pad Number	**Signal**	**Description**
41	VSS	Ground
35	VOUTLS	Output Voltage
40	V5	Supply Voltage for Logic
43	V100LS	100 Volt Supply
36	V95LS	95 Volt Bias Voltage
39	VIN	Input Voltage
NA	4	Intermediate Node 4
NA	3	Intermediate Node 3
NA	2	Intermediate Node 2
NA	1	Intermediate Node 1

Addition of the D Latch cell w/o M3 jumper as a test cell

A version of the D latch without the M3 jumper is also placed as a test cell on PFP5. The original D latch with M3 jumper is shown in Figure 19a and the updated D Latch without M3 jumper is shown in Figure 19b. The M3 jumper routes the CLRB signal from the left of the D latch to a point in the center of the circuit. Due to possible interference with the M3 electrode on the digital driver cell, the D latch has been modified to operate with the M3 jumper. Instead, the poly line that connects the CLRB signal is routed from the center of the cell out towards the right of the D latch as shown in Figure 19a. The D latch used in the driver array is still of the M3 jump type, however the jumper-less version has been included as a test cell for analysis. The bond pad signals for the D latch w/o M3 jumper are described in Table 10.

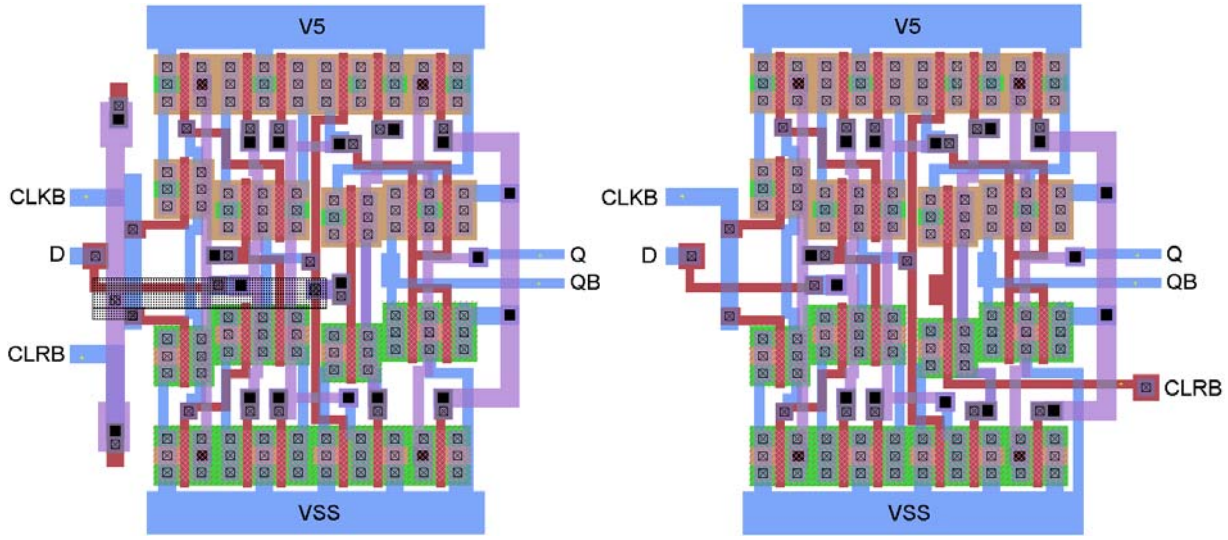


Figure 19. (a) D Latch M3 jumper test cell (b) D Latch without M3 jumper test cell

Table 10. Input and output signals for the D latch without M3 jumper test cell

Bonding Pad Number	**Signal**	**Description**
41	VSS	Ground
40	V5	5V supply Voltage
42	D	Input Data
38	CLKB	Clock signal
44	CLRB	Reset signal
34	Q_DLTEST	Latch output
31	QB_DLTEST	Latch output complement

PFP5 Test Results and Discussion

The PFP5 has been tested and the data showing operation of the programmable driver array and test circuits are provided in this section. The first set of test data illustrates the operation of the driver array at f=100Hz with V100=5V. A standard cell at (0,0) and injector column cell at (0,31) are tested for phase change and reset capability. Additionally, the injector column cell is tested for ground state capability. The same standard and injector column cells are then tested similarly at high voltage V100=100V. The ability to program the driver cells and reset the system verifies the full operation of the communications shift register, partial verification of the decoder operation, and the full operation of the driver cells. To further test the decoders, the row and column decoders are each tested using five addresses and the levels at the corresponding row and column monitor lines are verified.

The digital driver test cell is tested for phase change and reset capability at both low and high voltages. Additionally, the modified DL cell w/o M3 jumper is tested.

Data on the high voltage level shifter (HVLS) is provided in a separate report.

PFP driver array tests at V100=5V

A standard driver cell and injector column cell are both tested for phase programmability and reset capability. Additionally, the injector column cell is tested for ground state output using the third-state electronics. The operating frequency of these tests is 100Hz. Note that the output voltages will appear lower than the supply. This is due to the probe loading of the output which results in an output voltage about two-thirds the V100 supply.

Standard array cell

Array Cell Test 1: Programming from 0-degree to 180-degree phase output to reset

In this first test, the driver cell (0,0) on the PFP5 array is tested for 180-degree to 0-degree phase programmability and reset capability by programming it with a logic high data and then activating the reset.

The test data are shown in Figure 1. At time t=0.018s, CLRB1 and CLRB2 are released and the PFP system is activated. Between t=0.023s and t=0.133s, the address and phase state data from the DATAIN input are loaded into the shift register. The data sequence at DATAIN calls for a logic high phase program on cell (0,0). The LOAD signal is activated between t=0.138s and t=0.153s, allowing for the shift register data to pass to the decoders and array. During this time, at t=0.143s, the EN1B signal is activated and the logic high phase data is stored into the memory of cell (0,0). At t=0.158s, the EN2B signal is pulsed causing and update of the array phase states. The resulting phase change can be seen in the VO(0x0) plot. Finally, at t=0.193s, the CLRB1 and CLRB2 signals are activated and the output of cell(0,0) is reset to 180-degree phase.

This test shows the ability of a standard driver cell to be programmed with a logic high phase data and then reset.

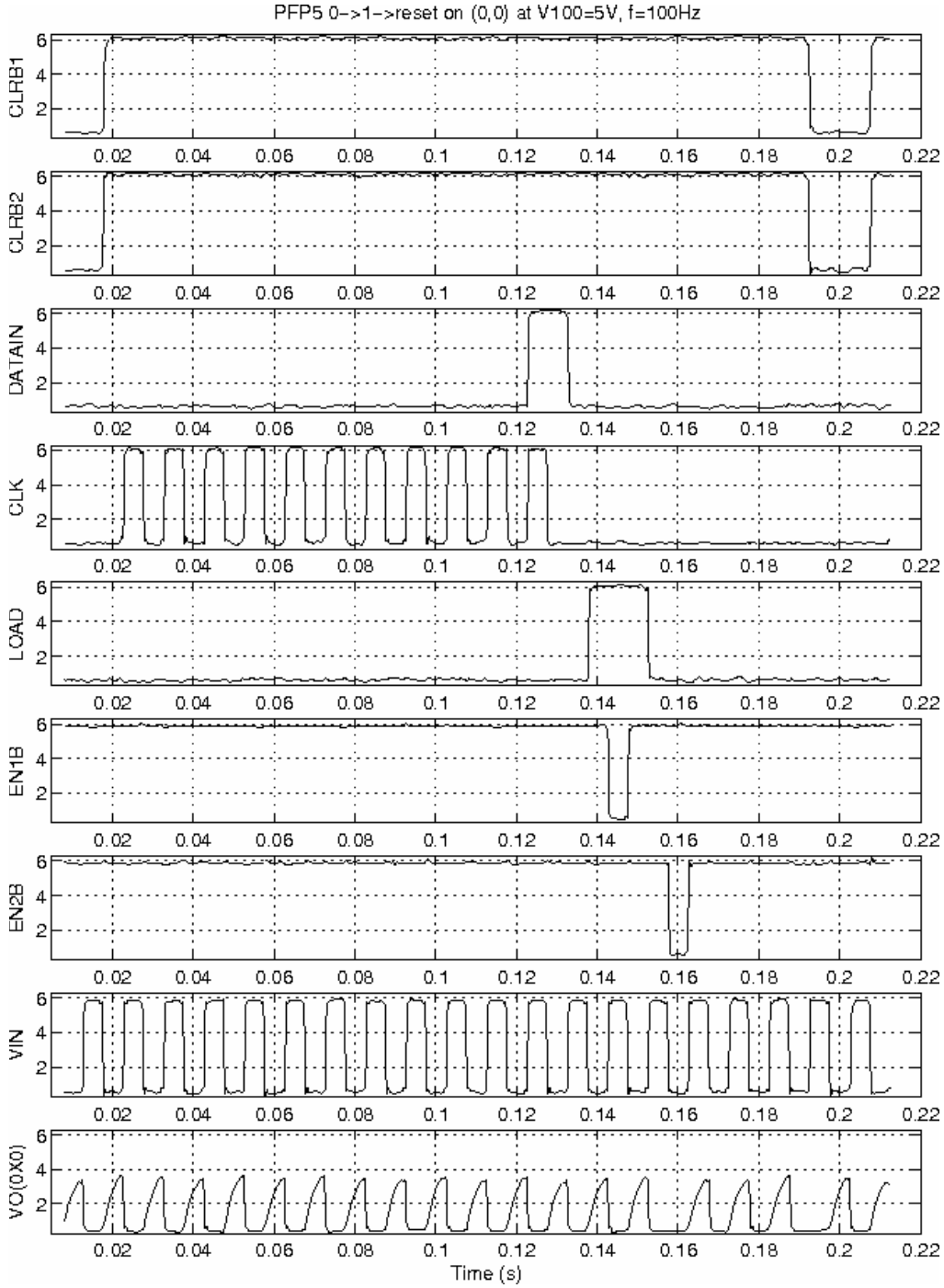


Figure 1. Logic high phase data program and reset on cell (0,0)

Array Cell Test 2: Programming from 0-degree to 180-degree phase

In the second test, the driver cell (0,0) is tested for 0-degree to 180-degree phase programmability by programming it with a logic high data and then with a logic low data. The test data is shown in Figure 2. At time t=0.273s, CLRB1 and CLRB2 are deactivated the PFP system is started. Between t=0.278s and t=0.388s, the data sequence calling for a logic high phase program at cell (0,0) is loaded into the shift register. During the time in which the LOAD signal is activated between t=0.393s to 0.408s, the EN1B signal is activated at t=0.399s and the logic high phase data is stored into the memory of cell(0,0). At

t=0.413s, the EN2B signal is activated the output of cell (0,0) is changed to 0-degree phase. At the same time, the logic low data for the next program of cell (0,0) is loaded into the shift register at t=0.413s until about t=0.523s. The LOAD is again activated at t=0.528s, EN1B is pulsed at t=0.534s, EN2B is pulsed at t=0.548s and the output is set back to 180-degree phase state.

This test shows that the driver cell can be programmed with a logic low phase data from a logic high phase state.

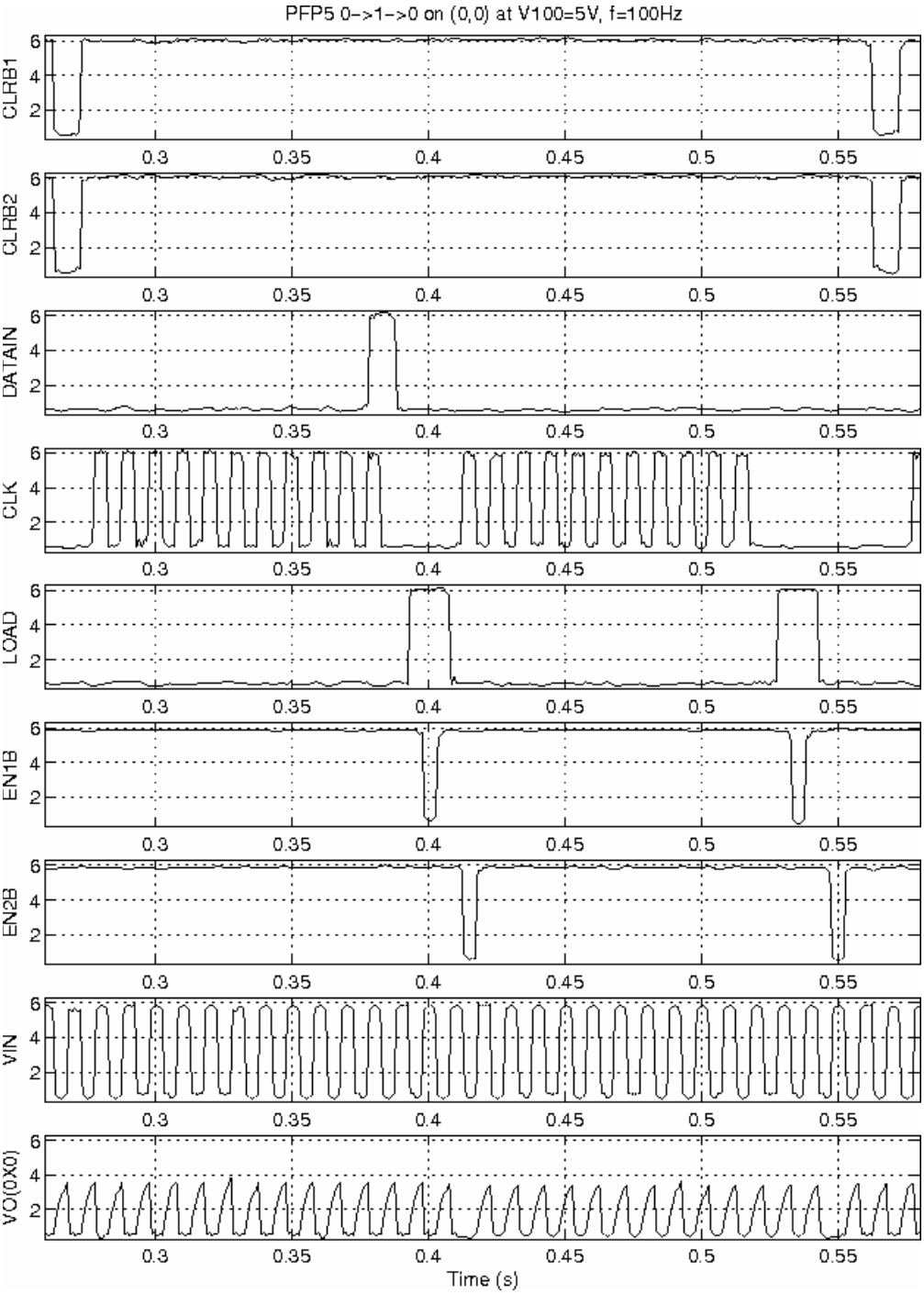


Figure 2. Logic high and logic low phase data program on cell (0,0)

Injector column cell

The injector column cell at (0,31) is tested in a similar way to the standard cell at (0,0). Phase programming from logic low to logic high and from logic high to logic low are performed at 100Hz at V100=5V. Additionally, a ground state program is shown, utilizing the cell's third-state electronics.

Injector Cell Test 1: Programming from 0-degree to 180-degree phase output to reset

The first test is exactly the same as the first test for cell (0,0). The output shows a 180-degree to 0-degree phase state change at the time EN1B is activated.

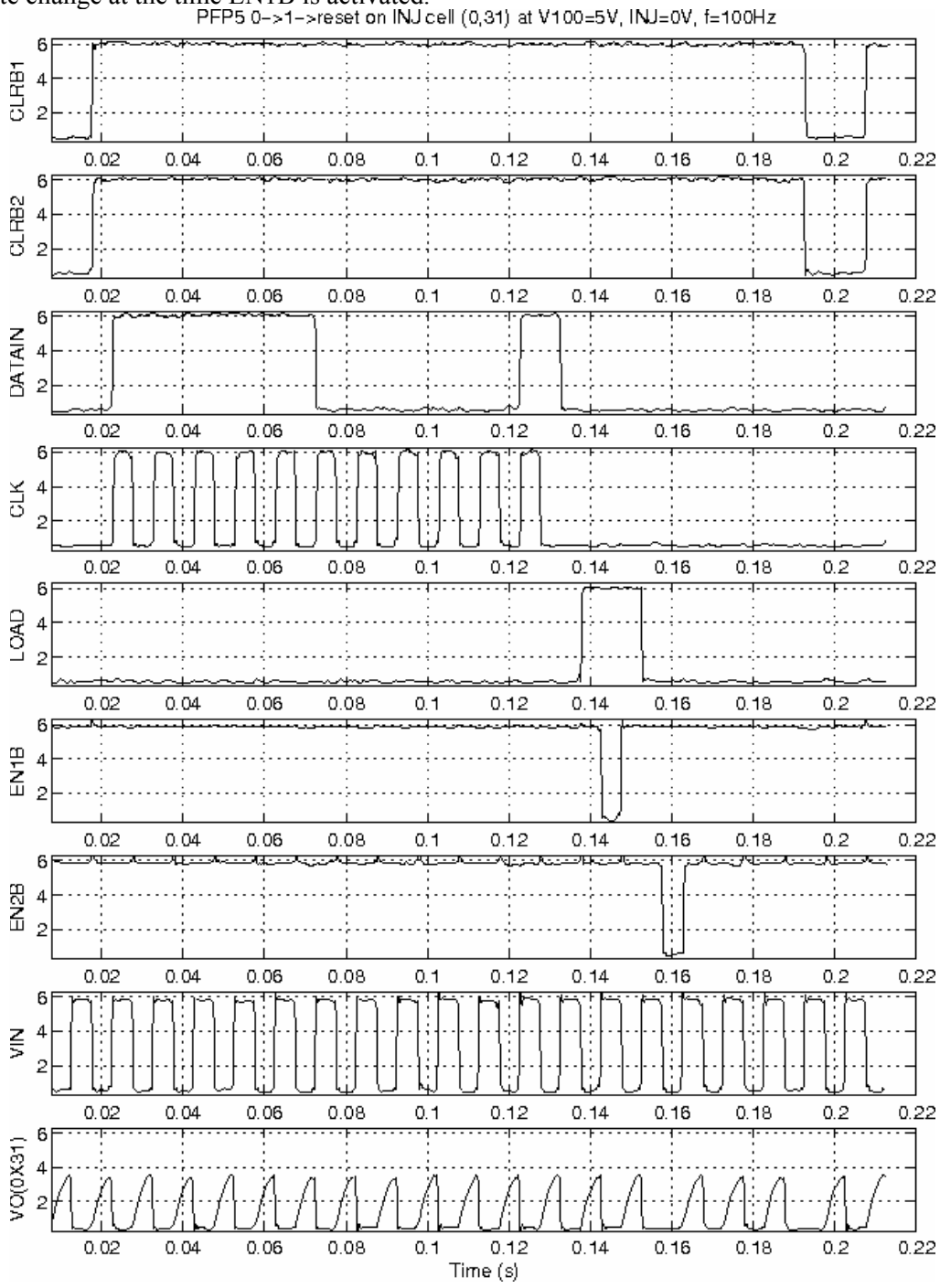


Figure 3. Logic high phase data program and reset on cell (0,31)

Injector Cell Test 2: Programming from 0-degree to 180-degree phase

The second test on the injector column cell (0,31) is the same logic low program as for cell (0,0). The test shows the driver cell's capability to be exert a 0-degree to 180-degree phase program.

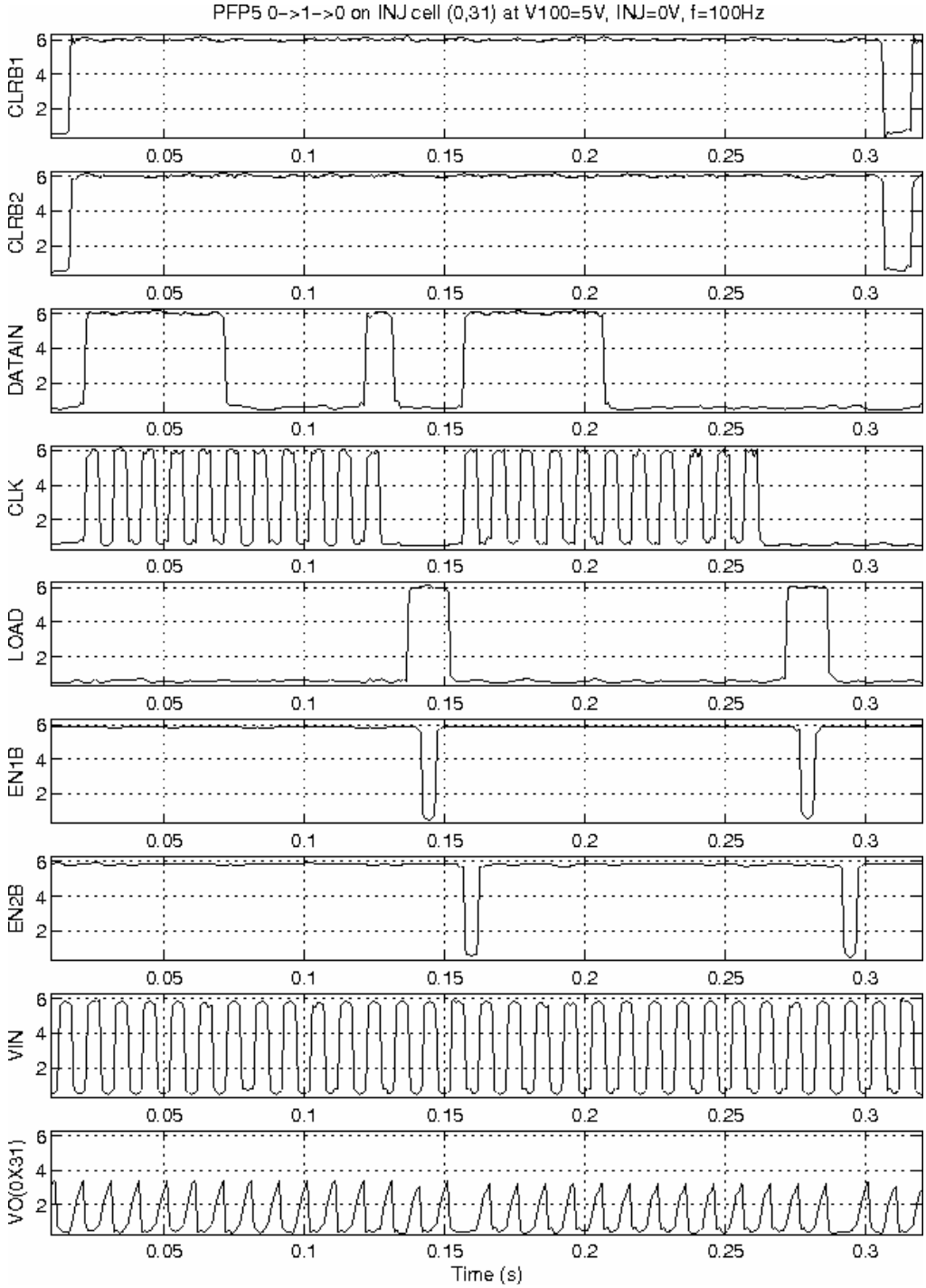


Figure 4. Logic high and logic low phase data program on cell (0,31)

Injector Cell Test 3: Programming from 180-degree phase to ground to reset

The third test performed on the injector cell (0,31) at V100=5V is the ground state test. The programming cycle is exactly like that used in the logic high phase data program except that the data signal INJ=5V, which commands the third-state electronics to pull the output towards ground.

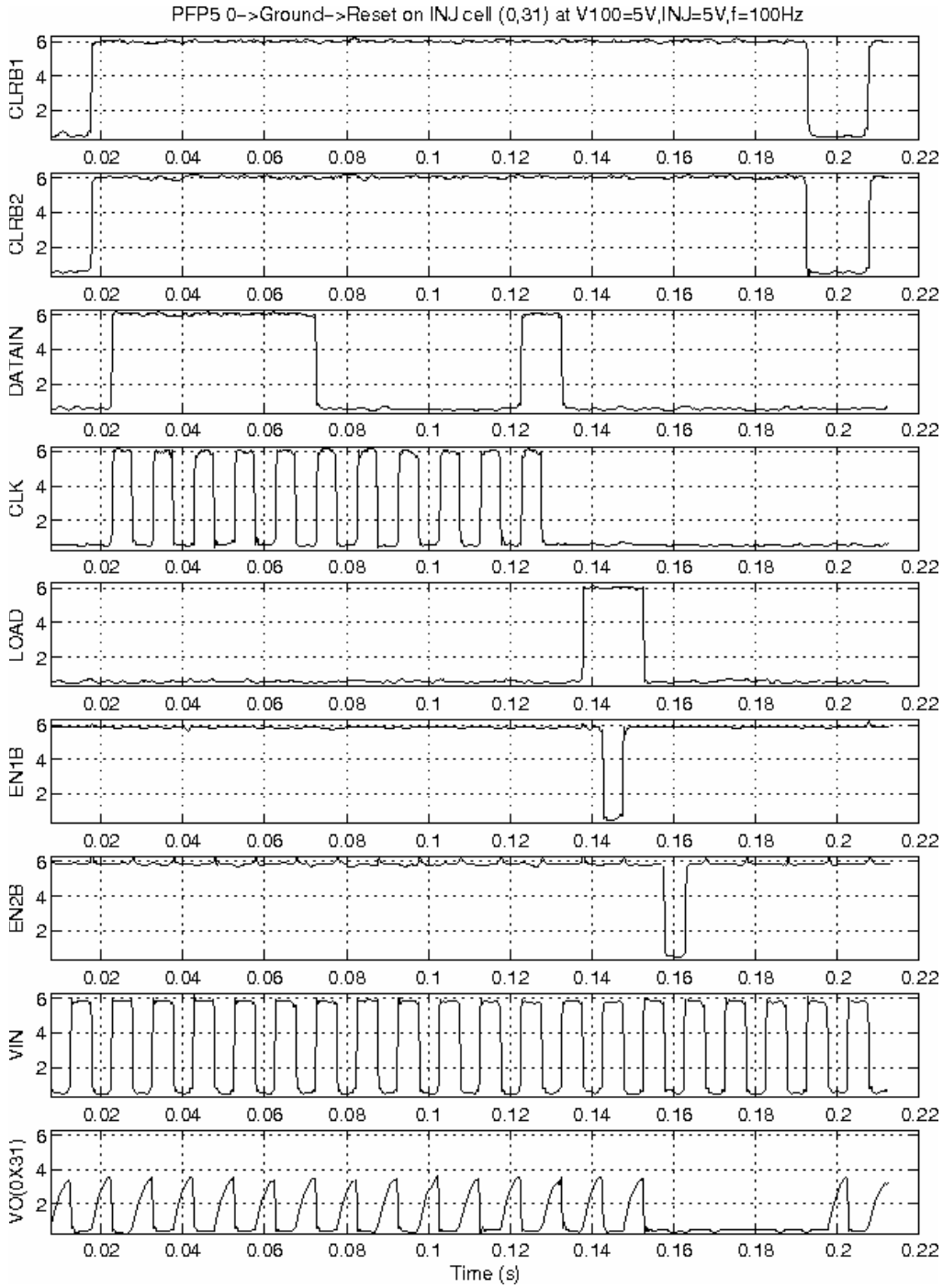


Figure 5. Ground state program on injector cell (0,31)

The test data for the ground state test is shown in Figure 5. At the same time that the injector cell (0,31) is addressed and programmed with a logic high phase data, the corresponding injection circuitry is also

being addressed and programmed. However, the injection circuitry's memory will receive data from the INJ input rather than from the shift register. When EN2B is pulsed at t=0.158s, the third-state electronics updates its output with the logic high INJ data and pulls the output towards ground as seen in Figure 5. This causes the output to be grounded rather than exhibiting a phase change to the 0-degree phase output state. Like the array driver circuitry, the injection circuitry is also reset by the CLRB2 signal. At time t=0.193s, CLRB2 is activated and the injection circuitry's memory is also reset. This causes the output to return to the original 180-degree phase state.

This test shows the correct operation of the injection circuitry and that the injection cell's output can successfully produce the 0V ground state needed for DEP-assisted droplet injection.

High voltage tests on PFP array cells

The driver cell is tested for phase change capability, reset capability and ground state capability at high voltage V100=100V. An injector cell is chosen for this test for convenience. Complete operation of the injector cell at high voltage will infer correct operation of the standard cell due to their similar design. A logic high phase data program is performed on cell (0,31), first with INJ=0V and then with INJ=5V. The first case will verify a transition from a 180-degree to 0-degree output signal, while the second case will demonstrate a 180-degree to ground state transition. In the third test, the injector cell is tested for 0-degree to 180-degree phase programming at high voltage. Note that in these high voltage tests, the output of the driver cell will update earlier than when the EN2B signal is pulsed. This phenomenon has been previously attributed to faultiness in the test setup and does not constitute misoperation of the circuit. Tests have been conducted to verify that the output will not update with out the use of both EN1B and EN2B in the designed order.

High Voltage Test 1 and 2: Programming to 0-degree phase output state at V100=100V. Programming to ground state at V100=100V.

The waveform data for these two tests are shown in Figure 6. The tests have been combined since the only difference in the input waveforms is the INJ data. In the first test, INJ=0V and the injector cell output should change phases from 180-degrees to 0-degrees and reset back to the 180-degree phase state like a standard driver cell. In the second test, INJ=5V, and the injector cell should change from a 180-degree phase state to the ground state and then reset back to the 180-degree state.

The injector cell (0,0) is programmed in the same way as in Test 1 of the low voltage standard cell test with the exception of the V100 voltage supply level. According to Figure 6, the output of the injector cell (0,31) correctly changes phases from 180-degrees to 0-degrees and then resets back to 180-degrees. While the output seems to update during the time at which EN1B activates, it is still controlled by the EN2B signal. Also, the actual voltage level shown in Figure 6 is only two-thirds of the V100 voltage supply, which is again due to the probe loading effect. This test shows the ability of the driver cell to change phases at V100=100V by programming a logic high phase data bit.

In the second test, the same inputs are used but INJ=5V, which causes the output to go to ground once the array is updated. The output signal is shown at the bottom of Figure 6. Similar to the above case, the output updates to a ground state earlier than when the EN2B signal is pulsed. Again, the output update has been verified to rely on the pulsing of EN1B and EN2B and will not change otherwise. This test shows that the injector cell can achieve a ground output state while operating at a V100=100V.

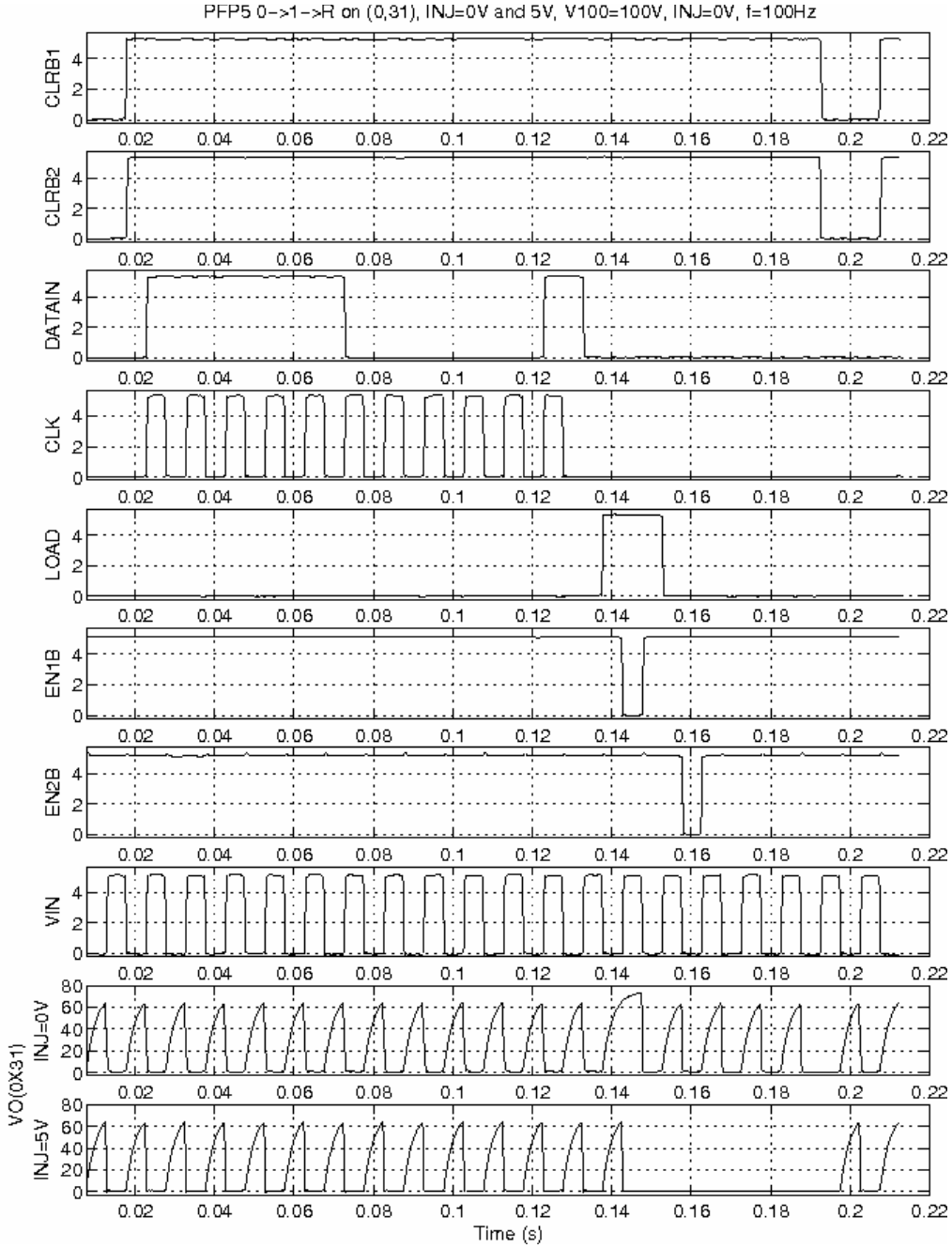


Figure 6. Logic high phase data program and reset on cell (0,0) at V100=100V

High Voltage Test 3: Programming from 0-degree to 180-degree phase

The test performed here is the same test as described in Test 2 of the standard cell test except that the high voltage supply V100=100V instead of 5V. The injector cell (0,31) is first programmed with a logic high phase data causing the output to transition from 180-degree to 0-degree phase. The cell is then programmed with a logic low phase data, causing the output to change back to the 180-degree phase output state. The reset does not change the output state since the cell has already been programmed with a logic low phase data.

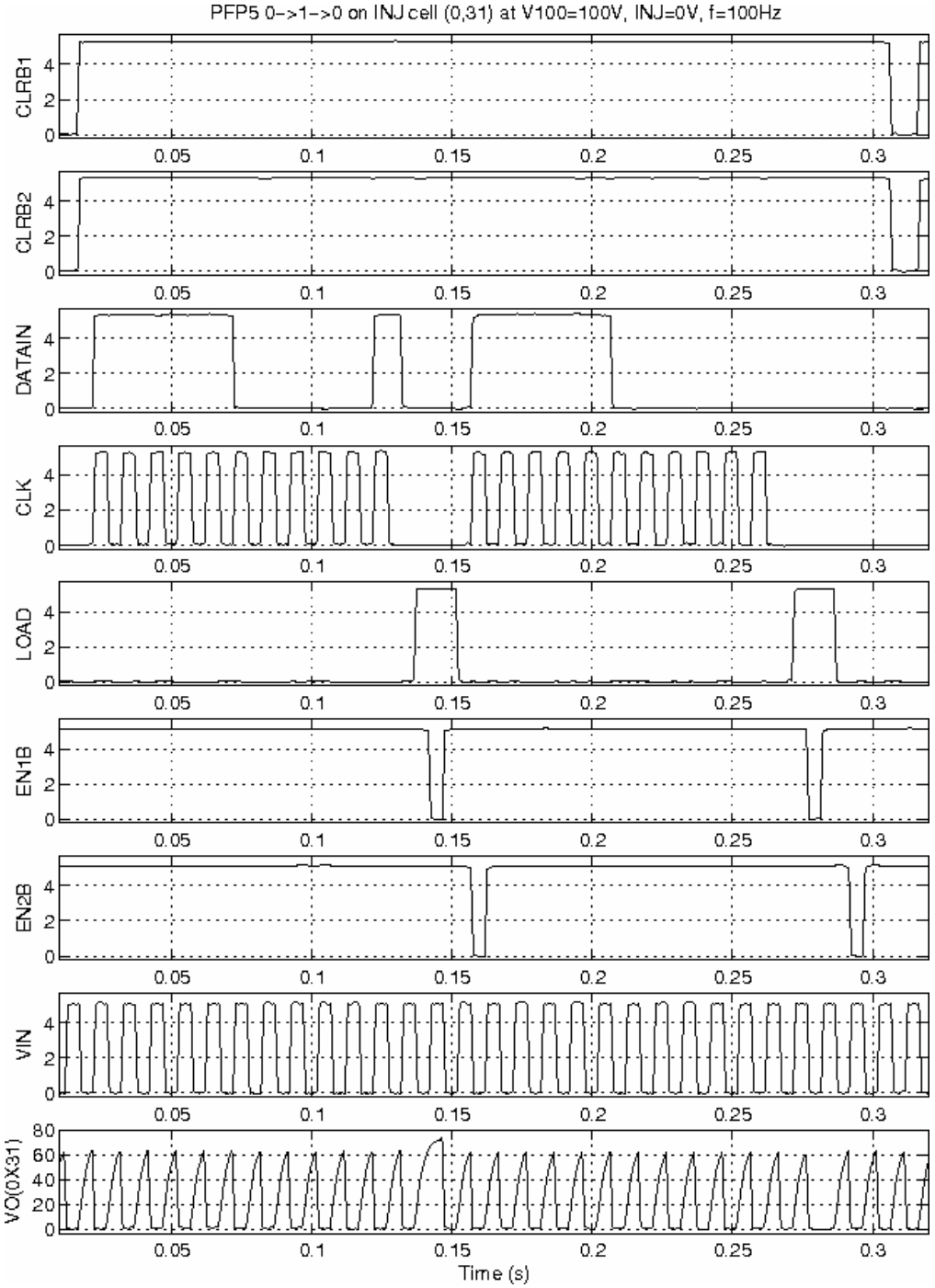


Figure 7. Logic high and logic low phase data program on cell (0,0) at V100=100V

This test shows that the injector cell is capable of being programmed with a logic low data at V100=100V. Again, note the presence of the early update and the reduction of the output peak voltage to two-thirds the V100 supply.

Column and Row Decoder Tests

The column and row decoders are tested directly using the monitor lines provided for 5 addresses. Each decoder is test by continuously loading the shift register with a series of addresses that correspond to the available column and row monitor lines. The column decoder is tested for columns 20, 19, 18, 17 and 16. The row decoder is tested for rows 15, 14, 13, 12, 11. The decoder tests are performed at 10kHz, the original performance goal for the circuitry frequency. Since complete testing by monitoring all row and column output lines is not efficient in terms of pad outs, the alternative used here is to test the decoders for a subset of addresses. Complete testing is still possible by attempting phase programs on cells residing on all rows and columns of the array, but is not performed for the sake of brevity.

Column Decoder Test

The column decoder is tested for operation using the five available column monitor lines for columns 20, 19, 18, 17 and 16. The waveform data is shown in Figure 8. At time t=0.17ms, the CLRB1 signal is deactivated and the shift register becomes ready to read in data. Between t=0.22ms to 3.42ms, the shift register continually loads in the binary sequence corresponding to the addresses 20, 19, 18, 17 and 16 in sequence. The 5-bit column addresses pass through the shift register and as each desired address becomes present within the column address portion of the shift register, the LOAD signal is activated and the corresponding column line is activated. For example, once the address for column 20 reaches the shift register's last 5 memory elements (corresponding to the column address) at t=1.28ms, the LOAD signal is activated, the address is decoded by the column decoder and COL20 is enabled high, verifying that the column address for 20 has been decoded correctly. The process is repeated for each of the five addresses. From the data presented in Figure 8, the column decoder seems to be working correctly.

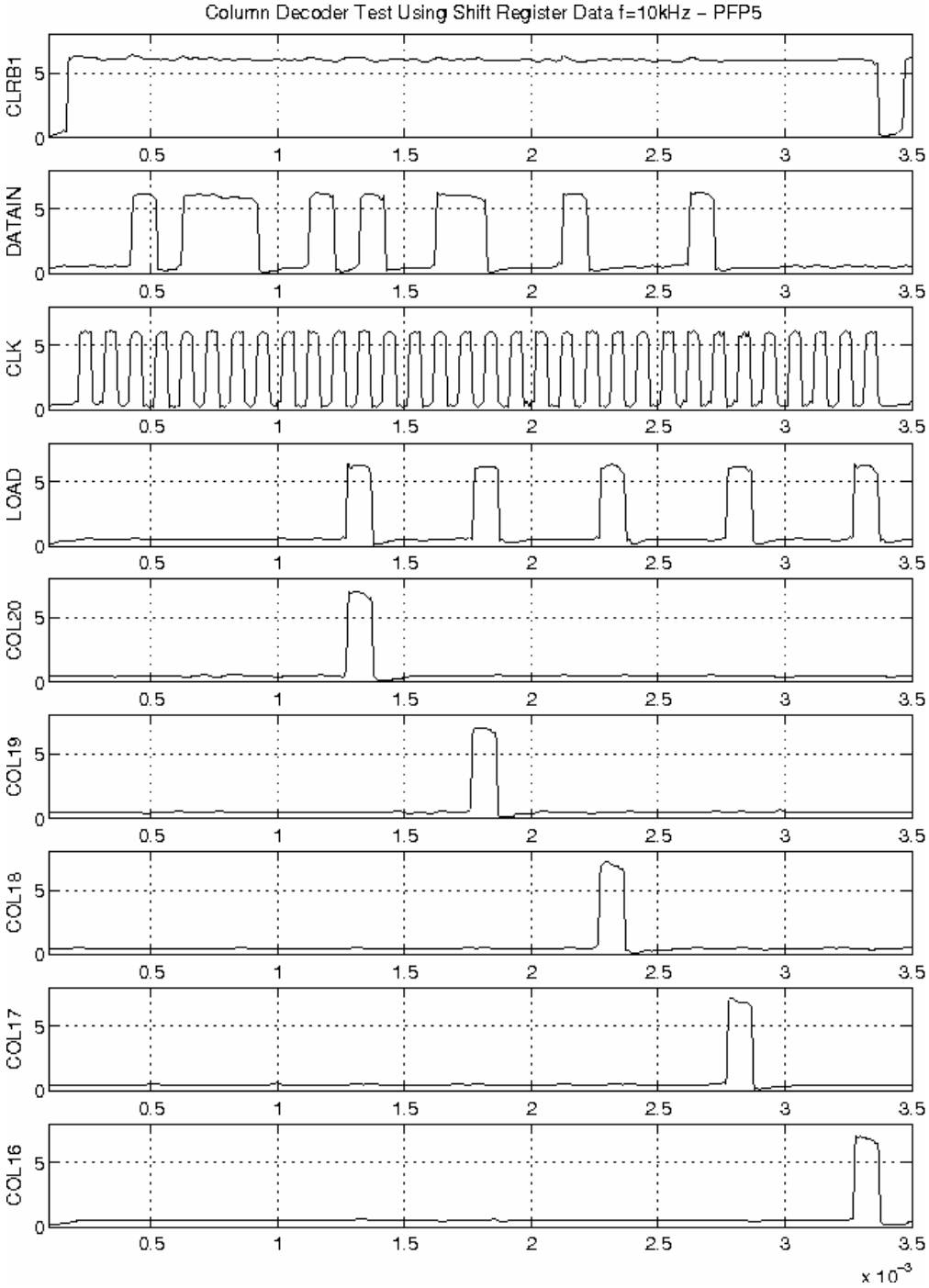


Figure 8. Column decoder test

Row Decoder Test

The row decoder test is similar to the column decoder test. The two differences are the addresses used and the timing of the LOAD signal pulses. The sequence of row addresses used for this test are rows 15, 14, 13, 12 and 11. These addresses are loaded into the shift register and as they pass into the row decoder portion of the shift register, the LOAD signal is pulsed, sending the address to the decoder. The row decoder decodes the address and activates the corresponding row line. The LOAD signal pulses earlier

for the row decoder test than for the column decoder test since the memory elements of the shift register assigned to the row address are located earlier.

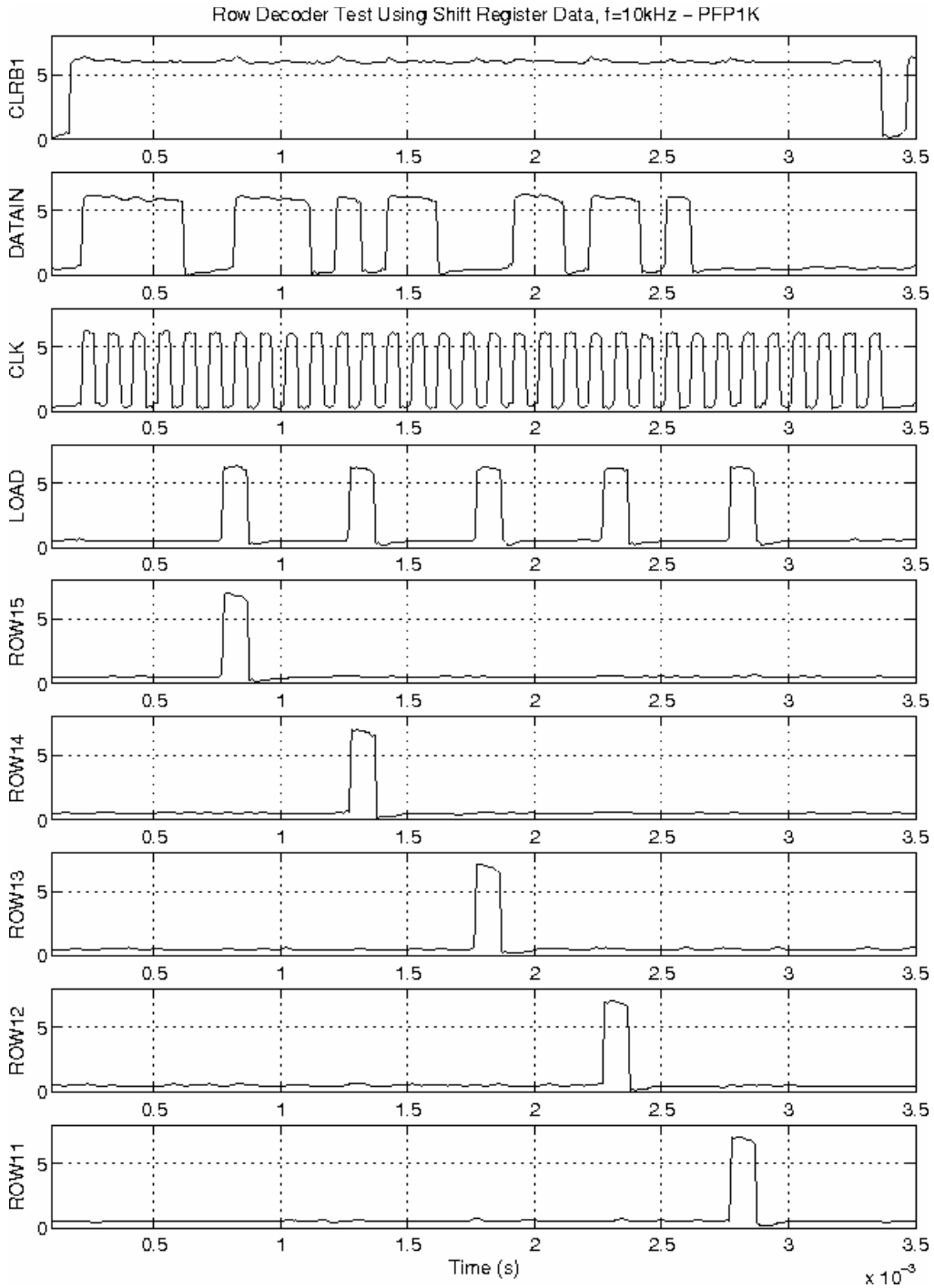


Figure 9. Row decoder test

The row decoder test waveforms in Figure 9 show that the appropriate row lines are enabling as the addresses are passed through the shift register and LOAD is pulsed. From the data presented in Figure 9, the row decoder seems to be working correctly.

Digital Driver Test Cell

The digital driver test cell is tested by directly programming its memory with a logic high phase data bit, enabling EN1B and EN2B to produce the 180-degree to 0-degree output phase transition and then a reset back to the 180-degree phase output. The test is performed at both V100=5V and V100=100V and the waveforms are shown in Figure 10.

At time t=0.0115s, the CLRB signal is deactivated and the driver cell memory begins operation. The data D is set to logic high at t=0.0165s. At t=0.0315s, EN1B is pulsed and the logic high D data is stored into the driver cell memory. At t=0.0464, EN2B is pulsed and the output changes from 180-degrees phase to 0-degrees phase. At t=0.0714, the driver memory is reset and output changes back to 180-degrees phase.

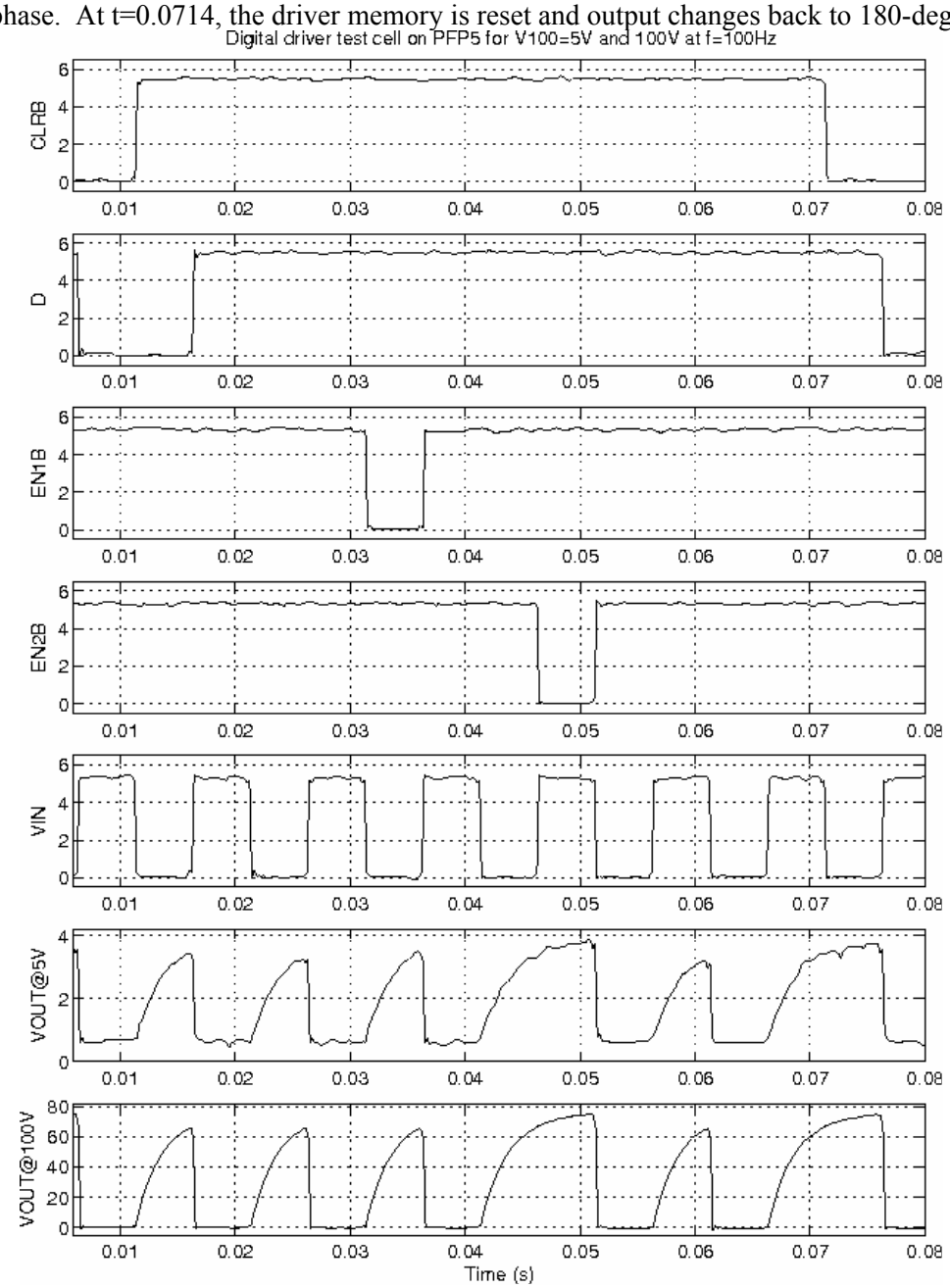


Figure 10. Digital driver test cell for V100=5V and V100=100V

The output for both V100=5V and V100=100V change phases properly. Again note that the output levels are only at two-thirds the V100 supply due to the probe loading effect. However, note that despite the use

of high voltage at V100, there is no early phase update of the output as seen in the driver array tests. This further affirms that the early updating is attributed to the test setup. This test verifies the programmability and phase change capability of the digital driver cell at both low and high voltages.

DL without M3 jumper

The DL without M3 jumper, DLNEW, has been tested successfully and the results are shown here. The DLNEW cell is the low logic level sensitive latch used in the dual stage memory of the shift register and the driver cell. It is tested here for latching a logic high and logic low memory as well as a memory reset operation at f=100kHz.

The test waveforms are shown in Figure 11. At time t=1.5us, CLRB is deactivated and the latch is ready to store data. At the same time, CLKB is set to logic high and D is pulsed for half a period, but the output remains logic low since the latch is low level sensitive. At time t=11.32us, D is set to logic high again, but the output does not change until CLKB goes to logic low at t=16.45us. The latch reads in the logic high D, Q changes to logic high and QB changes to logic low. The logic high Q output is held until CLKB is pulsed logic low again at t=31.45us, and the logic low D is stored into the latch. The Q output changes to logic low and remains there until CLKB is pulsed again at t=46.45us, which causes Q to change back to logic high. Finally, the memory is reset t=61.5us, and Q resets to logic low.

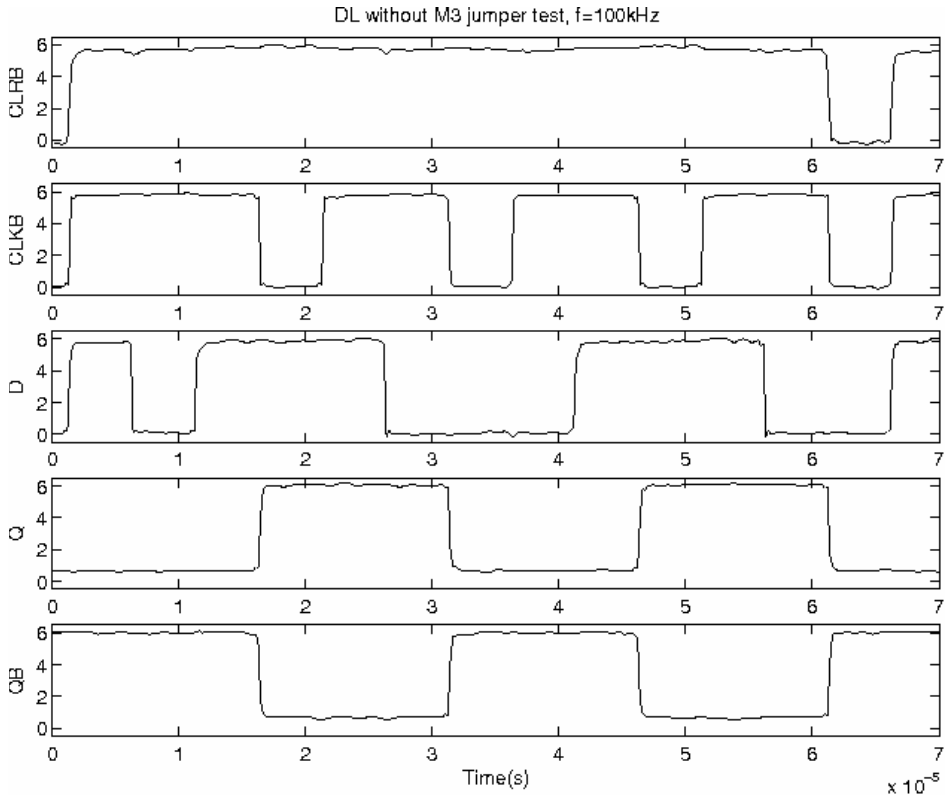


Figure 11. DL without M3 jumper

Note that in this test, the D data is held longer than the CLKB pulse in order to make sure that all set and hold times for the latch have been met. If D transitions too quickly after CLKB returns to logic high, that transition may be passed to the output. This test verifies that the DL without M3 jumper can store logic high and logic low data and can be reset.

Tasks 25. Test 3rd gen IC

We have successfully demonstrated the movement of a droplet across the surface of the new PFP chip, version 4. Figure 1) is a videotape frame that shows a hydrocarbon-suspended aqueous droplet moving across a PFP4 chip under low-level software control driven by the LynnTech Processor Board (Task 39).

The droplet is PBS (phosphate buffered saline), 700 microns in diameter (180 nl volume), suspended in 1-bromododecane. The chip is one of the new PGA-mounted PFP4s. The surface of the PFP has been coated with ~5 microns of SU-8 topped with a mono-layer of FluoroPel 1604 (containing vinyl granules ~4 microns across). The sequentially-switched PFP electrodes were driven by a 5 Vp-p, 19 Hz signal (Vin). The high-voltage supply rail, V100, was set to 25 V, which represents a tremendous improvement over earlier devices.

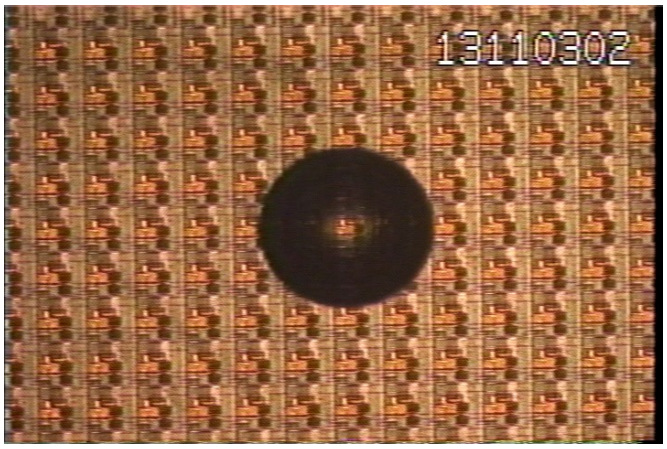


Figure 1) An 180 nl droplet of PBS executing software-controlled movement across the surface of the PFP version 4.

Control of droplet movement was exercised through via the LynnTech Processor Board using low-level keyboard commands via a hyper-terminal emulator that directly accessed the COM port. Each pad-to-pad movement utilized a four-step control sequence:

1) Set current electrode to secure droplet,
2) Reset current electrode to release droplet,
3) Set next electrode to move droplet between current and next electrode, and
4) Reset next electrode to centre up droplet on next electrode.

The above "break before make" sequence leads me to suspect that the droplet is experiencing a combination of dielectrophoresis and electrophoresis. The droplet tends to "stick" to the electrode after being reset in step 2) above. This has been attributed to a build-up of static charge either within the droplet or as a counter-charge on the dielectrically-coated surface of the electrode. This is believed to be the origin of the "tea effect" which was solved for metal-on-glass electrodes by a coating of the granular FluoroPel, creating a micro-roughened surface. Here, the density of granules was apparently insufficient to prevent charge build-up, and the droplet sticks even after the electrode beneath it has been reset. When the next electrode is set in step 3) above, the droplet tends to straddle the space between its current location and the energised electrode. This occurs because, although the electric field lines run to/from the set electrode and all of its nearest neighbours, the droplet experiences only the fields along the line between its current location and the set electrode. One can observe the droplet vibrate at this point as a result of the very low frequency of Vin. This suggests that the charge (or mirror charge) is thus moved from the current electrode location to the set electrode location. I suspect this because when the next electrode is reset in step 4) the droplet moves to the new position rather than recoiling back to its original position.

I also suspect that this is a result of electrostatics because the very low V100 (~25 V) necessary to get a droplet to straddle a pair of electrodes is essentially the same for the PFP coated with 5 microns of SU-8

and FluoroPel and for the PFP coated only with FluoroPel. The purely DEP component of the force falls off exponentially in the vertical direction, and we have repeatedly noticed that DEP-induced droplet motion requires much higher voltages if the passivation layer is thicker.

A few additional points of interest:
1) The lag time for droplet movement is a result of each command 1) – 4) above having to be keyed in by hand. The speed of droplet motion is a function of the very low V100, and is actually very encouraging.

2) V100 was limited to <~30 V. At higher settings the droplet would pull down too hard and remain immobile.

3) The low-frequency (19 Hz) Vin imparts a visible vibration to the droplet. This vibration is apparently necessary to "shake" the droplet loose from its initial position. Droplet motion becomes less likely above this frequency.

4) The SU-8 does apparently does not form an un-interrupted surface. I think that it does not adhere above some of the electrical traces. This may be a result of the vertical height or "steepness" of the traces, or some other reason. In any event, the SU-8 raises the droplet ~5 microns away from the electrical stuff going on below, but does not increase V100 required for droplet actuation.

5) The oxide layer on the PFP4 chip completely obviates hydrolysis for V100 up to (and occasionally in excess of) 100 V. It does not, however prevent the development of a static (or mirror) charge. The PFP4 chip coated only with the FluoroPel caused droplets to be too "sticky" to move reliably. Indeed, the only droplet motion that I was able to realise on the FluoroPel-only chip was within a couple of minutes of powering it up.

This is very encouraging, but clearly, we need to discuss what changes need (can) be made for the final chip. Several questions come to mind:

1) Should we increase the electrode-to-open space ratio? Both Mr. McConaghy and Dr. Current think that it is feasible. My motivation is asking for this is to use the electrode area to shield the droplets from the electrical signals that lie below. Specifically, the ability to pull down droplets on a completely un-switched array by adjusting V100 and the tendency of droplets to become immobile for V100 >25 V certainly indicates that the DC lines have an effect on droplet above the oxide surface. We have some blank metal-on-glass substrates on the way, from which I can make some electrodes to test the tradeoffs between different aspect ratios. Jun Zeng modelled this in May and concluded that a 2:1 ratio was optimal.

2) Can the layer immediately below Metal 3 (the electrodes) be made thicker to reduce the electrostatic effects on the droplet, or, since these effects are from DC components would a thicker layer do any good?

3) Can a "ground plane" be inserted below Metal 3, or would that simply pull the electric field (and the DEP force) into the chip?

Tasks 26, 28. 3rd generation integrated device fabrication

The University of Texas
MD Anderson Cancer Center
Programmable Fluidic Processor 5
Stage 3 Report
September 27, 2004

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Table of Contents

1. Stage 3 Overview

The following is a report of the work carried out by Applied MEMS, Inc. for The University of Texas, MD Anderson Cancer Center on the design and development of the microfluidic DEP device fabrication within the Programmable Fluidic Process project. The scope of work covered by this report will pertain to the final Stage 3 activities in accordance with the FDP Subaward Agreement under DOD Grant No. DAAD19-00-1-0515 "A General-Purpose Analysis System Based on a Programmable Fluid Processor".

The Stage 3 scope of work defined by the above referenced Subaward included Bisbenzocyclobutene (BCB) lithography on the PFP5 substrates, development of BCB bonding of silicon fluidic layer wafer and the PFP5 wafer, development of BCB bonding process for anodically bonded silicon fluidic layer and PFP5 wafer, and the dicing process development for the BCB bonded Version 3 device. Eleven PFP5 wafers were received from X-Fab, Germany. Figure 1 shows the photo of the wafer. Two of them were sent to Chuck at LLNL for electrical tests. The remaining wafers were used during Stage 3. The remaining two silicon fluidic layers processed during Stage 2 were carried over and are triple-stack bonded during stage 3. Four Version 3 silicon fluidic layers are bonded to PFP5 wafers with BCB as the adhesion layer individually. The definition of completion of Stage 3 work can be found in the memo sent out by Jon Schwartz via email on September 03.

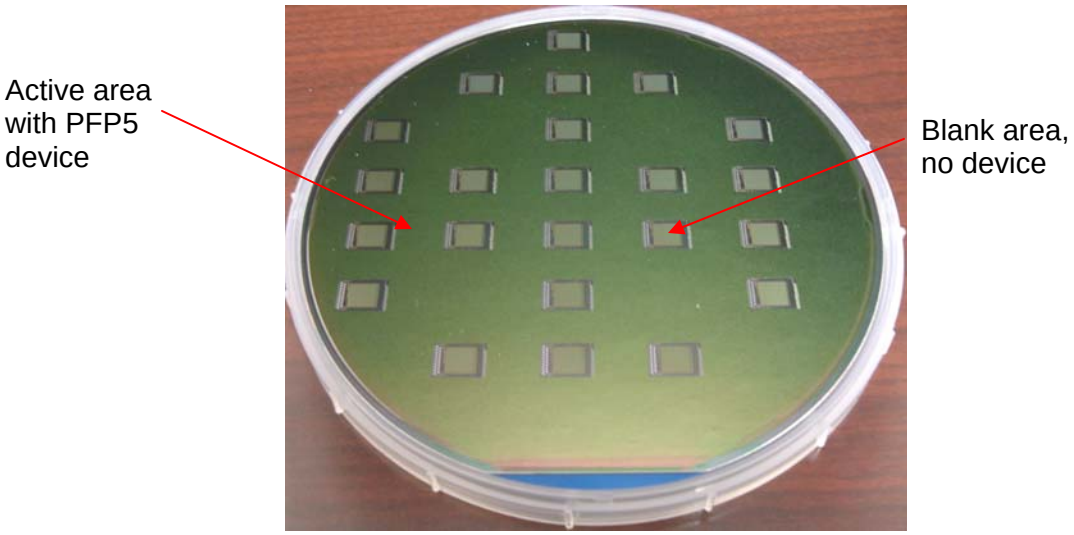

Figure 1. Picture of PFP5 wafer manufactured by X-Fab, Germany. There are active area defined where PFP5 devices are and blank region which has no active device, only layers deposited during fabrication.

1.1. Task 1: BCB Lithography on PFP5 Wafer

In previous work during Stage 2, BCB lithography was further developed to glue the electrode glass layer and silicon spacer layer together as well as to provide a hydrophobic

dielectric layer. In Stage 3, the substrate is PFP5 wafers with features to specifically address each DEP electrode using CMOS circuitry and to control the movement of the droplet. The BCB lithography is developed to accommodate the surface topography of the PFP5 wafer.

The biggest challenge is the planarization of the surface of the PFP5 wafer. With a blank area against every PFP5 device area, shown in Figure 1, the step height of the lowest point to the highest point on the wafer becomes ~ 7.3um, as seen the detailed photo in Figure 2. Table 1 shows the step height between each point.

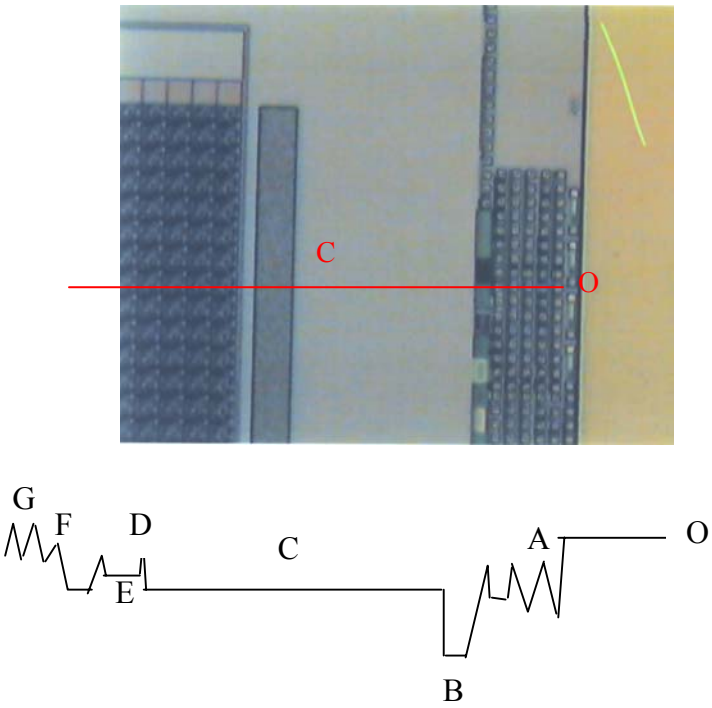

Figure 2. Illustration of the surface topography of PFP5 device. "O" represents the blank area which has no active PFP5 device.

Table 1. Step height between each point. "O" is the reference point.

O	A	B	C	D	E	F	G
0	-1.1um	-7.3um	-3.8um	-2um	-3um	-2.2um	-1um

"C" represents the area around the DEP pads which is about 3.8um lower than the reference point "O". It makes the planarization of the wafer surface with BCB thickness under 12um impossible. However, it could be possible that cross-channel leakage may not occur eventhough it is not completely sealed if the gap is limited and under the threshold inlet pressure.

1.2. Task 2: BCB Bonding of PFP5 Wafer and Silicon Fluidic Layer

Four silicon fluidic layers were prepared to bond to the PFP5 wafer with BCB as the intermediate layer. Two of them were bonded with 12um BCB; and the remaining were bonded with 14.5um BCB. Warpage of PFP5 wafer may negatively affect the BCB bonding result.

1.3 Task 3: Triple Stack Wafer Bonding

Two cover glass wafers with vent ports was bonded to the silicon spacer layer using anodic bonding technique in Stage 2. They were carried over to Stage 3 to bond to the PFP5 wafer with 12um and 14.5um BCB thickness respectively.

1.4 Task 4: Version 3 Dicing Process

Six sets of Version 3 wafers were diced after the BCB bonding process was completed. Blade type, dicing method and other dicing parameters were then optimized to cut the bonded Version 3 wafer set successfully and to deliver chips to MD Anderson.

2. Accomplishments and results

In this section, the detailed experimental results, fabrication and packaging methods and challenges are described.

2.1. BCB Lithography on PFP5 Wafer

In Stage 3, the top silicon fluidic layer was designed to bond to PFP5 wafer using BCB materials. With the design of PFP5 wafer, space was left between each PFP5 device, as seen in Figure 1. In X-fab's process design, layers of different materials were deposited onto the silicon wafer. Only layers at the active PFP5 device area were patterned and removed to create necessary features for dielectricity function. In other words, layers present in the blank area remained intact. It resulted in a step height as large as ~7.5um and more importantly over wide areas that were off-set in height. Planarization is easier over a high density of peaks and valleys as opposed to flat areas that are off set from each other.

Several BCB lithography recipes with thickness and techniques were developed to reduce the step height, such as manually dropping BCB onto the PFP5 device area, double layer coating, and spin-then-drop method. Unfortunately, no significant improvements were achieved in any of the trials, but in some cases worse surface finish was found. After communication with Jon Schwartz of MD Anderson, two thickness of BCB (12um and 18um) were selected for use in Stage 3. Due to the surface difference between glass wafer and PFP5 wafer, the recipe for 18um thickness of BCB on glass wafer developed in Pre-stage 1 phase gave 14.5um thickness of BCB on PFP5 wafers. Table 2 lists the details of these two recipes.

Table 2. Lithography steps of BCB

BCB	Adhesion promoter	Spin condition	Soft bake	Exposure	Pre-develop bake	Develop	Hard bake	Final thickness
4024-40	3000rpm, 30sec	Spread: 50rpm, 90sec Spin: 500rpm, 10sec → 1250rpm, 30sec	85°C, 90sec	600mJ	75°C, 90sec	Puddle: 35sec Rinse: 10sec Spin: 2500rpm, 30sec	120°C, 60sec	~ 10.3um
4024-40 + 4026-46	3000rpm, 30sec	Spin4024-40: 2500rpm, 30sec Spin 4026-46: same as 4024-40	80°C, 90sec, then 90°C, 90sec	3400mJ	80°C, 90sec	Puddle: 60sec Rinse: 10sec Spin: 2500rpm, 30sec	120°C, 60sec	~ 14.5um

From the surface measurement using a profilometer, it was found out the thicker BCB layer actually created a slightly larger step height at the "C" regions, as seen in Table 3. PFP5 device area acted as a recessed 'tub' for BCB. It is likely that when the wafer was spun to develop BCB, BCB emptied out from the device area and accumulated onto the blank area to leave a bigger step height for the thicker layer of BCB.

Table 3. Surface profilometeric measurement using alpha step tool. (in um)

BCB thickness	Step height at "C" region	Step height at "C" region
10.3	-3.6	-5.8
14.5	-4.0	-5.7

Area "C" within the device region is considered the biggest challenge for planarization. The "C" region is around DEP pads and around 3.8um lower than the blank area. In PFP3 and PFP4 design, "C" region is very limited due to the smaller size of the device. The surface planarization quality relies heavily on the feature depth/height and length. The size of "C" region is considered to be too large to fill out completely with only 12um of BCB theoretically. Since the thickness of BCB layer is limited by MD Anderson from the point of view of dielectric field strength, PFP5 wafers would be used as they are to bond to the silicon fluidic layer. In the meantime, the feedback from MD Anderson on the previous delivered chips were positive, even there were some voids within the chip. The leakage of the chemicals in the chip is a function of the applied pressure from the vent port. As long as the applied pressure is lower than the threshold pressure, no leakage occured. On the other hand, BCB refilling could happen during the bonding process, which hopefully reduces the step height.

BCB lithography with recipes in Table 3 showed good result without any bubbling issues in the Pre-stage 1 phase. Also, the alignment between BCB layer and the PFP5 patterns was within the machine's tolerance. However, wafer warpage caused difficulties during lithography with the PFP5 wafers often sticking to the mask. The mask had to be removed from the aligner almost each time after each wafer.

2.2. BCB Bonding of PFP5 Wafer and Silicon Fluidic Layer

The PFP5 wafers were found to be bowed by the stress measurement using the wafer-Laser mapping technique. The warpage is believed to be introduced during the CMOS process by X-Fab. The wafer warpage measurement showed PFP5 wafers bowed about 87um from the peak to the valley. The measurement was taken using the laser mapping technique. The laser measurement requires a flat surface and as such the backside of the wafers were used since they were flat. The front sides have step heights owing to the circuitry. However, the measurement could have some error because the back side of the wafer was not polished to typical prime silicon grade quality as polish marks could be observed.

BCB coating trials were carried out on 2 PFP5 wafers with goals of 12um and 14.5um layer thicknesses. They were then bonded to test-glass-wafers individually to verify the bond result. The bond result of both of test wafers showed the center of PFP5 wafer was not bonded to the glass layer. It is further evidence that points to the warpage of the PFP5 wafer. The bond result looked similar with no significant difference.

PFP5 wafers were then bonded to the silicon fluidic layer using the bond aligner. The alignment mark were located within each die. The PFP5 wafer was first loaded to the bond tool followed by the silicon fluidic layer with the channel and nozzle side facing the PFP5 wafer. The bond was done under vacuum at 250°C for 20minutes. No oxygen existed in the chamber to prevent from BCB oxidation. 6000 N of force was used to create a uniform contact. Figure 3 shows the bonding result of Version 3 device.

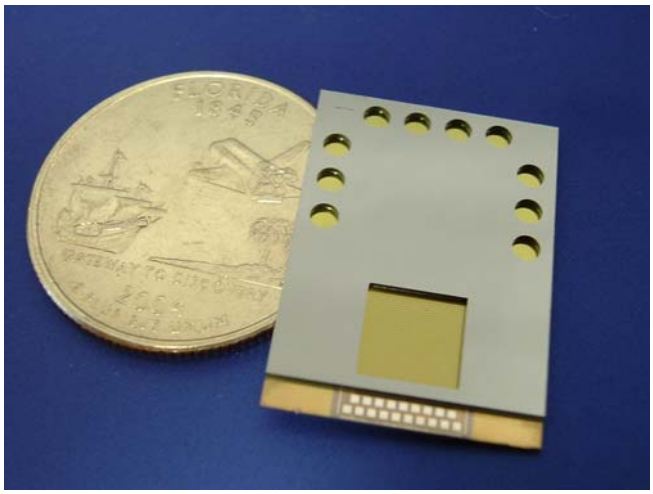

Figure 3. Photo of the Version 3 PFP5 microfluidic chip. It comprises the silicon fluidic layer and the PFP5 device and does not contain the top cover glass seal with reservoir ports. The picture shown here was after wafer dicing.

2.3 Triple Stack Wafer Bonding

Two anodic bonded wafers from Stage 2 were carried over to Stage 3 for triple-stack bonding. In the 3-stack, cover glass with drilled ports was anodically bonded to the silicon fluidic layer. Then the whole set of wafers was aligned to the PFP5 wafer on the bond tool in the bond aligner. The same BCB bonding recipe was used. After BCB bonding, the inspection showed a few artifacts within some vent ports. Figure 4 shows the zoomed-in picture. It was found only on triple stack wafers. The cause of the artifacts is not understood currently. The bonding result after dicing process can be seen in Figure 5.

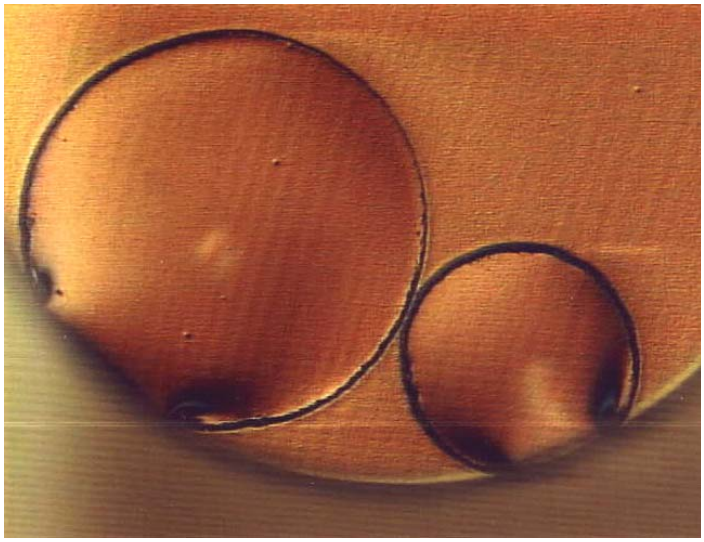

Figure 4. Artifacts showed up at the vent port region on some dies after BCB bonding in 3-stack wafer.

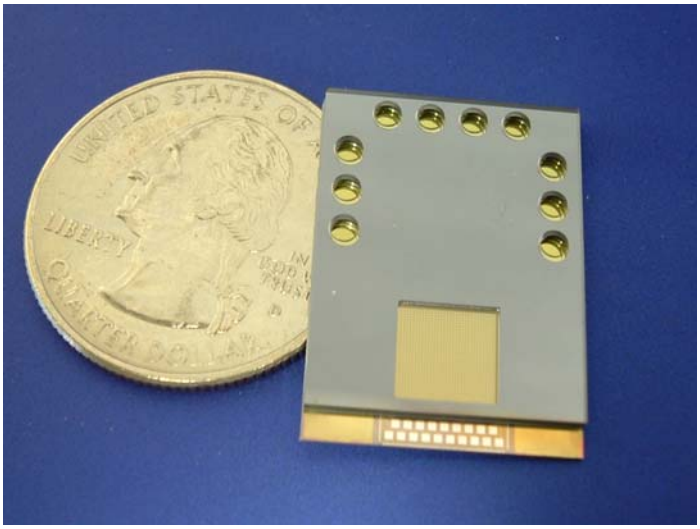

Figure 5. Photo of the Version 3 microfluidic chip. It comprises the cover glass, silicon fluidic layer and the PFP5 device. The picture shown here was after wafer dicing.

2.4 Version 3 Dicing Process

Two different dicing features were included in Stage 3. Four wafer sets were 2-stack, similar to Version 1 wafers. The remaining two sets of wafers were 3-stack, similar to Version 2 wafers. The Resin dicing blade was used to dice the silicon/PFP5 wafer and glass/silicon/PFP5

wafer due to the characteristics of the bonded wafers. The dicing program was generated to have one cut 2/3 way through the silicon wafer without touching the bottom metal electrodes. The dicing alignment between the scribing line and the saw blade in the 3-stack wafer was more difficult due to the alignment being carried out through the top cover glass and the focal plane being at a depth below the wafer stack surface. The result was comparable to the dicing result to V1 and V2 wafers. Figure 6 shows the cross-section view of sawed PFP5 device.

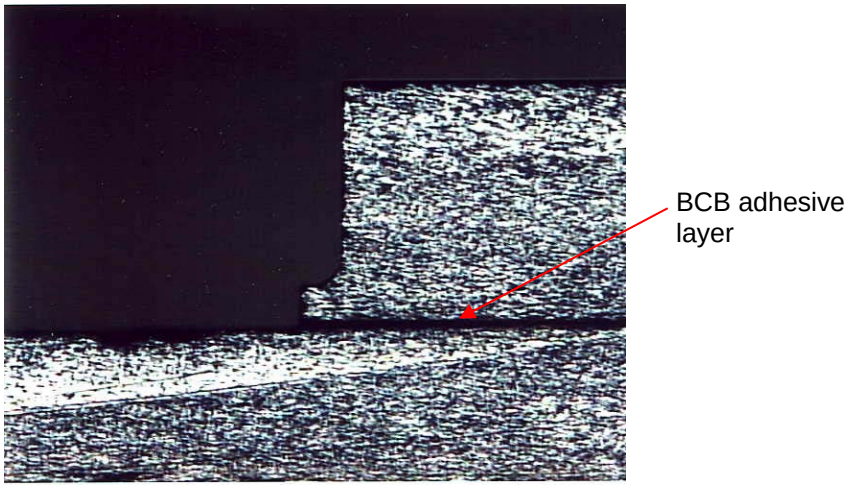

Figure 6. Cross-section view of PFP5 device.

The passivation film of PFP5 wafer peeled off at the corner of the sawed chip, as seen in Figure 7. It indicates the adhesion of the layer is marginal at the edges where exposed to the dicing blade.

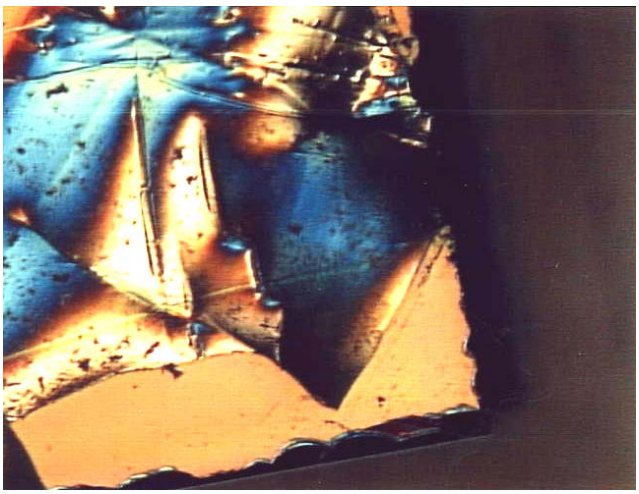

Figure 7. The top passivation layer of the PFP5 peeled away at the corner.

3. Further improvement

The peak-to-valley of PFP5 wafer is surprisingly high between the blanked regions and the active PFP5 circuit areas. The step height within the die was reduced as proposed to X-Fab. Due to the limited BCB thickness (12um is the maximum thickness MD Anderson can accept due to dielectric field strength requirements), complete planarization was not possible over the entire surface of the wafer. Front side grinding and polishing to reduce the step height was considered, but no grinding/polishing method suited this situation. It is because the layers at the blank region comprise several different materials, such as oxide, aluminum metal, silicon nitride, and poly-silicon. No grinding and polishing vendor could handle the work. For future improvement, the next revision of the ASIC would require extra masks to be applied to etch layers on the blank area away.

Unlike the glass electrode wafers used in the past, cracking was not observed in the PFP5 wafers during BCB bonding in both cases of 2-stack and 3-stack wafers. This is thought to be due to the higher material strength of Silicon as compared to pyrex as well as the better match of the thermal coefficient of expansion within the 3 stack layer.

4. Summary

Applied MEMS, Inc. has completed Stage 3 of the DEP project based on the contract as well as agreements with Dr. Jon Schwartz of MD Anderson during the program. As stated. Applied MEMS, Inc. completed 1) the development of BCB lithography process for PFP5 wafer with designated thickness required by MD Anderson, 2) the BCB bonding of 4 PFP5 wafer to the silicon fluidic layers without the cover glass individually, 3) the BCB bonding of 2 PFP5 wafer to anodically bonded silicon fluidic layer with the cover glass layer individually, 4) the sawing all six pairs of PFP5 Version 3 wafers.

The biggest challenge happened in the BCB planarization process of PFP5 wafer. As mentioned earlier, the step height of PFP5 wafer between the blank region and active PFP5 device is larger than 7um. It resulted in a recess within each circuitry region that needed to be filled with BCB for planarization relative to the blank regions. The 12um BCB thickness, was able to partially planarize the surface of the wafer.

However, the completed device could be used with a limited set of reagents. The hydrophobic surface property of BCB layer could help to prevent from chemical solution leaking out to adjacent channel.

Tasks 26, 27 Integrate and test final BioFlip

The final version of the device (PFP5) was laid out on a 25 x 19 mm die size that accommodated the 32 x 32 electrode array, switch-selection logic, and logic and supply contacts. The majority of the die area consists of blank space necessary to accommodate the microfluidics that were etched into a silicon substrate, and then bonded to the SOI wafer. Figure 1 is a schematic of the die layout, showing the spatial relationship of the active area to the fluid reservoirs and injectors.

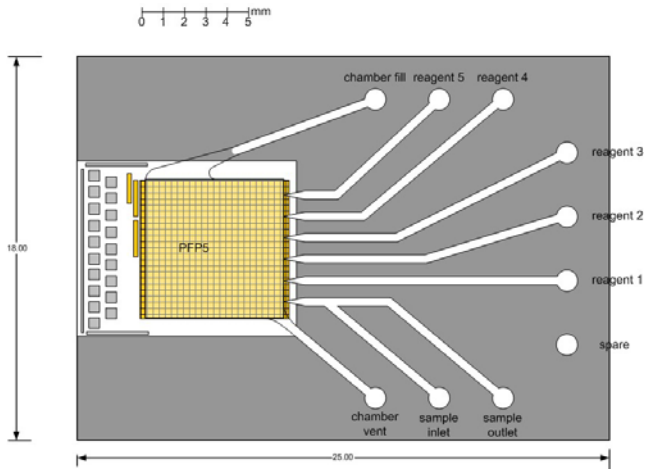

Figure 1: PPF5 die layout. The active area of the SOI chip occupies 25% of the die area, including the nineteen electrical contacts along the centre of the left edge. The balance of the die is occupied by the nine microfluidic ports and injectors.

The nine active microfluidics ports consist of a chamber fill port and chamber vent port, five reagent ports, and two ports that form a sample loop. This arrangement was chosen in order to facilitate a variety of chemical and biochemical assays. The sample loop enables different samples to be introduced to the PFP to perform the same assay on a series of samples without the need for changing the reagents.

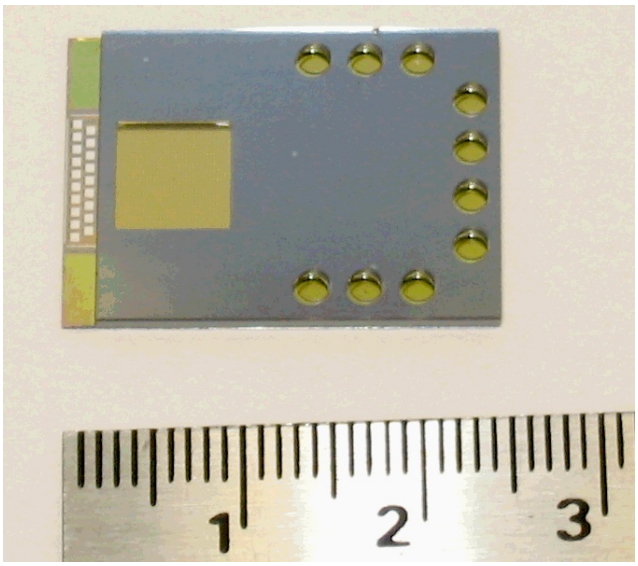

Figure 2: Individual PFP5 die. The diced 25 x 19 mm die is composed of a bonded stack of the SOI wafer, an etched silicon microfluidics layer and a top cap that seals the reaction chamber, but has openings for the fluidics ports.

The fifth version of the CMOS chip, as with the fourth version, has a 32 x 32 array of electrodes for droplet manipulation laid out on a 200 μm pitch, was fabricated to our design specifications by XFAB Semiconductor Foundries AG, (Erfurt, Germany) using a 100 V., silicon-on-insulator (SOI) process. In this design, each electrode is driven by an addressable switch that selects which of two opposite phases of an AC DEP excitation signal is applied to any combination of the 133 μm square droplet-actuating electrodes on the top metalisation layer. Addressing logic and the square wave oscillator that provides the high voltage AC DEP signal are incorporated on chip.

The external signals that must be supplied to the chip are the positive digital logic and high voltage rails (usually 40 V but up to 100 V if needed), a variable-frequency clock used to generate the AC excitation signals, and clocked digital “images” of the excitation state of the 32 x 32 array. Because the addressing and switching logic is included on chip, it interfaces directly with conventional electronic architectures and can be mounted in a conventional chip carrier to facilitate easy interfacing to control systems. The

assembled die, incorporating the silicon-etched fluidics layer and glass top layer is shown in Figure 2 next to a centimetre scale.

An electronic/fluidic interface adapter for the PFP5 was fabricated at M. D. Anderson in order to connect the die assembly to the external electronics power supply and logic board and the fluidics supply. The adapter permits the attachment of a 24-pin, 1-mm pitch ribbon cable to 19 miniature "pogo-pin" connectors aligned to the 19 electrical contacts on the PFP5 die. A custom formed gasket (the green area in Figure 3) provides a fluid-tight seal between externally-provided fluidics tubing and the fluidics ports on the PFP5 die. The electronic/fluidic interface adapter measures 44 x 30 x 5 mm.

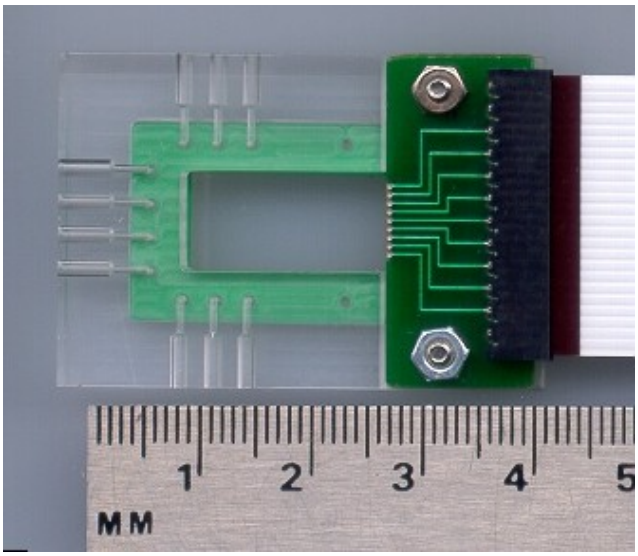

Figure 3: PFP5 electrical/fluidic interface adapter. A 24-pin, 1-mm pitch flex cable, at right, connects to a PC board that simultaneously secures 19 "pogo-pins" that provide electrical signals to the PFP. Ten fluid ports enter from the top, bottom, and left and connect through the green gasket to the fluidics ports on the PFP.

The complete PFP assembly is shown in Figure 4. The PFP5 die, at centre, is secured within the electronic/fluidic interface adapter and connected to the power supply/logic board at left and the fluidics supply lines on the right. The power supply/logic board derives power from a wall socket at provides all of the regulated voltages used by the PFP5. The nine fluid supply lines enter the electronic/fluidic interface adapter at right. Each chamber fill/vent, reagent, and sample line is regulated by a separate in-line valve.

The completed assembly contains all of the power supply, logic, and fluidic supply necessary to carry out the functions designed for the Programmable Fluidic Processor.

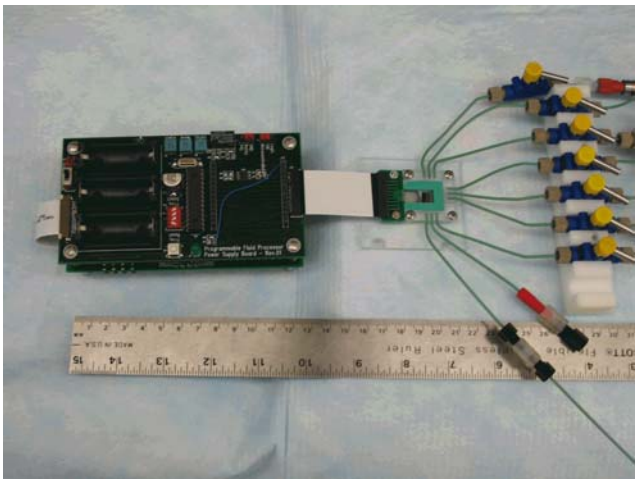
Figure 4: the complete PFP5 assembly mated to the power supply/control electronics and the fluidics supply lines.

Tasks 32, 39, 40. interface and controller, power supply/alarm system

Lynntech PFP Controller Board

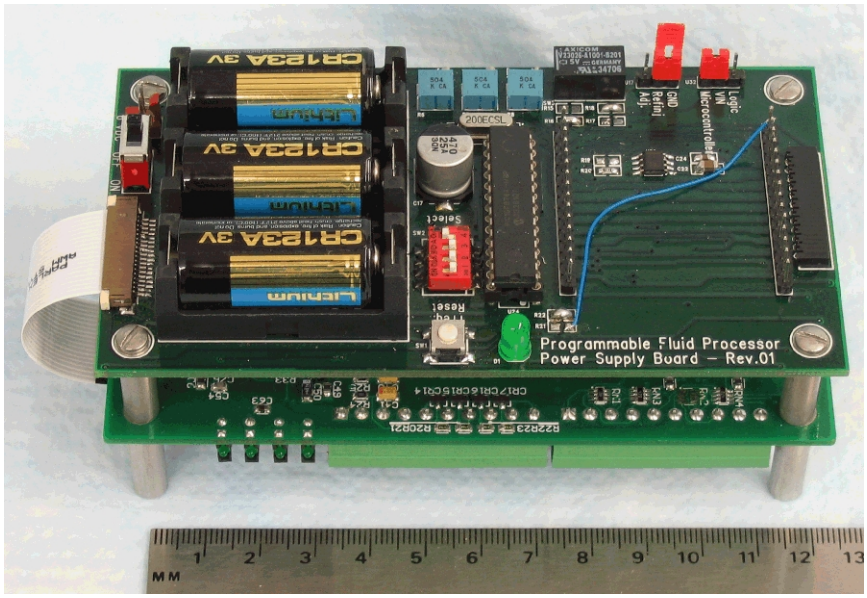

Figure 1

The PFP board can be used in two configurations (See Figure 1): PC-PFP and PDA-PFP. In PC-PFP configuration the board uses its own OPerated System (OPS). In this configuration the board is connected serially with a PC (HyperTerminal or other serial communication program) and is used to get information about the PFP controller board and like a low level manager and debugger. One command of the OPS is I17g. (See the Figure 2). After receiving this command the PFP controller board starts to receive PDA commands (PDA-PFP configuration). In this configuration the PFP controller board waits and executes commands from a PDA which is connected using its serial port.

When the board is powered the microcontroller controls the FPGA that stores in the SRAM memory two functions used to generate two external signals (sin and square). After all 4096 bytes are stored in the SRAM memory the board starts to do a self test routine. It actuates the rows and the columns of the PFP in a certain order. First, it actuates the rows from top to bottom and then will blink three times, then the columns are actuated from right to left.

In PC-PFP configuration, after the self test routine, the PFP control board will display the prompt. The board is ready to take OPS commands. An I17g command will make the PFP controller board to take commands from a PDA. Figure 3 presents the logic diagram of the system. The PFP board can be set it to start directly in PDA – PFP configuration. In this configuration the PFP board after it is powered up it is ready to take commands from the PDA.

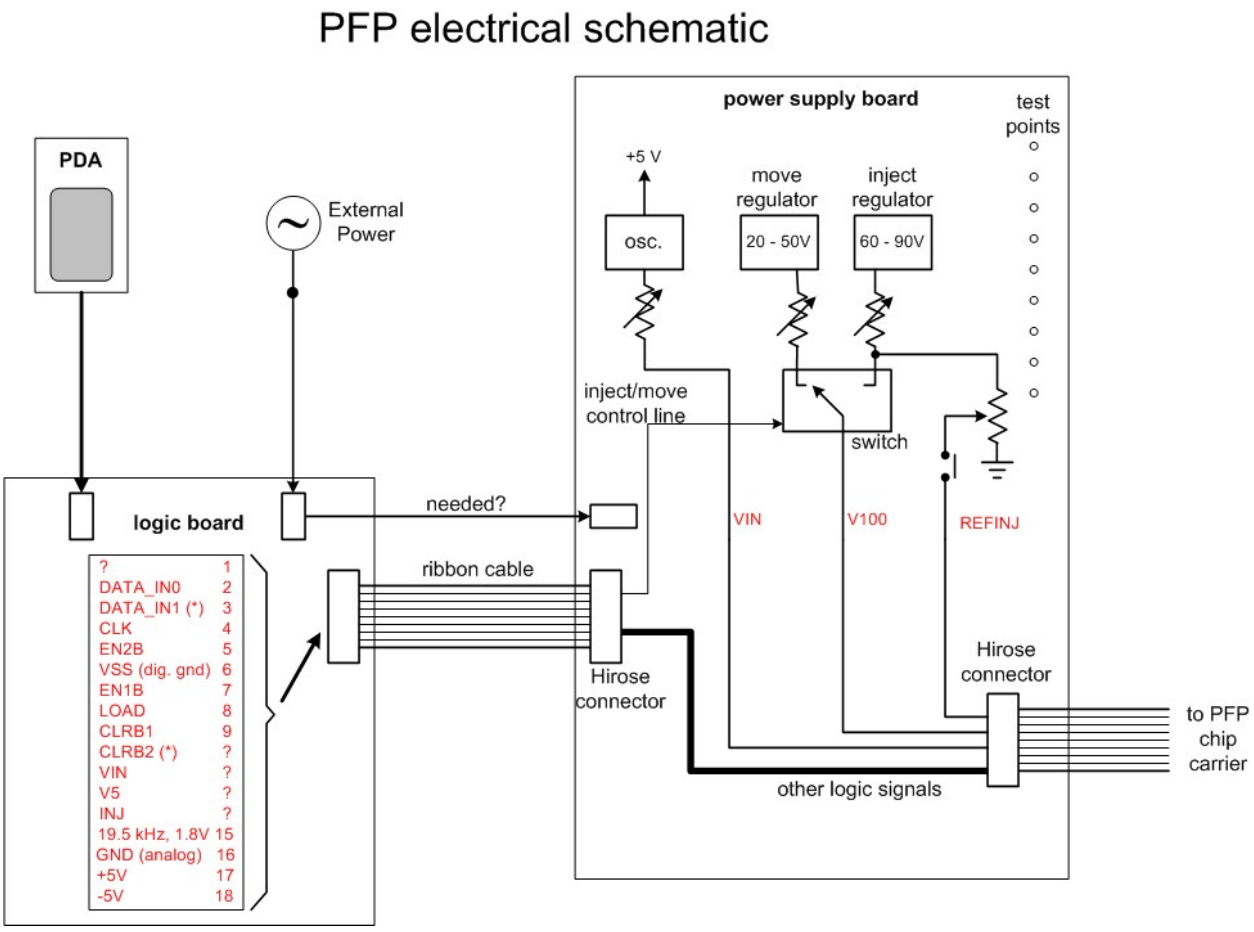
PFP electrical schematic
power supply board
test points
PDA
External Power
+5 V
move regulator
inject regulator
osc.
20 - 50V
60 - 90V
inject/move control line
switch
logic board
needed?
VIN
V100
REFINJ
ribbon cable
Hirose connector
Hirose connector
to PFP chip carrier
other logic signals
? 1
DATA_IN0 2
DATA_IN1 (*) 3
CLK 4
EN2B 5
VSS (dig. gnd) 6
EN1B 7
LOAD 8
CLRB1 9
CLRB2 (*) ?
VIN ?
V5 ?
INJ ?
19.5 kHz, 1.8V 15
GND (analog) 16
+5V 17
-5V 18

Figure 2

I17 command (CMD_PDA) - Receive and process commands from PDA (multitasking processes)

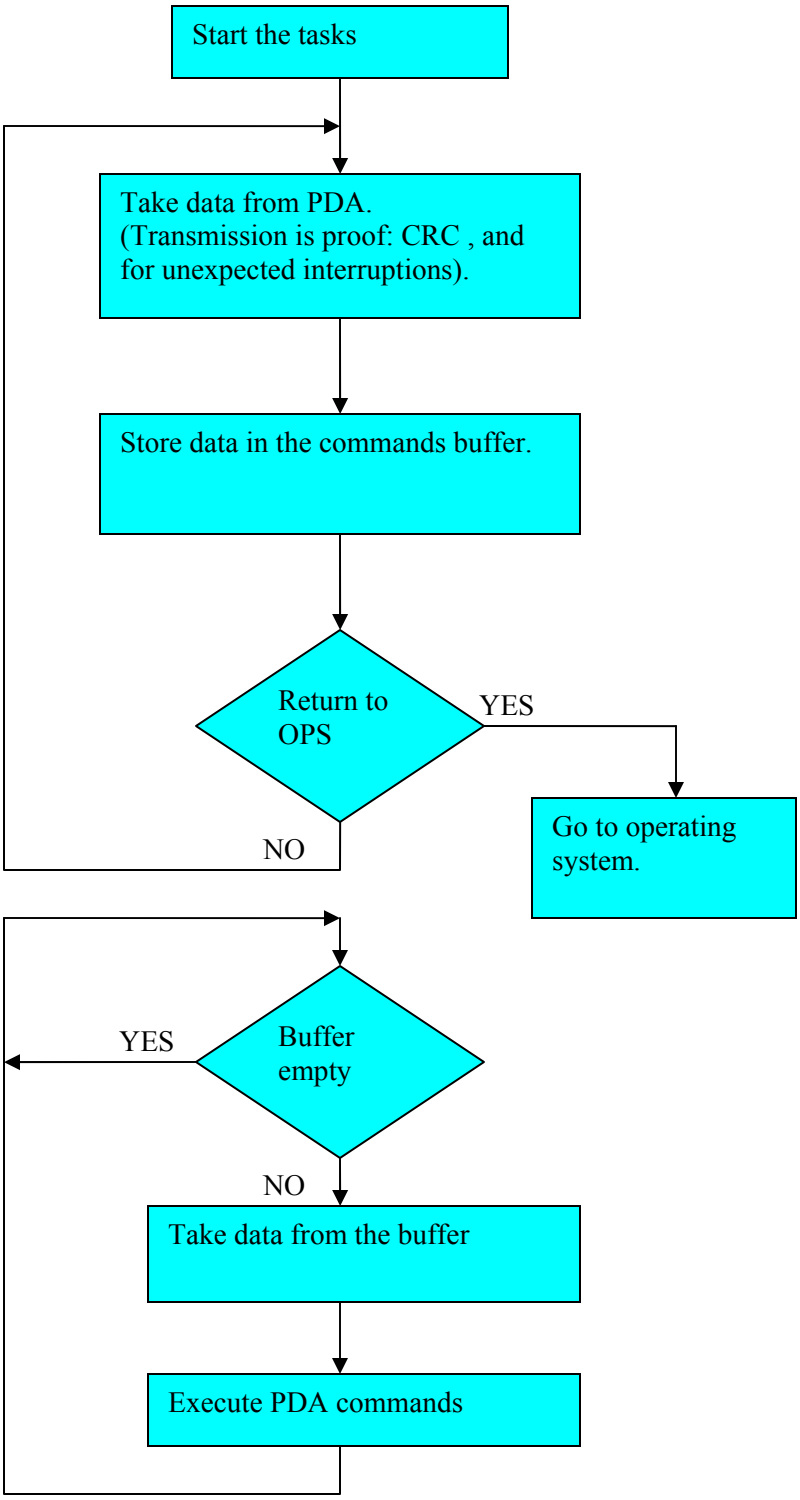

Figure 3

The Logic Diagram of the Overall System

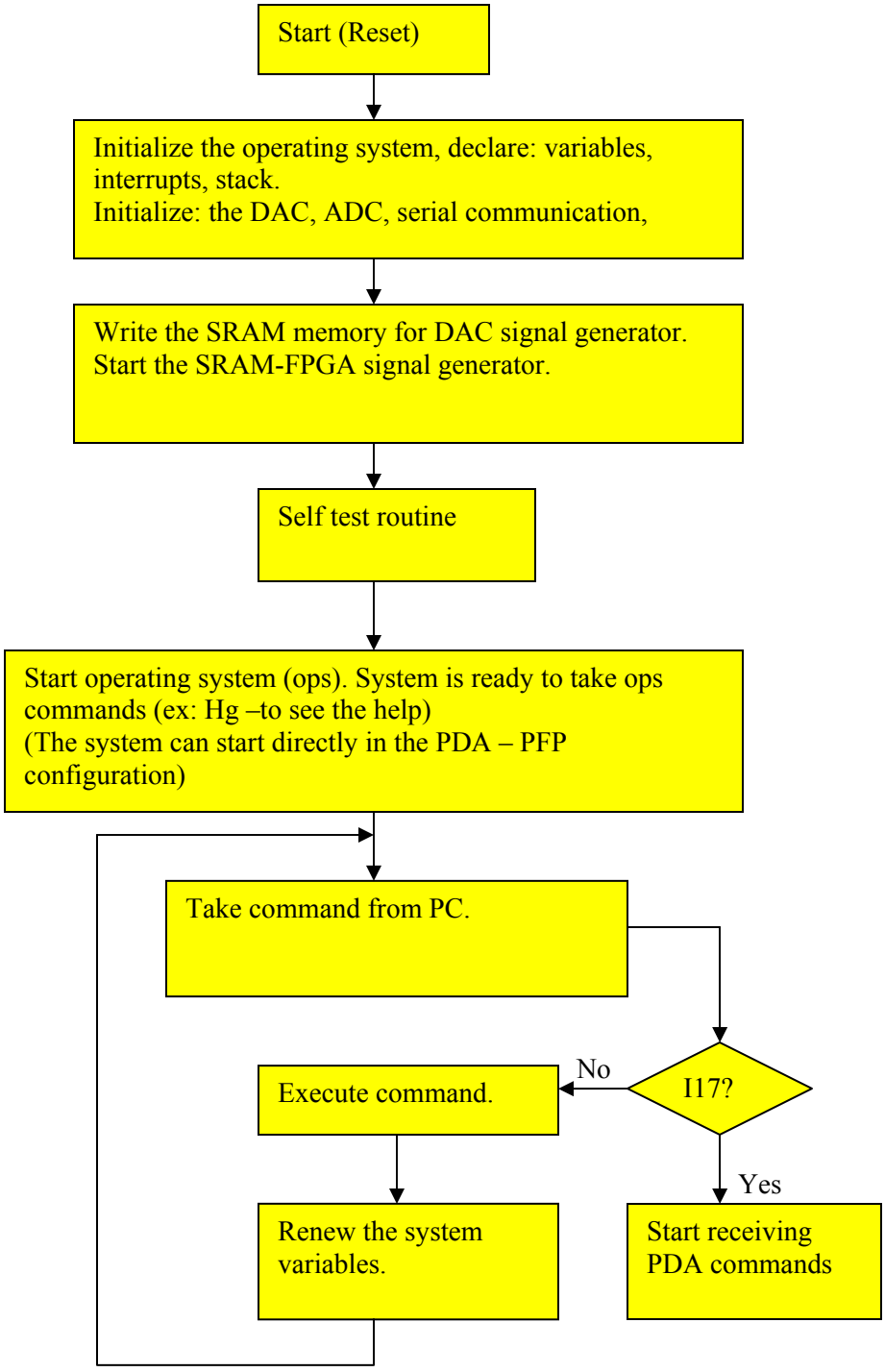

Figure 4

Task 40. System design refinements
A super-hydrophobic biocompatible MEMS surface

PROBLEM: stiction of droplets used in Biological Micro-Electro-Mechanical Systems (BioMEMS).

We use dielectric forces to resolve difficulties associated with electrophoretically-actuated channel-based systems[1,2 3]. Firstly, dielectric forces do not depend on the movement of charge, but on the polarisability of particles (cells, droplets) relative to their surroundings[4,5]. In this way we have used dielectrophoresis (DEP) to manipulate collections of cells whose interiors may be made dielectrically distinct from a low-conductivity suspending medium[6-8]. This also permits the manipulation of any type of liquid droplet within a dielectrically distinct immiscible carrier medium enabling the discreteness of droplet-based microchemistry. Secondly, dielectric forces are generated by spatially inhomogeneous electric fields. Hence, DEP requires no mechanical actuation. Thirdly, packaging analytes and reagents into discrete droplets, which also permit accurate quantification of reagents, can obviate dead volumes and continuity issues. Finally, packaging reagents and analytes in discrete droplets removes the need for channels in order to transport materials of interest. Droplets may in this way be manipulated arbitrarily and combined on a two-dimensional "reaction surface" composed of an array of individually energized electrodes. Surfaces in droplet-based micro-fluidic devices must facilitate the motion of micro-droplets across a micro-fluidic reaction space and permit droplet manipulations such as fusion, injection, division, and removal.

The large electric fields associated with DEP, however, can cause instant hydrolysis of droplets on the reaction surface. This results when electrical charge flows through an aqueous droplet between active electrodes used to generate the DEP force. To obviate this problem the reaction surface must be insulated so as to prevent the transfer of electrical charge into or through the droplets.

Additionally, the build-up of a counter-charge or the spatial concentration of electrolytes within droplets has the deleterious effect of causing droplets to adhere to the reaction surface rather than freely move in response to DEP forces. We have found experimentally that such a concentration of charge is cumulative. A result of this phenomenon is that droplets on an insufficiently hydrophobic surface become "sticky" over time requiring increases in voltage to manipulate. Figure 1) shows a water droplet adhered to the silanised surface of a previously energised electrode. The diameter of the droplet and the diameter of the surface contact area (the

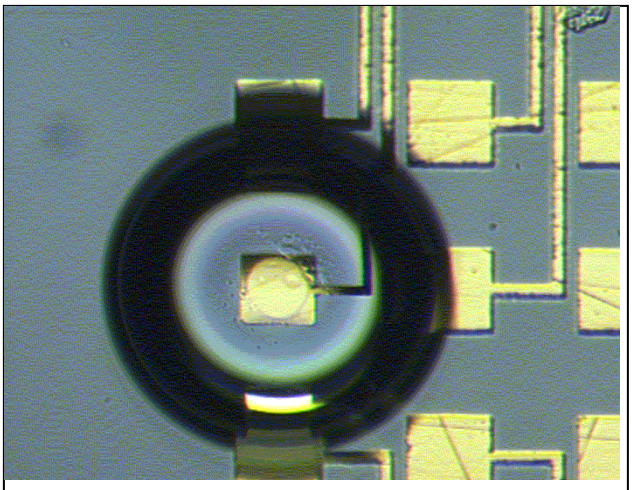

Figure 1) Water droplet (35 nl) on previously energized electrode. The surface was silanised.

bright circle centred on the electrode) permit a contact angle of 168.7° to be derived. It is further anticipated that this charge build-up can lead to unintended electrochemistry, one of the things that DEP manipulation ideally avoids. These effects have impelled us to develop reaction surface coatings that both insulate against electrical current and increase the hydrophobicity.

Additional desirable properties of surfaces used in micro-fluidics applications are: 1) that they are non-fluorescent in order to not interfere with fluorescence measurements of objects on the surface, 2) that they be non-reactive and not interfere with chemistry in the droplets.

SOLUTION: an electrically passivated, super-hydrophobic surface

The present surface is applied in two layers: 1) an electrically insulating passivation layer that is spun on and photo-patterned using conventional photo-lithographic techniques, and a super-hydrophobic layer that is essentially dip-coated and dried. Ideally, the functions of passivation and super-hydrophobicity will be combined in a single layer that can be photo-patterned to define precisely the areas to be coated.

Electrical passivation

The ceramic and metal that comprises the reaction surface of the programmable fluidic processor and similar devices that require insulated electrodes, may be electrically passivated using, for example, the epoxy-based photoresist SU-8 (Micro-Chem, Newton, MA). SU-8 is diluted to an appropriate consistency and spun onto the surface to be passivated. The specific area to be passivated is cross-linked in two stages: 1) by exposure to near UV (350-400 nm) radiation, and 2) by thermally driven epoxy cross linking.

The fully cross-linked photoresist provides a smooth, adherent and electrically insulating surface. We have used 1.5-2.0 μm thick SU-8 coatings over energized electrodes (100 V_{p-p}, 5kHz square wave) spaced 100 μm apart to prevent hydrolysis of aqueous droplets. Thicker coatings of up to 40 μm may be employed if necessary.

Super-hydrophobicity

Very low energy surfaces are produced by roughening a smooth surface. The roughened features on a super-hydrophobic surface are on the scale of 10s of nanometers to a few micrometers. The principle consists of using the roughened features to minimize the contact area between the surface and a sessile droplet[9]. Development of super-hydrophobic theory has encompassed understanding low surface energies and surface tension[10], high contact angles[11,12] and low sliding angles [13] for droplets. Surfaces may be roughened either by etching the native surface or by adding a "granular" coating to the native surface.

The granular, super-hydrophobic surface was composed of FluoroPel PFC M1604V (Cytonix Corp., Beltsville, MD), a proprietary colloid resin mixture of vinyl particles (4-8 µm across) suspended in a perfluoro carrier medium. The FluoroPel was applied over the SU-8 passivation layer and allowed to dry for a couple of hours. The substrate with the SU-8/FluoroPel surface was heated to harden and bond the two layers together. Non-polar suspending media such as liquid hydrocarbons or fluoropolymers wet the roughened surface composed of non-polar particles. Polar fluids such as aqueous droplets will not wet the rough, non-polar surface, but will instead tend to float over the non-polar suspending fluid that wets the spaces between the particles. The particles may be of different sizes as indicated above, but since the DEP force falls off geometrically with distance from an electrode edge, practical particle sizes are limited to a few micrometers. Figure 2) shows a 20 nl droplet of Phosphate Buffered Saline (PBS) over an electrode energised by a 52 V_{p-p}, 10 kHz square wave. Notice in comparison with Fig. 1) that there is no contact circle, indicating a surface contact angle of 180°. Due to the buoyancy provided by the suspending medium (specific density = 1.04) the droplet left the surface and floated away when the electrode was de-energised.

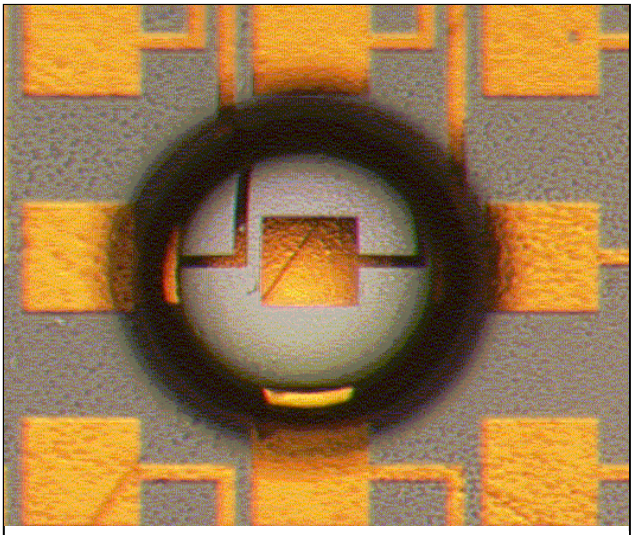

Figure 2 PBS droplet (20 nl) on an energised electrode (52 V_{p-p}, 10 kHz square wave). The deduced surface contact angle is 180°. The granular appearance of the surface is due to the 4-8 µm vinyl particles in the super-hydrophobic coating.

Minimising the contact area between a surface and a sessile droplet minimises the surface energy and hence, the stiction associated with attempting to move the droplet. In the present case where high electric field gradients in close proximity to the droplet are used as the motive force, minimising the surface contact area also tends to minimise charge transfer into and through the droplet. This enables droplet motion at a constant rate at a given applied voltage.

Figure 1) illustrates the increased rate of droplet motion on a super-hydrophobic, as opposed to a merely silanised, surface. Along the ordinate, average droplet velocities between energised electrodes are normalised (divided) by the droplet diameter, explicitly relating velocity to the Stokes

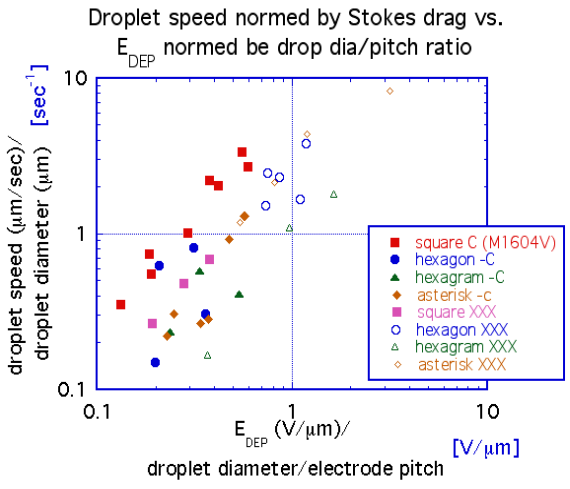

Figure 1) Speed of hydrocarbon-suspended aqueous droplets normalised by their diameter vs. applied inter-electrode electric field scaled by the normalised droplet diameter. Droplets moving across a super-hydrophobic surface are shown as ■.

drag through the viscous hydrocarbon suspending fluid.
Along the abscissa, the E-field is normalised by scaling it to the normalised droplet diameter, explicitly relating the size of the droplet relative to the pitch of the electrode array to the E-field. This also takes into account the distortion of the E-field by the change in permittivity at the droplet/suspending-medium interface. Note that for any given E-field, the normalised droplet velocity is higher on the super-hydrophobic surface (■).
Figure 2) graphs the same normalised droplet velocity data from Fig. 1) on a linear-linear scale. Linear curve fits are applied to droplet velocities on the super-hydrophobic surface (■) and to the other droplets which were moved across smooth, but silanised surfaces. These graphs highlight that not only does a super-hydrophobic surface yield higher velocities for a droplet of given size on an electrode array of a given pitch for a given applied electrical field (Fig. 1)), but that the reduced surface drag as shown by the higher slope of the fitted line yields a higher acceleration as well.

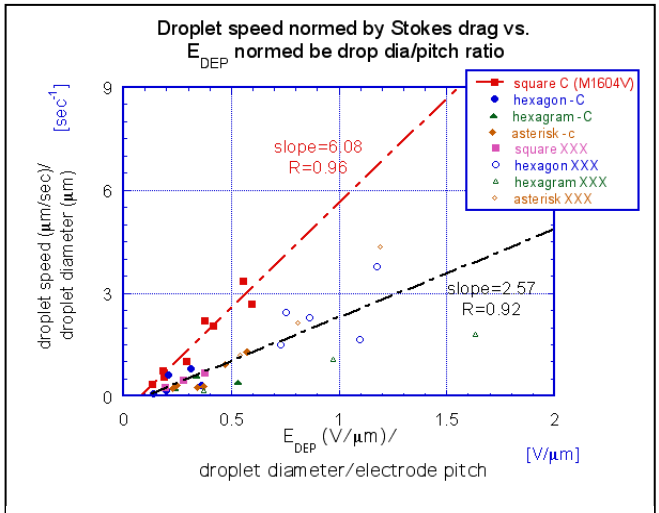

Figure 2) Normalised droplet velocity data from Fig. 1) plotted on a linear-linear scale. Linear curve fits are applied to droplet velocities on the super-hydrophobic surface (■) and to the other data.

Task 66. Simulate improved injector designs

On Liquid Disintegration

Modeling, Common Practice, and Control via Dielectrophoresis

Jun Zeng and Tom Korsmeyer
Coventor, Inc.

September 3, 2003

Introduction

Liquid disintegration includes the process of formation of droplets, or separating a liquid stream into discrete droplets; and the process of droplet fission, or dividing one droplet into smaller ones. Both processes share the same fundamental physics: from the energy perspective, both processes are nothing but energy transfer between surface potential and energy of other forms (thermal, electrical, kinetic, etc.). When the integrated surface area is increased, energy of other forms is required to be translated into surface potential to make up the difference; when the integrated surface area is reduced, the difference in surface potential is released.

Droplets are the most common carriers for chemicals in biomedical laboratories. Therefore it is not surprising that there has been growing attention in the biochip research community to the study of droplet manipulation via various means. Much of the research literature focuses on methods and results, and any discussion of the intrinsic physics is brief. In this report, the existing liquid disintegration methods are summarized, and the underlying physics are reviewed and discussed in a systematic fashion. The roles of both dielectrophoresis (DEP) and electro-wetting (EWOD) are discussed.

The report is composed of six sections, starting with a brief historical review covering the history of the discovery of the physics of liquid disintegration, progress of modeling methods, and device technology advances. Next is a short section discussing the relevance of liquid disintegration to biochip research. Following that is a summary of modeling approaches for the liquid disintegration process. These first three sections are intended to offer a global view of liquid disintegration: from history to state-of-art, from physics to applications, and from analysis to experiments.

In Section 4, our findings of device physics in the liquid disintegration process via detailed simulation are presented. This knowledge of the liquid disintegration process gained through detailed simulations lays the foundation for the next two sections.

Section 5 reports on the progress of our on-going effort to create a high-fidelity, highly portable, reduced-order model for the liquid disintegration process. The key point in discriminating modeling approaches: the recognition of the inherent directional dependency of the liquid disintegration process is fruit of the work described in section 4.

Section 6 concludes this report by proposing a new hybrid liquid disintegration method: continuous jetting + DEP gating. This method can fulfill the requirement for a liquid disintegration component in the Programmable-Fluid-Processor (PFP): a DEP controlled liquid disintegration process requiring only low voltage. Computational prototyping of this method has been carried out and indicates the feasibility of this method.

1 A Brief Historical Review

Liquid disintegration is a phenomenon ubiquitous in daily life. From the very beginning, man observed that a falling water stream turns into a series of disconnected droplets. However, it was not until the nineteenth century that the underlying physical mechanism, the role of the surface tension, was discovered and multiphase flow hydrodynamics, the science that deals with droplets and bubbles, was born. As one of the youngest areas of fluid mechanics, a science with thousands of years of heritage recording man's earliest attempts to interpret nature, multiphase flow hydrodynamics has been enriched quite rapidly over the years, partially owing to man's everlasting curiosity, partially owing to its root in fluid mechanics, where many methods were mature and ready to be borrowed. Multiphase flow hydrodynamics is the scientific basis of this report.

It is commonly recognized that the first systematic scientific study of liquid disintegration was reported by Savart (1833) [1]. He investigated the decay of liquid jets and observed small-amplitude undulations growing on a jet of water. These undulations later grow large enough to break the jet into a stream of droplets. Savart's research showed that breakup is an intrinsic property of the liquid motion, and the instability of the jet originates from small-amplitude perturbations applied to the jet at the opening of the nozzle.

Plateau (1849) [2] was the first to recognize the role of surface tension in droplet formation. He showed that the perturbations of long wavelength reduce the surface area and are thus favored by surface tension.

Rayleigh (1879) [3] [4] noticed the surface tension has to work against inertia and he was the first one to carry out the linear stability analysis for the liquid disintegration process. This analysis leads to the conclusion that the most dangerous wavelength is $\lambda \approx 9r$, where r is the jet radius. This conclusion, as well as the analytical method, was so successful that this phenomenon was named after him: Rayleigh instability. Since then, linear stability has been broadly applied to droplet formation analysis, most noticeably in work done by Tomotika (1935) [5], who accounted for the effect of ambient fluid, and Keller, Rubinow and Tu (1973) [6], who examined the growth of a progressive wave.

It should be emphasized that, strictly speaking, the much-developed linear stability analysis is applicable only to the small signal problem. However, historically the conclusions derived from linear stability analysis have found much broader application, partially due to the unavailability of non-linear, computational dynamics tools until recently.

Large disturbance problems, where spatial derivatives have to be accounted for, are beyond the reach of conventional analytical means. A high-fidelity predictive analysis of large disturbance problems was not possible until recent years when powerful computers and effective numerical methods made full-dimensional, non-linear Navier-Stokes solutions available. In the mean time, a compromise (between the lack of full-dimensional solution and the need to account for the spatial effects) was established on the basis of lubrication theory or the shallow-water approximation, which assumes that the dynamic variation in one particular direction is dominant. The resulting simplified Navier-Stokes equations contain spatial

[1] Savart, F., 1833, Annal. Chim., Vol. 53, 337,
[2] Plateu, J., 1849, Acad. Sci. Bruxelles Mem. Vol. 23, 5
[3] Rayleigh, Lord, J. W. S., 1879, Proc. London Math. Soc., Vol. 10, 4
[4] Rayleigh, Lord, J. W. S., 1879, Proc. R. Soc. London, Ser. A, Vol. 29, 94
[5] Tomotika, S., 1935, Proc. R. Soc. London, Ser. A, Vol. 150, 322
[6] Keller, J. B., Rubinow, S. I. & Tu, Y. O., 1973, Phys. Fluids, Vol. 16, 2052

derivative terms yet do not demand high computational power. [7] Lee (1974) [8] was the first to publish this approach and arrived at a one-dimensional dynamic equation. His model was limited to inviscid fluids. Eggers and Dupont (1994) [9] included the viscosity term, thus expanding this approach to deal with more generic situations.

Even today, with powerful computational means and full-dimensional simulation analysis as standard practice in device design and analysis, this simplified one-dimensional approach still holds strong practical interest to aid system level design. This approach has great potential to offer a high fidelity, highly-portable, low-computational-cost, reduced-order model for a generic liquid disintegration component, as is discussed in Section 5.

The shallow water assumption fails when the spatial variation along the jet radial direction also plays an important role. In this case, non-linear dynamic simulation of liquid disintegration calls for numerical methods that can solve the full-dimensional multi-phase flow Navier-Stokes equations (therefore more general problems can be dealt with). One of the earliest approaches would be Birkhoff (1954) [10], where it is assumed the liquid is inviscid and irrotational and thus a boundary integral method was used. Several methods that can deal with more general problems were originated at Los Alamos Scientific Laboratory: the marker-and-cell method (Harlow and Welch, 1965) [11], the volume-of-fluid method (Hirt and Nichols, 1981) [12], and the arbitrary-laglangian-eulerian method (Hirt, Cook and Butler, 1970) [13]. The one-fluid concept that originated at Los Alamos has inspired a class of hybrid methods, for instance, front tracking (Unverdi and Tryggvason, 1992) [14] [15]. The most recent addition to the collection of methods capable of simulating finite-Reynolds-number multiphase flows is the lattice boltzman method (for a detailed discussion, see Shan and Chen 1993 [16]) but the correctness, accuracy, and efficiency remain unproven. Since many of the liquid disintegration problems encountered in real life do not lend themselves to the simplifications of the analytical approaches, and since these numerical approaches can be fast and accurate on today's computing equipment, the latter are now widely used in scientific research and product design.

As in other fields, the point of understanding this theory and modeling practice is to make use of it in the design of real devices and systems. From the very beginning, droplet formation technology has been used in printing [17] [18]. In 1951, Elmqvist (Seimens) patented the first Rayleigh break-up inkjet device. This invention led to the introduction of the Mingograph, ink-jet chart recorders for analog voltage signals. In 1964, Sweet (Stanford University) patented a continuous ink-jet process, which led to the A. B. Dick VideoJet, Mead DIJIT products, and IBM's computer printers (e.g., IBM 4640 ink-jet printer, 1976). In 1972, Zoltan, Kyser and Sears patented a drop-on-demand ink-jet process. Their inventions were used in the Seimens PT-80 serial-character printer (1977) and by Silonics (1978). In these printers, on the application of voltage pulses, ink drops are ejected by a pressure wave created by the mechanical motion of the piezoelectric ceramic. In 1979, Endo and Hara (Canon) invented a vapor-bubble driven drop-on-

[7] This approach has made significant contribution in guiding ink-jet design during 1970s. It was not surprising that the early-year landmark papers on this topic were usually found at IBM Journal of Research and Development.
[8] Lee, H. C., 1974, IBM J. Res. Dev., Vol. 18, 364
[9] Eggers, J. & Dupont, T. F., 1994, J. Fluid Mech., Vol. 262, 205
[10] Birkhoff, G., 1954, Rep. LA-1862, Rep. LA-1927, Los Alamos Scientific Laboratory
[11] Harlow, F. H. & Welch, J. E., 1966, Phys. Fluid, 9, 842
[12] Hirt, C. W. and Nichols, B. D., 1981, J. Comput. Phys., 39, 201
[13] Hirt, C. W., Cook, J. L., & Butler, T. D., 1970, J. Comput. Phys., 5, 103
[14] Unverdi, S. O. & Tryggvason, G. 1992, Physica D, 60, 70
[15] Unverdi, S. O. and Tryggvason, G., 1992, J. Comput. Phys., 100, 25
[16] Shan, X. W. & Chen, H. D., 1993, Phys. Rev. E, 47, 1815
[17] Le, H. P., 1998, J. Imaging Sci. & Tech., Vol. 42, No. 1
[18] Moore, John, 1988, Output Hardcopy Devices, (Boston: Academic Press, Inc., 1988) p. 209

demand ink-jet, the bubble jet. During the same time period, Hewlett-Packard independently developed its similar ink-jet technology. In 1984, Hewlett-Packard commercialized the ThinkJet printer, the first successful low-cost ink-jet printer based on the bubble jet principle. The non-contact printing industry, whose core strength is based on droplet disintegration methods, has continuously been the primary driving force for developing better and cheaper droplet formation technology.

The application of liquid disintegration is also found in the biotechnology sector. Droplets are the most natural vehicles to carry biochemical agents. For instance the micro-array, (parallel-processed gene identification technology) that is on its way to being integrated into common biomedical practice, demands a means to generate minute amounts of chemical compounds in each of the many disassociated wells. Ink-jet technology is considered one of the promising methods to deliver chemicals for each well (Okamoto, Suzuki and Yamamoto, 2000 [19]). Other liquid disintegration methods for micro-array technology include pin-based printing[20]. A pin with liquid sample strikes and makes a physical contact onto a substrate, then pulls back. Upon the pin's retreat, the cohesive force between the substrate and the liquid breaks the liquid body in two, leaving a part on the substrate.

2 Liquid Disintegration on Biochips

Biochip, or lab-on-a-chip, is the miniaturization and integration of a biochemical lab onto a (roughly) 1cm chip. At any scale, liquid disintegration is one of the most commonly encountered procedures in a biochemical lab. For instance, in sample preparation the following is commonly seen: a pipette is dipped in a container and a small amount of sample is sipped into the pipette; then the pipette is moved into a test tube and the liquid sample is released. Through this process, the liquid body in the container is disintegrated into two parts: that remaining in the container and the sample in the test tube. The miniaturization of this process is not an easy task. In the macro world, the gravitational force helps the liquid disintegration process (viz. droplets dipping off from a nearly-closed faucet). But in the miniaturized world, the gravitational force is negligible compared to the surface tension force, so the latter can easily prevent a droplet from leaving an orifice. The orifice is said to be "gated" by the surface tension force.

To make the liquid disintegration work in a miniaturized environment, a force must be created with magnitude comparable to the surface tension force. For instance, dielectrophoresis (DEP) can create a force density inside a liquid body, and utilizing DEP to break up droplets has been investigated in a handful groups, such as those of, Peter Gascoyne of M. D. Anderson Cancer Center [21], and Thomas Jones of University of Rochester [22].

Another approach involves creating a tangential force field on the interface, in other words, modifying the surface tension force to trigger an interfacial instability (Marangoni effect). Current approaches to create an interfacial force density (more precisely, the gradient of an interfacial force density) are through a temperature field (thermo-capillary, for instance, Troian et al 2001 [23]), an electric field (electro-capillary, or EWOD, for instance, Kim et al 2003 [24]), or a distribution of surfactant.

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[19] Tadashi Okamoto, Tomohiro Suzuki, and Nobuko Yamamoto, 2000, Nature Biotechnology, Vol. 18, 438

[20] Zeng, J., Deshpande, M., Kan, H-C., Gilbert, J., 2001, Proc. Micro Total Analysis Systems 2001, Monterey, CA

[21] Vykoukal, J., Schwartz, J., Becker, F. and Gascoyne, P. 2001, Proc. Micro Total Analysis Systems 2001, Monterey, CA

[22] Ahmed R., Hsu D., Bailey C., and Jones T. B., First International Conference on Microchannels and Minichannels, April 24-25, 2003, Rochester, New York, USA

[23] Darhuber, A. A., Davis, J. M., Reisner, W. W. & Troian, S. M., 2001, Proc. Micro Total Analysis Systems 2001, Monterey, CA

[24] Cho S. K., Moon H., and Kim C-J, 2003, Journal of Microelectromechanical Systems, Vol. 12, No. 1, 70

3 Modeling Approaches for Liquid Disintegration

Modeling tools have always been an integral part of design practice, no matter whether the designer is running state-of-art simulation software or merely sketching ideas on the back of an envelope. There are two typical modeling approaches: detailed modeling and reduced-order modeling.

Detailed modeling approaches to model multi-phase flows, including the liquid disintegration process, were initiated in the 1950s [10]. The detailed simulation approaches have gradually matured over the years and now have been adopted as an integral component of common inkjet design practice. State-of-art multi-phase flow detailed simulation engines are now commercially available.

Detailed simulation approaches are based on first principles, that is, the conservation laws of mass, momentum and energy, with no or few additional assumptions. The physical domain is discretized into a set of elements or cells. The distribution of the field quantities (pressure, velocity, etc.) in each element is predefined. The conservation laws are enforced both in each element and in the entire physical domain, in the form of the field quantities in elements, and solved via numerical methods.

The detailed simulation approaches offer high-fidelity physical insights into device physics, owing to the characteristic that there are fewer no "artificial" assumptions involved in constructing a detailed simulation engine.

The detailed simulation approaches are highly portable. They do not utilize knowledge of particular device in their modeling of the physics. Rather, the information about a certain device and its operation is introduced into the simulations in the forms of geometric description, initial conditions, and boundary conditions. Unfortunately, the knowledge threshold required to master a detailed simulation engine is fairly high. The user bears the burden of making correct modeling assumptions and translating the constraints of a particular device into boundary conditions and initial conditions. To do this successfully demands a background not only in physics, but also in applied mathematics and numerical methods.

Also, the detailed simulation approaches are quite CPU-intensive. Even given state-of-art computational hardware, a detailed simulation for one specific design may take hours to days to accomplish. This cost of time can be unbearable at the initial design stage when many design options must be screened.

From user's perspective, it is either impossible or very difficult to increase or modify the capability of a detailed simulation engine. The user may not have access to the source code and the object code may not have hooks for linking dynamic library components. In any case, modification of the source code or writing linkable modules demands expert knowledge of physics and numerical methods.

System-level modeling approaches offer complementary capabilities. System-level modeling utilizes so-called reduced-order models to describe the dynamical properties of individual components. A reduced-order model usually has been derived with a specific component or device in mind. It may come from first principles with many simplifications based on the knowledge on this specific device. Or alternatively, it may come from a descriptive approach: a matrix that translates a set of input data into the corresponding output data that has been obtained by physical and/or numerical experiments.

System-level modeling approaches are easy to learn. The information required for users to input is very limited and usually descriptive. The principles of constructing system schematics are intuitive.

System-level modeling approaches run very fast, usually taking seconds to minutes. This enables rapid parametric studies that can narrow a design space efficiently.

It is not only possible but also encouraged for the user to increase the simulation capability under a system-level modeling environment. The simulation capability can grow by adding additional existing or novel, user-created, components to the system.

However, the reduced-order models are accurate only to a certain degree. They are applicable only to devices for which the assumptions made are valid. This also limits the reduced-order models' portability.

The following table summarizes the uniqueness of both modeling approaches. In design practice both detailed simulation approaches and reduced-order simulation approaches are expected to work hand in hand, for one makes up the other's shortcomings. A complete design environment should offer both detailed simulation and reduced-order modeling capabilities.

	Accuracy	**Portability**	**CPU Cost**	**User's Customization**
Detailed Simulation Approach	high	high	high	impossible or difficult
System Level Simulation	limited	limited	low	possible and encouraged

4 The Physics of Liquid Disintegration

As stated above, a detailed simulation engine is based on the conservation principles of mass, momentum and energy with which the Newtonian world complies. Therefore detailed simulation solutions are expected, and indeed do, present the same device behavior as one would observe in a laboratory. Importantly, this device behavior, created through detailed simulations, offers much more field data than experiments. Consequently, detailed simulation methods are broadly used to unveil device physics.

With financial support from DARPA through M. D. Anderson Cancer Center, we have developed and validated detailed simulation software that enables modeling of the liquid disintegration process energized by electrohydrodynamics (Zeng, Deshpande and Gilbert 2002 [25]). This detailed simulation engine has been successfully commercialized (for instance, Zeng, Sobek, and Korsmeyer 2003 [26]). In this section the newly constructed detailed simulation engine is deployed to analyze common practices of the liquid disintegration process, unveil the underlying mechanism that breaks a liquid body, and derive a "rule-of-thumb" for the design of liquid disintegration process.

As we briefly mentioned in Section 1, two typical droplet disintegration methods dominate industrial applications, namely, continuous jetting and drop-on-demand (DOD). In recent years, a third class of liquid disintegration methods that utilize Marangoni effect has gained significant presence in biochip research.

4.1 Continuous jetting

[25] Zeng, J., Deshpande, M. and Gilbert, J. R., 2002, "On Modeling of Dielectrophoretic-Driven Programmable Fluid Processor", report to P. R. G. Gascoyne of M. D. Anderson Cancer Center

[26] Zeng, J., Sobek, D. and Korsmeyer, F. T., 2003, Transducers '03, Boston MA

Figure 1 shows a time sequence of the continuous jetting process. A liquid column shoots out of the nozzle. The contour of the liquid column (jet) becomes wavy and at one point (the potential pinch-off

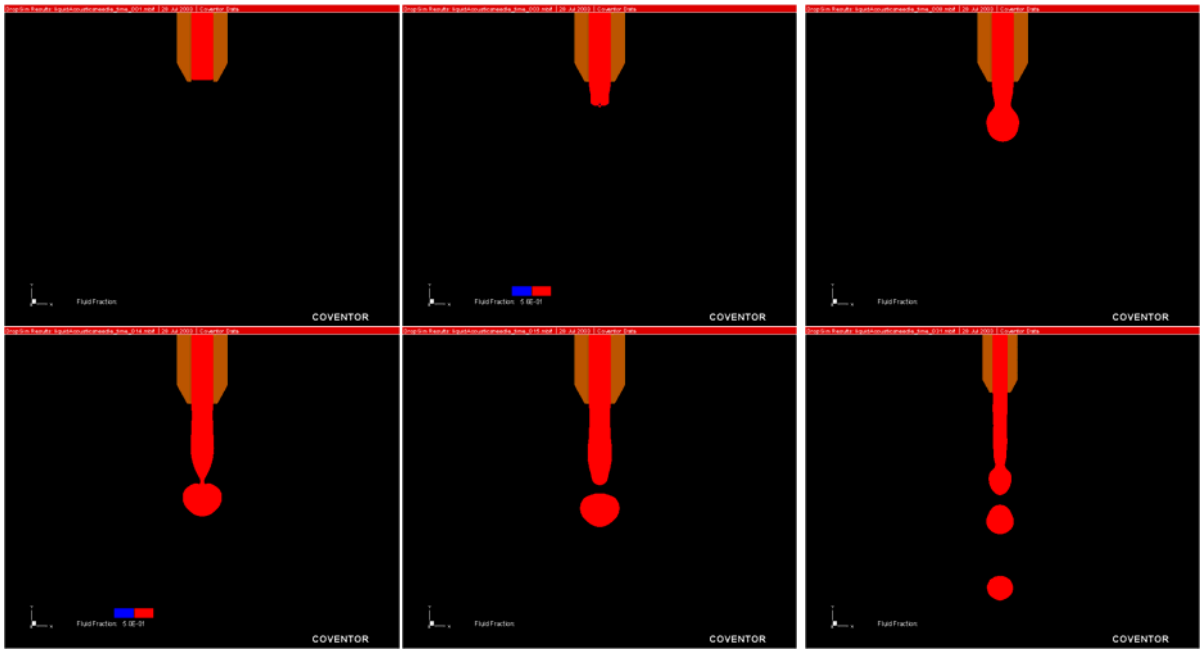

Figure 1: Liquid disintegration in the Continuous Jetting mode (simulation).

point, Figure 2) the jet cross-section narrows down. Should pinch-off occur, the cross-section area converges to a point. At this point, the local curvature becomes zero, which delivers an excessive liquid pressure to separate the liquid column and release a droplet.

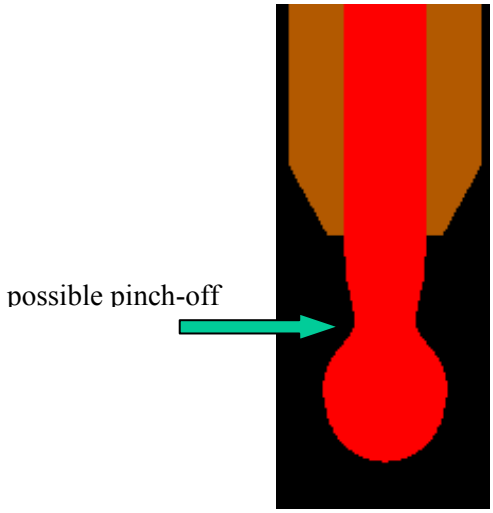

Figure 2: Droplet pinch-off.

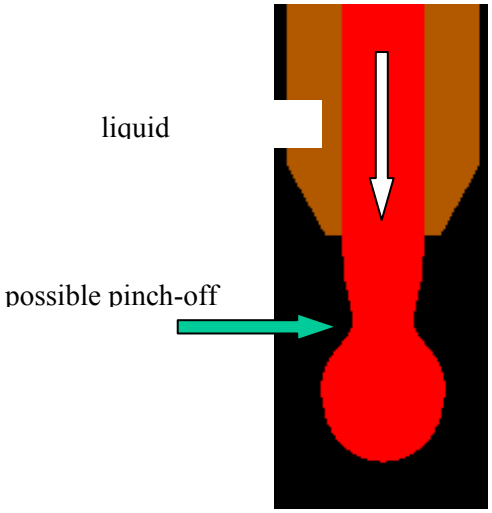

Figure 3: How Continuous jetting works

One can see that the key to liquid disintegration by this method is the emergence of the potential pinch-off point and the acceleration of the shrinkage of the jet cross-section at this point.

According to Plateau (1849) [2], an axisymmetric deformation of a jet reduces its surface area. Therefore the jet has less surface potential [27]. Consequently, a surface tension force prefers the "wavier" shape of the jet, i.e., the surface tension force should accelerate the shrinkage of the cross-section at the potential pinch-off point. Surface tension force in continuous jetting mode is a driving effect.

The continuous jetting mode does not demand a sophisticated actuating mechanism for the flow. Usually a simple pressure source in the chamber supplies either a constant pressure overhead or a constant liquid flow rate. The liquid inertia opposes the liquid motion over long distances; yet, it takes a certain distance

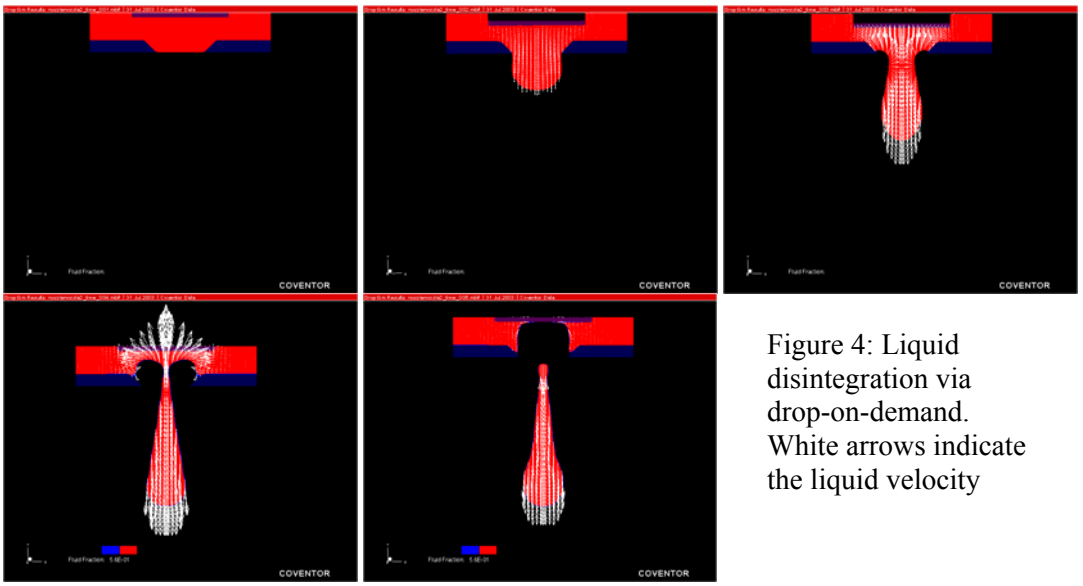

Figure 4: Liquid disintegration via drop-on-demand. White arrows indicate the liquid velocity

for the perturbations that are preferred by surface tension to grow and eventually break the jet. It was Rayleigh, 1879 [3] [4] who noticed that surface tension has to work against inertia to break the jet. The liquid inertia here is a counter effect to liquid disintegration.

4.2 Drop-on-demand

As stated in Section 4.1, the liquid inertia acts as the opposing effect in liquid disintegration in the continuous jetting method. On the other hand, a transient liquid flow could use liquid inertia to enhance jet breakup. Figure 4 shows a droplet formation process where a diaphragm delivers the actuation. The diaphragm first moves downwards then quickly retreats. When the diaphragm moves downwards, it pushes a liquid jet out of the nozzle. The liquid jet is accelerated downwards and has downward momentum (see the second image of Figure 4, the white arrows indicating the velocity vectors). When the diaphragm starts to retreat upwards, the liquid that is in the diaphragm's vicinity must move upwards (see the third image in Figure 5, the liquid in the reservoir has white arrows pointing upwards). However, the body of the liquid jet, due to its inertia, will continue to move downwards (the third and fourth images of Figure 5). Such a liquid momentum distribution pattern will drain the liquid mass from the potential pinch-off point (Figure 6) greatly accelerating the droplet pinch-off process.

[27] One can also arrive to this conclusion via an exercise of differential geometry.

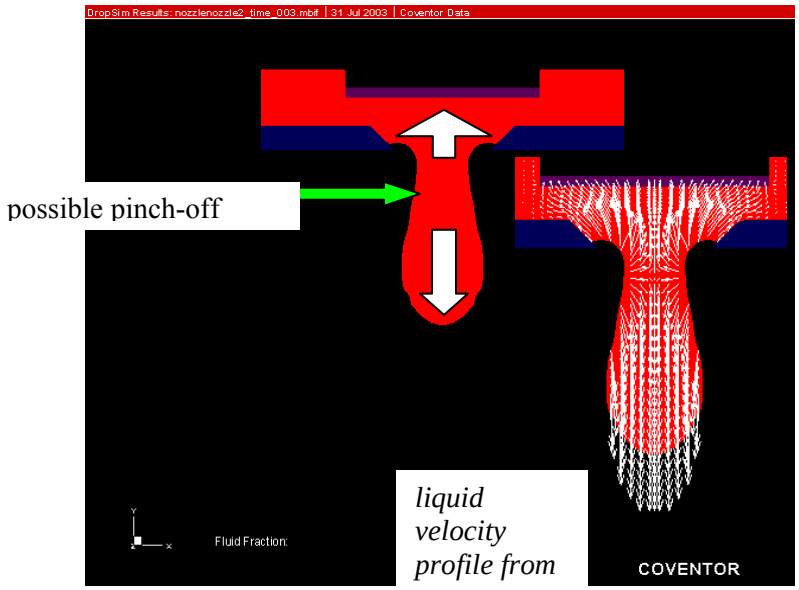

Figure 5: drop-on-demand. The white block arrows indicate the liquid momentum. Simulation result is pasted at side to show the liquid velocity

A cycle of diaphragm oscillation (moving downwards then retreating upwards to the original position) usually guarantees a discrete droplet shooting out of the nozzle. The liquid stays idle in the reservoir gated by the surface tension when the diaphragm is not actuated. Therefore, generation of an individual droplet can be precisely controlled by controlling the oscillation of the diaphragm; and furthermore, the terminal velocity and the size of the droplet can be altered by tuning the diaphragm oscillation duration and amplitude. The fact that almost all of the important design aspects of the droplet generation are under the designer's control warrants the process the name of "drop-on-demand".

However, the method demands a very sophisticated actuation mechanism. A large displacement of the liquid body is required to produce the liquid jet. Then a rapid directional switch of the actuation is required such that the droplet detachment occurs before the direction of the jet inertia is affected. Such an actuation mechanism in the microscopic environment is not easy to construct. Successful practices mostly fall into two categories: an oscillatory diaphragm or a nucleated vapor bubble.

4.3 The Marangoni effect

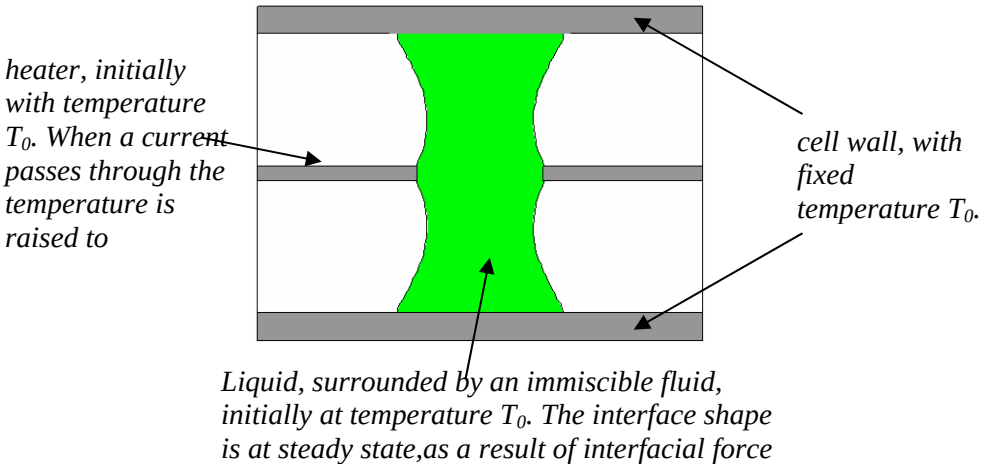

Figure 6: Liquid disintegration via creating a gradient of the interfacial tension: example – liquid breakup via thermo-capillarity.

As shown in previous sections, the success of liquid disintegration lies creating a mechanism to drain the liquid mass out of the potential pinch-off point such that the cross-section area at the pinch-off point shrinks and eventually becomes a point. Drop-on-demand satisfies that requirement by creating the directional disparity of the momentum.

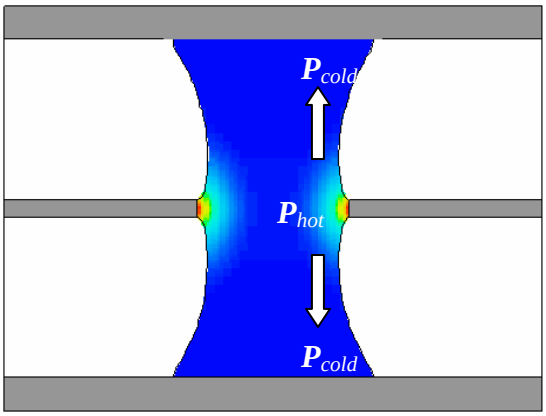

Figure 7: Liquid disintegration via thermo-capillarity. The high interfacial temperature at the middle of the liquid column reduces the local surface tension force. According to the Laplace equation, it results a high liquid pressure at high temperature surface and consequently induces a liquid flow (as shown in white block arrow). The liquid particle at center is dragged upwards or downwards, which effectively shrinks the cross-section of the liquid column at middle. When the cross-section area goes to zero, the liquid column is broken into two droplets.

Motion at the interface can also induce liquid flow in the bulk. Therefore, a pre-programmed flow pattern at the interface can induce the directional disparity of the flow in the liquid bulk to drain the liquid mass out of the potential pinch-off region. There has been a class of methods utilizing the Marangoni effect to achieve this that has gained significance in biochip research recently. The attractions of these methods are their ease-of-control (via electrostatic field or thermal field), no moving parts, and high-frequency response.

Traditionally, the Marangoni effect is that the presence of a temperature distribution on the interface modifies the surface tension force so that a non-zero gradient of the surface tension force is created The presence of the disparity of the surface tension will cause liquid motion at the interface. Such interfacial motion will in turn induce the liquid flow in the bulk due to liquid viscosity.[28] Here we use the term

[28] Adamson, A. W., "Physical Chemistry of Surfaces", 5th edition, John Wiley & Sons, Inc., 1990

Marangoni effect in a more general sense to refer a class of physico-chemical phenomena where dynamic alteration of the interfacial properties is involved, including thermo-capillarity, electro-capillarity, and surfactant effect.

Figure 7 illustrates a simple device that achieves droplet fission via thermo-capillarity. A droplet is entrapped in a cell. The cell wall maintains room temperature T_0 throughout the process. Inside the cell there are a pair of micro-heaters with initial temperature of T_0 touching the droplet. As shown in Figure 7, the geometry of the droplet is in equilibrium among the surface contacts with the cell walls and the micro heater.

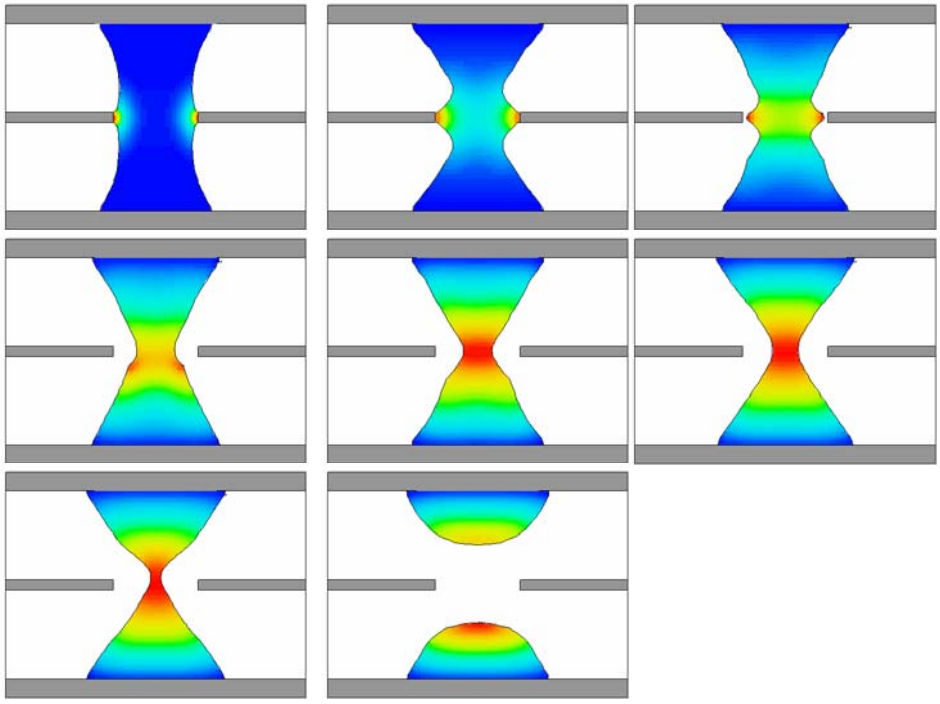

Figure 8: Liquid disintegration via thermocapillarity (simulation results). The images are colored by temperature distribution. A current passes through the heater and heats up its surrounding liquid. Since the interfacial tension coefficient decays with the increase of local temperature, an interfacial force gradient is established. The interfacial force difference eventually breaks up

At time $t=0+$, an electric current passes through the heater and the temperature at the heater is raised to $T_1=T_0+\Delta T$. Through thermal conduction, the liquid surface at the vicinity of the micro heater is heated up. The local surface tension coefficient decays with the increase of the local temperature. According to the Laplace equation,

$$P_{liquid} = P_{air} - \gamma\varepsilon \qquad (1)$$

where γ is the surface tension coefficient and ε is the local curvature, the decrease of γ at a hot interface results in a high liquid pressure in a hot liquid region. Such a pressure difference (from the hot region near the micro heater to the cold region near the cell wall) induces a liquid flow from the center of the droplet to the cell walls. This flow shrinks the cross-section of the liquid column at its middle. When the cross-section area goes to zero, the liquid column is broken into two droplets (Figure 7).

Figure 8 shows the results from a simulation of droplet fission by the Marangoni effect. The liquid body is colored by the temperature distribution. Initially the shrinkage of the cross-section happens at the two points that are slightly above and below the micro heater due to the adhesive force resulting from the direct contact of the heater surface and the liquid interface (the second picture of Figure 8). The reduction of the surface tension eventually pulls the liquid column off the micro heater and a single potential pinch-off point is achieved (the sixth picture in Figure 8). Eventually the liquid column breaks at this point and forms two discrete droplets (the eighth picture in Figure 8).

Droplet fission via electro-capillarity functions in a similar fashion. The presence of the electrical field does not alter the surface tension coefficient. However, the electrical energy stored in the thin dielectric coating that the droplet sits on does exert a force (an EWOD force) onto the contact rim [29] (an experimental observation would be the reduction of the contact angle). Such an EWOD force induces an expansion of the contact base and drains the liquid mass from the potential pinch-off point and eventually separate a liquid body.

The presence of a surfactant (a polymer with a hydrophobic end and a hydrophilic end) on the interface would modify the balance of the surface chemical energy, in other words, the surface tension coefficient. Distributing a surfactant in a pre-programmed fashion can result in a similar droplet fission as by thermo-capillarity. However, to the authors' knowledge, the practice of distributing surfactant to create liquid disintegration has not been reported in biochip research literature.

4.4 Summary of liquid disintegration physics

The requirement for successful liquid disintegration is creating a mechanism that accelerates the shrinkage of the jet cross-section at the potential pinch-off point. For cylindrical jets, the surface tension force accelerates the pinch-off process and is therefore a driving effect. The liquid inertia can be either a driving effect or a preventing effect due to the different liquid disintegration modes.

Through continuous jetting, the droplet size and terminal velocity can be controlled by altering a small amplitude disturbance signal (an acoustic wave). However, the production of droplets is not controllable – a stream of droplets is constantly produced. Continuous Jetting requires only a simple flow source (a fixed pressure overhead or a fixed flow) and a simple acoustic generator that is able to deliver a harmonic wave (small amplitude) at the nozzle. The rather simple actuation requirement (compared to drop-on-demand) is the reason that designers choose the continuous jetting method over drop-on-demand when precise control over the event of droplet generation may not be needed or the actuation method may not meet the requirements to deliver drop-on-demand (for instance, see Section 6).

Drop-on-demand offers complete control over the liquid disintegration process: the production of droplets itself, and the size and terminal velocity of the droplets. The key to carry out drop-on-demand successfully lies in a sophisticated actuation mechanism that delivers large amplitude displacement, creating the flow, and reverses the direction of the displacement rapidly. The most popular drop-on-demand actuators are diaphragms, controlled by piezoelectric or electrostatics; and thermal bubbles, created by embedding an electric resistor in the liquid reservoir that heats up the surrounding liquid and induces nucleation.

[29] Zeng J & Korsmeyer F T, "Electro-Wetting-Dielectro-Droplet-On-Dielectric (EWDDOD) - The Electro-Mechanical Origin of Electro-Wetting-On-Dielectric (EWOD)", report to prof. P. R. C. Gascoyne, 12/11/02

In order to utilize the Marangoni effect for liquid disintegration, design of the distribution of an electrical potential, temperature or surfactant concentration is required so that a desired disparity of the tangential interfacial stress can be created to induce a useful bulk flow. It should be noted that in a microscopic environment, the surface tension force usually dominates other forces. Therefore, methods that modify the surface tension force, either through changing the surface energy per unit area (surface tension coefficient) or changing the contact angle, can create a large impact in microscopic liquid flow. This is precisely the reason that utilizing the Marangoni effect as means to manipulate liquids in biochips has recently attracted much attention.

5 Reduced-Order Modeling of Liquid Disintegration

While detailed simulation is useful for the study of component physics, control and system optimization require models that are computationally cheap. A reduced-order model for liquid disintegration that is computationally cheap and ready to be integrated into a system design environment is the subject of this section.

5.1 Directional preference in liquid disintegration process

The liquid disintegration process is heavily influenced by the jet momentum, more precisely, the component along the direction that jet advances (hereafter referred as *z*-axis for convenience). In other words, the liquid disintegration process is inherently function of both *z* (space) and *t* (time).

The directional dependency of the liquid disintegration process is awkward from the conventional system-level programming perspective, which usually describes a device component using a lumped model that is solely a function of *t*, so that the system dynamics can be described via time-dependent ordinary differential equations (ODE).

Attempts have been made to incorporate the inherent directional dependency of the physical process under the ODE constraint of the system-level programming environment. There are two common practices.

The first practice is to use a so-called descriptive approach. The representative work is Kyser, Collins and Herbert 1981 [30]. The droplet formation and breakup process was divided into four stages:

Phase 1: The chamber pressure is positive; fluid in the orifice is accelerating outwards.

Phase 2: The chamber pressure is negative; fluid in the orifice is decelerated, but still has positive velocity.

Phase 3: The chamber pressure is negative; fluid velocity in the orifice has become negative and the droplet detaches.

Phase 4: The surface tension forces refill the orifice to replace the ejected fluid and pressures relax to equilibrium.

Note that the directional dependence is pre-assumed in each phase and the change in the direction is captured by switching the state among different phases (digital events). That is, the sequencing in time of each phase advances the liquid disintegration process.

This descriptive approach has achieved limited success. The major limitation lies at the fact that the applicability of the reduced-order model heavily depends on the observation of the liquid disintegration process with respect to the specific device through either physical or computational experiment. So while

[30] Kyser E., Collins L. F. & Herbert N., 1981, Journal of Applied Photographic Engineering, Vol. 7, No. 3, 73

a model may be successful for a given device, its application to another device, even if similar, is suspect. A recent description of this approach can be found in Koltay, Moosmann, Litterst, Streule, Birkenmaier & Zengerle 2002 [31].

Another approach is to use a group of elements to describe the behavior of one device/component. The disparity of the cross values (representing the state of each element) among elements is used to mimic the directional dependency of the physical process. An example application is Lee, Kim, Shin & Shin 2003 [32]. This approach has a basis in first principles but still requires tuning with experimental observation and so a given model's portability is limited.

5.2 A high-fidelity, reduced-order model for liquid disintegration: 1D-PDE

As previously noted, detailed simulation is too computationally expensive for the study of a system and its control. But the reduced-order approaches stated above have limitations as well: the designers carry the burden of constructing and testing the model; and the model's portability is poor. These limitations are due to the fact that these approaches are not derived from first principles and therefore, once tuned, are device specific.

In this section a hybrid approach will be introduced that is potentially computationally cheap and, at the same time, is derived from first principles. Hereafter it is called the *1D-PDE* model. This model is composed of a set of partial differential equations (PDE) with two variables: z representing the droplet flight direction and t representing time.

Historically there have been attempts to construct 1D-PDE models to study liquid disintegration as a compromise for lack of the computational power and an advanced simulation engine. The earliest work found was done by Lee 1974 [33], where the viscous aspect of the liquid was omitted. Lee's work, although not elegant from today's standpoint, made an important impact on IBM's ink-jet device design. A different 1D-PDE model has been presented by Shield, Bogy & Talke 1987 [34]. This model is complicated in its structural mechanics, but its connection to the Navier-Stokes equations is not clear.

The 1D-PDE model presented below is based on conservation of mass and momentum (Navier-Stokes equations) and a long wavelength assumption (Eggers & Dupont 1994 [35]). The long wavelength assumption indicates the jet is always slender, i.e., the jet radius (hereafter noted r) is small compared to the jet length L (the distance from the jet tip to the orifice projected in z-direction), ($r/L<<1$). Therefore we can write a Taylor expansion of Navier-Stokes equations with respect to r. Next we omit all the terms other than the lowest order with respect to r and now we have obtained a set of asymptotic equations that are independent of r, i.e., a set of 1D-PDE with only two variants t and z, as listed below [36]:

[31] Koltay P., Moosmann C., Litterst C., Streule W., Birkenmaier B., Zengerle R., 2002, the Fifth International Conference on Modeling and Simulation of Microsystems (MSM); April 22-25, San Juan, Puerto Rico

[32] Lee Y.-S., Kim M. S., Shin S. H. & Shin S. J., 2003, Nanotech 2003, February 23-27, San Francisco, CA

[33] Lee H. C., 1974, IBM J. Res. Dev., 18, 364

[34] Shield T. W., Bogy D. B. & Talke F. E., 1987, IBM J. Res. Dev., Vol. 31, No. 1, 96

[35] Eggers J. and Dupont T. F., 1994, J. Flui Mech., Vol. 262, 205

[36] It is rather straightforward to derive this set of 1D-PDE from Navier-Stokes equations. There is no additional mathematical complexity involved except for procedures mentioned here.

$$\frac{\partial v}{\partial t} = -v\frac{\partial v}{\partial z} - \frac{\partial p}{\rho \partial z} + \frac{3\nu}{h^2}\frac{\partial}{\partial z}(h^2\frac{\partial v}{\partial z}) - b \tag{2}$$

$$p = \gamma\left(\frac{1}{h[1+(\frac{\partial h}{\partial z})^2]^{1/2}} - \frac{\frac{\partial^2 h}{\partial z^2}}{[1+(\frac{\partial h}{\partial z})^2]^{3/2}}\right) \tag{3}$$

$$\frac{\partial h}{\partial t} = -v\frac{\partial h}{\partial z} - \frac{h}{2}\frac{\partial v}{\partial z} \tag{4}$$

where v and h are the primary variables recording the jet velocity and radius with respect to time t and space z, governed by equation 2 and equation 4. Pressure p is calculated according to equation 3 and introduced into the system via right-hand-side of equation 2. ρ, ν, γ represent the liquid material properties: density, kinetic viscosity and surface tension. b represents the body acceleration (for instance, gravitational acceleration, dielectrophoretic acceleration)[37]. Equation 2 is the reduced-form of the momentum conversation equation. Equation 3 states that the surface tension force is balanced by the liquid stress at interface. Equation 4 states the material (interface) advects with the liquid flow. The mass conservation is warranted implicitly, for the continuity equation was used during the derivation.

It should be noted that the long wavelength assumption fails at the jet initialization stage where the jet length L may be comparable to the jet radius r. However, this stage is usually very short (comparing to the droplet formation process) therefore it does not endanger the applicability of the long wavelength assumption to the liquid disintegration process overall.

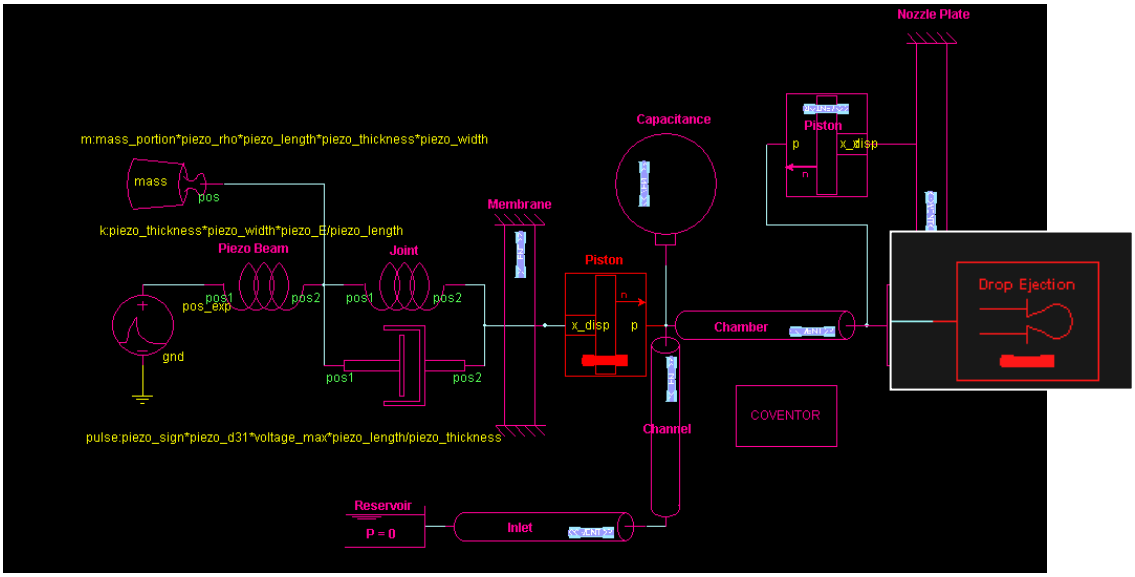

Figure 9: An example system model schematic for a droplet injection process. The 1D-PDE model is expected to be a component of the electro-hydro-mechanical library which includes components that execute transduction among different energy domains, actuation, gating, sensing, etc.

[37] The body force density can be expressed as ρb.

To close the problem, boundary conditions that specify *v* and *h* at the two ends of *z* are required. The boundary condition for *h* is geometrical. Usually *h* is set to the nozzle radius at *z=0* and is set to zero at *z=L*. On the other hand, the boundary condition for *v* carries the dynamic interaction of the liquid disintegration component with the rest of the system. Under system programming environment, the flow rate is considered the through variable passing between connected fluidic components. *v* can be obtained via flow rate divided by the area of nozzle cross section.

At this moment we have obtained the 1D-PDE in a closed mathematical form. However, it should be noted that the inherent singularity of $\left(\frac{\partial h}{\partial z}\right)$ close to the pinch-off point makes the numerical implementation a far from trivial project. In most simulations based on the 1D-PDE model, the computation was terminated before droplet detachment to avoid confronting this singularity issue (for instance, Eggers & Dupont 1994 [35]). This will not be acceptable when the behavior of multiple droplet formation is sought.

Additional numerical challenge may occur during the system-level integration (with respect to *t*). When the liquid disintegration process approaches to the pinch-off point, the component stiffness increases dramatically – in other words, the system integrator will be forced to choose much smaller time-step in order to maintain the system's convergence behavior. This 1D-PDE model is intended to be an integral component of a larger dynamic system that involves actuating, gating and sensing components. The presence of many heterogeneous components is expected to complicate the convergence behavior of the dynamic system even further. There are no results from such simulations published in the literature.

The numerical challenge of the 1D-PDE model stated above (the singularity with respect to both time and space) largely justifies the popularity of other reduced-order approaches (see Section 4.1). However, the reward of tackling this problem is high: a computationally cheap, highly accurate, highly portable, reduced-order model for liquid disintegration. The current strategy for overcoming the singularity with respect to space (*z*) includes artificially inserting two "pinch-off" points with a small (negligible) distance in between. The strategy to address this is to insert a channel with a tunable resistance between the injection nozzle and its actuator. The presence of this channel (a fluidic resistor) is expected to help reduce the stiffness of the liquid disintegration component. Current work is focused on the derivation and programming of the numerical scheme.

6 A Hybrid Droplet Generation Method: Continuous Jetting + DEP Gating

In the PFP, a liquid disintegration method that is controlled by DEP is desired. Such a liquid disintegration mechanism is the topic of this section. In section 5.1, the composition of the DEP force component and the implication to possibility of liquid disintegration methods are analyzed. In section 5.2, a new hybrid droplet generation concept that realizes DEP's control over droplet production: continuous jetting + DEP gating is proposed and further validated via computational prototyping.

6.1 Control of liquid disintegration by dielectrophoresis (DEP)

The force density of the DEP force can be expressed as follows,

$$\vec{F}^{EM} = \rho_e \vec{E} - \frac{1}{2} |\vec{E}|^2 \nabla\varepsilon + \nabla[\frac{1}{2}(\varepsilon - \varepsilon_0)|\vec{E}|^2] \qquad (5)$$

where ρ_e is the net free charge density, ε is the dielectric constant, and $\vec{E}$ is the electrical field. The significance of equation 4 is that it unveils the composition of the DEP force and the physical basis of

each component. The DEP force has three components: a body force due to free net change (the first term), an interfacial force due to the discontinuity of the dielectric constant (the second term), and a body force due to the electrical field non-uniformity (the third term).

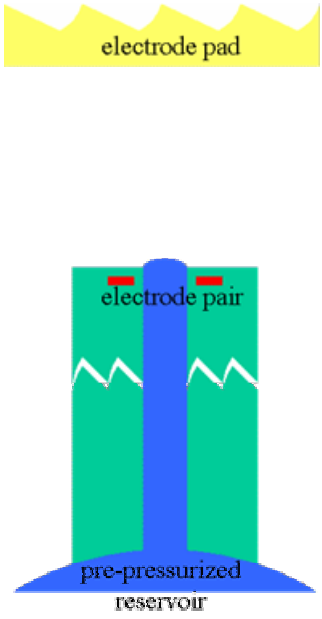

Figure 10: Set-up of continuous jetting + DEP

In an environment that is either charge-neutral or $\vec{E}$ oscillates at a frequency that is much higher than the charge relaxation time[38], the body force due to free net charge zero.

The direction of the interfacial force density is parallel to the gradient of the dielectric constant. That is, it is perpendicular to the interface and therefore does not contribute to the tangential interfacial stress. Clearly, the DEP force cannot trigger the Marangoni effect.

In order to successfully carry out Drop-on-demand, the actuation mechanism needs to be strong enough to induce flow. For DEP, this means an extremely high controlling voltage (for instance, order of 1000V[39]) is required. Such a high voltage presents a challenge for the supporting integrated circuitry to accommodate.

6.2 Making use of continuous jetting + DEP gating

Drop-on-demand offers control over all aspects of droplet production. However, conventional implementations require extremely high voltage. Continuous jetting uses the pressure-overhead that is built into the system to drive the liquid flow and so requires lower voltage, but it does not offer a mechanism to stop the production of the droplets when desired. In this section we propose a hybrid droplet generation method: continuous jetting + DEP gating. This method offers control over the droplet production, and does not require an extremely high actuation voltage.

Figure 10 shows the setup for the continuous jetting + DEP gating device. The setup differs from the second-generation solid-state injector [40] in that a pair of electrodes has been embedded right underneath the injector nozzle (shown in red in figure 10).

The liquid reservoir is pre-pressurized with a pressure-overhead ΔP of slightly less than the capillary gating $\gamma\varepsilon$, where ε is the interfacial curvature and may be estimated as $2/R$, with R the nozzle radius. $\Delta P \prec \gamma\varepsilon$ guarantees that the capillary gating will prevent liquid flow. Initially, the electrode pad (shown in yellow in figure 10) is turned off.

At time zero, the electrode pad is turned on. The generated DEP pressure (the second and third terms in equation 4) works with ΔP breaking up the capillary gating. Once the capillary gating is broken, the pressure overhead ΔP, by itself, can generate a liquid jet out of the nozzle [41].

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[38] Melcher J R & Taylor G I, Annual Review of Fluid Mechanics 1, 1969, pp. 111–146
[39] Jones, T. B., Journal of Electrostatics 51-52 (2001) pp.290-299
[40] J. Schwartz, "Notes to accompany Solid-State and high-speed videos of DEP injection", June 14, 2002, experiment "sequence 03040201-pressure fill.mpg." Also, personal communications with J. Schwartz.
[41] To estimate the jet velocity, one may refer to "On modeling of dielectrophoretic-driven programmable fluid processor", report to MDACC authored by Zeng J, Deshpande M and Gilbert J R, 06/21/02, Part3, section3.7.

A small-amplitude AC voltage is passed to the electrode pair and generates an acoustic wave. We denote as V_{aw} the amplitude of this AC voltage. The acoustic wave propagates along the jet and turns the jet into a stream of droplets. This is the continuous jetting phase. V_{aw} can be very small, as its purpose is simply to trigger the intrinsic jet instability. The energy consumed to break the jet is not from this acoustic wave, but is the interfacial energy released due to break-up plus the liquid jet kinetic energy.

At the time that the termination of the droplet production is desired, the voltage at the electrode pair is increased. We denote as V_{gate} the amplitude of this AC voltage. The DEP force induced by this voltage has a force component that works against the liquid flow.

Figure 11 illustrates the origin of the DEP force component that works against the liquid flow. For convenience, pairs of "fictitious" charges are used to represent the polarization of the dielectric material. [42]. The induced fictitious charge due to the presence of the electric field is advected upstream to a distance of $L = U\varepsilon/\sigma$, where U is the jet velocity, ε is the dielectric constant, σ is the conductivity, and ε/σ represents the charge relaxation time. The distribution of fictitious charge acts in concert with the presence of the electric field and results a downward dielectrophoretic force component.

It should be noted that the distance between the electrode pair is about the diameter of the nozzle (order of 10 microns). Therefore it does not require high V_{gate} to generate a DEP force that can successfully stop the jet flow. In the simulation shown in figure 12, V_{gate} is on the order of 100V, much less than the voltage required for operating in drop-on-demand mode.

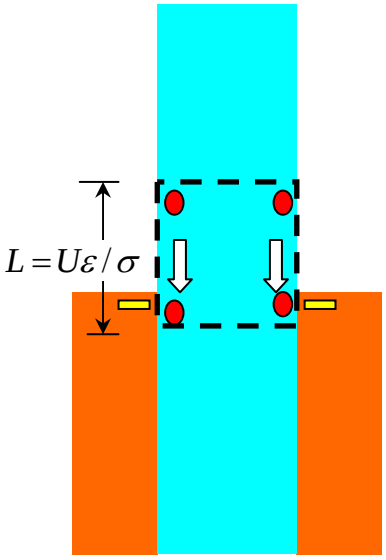


Figure 11: Schematics to illustrate the root of the DEP gating component. Advection of the fictitious charge induced by the presence of the electrical field results in a downward force component working against the liquid flow.

Figure 12 shows the computational prototyping of the device. When the termination of droplet generation is desired (*time=11.4τ* in figure 12), V_{gate} is applied to the embedded electrode pair. The advection of the induced "fictitious charge" acts in concert with the electrical field resulting a dielectrophoretic force that works against the liquid flow. Such a pulling-back force results in the release of the liquid column that is already out of the nozzle (between *time=11.4τ* and *time=13.4τ*), and recovery of the capillary gating at the nozzle (after *time=13.4τ*). After the liquid momentum dissipates, the electrode pair can be turned off and the capillary gating mechanism will be sufficient to prevent liquid flow.

[42] Such practice can also be found in Haus, H A & Melcher J R, "Electromagnetic Field and Energy",

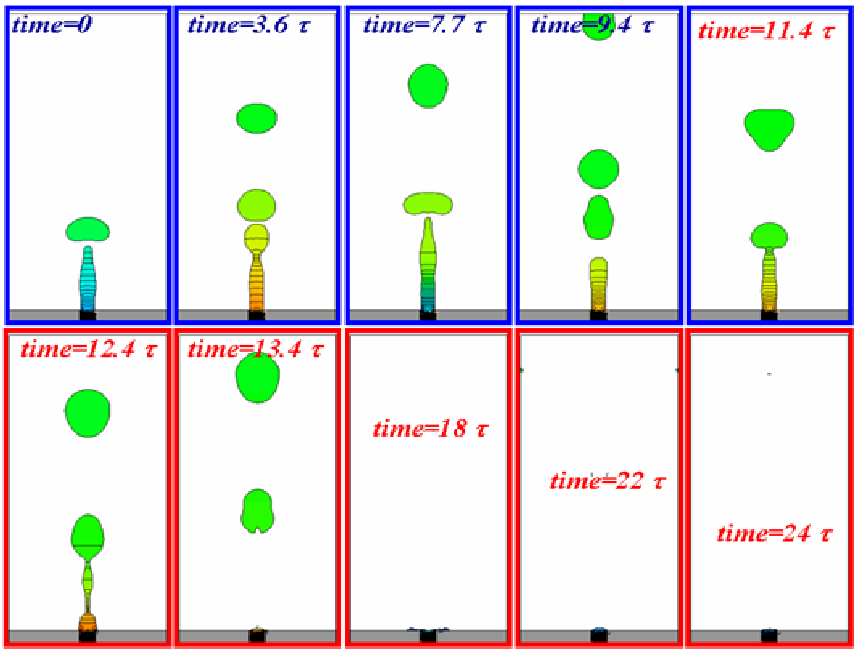


Figure 12: Computational prototyping of the hybrid droplet injection method: continuous jetting + DEP gating.

Task 75. Build DEPTrans and DropChem
Super-Hydrophobicity via Fabricating Micro-Structures onto Surfaces

Coventor, Inc.

- Intrinsic material property (***chemical composition***) of the liquid and solid surface combined with actively created ***surface morphology*** can deliver interfacial super-hydrophobicity. In this document, we summarize the background (theory), and issues associated with design and fabrication.

-

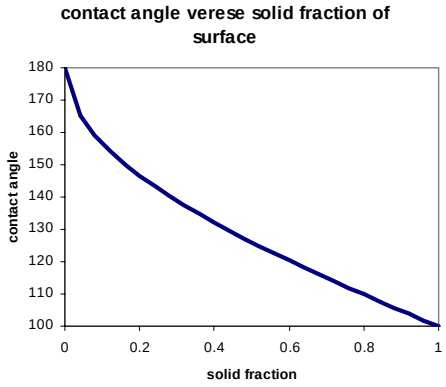
- **Background**

Water droplets rebound on lotus leaves quite efficiently. Such super-hydrophobicity is due to the combination of chemical composition of the lotus leaf surface (covered by wax that is strongly hydrophobic) and the physical structure of the surface (surface is made of bumps that are about 10 □m wide, the bumps are covered with hollow tubes that are roughly 1 □m in diameter). This is the so-called "lotus-effect"[43].

Surface roughness amplifies the surface wettability[44]: it makes chemically hydrophilic surfaces even more hydrophilic, chemically hydrophobic surfaces even more hydrophobic. Assuming the micro-structure on a surface has a repeatable pattern, Φ_s denotes the solid fraction of the surface, the modified contact angle is given by [45]

$$\cos\theta^* = -1 + \phi_s(\cos\theta + 1)$$

where θ* is the contact angle accounting for surface roughness, θ is the Young's contact angle representing the chemical composition of surface and liquid. To better illustrate this effect, for a moderately hydrophobic surface with contact angle 110 degree, super-hydrophobicity can be achieved via creating a micro-structure on the surface as shown in the figure below.



It should be noted that the model assumes: (1) droplets are very large compared to the dimension of the micro-structures; (2) the effect of the micro-structure can be well characterized via a lumped number Φ_s.

[43] Dr. W. Barthlott started to call that since 1992, and registered it as German trademark.
[44] Wenzel, R. N., Ind. Eng. Chem., 28 (1936) 988; J. Phys. Colloid. Chem. 53, (1949) 1466
[45] Bico, J., Marzolin, C. and Quere, D., Europhysics Letters, 47 (2), pp. 220-226, 1999

Design and Modeling (CAD)

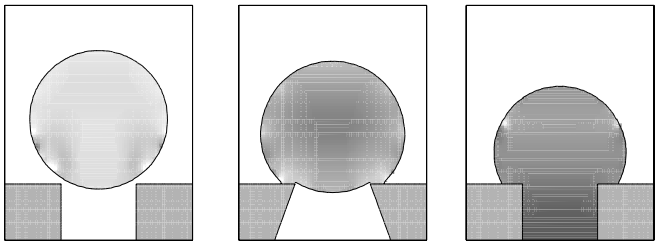
Advance of micro fabrication allows engineers to explore structures in sub-micron to nano scale. This opens up an avenue to actively design surface morphology to enhance surface wettability. Such treated surface technology has attracted noticeable attention since early last year (for instance, a Science article in March '01 on D. Beebe and Science News, Vol. 160, P.57, 07/28/01 on D. Quere). It has been reported[3] that super-hydrophobicity can be achieved for a droplet of 100 micron with surface roughness in micron dimension.

With a given desired droplet size, one needs to consider the following questions in designing optimal micro-structure to achieve super-hydrophobicity:

1. What is the density of the micro-structure (Φ_s)?
2. What is the optimal geometry of the micro-structure? The theory in Background section assumes only the dimension of the micro-structure matters (Φ_s). However, it has been reported that micro-structures with different shapes report different results, the spike-like surface roughness reports better efficiency. The optimal geometry remains to be seen.
3. What is the dimension of the micro-structure? The lower bound is limited by fabrication cost, the upper bound is limited by the given droplet size.

These questions CAD can help answer.

In addition, the surface roughness modifies the wall adhesion to the droplet and consequently affects the



135° Contact angle or larger drop | **Sloped Surface** | **120° Contact angle or smaller drop**

way a droplet moves on the surface: preliminary simulation shows the droplet rolls on the roughened surface rather than sliding. CAD can be used to quantify the enhancement of droplet migration by surface roughness.

Fabrication

Method 1: **soft lithography**

The fabrication detail see Whitesides 1998[46] and also Quere[3]. The basic idea is to generate sub-micron patterns of glasses on a substrate via molding of a sol-gel precursor against an elastomeric replica of the designed patterns. After gellation, the glass structures are then consolidated at 1100 ^{0}C for 2 hours and rendered hydrophobic.

It is reported that this technique allows the reproduction of fine features with 10 nm dimension.

Method 2: **coating**

Sunyx[47], a German company claims a smart coating technology that creates a coating with nano-scale bumps onto surface and achieve the super-hydrophobicity, or rather, in Sunyx's term, ultra-hydrophobicity. SEM graph shows that bumps of up to 100nm scale are distributed onto the surface

[46] Marzolin, C., Smith, S. P., Prentiss, M. and Whitesides, G. M., Advanced Materials, 1998 10, No. 8, pp.571-574

[47] http://www.sunyx.de/sunyx_engl/index.html

statistically. Comparing against soft lithography, it does not offer clear patterns of micro-structures rather randomly distributed.

Coventor has contact with Sunyx.

Task 83. Build ArraySim

Energy Transduction in the Programmable Fluidic Processor

Impact on Droplet Migration of Different Electrode Pad-Gap Ratio

Jun Zeng & Tom Korsmeyer
Coventor, Inc.
May 9, 2003

1. Problem Statement

In the Programmable Fluidic Processor (PFP), an array of electrode pads is used to deliver electrostatic energy into the system. The electrohydrodynamic force exerted on a dielectric liquid is a transducer, transferring energy from the electrical domain to the hydrodynamic domain. In other words, electrical power is translated into motion of droplets.

Now, the question is: if we pump electrostatic energy at a higher rate, will that enhance the droplet migration, *i.e.*, cause more rapid response of the droplet to the electronic control? The electrostatic power pumped into the chip is proportional to the square of the driving voltage. Raising the driving voltage does deliver rapid droplet response, as has been shown in previous simulations. There is an upper bound, however, on the electrostatic power, since the voltage is limited by the device's IC component.

Another option to increase the electrostatic energy input is to increase the dimension of the electrode pad while keeping the total device footprint fixed. If we assume a fixed device configuration, *i.e.*, the dimension of the chip, droplets and dielectric coating, material properties and operating condition, then the device capacitance should not vary much even if the dimension of the electrode pad is changed. Given the fixed footprint, a change in the electrode pad dimension will modify the gap between the electrode pads. However, the thickness of the electrode pads (the gold layer) is very small compared to other dimensions, so a change of the gap size should have negligible impact on the chip capacitance. In other words, the electrostatic power pumped into the system should increase linearly with the increase of the electrode pad surface area.

This report presents results from simulations investigating whether an increase in the electrode pad dimension gives rise to higher droplet momentum.

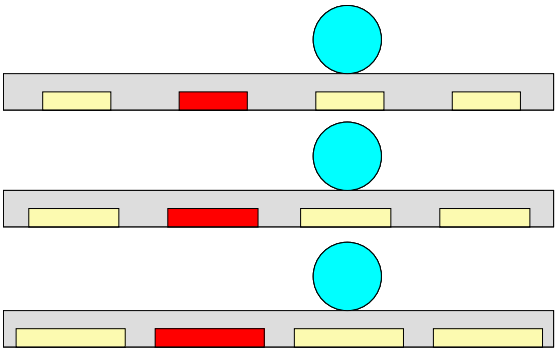


Figure 1: Simulation configurations. From top to bottom: electrode pad verses gap ratio equals one, the electrode pad size is 100 μm; electrode pad verses gap ratio equals two, the electrode pad size is 133 μm; electrode pad verses gap ratio equals four, the electrode pad size is 160 μm. The size of the footprint is 200 μm, and the droplet diameter is 100 μm.

2. Simulation Setup

Three simulations have been carried out with different sizes of electrode pads within a fixed footprint, as shown in Figure 1. The operating condition, droplet size, properties of the working fluids and coating material are kept the same. We record the time-of-flight, which is the time taken for a droplet centered at a "cold" electrode pad to slide to the neighboring "hot" electrode, as the indicator for the performance of the energy transduction from electrostatic energy to droplet translational kinetic energy.

3. Results and Discussion

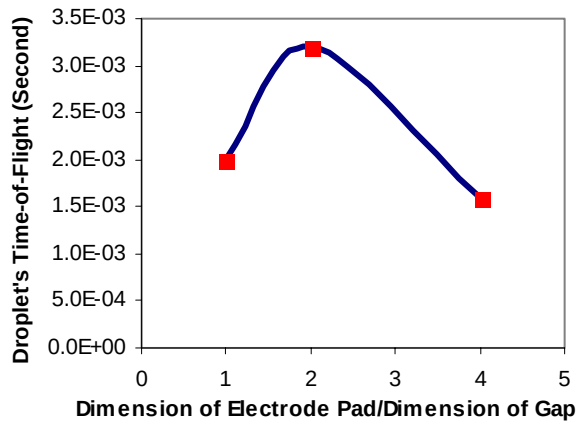


Figure 2: Recorded droplet time-of-flight

The time-of-flight of three different configurations is reported in Figure 2. The figure shows that the translational kinetic energy acquired by the droplet does not increase monotonically with the increase of the dimension ratio of the electrode pad to the gap. The average energy density in the domain of computation is plotted in Figure 3. The electrostatic energy – the dielectrophoretic potential in the droplet and the suspending medium, and the electro-wetting potential in the thin dielectric coating layer – increases linearly with the increase of the electrode pad dimension. The trend of the kinetic energy is more complicated. The variation of the kinetic energy with respect to the change of the electrode pad is noticeably smaller than the variation of the electrostatic energy. This indicates that the input energy through the electrode pad surface is efficiently distributed into the system (diffusion mechanism). However, converting the electrostatic energy into kinetic energy through the electrohydrodynamics transduction mechanism is less efficient.

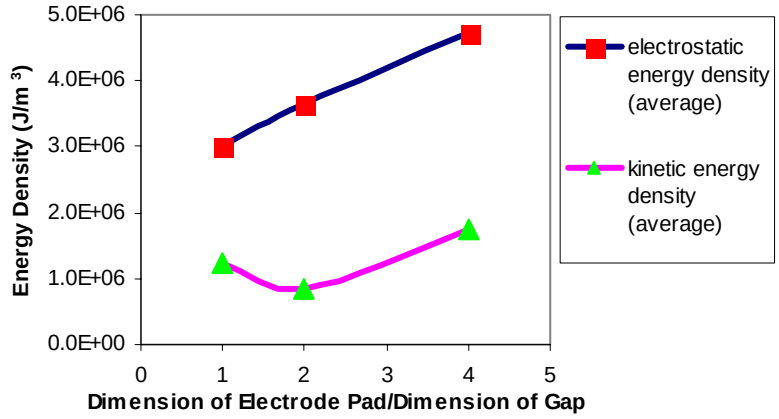


Figure 3: Average energy density in domain of

The highest efficiency (ratio of kinetic energy verses electrostatic energy) is achieved when the dimension ratio of the electrode pad and the gap equals one, as shown in figure 4.

A force analysis sheds some light on the complexity of the energy transduction mechanism in the Programmable Fluid Processor. Figure 5 shows the translational component of the dielectrophoretic force density on the droplet (volumetric average). The translational work done by the DEP force (the area under the curves) increases monotonically with the increase of the electrode pad dimension. However, the spring-like behavior of the DEP force requires that part of the work that contributes to drive the droplet be cancelled by the work that contributes to stop the droplet.

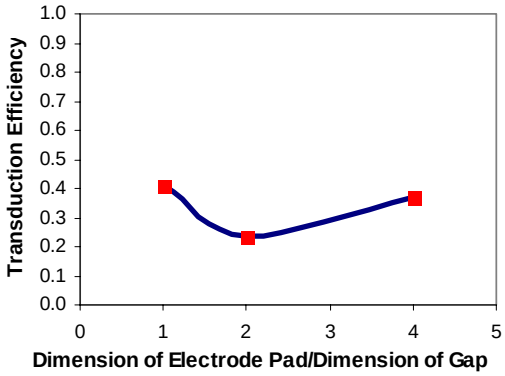


Figure 4: Energy transduction

From an efficiency of energy transduction point of view, the work that contributes to slowing down of the droplet is negative. However, it is the very presence of this "negative" work that makes the control of droplet motion through dielectrophoresis possible.

There is a local minimum of the transduction efficiency when the dimension ratio of the electrode pad to the gap equals two. A hypothesis is that the natural frequency of the device configuration is close to the natural frequency of the droplet. Therefore a large amount of electrostatic energy that is supposed to contribute to droplet translation is consumed by interfacial oscillation. This is a condition that should be avoided by design.

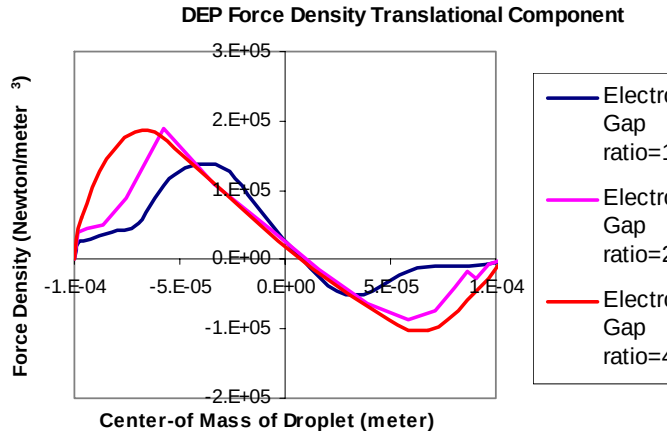


Figure 5: Translational component of dielectrophoretic force density (volumetric average) with respect to the droplet