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PHOTONIC ANALOG-TO-DIGITAL CONVERSION TECHNOLOGY

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13. ABSTRACT ***(Maximum 200 Words)***

This report documents the work undertaken by HRL Laboratories, LLC and its subcontractors, California Institute of Technology and Raytheon Electronics Systems, on the development of multi-GHz photonic analog-to-digital (A/D) conversion technologies (PACT). Using an electro-optic modulator, the analog-input to the A/D converter was impressed (i.e. photonically sampled) on a train of low-jitter picosecond pulses (wavelength - 1540 rim) generated by a mode-locked Er-fiber laser. After photodetection, the electrical outputs of the photodiodes were fed to a variety of electronic quantizers for digitization. Specifically, the HRL Program demonstrated InP-HBT bandpass Delta-Sigma A/D converter with 10 bits of resolution, using photonic sampling at 10 GHz. The Program also demonstrated photonic clock distribution to multiple flash A/D converters, and a 40 GHz photonic time-interleaved architecture based on wavelength division multiplexed technologies. For the 40 GHz time-interleaved architecture, the program achieved -- 4 SFDR-bits of resolution. PACT is compatible with antenna remoting systems that utilize fiber optic links for signal distribution.

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Photonic Analog-To-Digital Converter, Photonic Clock Distribution, Optical Analog-To-Digital Converter, A/D converter, Ultrafast Photonics

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INTRODUCTION AND SUMMARY

1.A Introduction

The interest in applying photonics technologies to analog-to-digital (A/D) conversion stemmed originally from a need, in defense systems, to accomplish high resolution A/D conversion at multi-GHz sampling rates (f_s). A well referenced 1999 publication[(1)] that tracked the advances of all-electronic A/D conversion technology attributed the observed limitations in resolution to timing-jitters (>0.5 psec) present in the sampling apertures of analog-to-digital converters (ADCs). We show, in Figure 1.1, a plot (derived from that survey) of the resolution attained by electronic ADCs versus their sampling rates. Specifically, the resolution of A/D conversion in the plot was quantified by the number of signal-to-noise ratio (SNR) bits[(1)] measured for the ADCs. As shown in the plot, an estimated aperture jitter of 0.5 psec bounds the performance of the Nyquist ADCs surveyed in Ref. 1.

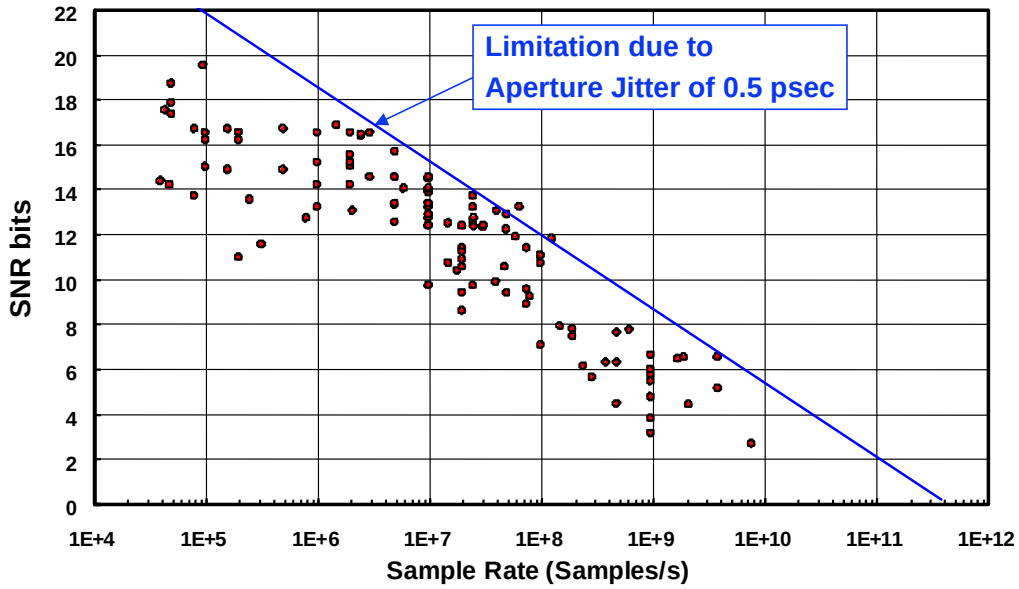


Figure 1.1 SNR-bits of electronic ADCs vs sampling rates.

In this Program, we demonstrated that photonics has many attributes that can impact and enhance the performance of high speed ADCs. Conceptually, the picosecond pulses generated by a mode-locked (ML) laser are ideal vehicles that would enable one to accomplish *impulse-sampling* of an analog signal. One can then use an electro-optic (EO) modulator to impress the analog input onto the optical pulse train. Figure 1.2 shows the schematic of such a photonic-assisted A/D conversion system. After photodetection, the received signal due to the modulated pulse train is fed, in turn, to an electronic quantizer for digitization. An obvious benefit that we gain via the incorporation of photonics in A/D conversion is the added capability to *remote*

various elements of the ADC. For instance, *several* modulators, each fed by a deployed antenna, can be remoted from a high resolution electronic quantizer via an ensemble of fiber links. One can also envisage the employment of a *remoted* ultra-stable microwave oscillator that would (i) drive a mode-locked laser, and (ii) clock several electronic ADC quantizers via RF-photonic links. Finally, the multi-GHz sampling rates offered by a stable picosecond pulse train will enable the direct sampling of high frequency analog input-signals. In particular, it will reduce the number of mixer-stages that are presently needed to downconvert high frequency signals before digitization. Over the course of this Program, we had demonstrated all the above features/benefits of incorporating photonics in A/D conversion. This Final Report documents, in detail, our technical accomplishments and results.

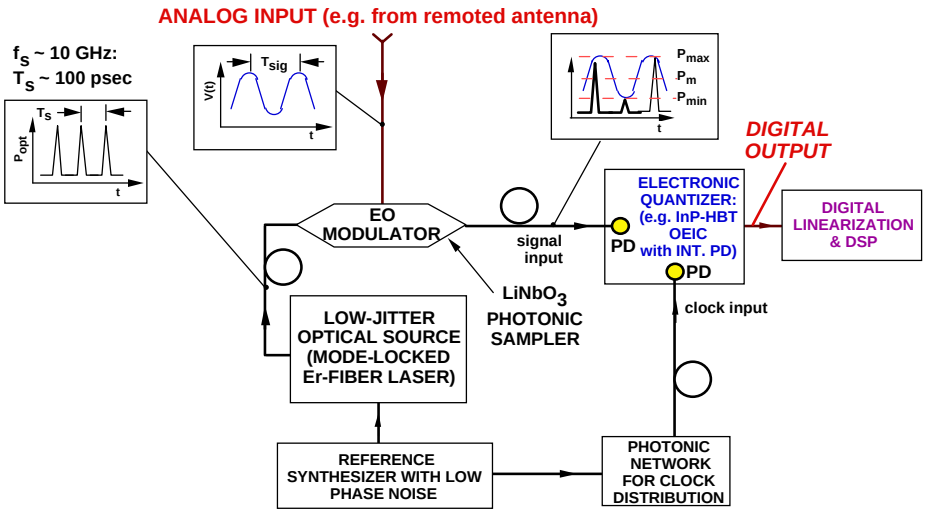


Fig. 1.2 Schematic of photonic analog-to-digital converter.

1.B Summary of Program Goals and Accomplishments

In this subsection, we first review the major technical goals of the HRL Photonic Analog-to-Digital Conversion (PACT) Program. This will be followed by a summary highlighting our accomplishments for each objective. Specifically, three major objectives were set for our Program, all of which we successfully completed. These objectives were:

- The demonstration of photonic clock distribution to multiple analog-to-digital converters.
- The demonstration of photonic ΔΣ ADCs with least 8-bits of resolution, at a sampling rate of 10 Gsamples/sec (GSPS). For this objective, we would develop ΔΣ quantizers as optoelectronic integrated circuits (OEICs) with on-chip photodetectors, using HRL's InP heterojunction bipolar transistor (HBT) technology.
- The demonstration of a 40 GSPS photonic time-interleaved ADC architecture with ~4 bits of resolution.

Below, we highlight our accomplishments with respect to these objectives, leaving the details for the rest of this Report.

As an intermediate milestone for the Program, we first demonstrated (see Section 4) the optical distribution of clock signals to remoted InP-HBT quantizers of the flash design. In the demonstration, we distributed 5-10 GHz clock signals to flash OEICs[2] via the use of analog photonic links (see Figure 1.3). The phase noise measurement shown in Figure 1.3 demonstrated that the optical link's phase noise followed that of its RF-input. Using a 10.24 GHz link-input derived from a high-quality Raytheon oscillator, we measured an absolute phase noise level of -125 dBc/Hz (at a frequency-offset Δf of 10 kHz) for the clock-distribution link. In addition, we demonstrated 3-bit A/D conversion for an optically remoted flash OEIC quantizer (see Fig.1.3). From the computed fast Fourier transform (FFT), we estimated a SNR of 18 dB (~ 2.7 SNR-bits), for an analog electrical-input located at f = 1.010 GHz. At the time of the optical clock distribution demonstration, the flash quantizers with a 3-bit design performed better as a Nyquist ADC than its 4-bit counterpart, which had too high a front-end parasitic capacitance for multi-GHz clock rates. Towards the end of our Program, we were able to accomplish the re-design of a 4-bit flash electronic quantizer (see Section 6.B), and demonstrate A/D conversion with ~3.9 effective number of bits (ENOB), over the Nyquist bandwidth of 5 GHz (for f_s = 10 GHz).

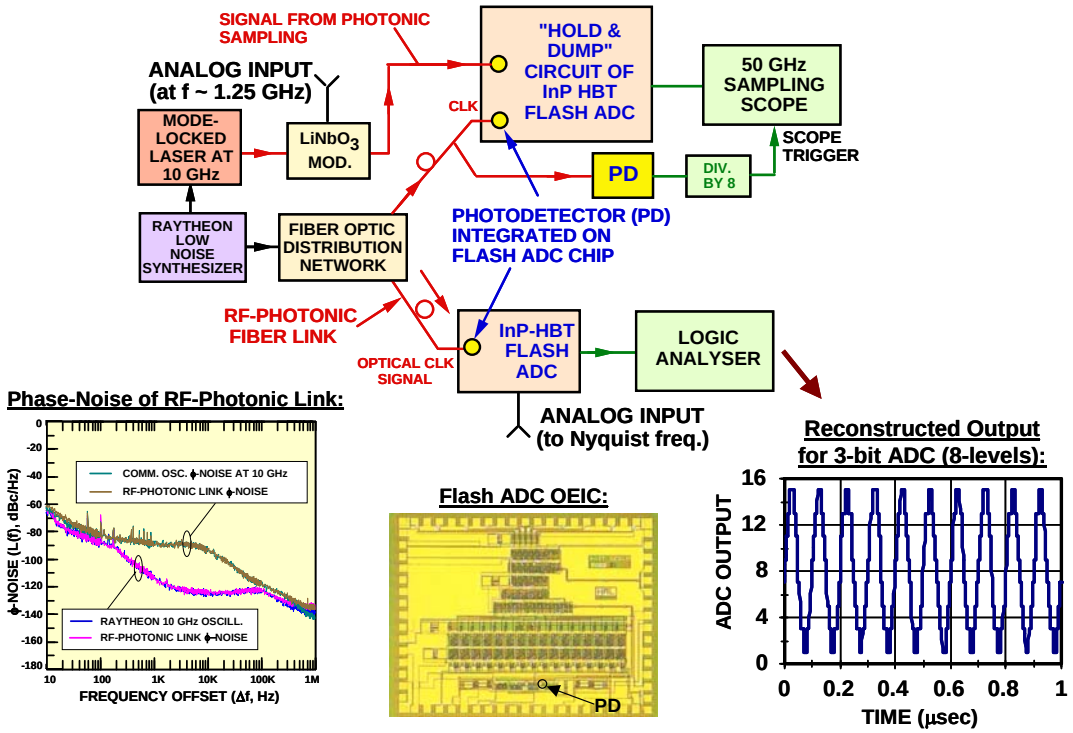
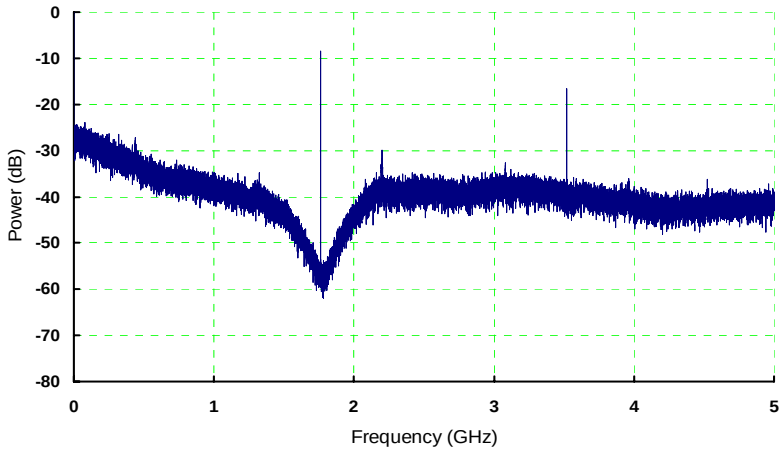


Figure 1.3 Schematic of Photonic Clock Distribution demonstration. The left inset shows the measured phase noise of an analog optical link that distributed clock signals to remoted flash ADCs. The right inset shows the 1 GHz subsampled output of a 1.010 GHz electronic signal fed to a 3-bit InP-HBT flash quantizer. The 8 levels of the subsampled signal was shown clearly in the time-domain output that we captured with a logic analyser.

For our second Program objective, we demonstrated photonic InP-HBT ΔΣ ADCs that operated at clock frequencies of 10 GHz, with quantization-noise notches (ΔΣ-passbands) formed in the frequency range of 1.5–2 GHz (see Figure 1.4a).

a.



b.

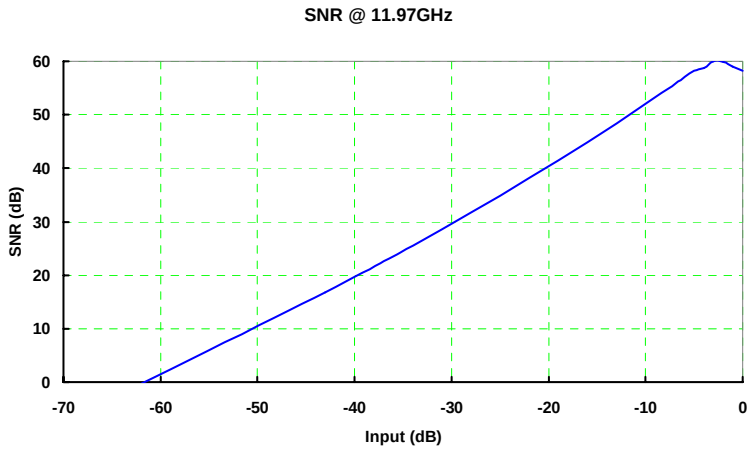


Figure 1.4 a. FFT of photonic ΔΣ ADC output, obtained from the direct photonic sampling of a 11.98 GHz analog input, using a quantization notch located at 1.76 GHz b. Measured SNR vs signal-input power, showing a maximum SNR of 59.9 dB and a dynamic range of ~ 62 dB.

In particular, we accomplished the *direct sampling* of a 12 GHz analog-input, when a stream of 10.24 GHz low-jitter, picosecond pulses (generated from our ML laser) was used to "downconvert" the X-band input to the ΔΣ notch-frequencies. Based on a timing-jitter (Δf = 10 Hz to 40 MHz) of 0.017%, and an amplitude-jitter of 0.041% measured for our ML pulse train (see Fig.I.5 and Ref. 12), we estimated that photonic sampling will support an A/D conversion resolution of ~11 bits, over a 40 MHz resolution bandwidth. The details of these jitter characterizations for our ML laser are provided in Section 2 of this Report. In our ΔΣ ADC

experiment, the photonically sampled signals were received by integrated photodetectors that possessed excellent linearity. The output 3rd order intercept (OIP3) of these on-chip photodetectors - measured via the optical heterodyning of two laser-pairs - was 29.2 dBm, with a corresponding –3 dB bandwidth of ~11.5 GHz (at a DC photocurrent level of 8 mA). From the FFT computed (see Fig.1.4a) for a 11.98 GHz analog-input fed to our ΔΣ ADC, we measured (at a notch-frequency of 1.76 GHz) a SNR of 59.9 dB in a 1 MHz bandwidth, which corresponded to ~10 SNR-bits. The large dynamic range of 62 dB (Fig.1.4b) obtained in our ΔΣ ADC experiment verified, in particular, the immunity of photonic sampling from signal-induced jitter, a notable feature of this technology. Finally, we also fabricated Y-fed directional coupler (YFDC) $LiNbO_3$ modulators that demonstrated bandwidths in excess of 15 GHz. In this task, we completed a detailed study for the impact of fabrication variance on the YFDC modulator's transfer characteristics and intermodulation products.

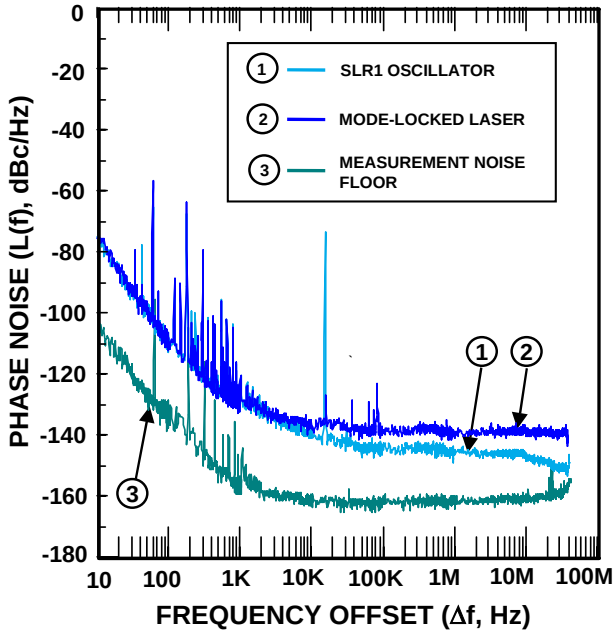


Fig. 1.5 Measured single sideband phase noise of fiber laser as it was mode-locked with sapphire loaded cavity resonator oscillator.

For the third objective, we demonstrated a 40 GSPS photonic time-interleaved architecture that was based on wavelength division multiplexed (WDM) technologies (see Fig.1.6). Here, we generated λ-coded pulses via the spectral slicing of an optical supercontinuum that was formed, in turn, by compressing picosecond pulses derived from our ML laser. After electro-optic sampling, we separated the λ-coded pulses into four parallel 10 GSPS electronic quantizers, via the use of an array-waveguide grating (AWG) wavelength demultiplexer. Figure 1.7 shows a plot of the spur free dynamic range (SFDR) and measured SFDR-bits for our 40 GSPS photonic time-interleaved ADC. As shown, we achieved close to 4 SFDR-bits for analog input frequencies f_{in} that were less than 5 GHz, and ~3.4 SFDR-bits for f_{in} = 17 GHz. Further details on our 40 GSPS WDM time-interleaved experiment are provided in Section 5.

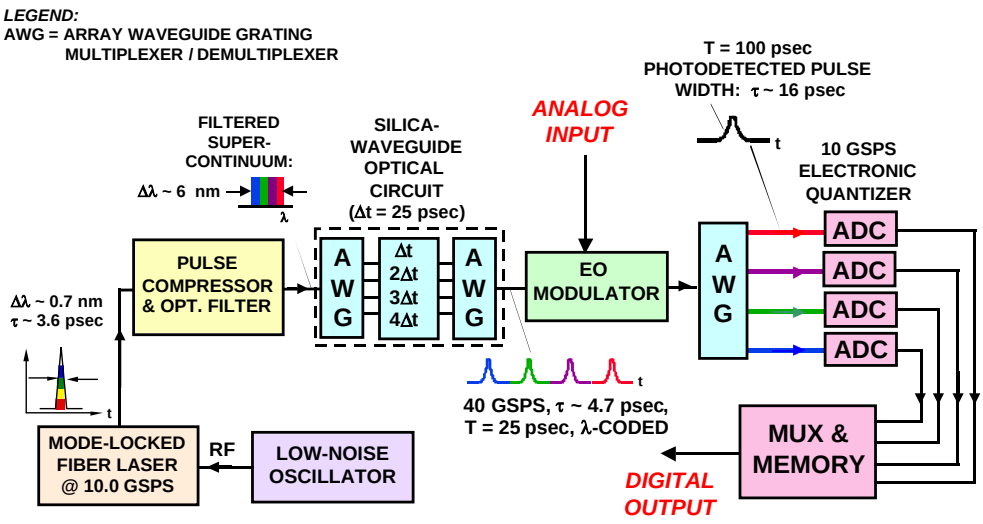


Fig. 1.6 Schematic of 40 GSPS WDM Time-Interleaved ADC system, showing the generation of 40 GHz wavelength-coded pulses for photonic sampling, and its demultiplexing into four parallel ADC channels, each clocked at 10 GSPS.

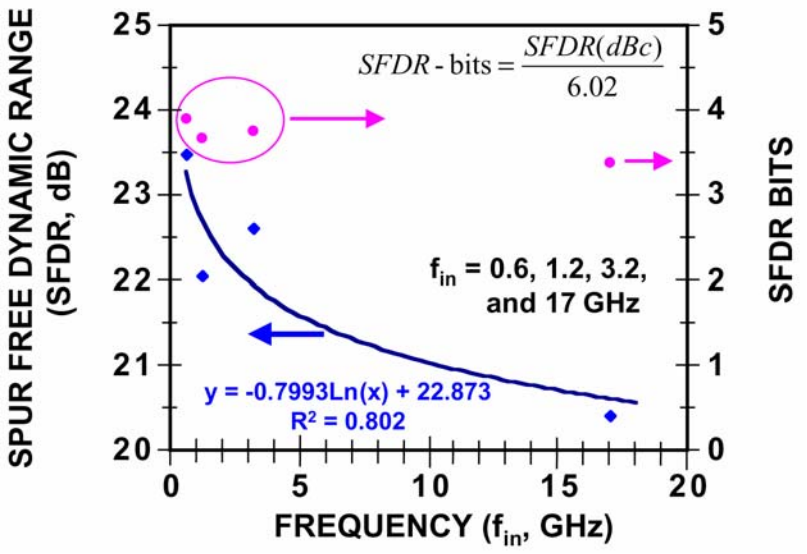


Fig. 1.7 Measured spur free dynamic range (SFDR) and estimated SFDR-bits obtained for 40 GSPS photonic time-interleave ADC, vs frequency of the analog signal-input.

1.C Organization of the Final Report

To support the objectives/demonstrations described in the last Section , we had organized our technical effort into several major tasks. The rest of this Report is organized into Sections that describe, in further detail, the results and accomplishments obtained in each of these tasks. Specifically, the Tasks and Sections corresponding to their description are:

1. Evaluation of Photonic Sampling for A/D Conversion (Section 2): Under this task, we characterized the amplitude- and timing-jitter of a mode-locked (ML) Er-fiber laser. Using a 10 GHz digitizer with 8-bits of resolution, we also demonstrated spur free dynamic ranges (SFDR) of ~48.5 dB (over a Nyquist bandwidth Δf_{NQ} of 5 GHz) in photonic sampling experiments, where multiple analog inputs at L band (1 – 2.6 GHz) were fed to a pair of $LiNbO_3$ EO modulators. These results corresponded to an A/D CONVERSION resolution of ~ 8 SFDR-bits at 10 GSPS (over a Δf_{NQ} of 5 GHz). Finally, we demonstrated, under this task, the use of "instantaneous companding" to correct for third-order distortions generated by a Mach-Zehnder (MZ) EO modulator.

2. Development of $LiNbO_3$ modulators with Enhanced Linearity for Photonic Sampling (Section 3): Under this task, we developed velocity-matched Y-fed directional coupler modulators (YFDC) with a modulation bandwidth in excess of 15 GHz. We discussed the advantages of employing these modulators for enhanced SFDR and SNR in a photonic ADC system. Extensive modeling was also accomplished to study the impact of fabrication variances on the DC-transfer characteristics and intermodulation products measured for the YFDC modulators.

3. Photonic Bandpass ΔΣ InP-HBT ADCs (Section 4): Under this task, we designed and fabricated 10 GHz continuous-time ADCs that demonstrated ΔΣ-passbands located in the frequency range of 1.5–2 GHz. In particular, we demonstrated the direct sampling of 12 GHz analog-inputs for photodetected signals derived from a modulated 10.24 GHz ML optical pulse train.

4. Demonstration of 40 GSPS Photonic Time-Interleaved Architecture (Section 5): In this task, we demonstrated a 40 GSPS photonic time-interleaved architecture that were based on wavelength division multiplexed (WDM) technologies. Here, we demultiplexed 40 GHz λ-coded pulses into four parallel channels, each comprised of 10 GSPS electronic quantizers, to achieve ~4 SFDR-bits.

5. Optical Clock Distribution and InP-HBT Flash Quantizer Development (Section 6): In this task, we demonstrated the distribution of optical clock signals to remoted InP-HBT OEIC quantizers of the 3-4 bits flash design. We also demonstrated an electrical Nyquist 4-bit flash ADC that was clocked at 10 GSPS.

SECTION 2

EVALUATION OF PHOTONIC SAMPLING FOR ANALOG-TO-DIGITAL CONVERSION

In this Section, we present our results on the evaluation of photonic sampling for analog-to-digital conversion. In Sections 2.A.1 and 2.A.2, we describe two approaches for evaluating the jitter of mode-locked (ML) pulses generated by our Er-fiber laser. This will be followed by a description (Section 2.A.3) on the characterizations of the absolute phase noise in the Er-fiber laser, as it was mode-locked (at 10.24 GHz) by a sapphire-loaded cavity resonator (SLCR) oscillator. Using an ultra-stable SLCR oscillator to mode-lock the fiber laser, we present some of the lowest phase noise ever reported for ML lasers. We then describe (in Section 2.B) the application of our ML pulse train to the photonic sampling of analog signals in the multi-GHz frequency range. In particular, we present the demonstration of 8 spur-free-dynamic-range (SFDR) bits, at 10 GSPS, for the photonic sampling of multiple analog input signals that lied in the L-band (1-2.6 GHz). Finally, in Section 2.C, we describe the digital linearization of photonic sampling links, via the application of "instantaneous companding" to the time-domain data obtained with our ML pulse train. The results presented in Section 2.C constitute the first report of digital linearization for photonic sampling links carrying analog-inputs at multi-GHz frequencies.

2.A Evaluation of the Timing and Amplitude Jitter in ML Fiber Laser

In this Section, we present a detailed discussion[3] on the evaluation of jitter in our ML laser. Specifically, the laser characterized was an actively mode-locked Er-Yb fiber-ring laser that emitted at the wavelength λ of ~1540 nm. In this laser, the timing-synchronization for its mode-locking was derived from a Mach-Zehnder (MZ) modulator that formed part of the ring. During mode-locking, the MZ modulator was driven with an external microwave synthesizer that delivered an RF-signal at the mode-locking frequency f_m of ~ 10 GHz. Finally, a phase-lock-loop was installed in the ring to maintain long-term synchronization between the laser and its drive oscillator.

In Sections 2.A.1 and 2.A.2, we compare the performance of the fiber-laser as it was mode-locked with RF-inputs derived from two different microwave synthesizers. Section 2.A.1 presents a characterization of the ML laser's phase noise via the use of a microwave phase-noise test set. We then present, in Section 2A.2, an evaluation of its amplitude and timing jitter via a characterization[4]-[5] of the "noise-pedestals" present in the harmonics of the ML pulse train. Finally, Section 2.A.3 describes our characterization of the ML fiber laser's absolute phase noise, as it was mode-locked by an ultra-stable sapphire-loaded cavity resonator oscillator at f_m = 10.24 GHz.

2.A.1. Measurement of the Single Sideband Phase Noise with a Microwave Phase Noise Test Set

In this first approach, we measured the phase-noise (ϕ-noise) of the ML laser with a microwave phase-noise test set (Aeroflex PN9000). During these measurements, the fiber laser was mode-locked at $f_m \sim 10$ GHz. We also monitored the ML pulse train continuously with an autocorrelator and an optical spectrum analyzer (OSA) during the course of the experiment. The autocorrelator trace of Fig.2.1a shows that the full width at half maximum (FWHM) of our ML pulses was ~3 psec. Its corresponding spectral width, measured simultaneously with an OSA, was ~0.8 nm (see Fig.2.1b). Thus, the time-bandwidth product of our pulses came close to the transform-limited product (for a $sech^2$-pulse) of 0.31. As shown in Fig.2.1b, we can resolve, with the help of a high resolution (res. = 0.05 nm) OSA, optical modes that were spaced precisely by the mode-locking frequency of 10.24 GHz (~0.081 nm).

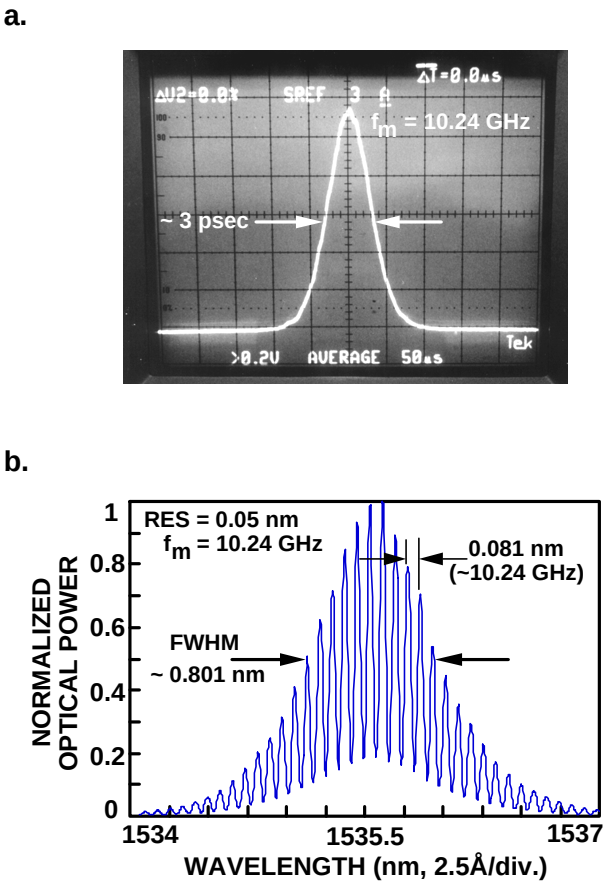


Fig. 2.1 a. Autocorrelation trace of optical pulse emitted by ML fiber laser b. Optical spectrum of ML pulses emitted by fiber laser.

In the phase-noise test set, we compared the ϕ-noise of the detected optical pulses with that of a calibrated reference oscillator. Specifically, the signal arm and reference arm (locked via a phase-lock-loop) were mixed at phase-quadrature in the test set. This mixing enabled a phase-

discriminator to be formed in the RF-regime. The IF-output of the mixer was subsequently sent to a low-pass filter, from which we obtained a baseband signal for RF-spectral analysis. Using a calibrated demodulation factor (in V/rad), one can now measure and compute the single-sideband (SSB) phase-noise [L(f) in dBc/Hz] of the signal. We show, in Fig.2.2, the measured L(f) of: (i) two microwave sources (Oscillators 1 and 2) used to drive the ML laser, and (ii) the first harmonic in the detected optical pulses, as the laser was mode-locked successively via Oscillators 1 and 2. Oscillator 1 was a commercial synthesizer (2 –18 GHz), and Oscillator 2 was a crystal-multiplied oscillator we obtained from Raytheon Electronics Systems. During the measurement, we used a high speed PIN photodiode (bandwidth > 20 GHz) to detect the ML pulse train. In addition, a 6 – 18 GHz low noise amplifier (LNA) with a low noise figure (NF) of 2 dB was used to amplify the photodetected first harmonic of the ML pulse train, after it was filtered out (from other harmonics), via the use of an RF bandpass filter. The DC photocurrents (I_{dc}) used for the L(f) measurements, presented as plots 2 and 4 of Fig.2.2, were both $I_{dc} \sim 0.53$ mA. Using the above photoreceiver and I_{dc} enabled the dynamic range of our photoreceiver to be set, at its lower bound, by shot noise. As discussed in ref. 6, this choice of measurement conditions provides an optimal signal level for characterizing laser noise.

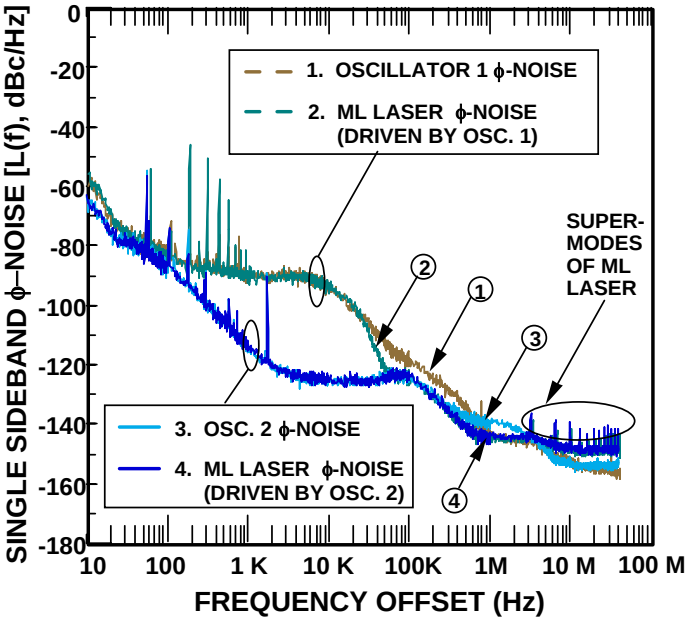


Fig. 2.2 Single sideband phase-noise (L(f)) of ML fiber laser and its drive oscillators: Upper traces: L(f) pertaining to mode-locking with Oscillator 1, Lower traces: L(f) pertaining to mode-locking with Oscillator 2.

From Fig.2.2, we see that the single sideband phase-noise measured for the ML fiber laser tracked closely the phase noise of its drive oscillators for frequency offsets (Δf) less than 3.23 MHz. For $\Delta f > 3.23$ MHz, the ML laser introduced a series of supermode spikes[7] that were spaced $\Delta f_{SM} = 3.23$ MHz apart, as determined by the inverse of the round-trip time in the laser's ring-cavity. By computing the integral:

$$\sigma_{Jt} = \frac{1}{(2\pi f_m)} \sqrt{2\int_{\Delta f_L}^{\Delta f_H} L(f)df} \qquad (2.1)$$

one can now estimate σ_{Jt}, the timing jitter of the picosecond pulse train. Using an integration range of Δf_L = 100 Hz and Δf_H = 40 MHz, we obtained a σ_{Jt} ~72.4 fsec and σ_{Jt} ~14.9 fsec, respectively, for the mode-locking accomplished via Oscillator 1 and Oscillator 2. The lower limit Δf_L of our integration range was set by the long-term time (ΔT) stability ($\Delta T \sim 1/(\sqrt{2}\pi\Delta f_L)$) of interest to our applications. The upper limit of integration Δf_H was determined by the maximum Δf of measurement in the Aeroflex PN9000. For Oscillator 2, the above timing jitter of 14.9 fsec corresponds to a percentage jitter σ_J of 0.0153% for a pulse period (T_m) of 97.656 psec, where $T_m = f_m^{-1}$. The above results also show that the timing-jitter of our ML fiber laser was set primarily by the phase noise in its drive oscillators. To compare our result with the timing jitter reported in ref. 8, where a similar approach was used to evaluate L(f), we also estimated σ_{Jt} for the integration range of Δf = 100 Hz - 1 MHz, for the mode-locking accomplished via Oscillator 2. As noted above, our harmonically ML fiber laser did not have any supermodes in this narrower Δf -range. Here, we obtained a σ_{Jt} of ~10.3 fsec, which was comparable to the jitter of ~ 9.9 fsec that ref. 8 reported, for precisely the same integration range.

While the use of Δf_L = 100 Hz (for Eq. 2.1) provided an estimation of σ_{Jt} that was of direct relevance to our application, we also integrated L(f) from a lower Δf_L of 10 Hz (to different values of Δf_H), to accomplish additional comparison with other published results. For our mode-locking with Oscillator 2, we note that L(f) decreased at a rate ~ $1/f^n$, where $n \geq 2$, for the first two decades of measurement (Δf = 10 Hz - 1 KHz, see Fig.2.2). Therefore, we expect the integrated timing-jitter from the first decade (of Δf = 10 Hz - 100 Hz) to dominate over that derived from the second decade. Taking into account the integrated timing jitter (of ~ 28.3 fsec) from this first decade, we obtained (via Eq. 2.1) a σ_{Jt} ~ 31 fsec for Δf_L = 10 Hz and Δf_H = 40 MHz, the full Δf-range of our L(f) measurement. To accomplish a precise comparison with the residual timing jitter reported in ref. 9 (f_m = 9 GHz), we also integrated L(f) over the Δf-range of 10 Hz to 10 MHz. Over this particular integration range, the absolute jitter of σ_{Jt} = 30.58 fsec estimated for our ML laser was slightly lower than the residual jitter of 37 fsec published in ref. 9.

2.A.2. Jitter Evaluation via the Harmonic Approach

Next, we applied the technique of harmonic analysis [Ref. 4, 5] to evaluate the amplitude and timing jitter. While the mixer/phase-detector approach (presented in Section 2.A.1) used in commercial phase noise test-sets (such as the Aeroflex PN 9000 adopted in this work) provides the most accurate characterization of phase noise, the harmonic approach described in this section involves simpler measurement instrumentation. To characterize the amplitude and timing jitter of a laser mode-locked at f_m ~ 10 GHz, one only needs to acquire: a photodetector that has the bandwidth to detect a few harmonics of the ML pulse train (e.g. $4f_m$ ~ 40 GHz), and an RF spectrum analyzer (RFSA) capable of measuring the photodetected harmonics. As we

will show, this approach provides good agreement with the results (for σ_J) obtained via a phase noise test set, once the noise pedestals of a few harmonics are characterized, and modeled via the relationship between the pedestal power (in dBc/Hz) and harmonic-order (see Equation 2.4 below). As such, it is valuable as a simple approach for evaluating the amplitude and timing jitter of a ML laser.

As mentioned above, we examine the noise pedestals present in the detected harmonics of the ML pulse train. One can write the ML pulse train [with fractional timing jitter J(t) and relative amplitude jitter A(t)] as:

$$G(t) = (1 + A(t))G_o(t) + G_o^{/}(t)J(t)T_m \tag{2.2}$$

where $G_o(t) = \sum_n g(t - nT_m)$ denotes a train of perfect (i.e. jitter-less) periodic pulses ($T_m = 1/f_m$), and G_o'(t) its time-derivative. If the Fourier transform of an individual pulse [g(t)] is $\tilde{g}(\omega)$, where $\omega = 2\pi f$, then the power spectrum $S_G(\omega)$ of G(t) can be obtained[4] from a Fourier transform of its autocorrelation function. Specifically, $S_G(\omega)$ is given by:

$$S_G(\omega) = \left| \frac{2\pi \cdot \tilde{g}(\omega)}{T_m} \right|^2 \sum_N \{\delta(\omega - N\omega_m) + S_A(\omega - N\omega_m) + (2\pi N)^2 S_J(\omega - N\omega_m)\} \tag{2.3}$$

where $\omega_m = (2\pi)/T_m$, and N is the harmonic-number of the ML frequency f_m. In Equation 2.3, $S_A(\omega)$ and $S_J(\omega)$ are, respectively, the spectral densities of the amplitude jitter A(t) and timing jitter J(t). When we characterize the RF spectrum of the detected harmonics with a microwave spectrum analyzer, the above spectral densities are integrated over the resolution bandwidth (RBW) of the measurement. Therefore, the relative power between the peak ($P_p(0)$) of the "pedestal" for the Nth harmonic and its carrier (P_c), the Nth harmonic, is given by the following equation:

$$\frac{P_p(0)}{P_c} = RBW \cdot \{S_A(0) + (2\pi N)^2 S_J(0)\} \tag{2.4}$$

In the Equation 2.4, $S_A(0)$ and $S_J(0)$ denote, respectively, the spectral densities of the amplitude and timing jitter at the harmonic frequencies of $\omega = N\omega_m$. From Eq. 2.4, we notice that the power (relative to its carrier) for the pedestal of the Nth harmonic consists of two components: (i) a component due to the amplitude jitter that is invariant with the harmonic number N, and (ii) a second component due to the timing jitter that varies as the square of N. Hence, the slope obtained from a plot of ($P_p(0)/P_c$) vs N^2 gives us an estimation of $S_J(0)$. The square of the fractional timing jitter, $\sigma_J^2 = \langle J^2(t) \rangle$, can now be estimated from the product $S_J(0)$ x (FWHM of the pedestals). Finally, we can evaluate $S_A(0)$ via an integration of the noise spectrum measured at low frequencies (i.e., for N = 0).

Fig.2.3 and Fig.2.4 show the RF spectrum measured for the first four harmonics of our fiber laser (f_m ~ 10.24 GHz) as it was mode-locked, respectively, by Oscillators 1 and 2. As we recall from Section 2.A.1, Oscillator 1 exhibited a higher phase noise, over the offset frequency range of Δf = 100 Hz to Δf = 1 MHz, than Oscillator 2 (see Fig.2.2). That Oscillator 2 was a "quieter" oscillator was reflected by the fact that we needed to drop the noise floor of our measurement – via a lowering of the RBW – before its noise pedestals could be characterized. Specifically, the noise-pedestal data were taken at a RBW of 1 kHz for Oscillator 1 (Fig.2.3), and a RBW of 100 Hz for Oscillator 2 (Fig.2.4). As shown, the noise pedestals for the harmonics of the ML pulses were noticeably smaller - in both magnitude and FWHM - for the mode-locking accomplished via Oscillator 2.

We evaluated the ratio ($P_p(0) / P_c$) from these data, and plotted them (in dBc/Hz) vs the harmonic number N in Fig. 2.5. From the $S_J(0)$ evaluated, we estimated a fractional timing jitter of $\sigma_J \sim 7 \times 10^{-4}$ and $\sigma_J \sim 10^{-4}$ respectively for Oscillators 1 and 2. For both oscillators, the above σ_J value was in good agreement with that obtained via an integration of L(f) (see Section 2.A.1). We summarize, in Table 2.1, the results of our jitter evaluation from the two approaches.

Table 2.1 Comparison of the Timing Jitter (J, Jt)* and Amplitude Jitter (A)* evaluated from (i) L(f) and (ii) Harmonic Analysis

f_m ~ 10 GHz (T_m ~ 100 psec)	σ_J and σ_{Jt} (in fsec) from L(f)**	σ_J and σ_{Jt} (in fsec) from Harmonic Analysis	σ_A from Harmonic Analysis
Mode-locking with Oscillator 1	$\sigma_J \sim 7.4 \times 10^{-4}$ (σ_{Jt} ~ 72.4 fsec)	$\sigma_J \sim 7 \times 10^{-4}$ (σ_{Jt} ~ 70 fsec)	$\sigma_A \sim 2.3 \times 10^{-3}$
Mode-locking with Oscillator 2	$\sigma_J \sim 1.53 \times 10^{-4}$ (σ_{Jt} ~ 14.9 fsec)	$\sigma_J \sim 1 \times 10^{-4}$ (σ_{Jt} ~ 10 fsec)	$\sigma_A \sim 3.84 \times 10^{-4}$

* $\sigma_J = \sqrt{\langle J^2(t) \rangle}$, $\sigma_{Jt} = \sigma_J \cdot T_m$, $\sigma_A = \sqrt{\langle A^2(t) \rangle}$

**Evaluated from the integration of L(f) over the offset frequency (Δf) range of Δf=100 Hz to Δf =40 MHz (see Section 2.A.1).

The σ_J estimated via the approach of harmonic analysis was slightly lower than that obtained from L(f). This small difference could be due to slight inaccuracies in the characterization of the noise pedestals as their RF-power levels approached the noise floor of the RF spectrum analyzer. This, in turn, led to a small underestimation of the product $S_J(0)$ x (FWHM of the pedestals). Finally, we evaluated the corresponding ratios for the amplitude jitter from the low-frequency noise spectrum, and marked them as the amplitude noise floor in Fig. 2.5. The integration of this noise spectrum gave a value of σ_A = 0.23% (Oscillator 1) and σ_A = 0.0384% (Oscillator 2) for the fractional amplitude jitter σ_A, where $\sigma_A = \sqrt{\langle A^2(t) \rangle}$.

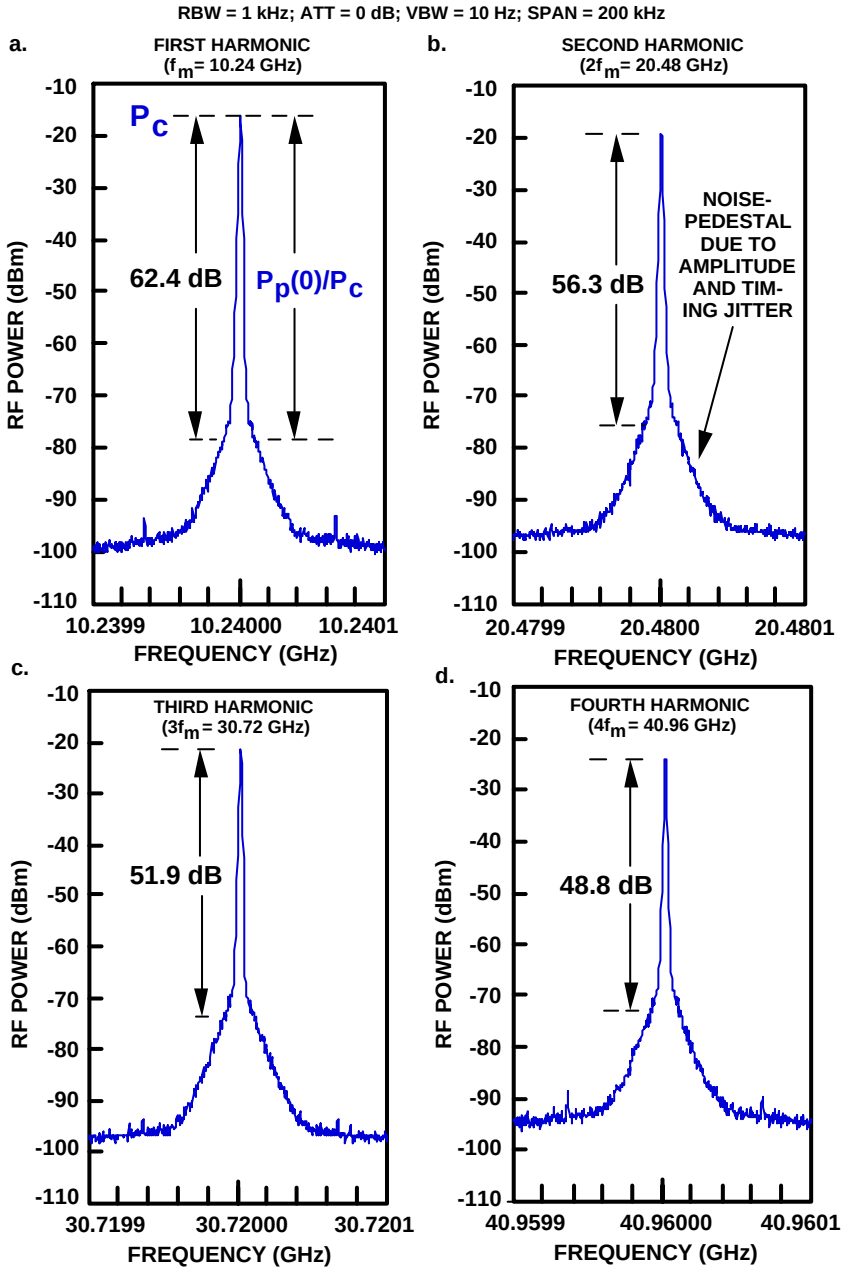


Fig. 2.3 RF spectrum (RBW = 1 kHz, frequency span = 200 kHz) of the first four harmonics [(a)-(d)] from the ML pulse train (f_m~10.24 GHz), observed during mode-locking with Oscillator 1.

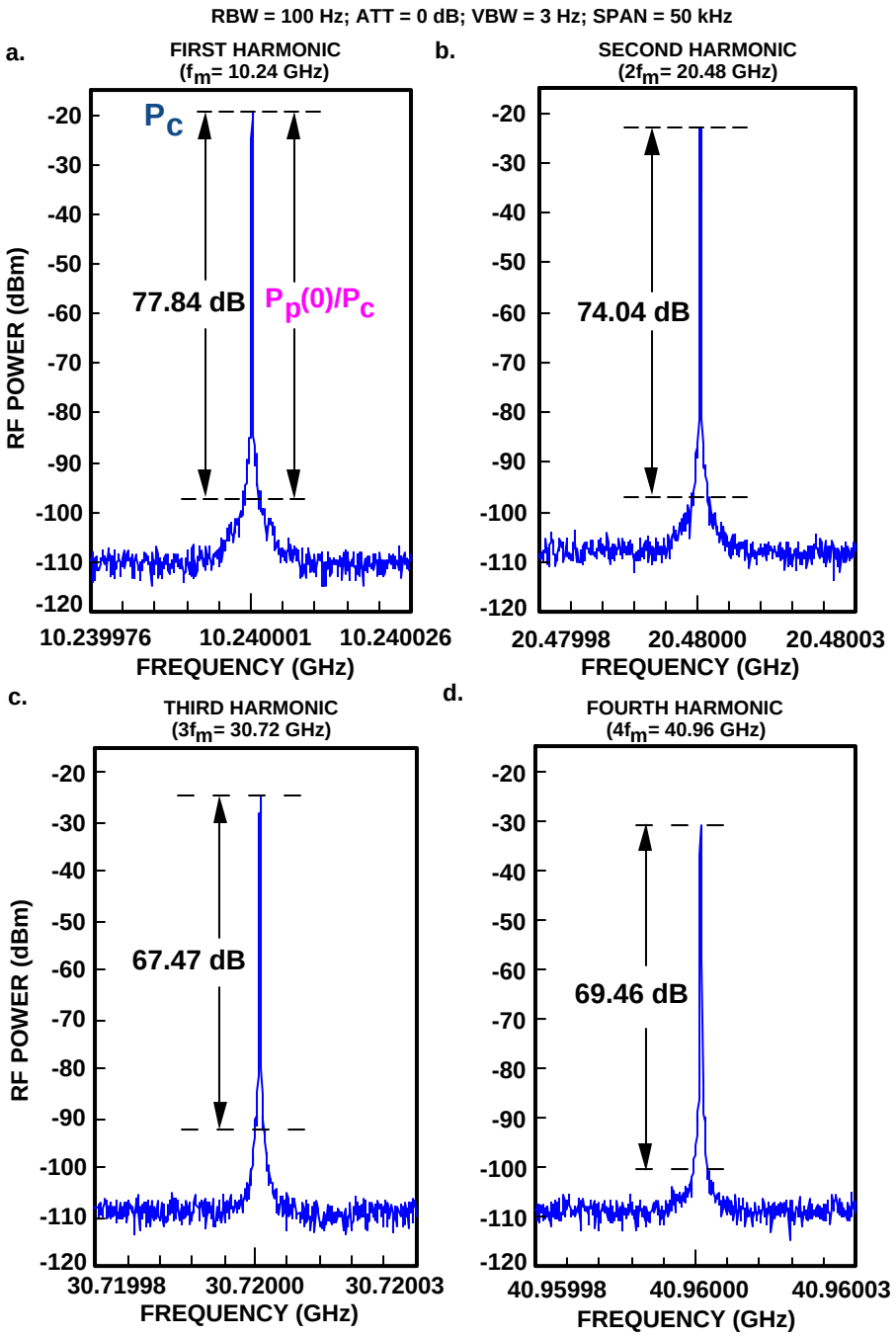


Fig. 2.4 RF spectrum (RBW = 100 Hz, frequency span = 50 kHz) of the first four harmonics [(a)-(d)] from the ML pulse train (f_m~10.24 GHz), observed during mode-locking with Oscillator 2.

Although our phase noise test set can only measure L(f) for frequency offsets Δf (from the mode-locking frequency f_m) that were less than 40 MHz, one can obtain an estimate of the timing-jitter, over the Nyquist frequency range of 5.12 GHz, via an extrapolation. For the mode-locking with Oscillator 2, we can assume, for example, that the supermode amplitudes in the

extrapolated Δf range of 40 MHz – 5.12 GHz frequency range were given, in the worst case, by the largest supermode we had recorded in the Δf-range of 10 Hz to 40 MHz. According to the L(f) data presented in Fig.2.2, this highest supermode SM1 occurred at the offset frequency of Δf = 3.23 MHz, and its amplitude was $L(f)_{SM1}$ = –136.09 dBc/Hz. We used this value of $L(f)_{SM1}$ as the extrapolated amplitude for the supermodes in the Δf-range of 40 MHz to 5.12 GHz, along with a L(f) noise-floor of ~ –149.2 dBc/Hz. Specifically, we performed an integration (according to Eq. 2.1) for an extrapolated L(f) that consisted of supermodes - with amplitudes and spectral-widths identical to SM1 – rising every 3.23 MHz above a flat L(f) floor of –149.2 dBc/Hz. Hence, the contribution to the integration in the extrapolated Δf-range came from both the extrapolated supermode spikes and the assumed L(f) noise-floor of –149.2 dBc/Hz. Using Eq. 2.1, we obtained, for Oscillator 2, a σ_{Jt} of 69 fsec for an integration range with Δf_L = 100 Hz to Δf_H = 5.12 GHz, the Nyquist bandwidth. Similarly, for Oscillator 1, we obtained a σ_{Jt} of 102.26 fsec over the Nyquist bandwidth of 5.12 GHz.

Using the above σ_{Jt}, one can now estimate[1] the bits of resolution that can be supported, during photonic sampling, by this low-jitter picosecond pulse train. Specifically, to achieve Q-bits of resolution, the fractional timing-jitter σ_J and the fractional amplitude-jitter σ_A must satisfy, respectively, $\sigma_J < 1/(\pi 2^Q)$ and $\sigma_A < 1/(2^Q)$. Using this criteria, we estimate that the 10 GHz ML pulse train generated by our laser can support (over a Nyquist bandwidth of ~5 GHz), a photonic sampling accuracy of ~ 8.8 bits with Oscillator 2, and ~ 8.3 bits with Oscillator 1 respectively.

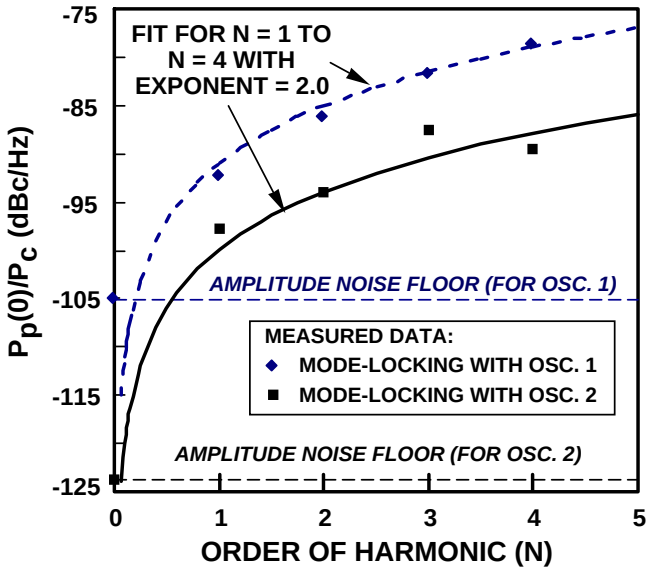


Fig. 2.5 Relative pedestal power (in dBc/Hz) vs harmonic order for mode-locking accomplished with Oscillators 1 and 2. The dashed and solid traces are derived from least square fits (with exponent = 2.0) for the harmonics N=1 to N=4. The amplitude noise floors of the ML pulses are also indicated.

2.A.3. Evaluation of the Absolute Phase Noise in Fiber-Laser Modelocked by Sapphire-Loaded Cavity Resonator Oscillator at 10.24 GHz

There had been several reports[9]-[10] in other PACT Programs on the characterizations of phase noise in fiber- or diode-lasers ($\lambda \sim 1550$ nm) that were actively mode-locked by ultra-stable oscillators at $f_m \sim 9$ GHz. In particular, these oscillators utilized[11] ultra-high Q (Q of ~ 10^5) sapphire-loaded cavity resonators (SLCR) to achieve low phase noise at their oscillation frequencies. As a microwave source, these SLCR oscillators[11] have demonstrated some of the lowest phase noise ever reported. Therefore, mode-locking the above lasers with SLCR oscillators allows one to investigate the state-of-the-art limitations on the lasers' phase noise and timing-jitter. However, the previous measurements[9]-[10] were all residual phase noise characterizations that reported the laser's phase noise in excess of the SLCR oscillator driving it. In this Section, we describe the first absolute phase noise characterizations of a fiber laser ML by a SLCR oscillator[12]. In particular, we compare the results obtained at the mode-locking frequency (f_m) of 10.24 GHz from two experimental arrangements. To accurately characterize the single sideband phase noise [L(f)] of our ML fiber laser, we employed: (i) a second SLCR oscillator[11] as an ultra-low noise downconverter, and (ii) a calibrated phase noise test set Aeroflex PN 9000[13], with reference signals (at the much lower frequencies of 40 MHz or 1.24 GHz) that possessed low phase noise characteristics. Our choice of measurement schemes enabled us to report an absolute timing-jitter σ_{Jt} that was as low as 2.48 fsec over an integration range of $\Delta f = 100$ Hz – 1 MHz, a frequency-offset (Δf) span where supermodes were absent in our ML laser. For the Δf-range of 10 Hz – 10 MHz, where we took into account the contributions of measured supermodes to σ_{Jt}, we estimated a timing-jitter that was ~1/3 the residual jitter reported in ref. 9.

The fiber laser ($\lambda \sim 1540$ nm) mode-locked by the 10.24 GHz SLCR oscillator (SLR1) was described in Section 2.A.1. In a first set of measurements (see Figure 2.6), we used the second SLCR oscillator (SLR2 at 9 GHz) to downconvert the 10.24 GHz harmonic of the mode-locked pulses to a lower IF frequency of 1.24 GHz. The use of another SLCR oscillator - of equivalent stability to SLR1 - for RF-downconversion enabled us to: (i) minimize any corruption of the signal's phase noise by commonplace downconverters that exhibit L(f) inferior to SLR1 or SLR2, and (ii) obtain a lower IF frequency of 1.24 GHz, where oscillators with low phase noise are available to serve as a reference [i.e. as the local oscillator (LO) signal] for the phase noise test set. As shown in Fig.2.6a, we first filtered out, using a bandpass (BP) filter, the photodetected first harmonic of the ML pulse train. After downconversion, the 1.24 GHz IF signal was fed to the R-input of the PN9000, where it was mixed with a reference oscillator (fed to the L-input) at the same frequency, but locked at quadrature. The phase-lock loop for the L(f) characterization was completed by feeding a tuned voltage-output from the PN9000 to the voltage-controlled oscillator input of SLR2. Fig.2.6b shows the result of our L(f) measurements. As shown, the phase noise of the fiber laser tracked closely that of SLR1 - measured with similar downconversion arrangements - until an offset frequency Δf of 5 MHz. For $\Delta f > 5$ MHz, the L(f) for SLR1 was measured to be ~-148 dBc/Hz, whereas the ML laser's L(f) was ~ 6-7 dB higher. Here, the excess phase noise due to the mode-locking, coupled with contributions from the phase-components of the shot noise and thermal noise (due to an extra pre-amplifier used in

the ML laser's characterization), combined to yield a higher L(f) for the laser. Finally, we estimated σ_{Jt} via an integration of L(f), using Equation 2.1 (shown also as an inset to Fig.2.6b). From the set of data shown in Fig.2.6b, we obtained: (i) for the integration range of Δf_L = 100 Hz to Δf_H = 1 MHz, a σ_{Jt} of ~ 3 fsec, and (ii) for the integration range of Δf_L = 100 Hz to Δf_H = 40 MHz, a σ_{Jt} of ~ 11.3 fsec. In particular, we made the observation that the minimal L(f) one could measure using this downconversion arrangement was limited by the phase noise of the 1.24 GHz LO reference. In fact, a plot of L(f) for the 1.24 GHz LO tracked closely that measured for SLR1 (Curve 1 of Fig.2.6b). To characterize more accurately the ML laser's close-in phase noise, we performed an extra step of downconversion in a second experimental arrangement.

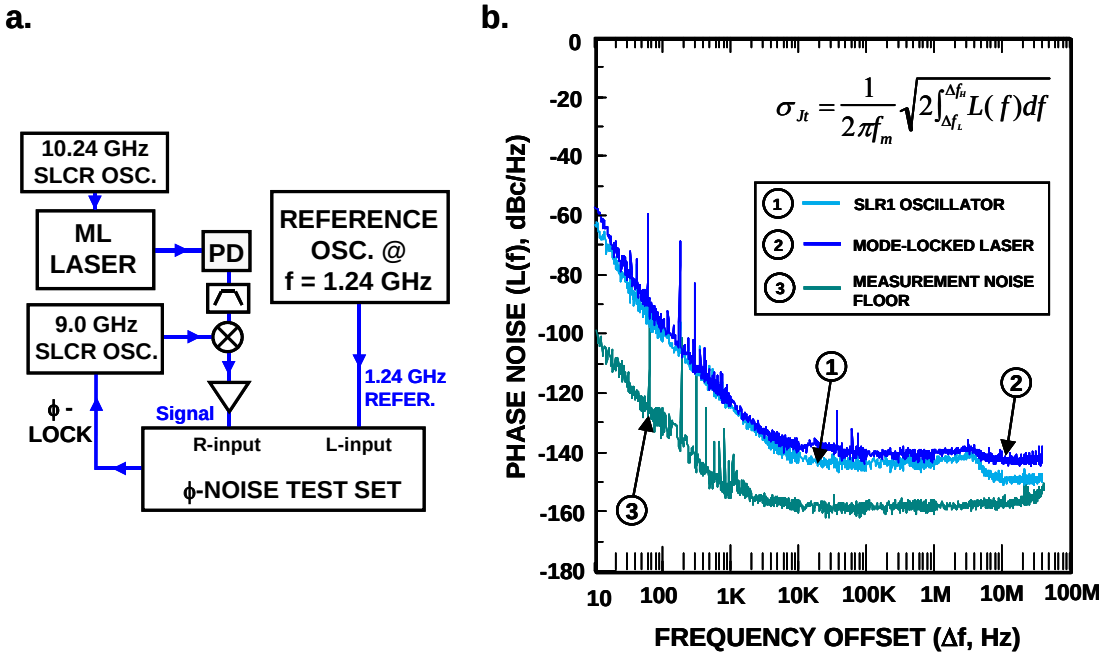


Fig. 2.6 a. First experimental arrangement for characterizing the phase-noise of fiber laser actively mode-locked by the SLR1 oscillator. b. Measured single sideband phase noise [L(f)] of SLR1 oscillator (curve 1) and ML fiber laser (curve 2), using the experimental arrangement of Fig. 6a.

In this second set of measurements, we used a 1.28 GHz output derived from Oscillator 2 (see Section 2.A.1) as a second downconverter. Fig.2.7a shows this second measurement setup. As illustrated, we mixed the 1.28 GHz downconverter output with the 1.24 GHz IF, formed as described above. This second stage of downconversion enabled us to use a even lower LO frequency of 40 MHz as the reference during our phase noise characterization. In particular, we expected the reference oscillator's 40 MHz output to demonstrate even lower close-in phase noise than its 1.24 GHz output (which was used as the LO reference in Fig.2.6a). Fig.2.7b shows the L(f) thus measured. As shown, we measured an L(f) for the ML laser (Curve 2) that was at least 5 dB lower (for Δf < 1 kHz), when compared with data (Curve 4) obtained via the first measurement approach. For this data, over an integration range of Δf_L = 100 Hz to Δf_H =

1 MHz, we estimated an absolute timing-jitter σ_{Jt} of only 2.48 fsec. Over a wider integration range of Δf_L = 100 Hz to Δf_H = 40 MHz, the σ_{Jt} estimated, taking into account of supermodes observed, was ~ 14.3 fsec. To compare with other published results, we integrated L(f) from Δf_L = 10 Hz to Δf_H = 10 MHz. Here, we obtained a σ_{Jt} of 11 fsec. This is ~1/3 the residual timing-jitter value of 37 fsec reported in ref. 9, for precisely the same Δf integration-range. When $\Delta f >$ 20 kHz, Fig.2.7b shows that the L(f) measured for the ML laser was higher than that of SLR1 (Curve 1) measured under similar downconversion arrangements. Again, we attribute this to the combined effects of the ML laser's excess phase-noise, its shot-noise, as well as thermal noise derived from the extra pre-amplifiers used in the laser's L(f) characterization.

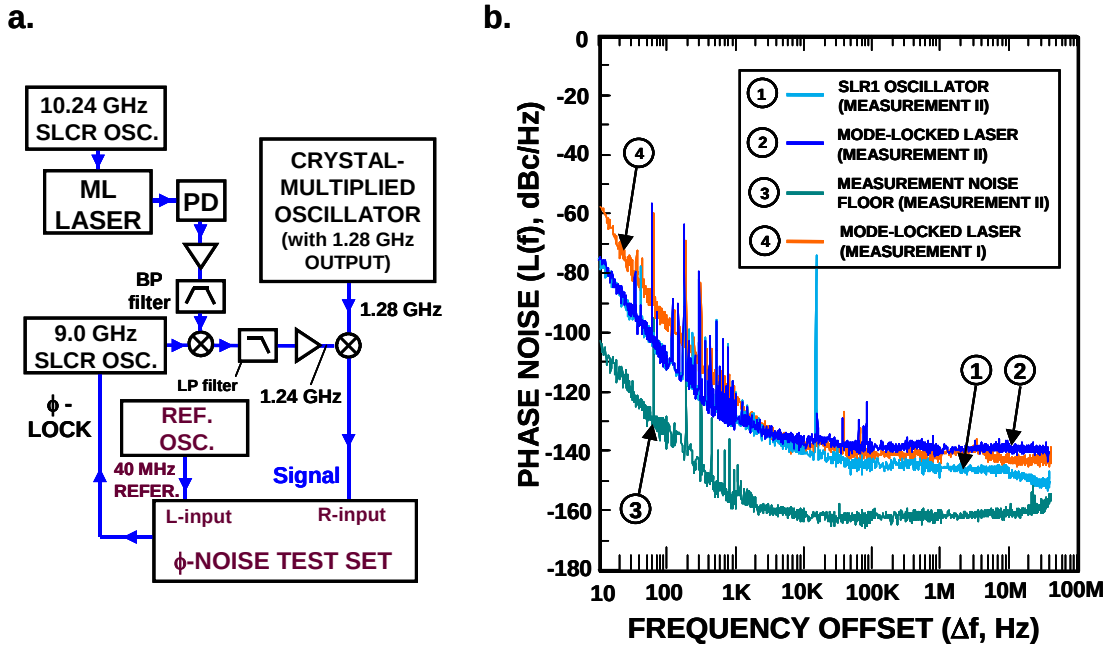


Fig. 2.7 a. Second experimental arrangement for characterizing the phase-noise of fiber laser mode-locked by the SLR1 oscillator. b. Measured L(f) of SLR1 oscillator (curve 1) and ML fiber laser (curve 2), using the experimental arrangement of Fig. 7a. The L(f) of the ML laser obtained, via the measurement setup of Fig. 6a, is replotted as curve 4 for comparison.

Table 2.2 summarizes the estimated timing jitter σ_{Jt} for different ranges of integration (set by Δf_L and Δf_H), and bits of resolution Q that a specific σ_{Jt} supports, based on this second measurement arrangement for L(f).

Table 2.2 Estimated σ_{Jt} and Bits of Resolution Q derived from L(f) for Mode-Locking with SLSR Osc.

σ_{Jt} and bits of resolution (Q)	Δf_H = 1 MHz	Δf_H = 40 MHz
Δf_L = 100 Hz	2.48 fsec (Q = 13.6 bits)	14.3 fsec (Q = 11.1 bits)
Δf_L = 10 Hz	8.28 fsec (Q = 11.9 bits)	16.4 fsec (Q = 10.9 bits)

Finally, after comparing our data with the L(f) of downconverters used in this second measurement setup, we noted that for $\Delta f < 10$ kHz, the L(f) measured (for both SLR1 and the ML laser) are limited by the 1.28 GHz downconverter. Therefore, albeit reporting the lowest σ_{Jt} for an actively ML laser at 10 GHz, the phase noise measured via our two experimental approaches were still limited, in specific Δf-ranges, by the instrumentation used in the characterization.

In summary, we have presented in Section 2.A.3, the results of two measurements for the absolute phase noise of a ML fiber laser driven by a 10.24 GHz SLCR oscillator. By integrating the L(f) measured, we estimated a timing jitter of ~ 2.48 fsec and ~ 14.3 fsec respectively for frequency-offset (Δf) ranges that spanned $\Delta f = 100$ Hz to 1 MHz, and $\Delta f = 100$ Hz to 40 MHz. These L(f) and timing jitter correspond to some of the lowest ever reported. In both measurements, we observed laser phase noise that were in excess of the SLCR oscillators. We attribute this to a combination of excess noise sources, including those due to the mode-locking. Even though we are still limited (in some Δf-ranges of measurement) by the phase noise of the downconverters, the data presented demonstrate how low an absolute timing jitter one can achieve to date for a fiber laser that we actively mode-locked (at $f_m = 10.24$ GHz) with an ultra-stable SLCR oscillator.

2.B. Photonic Sampling for Analog-to-Digital Conversion at 10 GSPS

In this Section, we describe the application of these low-jitter ML pulses to photonic sampling in analog-to-digital conversion. In these experiments (see Fig. 2.8), we modulated the picosecond pulse train with an electro-optic $LiNbO_3$ Mach Zehnder (MZ) modulator that was biased at quadrature. As discussed in Section 2.A.2, these highly stable ML pulses enabled us to accomplish accurate impulse sampling – supporting better than 8 bits of resolution - of an analog-input fed to the MZ modulator. The modulated pulse train was subsequently photodetected, and then sent to an electronic digitizer for quantization, as in a photonic A/D system. In this series of experiments, we utilized a state-of-the-art electronic digitizer that also possessed 8-bits of resolution (at 10 GSPS) as the output stage of our photonic A/D conversion system. As discussed below, this enabled us to demonstrate 8-bits of A/D conversion accuracy at 10 GSPS for the *entire* photonic A/D conversion cascade shown in Figure 2.8. We first describe (in Section 2.B.1) the photonic A/D conversion accomplished for a single analog input (at 2.49 GHz). We then describe (in Section 2.B.2) an experiment where the ML pulse train was *split*, and sent to separate MZ modulators for the *simultaneous* sampling of two analog inputs. As mentioned above, we demonstrated the achievement of 8 SFDR-bits (over the Nyquist bandwidth of 5 GHz) in each case.

2.B.1 Photonic Sampling of an Analog Input at 2.49 GHz

Fig. 2.8 shows a schematic of our photonic sampling experiment.

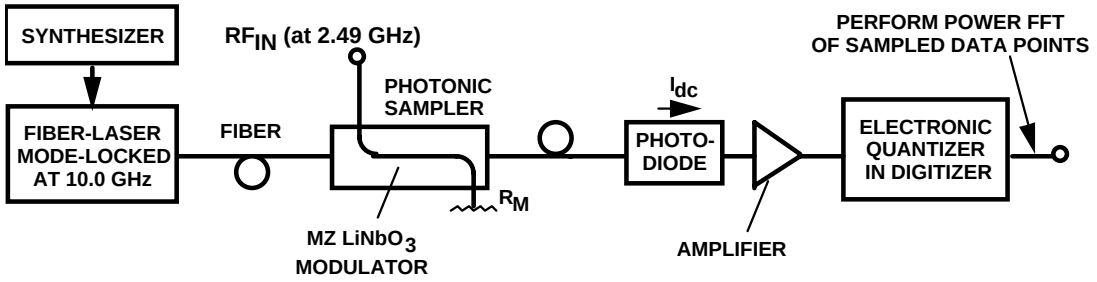


Fig. 2.8 Schematic of photonic sampling experiment (at 10 GSPS) with a 2.49 GHz analog-input to $LiNbO_3$ MZ modulator (photonic sampler).

During this series of experiments, we mode-locked the fiber laser at f_m = 10.0 GHz with Oscillator 1, which offered > 8 bits of resolution, and more flexibility in power/frequency adjustments than Oscillator 2. After photodetection and digitization, we performed a fast Fourier transform (FFT) of the sampled data points taken from the digitizer, which was specified to support 8 SFDR-bits. From the spur free dynamic range (SFDR) of the FFT, one can now estimate the number of SFDR-bits achieved in our photonic A/D conversion system. Specifically, the effective number of bits associated with a measured SFDR is given[(1)] by: SFDR-bits = SFDR (dBc) / 6.02. In the above expression, the SFDR (obtained via the FFT) is defined[(1)] as the ratio of the single-tone signal power to the highest spur (within the RF-spectrum of interest). Fig.2.9 shows the power-FFT of a set of 120,000 data points that we sampled (at 10 GSPS) for the modulator's 2.49 GHz analog input. Since T_m = 100 psec, the record length of our photonic sampling experiment was 12 μsec. As shown in the figure, we obtained a SFDR of ~ 50 dB, which corresponded to ~ 8 SFDR-bits. We have, therefore, demonstrated a resolution of ~8 SFDR-bits (over the Nyquist band of 5 GHz) for the entire cascade in our 10 GSPS A/D conversion system, that encompassed photonic sampling at the front end.

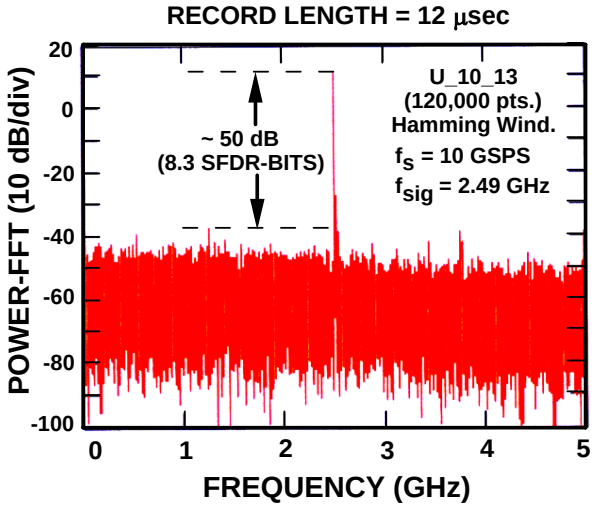


Fig. 2.9 Power-FFT of photonically sampled signal with record length of 12 μsec. The SFDR obtained was ~50 dB, which corresponded to ~8 SFDR-bits at 10 GSPS.

2.B.2 Photonic Sampling of Two Analog Inputs (at 1.1 GHz and 2.49 GHz)

Next, we split the optical output of our mode-locked laser (f_m = 10.0 GHz), and sent the split pulse trains to two $LiNbO_3$ MZ modulators (see Fig.2.10).

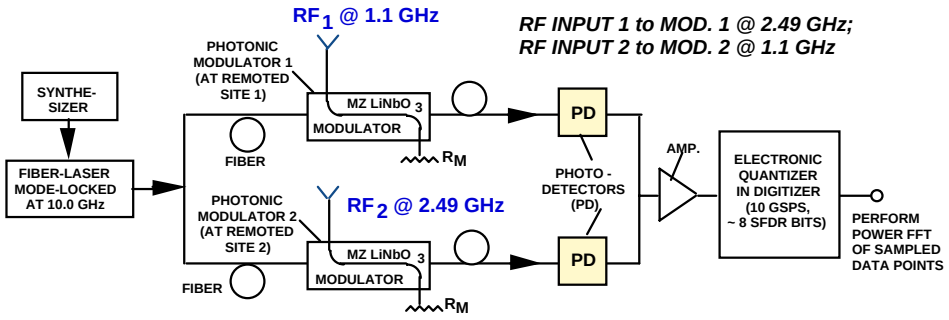


Fig. 2.10 Schematic of photonic sampling experiment (at 10 GSPS) with multiple analog inputs: f_1 = 1.1 GHz to modulator 1, f_2 = 2.49 GHz to modulator 2.

We then applied analog signals at 1.1 GHz and 2.49 GHz, respectively, to the RF-inputs of MZ Modulators 1 and 2. Physically, the two modulators were remoted from the electronic quantizer via lengths of fibers. In a system application, one can envisage the deployment of these photonics modulators at two remoted antenna sites for the tuned reception of targeted RF-signals. Fig.2.11 shows the power-FFT for a sample of 50,000 data points (record length = 5 μsec) that we obtained from the digitizer. As shown, the FFT spectrum displayed the signal components at 1.1 GHz and 2.49 GHz with a SFDR of 48.5 dB, which corresponded to a resolution of ~8 SFDR-bits. In this manner, one can perform a spectral analysis of the RF-signals picked up by an "antenna farm" whose elements are spread over diverse physical locations.

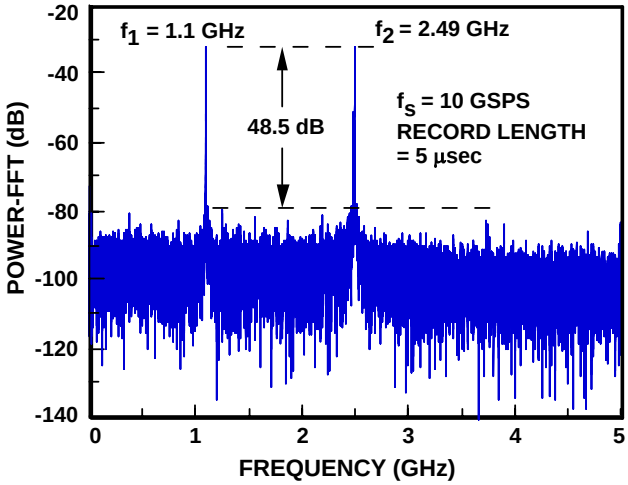


Fig. 2.11 Power-FFT of photonically sampled signals from multiple analog inputs (with record length of 5 μsec). The SFDR obtained was ~48.5 dB, which corresponded to ~8 SFDR-bits at 10 GSPS.

2.C Digital Linearization of Photonic Sampling Links at GHz Frequencies

In the photonic sampling experiments described in Section 2.B, the nonlinearities due to the raised-cosine transfer function of the MZ modulator was not noticeable (above the noise floor of our measurement) because the optical modulation m_{opt} of the picosecond pulse train was kept smaller than 20%. In other applications, two or more strong RF-tones (f_1, f_2) might be present at the analog-input of one MZ modulator (photonic sampler). Third-order harmonics (at $3f_1$ and $3f_2$) and intermodulation products (IM3), at the frequencies ($2f_1 \pm f_2$ and $2f_2 \pm f_1$) could then be generated via the nonlinearity present in the modulator, especially for large m_{opt}. These third order harmonics and intermodulation products constitute distortions that reduce the SFDR of the photonic link. Fortunately, for modulators with a well-modeled transfer function [e.g. the raised-cosine transfer function of a Mach Zehnder (MZ) modulator], one can take advantage of the *time-domain* data obtained via photonic sampling to *digitally linearize*[14] the antenna remoting link. Specifically, one can apply "instantaneous companding" to the sequence of time-domain data obtained via our impulse sampling. As we will demonstrate, this post-processing approach to link-linearization offers a viable alternative to the insertion of a linearized modulator - i.e. an electro-optic modulator with a linearized transfer curve - in place of the MZ modulator for the photonic sampling link (see Section 3 on the development of modulators with enhanced linearity).

The output transfer characteristics of a MZ modulator (with half-wave voltage V_π) can be represented as: $P_{out} = P_{full}\cos^2(\frac{\pi V}{2V_\pi})$, where P_{out} and P_{full} denote, respectively, its optical output (for an input voltage V) and its maximum throughput intensity (at V=0). When biased at quadrature (i.e. $V_{DC} = V_\pi/2$), the photodetected signal $V_{out}(t)$ of the link is given by:

$$V_{out}(t) = \frac{V_{full}}{2}\left[1 - \sin\left(\pi \frac{V_{RF}(t)}{V_\pi}\right)\right] \tag{2.5}$$

where $V_{RF}(t)$ and V_{full} denote, respectively, the modulation voltage on the MZ and the detected signal (voltage) corresponding to P_{full}. Physically, one can see that the RF-input voltage $V_{RF}(t)$ is compressed, especially for large m_{opt}, via the raised-cosine modulation transfer function, so that $V_{out}(t)$ is a slightly distorted version of $V_{RF}(t)$. In the frequency domain, this distortion is exhibited in the form of odd-order harmonics and intermodulation spurs that ultimately limit the SFDR of the link.

Taking advantage of *time-domain* data available via photonic sampling, we now implement - with software algorithms - an "inverse" of the modulation transfer function for *each* sampled voltage $V_{out}(t_n)$ (at time instant t_n) from the link, i.e. we compute $V_{sig}(t_n)$ according to:

$$V_{sig}(t_n) = \frac{V_\pi}{\pi}\sin^{-1}\left[1 - 2\frac{V_{out}(t_n)}{V_{full}}\right] \tag{2.6}$$

Within the modeling accuracy of the raised-cosine transfer function, $V_{sig}(t_n)$ should give us an *undistorted* replica of $V_{RF}(t_n)$. In the frequency domain, one should then be able to eliminate the third-order spurs that would otherwise reduce the link's SFDR. Below, we show that one can indeed take advantage of photonic sampling to correct for distortions generated by the raised cosine transfer function of a MZ modulator.

First, we illustrate, in Fig.2.12a, the FFT of detected signals for a photonic sampling link (see Figure 2.10 for schematic) where there were two strong RF-input tones (f_1 and f_2) to the MZ modulator.

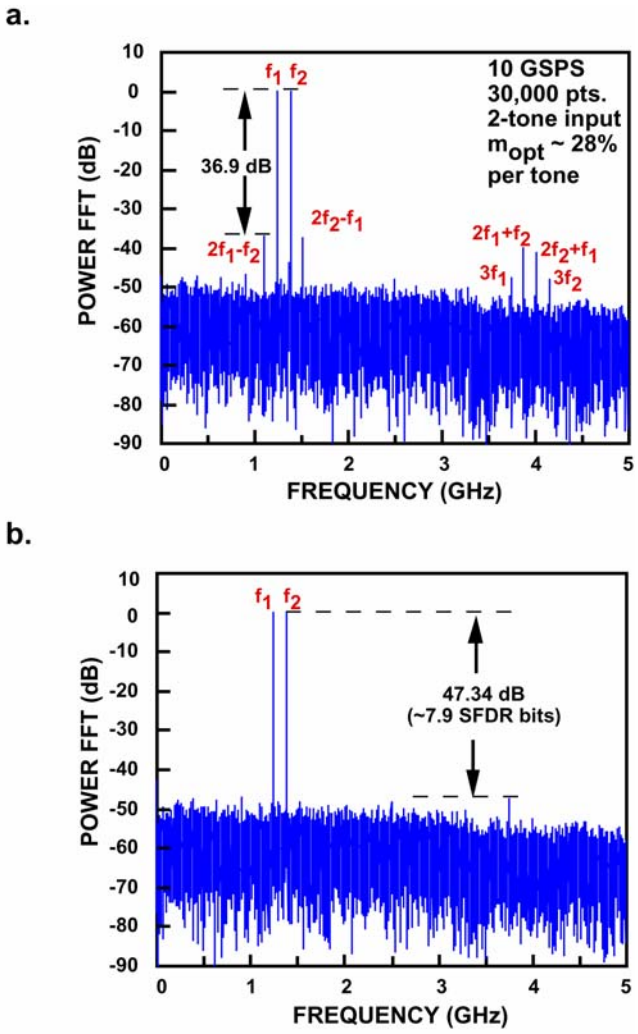


Fig. 2.12 a. FFT of photonically sampled RF-signal before time-domain linearization. Note the presence of 3rd order distortions within the Nyquist bandwidth of 5 GHz. b. FFT of instantaneously companded, i.e. digitally linearized, data (30,000 points).

During the experiment, the input frequencies for the MZ modulator were located, respectively, at $f_1 = 1.247$ GHz, and $f_2 = 1.385$ GHz, and their optical modulation indices were $m_{opt} \sim 28\%$/tone. As shown, the FFT (30,000 points) demonstrated significant third order

distortions. These intermodulation products limited the SFDR of the link to 36.9 dB (in a 5 GHz Nyquist bandwidth). Next, we corrected for the nonlinearity of the MZ modulator via Equation 2.6. Fig.2.12b shows the FFT computed for $V_{sig}(t_n)$ in Equation 2.6. As shown in Fig.2.12b, we were able to remove all the optically generated 3rd order distortions, and demonstrate a SFDR enhancement of 10.44 dB. This SFDR improvement corresponded to a significant ADC resolution enhancement of ~1.73 SFDR-bits.

In summary, we measured a timing-jitter (Δf = 10 Hz to 40 MHz) as low as 0.017%, and an amplitude-jitter of 0.041% when our fiber laser was actively mode-locked by a SLCR oscillator. Based on these measurements, we estimated that photonic sampling will support an A/D conversion resolution of ~11 bits, over a 40 MHz resolution bandwidth. We also demonstrated the application of these low-jitter pulses for photonic sampling in a 10 GSPS photonic ADC. Finally, we described the use of "instantaneous companding" to correct for third-order intermodulation distortions generated by a Mach Zehnder modulator used in our photonic sampling experiment. These photonic sampling links will find applications in the remoting of antenna farms.

SECTION 3

ENHANCED LINEARITY PHOTONIC SAMPLER

In our Program, we utilized an electro-optic $LiNbO_3$ modulator as a photonic sampler to impress the analog-input (of the ADC) on a low-jitter pulse stream generated by a ML laser (see Section 2). Therefore, the modulator's optical input is a series of optical pulses (of uniform intensity) generated by the ML laser, and its RF-input is the analog electrical signal to be sampled. The output of the sampler is a series of optical pulses whose intensities represent the time-sampled analog values of the input signal (see Fig. 1.2). For our Program, we have as a goal a sampler that can perform Nyquist sampling at 10 GSPS. Thus, the modulator must possess a bandwidth of at least 5 GHz. We describe in this Section our investigation of a new optical modulator, the Y-fed directional coupler modulator (YFDCM) that can have a more linear transfer function, and thus a larger SFDR, than the conventional Mach Zehnder modulator (MZM). Section 3.A and Section 3.B describe the design of the YFDCM for wideband photonic sampling. Next, Section 3.C describes the linearity enhancement of single-section YFDCM. The characterization of fabricated $LiNbO_3$ single-section YFDCMs and associated modeling are then presented in Section 3.D. Finally, Section 3.E describes advanced YFDC modulators that have multiple electrode sections. Specifically, we discuss YFDCM with the incorporation of (i) additional DC-bias electrodes to correct for asymmetries in the modulator's Y-splitter, and (ii) two-section RF-electrodes for enhanced fabrication tolerance and linearity operation.

3.A Y-Fed Directional Coupler (YFDC) for Photonic Sampling

A number of modulators that have enhanced linearity have been investigated in the past. Since the sampler may need to operate at or near baseband, narrow-band approaches for suppressing odd-order distortion products, such as those based on operating at certain bias voltages, may not always be applicable. The prior wideband, enhanced-linearity modulators include parallel or series combinations of two MZMs and a directional-coupler modulator (DCM) that has two additional DC bias electrodes along the length of the device.[15,16] The MZM-based approaches require splitting of the analog RF input into several portions whose relative amplitudes and phases must be controlled precisely. The DCM-based approach requires precise adjustment of the bias voltages. The device that we have investigated is an Y-fed directional coupler modulator (YFDCM) which requires only a single RF input and, ideally, does not require any DC bias voltage. The YFDCM was proposed originally as a means to achieve strong extinction or on/off modulation at a DC operating point or bias voltage of zero.[17] It has been demonstrated both in lithium niobate and polymer materials.[17,18] Shortly before the start of our PACT Program, Tavlykaev and Ramaswamy published a paper suggesting that an Y-fed DCM of a certain length could have a highly linear transfer function and low intermodulation distortion.[19] Their publication presented a theoretical study of the YFDCM. In our Program, we have conducted a combined analytical and experimental study of the suitability of the Y-fed

DCM as a wideband, enhanced linearity sampler. The YFDCM that we have demonstrated are fabricated as titanium-diffused lithium niobate waveguide devices.

The basic structure of a Y-fed directional-coupler modulator (YFDCM) is shown in Figure 3.1. The YFDCM has a single optical input port and two optical output ports. This modulator is different from conventional directional coupler modulators in that its pair of coupled optical waveguides is fed by a single symmetric waveguide Y-branch rather than by a pair of input waveguides. At the output end of the coupled waveguide section, the two waveguides separate and are no longer coupled. The output portion of the YFDCM is similar to conventional directional coupler modulators. The two optical outputs of the YFDCM are complements of each other. The YFDCM is a symmetric device. Thus, it is beneficial for the electrode structure of the YFDCM to also be symmetric. We have developed a new high-frequency symmetric electrode structure for the YFDCM, which is described in Section 3.B. Unlike the YFDCM, conventional 2x2 DCMs do not need to be symmetric and can make use of asymmetric electrode structures, which are fabricated more easily.

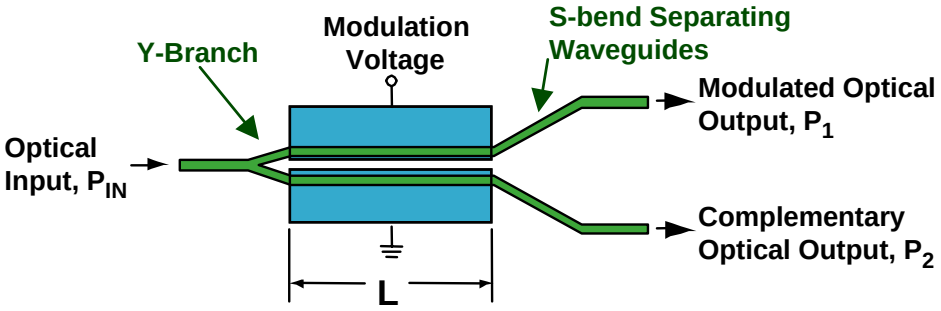


Figure 3.1 Basic structure of Y-fed directional coupler optical modulator. This device contains a single optical input with a waveguide Y-branch feeding a pair of coupled waveguides whose coupling is modulated by means of a set of electrodes. The coupled waveguides connect to a pair of waveguide S-bends that lead to two complementary optical outputs.

The input/output transfer function of the YFDCM is described by the following expression:

$$\frac{P_1}{P_{IN}} = \frac{1}{2} + \frac{x}{1+x^2} \sin^2\left[\frac{\pi}{2} s \sqrt{1+x^2}\right] \qquad \text{with} \quad s = \frac{L}{l}$$

$l = \frac{\pi}{2\kappa}$ = Transfer Length

κ = Coupling Coefficient

$x = \frac{\beta_A - \beta_B}{2\kappa} \propto$ Modulation Voltage

The optical output power is given by P_1 (or by P_2, for the complementary output port) and the optical input power is given by P_{IN}. When the YFDCM is operated as a sampler, these powers are the intensities of the input (sampling) pulses and the output (analog sample) pulses. The modulation voltage is described by a dimensionless parameter, x, that represents the dissimilarity between the two coupled waveguides. The transfer function of this device depends on the physical length, L, of the section having the coupled waveguides. It also depends on the strength of the coupling between the two waveguides. This coupling strength is typically described by a

coupling coefficient, κ. The full-transfer length, l, is defined as the physical length of the coupling section for which full transfer from one input waveguide to its opposite output waveguide (i.e., the cross state) is achieved in a conventional (2 input x 2 output) DCM having the same coupling strength as the YFDCM. The electrical length, *s*, of the YFDCM is defined as L/l and is the main parameter used for determining the behavior of the device. Note that this length is a physical parameter and generally cannot be adjusted electrically after a device has been fabricated, unlike the operation of the prior enhanced-linearity modulators.

Figure 3.2 shows the calculated input/output transfer functions of two different YFDCM. The YFDCM is a symmetric device and thus splits the optical signal equally between its two outputs when zero volts is applied to the electrodes, regardless of the length of the device. This is because the transfer of light from the first of the two coupled waveguides to the second is balanced by the transfer of light in the opposite direction, from the second waveguide to the first. Also, the input light is divided equally by the Y-branch between those two waveguides. Application of a voltage difference across the two electrodes, however, breaks this symmetry. The applied electric fields increase the refractive index of one of the coupled waveguides and decrease the refractive index of the other waveguide. For certain values of the electrical length, such as *s*=0.71, the light can be made to exit solely from a single output port of the YFDCM at particular input voltages.[17,18] The performance of a YFDCM having this length is comparable to the performance of optical 2x2 directional coupler modulators having the full-transfer length and of MZM biased at the quadrature point. For certain other values of *s*, such as *s*=2.84, the YFDCM transfer function has enhanced linearity in the vicinity of zero volts. We exploit this enhanced linearity for the samplers. Note that the full swing between a null output and a maximum output only occurs at low voltages, both positive and negative. As the voltage is increased further in either the positive or negative direction, the additional output swings occur only between the extreme values (either local maximum powers or nulls) and the equal-splitting value. When operated as a sampler, the YFDCM would typically be driven only with voltages that keep the device within its first maximum and minimum output values.

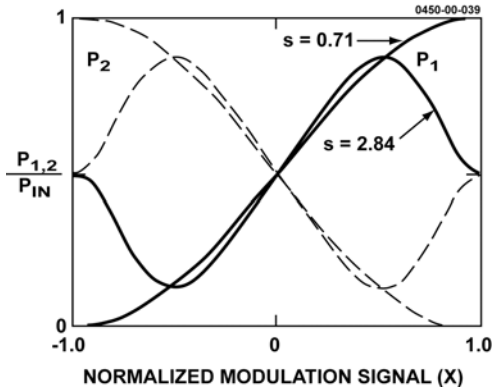


Figure 3.2 Normalized input/output transfer functions of YFDC modulators, calculated for devices at two different values of the electrical length, *s*. The transfer functions for outputs P_1 and P_2 are complementary.

The prior analyses by Tavlykaev and Ramaswamy predicted the suppression of the third-order intermodulation distortion (IM3) products for certain values of *s*. Provided the fundamental

frequency component of the output signal is not attenuated, this suppression of IM3 and 3rd harmonics should result in enhanced distortion-limited dynamic range (DLDR). Note that even-order distortion products and even harmonics are automatically suppressed by the symmetry of an ideal YFDCM. A standard MZM can have very large DLDR but that performance is limited to small modulation indices. Since the intensities of the optical sampling pulses are modulated only slightly in such cases, the resultant signal at the optical receiver may have high shot noise or laser-intensity noise compared to the useful analog information. The DLDR of a YFDCM of the proper length is as large as the DLDR of the MZM but that DLDR is achieved over a much larger range of modulation indices. For example, this improvement in modulation index is approximately a factor of 5 for a YFDCM sampler capable of 12 distortion-limited dynamic-range bits, as illustrated in Figure 3.3. We note, however, that for photonic sampling links that target high sampling rates (e.g. 40 GHz) but coarse resolution (e.g. 4-bits), a conventional MZM with sufficient bandwidth actually has better performance than a YFDCM (see Figure 3.3).

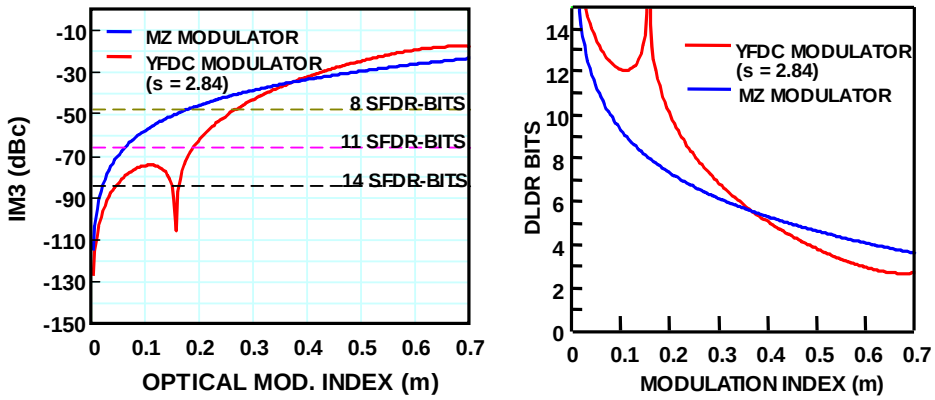


Figure 3.3 Comparison of YFDC and Mach-Zehnder optical modulators, showing dependence on the optical modulation index of 3rd-order intermodulation distortion (IM3) and distortion limited dynamic range. The amount of distortion that is permitted for and ADC system with 8, 11 and 14 spur-free dynamic range bits also is shown. The YFDCM of this example has an electrical length of 2.84.

The range of values for *s* over which the YFDCM structure exhibits reduced intermodulation distortion is limited. Figure 3.4 shows the effect of electrical length on the suppression of 3rd-order intermodulation distortion. The IM3 for a YFDCM with *s*=0.71 is similar to the IM3 for a standard MZM. Consider, for example, a 10-bit ADC system. The YFDCM sampler for such a system could have an electrical length that ranges from 2.82 to 2.86 (a variation of 1.4%) and an optical modulation index of 0.16. Since the value for *s* depends on the physical construction of the YFDCM, this range represents the fabrication tolerance for the enhanced-linearity device. Additional insights can be gained from the plots in Figure 3.4. First, when the value for *s* is outside the range of optimal values, the IM3 actually is even higher than that of a MZM, even at small modulation indices (see the plots for *s*=2.5 and *s*=2.63). Second, if the ADC system needs to have only a small number of dynamic-range bits, quite large modulation indices can be permitted. For example, a sampler with 4-bit resolution can have a modulation index of 0.5 or higher. Such a large modulation index increases the analog signal power at the photodetector so that the SNR is improved. Many approaches for ultra-wideband 4-bit ADC systems involve

distributing the sampled signals among multiple quantizers. The improved SNR may be needed to compensate the additional losses associated with such signal distribution. Note, however, that the MZM actually can have a larger modulation index than the YFDCM when the resolution of the ADC system is less than 6 bits. Finally, the target value for *s* will depend on the dynamic range that is desired. For example, if 10 DLDR bits is desired, the target value for *s* might be 2.84, with a tolerance of ±0.002. On the other hand, if only 4 DLDR bits is desired, the target value for *s* might be 2.75, with a tolerance of ±0.11. Thus, the YFDCM must be optimized for a particular set of ADC system requirements.

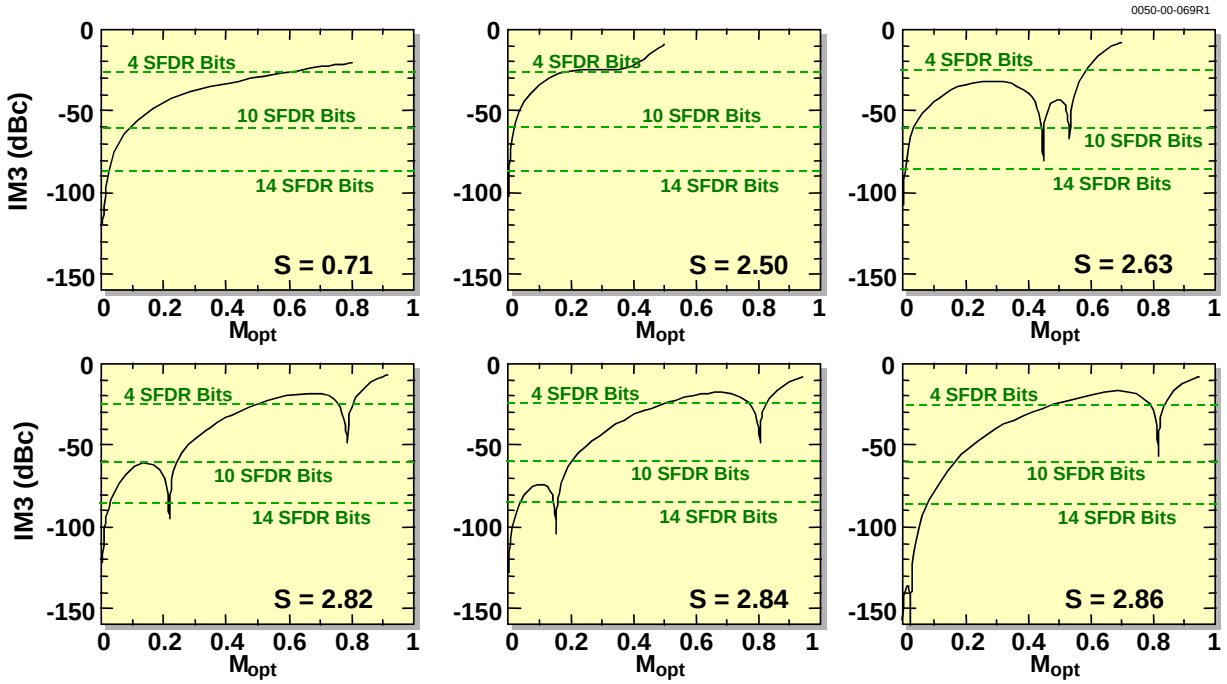


Figure 3.4 Examples of the IM3 dependence on the modulation depth calculated for YFDCM having various values of *s*.

A similar consideration applies for the bandwidth of the ADC system, since the desired value for *s* that yields the optimal spur-free dynamic range (SFDR) of the YFDCM also depends on the noise bandwidth. Figure 3.5 shows calculated RF output powers in the fundamental frequency component and the intermodulation distortion product that would be obtained from a two-tone measurement of a shot-noise limited photonic sampling link. The spur-free dynamic range (SFDR) is the difference between the fundamental and distortion powers when the distortion spur equals the noise floor. Since the noise floor rises as the receiver bandwidth is increased, the SFDR is reduced. Note that a SFDR of 10-12 bits cannot be achieved for a noise bandwidth of 5 GHz. Thus, if the 10 GSPS ADC system is required have such a large dynamic range, its bandwidth must be reduced. Many analog RF receiver systems are inherently band-limited (e.g., radar or communications systems) or use some frequency channelization to limit the instantaneous bandwidth (e.g., in ESM systems). The noise bandwidth the ADC system must have is determined by the instantaneous signal bandwidth and/or the range of frequencies over which the input signal might be scanned or hopped. To make optimal use of a 10 GSPS

photonic sampled ADC system, it is preferable to employ bandpass sampling rather than baseband sampling. The sensitivity of the SFDR to the electrical length *s* of a YFDCM depends on the noise bandwidth. As shown in Figure 3.6, a larger range of *s* can be tolerated for larger noise bandwidths.[20] However, the enhancement in SFDR is smaller for the larger noise bandwidths. The figure also shows that the target value for *s* will be progressively smaller when the noise bandwidth is progressively larger.

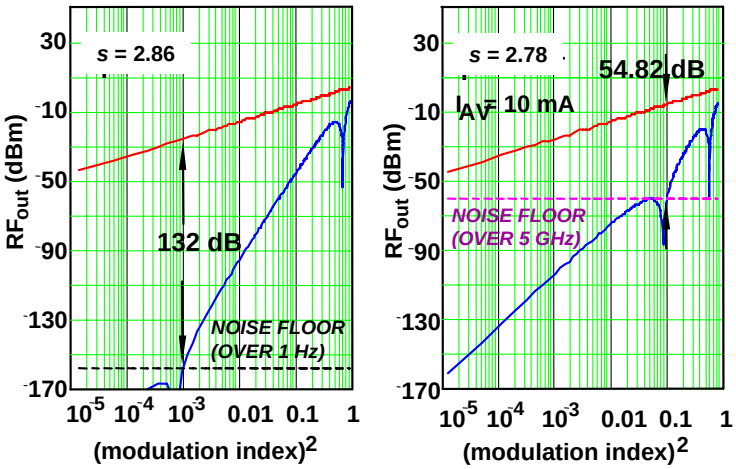


Figure 3.5 Output powers of a photonic sampling link containing a YFDCM. The powers in the fundamental frequency component and the intermodulation distortion product are plotted vs the modulation index of the YFDCM. The plot at the left is for a device optimized for a 1 Hz noise bandwidth and the plot at the right is for a device optimized for 5 GHz noise bandwidth.

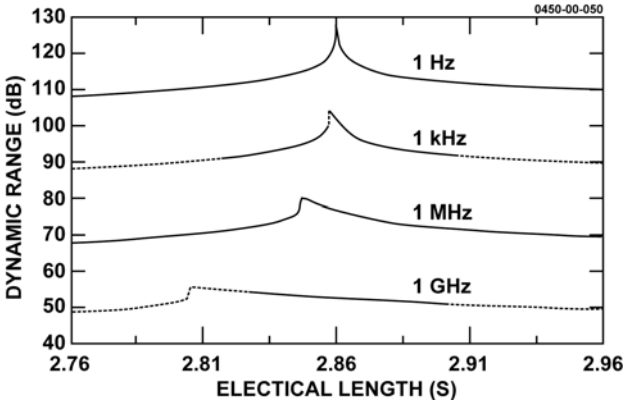


Figure 3.6 Calculated *s* dependence of the spur free dynamic range of a RF photonic link that contains a YFDCM. The link parameter values used for these calculations are the same as the ones used in reference 1. Curves are shown for noise bandwidths of 1 Hz, 1 kHz, 1 MHz and 1 GHz. These curves have been copied from Reference 20.

3.B Wideband, Symmetric YFDCM

The enhanced dynamic range of a YFDCM is achieved over a limited range of frequencies. This frequency bandwidth depends on the degree of velocity mismatch between the microwave field propagating in the transmission line electrodes and the optical field propagating in the

coupled optical waveguide structure. The dependence of the dynamic range on the modulation frequency is shown in Figure 3.7. These calculations make use of canonical parameters for the RF photonic link.[15,16] The dynamic range was calculated assuming a receiver noise bandwidth of 5 GHz. At low frequencies the SFDR is greatest when *s*=2.766. A maximum of 8.5 SFDR bits is predicted for this receiver bandwidth. This dynamic range, for a 5 GHz bandwidth, is one bit larger than the dynamic range that can be achieved with a simple MZM. The large dynamic range obtained for *s*=2.766 drops very quickly as the signal frequency is increased. However, by using a slightly larger value of *s*=2.80, the range of signal frequencies experiencing enhanced dynamic range is increased substantially, with only a minor degradation in the peak dynamic range. The maximum dynamic range for *s*=2.80 is only 1 dB lower than the maximum dynamic range for *s*=2.766.

When both the microwave and optical fields are assumed to be propagating entirely in the lithium niobate material from which our YFDCM is constructed, the velocity mismatch is quite severe. The difference between the refractive index of the optical field and the equivalent index of the microwave field (the square root of the dielectric constant at the microwave frequency) in this case is 1.8. The velocity of the optical field is approximately 1.8 times higher than the velocity of the microwave field. The microwave modulation signal becomes more and more out-of-phase compared with the modulated optical signal as they travel along the length of the device. Figure 3.7 shows that even for such a large velocity mismatch, the enhanced dynamic range is achieved for a signal bandwidth of 2.5 GHz when *s*=2.80. Reducing the mismatch Δn by a factor of 10, from 1.8 to 0.18 using the designs described later in this section of the report will extend the bandwidth by one order of magnitude, to 25 GHz. If the maximum signal frequency is 5 GHz, a mismatch Δn as large as 0.9 (40% difference in velocities) can be tolerated. However, if the maximum signal frequency is 100 GHz, Δn must be 0.045 or less, which corresponds to a velocity mismatch of 2%.

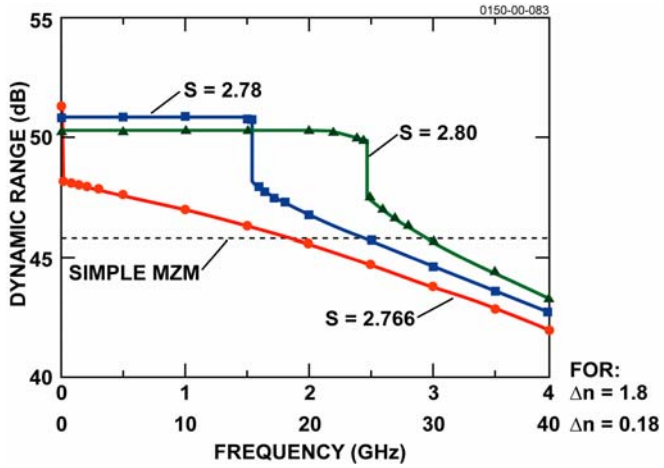


Figure 3.7 Calculated dynamic range as a function of frequency for a photonic link using a linearized Y-fed DCM with parameters specified in reference 1, with a noise bandwidth of 5 GHz. The curves are for different values of *s*. Two cases are considered. In one case, the velocities of the microwave and optical fields are completely mismatched, Δn= 1.8. In the other case, Δn = 0.18, which still represents substantial velocity mismatch.

The sensitivity of the SFDR to velocity mismatch was analyzed by Cummings.[21] Figure 3.8 shows calculated SFDR for several different wideband modulator approaches assuming complete velocity mismatch. Results for standard MZM and DCM are compared with results for the YFDCM, the dual parallel MZM (DP-MZM) and the DCM with additional DC electrodes (DCM+2). One effect of velocity mismatch is a drop in the SFDR as the modulation signal frequency is increased. Note that the dual parallel MZM is not sensitive to velocity mismatch. It also has the greatest enhancement in SFDR compared to a standard MZM or DCM. The YFDCM is less sensitive to velocity mismatch than both the dual series MZM and the enhanced linearity DCM. Although these other two approaches can give slightly better SFDR than the YFDCM, their sensitivity to velocity mismatch may make these devices difficult to produce. Note that the degree of velocity match needed for the YFDCM to achieve enhanced linearity at 5 GHz for an ADC system noise bandwidth of 1 MHz is quite minimal. The improvement obtained in SFDR is almost 7 dB for this bandwidth. For comparison, the SFDR enhancement obtained with a dual parallel MZM is somewhat higher, more than 8.5 dB. Incidentally, even a standard DCM is sensitive to velocity mismatch, as shown in the figure.

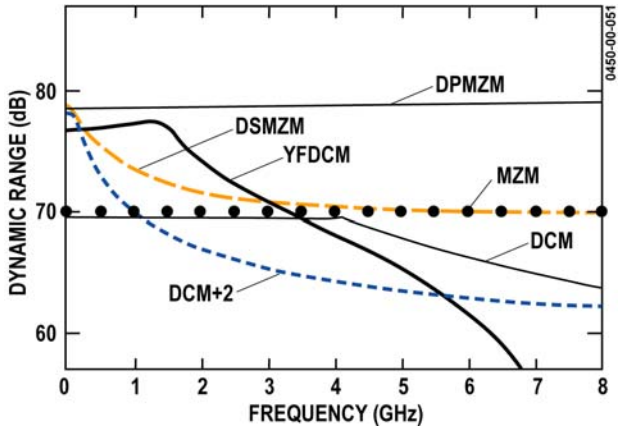


Figure 3.8 Calculated SFDR dependence on signal frequency comparing various approaches for various wideband optical modulators. The results for 1 MHz noise bandwidth is shown. These curves were copied from Reference 21.

In the first part of this effort, YFDC modulators were fabricated for operation at only low frequencies and were used to investigate the effects of the parameter *s*. These devices have a pair of wide electrodes, with the inside portion of each electrode overlapping the waveguide, as illustrated in Figure 3.9a. High frequency devices were then designed and fabricated which have coplanar strip (CPS) transmission-line electrodes.[22] The two narrow metal strips of these electrodes, illustrated in Figure 3.9b, are aligned directly above the two coupled waveguides. A layer of silicon dioxide separates the metal electrodes from the lithium niobate material. We used a finite-element electromagnetic field simulation tool (IE3D from Bay Technology) to design the electrode structure for the YFDC modulators. An example of the electric field pattern calculated by the simulation tool is shown in Figure 3.9c. Note that the ground plane is located a substantial distance away from the two electrode strips, since the lithium niobate substrate on which the devices are fabricated has a thickness of 900 microns. Note, also, that many of the electric field lines travel in the air rather than through the lithium niobate material.

This increases the velocity of the propagating microwave field to match the velocity of the propagating optical field. One disadvantage of the CPS electrodes when compared to the coplanar-waveguide electrodes commonly used in MZM is a somewhat higher attenuation (by approximately a factor of 2).[22] This higher attenuation results from the comparatively larger surface-to-volume ratio of the narrow and tall electrode strips. High-frequency electrodes also have been fabricated recently, by another research group, for YFDC modulators in polymer material.[23] In the polymer devices, the ground plane is located only several microns away from the electrode strips. Thus, those electrodes resemble coupled microstrip lines rather than CPS structures.

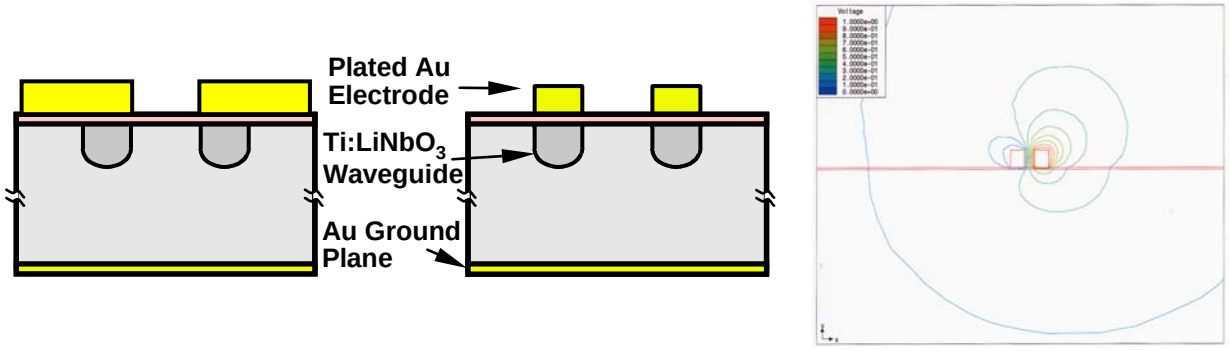


Figure 3.9 Electrode structure for YFDC, showing (a) electrodes for low-frequency device, (b) coplanar strip (CPS) electrodes for wideband device, and (c) simulated electric-field patterns for device with CPS electrodes.

The electromagnetic field solver was used to determine the propagation velocity of the microwave field and the characteristic impedance of the electrodes. Calculations were made for various combinations of the electrode spacing, electrode width and electrode height. One example is shown in Figure 3.10. In this case, the desired electrode spacing is 6 microns and the two electrodes have a width of 6.5 microns and a height of 10 microns. It is possible to obtain designs for which both velocity match and impedance match (to 50 ohms) is achieved.

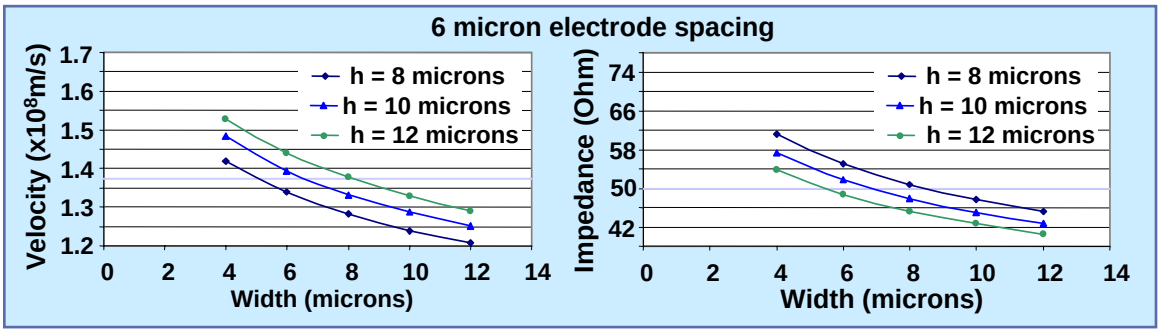


Figure 3.10 Example of calculated dependence of RF group velocity and electrode impedance on dimensions of CPS electrodes. The velocity of the optical field propagating in the modulator is indicated by the blue line in the plot at the left. Note that both velocity match and impedance match (to 50 ohms) can be achieved for a particular set of electrode dimensions.

A large number of wideband YFDC modulators have been fabricated and characterized in this PACT project. The photographs in Figure 3.11 show several portions of the fabricated devices. A titanium-diffused waveguide Y-branch is shown in the photo at the left. The width of the waveguide, which supports a single optical mode at 1550 nm wavelength, is approximately 6.5 microns. Note that the inner tip of the Y-branch has been defined quite sharply. The center photo shows the start of the active portion of a YFDCM. The close alignment of the CPS electrode over the optical waveguides in this coupling section is evident. The contact pads connected to the electrodes permit the RF input signal to be applied through conventional RF probes. Some devices that were fabricated also have air bridges where the metal crosses over an optical waveguide, as shown in the figure. The ends of the active portion of two YFDCM are shown in photo at the right. Each YFDCM has a length of approximately 6-cm. The spacing between adjacent devices fabricated on a wafer is 250 μm.

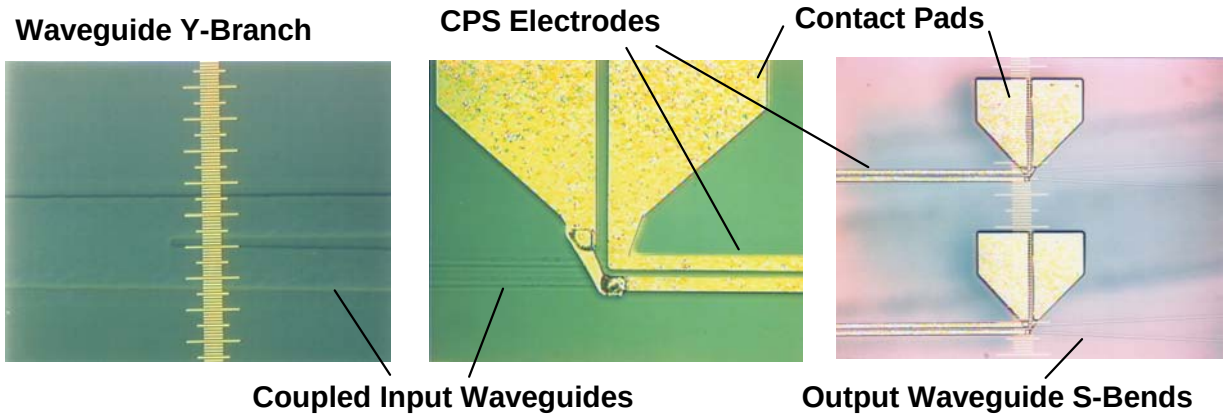


Figure 3.11 Photographs of YFDC, showing (from left to right) waveguide Y-branch, start of CPS electrodes, and end of CPS electrodes. The scale shown in the photo of the Y-branch indicates a size of 0.5 microns per small division. The coupled optical waveguides and portions of the waveguide S-bends also are evident in the photos of the electrodes.

The frequency response of one YFDCM is shown in Figure 3.12. The bandwidth of this device, approximately 20 GHz, well exceeds the requirement for the 10 GSPS ADC system. The response of the YFDCM was extracted from a network-analyzer measurement of a RF-photonic link that contains the YFDCM. The characteristics of other components in the link, such as the photodetector and the RF cables, were removed from the overall link response by first performing calibration measurements of those components. The characteristic impedance of the YFDCM was determined by measuring the input S-parameter, s_{11}, of a device that has a 50-ohm load connected to its output pads. Impedance close to 50 ohms was achieved at low frequencies.

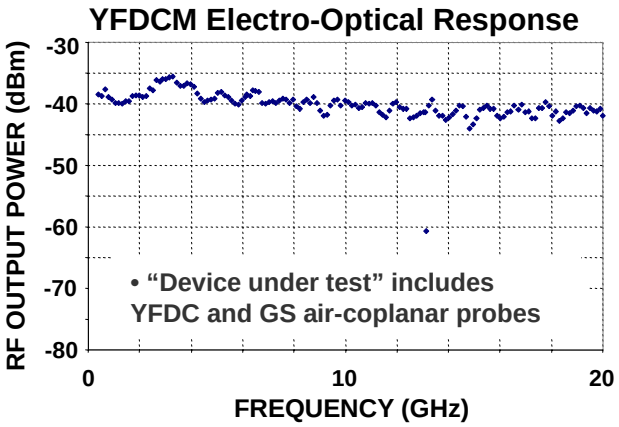


Figure 3.12 Frequency response of a YFDCM inserted in RF-photonic link. The response of the "device under test," which includes the YFDCM and a pair of GS/SG air-coplanar probes (from Cascade Technologies) was extracted from the overall link response.

A total of 28 3-inch lithium niobate wafers were fabricated that contain the high-frequency YFDC modulators. Each wafer contains single-section YFDC devices with combinations of 5 different active section lengths and 4 different center-to-center spacings (ranging from 13.0 μm to 14.5 μm) between the coupled waveguides. The lengths of the active sections are 30, 31, 32, 33 and 34 mm. Each wafer also contains some YFDC devices that have active-section lengths of 8 mm and some conventional 2x2 DCM. The thickness of the titanium layer deposited and patterned for the Ti-diffused waveguides was varied deliberately to change the effective coupling strength, κ. Note that κ can be changed by adjusting the titanium thickness, the titanium strip width (which was kept constant for these wafers) and the coupled waveguide spacing. In the early experiments, the programmed titanium thickness was varied between 650 and 950 angstroms. However, for the wafers fabricated later in the project, the programmed titanium ranged from 750 to 825 angstroms. Note that the actual thickness of the titanium could be, and often was, somewhat different from the programmed thickness. An evaporator system was used for the titanium deposition and the waveguide pattern was produced by a lift-off photolithographic process.

A layer of silicon dioxide was deposited on top of the Ti-diffused waveguide sample. The oxide thickness of approximately 1 microns and the roughly square cross-section of the CPS electrodes enable velocity match to be achieved with moderately short (less than 10-micron thickness) electrodes. The gold electrodes and the contact/probe pads for the YFDCM were formed by electroplating. Some of the wafers also contain plated air-bridge crossovers in the electrodes. These air bridges were formed by an additional plating step. The air bridges are needed for the two-section YFDCM that also were fabricated on some wafers. Other wafers also contain YFDCM having additional DC bias electrodes located between the Y-branch and the RF-modulated coupled-waveguide section. These two kinds of multi-section YFDC devices are discussed later, in Section 3.E of the report.

3.C Enhanced Linearity Operation of Single-Section YFDCM

The enhanced linearity of a YFDCM is obtained for a small range of values of the parameter *s*. Figure 3.13 illustrates how the low-frequency transfer function changes as the value for *s* is increased from 2.4 to 3.0. Whether the YFDCM has enhanced SFDR may be anticipated by examining its transfer function. Note from the discussions above that enhanced linearity is expected only for values of *s* in the vicinity of 2.8. When the value for *s* is much smaller than 2.8, the transfer function has a kink at zero volts. When the value for *s* is somewhat larger than 2.8, it is difficult to determine the linearity of the transfer function by eye. However, the relative heights of the various peaks are different and might be used as a coarse indication of the value for *s*. For example, the first peak away from zero volts becomes smaller and smaller compared to the second peak as the value for *s* is increased from 2.8 to 3.0 and higher.

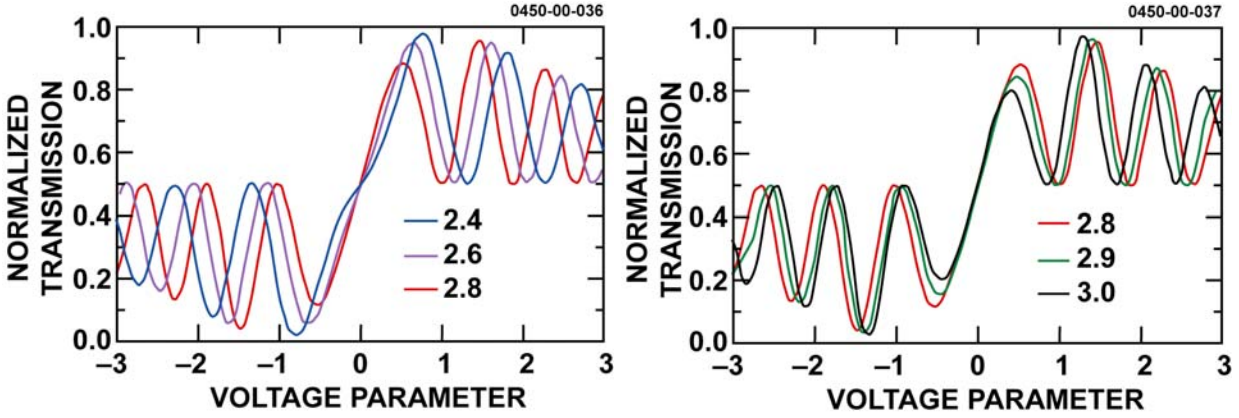


Figure 3.13 Dependence of calculated transfer function on electrical length, *s*. The transfer functions for *s*=2.4, 2.6 and 2.8 are plotted on the left and the transfer functions for *s*=2.8, 2.9 and 3.0 are plotted on the right.

Figure 3.14 shows the dependence of the intermodulation distortion of a YFDCM on the electrical length, *s*. The curves in this figure were calculated for a canonical RF photonic link that contains a YFDCM of the specified *s* as its optical modulator. We have used these same link parameter values in the past to compare other enhanced linearity optical modulators.[15,16] Thus our continued use of these link values enable us to compare the new results for the YFDCM with the previous results for multi-section 2x2 DCM and dual MZM. The link values are given in Table 1 of the paper by Bridges and Schaffner.[15] Note that although the optical sampling link in a particular ADC system may have other values for the laser power, the laser intensity noise, the optical loss, the modulation sensitivity of the modulator, the photodetector responsivity and the noise bandwidth, the basic features of the curves shown in the figure would still be applicable. The figure shows curves for the power in the intermodulation product that would be produced in a two-tone measurement plotted as a function of the signal input power. The different curves are for YFDCM with different values of *s* between 2.4 and 3.0.

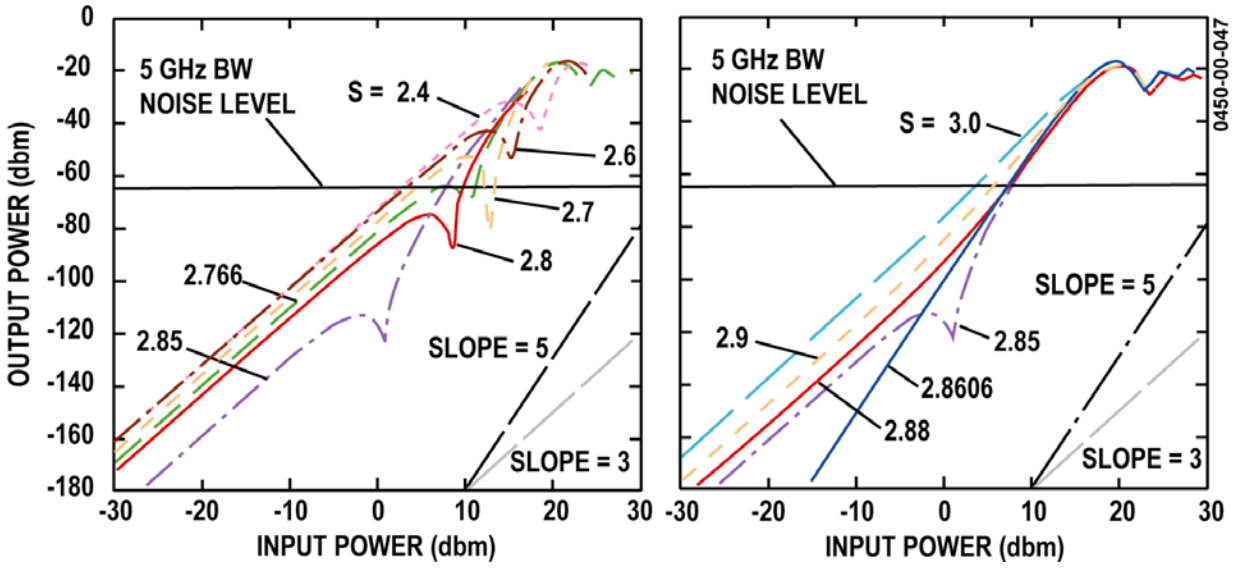


Figure 3.14 Calculated two-tone intermodulation power generated by an Y-fed DCM in a photonic link, plotted as a function of the signal input power to the YFDCM. Additional link parameters are specified in reference 1. The parameter in the graphs is the electrical length s of the YFDCM. The graph at the left covers the range s=2.4 to s=2.85, while the graph at the right covers s=2.85 to s=3.0. Note that a null in distortion occurs at a particular power level in each curve of the graph at the left. The null begins at higher input powers for s=2.4, moves to lower powers as s increases, and disappears off the lower left corner of the graph for s=2.8606. For this value of S, the intermodulation distortion has essentially a slope of 5, indicating the third derivative of the transfer function is exactly zero. At higher s, a slope 3 region begins to form at the lower powers. The transitions from slope 3 to slope 5 moves to the right for increasing s.

For $s < 2.4$ and $s > 3.0$, the two-tone intermodulation response curve has a simple slope of 3. For values of s between 2.4 and 2.86, the curve has a characteristic notch that occurs at a particular input power level. The location of the notch moves from higher to lower values of the input power as s is increased. The slope of this input/output response has a slope of 3 for input powers less than the notch power. For input powers greater than the notch power, the response has a slope of 5. The presence of the slope 5 region indicates that the intermodulation distortion due primarily to 3rd-order non-linearities has been partially cancelled. When s=2.8606, the entire intermodulation response curve has a slope of 5. This might be considered a case of "ideal" linearization (although it does not necessarily yield the largest SFDR) and is the point at which the third derivative of the transfer function exactly equals zero. When s is greater than 2.86 and yet still is less than 3.0, the response curve has a slope of 3 at the lower input powers and a slope of 5 at the higher powers. There is no notch, however. The transition between slope 3 and slope 5 moves to higher power as s is increased.

It is instructive to make several points about the intermodulation response curves. The presence of a region with slope 5 often is used as an indication that a device has enhanced linearity. To observe the slope 5 portions of the curves, which occur at the higher input powers, the two-tone measurement should supply input powers that are high enough to approach saturation of the input/output transfer function. The presence of a slope 5 region is clearly noticeable only for values of s between about 2.7 and 2.88. This represents a variation of about

6-7%. Note that the presence of a region with slope 5 and a notch in the response curve is not necessarily an indication that the dynamic range is actually enhanced in a particular ADC application. This point is illustrated in Figure 3.15, which also shows the noise level associated with a receiver bandwidth of 5 GHz. Such a noise level would apply for an input analog signal that has a bandwidth of 5 GHz. Consider the curves for *s*=2.7 and *s*=2.8. The curve for *s*=2.7 has a notch that drops below the noise level. However, the peak in the curve on the lower input power side of the notch extends above that noise level. Thus, it is the slope 3 portion of this curve rather than the slope 5 portion of this curve that determines the SFDR. On the other hand, the peak on the low power side of the notch in the curve for *s*=2.8 lies below the noise level. In this case, it is the slope 5 portion of the curve that determines the SFDR. At the optimal value of *s*=2.766, assuming the canonical link values used in our calculations, the peak on the low-power side of the notch is just barely below the noise level. This feature is the reason that different optimal values for *s* are associated with different values of ADC system noise bandwidth.

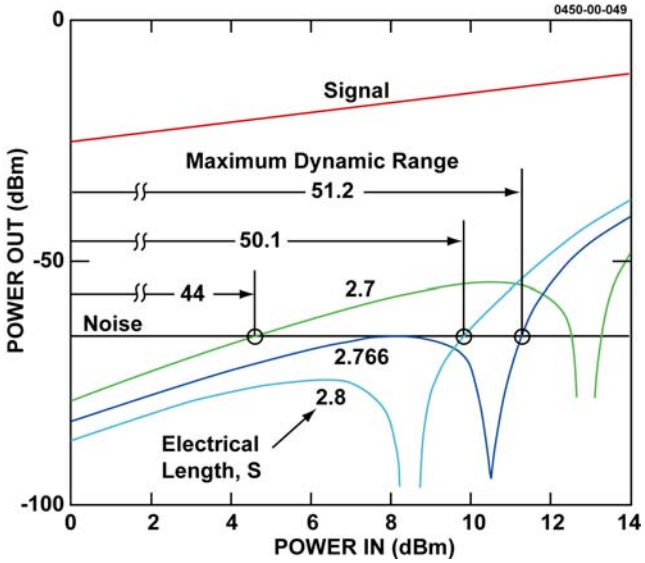


Figure 3.15 Calculated output power in fundamental and intermodulation distortion frequency components versus input power for a two-tone excitation. Results are given for YFDCM with *s* values of 2.7, 2.766 and 2.8.

Figure 3.16 illustrates the dependence of the SFDR on the electrical length, *s*, of a YFDCM. The discontinuity visible to the left of the s=2.766 point occurs because the peak of the two-tone intermodulation response curve is higher than the noise floor for values of *s* smaller than that point. However, since there is no notch (and also no local peak in the curve) for values of *s* larger than 2.86, the SFDR exhibits a gradual degradation as *s* is increased above 2.766. For a noise bandwidth of 5 GHz, the SFDR that is obtained with a YFDCM of the optimal length is more than 6 dB higher than the SFDR of a standard MZM. By reducing the noise bandwidth, to 1 Hz, the enhancement in dynamic range for the YFDCM can be made even greater, by nearly 12 dB. [21] SFDR enhancements between 6 dB and 12 dB are achieved for intermediate values of the noise bandwidth.

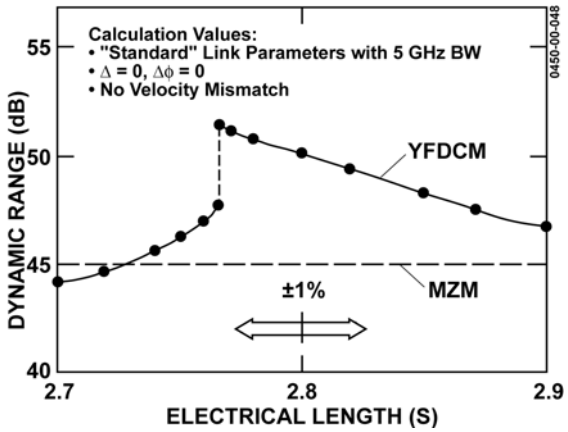


Figure 3.16 Dynamic range as a function of electrical length *s*, obtained from the intersections of the intermodulation distortion curves shown in Figure 3.11 with the noise level for 5 GHz noise bandwidth. Note the maximum value of 51.2 dB occurs at a discontinuous peak for S= 2.766, but backing off to s= 2.8 with a sacrifice in dynamic range of 1 dB will allow a ± 1% fabrication tolerance in s. The dynamic range of the MZM also is indicated in the plot, for comparison.

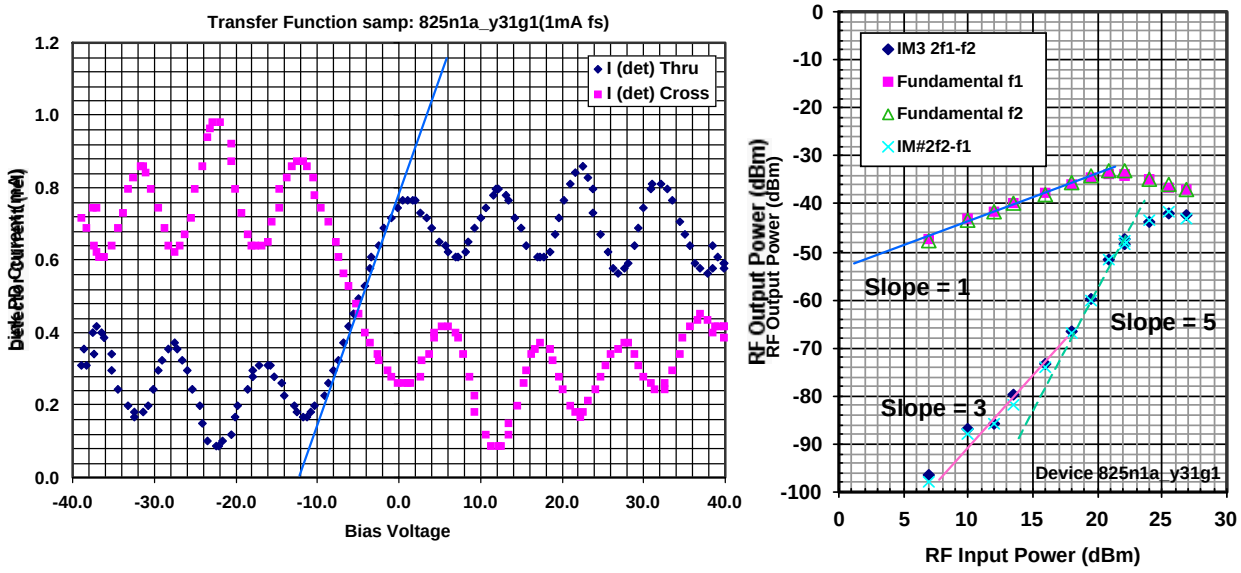
Note that the SFDR for a value of *s* just below 2.766 is similar to the SFDR for *s*=2.86. For values of *s* between 2.766 and 2.86, equal to a 3% variation in the value of *s*, an additional enhancement in SFDR is obtained. The amount of this additional enhancement depends on the noise bandwidth, with greater additional enhancement obtained for smaller bandwidths. However, the maximum amount of this additional enhancement is only about 3 dB. The electrical length *s* of the YFDCM is determined by both the physical length L of the electrode region over the underlying coupled optical waveguides and also by the value of the coupling coefficient κ. The value of L can be easily fixed with an accuracy of better than ± 0.01% by photolithography, but the value of κ is more difficult to pin down. Its value depends on the overlap of the modes in the two optical waveguides of the directional coupler, which, in turn, depends on the mode index and the physical size of the optical guides. These values ultimately depend on the distribution of titanium diffusion into the lithium niobate substrate, which is a function of the amount and uniformity of the titanium evaporations, and the time and temperature of the high temperature diffusion. As a practical matter, we can determine κ by fabricating YFDCM of varying lengths and measuring their transfer properties, thereby deducing κ from the results. The desired enhanced linearity modulators can then be designed, provided the device processing steps are all under control and are held identical to those used to deduce κ.

3.D Characterization of Single-Section YFDC Devices

A newly fabricated wafer of YFDCM would first be characterized by measuring the transfer functions of the short devices, which have an active section length of 8 mm. This physical length is designed to correspond approximately to the electrical length of *s*=0.7. The waveguide separation for which the 8-mm device has the best extinction is then selected. For this waveguide separation, the value of *s*=2.8 could then be achieved for a physical length, L, of

32 mm, which is at the midpoint of the device lengths fabricated on the wafer. The total range in length of 30-34 mm corresponds, then, to a variation in *s* of 12%. It was expected that samples having different titanium thickness would show enhanced-linearity performance for different waveguide separations. Note that both the titanium thickness and the waveguide separation contribute to the value for κ, and thus for l.

Figure 3.17a shows the measured transfer functions of a YFDCM that was fabricated. This device has a physical length L of 31 mm and a waveguide spacing of 13 μm. The transfer functions were measured by applying a low-frequency periodic voltage ramp to the device and using a broad-area photodetector. The photodetector current provides an indication of the output optical power. The peak-to-peak voltage swing is approximately 13 volts. Thus, a peak-to-peak signal of ±1 volts would produce a modulation depth of 15%. The general shape of the transfer functions is consistent with the calculated curves shown in Figure 3.13. Perhaps the most noticeable feature of these measured transfer functions, though, is that they are not symmetric about zero volt bias but rather are offset by approximately -5 volts. Another noticeable feature is that the curves for the two outputs are not exact complements of each other. Also, the peaks at the larger voltages do not return to the mid-point value of output intensity (or photocurrent). These non-ideal characteristics will be discussed later.



(a) **(b)**

Figure 3.17 Measured characteristics of a high-frequency YFDCM fabricated in Ti-diffused lithium niobate, showing (a) transfer functions for both outputs and (b) two-tone modulation response of one of those outputs.

Two-tone measurements were taken using input signals at 28.06 and 28.16 MHz. These frequencies were selected because commercial citizens-band equipment can be used to generate the high-power input signals needed to drive the YFDC devices into saturation. The set-up we

used can supply RF input power levels as high as +30 dBm per tone. This capability enabled us to investigate the slope of the intermodulation products at high RF-input levels, and to confirm the enhanced linearity of the YFDCM. Figure 3.17b shows the results of the two-tone measurements for the device whose transfer function is shown in Figure 3.17a. The power in both of the fundamental frequency components and the two 3rd-order intermodulation components are plotted versus the combined input power. As expected, the input/output curves for the fundamental components have a slope of one until compression is reached. The power in the fundamental output components actually begins to decrease again when the input power well exceeds the compression point. This is consistent with the reduction of the optical output power when the drive voltage is greater than what is needed to reach the first maximum and minimum points of the transfer function. Note that the input/output curves for the IM3 components have a slope of 3 at the lower input powers and a slope of 5 at the higher input powers. The slope 5 region coincides with input powers within a few dB of the compression point. These characteristics of the two-tone intermodulation response are consistent with a device that has a value for *s* between 2.86 and 3.0, as illustrated previously in Figure 3.14.

Two of the features of these measured transfer functions actually are mainly artifacts of the measurement set-up and procedure that were corrected in measurements of later wafers. The large voltage offset and the failure of the outputs to return to the midpoint value were corrected by using a slower sweep of the voltage ramp. However, a smaller voltage offset (typically ±0.5 to ±2.0 volts) still is observed for most of the devices measured using the slower voltage sweep. A second observation is that for high-frequency YFDC devices from the earlier wafer runs, the exact two-tone response curves were difficult to reproduce in repeated measurements of the same device. This is because a DC bias voltage was applied to the devices when doing the two-tone measurements. We observed a drift of the transfer function when a DC bias is applied. Such bias drift effects are common to many lithium niobate waveguide devices and have been attributed to the presence of impurities, such as iron ions, in the lithium niobate substrate. Although higher quality substrate materials are now available, so that the bias drift is reduced, some drift usually still is present unless measures are taken in the device fabrication process to address it. The later wafer runs make use of a slightly conductive oxide layer to reduce the bias drift.

We have attempted to fit some of the experimental transfer function data to the theoretical curves for an Y-fed DCM. The parameters used in the theoretical fit were:

s	Modulator electrical length	⎫
V_s	Modulator voltage sensitivity [V]	⎪
Δ	Intensity split error in Y junction	⎬ Modulator Properties
$\Delta\phi$	Phase error in Y junction [rad.]	⎪
	Photocurrent scale factor	⎧
	Voltage offset [V]	⎬ Measurement Setup
	Photocurrent offset	⎩

The first four of these parameters are properties of the modulator alone, and the last two are properties of the measurement instrumentation. The photocurrent scale factor is a property of the modulator, due to the attenuation in the chip, and also of the measurement setup. The values of these parameters were varied and the sum of the squared errors between the experiment points (98 points) and the theoretical curve was reduced to a small value. Results for a typical modulator is shown in Figure 3.18. We see that a value of s=2.88 is a good fit for this 30 mm long modulator. This modulator has an active section length of 30 mm, a waveguide separation of 13.5 μm, and a programmed titanium thickness of 800 angstroms. Note that relatively small values of the Y-branch asymmetry are needed for this fit, indicating a good Y-junction. Note, also, that the curve fit parameter values for the two outputs of this Y-fed DCM although similar are not identical.

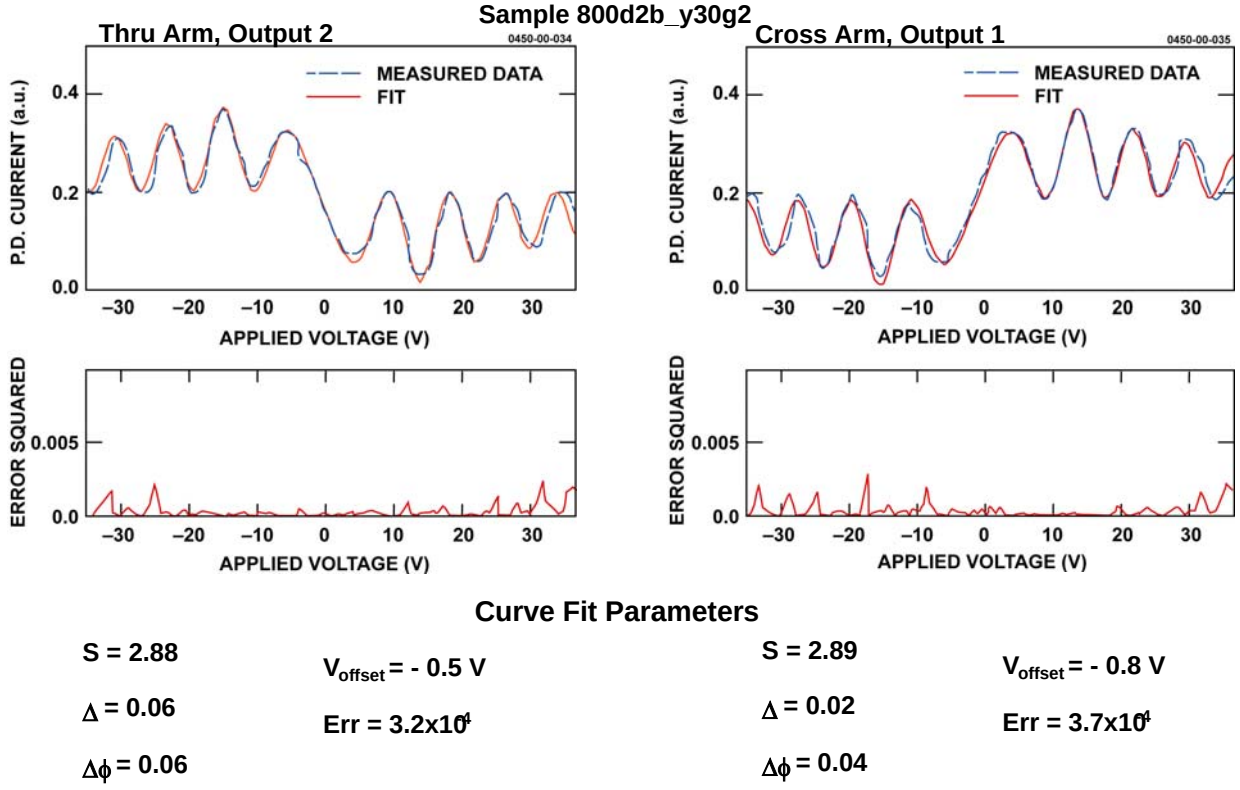


Figure 3.18 Example of a curve fit to 98 points of the experimental transfer function data for a particular YFDCM, 800d2b_y30g2. The curves are for the two output arms of the directional coupler. The fit parameters are given below each graph, and ideally would be identical for the two arms. The squared error is also shown, and the sum of these 98 squared errors is given with the fit parameters.

Each wafer contains two sets of devices that should have nominally the same physical lengths and coupling coefficients. Using this fitting technique, fits were made for the modulators of each set, to see how s varied with the physical length L. Figure 3.19 shows results for two sets of modulators, the "a" and "b" sets fabricated on a single wafer. Note that s varies linearly

with L for both sets (although there is a small offset value) and that both optical outputs of each device give the same parameters for the fit, except for the L = 30 mm modulator in the "a" set. Unfortunately, the 31-mm long modulators in each set had shorted electrodes and could not be measured. Note that *s* is reasonably proportional to L for both sets, but that the values of *s* are not the same at a given L in the two sets of modulators, for which the same programmed titanium thickness was deposited. Instead, the values of *s* for the two sets disagree by 8%, which is outside the "± 1%" tolerance we would like to achieve on *s*. This gives some measure of the non-uniformity in the modulator characteristics across a wafer. The titanium film for the waveguides of this wafer was deposited by an electron-beam evaporator that does not employ sample translation to improve the thickness uniformity. We have obtained much more uniform titanium thicknesses using a sputtering system that also employs some means for sample translation. A deposition system like that one should be used for any future work. These curve-fitting results, which pointed out the non-uniformity in device characteristics across the 3-inch wafers were obtained too late in the project for us to fabricate another set of wafers using the improved techniques. Note also that the 1 mm increment in L available on these wafers is larger than the desired ± 1% variation in *s*. Thus, either better run-to-run control is needed on κ of the fabricated devices or a finer length increment should be used in future mask designs for the various devices fabricated on a wafer.

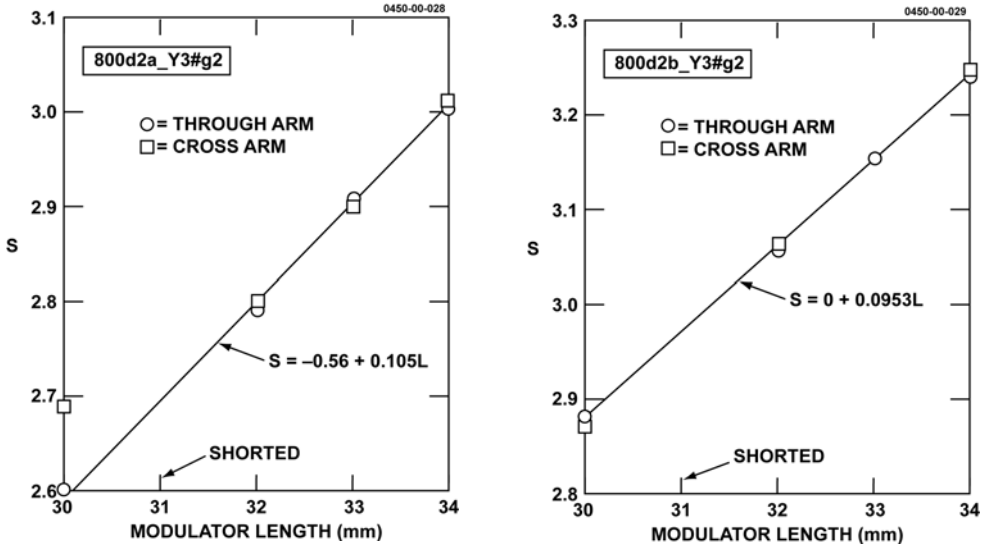


Figure 3.19 Graphs of electrical length *s* versus physical length L for the a-set and b-set of modulators with 13.5 μm spacing on the same wafer, 800d2. Fits for both outputs of the directional coupler are shown. The 31 mm-length modulators were shorted in both sets, so no data were available for that length.

The results of two-tone measurements for device 800d2b_y30g2 are shown in Figure 3.20. Input/output curves are shown for the two sets of fundamental, 2nd harmonic and 3rd-order intermodulation distortion frequency components of the output signal. Note that the curves for the fundamental components have a slope of one, the 2nd harmonic component curves have a slope of two and the IM3 components have a slope of three until they reach compression. These measured results can be compared with the results from the curve fitting of the transfer function. Note that the curve fitting suggests that *s*=2.89 for this device. For such a length of s, the curve

for the intermodulation distortion should have primarily a slope of 3, with a small region at the highest input powers that has a slope of 5. The region with slope 5 is not evident for the input power levels shown in the two-tone measurement data.

The measured transfer function of this device exhibits a small voltage offset, of approximately –0.8 volts. A DC bias voltage was applied to this device when the two-tone responses were measured. Figure 3.20 shows two-tone modulation response curves measured at the bias voltages of –0.5, -0.8 and –1,0 volts. Note that when the device is unbiased, or has a bias voltage of only –0.5 volts, the power in the second harmonic frequency components can be comparable to the power in the IM3 components, at low input levels. For such cases, the second harmonic spurs could then limit the SFDR. However, when the device is biased to a voltage of –0.8 or –1.0 volts, the second harmonic components remain weaker than the IM3 components. The need to apply a DC bias indicates that this YFDCM is not perfectly symmetric. Some potential factors that may contribute to the asymmetry are discussed in the next section of this report. The application of these small bias voltages does not have a significant effect on the power in the IM3 components.

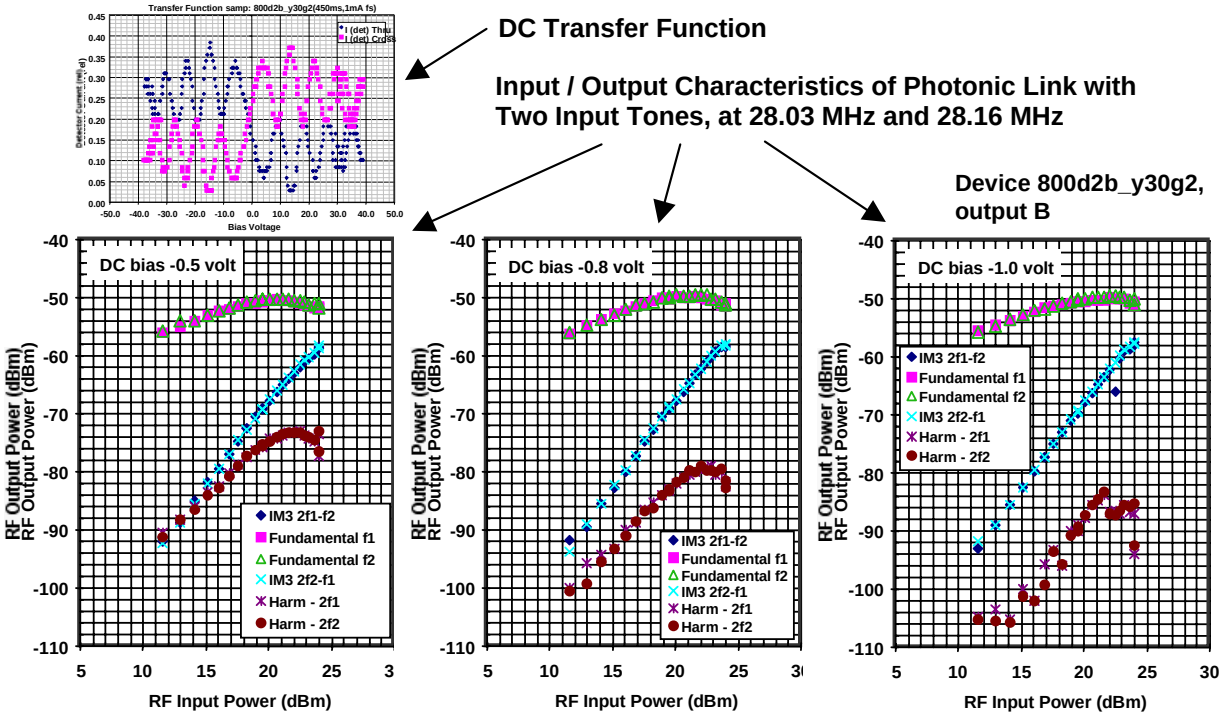


Figure 3.20 Measured two-tone modulation response of a RF photonic link containing the YFDCM, 800d2b_y30g2, whose transfer functions are shown in Figure 3.18. Response curves for the fundamental, 2nd harmonic and 3rd-order intermodulation distortion components are shown for 3 different values of the DC bias voltage. The transfer functions are shown, again, in the insert.

Not all curve fits were as good as those in Figure 3.18. Additional degrees of freedom would be required to fit to those difficult to fit transfer functions, which indicates that not all the physics of the devices have been included in the theoretical model. Further extensions of the theoretical

model might include additional parameters that describe, for example, variation of κ, β_A and β_B along the longitudinal direction of the waveguides.

3.E Multi-Section YFDC Devices

Two different kinds of advanced YFDCM were investigated in this project. These devices have multiple electrode sections and are somewhat longer than the single-section YFDCM discussed above. These devices either have additional DC bias electrodes on them, or their RF electrodes are longer and have multiple sections. The devices with the additional DC bias electrodes are discussed in Section 3.E.1. The devices with multiple sections of RF electrodes are discussed in Section 3.E.2.

3.E.1 YFDC Device with Additional DC Bias Electrodes

The function of the input waveguide Y-splitter is to feed each guide of the directional coupler with optical waves that are exactly equal in amplitude and phase. If these waves are exactly equal, then all even-order derivatives are zero at zero voltage applied to the modulator, and thus all even-order harmonics and even-order intermodulation products are identically zero. However, if the Y-splitter is not exactly symmetric, there can be a fractional difference Δ in the intensities of the two waves and a difference $\Delta\phi$ [radians] in their phases. We have calculated the effects of these errors on a typical YFDC modulator (s=2.76 and noise bandwidth of 5 GHz). The results show that the modulator is relatively insensitive to intensity errors Δ; values of Δ smaller than 0.2 (20% difference between the two intensities) will not degrade the third order intermodulation distortion limited dynamic range, and also keep the second-harmonic-limited dynamic range greater than the IM3-limited dynamic range. Intensity splits in practical Y-junctions are usually much better than this, so that Δ is not really a problem.

On the other hand, phase errors are found to be much more critical; while small values of $\Delta\phi$ have virtually no effect on the third-order-distortion limited dynamic range, even very small values of $\Delta\phi$ will generate second harmonic power sufficient to degrade the overall dynamic range. Figure 3.21 shows the calculated signal, noise, third-order intermodulation and second harmonic output components for a range of $\Delta\phi$ values. To keep the second harmonic below the noise over the 51.2 dB dynamic range for this link means that $\Delta\phi$ must be less than 0.01 radians, or about 0.5 optical degrees.

It is difficult to imagine that such tight tolerances can be held in the junction fabrication. For example, the curve fitting results shown in Figure 3.18 indicate that $\Delta\phi$ = 0.04-0.06 for that device. Unlike Mach-Zehnder modulators for which differences in phase in the two arms of the interferometer can be compensated by shifting the d-c bias point, this modulator requires symmetry at zero bias. The analyses suggest that attempts to apply a DC bias to the RF modulation section of the YFDC device to compensate for the phase error at the start of that RF modulation section have limited effectiveness.

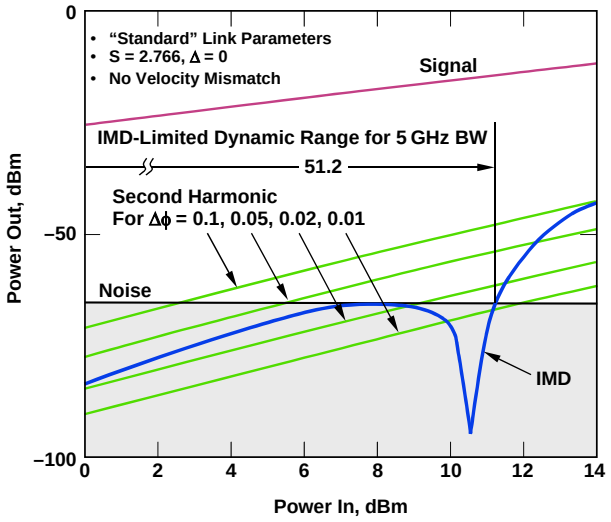


Figure 3.21 Signal, noise, second harmonic, and third-order intermodulation distortion (IMD) as a function of input power for a photonic link using a YFDCM described by the various curve-fitting parameters. The parameter varied for these plots is the phase imbalance Δϕ [radians] in the optical signal from the two arms of the Y-splitter. Signal, noise, and IMD are essentially unaffected over the range of Δϕ shown, but the second harmonic increases significantly. The value of Δϕ must be kept below about 0.012 radians to keep the second harmonic level everywhere below the noise or IMD, so that it does not affect the dynamic range.

Fortunately, there can be a relatively simple solution to this problem. The relative phases in the two arms may be made exactly equal by applying voltages to short electrode sections situated between the Y-branch and the RF modulation section. In fact, by using two such electrode sections, errors in both intensity balance and phase difference may be compensated exactly. Figure 3.22 shows a schematic illustration of a 3-section YFDCM that has these two input-adjustment DC electrode sections and the RF modulation section. One version of the fabrication masks for the YFDCM wafers contain these 3-section devices in addition to the single-section devices discussed earlier. The 3-section devices have a RF-modulation section of length 30, 32 or 34 mm as well as the 4 possible values for waveguide spacing used for the single-section devices.

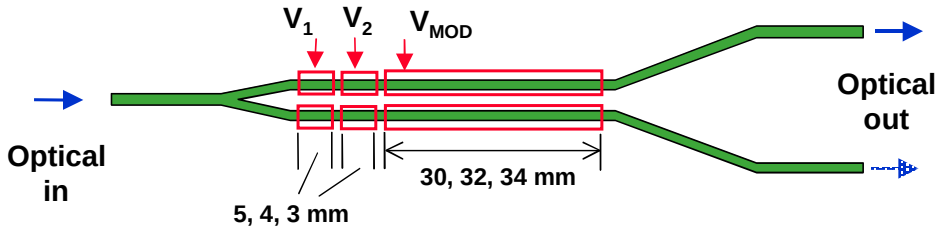


Figure 3.22 Illustration of 3-section YFDC device with two DC bias electrodes in addition to the RF modulation electrode. These two DC bias electrodes correct for asymmetries in the Y-splitter at the front of the device.

Examples of the combination of bias voltages that can provide complete compensation for the errors of $0 < \Delta < 0.5$ and $0 < \Delta\phi < 0.5$ [radians] are shown in Figure 3.23. These calculations are for bias electrodes that are only 1 mm in length. The electrodes in the fabricated devices are longer, 3-5 mm lengths, and can accomplish the same task at progressively lower values of the bias voltages. Essentially, these first two sections of the YFDCM act like two short d-c directional coupler modulators that are used to "precondition" the optical signals to be exactly equal in intensity and phase before entering the RF-driven modulator, no matter what the errors in the Y-splitter are.

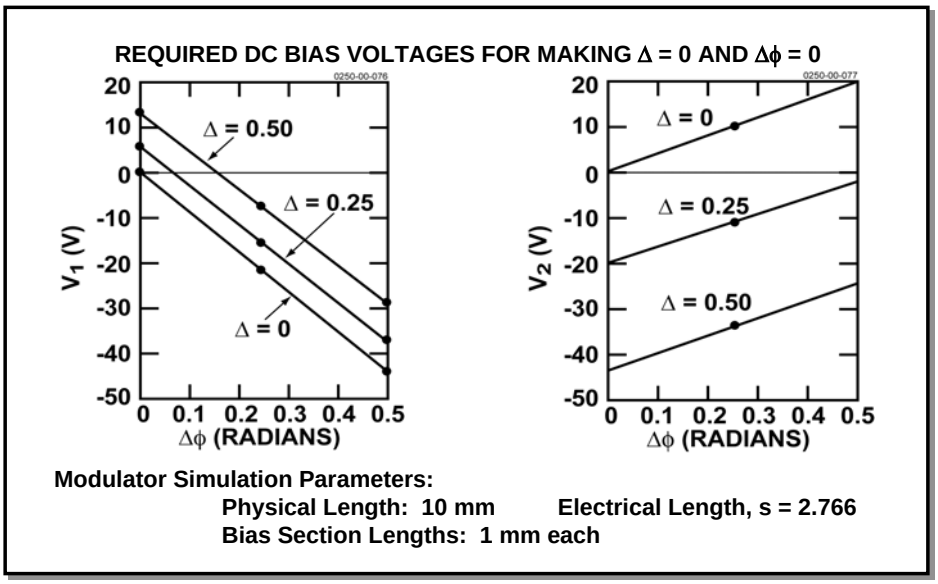
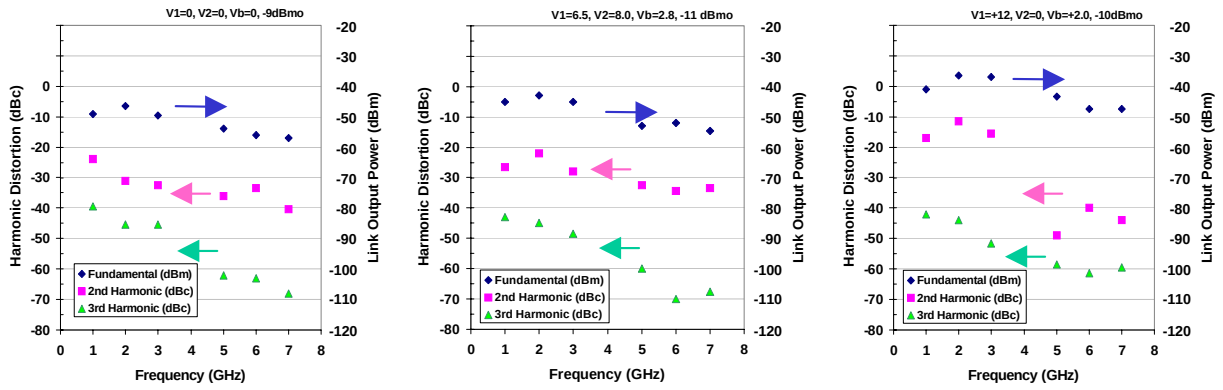


Figure 3.23 Plots of the DC voltages V_1 and V_2 applied to the two short electrode sections at the front of a 3-section YFDCM. These voltages are required to compensate for errors Δ in optical amplitude and $\Delta\phi$ in optical phase due to an asymmetric Y-splitter. The voltages shown are for front electrode lengths of 1 mm.

We have fabricated a number of 3-section YFDCM. One way to characterize them is to measure the fundamental, 2nd harmonic and 3rd harmonic output powers for a single-tone RF drive signal. Since the maximum frequency required for the photonic sampler is only 5 GHz, this measurement can be done using conventional photodetectors and test equipment. We discuss, as an example, the results obtained for one device, 800n1b_b32g2_u, from a wafer 800n1 that has quite large asymmetry compared to the devices from wafer 800d2, for which other device results have been discussed earlier. Figure 3.24 shows data taken for single-tone input signals having frequencies of 1, 2, 3, 5, 6 and 7 GHz. There are three bias voltages that could be applied to this device. Two of those voltages, V_1 and V_2, are for the two sets of electrodes at the front portion of the coupling region. The other bias voltage, V_b, is for the RF electrode. The figure compares the results when all bias voltages are set to zero and when those voltages are set to minimize the 2nd and 3rd harmonics, in an iterative manner, at an input frequency of 1 GHz or 5 GHz. Note that the primary effect of adjusting the bias voltage is the change of the 2nd harmonic power. The bias voltages have a weaker effect on the 3rd harmonic power. Note, also, that minimization of the 2nd and 3rd harmonic powers for one frequency could

degrade those harmonic levels for another frequency. Thus, the entire frequency range of interest must be considered when performing the bias adjustments.



(a) **(b)** **(c)**

Figure 3.24 Measured effect of bias electrodes on 2nd and 3rd harmonic distortion powers of a 3-section YFDCM. The value of the output components at the fundamental frequency (given in dBm) and the 2nd and 3rd harmonic frequencies (given in dBc) are shown plotted versus the input frequency. The cases shown are for zero applied bias voltage (a) and for all 3 bias voltages set to minimize both the 2nd and 3rd harmonic powers for for 1-GHz input (b), or for 5 GHz input (c).

Some comparisons may be made of the 3-section YFDCM with a prior enhanced linearity 2x2 DCM that has a RF modulation section followed by two DC bias sections.[24] For that device, the total length of the coupled waveguides is greater than one full transfer length. The optical input is fed into one of the input waveguide arms. The RF-modulation section is designed for full transfer of that input signal into the opposite output arm (cross state). The remaining portion of the coupled waveguides is used to slightly adjust the amount of light exiting the cross output arm, by coupling in or out the light that would have exited from the other output arm (the thru arm) of the DCM. The two additional bias electrode sections are used to control the amount of light that is additionally coupled. For the 3-section YFDCM, the length of the RF modulation section is set at approximately the enhanced-linearity length (with the desired value for *s* determined by the noise bandwidth and modulation depth). The additional bias electrode sections of this device are used, to first order, to correct for asymmetries in the input to the RF modulation section. If the input splitter is perfectly symmetric, one might think that those two bias sections could be used to slightly unbalance the input optical field of the coupling section in such a way that this imbalance compensates for small departures of the length for the RF modulation section from the optimal value of *s*. However, our preliminary analysis of this secondary use of the additional bias electrodes suggests that the effects of second harmonics created thereby would dominate any reductions to the IM3 components.

3.E.2 YFDC Device with Two-Section RF Electrode

An Y-fed directional coupler modulator (DCM) with two RF-modulation sections was proposed by Tavlykaev and Ramaswamy as an improvement on the simple Y-fed DCM.[19]

Instead of making a simple modulator of a specific electrical length (e.g., $s = 2.76$, optimum for a 5 GHz noise bandwidth), they proposed to separate the modulating electrodes into two sections, with a 180 degree phase reversal between the two sections. These authors later demonstrated a low-frequency two-section YFDCM by applying voltages of equal amplitude and opposite polarity to the two electrode sections.[25] A two-section device that needs only a single electrode section also has been demonstrated, by using domain-inverted electro-optic polymer waveguides.[26] This polymer device is potentially capable of high frequency operation, although only those authors showed only a DC transfer function. We have developed high-frequency versions of a two-section YFDCM with conventional titanium-diffused lithium niobate waveguides, which is illustrated in Figure 3.25a. This device has coplanar strip (CPS) transmission-line electrodes like the ones used in the single-section YFDCM described earlier in the report. The key to using high-frequency CPS electrodes is the fabrication of a phase-reversing junction. We accomplish this by fabricating an air-bridge crossover. A photograph of this crossover is shown in Figure 3.25b.

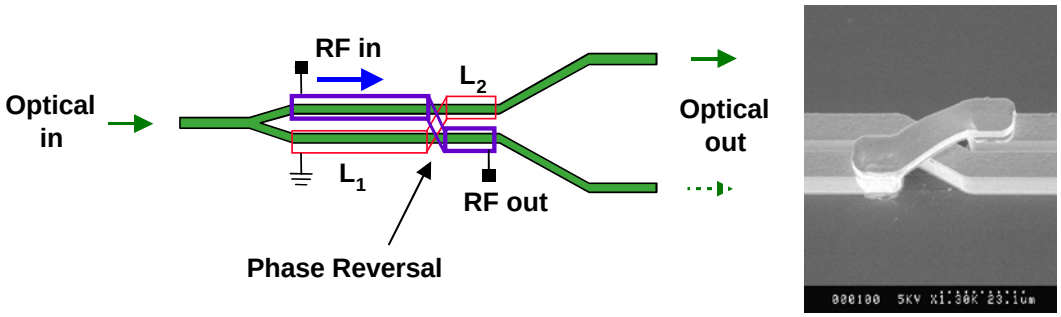
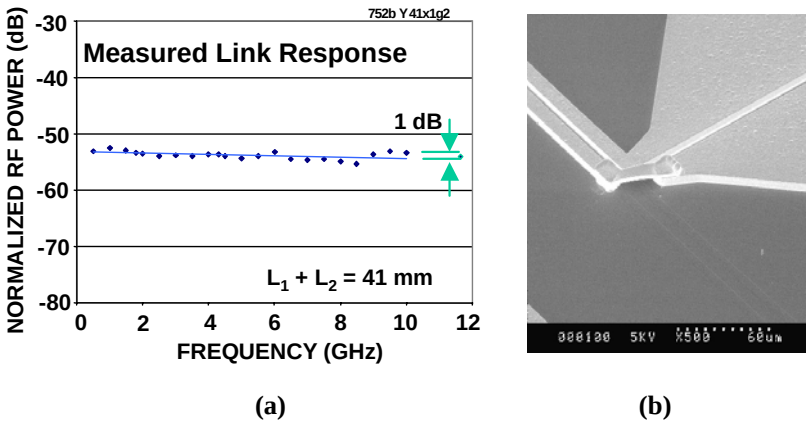


Figure 3.25 YFDCM with a two-section RF electrode, showing (a) illustration of device and (b) photograph of fabricated CPS electrode crossover. One of the titanium-diffused waveguides can be seen under the air bridge.

The two-section YFDCM is somewhat longer than a comparable single-section device. The total length of the modulation section for the fabricated two-section devices is 41 mm, compared to a length of around 32 mm for the single-section devices. The crossover has fairly low attenuation and does not substantially degrade the RF performance of the device. Figure 3.26a shows the measured frequency response of a RF photonic link that contains a two-section YFDCM. The link response has been attenuated by only 1 dB at 10 GHz, which is twice the maximum frequency required of the photonic sampler. A SEM photograph of the end of the RF modulation portion of a two-section YFDCM is shown in Figure 3.26b. Note that the two coupled optical waveguides also are visible in the photograph. This photographs shows the relative sizes of the electrode strips, the air bridge and the waveguides. The high frequency response is achieved because we have been able to fabricate the tall and closely space electrodes and the air bridge that is above those electrodes as well as to accurately align those electrodes over the optical waveguides.



(a) **(b)**

Figure 3.26 Measured frequency response of two-section YFDCM derived from measurement of a RF photonic link containing that device (a) and photograph of end portion of CPS electrodes in a two-section YFDCM (b).

The initial motivation for the interest in the two-section YFDCM is the claim made by Tavlykaev and Ramaswamy that this device can maintain enhanced linearity over a larger range of physical lengths. [5] However, the definition of linearity used by these authors actually corresponds to a fairly low value of SFDR, since it is based on a coarse fit of the transfer function to a straight line. Figure 3.27 shows the results of their calculations of the enhanced linearity. The two sections of this modulator have lengths of S_1 and S_2. The lighter areas are regions of low-distortion and the darker areas are those of high distortion. Note that the results for a comparable enhanced-linearity single-section device are shown on this figure as $S_1 = 2.7$, $S_2 = 0$ and $S_1 = 0$, $S_2 = 2.7$. The two-section values the authors deemed worthy of use are indicated by the points in the light regions around $S_1 = 2.4$, $S_2 = 1$ and $S_1 = 4.3$, $S_2 = 1$, which are claimed to have even lower distortion than the single-section YFDCM.

We have investigated the spur-free dynamic range of the two-section YFDCM to evaluate the applicability of such a device for photonic sampling in ADC systems. A direct comparison of our computer simulations with the prior results is complicated somewhat by the fact that Tavlykaev and Ramaswamy do not use two-tone intermodulation distortion as their measure of "linearity". Instead, they adopted a measure of "straightness" of the transfer function around the operating region that is more appropriate for large-signal operation. Such "straightness" may have significant curvature near the origin and thus significant small-signal distortion. In addition, when Tavlykaev and Ramaswamy considered the effect of S_1 and S_2 on the intermodulation distortion, they did not also consider the effect of those lengths on the signal component. Figure 3.27a does not provide an indication of dynamic range, which is a ratio of signal to distortion. For example, consider a diagonal line $S_1 = S_2$ on their graph. Clearly, signals along this line will be identically zero, since the device now consists of two identical out-of-phase modulators in series. The distortion varies along this line, but with zero signal, the dynamic range is identically zero.

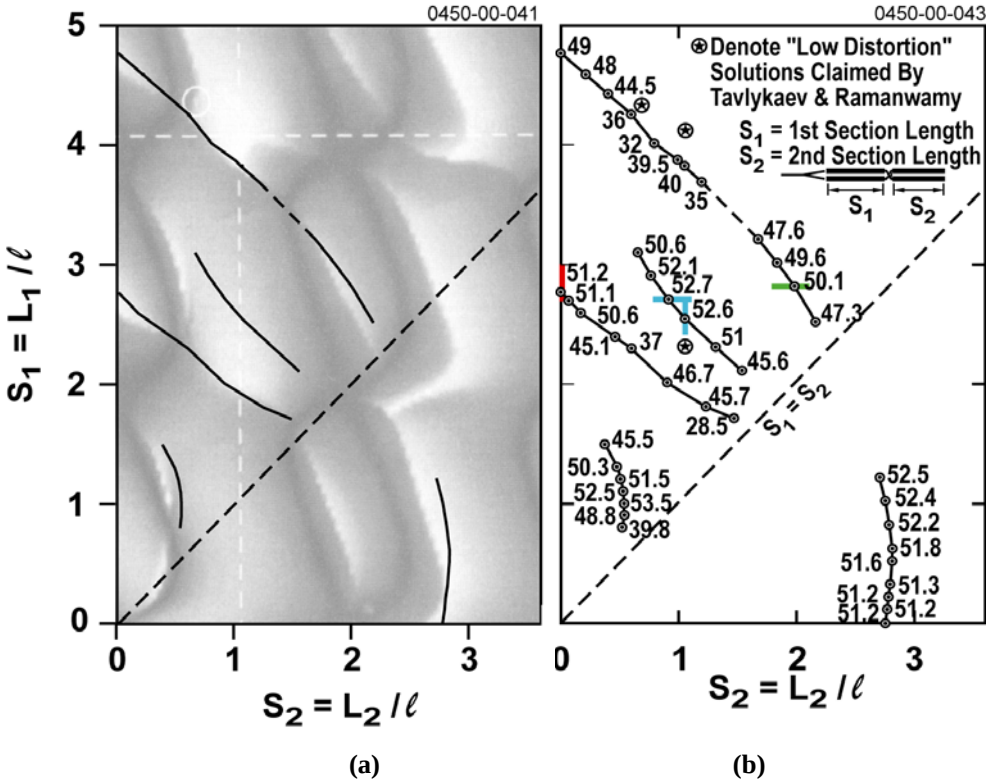


Figure 3.27 Linearity as calculated in Reference 19 is shown in (a) as a function of the electrical lengths S_1 and S_2 for the two sections of the modulator. Light shading represents greater linearity and dark shading poorer linearity. The HRL calculations of dynamic range are shown in (b), using the standard two-tone definition of distortion, calculated signal levels, and a noise bandwidth of 5 GHz. The curves show the "ridges" of maximum dynamic range, with the values of dynamic range (for 5 GHz noise bandwidth) shown numerically along the curve. These calculated "ridges" are also shown superposed on the shaded plot in (a) for comparison. There is a general agreement in the location of the maximum dynamic range, but also some obvious differences as well, since Reference 5 used a definition of distortion different from the two-tone IMD typically applicable for ADC systems.

In our theoretical analyses, we calculated the dynamic range defined in the usual two-tone fashion for intermodulation distortion. The results are shown in both Figure 3.27b and Figure 3.28b. The results are plotted using the same scale as the plots in Figures 3.27a, and also Figure 3.28a, so the two sets of results can be compared directly. Calculations were made with combinations of S_1, S_2 to find the "ridges" of maximum dynamic range. The ridges are traced in Figure 3.27b as lines connecting points at which the values of dynamic range (in dB) are given. The canonical link values and a 5 GHz noise bandwidth were assumed for these calculations. The "ridges" determined by our SFDR calculations also are indicated in Figure 3.27a by the black lines. The variation in dynamic range generally follows the bright regions shown in Figure 3.27a. However, it differs in detail because of the differing definition of "linearity" and the inclusion of the signal variation in our dynamic range calculations. In our calculation, the dynamic range becomes equal to zero when the line $S_1 = S_2$ is approached. The entire domain of S_1, S_2 was not mapped, but enough of it was done to come to the conclusion that the enhanced "linearity" points specified by Tavlykaev and Ramaswamy do not correspond to strikingly higher

dynamic range, when the change in signal power is taken into account. For example, note that the SFDR at the point on Figure 3.27b near (4.3, 1) is actually much worse than the SFDR of an optimal single-section YFDCM. Note, also, that the SFDR at the point near (2.6, 1) is only 1.5 dB better than the SFDR of an optimal single-section device. Thus, improvement in SFDR would not be a motivation for accepting the additional complexity and slightly reduced bandwidth of a two-section device. Although not all of the "white areas" in Figure 3.27a were explored, no values of dynamic range more than 2 dB larger than those for a single-section Y-fed DCM (51.2 dB) were found in the regions that were explored.

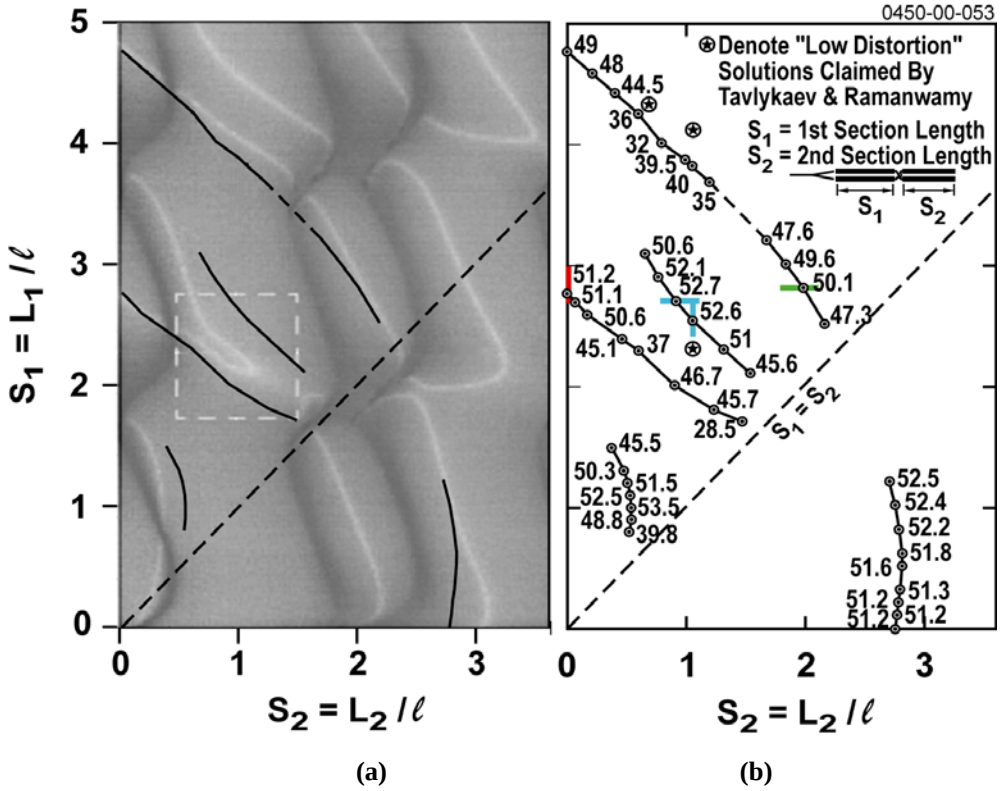


Figure 3.28 Calculated dependence of intermodulation distortion and dynamic range on electrical lengths of the two sections, showing (a) estimated inter-modulation distortion contours from Reference 19 and (b) loci of maximum dynamic range calculated for canonical device parameters.

Tavlykaev and Ramaswamy also indicated that the two-section YFDCM maintains high suppression of the intermodulation distortion over a larger range of S_1 and S_2 values, but they did not consider the dynamic range. The contour plot of IM3 versus the values of S_1 and S_2 given by Tavlykaev and Ramaswamy is shown in Figure 3.28a. Regions where the IM3 is suppressed have a light shade and regions of large intermodulation distortion have a dark shade. Overlain on that contour plot are the ridges of peak SFDR shown in Figure 3.28b. Note that the points having minimum IM3 are not necessarily the points having maximum SFDR. We have investigated the sensitivity of the SFDR to possible fabrication errors in S_1 and S_2. We calculated dynamic range as a function of S_1 keeping S_2 constant and vice versa around the optimum values shown in Figure 3.28a to see if the decrease in dynamic range is less sensitive

for the two-section modulator than for the single section modulator. The range of S_1 and S_2 values used in these calculations are shown as the short horizontal or vertical bars in Figure 3.28b. The results are given in Figure 3.29. Consider the sensitivity of the SFDR to the values for S_1 and S_2 of a two-section device compared with the sensitivity to the value for *s* of a single-section device. We define, for the sake of this comparison, this sensitivity as the deviation in *s*, S_1 or S_2 that will degrade the SFDR by 3 dB from its peak value. It appears that in some (but not all) cases a 10% to 20% relaxation in sensitivity can be realized for the two-section device when compared with a single-section device.

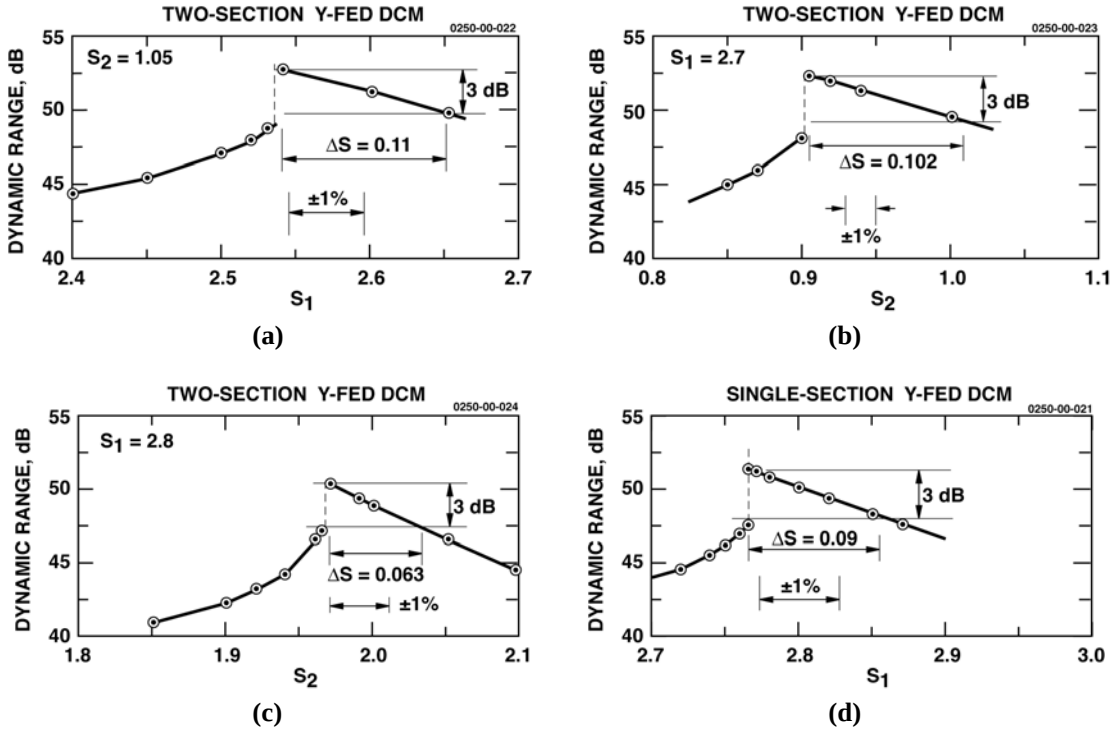


Figure 3.29 Dependence of estimated spur free dynamic range on section lengths S_1 (a) or S_2 (b,c) around the optimum solutions indicated in Figure 3.27b. The dependence of dynamic range on s for a single section Y-fed DCM is shown in (d) for comparison. These cuts are also indicated as short bars in Figure 3.27b. The range of s, S1 or S2 that results in a 3 dB change in dynamic range is also indicated in the figure, along with a range representing a ± 1% change in s, S1 or S2.

As we were performing the theoretical analyses, we also were developing the fabrication process for the two-section YFDC devices in a parallel effort. Two section devices were fabricated on some of the YFDCM wafers. Figure 3.30 shows the measured transfer functions and two-tone modulation response curves obtained for a two-section YFDCM, device 775d1b_y41x1g1. The lengths of the two sections are L_1=31.8mm and L_2=9.3mm. The transfer functions for this two-section device are more complicated than the transfer functions for a single-section device. Note that the voltage excursion needed to swing the output between the maximum and the minimum values is smaller, only 8 to 8.5 volts. The amount of this reduction in voltage swing is consistent with the longer total length of the RF modulation section. The reason for this voltage reduction is not yet fully understood. The transfer functions appear to

have an offset of approximately –2 volts. The two-tone modulation measurements were done with a bias voltage of –1.8 volts applied to the device, which is needed to reduce the power of the 2nd harmonic components below the power of the intermodulation distortion components. The curves for the 3rd-order distortion components have a slope of 5 or more at the higher input powers. This region of the curves is separated from the slope 3 region, which occurs at the low input powers, by a deep notch. The intermodulation distortion is suppressed to a large degree, by at least 40 dBc, at the modulation voltage of the notch. Note that a notch also is evident in the curves for the 2nd harmonic components.

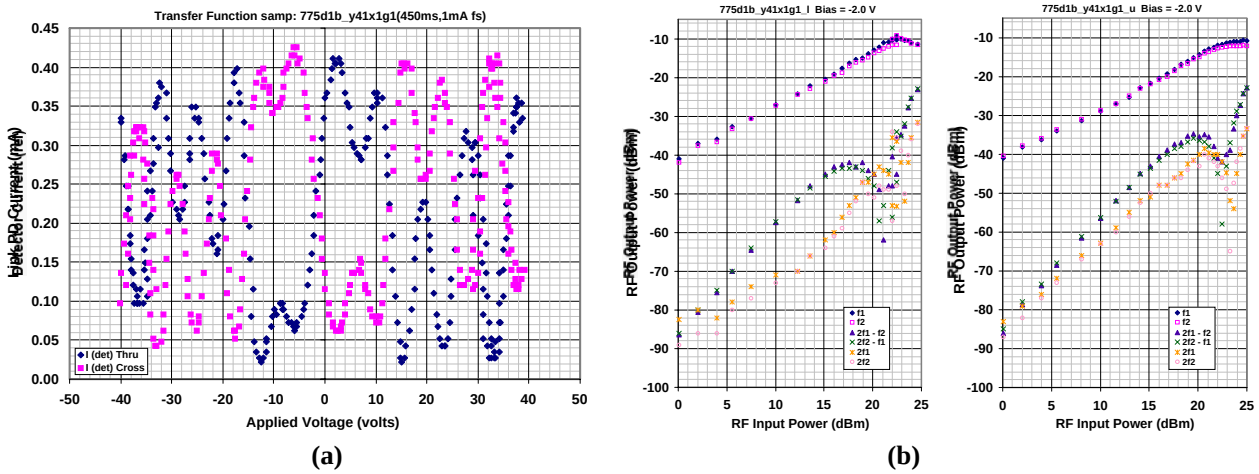


Figure 3.30 Measured characteristics of two-section YFDC device, showing (a) transfer functions for the two complementary outputs and (b) two-tone modulation responses for these two outputs.

Note from Figure 3.30a that the transfer functions for the two outputs are not exactly complementary. The output for the "cross" arm, port 2, is more symmetric than the output for the "thru" arm, port 1. The two-tone responses for both output arms have curves for the IM3 components that have a notch and a region with slope greater than 3. However, those response curves differ from each other both in the input power level at which the notch occurs and the height of the peak on the low-power side of the notch. Thus, although enhanced linearity has been demonstrated on some YFDCM, for both single-section and multi-section devices, the fabrication processes for these devices were not under sufficient control to produce enhanced-linearity YFDCM in a highly repeatable and symmetric manner. One problem we have observed in the fabrication of the current YFDCM wafers, for both the single-section and the multi-section devices, is that in some wafers the electrodes are not aligned perfectly over the waveguides for the entire length of the RF modulation section. Also, on some of the wafers, the width of the electrodes and thus also their spacing varies along the device. This misalignment and longitudinal variation in the overlap between the optical field in the coupled waveguides and the applied electric field causes the modulation voltage to vary over the length of the device. The thickness of the titanium deposited for the waveguides varies along the 3-4 cm active length of the devices, causing a fluctuation in κ (and l) along the device. The effects of fluctuation such these in x and κ along the length of the YFDCM has been investigated in prior studies and were

shown to degrade the suppression of the intermodulation distortion.[19] Thus, our prior problems with the electrode fabrication and titanium deposition likely reduced our yield of devices having enhanced linearity. However, we have a modified fabrication process, using already established in-house processing techniques and equipment, that is expected to improve the reproducibility and fabrication yield of devices having suitably enhanced linearity and SFDR.

SECTION 4

PHOTONIC BANDPASS ΔΣ InP-HBT ANALOG-TO-DIGITAL CONVERTER

This Section describes our development of photonic bandpass ΔΣ InP-HBT ADCs. Specifically, we combined the high resolution quantization capability of ΔΣ ADCs and the low-jitter sampling capability of mode-locked (ML) pulses to demonstrate the direct digitization of X-band (8 – 12 GHz) signals. Presently, the A/D conversion of these high frequency signals is accomplished by downconverting them to intermediate frequencies (IF), using cascades of well-matched mixers, RF-filters and high quality local oscillators (LO). After frequency downconversion, the analog signal could then be digitized with high resolution via the adoption of oversampling and noise-shaping approaches, as in ΔΣ analog-to-digital converters (ADC). A direct sampling approach that reduces the number of downconversion mixers - but maintains the A/D conversion resolution - will greatly simplify the system architecture and implementation of digital receivers. In this Section, we describe a photonic A/D conversion approach that utilizes the harmonics of low-jitter picosecond pulses to *downsample* analog signal-inputs at high frequencies. In our approach, the photonic sampling process itself "downconverts" the high frequency analog-input to a lower frequency signal that falls within the quantization notch (bandpass) of a ΔΣ ADC. The organization of this Section is as follows. Section 4.A discusses the basic architecture of bandpass ΔΣ ADCs and its circuit implementation using HRL's InP-HBT technology. Section 4.B presents our test data for the fabricated InP-HBT bandpass ΔΣ ADCs.

4.A InP-HBT ΔΣ Analog-to-Digital Converters

4.A.1 Architecture and Design of ΔΣ Modulators

A conventional ADC's quantization noise is spread evenly over the signal bandwidth. This is illustrated in Fig.4.1.

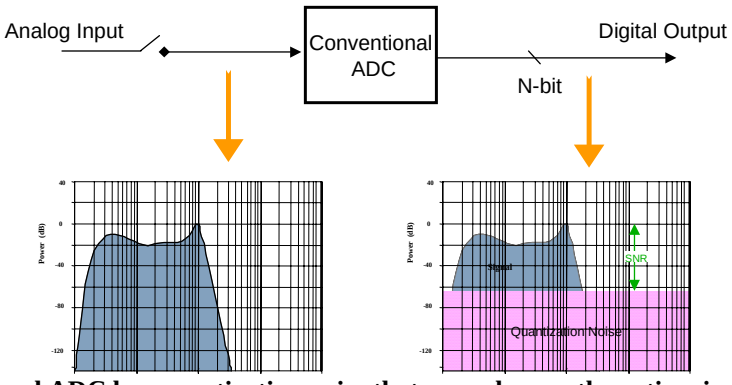


Figure 4.1 A conventional ADC has quantization noise that spreads over the entire signal bandwidth of interest.

As illustrated, the signal-to-noise ratio at the ADC output is degraded by the quantization noise. Furthermore, a low-amplitude signal buried by the quantization noise cannot be recovered by any digital processing. In contrast, a ΔΣ ADC uses a high-gain loop filter inside a feedback circuit to shape the quantization noise, so that a large fraction of the noise lies outside the signal bandwidth. This is illustrated in Fig.4.2, and in the upper figure of Fig. 4.3. As a result, A/D conversion can be accomplished with a high signal-to-noise ratio (SNR) inside the ΔΣ ADC's passband frequencies. This high resolution, noise-shaped A/D conversion process is illustrated for a lowpass ΔΣ ADC in the upper part of Fig.4.3. Using post digital filtering, one can now recover the low level signal located in the ADC's ΔΣ passband, where the quantization noise is low. Therefore, within a targeted signal bandwidth, a ΔΣ ADC can typically achieve much higher SNR than ADCs of other architectures.

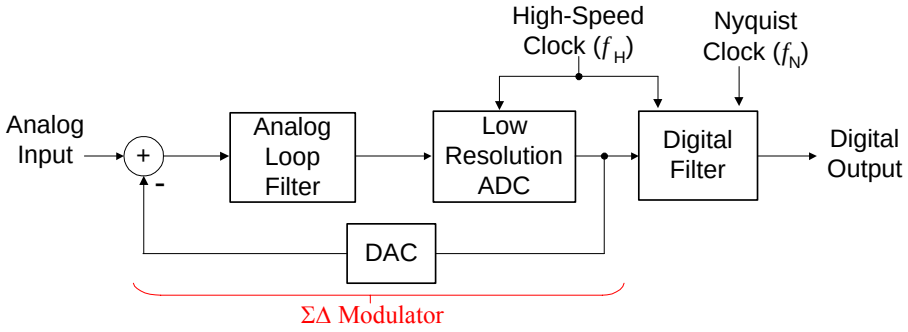


Figure 4.2 Architecture of a ΔΣ ADC. The part marked ΣΔ Modulator was implemented as an InP-HBT circuit in our Program.

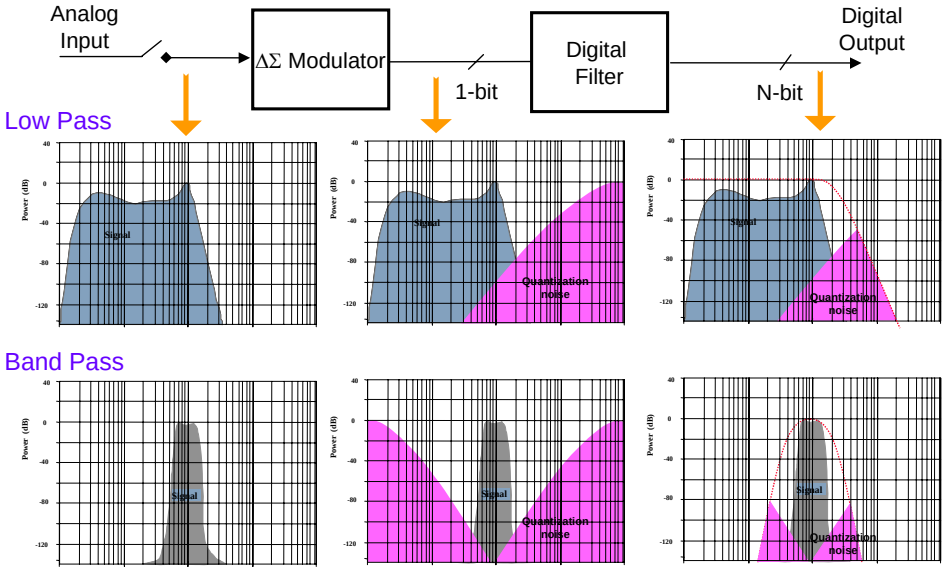


Figure 4.3 A ΔΣ ADC shapes the quantization noise so that it lies outside the signal bandwidth. After post digital filtering, very high resolution (signal-to-noise ratio) A/D conversion can be achieved.

An important feature of ΔΣ ADC is its capability to be adopted as a bandpass ADC. Specifically, a bandpass ADC can digitize a narrowband signal modulated on a high frequency carrier, without downconverting it to baseband (i.e. close to DC). The lower figure of Fig.4.3 illustrates the formation of a quantization notch (at the carrier frequency of the signal) in a bandpass ΔΣ ADC, so that one can accomplish A/D conversion with high signal-to-noise ratio (SNR) within the ΔΣ ADC's passband. Hence, the use of a bandpass ADC avoids the incurrence of extra noise and distortions in a multi-stage mixer-based downconversion process.

Figure 4.4 illustrates the architecture of the 4th-order, single-bit bandpass ΔΣ modulator we adopted for this Program. In particular, it was a Gm-C type continuous-time ΔΣ modulator. This 4th-order bandpass ΔΣ modulator consisted of two Gm-C type resonators (each with two integrators and two Gm-cells, g_{m1} & g_{m3}) to form two notches (see Figure 4.4). The frequency tuning of the two notches were achieved by varying the gains of the g_{m3} cell in the feedback path of the resonator. Four Gm cells (g_{mf}) formed the distributed feed-forward paths and their outputs were wired together to the comparator (1-bit quantizer). The feedback DAC was composed of a differential pair and a constant, but tunable current sink.

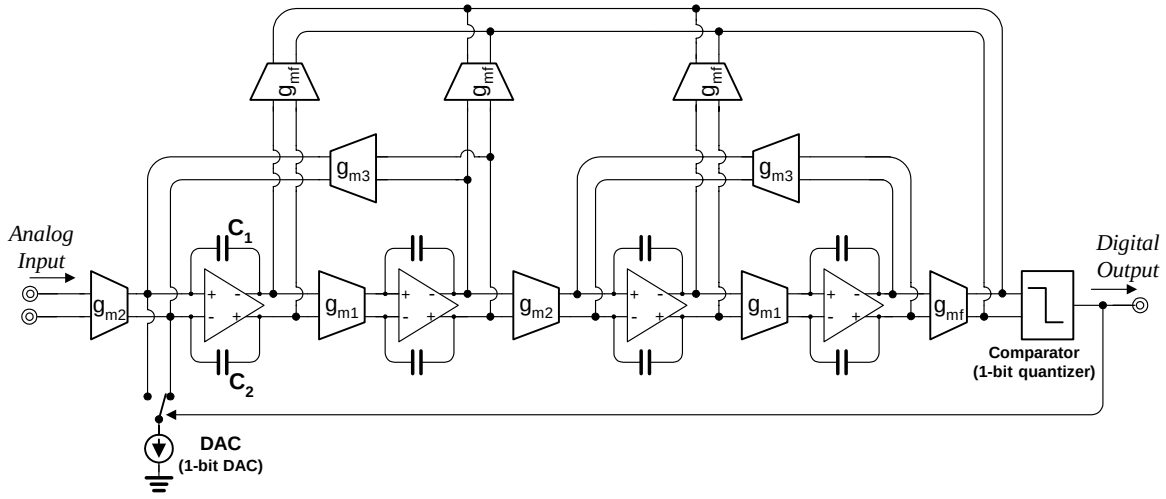


Figure 4.4 Architecture of the 4th-order single-bit Bandpass ΔΣ modulator.

To accomplish photonic sampling with mode-locked laser pulses, we integrated two InGaAs photodiodes, as differential pair, to convert the optical inputs into electrical signals. Figure 4.5 shows the implementation of such a photonic bandpass ΔΣ ADC. As shown, the input Gm cell (g_{m2}) was replaced by a pair of differential photodiodes.

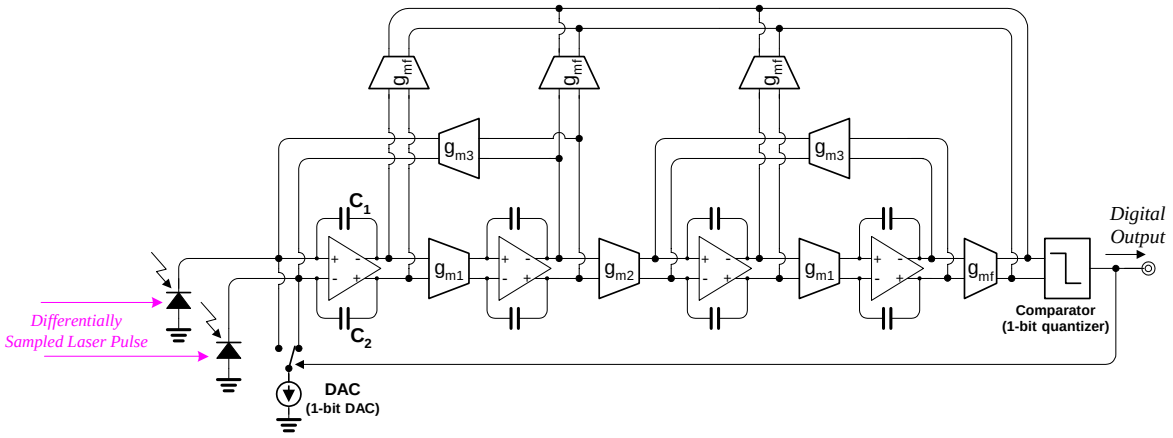


Figure 4.5 Photonic ΔΣ modulator integrated with a pair of differential photodiodes.

The photodiodes and the single-bit bandpass ΔΣ modulator were designed and fabricated in-house with HRL Laboratories' second-generation photonic InP heterojunction bipolar transistor (HBT) process. This photonic InP process supports a transistor f_T of 150 GHz and f_{MAX} of 180 GHz, with a minimum feature size of 1 μm. The circuit was implemented with 1263 InP HBT transistors with an active area of 1800 μm x 1300 μm and a die size of 3200 x 1880 μm. Figure 4.6 shows the transistor count of each component in the modulator.

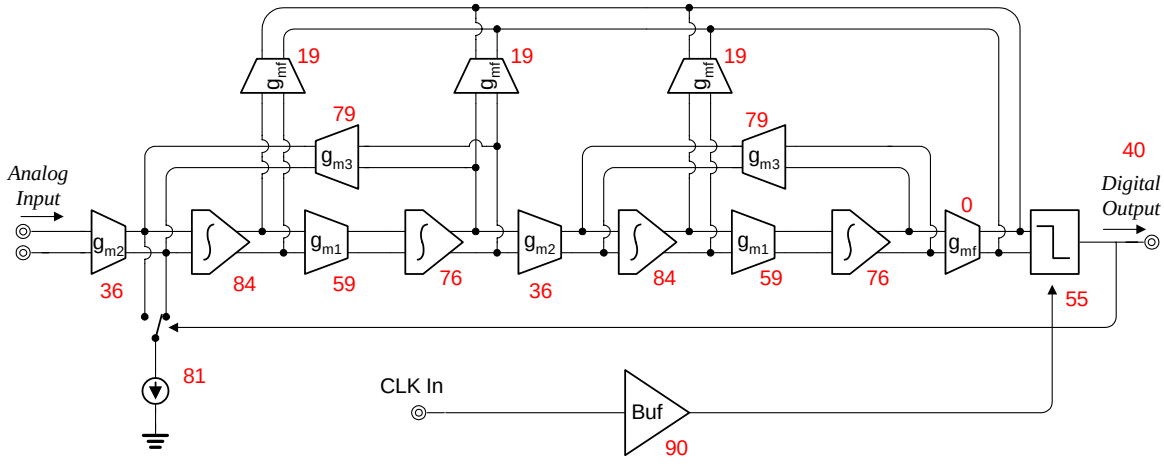


Figure 4.6 Schematic illustrating transistor count of each components in the ΔΣ modulator.

In total, 12 different bandpass ΔΣ modulators had been designed and fabricated. Figure 4.7 shows the layout of the 12 different modulator circuits that formed one reticle of a processed

InP-HBT wafer. The nominal IF frequency for the quantization notch was ~2 GHz. These 12 modulators (with sampling frequency Fs) were:

- All electrical 10 GHz Fs, 2 GHz IF ΔΣ ADC
- All electrical 10 GHz Fs, 2GHz IF, wide bandwidth (300MHz) ΔΣ ADC
- All electrical 10 GHz Fs, 2.5GHz IF ΔΣ ADC
- All electrical 10 GHz Fs, 2GHz IF, optimized for higher IF ΔΣ ADC
- All electrical 10 GHz Fs, 2.5GHz IF, optimized for higher IF ΔΣ ADC
- All electrical open loop 2GHz IF ΔΣ ADC for testing the loop filter
- 10 GHz Fs, 2GHz IF w/ photonic signal input ΔΣ ADC
- 10 GHz Fs, 2GHz IF w/ photonic clocked DAC ΔΣ ADC
- All electrical 20 GHz Fs, 2GHz IF ΔΣ ADC
- All electrical 20 GHz Fs, 2GHz IF w/ external adjustable DAC clock ΔΣ ADC
- 20 GHz Fs, 2GHz IF w/ photonic clocked DAC ΔΣ ADC
- 20 GHz Fs, 2GHz IF w/ photonic sampled signal & clocked DAC ΔΣ ADC

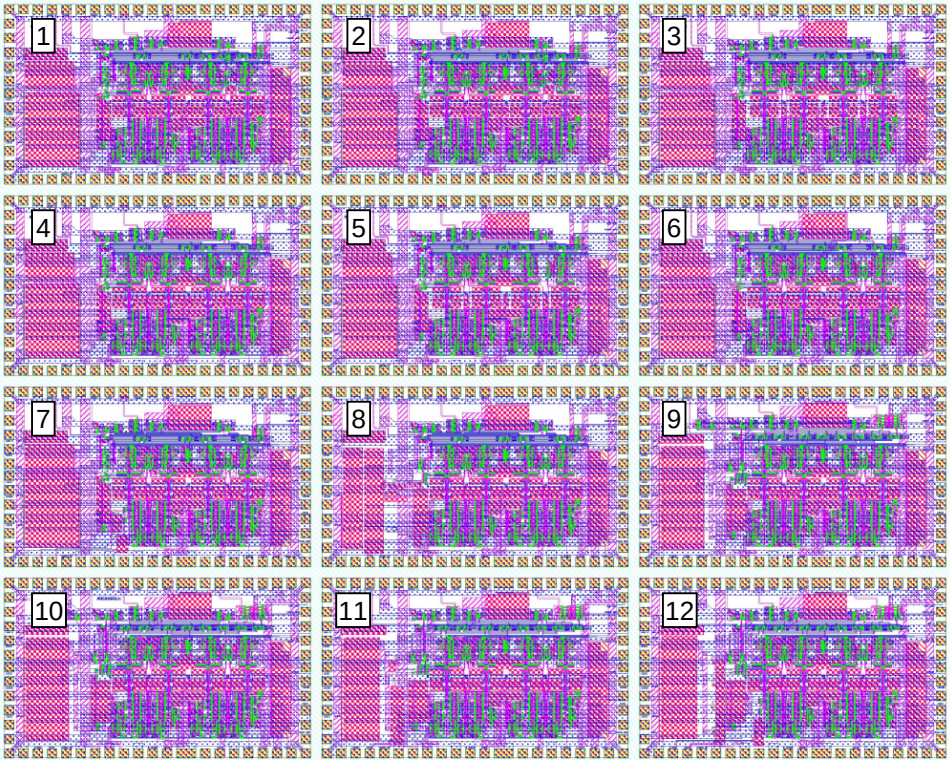


Figure 4.7 Layout of 12 different ΔΣ modulators implemented using HRL InP-HBT technology.

Figure 4.8 shows the photograph of a fabricated InP wafer, which was 3 inches in diameter with 38 reticles.

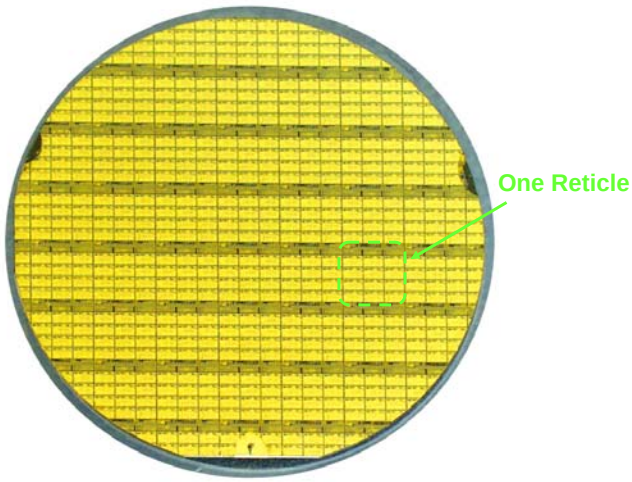


Figure 4.8 Photograph of a finished 3-inch InP-HBT OEIC wafer with photonic ΔΣ modulator circuit fabricated.

Figure 4.9 shows the die photograph of an f_s =10 GHz, IF = 2 GHz photonic ΔΣ modulator. The modulator circuit had a die size of 3200μm x 1800μm, with 1263 InP HBT transistors.

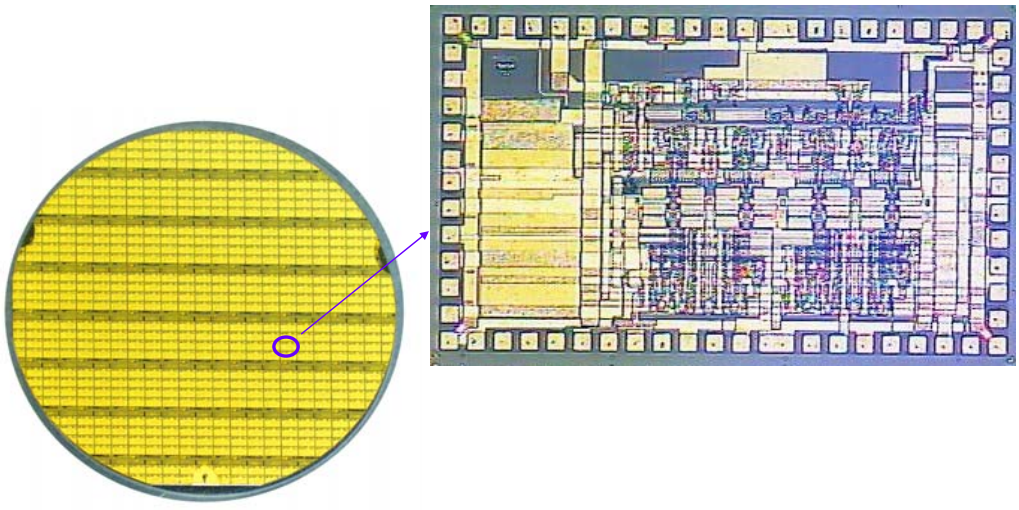


Figure 4.9 Die photo of the photonic ΔΣ modulator.

4.A.2 Design and Fabrication of Photonic ΔΣ Modulator

As mentioned earlier, present digital receivers used in radar or satellite communication systems for high frequency signals (> 10GHz) require multi-stage down conversion before the digitizer. The implementation of such a downconversion architecture involves many well-matched mixers, filters, and high quality local oscillators. The incorporation of all these components in the digital receiver adds cost, size, and power consumption. Moreover, they require careful calibration before delivery.

A direct sampling ADC will reduce a substantial fraction of the cost, power consumption, and hardware complexity, as well as labor involved in calibrating a digital receiver before its system insertion. However, the resolution obtained in previous direct sampling schemes for high frequency signals is typically degraded by signal-dependent jitter in the front-end electronic sampler. In particular, the switching threshold of most electronic input sampler is modulated by the input signal. This *signal-induced* input-sampling jitter is therefore signal-dependent, and reduces significantly the A/D conversion resolution for high frequency analog-inputs. Conventional direct sampling also requires high power consumption to minimize distortion incurred in the input sampling of a high frequency signal. In our photonic approach, we used low-jitter photonic sampling (see Section 2) in conjunction with a continuous-time bandpass ΔΣ modulator to accomplish direct sampling. To be specific, the ΔΣ modulator OEIC was integrated with a pair of differential photodiodes to receive modulated picosecond pulses. We demonstrated that it can be utilized to directly digitize very-high frequency signal, *without* the employment of input electronic sampling, or down-conversion using mixers.

Figure 4.10 shows the block diagram of such a photonic ΔΣ modulator.

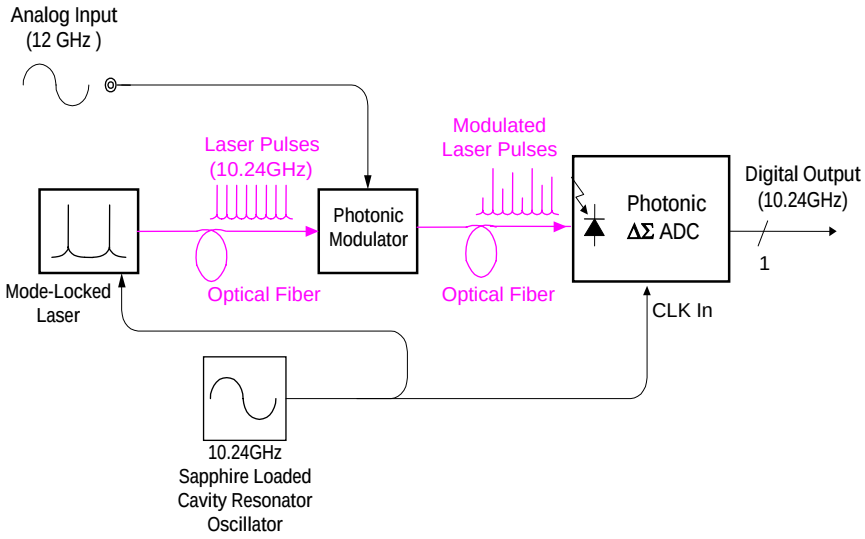


Figure 4.10 Architecture of photonically sampled ΔΣ ADC.

A fiber laser, mode-locked [see Section 2.A.3] via synchronization with a sapphire-loaded cavity resonator, was used to generate a train of low-jitter picosecond pulses (~ 3–5 psec wide). The mode-locked pulses were subsequently fed to a $LiNbO_3$ optical modulator with a bandwidth of ~12 GHz. In the optical modulator, the picosecond pulses were intensity-modulated by the electrical input signal (~ 12GHz) into complementary optical outputs. Using a pair of length-matched optical fibers, these two laser outputs were fed to a pair of differential InGaAs photodiodes integrated on-chip the ΔΣ modulator. These two on-chip photodiodes then converted the modulated ML pulses into electrical charges, which we fed directly to the first stage integrator of the ΔΣ modulator.

In our experiment, the mode-locked laser generated very short (3~5 psec) pulses, which should enable us to downsample analog input signals with frequencies as high as ~100 GHz. However, the optical modulator used in our experiments possessed a cut-off frequency of 12 GHz. Using the modulator at hand, we demonstrated the direct sampling of an analog-input at f_{in} ~ 12GHz. Our mode-locked pulses had an integrated timing jitter of 8.28 fsec, which would support a photonic sampling resolution of 11.9 bits (in a 1 MHz bandwidth), for a signal-input at 12 GHz [see Section 2]. Since the optical modulator only modulates the amplitude (power) of the mode-locked pulses and not its timing, photonic sampling *does not* introduce extra aperture jitter.

The photodiodes and the single-bit bandpass ΔΣ modulator were fabricated in house with HRL Laboratories' second-generation photonic InP heterojunction bipolar transistor (HBT) process. The integrated GaInAs photodiodes (see also Section VI), formed by the base-collector junction of an InP HBT, had an aperture size of 20 μm in diameter (see Figure 4.11).

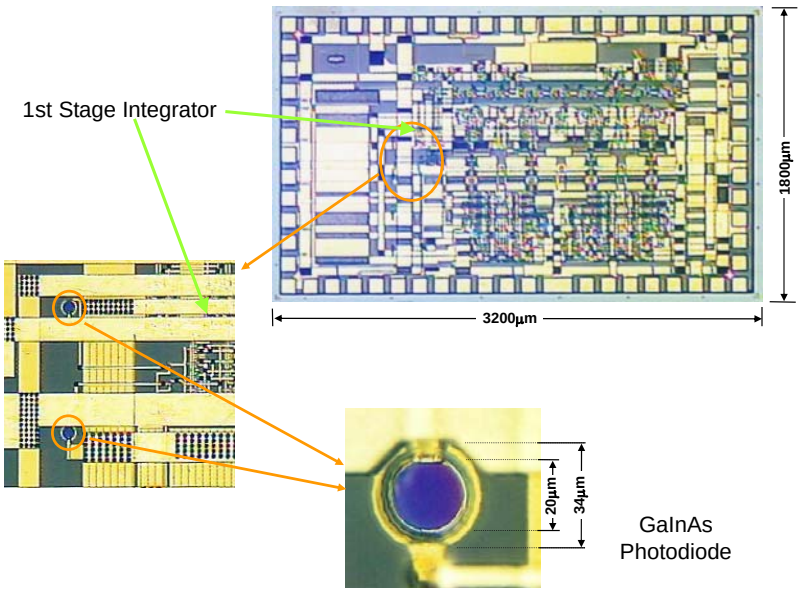


Figure 4.11 Integrated GaInAs photodiodes fabricated with a separation of less than 100 μm from the 1st stage integrator of the HRL photonic ΔΣ Modulator.

The output currents of the integrated photodiodes were directly coupled to the inputs of the first stage integrator, and then integrated onto the integration-capacitors (**C_1** & **C_2** in Figure 4.4). In addition, these photodiodes were fabricated with a separation that was less than 100μm away from the first stage integrator, so that transmission loss and reflection for the photocurrents derived from short pulse excitation could be minimized. The virtually-grounded input nodes of the first stage integrator also offered very low impedance to the photodiodes, and was able to collect the very high speed photocurrents without much capacitive attenuation. Since our ΔΣ modulator was a continuous-time ΔΣ modulator, it did not require input electronic sampling, and therefore did not suffer the signal-dependent sampling jitter we discussed above.

In addition, the bandpass ΔΣ modulator designed for this Program possessed a very high passband (notch) frequency (1.4 ~ 2GHz) for ease of anti-alias filtering. Operating at a 1.76 GHz passband frequency, the closest alias signal would be located 3.52 GHz away. The high notch frequency is particularly advantageous when we directly sample very high frequency signals - such as Q, V, or W-band signals - with a wideband photonic modulator, because we need not implement a very high-Q or delicate filter design to attenuate the alias. The high notch frequency mentioned above requires, however, very high transconductance for the Gm cells, and hence, higher power consumption. In our design, C is 2.5pF and Gm is about 30mS.

Since the analog-input to our photonic ΔΣ ADC was first modulated onto the picosecond pulse train, and then photodetected, we also characterized the photodetection linearity of these integrated photodiodes to ensure that any intermodulation products generated in the photodetection process does not degrade the spur free dynamic range of the A/D conversion. Specifically, these on-chip InGaAs detectors were fabricated from the base-collector junctions of InP-HBTs. Below, we present data obtained on the bandwidth and photodetection linearity of the integrated photodetectors. Figure 4.12 shows the RF-response and 3rd order intermodulation products (IM3) measured via the optical heterodyning of λ = 1300 nm Nd:YAG lasers.

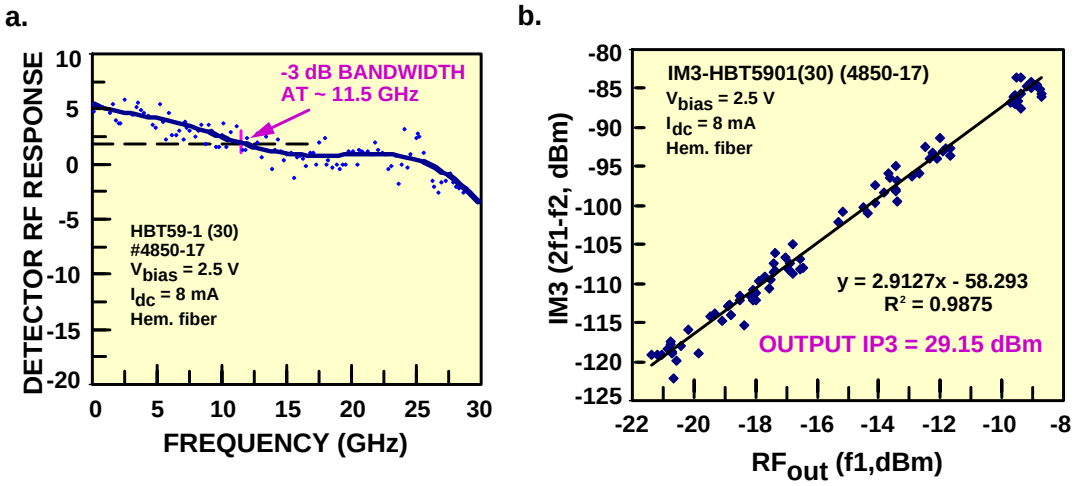


Fig. 4.12 Bandwidth and 3rd order intermodulation product (IM3) of photodiodes integrated on InP-HBT OEIC ADCs. Both sets of measurements were measured at a DC photocurrent level of I_{dc} = 8 mA. a. RF-response vs frequency b. RF power of 3rd order intermodulation product (2f1-f2) vs RF power of the fundamental (f1).

Fig.4.12a shows the photodetector RF-response, measured at a DC photocurrent I_{dc} of 8 mA, for an integrated photodiode. As shown, we measured a –3 dB bandwidth of ~11.5 GHz. Next, we generated RF-outputs at the fundamental frequencies f1, f2 (at ~ 8.7 GHz) and the inband IM3 frequencies 2f1-f2, 2f2-f1 (at ~ 8.7 GHz) via the optical heterodyning of two pairs of $\lambda = 1300$ nm Nd:YAG lasers. Fig. 4.12b shows a plot of the RF-power we measured for the IM3 (at 2f1-f2) vs the fundamental (f1) obtained from the photodiode output. As our data shows, the output 3rd order intercept of these integrated photodiodes demonstrated an excellent value of 29.15 dBm. Based on these measurements, we conclude that any IM3 generated in the photodetection process would be at least 15 dB below the fundamental signal in our A/D conversion experiments.

4.B Characterization of InP-HBT Photonic ΔΣ Modulator OEIC

Figure 4.13 shows the block diagram of our test setup for the photonic ΔΣ modulator. First, we fed part of the output from the ΔΣ modulator to an RF spectrum analyzer (RFSA), so that the its noise shaping characteristics can be monitored as we adjusted the ΔΣ modulator circuit's operating parameters. Simultaneously, we fed part of the circuit's output to a 50 GHz sampling scope (Tektronix CSA 8000) for a continuous monitoring of the eye-diagram derived from the ΔΣ modulator's (time-domain) digital output pattern.

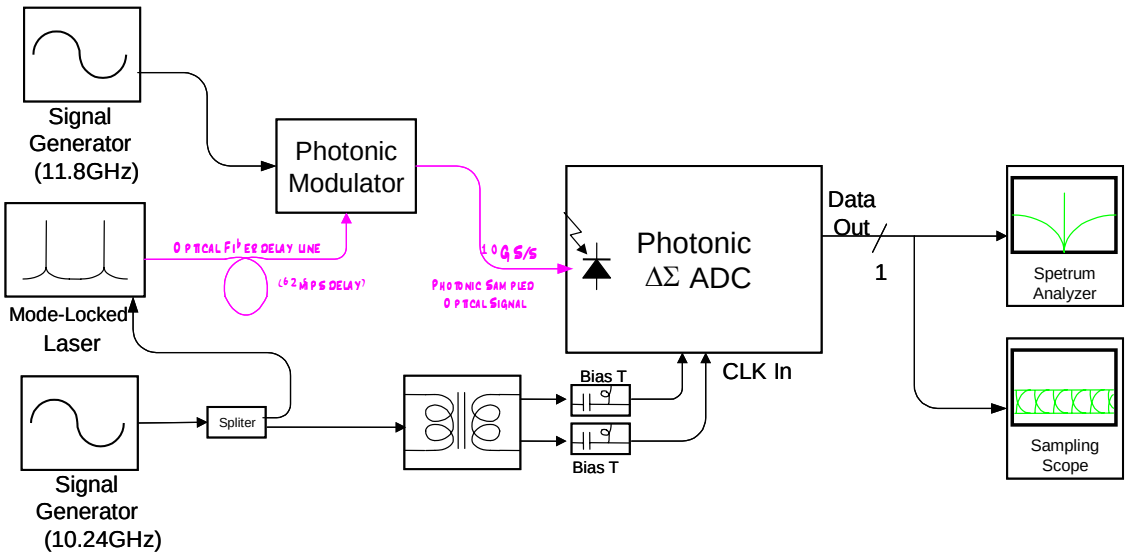


Figure 4.13 Test setup for the photonically sampled InP-HBT ΔΣ modulator OEIC.

Figure 4.14 shows a photograph of the probe-card we used to test, on a probe station, a finished wafer of photonic ΔΣ circuits. Our test setup is shown in Figure 4.15. The left and right figures of Figure 4.16 show, respectively, a screen shot of the display derived from the RF spectrum analyzer and the CSA 8000 sampling scope.

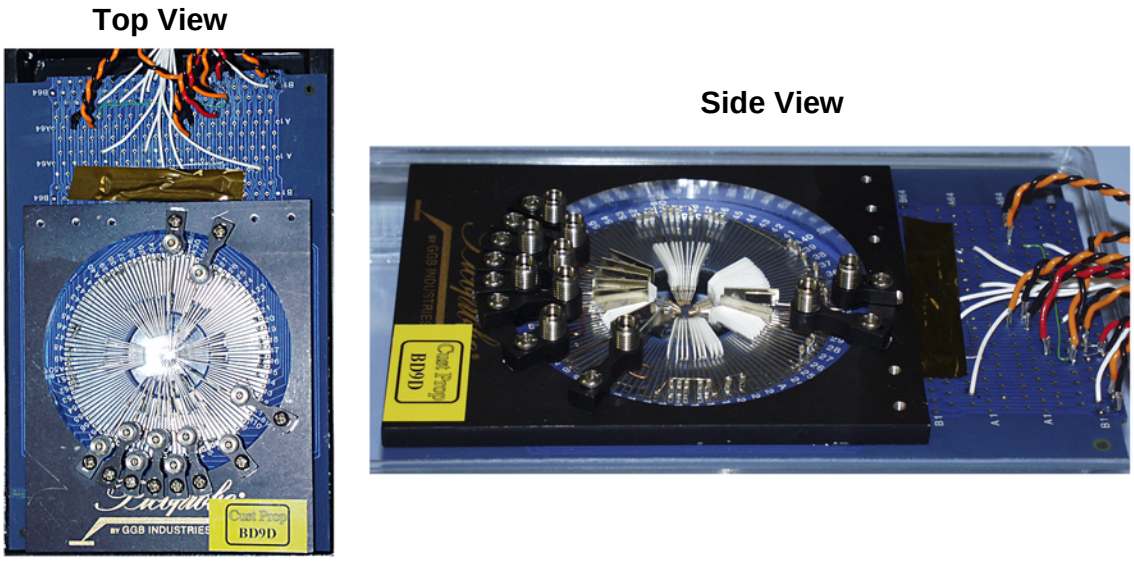


Figure 4.14 Photograph of probe card used to test a photonic ΔΣ modulator OEIC.

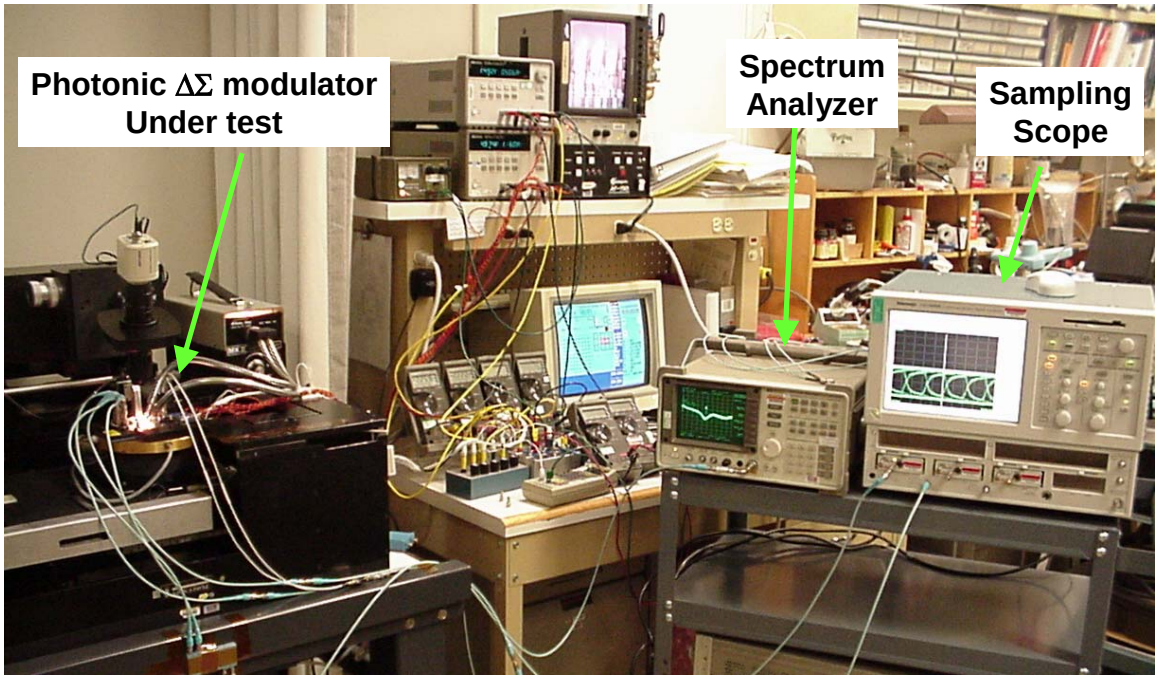


Figure 4.15 Photograph of test setup for the InP-HBT ΔΣ Modulator circuit.

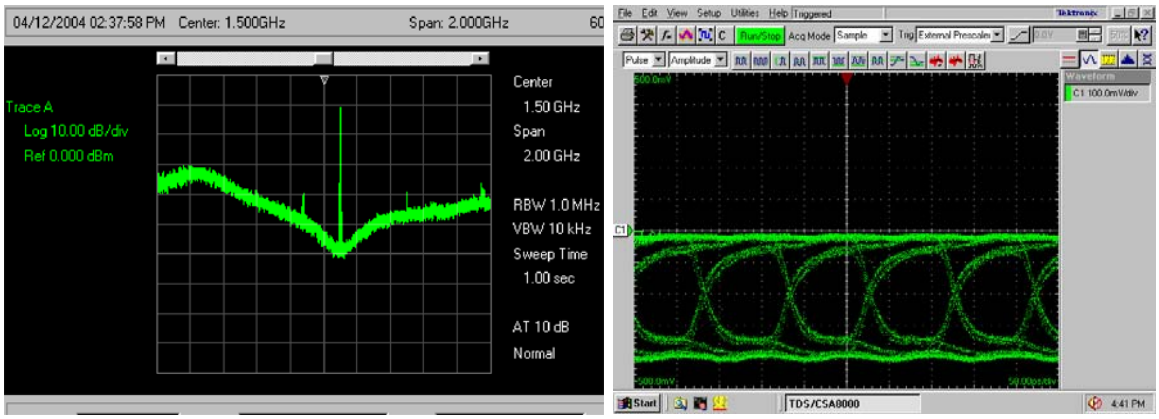


Figure 4.16 Screen shot of the ΔΣ OEIC output using (i) an RF spectrum analyzer (left figure) and (ii) a 50 GHz sampling scope (right figure).

To capture the digital output from the ΔΣ modulator, we fed the signal to a 1:16 demultiplexing circuit to reduce the clock rate to 640MHz. The demultiplexed output was then captured by a logic analyzer, and finally sent to a PC to perform an FFT analysis of the recorded digital data. Figure 4.17 and Figure 4.18 shows, respectively, the block diagram and photograph of our test setup for capturing digital data from the ΔΣ modulator OEIC.

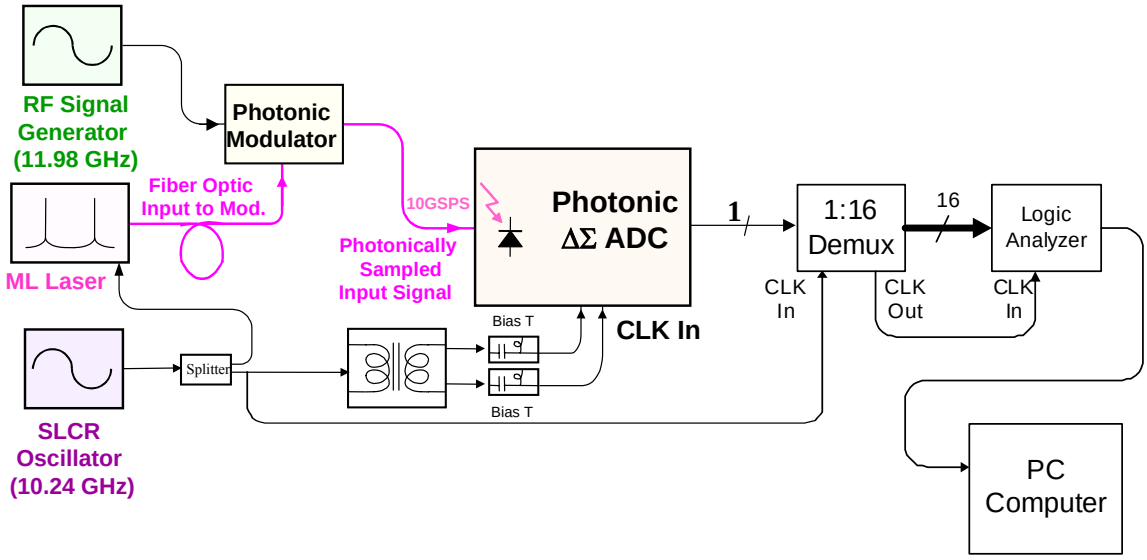


Figure 4.17 Test setup for capturing and processing the digital output of the photonically sampled ΔΣ modulator OEIC.

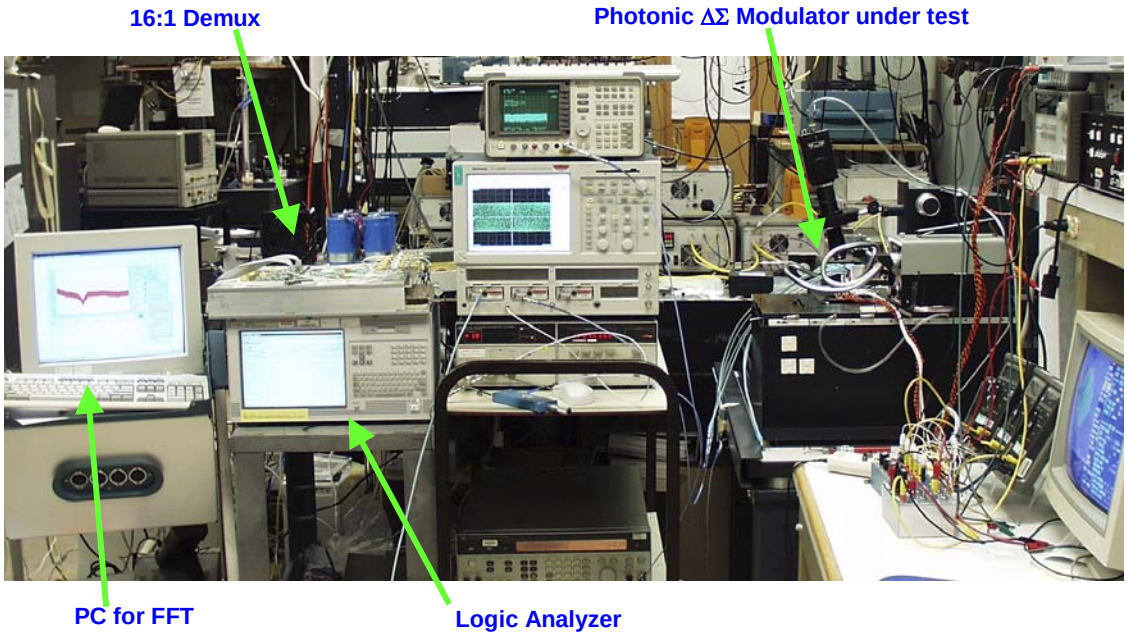


Figure 4.18 Photograph of our test setup for capturing the digital output of the ΔΣ modulator OEIC that received photonically sampled optical inputs.

Specifically, the bandpass ΔΣ modulator had a tunable passband (quantization notch) frequency that ranged from 1.4 GHz to 2 GHz. It could also be operated with a sampling rate that ranged from 7 GHz to 12 GHz. First, we show in Figure 4.19, the computed FFT of an all-electrical version of the ΔΣ modulator that sampled at 8 GHz, for a 1.6 GHz analog-input. As shown, the measured peak SNR with an 8 GHz sampling rate and a 1.6 GHz analog-input was 57.67 dB.

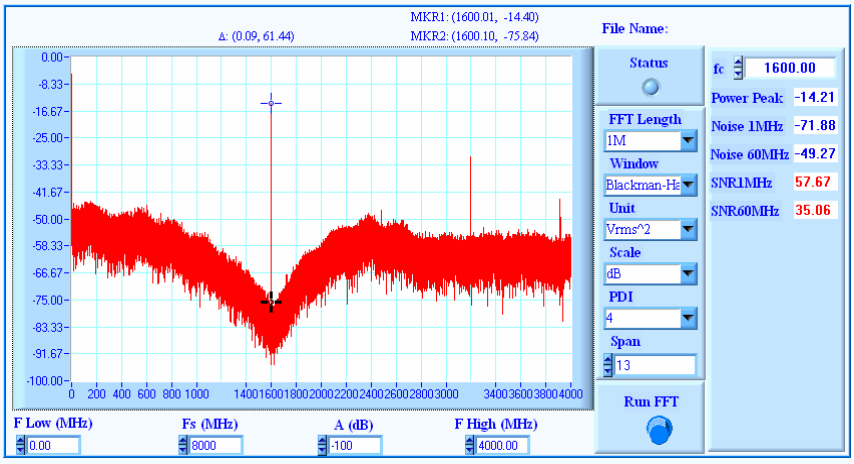


Figure 4.19 FFT computed for an all-electrical version of the ΔΣ modulator: for an 8 GHz sampling rate and a 1.6 GHz analog input.

Next, Figure 4.20 shows the measured FFT of 64K-samples for a ΔΣ modulator that received a photonically sampled 1.75 GHz signal at a clock rate of 10.24 GHz. As shown, the notch frequency of our ΔΣ modulator was located at 1.75GHz. Figure 4.21 plots the measured signal-to-noise ratio (SNR) in a 1 MHz bandwidth vs, RF-input level to the ADC. As shown, it achieved a peak SNR of 58.1dB in a 1 MHz bandwidth.

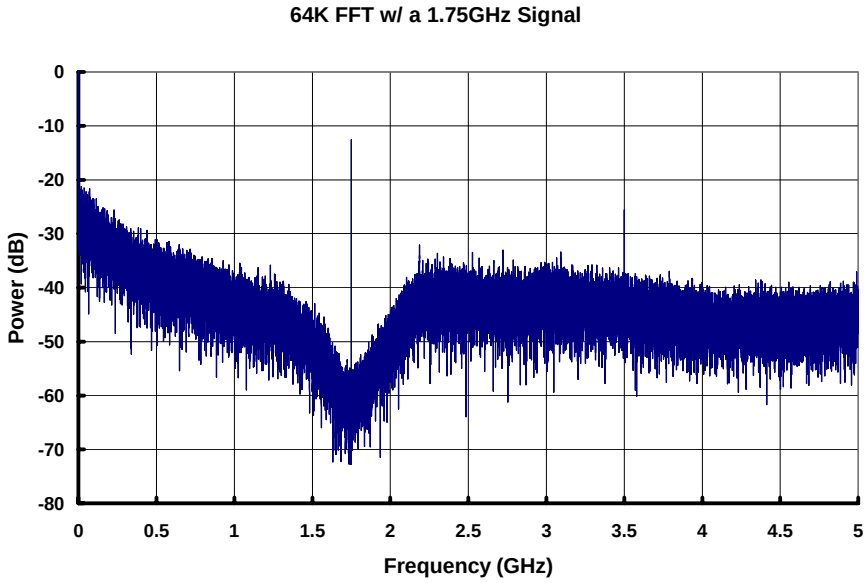


Figure 4.20 A 64K-sample FFT computed from the ΔΣ ADC output: for a 1.75GHz analog input, photonically sampled at f_s = 10.24GHz. The notch frequency of the ΔΣ modulator was also at 1.75 GHz.

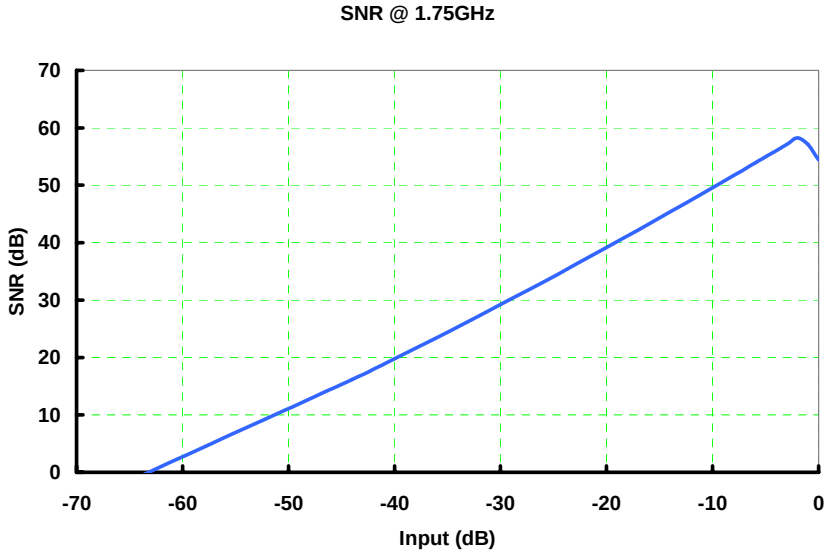


Figure 4.21 Measured SNR for a 1.75GHz analog input, photonically sampled at 10.24 GHz.

Finally, Figure 4.22 shows the FFT (64K-sample) computed for digital data captured for an 11.98 GHz analog input signal, sampled photonically at a 10.24 GHz clock-rate. Notice that the notch frequency of the ΔΣ modulator was located at 1.76 GHz. These data demonstrated the *direct* sampling of an analog input via the use of ML picosecond pulses. Figure 4.23 shows the measured signal-to-noise ratio (in a 1 MHz bandwidth) vs. the ADC's RF-input level.

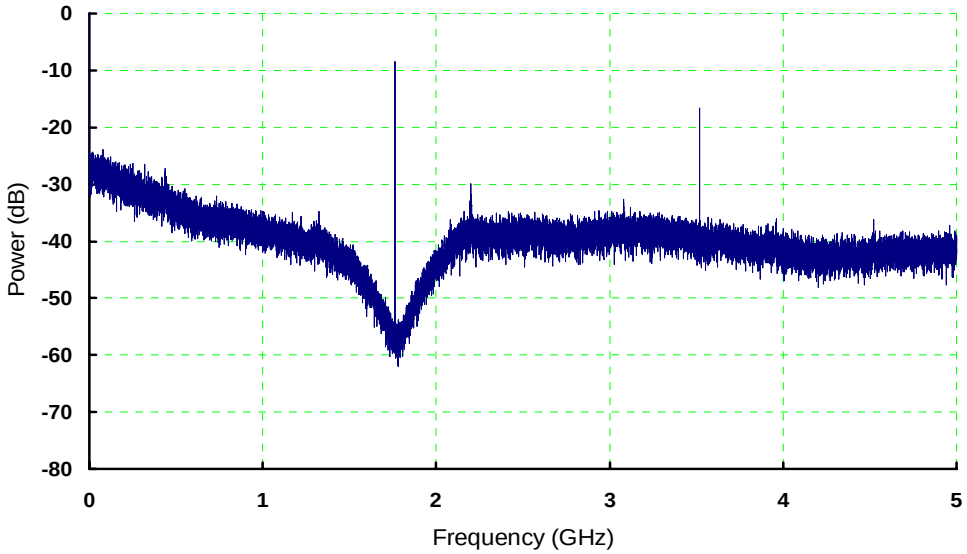


Figure 4.22 64K-sample FFT of photonic ΔΣ modulator circuit output: for an 11.98 GHz input signal, 1.76 GHz quantization notch, and a 10.24 GHz photonic sampling rate.

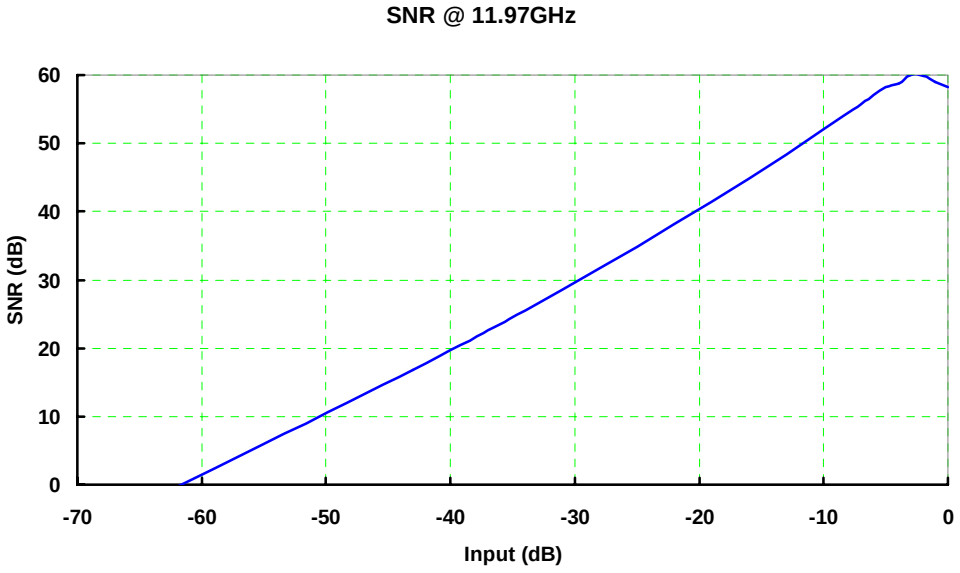


Figure 4.23 Measured SNR vs. input level for an 11.98 GHz input, photonically sampled at 10.24 GHz.

Specifically, we achieved a peak SNR of 59.9dB (in 1MHz bandwidth). The InP-HBT circuit consumed 7.4 W from $\pm$ 5V and 10V power supplies. The ΔΣ modulator circuit was implemented with 1263 InP HBT transistors with an active area of 1800 μm × 1300 μm and a die size of 3200 μm × 1880 μm. Table 1 summarizes the performance of this photonic ΔΣ modulator.

Table 4.1 Performance Summary of the Photonically-Sampled Bandpass ADC

Technology	HRL Laboratories 2nd generation 1um photonic InP HBT process
Transistor count	1263 HBT
Sampling frequency	10.24 GHz
Passband (notch) frequency	1.4 GHz ~ 2 GHz
Signal Bandwidth	1MHz
Maximum SNR	59.9 dB
Dynamic range	62 dB
Size	6 mm^2 (3200um x 1880um)
Power consumption	7.4 W

The photonic ΔΣ ADC described in this Section is compatible with antenna remoting and phased array radar applications. In these system architectures, only the LNA's and optical modulators need to be located at the antenna site. All the other components can be remoted via the employment of optical fiber links. Since the optical modulators are passive devices, only the LNA's consumes electrical power at the remoted antenna site. In summary, we demonstrated a direct-sampling ADC for a ~11.98 GHz analog input, using a f_s = 10.24 GHz photonic sampling rate and an InP-HBT bandpass ΔΣ ADC with a quantization notch at 1.76GHz. We achieved ~ 10 SNR-bits of resolution.

SECTION 5

DEMONSTRATION OF 40 GSPS PHOTONIC TIME-INTERLEAVED ARCHITECTURE

In this Section, we describe the use of wavelength-coded ($\tilde{\lambda}$coded) pulses to accomplish time-interleaved photonic A/D conversion at 40 GSPS. Specifically, our λ-coded pulses were generated by the spectral slicing of an optical supercontinuum that we formed, in turn, by compressing picosecond pulses from our mode-locked laser. We first introduce the concept of time-interleaved A/D conversion in Section 5.A. In this Section, we discuss, the origin and occurrence of alias-spurs during the implementation of time-interleaved A/D conversion architectures in general. We then present, in Section 5.B, the details of our WDM time-interleaved experiments. Section 5.B.1 describes the generation and jitter-evaluation of the 40 GHz $\tilde{\lambda}$coded pulses. In addition, we present results on their demultiplexing during time-interleaved A/D conversion. Finally, in Section 5.B.2, we describe 40 GSPS photonic time-interleaved experiments. In this Section, we report photonic A/D conversion at 40 GSPS, with a resolution of ~4 SFDR-bits.

5.A Introduction to Time-Interleaved Analog-to-Digital Conversion

Fig.5.1a shows a schematic that illustrates a basic time-interleaved ADC consisting of M (= 4) parallel channels. The aggregate sampling rate derived from these four time-interleaved channels is denoted f_s, which was 40 GHz in our experiment.

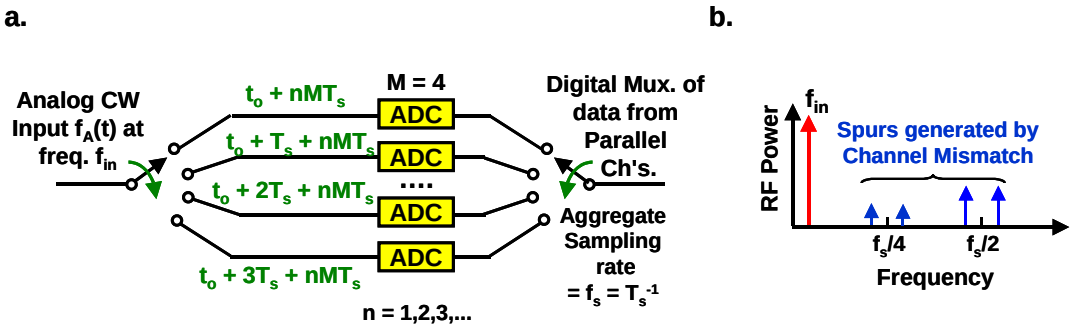


Fig. 5.1 a. Schematic of a Time-Interleaved ADC with M parallel channels (Ch's), b. Location of time-interleaved spurs due to channel mismatch.

As illustrated in the schematic, an analog sinusoidal input $f_A(t)$ (with frequency $f = f_{in}$) is first sampled successively by the four parallel ADCs, at time-intervals of T_s (= f_s^{-1}). Hence, each of the four time-interleaved ADCs performs A/D conversion at a lower sampling rate of $f_s/4$. At the output end of the four ADCs, we multiplex the discrete data streams $S_m(t)$ (m = 0, 1, 2, 3) from the four parallel channels to obtain - in a channel-interleaved sequence - a combined output S(t) that now has digitized samples separated by T_s. Thus, performing time-interleaved A/D

conversion with four parallel channels enables one to accomplish digitization at an aggregate sampling rate f_s that is four times the individual sampling rate (= $f_s/4$) of each channel. For example, one can now accomplish the 40 GSPS A/D conversion of an analog input at f_{in} = 17 GHz, via the time-interleaving of four parallel channels, each sampling at only 10 GSPS. If we assume perfect timing-offset between the four parallel channels, then the time-interleaved sampling process can be modeled with the following equation:

$$S(t) = \sum_{m=0}^{3} S_m(t) \qquad \text{where } S_m(t) = f_A(t) \cdot G_m \cdot \sum_n \delta(t - mT_s - nMT_s) \tag{5.1}$$

In the above equation, G_m denotes the channel-gain for the m^{th} time-interleaved channel (m = 0, 1, 2, 3 for M = 4). From Eq.5.1, we easily see that each time-interleaved channel samples at a rate of f_s/M, but is offset in its timing by precisely mT_s from the first channel (where m = 0). Therefore, for a sinusoidal analog input at f = f_{in}, each channel will form aliases [of $f_A(t)$] that are centered at integral multiples of their individual sampling rates of $f_K = K(f_s/4)$, where K is an integer. Thus, we expect to observe, in the frequency spectrum of $S_m(t)$, "alias-sidebands" at the frequencies $f_{SB} = f_K \pm f_{in}$. The timing-offset imposed between the four parallel channels will, however, create a π phase-shift between sidebands derived from selected channel-pairs (e.g. between Ch.1 and Ch.3). If the gains G_m of the four channels are *perfectly* matched (i.e. $G_m = G_0$), the complementary phase-shift between the sidebands of selected channel-pairs will lead to their cancellation in the summation for S(t) (see Eq. 5.1), *except* for the signal located at f_{in} and aliases separated from f_{in} by integral multiples of f_s. However, if some gain-mismatch exists between the time-interleaved channels, the sideband cancellation (for selected channel-pairs) will not be complete. As a result, interleave-spurs (due to aliasing within each channel) will now appear at f_{SB} in the frequency spectrum of the combined output S(t) (see Fig.5.1b). Likewise, one will observe alias-spurs at f_{SB} if there is imperfect timing-offset between the parallel channels. In Section 5.B.2, we will see how the A/D conversion resolution in our 40 GSPS photonic time-interleave ADC is limited to ~4 SFDR-bits by these channel-mismatch spurs. In the next Section, we first describe our wavelength division multiplexing (WDM) approach for demonstrating time-interleaved photonic ADC at 40 GSPS.

5.B Photonic Time-Interleaved Analog-to-Digital Conversion at 40 GSPS

In our photonic approach to accomplish time-interleaved A/D conversion at 40 GSPS, the analog sinusoidal input $f_A(t)$ was first optically sampled by a stream of λ–coded pulses. For f_s = 40 GSPS, these λ-coded pulses were separated by only 25 psec from each other. Figure 5.2 shows a schematic of our WDM-based time-interleaved A/D conversion system. As illustrated, we generated the 40 GHz λ–coded pulse train by "carving" the optical spectrum of a supercontinuum derived from the output of a pulse compressor. In particular, this spectral slicing was accomplished via the use of a silica waveguide optical circuit consisting of an array-waveguide grating (AWG) multiplexer, waveguide delay-lines, and an AWG demultiplexer. We sent the 40 GHz pulse stream to a $LiNbO_3$ electro-optic modulator to sample the analog input. After the analog input was impressed on the 40 GHz pulse stream, the λ–coded pulses were

demultiplexed (in wavelength) to feed four parallel ADC channels. As discussed in the last Section, each of these four parallel electronic quantizers needs to operate at only a quarter of the aggregate sample rate f_s of 40 GHz, i.e. at 10 GSPS. Using software, we then re-combined the discrete outputs $[S_m(t)]$ from the four parallel quantizers to one data-sequence [S(t)]. Finally, we performed an analysis of our WDM-based time-interleaved A/D conversion by computing a power-FFT for S(t). We estimated the resolution of our time-interleaved A/D conversion system by calculating the number of SFDR-bits obtained in the FFT-spectrum of S(t).

5.B.1 Generation of 40 GHz Wavelength-Coded Pulses for Photonic Sampling and their Demultiplexing for Time-Interleaved A/D conversion

In this Section, we describe the details for generating the 40 GHz λ–coded pulse train from our ML fiber laser. We present, in addition, measurements of their phase noise, from which we derived their timing-jitter σ_{Jt}.

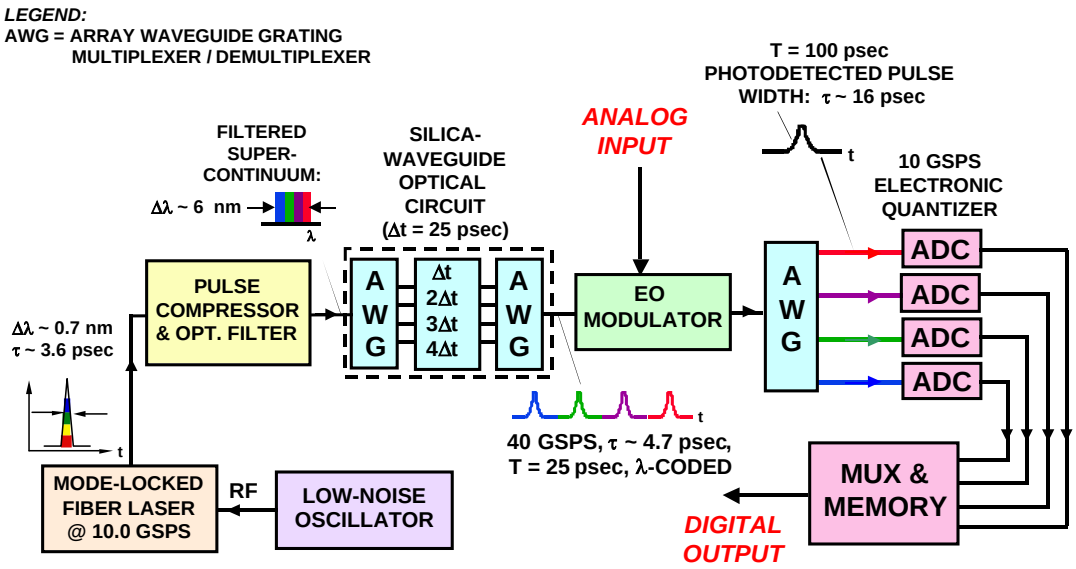


Fig. 5.2 Schematic of 40 GSPS WDM Time-Interleaved ADC system, showing the generation of 40 GHz wavelength-coded pulses for photonic sampling, and its demultiplexing into four parallel ADC channels, each clocked at 10 GSPS.

As illustrated in Fig.5.2, we first fed the 10 GHz ML pulse train to a pulse compressor that consisted of an Er-fiber amplifier and a length of dispersion-decreasing fiber. Via the occurrence of nonlinear effects in the pulse compressor, a supercontinuum (see Fig.5.3a) that demonstrated a spectral span with uniform amplitude (< 0.64 dB variation over $\Delta\lambda = 6$ nm) was generated. A high resolution scan (Fig.5.3b) of a 2 nm segment (bounded by the markers in Fig.5.3a) of this uniform spectral span (USS) shows optical modes that were separated precisely by the mode-locking frequency of 10 GHz.

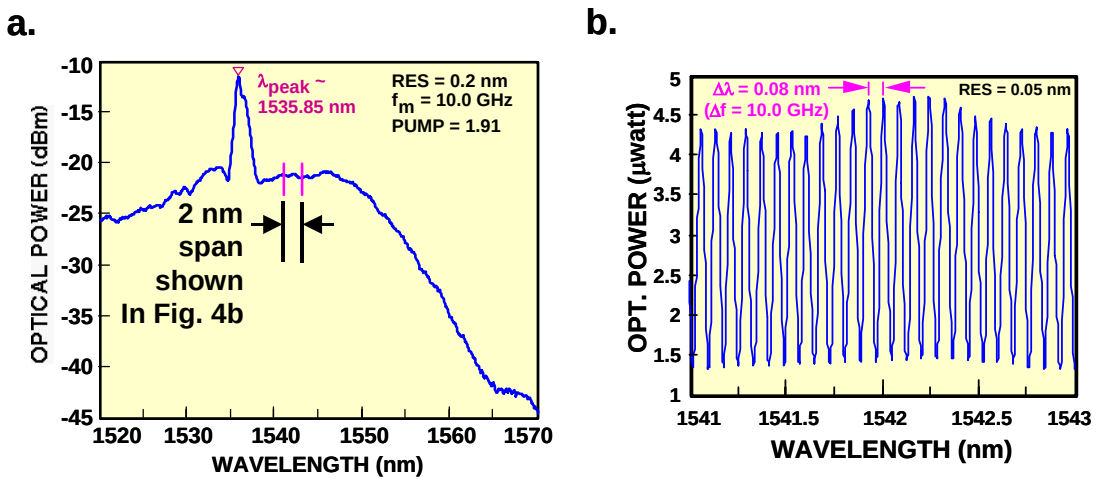


Fig. 5.3 a. Supercontimuum spectrum generated by ML laser and Pulse Compressor b. High resolution scan of spectral region marked in Fig. 3a.

Fig.5.4 shows the single sideband phase noise [L(f)] measured for a $\Delta\lambda \sim 10$ nm span that we filtered from the supercontinuum. In particular, this 10 nm span excluded the pump-spike (at $\lambda =$ 1538.85 nm) due to the ML laser, and was centered at the USS of the supercontinuum spectrum (see Fig.5.3a). All the phase noise plots shown in Figure 5.4 were measured with our Aeroflex PN9000 phase noise test set.

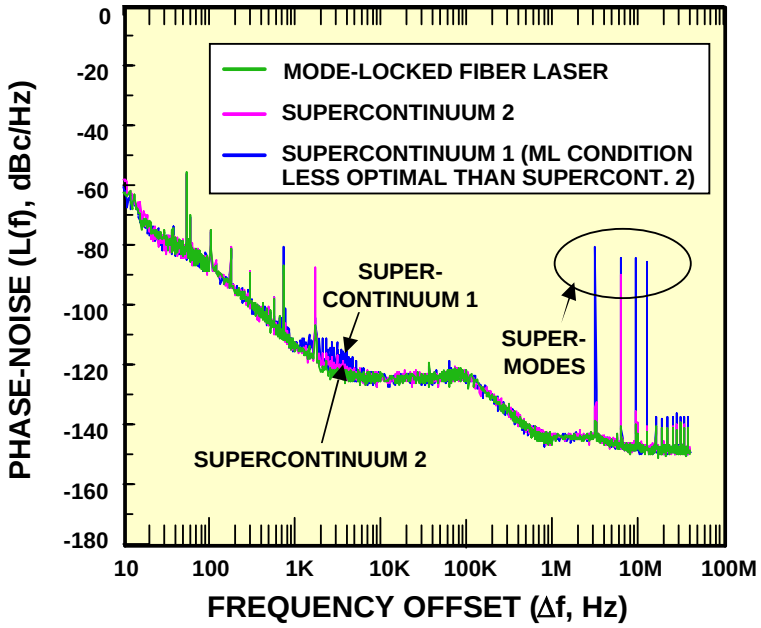


Fig. 5.4 Single sideband phase noise L(f) measured for a 10 nm span of the supercontinuum generated by the pulse compressor.

As shown in Fig.5.4, we observed supermodes with much higher amplitudes than the original ML pulse train. In the L(f) plot, we show two cases measured for the supercontinuum phase noise. The green-colored curve was the phase noise of the ML pulse train, taken at the input to the pulse compressor. The purplish-colored curve (marked Supercontinuum 2) represents the best case we observed for the supercontinuum pulses. In particular, it demonstrated only one large supermode spike. Integrating over the offset frequency range of Δf = 100 Hz - 40 MHz, we found that the timing jitter σ_{Jt} for Supercontinuum 2 was ~29 fsec higher than that of the ML laser. The blue curve (marked Supercontinuum 1) represents a more typical case where we observed several supermode spikes. The integrated timing jitter σ_{Jt} for Supercontinuum 1, integrated over the same offset frequency range, was 109 fsec. Note, however, that even with the 4 supermodes, one can still obtain a timing jitter of 131 fsec (~ 5.9 bits) over a bandwidth of 5 GHz. Table 5.1 summarizes the results of our timing-jitter estimations and bits of resolution N supported for a sampling rate of 40 GSPS.

Table 5.1 Estimated Jt and Bits of Resolution N (for 40 GSPS) derived from L(f) Measurements

40 GSPS	Δf = 100 Hz – 40 MHz	Δf = 100 Hz – 5 GHz*
ML Laser	14.9 fsec (9.1 bits)	~ 69 fsec (6.85 bits)
Supercontinuum 2	44 fsec (7.5 bits)	~ 82 fsec (6.6 bits)
Supercontinuum 1	109 fsec (6.2 bits)	~ 131 fsec (5.9 bits)

* Taking into account of supermodes spaced 3.23 MHz apart

In addition, by characterizing the low frequency pedestal of the supercontinuum pulse train, we measured a fractional timing jitter σ_A of 0.375 – 0.8 %. Using the relationship Q = -log(σ_A)/log2 that relates the bits of resolution Q to σ_A, we estimated that the above σ_A will support a photonic sampling accuracy of ~ 6.97 - 8 bits. Therefore, for Supercontinuum 1, the timing-jitter σ_{Jt} would limit the bits of resolution supported by the photonic sampling to Q ~ 6.2 bits for a Δf of 100 Hz – 40 MHz, and Q ~ 5.9 bits for a Δf of 100 Hz – 5 GHz.

In our WDM-based time-interleaved photonic ADC system, we first filtered out the pump spike, as in the phase-noise measurements described above. We then sent a ~10 nm wide USS of the supercontinuum to a silica-waveguide optical circuit that consisted of an AWG demultiplexer, waveguide delay-lines, and an AWG multiplexer (see Figure 5.2). The channel separation of the two flat-top AWG's in the silica-waveguide circuit was 200 GHz ($\Delta\lambda$ ~1.6 nm), and the widths of their (–1 dB) passbands were ~ 0.8 nm. Specifically, the center-wavelengths of the AWG channels were aligned precisely to the International Telecommunications (ITU) grid at preset temperatures: λ_1 = 1540.557 nm (194.6 THz), λ_2 = 1542.142 nm (194.4 THz), λ_3 = 1543.730 nm (194.2 THz) and λ_4 = 1545.332 nm (194.0 THz). Inside the silica-waveguide

module, the AWG demultiplexer first carved four pulses - with center-wavelengths corresponding to the above λ_i, i = 1, 2, 3, 4 - from the USS of the filtered supercontinuum. The FWHM of the pulses formed by the AWG slicing was ~ 4.71 psec, as measured by an optical autocorrelator (see Figure 5.5a). These four pulses were next separated in time, via the use of silica waveguide delay-lines designed to provide delay-increments of Δt, $2\Delta t$, $3\Delta t$ and $4\Delta t$, where Δt = 25 psec. Using the AWG multiplexer (in the same silica-waveguide circuit), we finally combined the time-delayed pulses (see Figure 5.5b) onto a single output fiber. A fast Fourier transform (FFT) of the multiplexed λ–coded pulses showed a dominant Fourier component, as expected, at f = 40 GHz. However, a 10 GHz spur that was ~ 11 dB below the 40 GHz signal was also observed. We attribute the occurrence of this 10 GHz spur to the slightly nonuniform insertion losses observed for the different λ–channels of the cascaded AWG's. Since these nonuniformities were static, one could calibrate them out via the use of software in a time-interleaved A/D conversion system.

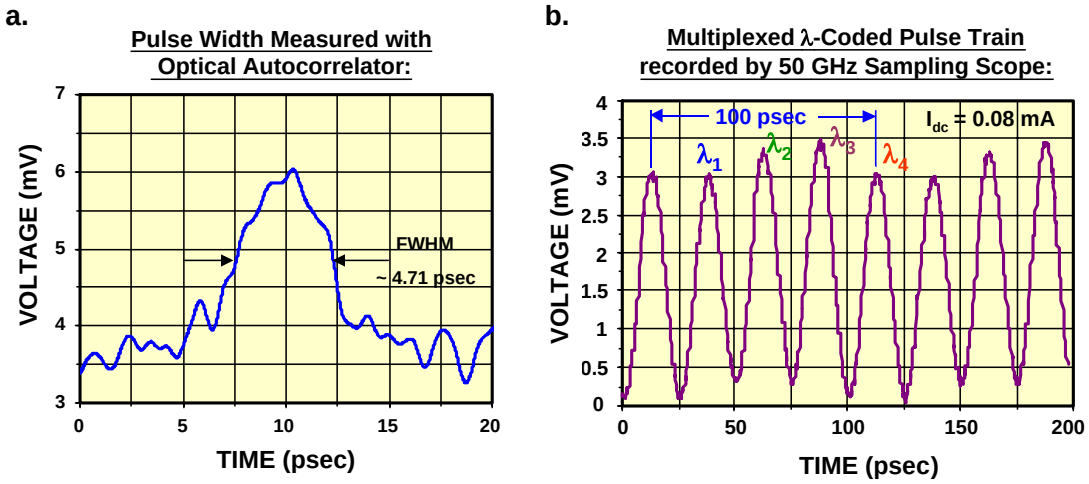


Fig. 5.5 Time-Domain Response of Pulses derived from Silica-Waveguide Circuit: a. Autocorrelation trace of pulse b. 40 GHz λ–coded pulse-stream observed with sampling scope.

Next, we fed the multiplexed pulse train to an EO modulator (see Fig.5.2). At the EO modulator, the analog input $f_A(t)$ to the photonic ADC system was modulated onto the 40 GHz picosecond pulse train. As discussed earlier, to accomplish time-interleaved A/D conversion with quantizers that operate at only 10 GSPS, we need to demultiplex the 40 GHz pulses to form four 10 GHz pulse trains. In our WDM time-interleave scheme, this was accomplished by taking advantage of the fact that the pulses were all wavelength-coded. Here, we used a third AWG (with channels aligned along the same ITU-wavelengths) for the demultiplexing. Figure 5.6 shows the 10 GHz pulse trains, as detected by four high speed photodetectors connected to the output end of this 1:4 AWG demultiplexer. We recorded the 10 GHz demultiplexed optical outputs via the use of parallel channels available in a 50 GHz sampling scope (Tektronix CSA 8000B). As the data shows, this last AWG successfully demultiplexed the wavelength-coded pulses to 10 GHz pulse streams that were displaced by precisely 25 psec from each other.

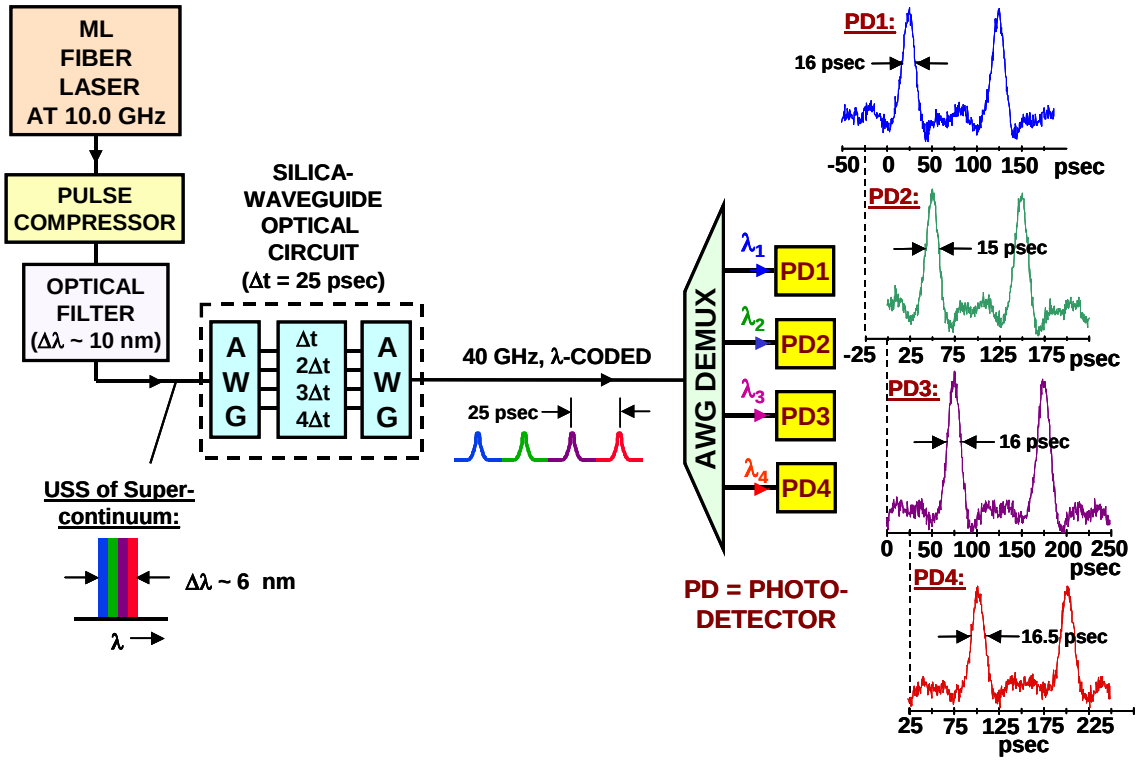


Fig. 5.6 Experimental setup with inset showing the signal-outputs of four photodetectors connected to the 1:4 AWG. The AWG demultiplexed the 40 GHz wavelength-coded pulses to 10 GHz pulse streams.

5.B.2 Results from 40 GSPS Photonic Time-Interleave Experiments

In this Section, we present our results from the 40 GSPS photonic time-interleave experiments. We will show data obtained for different input frequencies f_{in} of the analog input $f_A(t)$. These data include: (i) the power-FFT spectrum observed from one time-interleaved channel, (ii) the discrete channel-multiplexed data for S(t) in the time-domain, and (iii) the power-FFT computed for S(t), from which we can determine the number of SFDR-bits obtained in the experiment. Figure 5.7 shows a more detailed schematic of our experiment. As illustrated, we used a polarization maintaining (PM) Er-amplifier to boost the optical power of the λ–coded pulses before they were sent to the $LiNbO_3$ electro-optic modulator to accomplish photonic sampling. We used four 10 GSPS parallel channels available within a high speed digitizer as our electronic quantizers. Since these four digitizer-channels were designed to have a common trigger, we brought (re-aligned) the demultiplexed pulses to the same point in time at the input to these four quantizer channels. This was accomplished with precisely trimmed fiber delay-lines that provided stepped time-delays of 4Δt, 3Δt, 2Δt and Δt, where Δt was again 25 psec. As mentioned earlier, the discrete outputs ($S_m(t)$) of the four parallel channels from the digitizer was multiplexed again (by software) to form a combined output S(t). Below, we present data for the input frequencies f_{in} of 1.2 GHz, 3.2 GHz and 17 GHz. The first two input

frequencies were below the Nyquist frequency of 5 GHz for each individual channel. However, the input frequency of 17 GHz for $f_A(t)$ was higher than each channel's Nyquist frequency of 5 GHz, but lied below the Nyquist frequency of 20 GHz for the aggregate sampling rate of 40 GSPS (for the four interleaved channels).

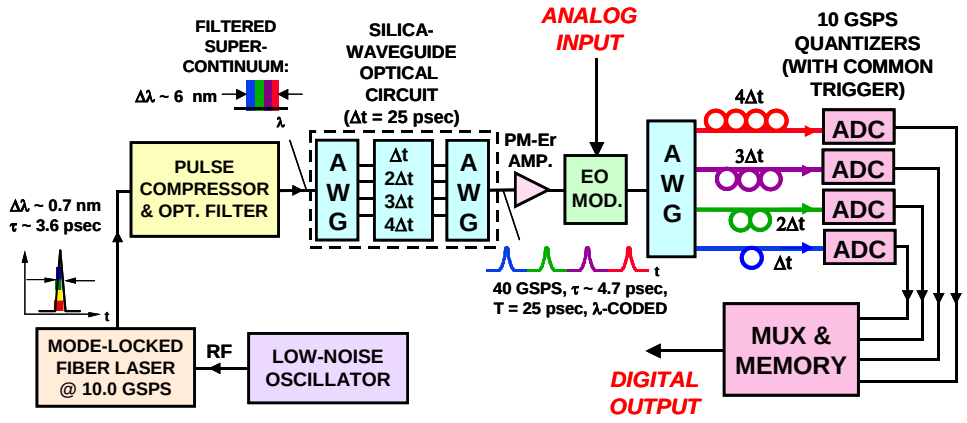


Fig. 5.7 Detailed schematic of 40 GSPS WDM-based photonic time-interleaved experiment with four parallel channels.

Figure 5.8 shows the FFT spectrum and multiplexed time-domain data for an analog input frequency of f_{in} = 1.2 GHz.

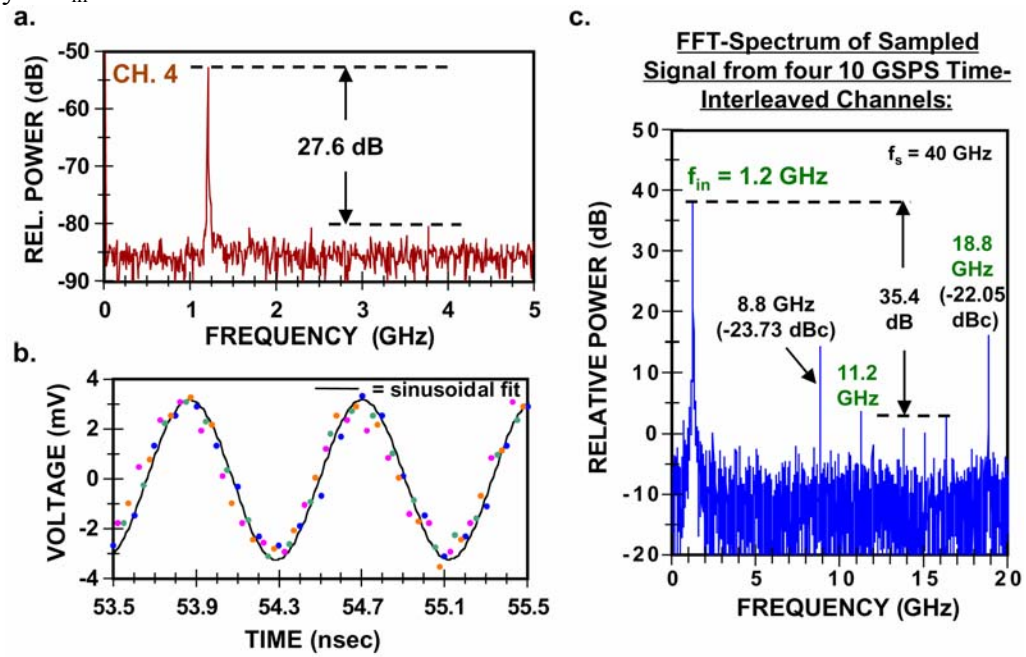


Fig. 5.8 FFT Spectrum and multiplexed time-domain data for an analog input frequency of f_{in} = 1.2 GHz to the photonic time-interleaved ADC system: a. FFT spectrum of Ch. 4, b. Multiplexed time-domain data from S(t), and c. 4000 point FFT spectrum of S(t), photonic ADC output.

Fig.5.8a shows the FFT spectrum derived (from 1000 sampled data points of $S_m(t)$) for one channel (Ch. 4) of the four parallel electronic quantizers. Fig.5.8b shows the time-domain data for S(t) where digital data from the four parallel channels were multiplexed to form one sequence. In addition, we show a sinusoidal fit (f = 1.2 GHz) through the data points. Fig.5.8c shows the FFT spectrum of the 4000 sampled points (T_s = 25 psec) multiplexed to form S(t). As shown, we observed the occurrence of time-interleaved spurs at: 8.8 GHz (= $f_s/4 - f_{in}$), 11.2 GHz (= $f_s/4 + f_{in}$), and 18.8 GHz (= $f_s/2 - f_{in}$), all of which lied below the Nyquist frequency of 20 GHz for f_s = 40 GHz. Although the highest spur that was non-interleave in origin occurred at a power level -35.4 dBc, the alias-spur at 18.8 GHz limited our spur free dynamic range (SFDR) to 22.05 dB, which corresponded to ~3.7 SFDR-bits.

Next, Figure 5.9 shows the FFT spectrum and multiplexed time-domain data for an analog input frequency of f_{in} = 3.2 GHz. Fig.5.9.a shows the FFT spectrum derived from Ch. 3 (using from 1000 sampled data points of $S_2(t)$), one of the four parallel electronic quantizers. Fig.5.9.b shows the time-domain data for S(t), where digital data from the four parallel channels were multiplexed to form one sequence. We also show a sinusoidal fit (f = 3.2 GHz) through the data points. Fig.5.9.c shows the FFT spectrum of the 4000 sampled points (T_s = 25 psec) multiplexed to form S(t). As shown, we observed the occurrence of time-interleaved spurs at: 6.8 GHz (= $f_s/4 - f_{in}$), and 16.8 GHz (= $f_s/2 - f_{in}$), both of which lied below the Nyquist frequency of 20 GHz for f_s = 40 GHz. The highest time-interleave spur at 16.8 GHz limited our SFDR to 22.62 dB, which corresponded to ~3.76 SFDR-bits.

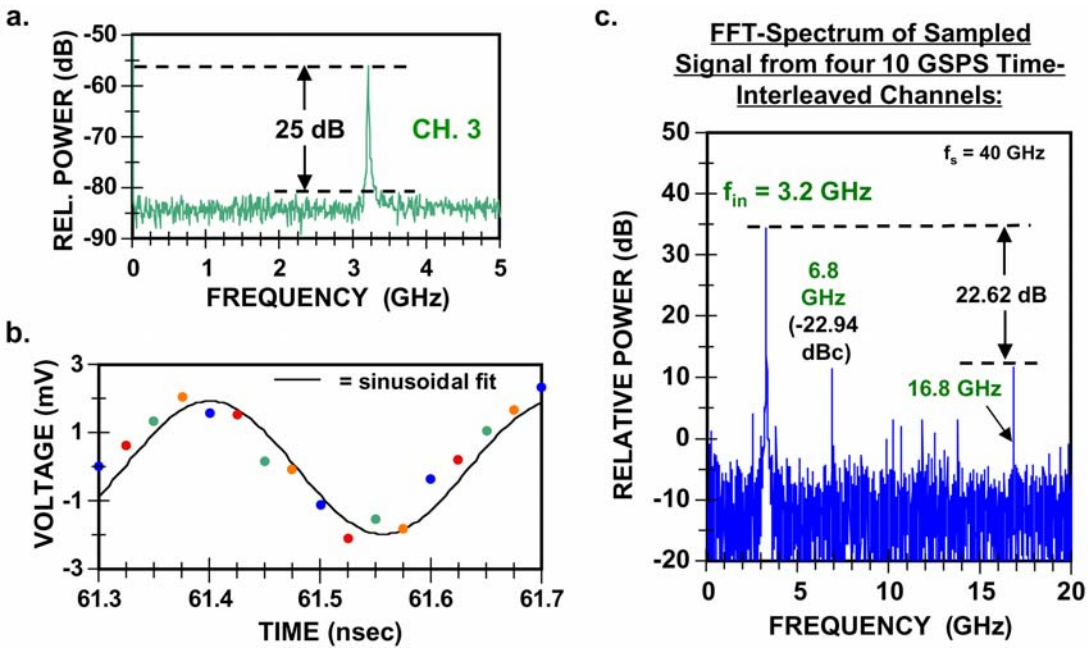


Fig. 5.9 FFT Spectrum and multiplexed time-domain data for an analog input frequency of f_{in} = 3.2 GHz to the photonic time-interleaved ADC system: a. FFT spectrum of Ch. 3, b. Multiplexed time-domain data from S(t), and c. 4000 point FFT spectrum of S(t), photonic ADC output.

Finally, Figure 5.10 shows the FFT spectrum and multiplexed time-domain data for an analog input frequency of f_{in} = 17 GHz. Our photonic ADC system's capability to sample this

high frequency signal demonstrated the enhancement of A/D conversion capability offered by our WDM time-interleaved architecture. Fig.5.10a shows the FFT spectrum derived from Ch. 3 (using 1000 sampled data points of $S_2(t)$), one of the four time-interleaved electronic quantizers. In particular, we notice that the spectrum shows an alias at 3 GHz [= (2 x 10) – 17 GHz], that stemmed from the 10 GHz subsampling (by Ch. 3) of the 17 GHz input signal fed to the EO modulator. Another alias at 7 GHz (= 17 – 10 GHz) that completed the symmetry about the Nyquist frequency of 5 GHz (for the 10 GHz subsampling) was not shown in this plot. Fig.5.10.b shows the time-domain data for S(t) where digital data from the four parallel channels were multiplexed to form one sequence. The two sinusoidal curves (with f = 17 GHz) fitted through the data points for two of the four channels show the complementary phase derived from the timing offset that we mentioned in Section 5.A. Fig.5.10c shows the FFT spectrum of the 4000 sampled points (T_s = 25 psec) multiplexed to form S(t). As shown, we observed the occurrence of time-interleaved spurs at alias frequencies that corresponded to the 10 GHz subsampling: at 3 GHz (= $f_s/2 - f_{in}$), and 7 GHz (= $f_{in} - f_s/4$), as well as at 13 GHz (= $3f_s/4 - f_{in}$), all of which lied below the Nyquist frequency of 20 GHz (for f_s = 40 GHz). The highest time-interleave spur at 3 GHz limited our SFDR to 20.4 dB, which corresponded to ~ 3.4 SFDR-bits.

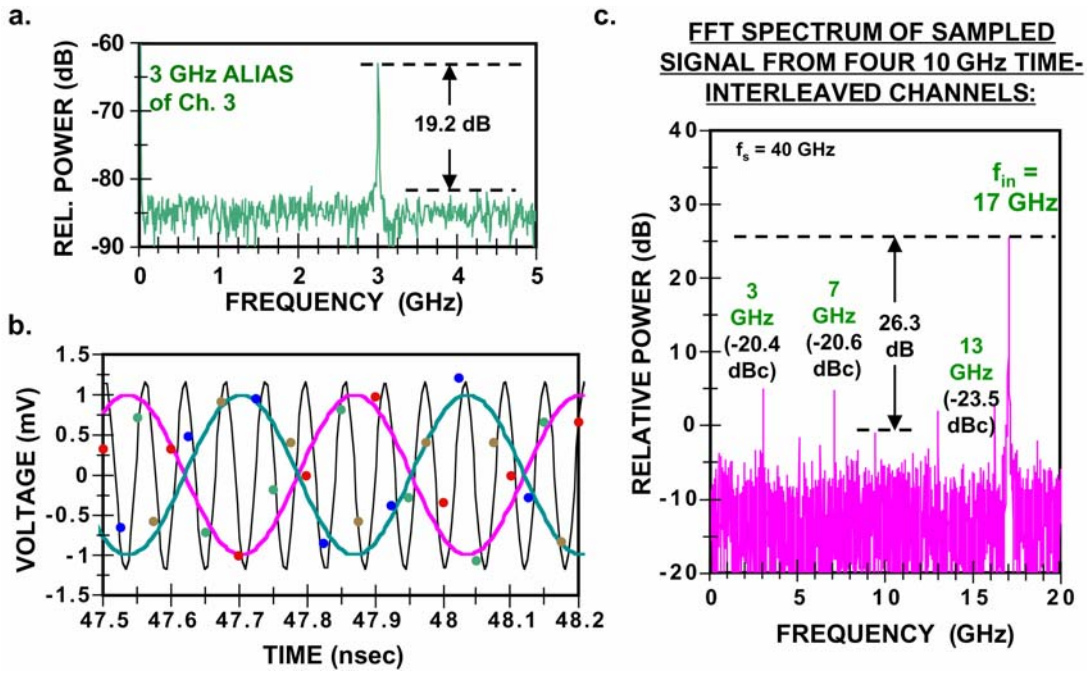


Fig. 5.10 FFT Spectrum and multiplexed time-domain data for an analog input frequency of f_{in} = 17 GHz to the photonic time-interleaved ADC system: a. FFT spectrum of Ch. 3, b. Multiplexed time-domain data from S(t), and c. 4000 point FFT spectrum of S(t), photonic ADC output.

Figure 5.11 shows a plot of the spur free dynamic range and the bits of resolution, calculated according to the equation, SFDR-bits = SFDR (in dBc)/6.02, for our 40 GHz photonic time-interleave experiments.

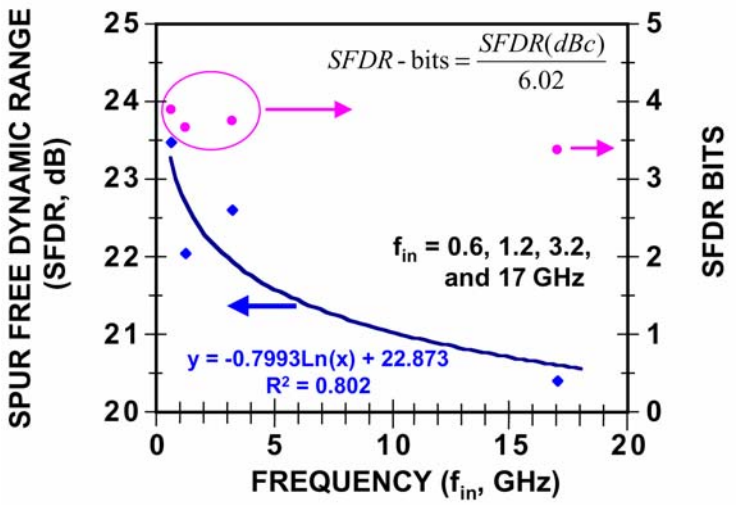


Fig. 5.11 Measured spur free dynamic range (SFDR) for 40 GSPS photonic time-interleave system and estimated SFDR-bits.

As shown, we achieved close to 4 SFDR-bits for analog input frequencies f_{in} that were less than 5 GHz, and ~ 3.4 SFDR-bits for f_{in} = 17 GHz. In summary, we demonstrated the viability of applying spectral-slicing and WDM technologies to photonic A/D conversion at sampling frequencies as high as 40 GHz. The bits of resolution that one can achieve using the approach described in this Section can be improved by performing better channel-matching and calibration for the optoelectronic time-interleaved channels. Along with other published reports on photonic ADCs[28]-[29], our photonic time-interleaved sampling experiments constituted some of the highest sampling rates ever demonstrated in A/D conversion technologies.

SECTION 6

OPTICAL CLOCK DISTRIBUTION AND InP-HBT FLASH QUANTIZER DEVELOPMENT

In Section 6.A, we first describe our experiment on the optical distribution of clock signals to remoted InP-HBT OEIC quantizers of the flash architecture. Section 6.A.1 presents experimental data obtained for the pulse and frequency response of InGaAs/InP photodiodes that were integrated on-chip the flash OEICs. In particular, these on-chip photodiodes were fabricated from the base-collector junctions of InP-HBTs. The performance of 3-bit flash quantizers that were optically clocked will then be described (Section 6.A.2). In the second part of this Section (Section 6.B), we will summarize the electrical performance of a re-designed 4-bit flash quantizer that utilizes a novel distributed ladder structure to create the quantization reference voltages. Based on signal-to-noise ratio (SNR) and distortion measurements of this electrical flash ADC, we estimated an effective number of bits (ENOB) of ~ 3.9 bits at 10 GSPS, for an analog input frequency of 4.9 GHz.

6.A Optical Distribution of Clock Signals to InP-HBT Flash Quantizers

6.A.1 Characterizations of Integrated Photodetectors

Figure 6.1.a shows a photograph of the flash OEIC quantizer[2] that was used in our optical clock distribution demonstration.

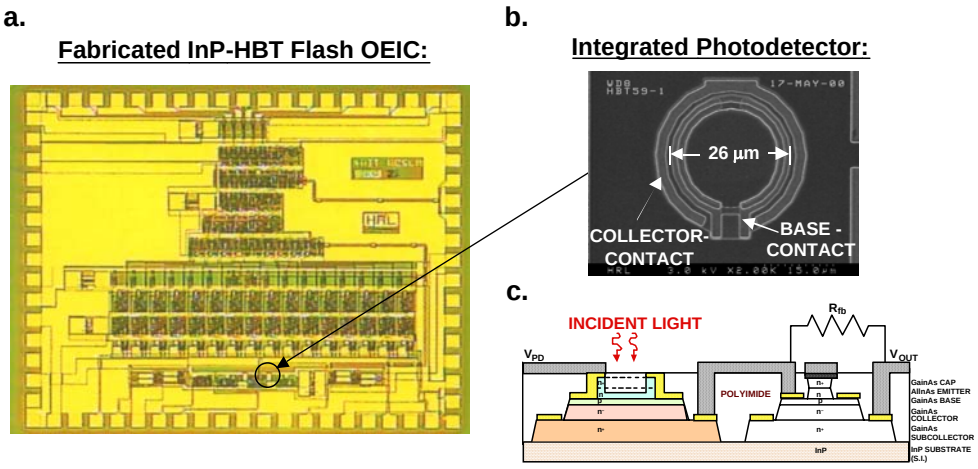


Fig. 6.1 a. Fabricated InP-HBT Flash OEIC with integrated photodetector (PD) b. SEM micrograph of integrated PD c. Epitaxial structure for integrated PD.

The SEM micrograph and epitaxial structure of the integrated photodetectors (PD) on the OEIC are shown, respectively, in Fig. 6.1b and Fig. 6.1c. As shown, they were fabricated from the base-collector junction of an InP-HBT, making their incorporation in the flash ADC compatible

with the fabrication for the rest of the InP-HBT electronic circuit. The active region of the integrated PD was ~26 μm in diameter.

Figure 6.2b shows the pulse response for these integrated PDs, when they were excited by ~3 psec wide mode-locked (ML) optical pulses. The experimental setup for the pulse response measurement was illustrated in Fig.6.2a.

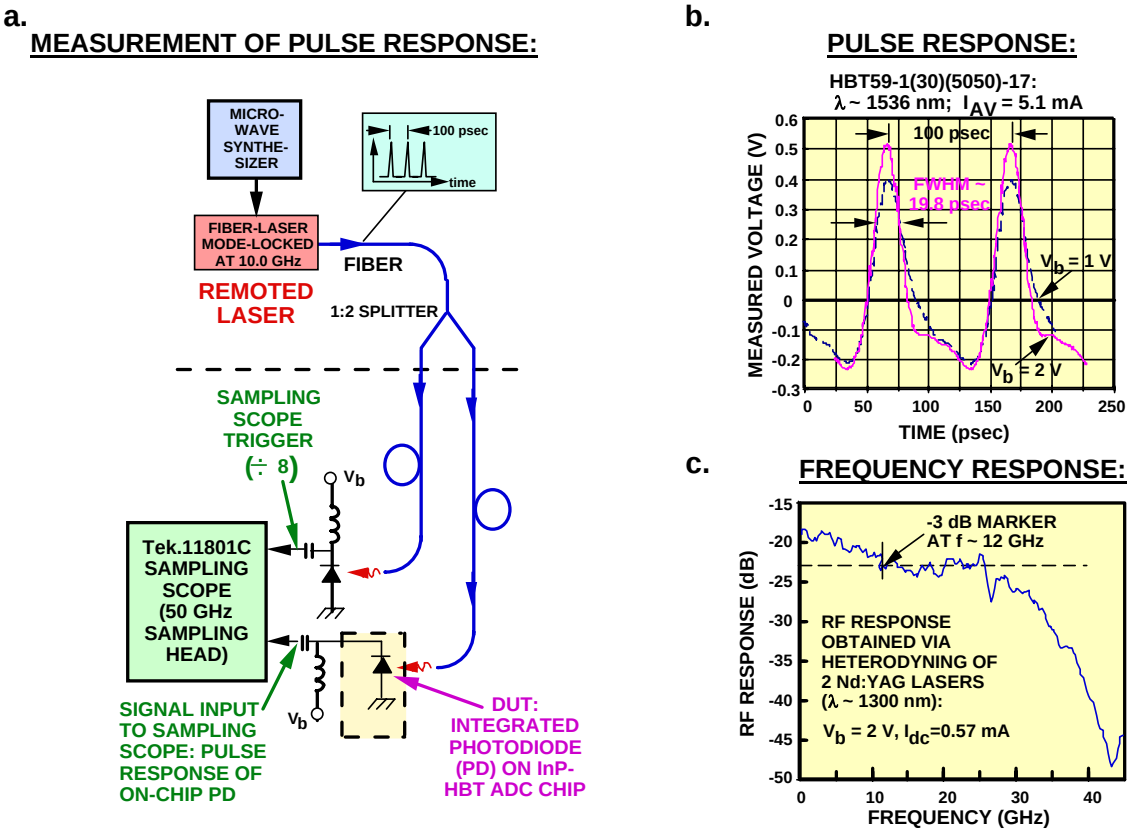


Fig. 6.2 a. Experimental setup for characterizing the pulse response of PDs integrated on InP-HBT OEICs b. Measured pulse response at bias voltages V_b of 1 V and 2 V. c. RF response of the same PD measured by the optical heterodyning of two λ = 1300 nm Nd:YAG lasers.

As illustrated, the high speed sampling scope (Tektronix 11801C) was triggered optically by 10 GHz pulses derived from the same ML laser (see Section 2). We measured a full width half maximum (FWHM) of ~19.8 psec for a voltage bias V_b of ~ 2 V. This recorded FWHM was in good agreement with the -3 dB bandwidth of ~ 12 GHz for the frequency response shown in Fig.6.2c, after we took into account the bandwidth of the bias-TEE and the sampling scope. Fig.6.2b also shows that the pulse response broadened slightly (with a tail-response) at a V_b of ~ 1 V. These data indicated that the PD should be biased at voltages above a volt in our optical clock distribution or photonic A/D conversion experiments. Finally, Fig.6.3 shows the frequency response of an integrated PD measured (via optical heterodyning) at DC photocurrent (I_{dc}) levels of 1 mA, 10 mA and 20 mA. As shown in our plots, the PD maintained a –3 dB bandwidth of 11.5 GHz, even for an I_{dc} as high as 20 mA.

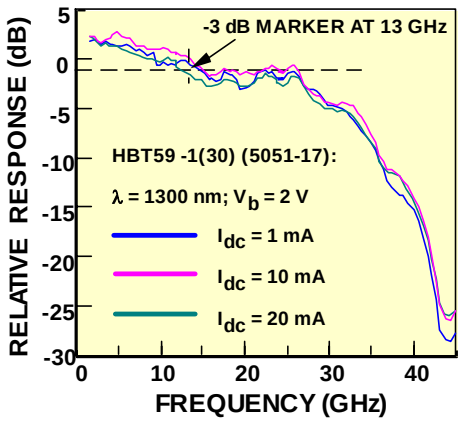


Fig. 6.3 Measured frequency response for integrated PD at DC photocurrents of 1 mA, 10 mA and 20 mA.

6.A.2 Optically Clocked Flash OEIC Quantizers

In this Section, we summarize the results obtained for the optically clocked 3-bit flash quantizers. The flash OEIC consisted of an optical receiver front-end, followed by a comparator bank, and then a thermometer-to-binary converter. The circuit consisted of ~960 transistors, operated with 4 V supplies and dissipated 4.25 W of power. The flash OEIC was optically clocked by either pulses from the ML laser, or an RF-photonic link (see Fig. 1.3) that we synchronized with the ML laser. We show, in Fig.6.4, the A/D conversion output of a flash OEIC that we clocked optically at 5 GHz, for an analog electrical-input at the frequency f_{in} of 1.010 GHz. After A/D conversion, the 1.010 GHz output was subsampled again at 1 GHz to form a 10 MHz alias, whose data was subsequently analyzed via the computation of an FFT. The reconstructed ADC output of Figure 6.4a shows clearly the 8 quantized levels derived from the 3-bit flash ADC. Fig. 6.4b shows the 500-point FFT of our flash A/D conversion output. As shown in the plot, we obtained a SNR of 18 dB, which corresponded to an ENOB of 2.7 bits.

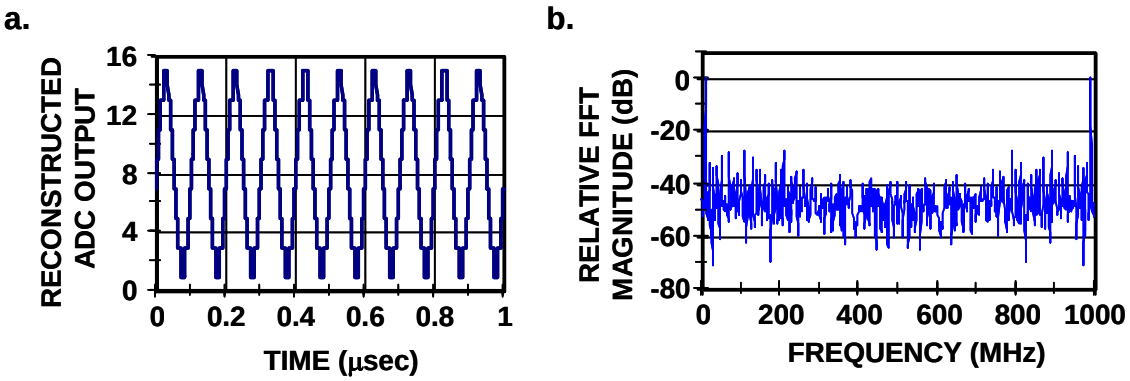


Fig. 6.4 Performance of optically clocked 3-bit flash ADC: a. Reconstructed time-domain output of flash ADC b. 500 point FFT of A/D conversion output, subsampled at 1 GHz, for an analog input at 1.010 GHz.

Figure 6.5a shows a plot of the measured effective number of bits (ENOB) and SFDR-bits for the 3-bit flash quantizer vs the frequency f_{in} of its analog-input, for a sampling (clock) rate of 10 GSPS. Here, ENOB was obtained from the SNR (in dB) with the use of the equation: ENOB = (SNR - 1.76)/6.02, while the number of SFDR-bits was obtained from the equation: SFDR(in dB)/6.02 (see Ref.1). In addition, f_{in} = (n x 1 GHz) + 1 MHz, where n is an integer. The data were obtained by electrical or optical clocking. As illustrated, we obtained 2.8 ENOB at low input frequencies. At frequencies that were close to the Nyquist frequency of 5 GHz, we still maintained an ENOB of 2.4 bits. Fig. 6.5b plots the measured ENOB and SFDR-bits vs the clock rate for the 3-bit flash ADC. The data showed that we obtained an ENOB of ~1.7 bits at clock frequencies as high as 18 GHz.

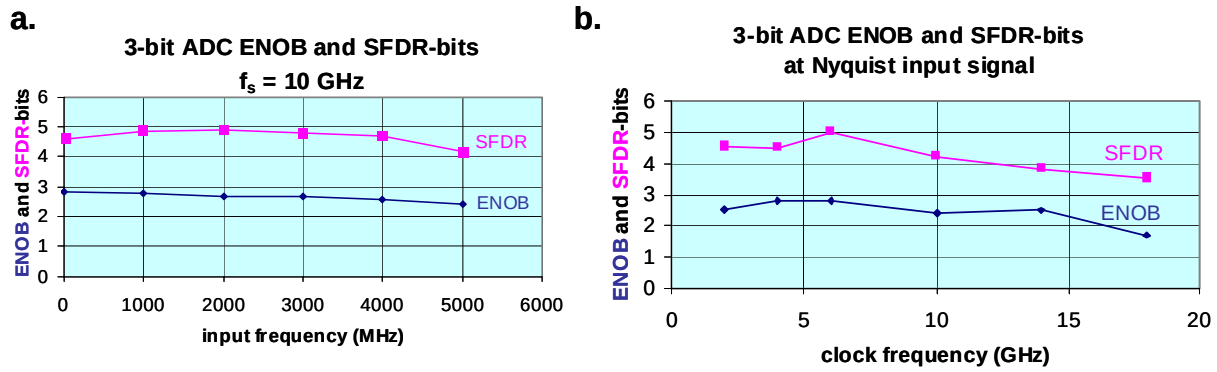


Fig. 6.5 Performance of 3-bit InP-HBT flash ADC: a. Bits of resolution vs analog input-frequency f_{in} b. Bits of resolution vs clock frequency (f_s) of flash ADC.

6.B Electrical Performance of 4-bit InP-HBT Flash Quantizer with Distributed Resistor Ladder Architecture

To improve the performance of the 4-bit flash quantizer designed in the early part of the Program, we revised in a second iteration, its comparator design - to one using a distributed resistor ladder architecture – as well as the circuit's mask-layout. In particular, the layout improvement included a reduction in the maximum Δ-path - from 1050 μm to 115 μm – for the interconnect from the analog-input to the circuit's comparator cells. In this Section, we describe the electrical performance of this revised 4-bit flash InP-HBT quantizer[30]. With the new circuit-design and layout, we demonstrated an ENOB of ~3.9 bits at 10 GSPS (for the full Nyquist bandwidth). The 4-bit flash was fabricated using HRL's InP-HBT G-2 technologies. In addition to the active devices (InP-HBTs), the technology offers 50 ohm/sq TaN resistors, 0.3 fF/mm^2 MIM capacitors and 3 layers of interconnect on 3" semi-insulating (SI) InP-Wafers. The architecture and topologies were formed based on the results of pre-analysis, the technology capabilities, and available measurement equipment. We show, in Figure 6.6, the overall structure of the ADC. The analog input feeds, directly, the comparator cell array. After a glitch improvement algorithm, the thermometer code is converted to pulse-form. The pulses drive a ROM cell, which produces the binary representation of the analog input. The binary code is then retimed, and fed into 50-ohm/output driver-buffers. A selector controls the re-timing block. The

selector inputs are provided by sampling-clock and output-enable signals. The output-enable signal is, nominally a steady state signal that could differ from the clock. The converters have been provided with a separate clock input (output-enable) in order to, among others, enable down conversion of the input analog signal (in the digital domain). The down converted signal's frequency is a function of sampling- and output-enable– clock frequencies. This function would not only enable "ADC + down-conversion" functions, but also decreases the outputs' data rate to such speeds that allow use of available Logic Analyzer. Therefore, most commonly a lower repetition rate than the sampling clock is desired. However, the output-enable may be equal to or higher than the sampling-clock. If the sampling-clock and output-enable have the same rate, the outputs have simply been subject to a retiming, and the output-rate is the same as the sample-rate.

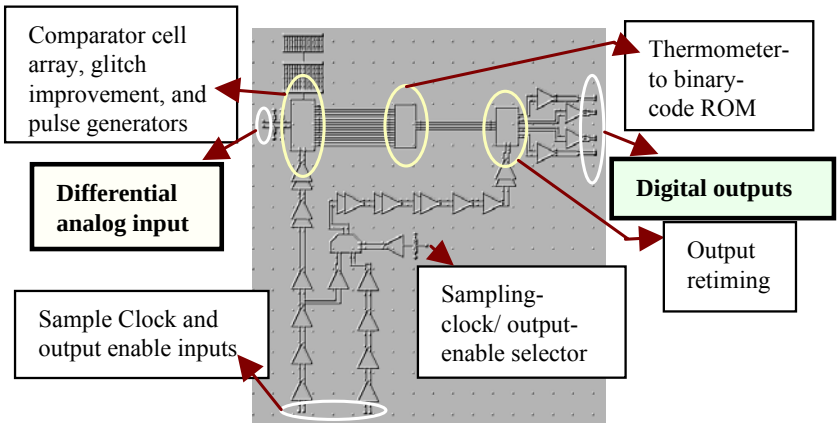


Fig. 6.6 Overall structure of 4-bit InP-HBT flash ADC.

If the output-enable has a higher repetition rate than the sampling-clock, the outputs would be providing a different position of the digital output transitions. Amplifier/buffer chains are used to create correct synchronization between various blocks and I/Os, under all modes of operation. All the transistor level implementations in the digital parts are based on ECL and CML topologies. All the analog parts are utilized using balanced structures.

Figure 6.7.a presents the block level schematics of the comparator cells. In the circuit, a dual differential comparator amplifier senses the analog signal. When the amplitude of the analog signal passes the locally defined threshold voltage at the comparator, the output of the comparator is toggled and amplified by the following amplifier chain and provided to the comparator latch. An "inhibit"-signal is generated at the internal state of the flip-flop and propagated to the two nearest neighbors of each comparator cell. The input interconnects carrying the analog inputs to the comparator cell array were designed to have low path delay variations to different elements of the array. The input capacitive load, due to interconnects, was calculated to be about 50 fF (at full substrate thickness), and the maximum length variation to array elements was: Max Δpath = 115 μm.

a. Comparator cell block diagram: **b. Distributed resistor ladder cell:**

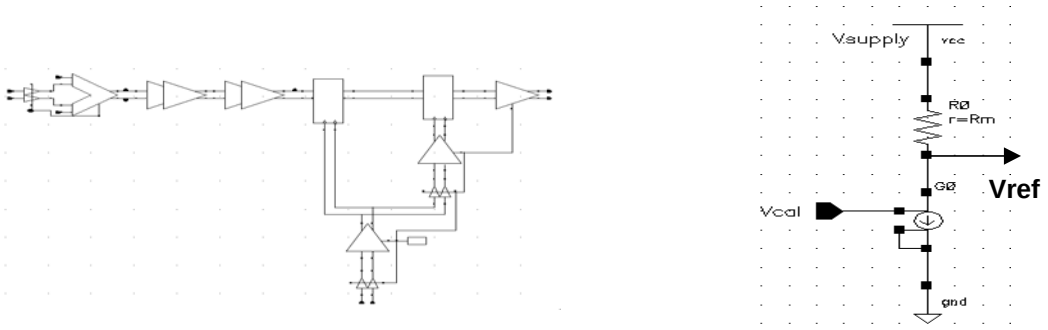


Fig. 6.7 a. Block diagram of comparator cell in InP-HBT flash ADC b. Distributed resistor ladder cell.

Next, we discuss the design of the distributed resistor ladder. The distortion caused by resistor ladders and the inevitable crossing of the interconnects carrying the reference voltages and the analog input, in any realistic and practical physical realization, causes further signal dependent distortion of the input to the comparator cells, degrading dynamic characteristics of the converters, especially wide-band ADCs. A distributed resistor ladder approach was therefore adopted to improve the integrity of reference voltages as well as the input analog signal. The structure incorporates the reference-creating circuit in a distributed manner allowing the reference generator to be inside the comparator cell, thereby never crossing the analog input. A schematic of the reference generator cell may be viewed in Figure 6.7b. The voltage controlled current source "G0" is calibrated by Vcal. Resistor Rm's value is calculated from equation 6.1.

$$Rm = (m+0.5)xV_{FS}/(2^{n}xI_{G0}) \qquad (6.1)$$

The structure may be implemented in a full differential design. This is accomplished by utilizing dual differential comparators to recover some of the performance degradations due to decreased transconductance at the input stage, as a result of variations in the input bias-conditions. The final chip size, including pads, is 3225x 1875 μm^2 and the simulated power consumption of the circuit was 1.6 A x 3.0 V = 4.8 W. The circuit consists of 3864 InP-HBTs and more than more than 2600 thin-film resistors. A part of the power consumption is due to the amplifier chains that were introduced to deal with synchronicity issues on board.

Figure 6.8.a and Fig. 6.8.b shows, respectively, the mask layout and micrograph of a fabricated 4-bit flash ADC. The measurement set-up for the completed flash quantizer-wafers was developed around a probe-station equipped with 4 probe manipulators. All the custom probes were fabricated by GGB-industries. The high frequency I/Os were provided with K-type connectors offering phase and mode consistency, and low attenuation up to about 40 GHz (K-band). During the characterization, we split the generator signal, and phase shifted one branch by 180 degrees to create a differential analog signal source. The output-enable signal was created using a second generator set to 1 GHz. This frequency was selected based on the maximum allowed data-rate by the Logic Analyzer. The 1 GHz signal was divided into two branches. One

branch was fed to the output-enable port of the circuit, through an adjustable phase-shifter, while the other branch was directed to the Logic Analyzer's clock input through a Bias-T. The inverted digital outputs were used to monitor the ADC while powering up and tweaking external delay elements and analog input power. The non-inverting outputs were fed to the Logic Analyzer for storage and further processing.

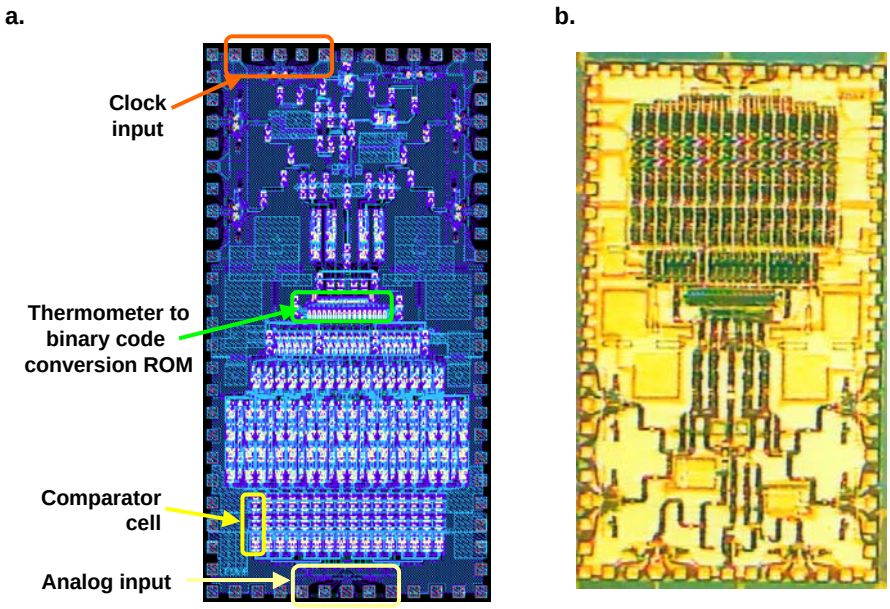


Fig. 6.8 a. Mask layout of 4-bit flash ADC b. Micrograph of fabricated chip.

Through a set of attenuators and power-splitters, a passive DAC was built to recreate a rough estimate of the sampled analog input signal though the digital outputs. This method proved to be useful, as it allowed a real time tracking of the spectrum changes of the analog equivalent of the digital outputs when delays and input power was being optimized (The optimization of the delays was crucial to compensate for the cable and instrumentation delay). However, the variations in delay between chip outputs and DAC inputs could cause an error, which makes the DAC output too inaccurate for a reliable estimate of the real performance. Nevertheless, the method provided valuable as a means of initial evaluation. The sampling oscilloscope was used in a similar manner to study the waveform in the time-domain. The sampling oscilloscope's built-in math functions were used as a "soft"-DAC during the characterization.

The circuits (F4V1) were measured on 6 wafers. All the measured circuits on 4 wafers were fully functional with less than 5% variation on power supply currents. The 1.9A of current consumption resulted in 5.89W of total power dissipation, All the measurement reported here were verified on several circuits and on 4 wafers.

We now present the results of our characterization for the 4-bit flash ADC. The Effective Number of Bits (ENOB) was calculated, based on extraction of Signal to Noise and Distortion Ratio (SNDR) from measured spectrums. We created the frequency spectrums by performing Fast Fourier Transform on 64K packages of data obtained from the 1GHz Logic Analyzer. Figure 6.9a presents the SNDR, Total Harmonic Distortion (THD), and ENOB for analog input

frequencies ranging from 1.8GHz to 4.9GHz for a sampling rate of f_s = 10 GSPS. As shown, we achieved ~3.9 ENOB over the whole Nyquist frequency range of 5 GHz.

Figure 6.9b shows data that reflected the quality of a converted 200 MHz signal, when the sample rate was varied between 1 and 20 GSPS. Note that the differential input signal at 200 MHz did not have an equivalent resolution better than 3.8 bits, at the source, while the signal accuracy was about 3.9 bits, at 4.9 GHz, at the source. The relatively sharp drop in ENOB at sampling frequencies beyond 10 GHz (Figure 6.9b), is believed to be partially due to limited input clock power at the source and degraded internal synchronicity. Note that the designs were primarily optimized for 10 GHz with respect to bandwidth of various parts and internal synchronization.

In summary, we designed and fabricated a 4-bit InP-HBT flash quantizer. Using the HRL OEIC G-2 InP-HBT technology in its fabrication, we demonstrated that the quantizer circuit was compatible with OEIC implementations. The electrical quantizer circuit demonstrated a power dissipation of about 5.9W, and consisted of 3864 HBTs. The circuit occupied a total area of 3225 x 1875 μm^2. We also implemented a novel distributed ladder structure, with dual differential input amplifier, in the quantizer's comparator cells. Finally, we measured an ENOB of ~ 3.9, for a 4.9 GHz analog input-frequency and a sampling-clock rate of 10 GSPS.

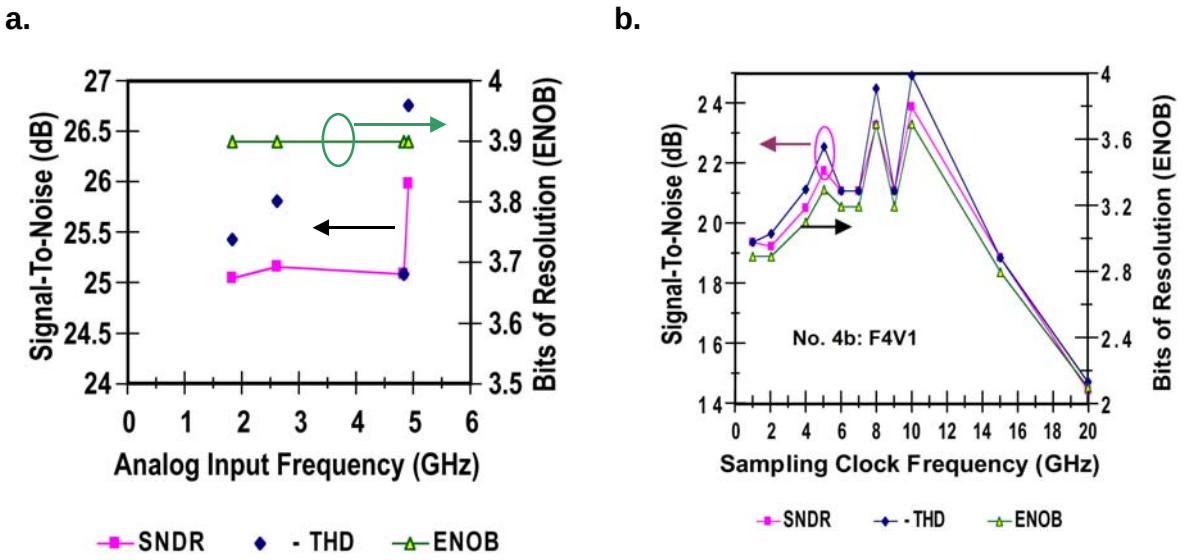


Fig. 6.9 Performance of 4-bit flash electrical quantizer: a. Signal-to-Noise and Distortion Ratio (SNDR), Total Harmonic Distortion (THD) and ENOB vs the Analog Input Frequency f_{in}, at a sampling-clock frequency f_s of 10 GSPS b. SNDR, THD and ENOB obtained for a f_{in} =200 MHz analog input vs the Sampling-Clock Frequency f_s.

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