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BATTLEFIELD ONLINE WITH SUPERCONDUCTIVE SYSTEMS TECHNOLOGY DEMONSTRATION

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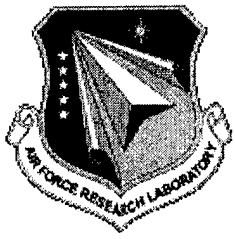
Final Technical Report: April 1999 – December 2003



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TECHNICAL REPORT

Battlefield Online With Superconductive System Technology Demonstration

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14. ABSTRACT
The contract for Battlefield Online with Superconductive Systems build upon the success of previous AFRL contracts to develop components based on superconductive electronics for spread spectrum modems. The prior work had demonstrated a low power chip that operated at 2 GHz and performed spread spectrum functions. This contract developed a Digital Correlator and a rapid Synchronizer and demonstrated that the correlation and synchronization could be performed with superconductive digital electronics.
The Digital Correlator demonstrated correct mixing of 2-bit Data with Code and accumulation of the correlation sum at speeds of to 320 MHz. It correctly accumulated single inputs at rates up to 3 GHz. The synchronizer demonstrated most of its functions at low speed.
Another task supported the design of a Glue Chip for use in a Crossbar data switch. The Glue Chip is part of a multichip module that forms the switch fabric. The Glue Chip was designed to have high sensitivity to weal signals, but changes in the design of the Switch Chip created a stronger signal, so the sensitive Glue Chips were not built.
The high-speed circuits developed under these AFRL contracts have the ability to transform communications.

15. SUBJECT TERMS
digital communications, superconductive electronics, GHz modem, code generator, single flux quantum

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The Glue Chip task was funded by the National Security Agency. Thank you to Dr. Fernand Bedard for guiding that effort.

Executive Summary

The contract for Battlefield Online with Superconductive Systems (BOSS) built upon the success of previous AFRL contracts to develop components based on superconductive electronics for spread spectrum modems. The prior work had demonstrated low power chips that operated at 2 GHz (Figure EX.1) and performed important spread spectrum functions (Figure EX.2). This final contract developed a Digital Correlator and a rapid Synchronizer and demonstrated that the correlation and rapid synchronization could also be performed with superconductive digital electronics.

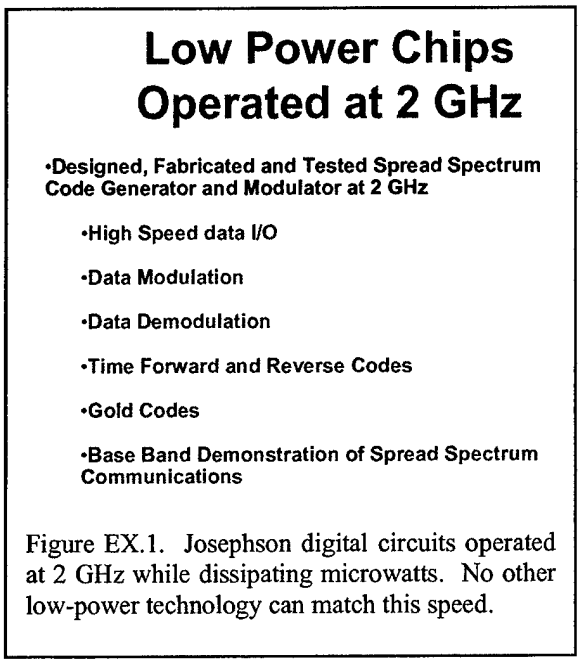


Figure EX.1. Josephson digital circuits operated at 2 GHz while dissipating microwatts. No other low-power technology can match this speed.

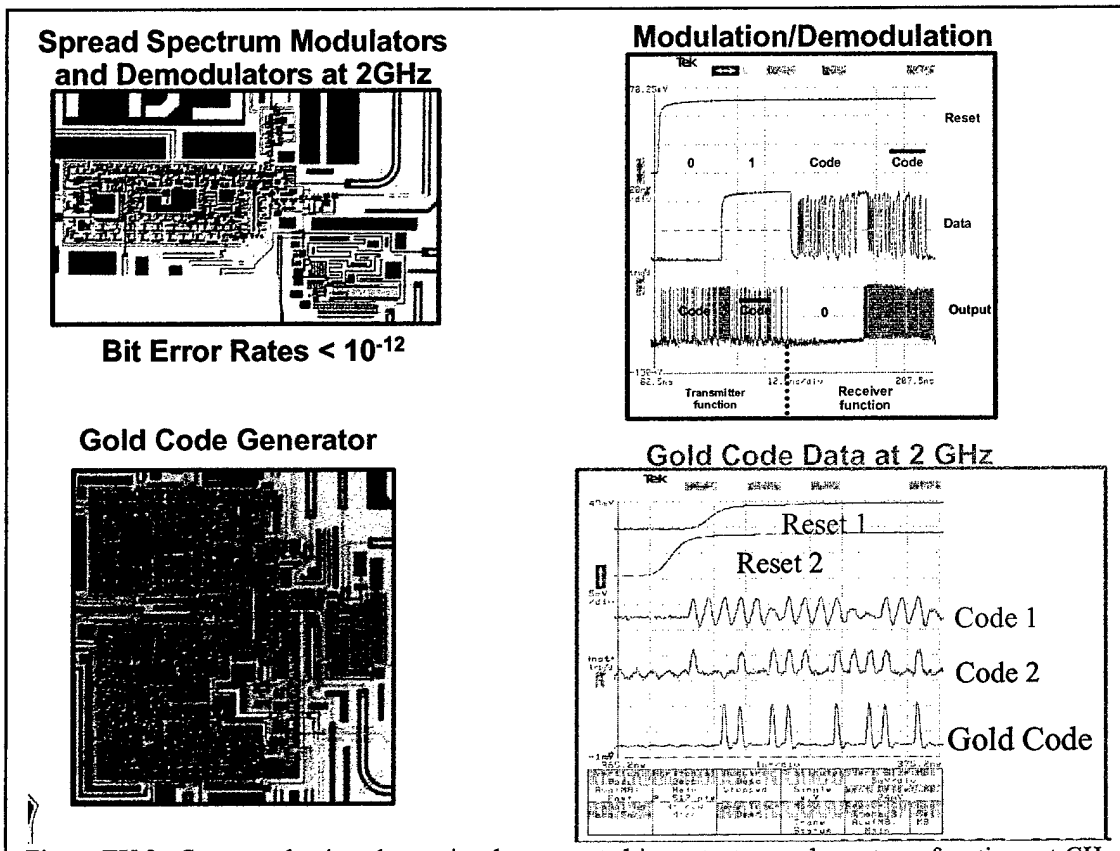


Figure EX.2. Superconductive electronics demonstrated important spread spectrum functions at GHz speed.

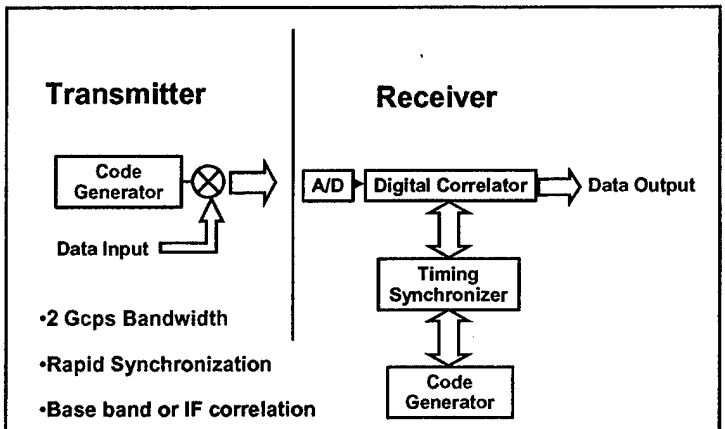


Figure EX.3. The Digital Correlator compares the output of the receiver's analog to digital converter to the local Code Generator and accumulates the correlation.

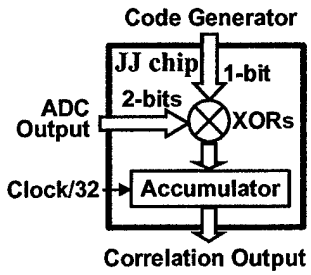


Figure EX.4. The superconductive Digital Correlator can perform GHz correlations while dissipating only 150 microwatts.

The BOSS program was directed toward the development and demonstration of a digital correlator and of a synchronizer (Figure EX.3). The correlator accumulates the correlation sum between a received packet and the local code generator. The synchronizer sets the timing of the local code generator to match an incoming packet. Only superconductive electronics can enable rapid synchronization at low power, because only superconductive electronics has microwatt circuits that can digitize GHz signals and perform GHz logic operations.

The Digital Correlator demonstrated correct mixing of 2-bit Data with Code and accumulation of the correlation sum (Figure EX.4) at speeds up to 320 MHz. It correctly accumulated single inputs at rates up to 3 GHz. The Synchronizer demonstrated most of its functions at low speed, but there were not enough funds remaining at the end of the program to complete the high-speed tests.

Another task on this contract supported the design of a Glue Chip for use in a Crossbar data switch. The Glue Chip is part of a multichip module of superconductive digital chips that form the switch fabric. The Crossbar design can sustain data rates of 2.5 Gbps on each of 1,000 circuits, in a low-latency, high-throughput configuration. The Glue Chip was designed to have high sensitivity to weak signals received from the Switch Chip. Changes in the design of the Switch Chip created a stronger signal, so the sensitive Glue Chips were not built.

Superconductive electronics is still the fastest digital technology. Network-centric warfare has an insatiable desire for increased data bandwidth. The high-speed circuits developed under these AFRL contracts have the ability to transform communications.

I. Introduction

This is the final report of the contract for Battlefield Online with Superconductive Systems (BOSS). The BOSS program sought to exploit the high speed and low power of superconductive digital electronics to develop communications links that cannot be built with conventional semiconductor components. Previous accomplishments, also supported by the same sponsor as the current contract, include the design, fabrication and demonstration of spread spectrum code generators and data modulators, which performed all of the following functions at 2 GHz:

High Speed data I/O
Data Modulation
Data Demodulation
Time Forward and Reverse Codes
Gold Codes
Base Band Demonstration of Spread Spectrum Communications.

The just-completed program was directed toward the development and demonstration of a digital correlator and of a synchronizer. The correlator accumulates the correlation sum between a received packet and the local code generator. The synchronizer sets the timing of the local code generator to match an incoming packet. Only superconductive electronics can enable rapid synchronization at low power, because only superconductive electronics has microwatt circuits that can digitize GHz signals and perform GHz logic operations.

Another task supported by this contract was the design of a Glue Chip for use in a Crossbar data switch. The Glue Chip is part of a multichip module of superconductive digital chips that form the heart of a 32x32-port Crossbar switch. The Crossbar can sustain data rates of 2.5 Gbps on each of the 32 circuits. It is a scalable design, intended to connect 1,000 processors with 1,000 memories in a low-latency, high-throughput configuration. The Glue Chip design was intended to have higher sensitivity to input signals, compared to an alternative design based on Modified Variable Threshold Logic (MVTL) gates. Changes in the design of the Switch Chips created a stronger signal, so the sensitive Glue Chips were not built.

The contract was not fully funded, due to changing priorities of the sponsors. The original value was $1,561,702 sell price. The amount obligated from the initial sponsors was only $910,000, and contract modification P00008 reduced the scope of work to conform to that funding. A final increment of $24,486 was added in modification P00009, to support one more fabrication and test cycle.

The money was all well spent, advancing our knowledge and ability to exploit superconductive electronics in the defense of freedom, as this report will illustrate. Section II reviews the status of spread spectrum modem work at the start of this program. Section III reports on the results of the Glue Chip task. Section IV describes the design and test of digital correlator chips and synchronizer chips. Section V summarizes the results and discusses the implications of this work.

II. Background in Superconductive Spread Spectrum Modem

This program built upon the success of previous contracts with AFRL to develop superconductive electronic (SCE) circuits for spread spectrum modems, most recently Air Force contract F19628-94-C-0097, "Superconducting Spread Spectrum Modem for Packet Switched Satellite Communications." Under these AFRL contracts, all of the necessary functions and interfaces for data modulation and demodulation were performed at 2 GHz. Both the transmitter and receiver functions were demonstrated, mixing data with 63-chip pseudorandom code at 2 Gcps, and demodulating mixed data.

Suppression of launch is the first stage of missile defense (Figure II.1). Rapid secure communications between theatre assets is a key feature, to find and prosecute threats. Superconductive electronics offers high speed, low power electronics to provide high data rate communications, well beyond the state of the art of semiconductor electronics.

Lincoln Laboratory was developing an analog matched filter to perform the correlation function in the spread spectrum receiver. Superconductive electronics provides GHz logic at low power, to quickly synchronize the Receiver Code Generator to the timing of the incoming packet (Figure II.2). This combination of an analog matched filter with digital code generators, modulators, and synchronization circuits formed the system concept to guide the prior work. Northrop Grumman was responsible for all of the digital circuits.

A unique aspect of the superconductive spread spectrum research was the development of high-speed interface circuits to permit real-time transfer of GHz data. For example, the code generator in Figure II.3 had an integrated 10X voltage amplifier on the output, for easy viewing on a scope. All of the inputs, Clock, Data, and Reset, could respond to signals up to 7 GHz. The operation of the code generator is shown in Figure II.4.

The code generator was designed to mix low speed DATA with CODE in an XOR gate, then output the modulated signal through a 10X interface amplifier (Figure II.5). The Lincoln Lab analog correlator required a local code generator in the receiver that produced the time-reversed version of the transmitter code. Switching the bias between the feedback taps, caused the chip to reverse the code sequence, as shown in Figure II.6.

The Josephson logic chips successfully modulated data, mixing low speed Data with 2 GHz code. As shown in Figure II.7, each Data bit produced a cycle of Code or CodeBar.

Both the Transmit and the Receive functions were demonstrated at 2 gigachips per second (Gcps), as shown in Figure II.8. Demonstration of the Receive function was prophetic, because it indicated that a digital correlator could be used instead of the Lincoln Lab analog correlator. The current BOSS program did develop a digital correlator, to be used in place of the analog correlator.

An appealing feature of shift registers with non-linear feedback is the simplicity of generating longer codes. Each additional shift register bit doubles the length of the

code. A 6-bit code generator produced the 63-chip code shown in Figure II.9. The 6-bit digital modulator also demonstrated the ability to perform both the Transmit and Receive functions at 2 Gcps (Figure II.10).

More sophisticated communications links use Gold Code generators to provide a wider selection of minimal cross correlation codes. Rapid Single Flux Quantum (RSFQ) logic was used to make 63-chip Gold Codes, as shown in Figure II.11. The relative time delay between the start of each code generator determined which of the 63 Gold codes would be generated. All 63 codes were demonstrated.

These chips work in the real world (Figure II.12). One of the most impressive demonstrations involved an electric drill with a dull bit. The technician proceeded to drill on the 19-inch equipment rack while the data modulators continued to operate, without upset, at 2 GHz. Josephson logic is low power, with small signal levels. It is more sensitive to interference than standard semiconductor logic. The spread spectrum modem programs always stressed the need to operate in tough environments. These programs led the world in the development of methods to input and output signals with multi-GHz bandwidth, while maintaining high noise immunity.

Spread spectrum communication was demonstrated between a pair of digital modulator chips located in separate dewars (Figure II.13). The block diagram illustrates the 7-chip code "0001101" being mixed with data bits "01" to produce the 14-chip modulated code sequence. A Receiver chip in another dewar demodulates the data into seven "0"s and seven 1"s. The scope traces show that in the actual demonstration a 15-chip code modulator was used. Thus, the 133-MHz data was converted to code at 2 Gcps. The scope showed the original Data "1" was recovered as 15 demodulated "1"s. Similarly, the Data "0" was demodulated as 15 "0"s.

This milestone, known as the Base Band Demonstration of Spread Spectrum Communications was described in a scientific paper, first presented at the 2000 Applied Superconductivity Conference in Virginia Beach, VA. The paper was published the following year in IEEE Transactions on Applied Superconductivity. A copy of the paper is included at the end of this section.

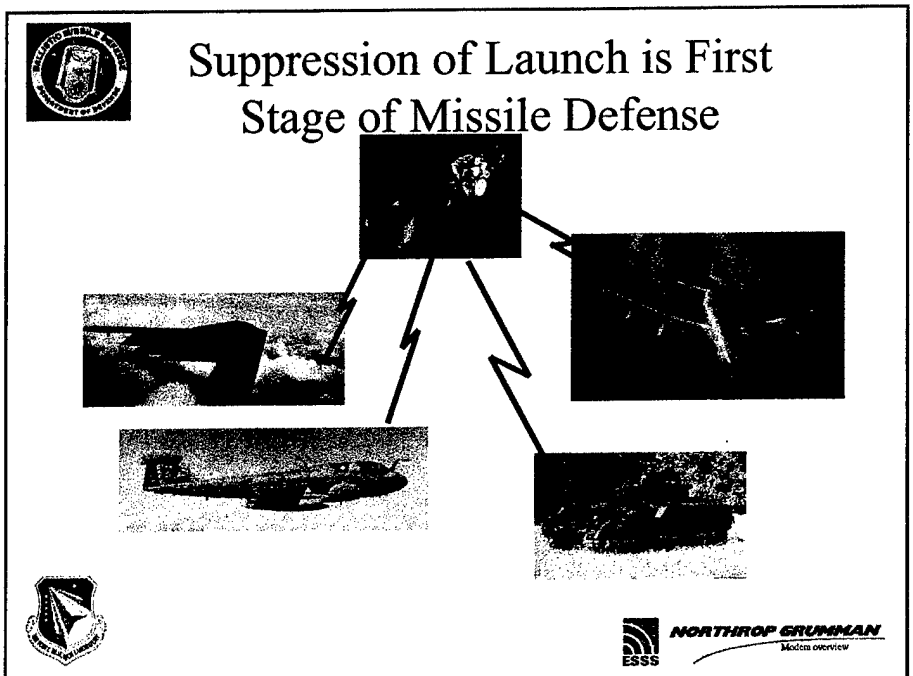


Figure II.1. Superconductive electronics provides rapid, secure, high-throughput communications to theatre task forces.

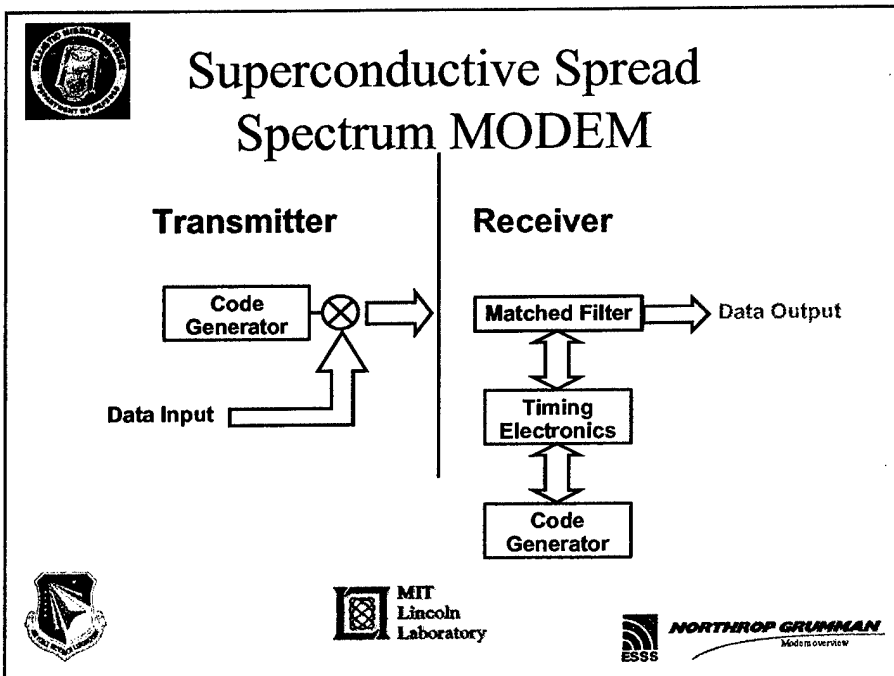


Figure II.2. Team member Lincoln Laboratory was developing the matched filter for the receiver. High speed digital logic, based on SCE, can rapidly synchronize the local code generator to the received packet.

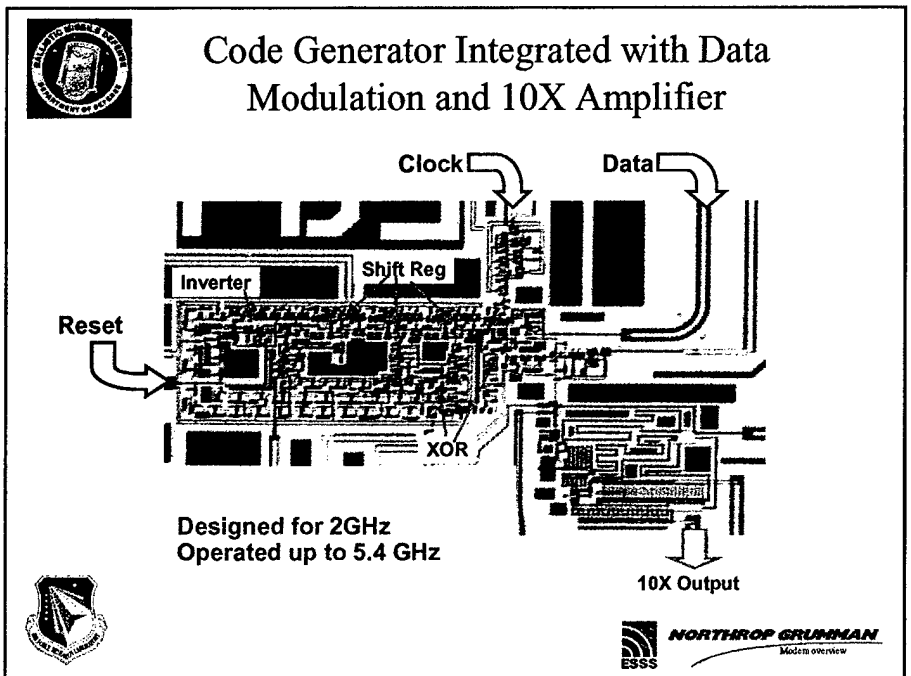


Figure II.3. The code generator signal was amplified to 18-mV by the output amplifier for easy viewing on a scope.

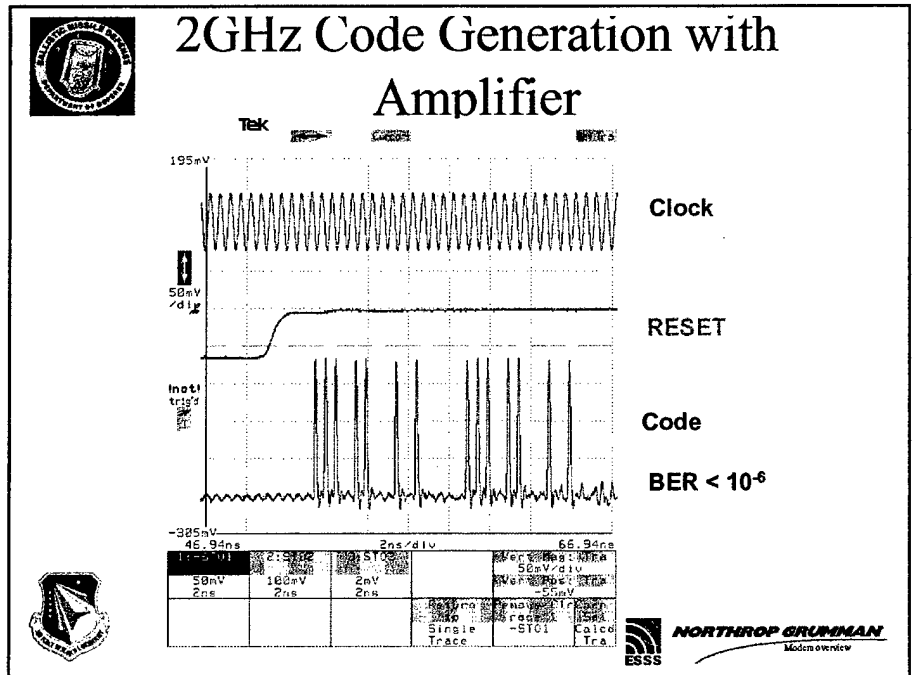


Figure II.4. Operation of the code generator at 2 GHz produced the 15-chip code, starting with the rise of the RESET signal. The 10X output amplifier had a bit error rate less than 10^{-6}. Code generator BER was below 10^{-12}.

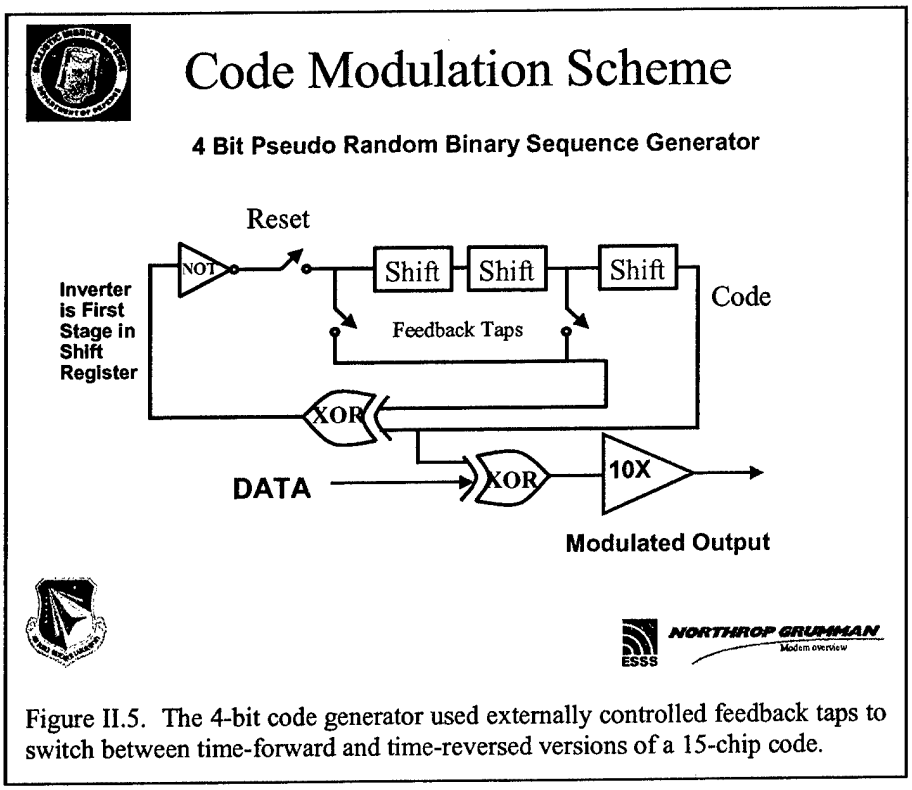


Figure II.5. The 4-bit code generator used externally controlled feedback taps to switch between time-forward and time-reversed versions of a 15-chip code.

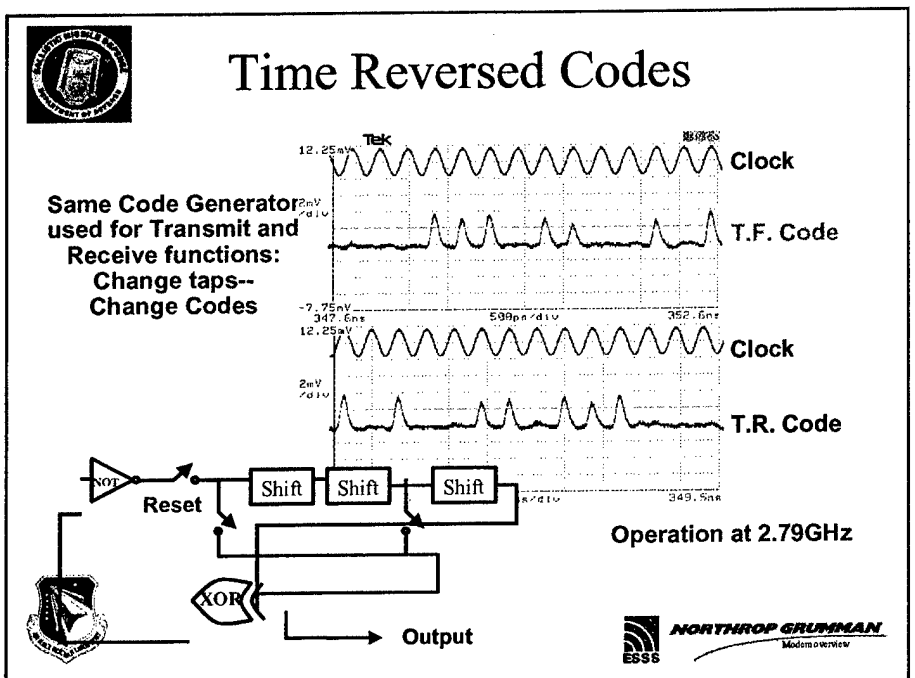


Figure II.6. The same code generator chip could be used for either the transmitter or the receiver. Switching the feedback bias current reversed the code sequence, as demonstrated here at 2.79 GHz.

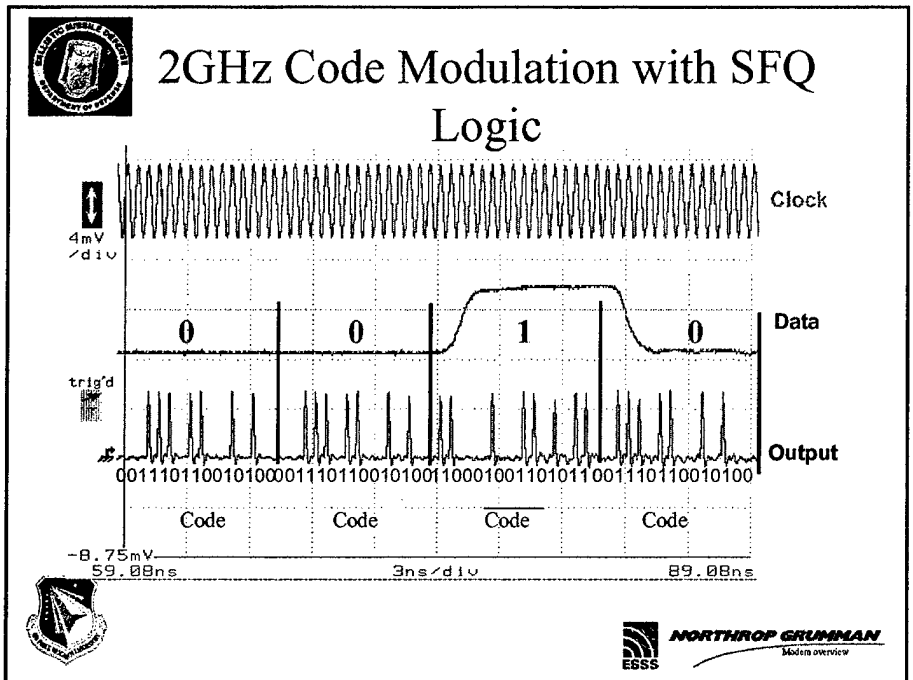


Figure II.7. The digital modulator operated at 2 gigachips per second (Gcps). Each Data_0 produced 15 chips of Code. Data_1 produced a cycle of the complement of Code. Traces are not exactly aligned due to different cable lengths.

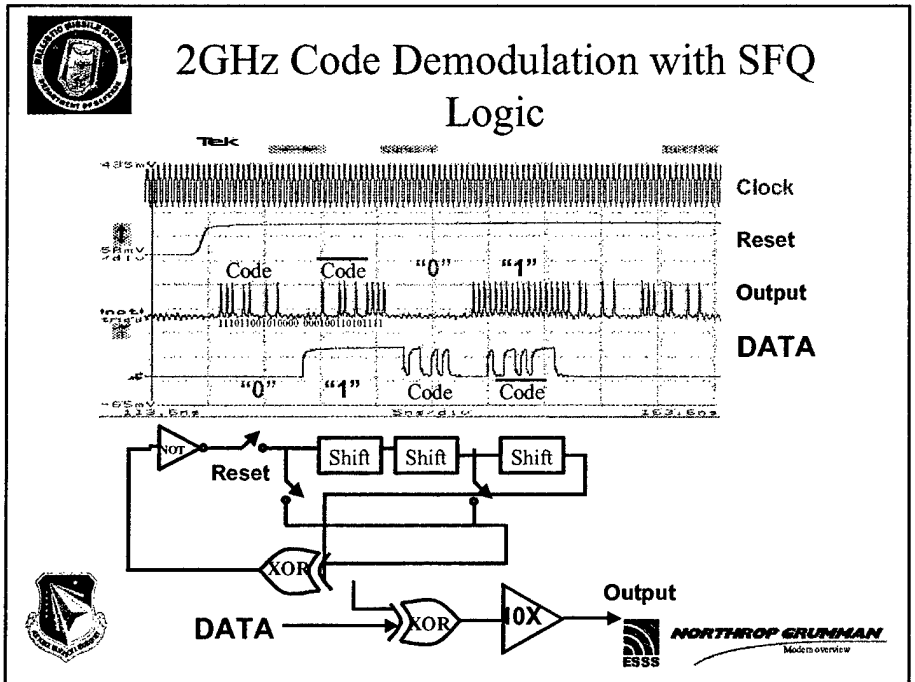


Figure II.8. The same chip could be used to demonstrate both the Transmit and the Receive functions. First DATA_0 and DATA_1 produced a cycle of Code and its complement – the Transmit function. Then a cycle of Code was demodulated as 15 "0"s, followed by a cycle of CodeBar mixed back to 15 "1"s.

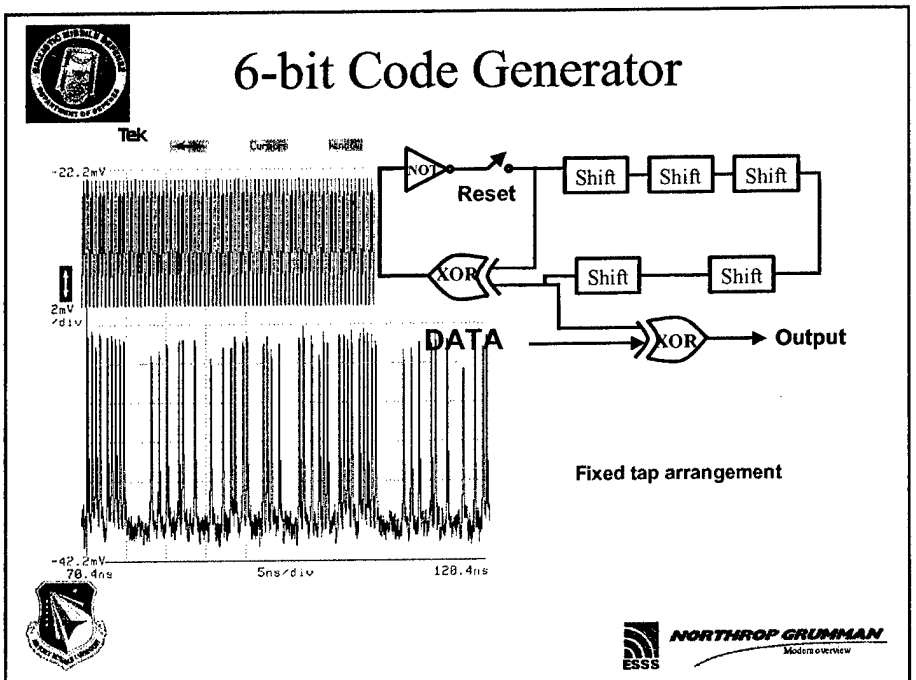


Figure II.9. Adding two more bits to the shift register made a 63-chip code generator, demonstrated here at 2 GHz.

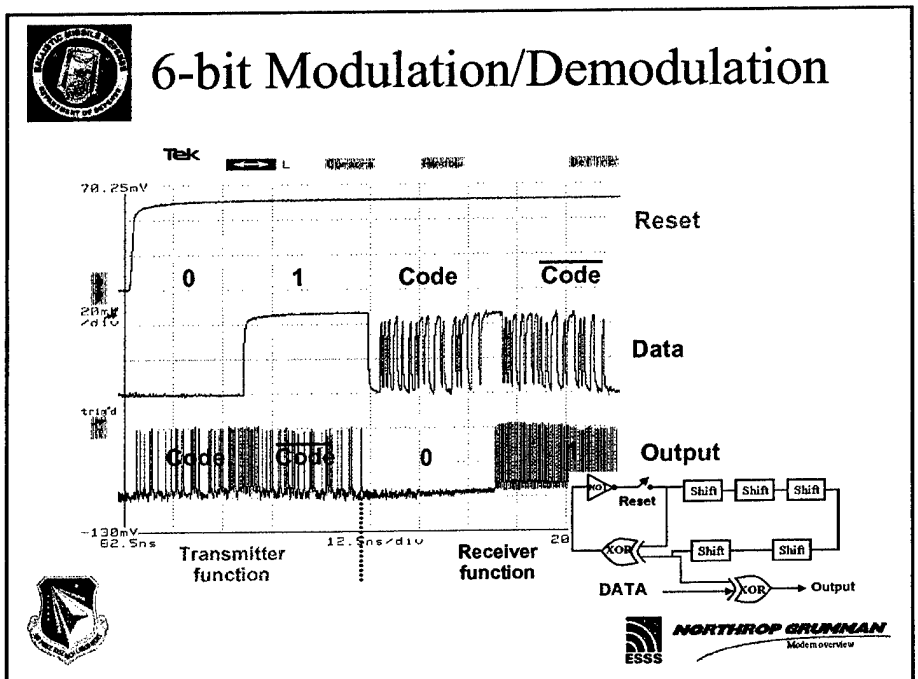
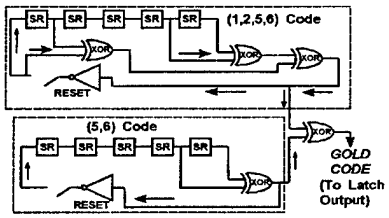
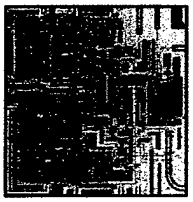
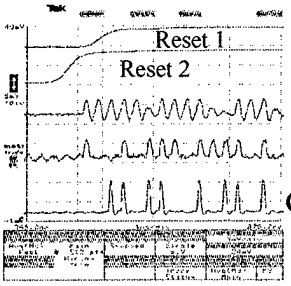


Figure II.10. The 6-bit modulator also demonstrated both the Transmit and Receive functions at 2 GHz.

Gold Codes Generated at 2 GHz







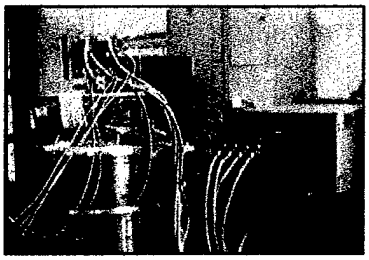
- Gold Codes were produced by XORing the two code generators together with a variable offset.

- There are 63 different Gold Codes for the 63 different time offsets in this circuit.

NORTHROP GRUMMAN
Modem overview

Figure II.11. The 700-junction chip shown in upper right used a pair of 6-bit code generators to produce 63-chip Gold codes. Design software was so good that the first chip tested worked at full speed, 2 Gcps.

Chip Performance Verified in Open Environment



- **Open Environment:**
  - **no external shielding**
- **VXI/computer controlled DC biases**
  - **margin analysis**
- **24 x 10 GHz connections to the chip**
- **Real Time high speed measurements at GHz**
- **No external high speed amplifiers**
- **Chip-to-Chip communications**

Tricks:
Inductively couple HS inputs
DC Block HS outputs

NORTHROP GRUMMAN
Modem overview

Figure II.12. These spread spectrum modem chips operated in an open lab environment, near fluorescent lights, computer monitors, and daylight streaming in the windows. They did not need shielded rooms or excessive filters.

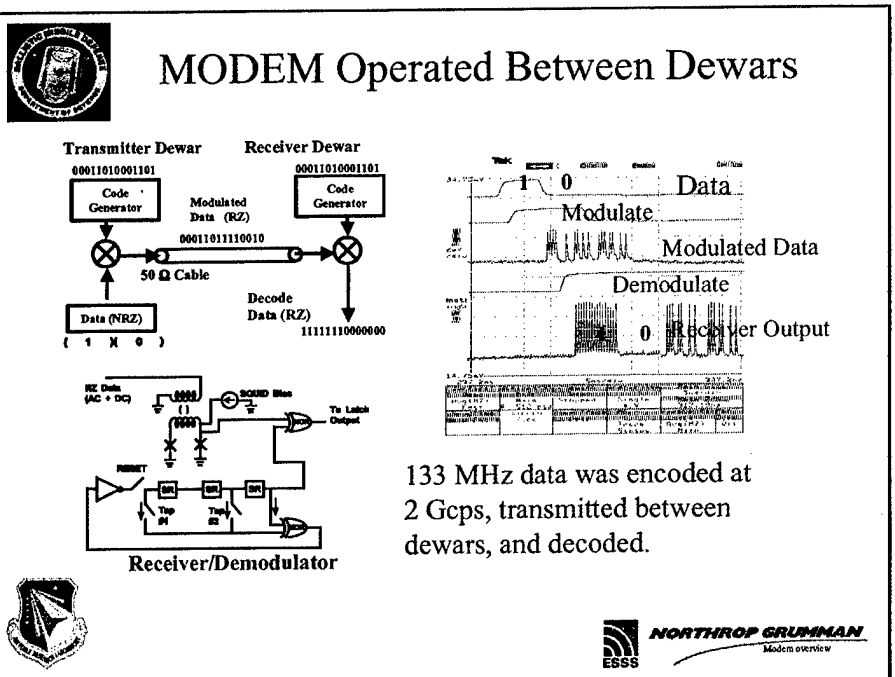


Figure II.13. For the Baseband demonstration, digital modulator chips were located in separate dewars. The first chip converted the Data "1 0" to the chip sequences "CodeBar Code". The second chip demodulated the coded Data as 15 "1"s followed by 15 "0"s. Finally, the Receiver Output showed cycles of Code, indicating an idle input.

Scientific Paper, "Spread Spectrum Data Transfer from Dewar to Dewar at 2 Gigachips per Second"

John X. Przybysz, Eric J. Dean, Paul D. Dresselhaus, Donald L. Miller, A. Hodge Worsham, and Stas V. Polonsky, "Spread spectrum data transfer from dewar to dewar at 2 gigachips per second," IEEE Transactions on Applied Superconductivity, vol. 11, no. 1, pp. 982 –985, March 2001.

Spread Spectrum Data Transfer from Dewar to Dewar at 2 Gigachips per Second

John X. Przybysz, Eric J. Dean, Paul D. Dresselhaus, Donald L. Miller, A. Hodge Worsham, and Stas V. Polonsky

***Abstract*—Spread spectrum data modulation, transmission, and demodulation has been demonstrated between SFQ chips in separate dewars. The baseband demonstration consisted of modulating (encoding) data with a spreading code, transmitting the coded data to a Receiver and demodulating (decoding) the data using an identical spreading code. The Transmitter code was produced by a 2 GHz, 4-bit SFQ pseudorandom sequence generator creating a 15-chip spreading code, which modulated a ~133 MHz data source. This data was output by a 10X superconducting latch providing ~8 mV of AC drive. This signal was fed through 50-Ω coaxial cable to a SFQ Receiver chip in a separate dewar. No amplification of the AC signal between the dewars was needed, however, a slight DC bias was added to the signal as a flux bias for the input SQUID on the Receiver. The Receiver chip consisted of an identical SFQ pseudorandom sequence generator and a data demodulation gate. Demodulating the received data with the code generator produced a replica of the data signal in RZ form. Both time forward and time reversed codes for the spreading/despreading sequence were created.**

***Index Terms*—Spread spectrum modem, Josephson digital electronics, GHz logic, single flux quantum.**

I. Introduction

JOSEPHSON digital electronics has potential advantages in wide bandwidth, spread spectrum communications. Only Josephson technology can provide low-power, multi-GHz logic for code generation, data modulation and demodulation. With the increased emphasis on frequency reuse through digital techniques, such as Code Division Multiple Access (CDMA), Josephson electronics can be a serious competitor in wideband digital communications.

High bandwidth spread spectrum communications provides a demonstration of the strengths offered by SFQ technology [1]. The speed of operation of SFQ technology is superior to that offered in silicon technologies. This speed advantage is at a premium when faced with problems that are not easily parallelized. The spread spectrum modulator/demodulator (MODEM) that we are developing emphasizes the use of a fast bit-serial technology. Correlation and data demodulation in the Receiver can be done within a few clock cycles.

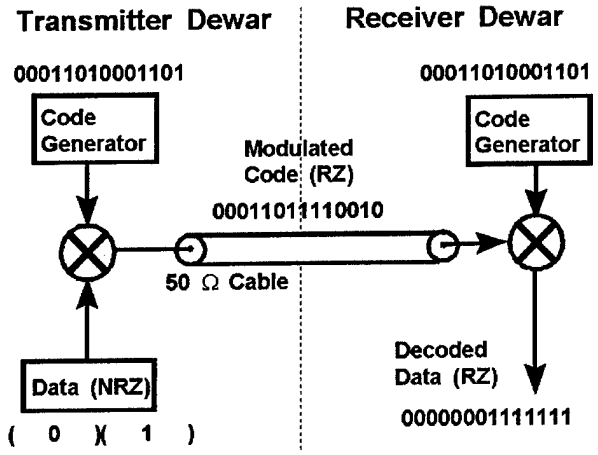


Figure 1: Josephson logic chips in separate dewars demonstrated spread spectrum communication. For illustration, the 7-chip code "0001101" is mixed with data bits "01" to produce the 14-chip modulated code sequence. A Receiver chip in another dewar demodulates the data into seven "0"s and seven "1"s. In the actual demonstration, 15-chip codes at 2-GHz rate operated on 133-Mbit/second data.

A major part of a spread spectrum modem consists of the baseband construction. This consists of taking a data pattern, modulating it with a predetermined code and transmitting the modulated (encoded) data to the outside world. This encoded data is received at a separate location and the modulation is removed, thus recovering the original data pattern. In this work, the data are modulated and demodulated by codes produced by a 4-bit pseudorandom binary sequence (PRBS) generator, which produces a 15-chip code. This requires a PRBS generator with a clock rate much greater (2 GHz) than the data rate (~133 MHz). Each data bit is encoded with a sequence of 15 code chips through an exclusive OR (XOR) operation. These encoded data are then transmitted to a receiving station on a separate chip in a separate dewar. The Receiver chip contains its own identical PRBS code generator. Data is recovered by demodulating the received code with the code produced on-chip, with manual synchronization of the two codes. A block diagram of this demonstration is shown in Figure 1.

This paper will discuss the data modulation, transmission and demodulation aspects. The aspects of code generation are discussed in more detail in [2].

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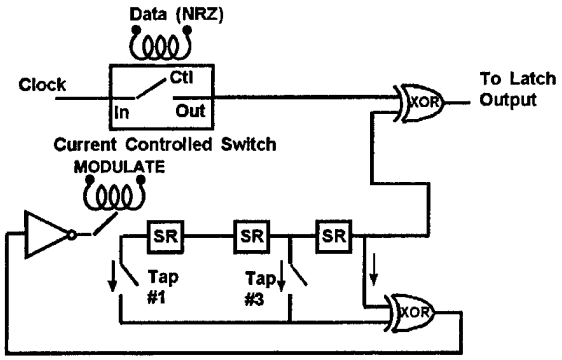

Figure 2: In the modem Transmitter, the high-speed control signals for Clock, Data and MODULATE were all inductively coupled to the SFQ functional blocks to minimize ground bounce. The code generator produced time-forward or time-reversed code in response to external control signals which closed Tap #3 or Tap #1, respectively.

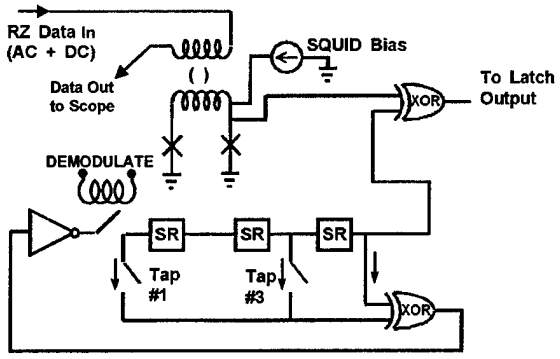

Figure 3: The modem Receiver used a 2-JJ SQUID to convert RZ data to SFQ pulses. Inductive coupling blocked 2-GHz ground ripple cross-talk between the high-speed logic chips.

II. Circuit Design

The Transmitter and Receiver circuits are almost identical. They each consist of a code generator operating at a 2 GHz clock rate that produces two possible 4-bit pseudorandom codes, an XOR cell to modulate the data signal with the code, and I/O circuitry.

The transmit circuit is shown in Figure 2. The code generator can produce two different 15-chip codes, depending on the feedback configuration. Feeding back the output of stages 3 and 4 produced the time forward code (000011101100101), while feeding back the output of stages 1 and 4 produced the time reversed code (000010100110111). The code was enabled or disabled by the "MODULATE" line. When enabled, the code generator fed out the 15-chip code indefinitely; when disabled, the code generator fed out all 0's. The code was then modulated via the XOR gate with the data.

The data arrived on chip as an NRZ signal and had to be converted to RZ for use in the SFQ circuit. The current controlled switch accomplishes just that. The NRZ data pattern provides a control signal to the current switch that causes the passing or blocking of SFQ clock pulses. The NRZ data is thus converted to SFQ pulses for use in the modulator XOR gate. Details of its operation may be found in [2]. The output of the modem XOR gate is fed to a 10X latching amplifier [3].

The Receiver circuit is shown in Figure 3. It has an input SQUID that receives the RZ data from the Transmitter and converts it into SFQ data. The Receiver has a code generator identical to the one in the Transmitter. This code generator also produces two possible 15-chip codes and is enabled or disabled by a separate "DEMODULATE" line. This code was then XORed with the data from the input SQUID. The output of the XOR, which is an RZ representation of the original data pattern, is then sent to a latching output amplifier.

III. Testing Setup

The experimental setup is shown in Figure 4. It consists of a transmitter chip containing a code generator and a data modulator in one dewar and a Receiver chip consisting of an identical code generator and a data demodulator in another dewar. Both the Transmitter and Receiver chips receive RF power from the same HP83624 RF frequency synthesizer fed through a phase shifter/power splitter box. This allows for independent amplitude and phase control for the output latches for each circuit and for the clock. The two circuits share the same clock signal.

The 10 MHz reference signal on the frequency synthesizer provided a common trigger for three HP8082A pulse generators and for a Tektronix 11801A digital sampling scope [4]. While all of the pulse generators received the identical trigger signal, the pulse parameters (signal amplitude, DC offset, pulse width and pulse delay from trigger signal) could all be adjusted independently. The pulse generators provided a "MODULATE" signal for the Transmitter, a "DATA" signal for the Transmitter and a "DEMODULATE" signal for the Receiver. The three pulse generator signals, plus the output signals for the Transmitter and Receiver circuits were all fed into the sampling scope. For both the Transmitter and Receiver chips, the SFQ modulated/demodulated data were amplified by a superconducting 10X output latch for transmission outside of the dewar. The latching amplifier outputs and the clock lines were AC coupled (~10 MHz cutoff frequency) to eliminate the presence of low frequency ground loops [3].

Both the Transmitter and Receiver circuits received DC bias from a Tektronix VXI mainframe containing five Tektronix VX4730 D/A converters (60 D/A channels total). DC bias control and data acquisition were controlled by a Power Macintosh computer running LabView software [4]. All measurements were performed in an unshielded room.

IV. Results

The results will be described in separate segments with the assistance of Figures 5 and 6.

A. Transmitter Data Modulation

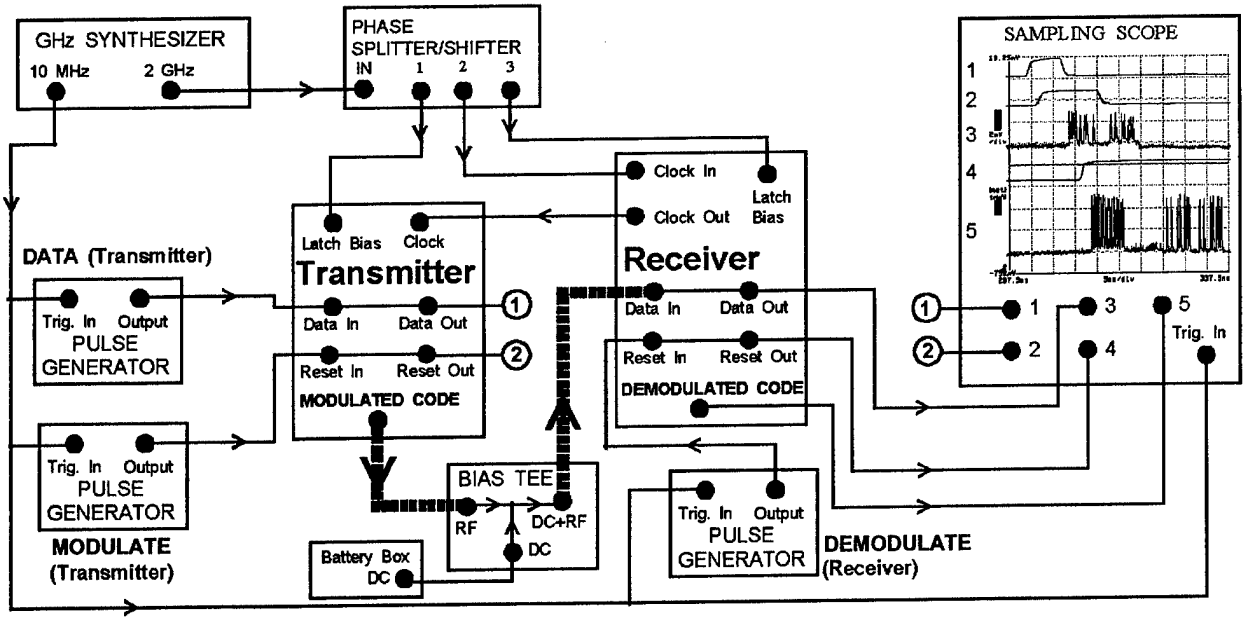

Figure 4: In this baseband demonstration, the 2 gigachips/second coded data flowed through a 50-Ω cable, indicated by the heavy dotted line, from the dewar with the Transmitter chip to the dewar with the Receiver chip. The bias Tee was used to maximize the sensitivity of the Receiver input SQUID. No power-hungry high-speed amplifiers were needed in the signal line between the dewars.

The Transmitter is responsible for the top three scope traces on Figures 5 and 6. The top trace represents a data signal. A high level indicates a data "1" while a low signal indicates a data "0". The width of the data "1" should be one period of the code generator (15 chips). The second trace represents the "MODULATE" signal enabling (high) and disabling (low) the code generator. The "MODULATE" signal allows the transmitter's code generator to produce two complete periods of code before being disabled. The output of the transmitter is shown as the third trace. Both the forward (Figure 5) and time reversed (Figure 6) codes were produced by altering the feedback configuration in the Transmitter code generator. Careful examination of Figure 5 shows a slight timing imbalance: 16 chips of complementary CODE and 14 chips of CODE, which were received as 16 "1"s and 14 "0"s. Figure 6 is exactly balanced, 15 chips of true and 15 of complement.

B. Data Transmission, Reception and Demodulation

The modulated code was sent through the 10X latching amplifier producing 2 GHz, RZ data of roughly 8 mV peak-to-peak. Ideally this signal would be sent through only 50 Ω cables to the Receiver circuit where it would be sensed by the input SQUID on the Receiver. The Receiver SQUID has its own separate bias line to adjust its sensitivity to incoming signals. However when testing the SQUID with a separate data source, we found that the SQUID would not sense any AC coupled signals with less than a 20-mV peak-to-peak level regardless of the bias current setting. This prompted us to add the bias tee to the circuit. The bias tee provides a bit of additional flux bias to the input SQUID, to ensure it will swing from lobe n=0 to n=1 and back, causing it to trigger on smaller peak-to-peak signals. We typically added 200 μA of DC bias. The DC bias through the bias tee can be reduced (but not eliminated) to roughly 50 μA by increasing the on chip DC bias of the SQUID, however, increasing the DC bias of the SQUID too much will send it into the voltage state. The latching output of the Transmitter dewar was left AC

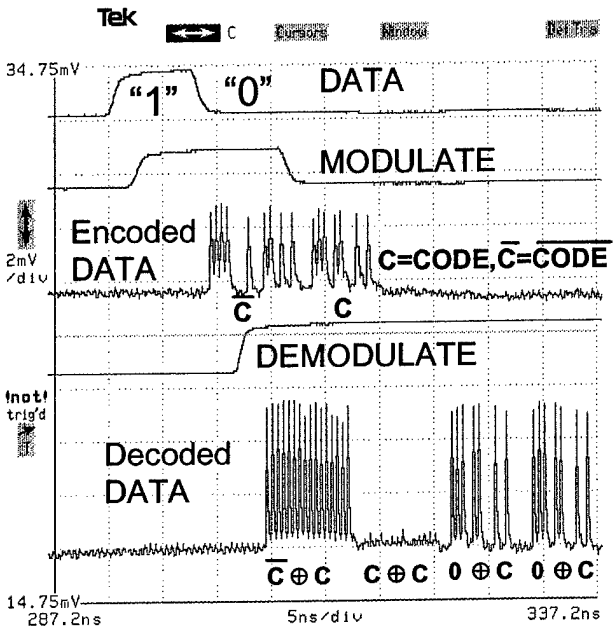

Figure 5: Data modulation and demodulation at 2 GHz with a 15-chip time forward code. Traces from the top show: the Data input to the Transmitter, MODULATE command for 2 cycles of Transmitter code, Modulated data from the Transmitter, DEMODULATE command starting the Receiver reference code, and data output from the Receiver. CODE = 000011101100101 and $\overline{\text{CODE}}$ = 111100010011010 The ⊕ symbol represents the XOR operation. The relative timing of the scope traces should be disregarded due to cable delays.

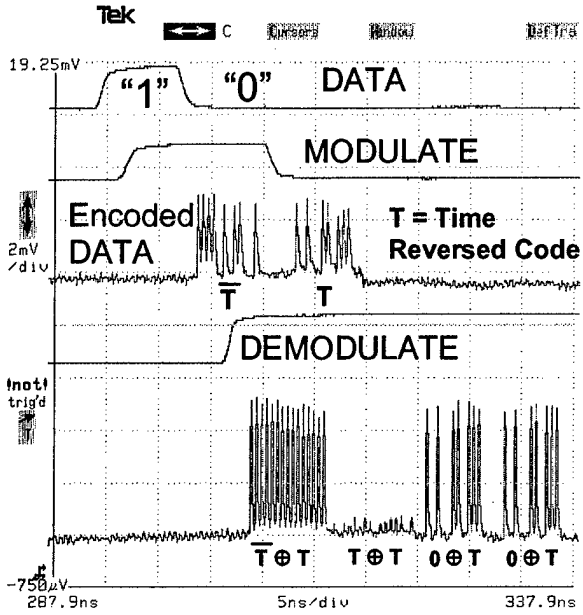

Figure 6: Data modulation and demodulation at 2 GHz with a 15-chip time reversed code. Traces from the top show: the Data input to the Transmitter, MODULATE command for 2 cycles of Transmitter code, Modulated data from the Transmitter, DEMODULATE command starting the Receiver reference code, and demodulated data output from the Receiver. T = 000010100110111 and $\overline{T}$ = 111101011001000. The ⊕ symbol represents the XOR operation. The relative timing of the scope traces should be disregarded due to cable delays.

coupled for noise considerations.

Providing the proper DC bias to the input SQUID on the Receiver led to the proper operation of the demodulator. The fourth trace on Figures 5 and 6 shows the "DEMODULATE" line enabling the code generator on the Receiver chip. This code generator produced the identical code (either forward or time reversed) as the code generator on the transmit chip. The XOR gate in the modulation portion of the Receiver chip removed the modulation impressed on the data in the transmit chip, replicating the original data signal, but now in RZ form, shown as the bottom trace in the figures.

C. Margins

Despite the fact that we now have two code generators operating, we do not expect the margins of the circuit to be significantly worse than that of a single code generator/modulator. The only two "connected" points between the two circuits are the clock line and the data line containing the modulated data. The AC margins on the DC/SFQ converter used for the clock permit as much as ±5 dB variance in the clock amplitude while still operating properly. The line carrying the encoded data has four different bias variables (AC latch bias on Transmitter, DC latch bias on Transmitter, flux bias to the bias tee and DC bias to the input SQUID on the Receiver); these bias levels may be adjusted to ensure reliable data transfer while providing little or no perturbation to the remainder of their respective circuits.

V. Conclusions

We have demonstrated a baseband construction of a spread spectrum communications system. It provides for data modulation with a PRBS code, transmission to a separate receiving station over 50 Ω cables, and demodulation of the signal to provide a replica of the original data signal. This method shows an advance over previous dewar-to-dewar data transfer methods using MVTL logic [5]. The Receiver input SQUID does not need to be clocked, which removes one additional place where synchronization of the incoming code must be performed. The additional DC flux bias that we added, while inconvenient, entails no additional synchronization issues. A redesign of the receiver input could eliminate the need for flux bias.

RSFQ circuits can spread signals across a much wider bandwidth than the 2 GHz shown here. The bandwidth of analog components, such as antennas, filters, mixers, and amplifiers, as well as legal restrictions on spectrum use, set the 2 GHz spreading rate. The much higher logic speed of RSFQ is more likely to be exploited for rapid synchronization of spread spectrum communications links.

The continued growth of wireless communications faces a challenge from the natural fixed limit of available bandwidth. CDMA has provided some relief for cellular phone service providers, using spread spectrum techniques to put more users in the same frequency bands. Future systems will user higher carrier frequencies, which can accommodate larger spreading bandwidths and higher data rates. The high speed and low power consumption of Josephson digital logic are significant advantages, which may prove decisive in the technology competition.

Acknowledgment

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References

[1] K. Likharev and V. Semenov, "RSFQ logic/memory family: a new josephson junction technology for sub-terahertz clock frequency digital systems," IEEE Trans. on Appl. Supercond., vol. 1, pp. 3-28, 1991.

[2] Paul D. Dresselhaus, Eric J. Dean, John X. Przybysz, and Stas V. Polonsky, "Modulation and Demodulation of 2 GHz Pseudo Random Binary Sequence Using SFQ Digital Circuits," IEEE Transactions on Applied Superconductivity, vol. 9, no. 2, pp. 3585-3589, June 1999.

[3] J. X. Przybysz, D. L. Miller, S. S. Martinet, J. H. Kang, A. H. Worsham and M. L. Farich, "Interface circuits for chip-to-chip data transfer at GHz rates," IEEE Trans. Appl. Supercond., vol. 7, No. 2, June 1997, pp. 2657-2660.

[4] Eric J. Dean, Paul D. Dresselhaus, John X. Przybysz, Andrew H. Miklich, A. Hodge Worsham, and Stas V. Polonsky, "Bit Error Rate Measurements for GHz Code Generator Circuits," IEEE Transactions on Applied Superconductivity, vol. 9, no. 2, pp. 3598-3601, June 1999.

[5] J. X. Przybysz, J. D. McCambridge, and P. D. Dresselhaus, E. J. Dean, J. P. Sage, and T. J. Weir, "Dewar-to-Dewar Data Transfer at GHz Rates," IEEE Transactions on Applied Superconductivity, vol. 9, no. 2, pp. 2981-2984, June 1999.

III. Glue Chip Design

The success of the Base Band Demonstration illustrates the progress that was made during the 1990s in the design and fabrication of Josephson integrated circuits. A 700-junction chip worked on the first try. The first chip tested performed better than the requirements. Especially impressive was the progress in design software.

Prof. Kostya Likharev's group at Stony Brook University developed the best software for use in designing Rapid Single Flux Quantum (RSFQ) digital logic chips. They started with Cadence simulation and layout tools, and then added the Josephson models and inductance extraction codes that they had developed at Moscow State University during the 1980s.

RSFQ logic employs inductance as a critical design parameter. CMOS circuits are less sensitive to parasitic inductance, so the standard Cadence software did not have good tools for parameter extraction. The Stony Brook software made it possible to ensure that the chip layout gave a good match to the SPICE-like circuits schematic. Northrop Grumman obtained this software under AFRL program sponsorship in 1996 and immediately applied it to the design of spread spectrum communications circuits.

The BOSS contract included a task to use this software to design a Glue Chip for the superconductive Crossbar data switch. Funds were transferred by MIPR from the Crossbar program to this contract to pay for the effort.

The Crossbar data switch used two kinds of Josephson integrated circuits, Switch chips and Glue chips. Switch chips are at the center of the multichip module and switch the circuit path among inputs and outputs. Glue chips are at the periphery of the module and serve as interfaces between Switch chip and external semiconductor circuits.

Like the spread spectrum modem chips, Glue chips use latching logic circuits to develop high signal levels on the outputs. RSFQ is a more advanced form of Josephson logic that does not employ latching junctions. Unfortunately, the RSFQ design software was not efficient at designing latching logic circuits. After considerable effort to modify the RSFQ design tools for use with latching logic, the older design tools were used to complete the design of the Glue chip.

The Glue chip designed on this program was a good design, but it was never used. It was overcome by events. Our Glue chip was designed to have high sensitivity to weak signals received from the Switch chips. A system-level design modification changed the Switch chips so that they would output a stronger signal. The program already had Glue chips that could respond to the stronger signal, so the sensitive Glue chips were never fabricated. The following is a detailed description of the Glue chip design effort.

Northrop Grumman completed work on the contract task to design a Glue Chip for use in a Crossbar data switch. Particular challenges overcome include:

Use of low critical current density (low J_c) Josephson junctions,

Lack of gain in Quantum Flux Parametron (QFP) gates,

Minimization of QFP gate count,

Optimization of latching logic circuits with PSCAN, and

High output voltage.

The Northrop Grumman fabrication process uses a Josephson critical current density of 1180 A/cm^2. These junctions are too slow to use voltage regulators that are common in other parts of the crossbar switch. In previous circuits, without voltage regulators, a bit error rate (BER) of 10^{-7} was measured for a 10X latching output amplifier. The goal here was a lower BER at a lower output voltage, only 3-4X. We used a race design, which is faster and more tolerant of variations in bias current.

The circuit schematic of Figure III.1 shows the Glue Chip design. The output stage has two sets of 4X latching amplifiers. The top set has a lower critical current. It latches on the rising edge of Vclock, if there is no input signal. An input signal will reduce the triggering current of the lower set of latching junctions. In that case, the lower set will win the race. It will latch on the rising edge of Vclock.

Hence, a race occurs on each cycle of the clock. Only one set can latch. The set that latches will divert enough current through the shunting resistor, Rdump, so that the other set will not trigger on that clock cycle. Race circuits are the fastest form of latching logic. They are only suitable for simple logic operations, like the Glue Chip.

The Northrop Grumman design was intended to use Quantum Flux Parametrons (QFPs) as an alternative to Modified Variable Threshold Logic (MVTL) gates, used in the TRW design. Since the QFPs have difficult analog properties our design methodology sought to minimize the number of QFPs. The circuit worked well with no QFPs. An earlier system level change in the crossbar switch had placed output interface circuits on the Switch chips. This raised the input signal level to the Glue chips and obviated the need for parametric amplification.

The two chief problems with QFPs are timing sensitivity and gain saturation. The QFP decision occurs when the exciter signal rises. This rise must not come too early or too late. In a circuit without voltage regulators, it was difficult to control the timing of the QFP decision. In earlier versions of the Crossbar, it was important to use QFPs because they are sensitive to small input currents. An input of only 40 μA could produce a 150-μA output. But a recent change in architecture placed a decision circuit on each Switch chip, so the input to the Glue chip was increased to 150 μA. Gain saturation in QFPs causes a 150-μA input to produce a 150-μA output. Furthermore, a 150-μA input is sufficient to trigger most standard latching gates. With a decision circuit on the Switch chip, it is no longer necessary to use a QFP on the Glue chip.

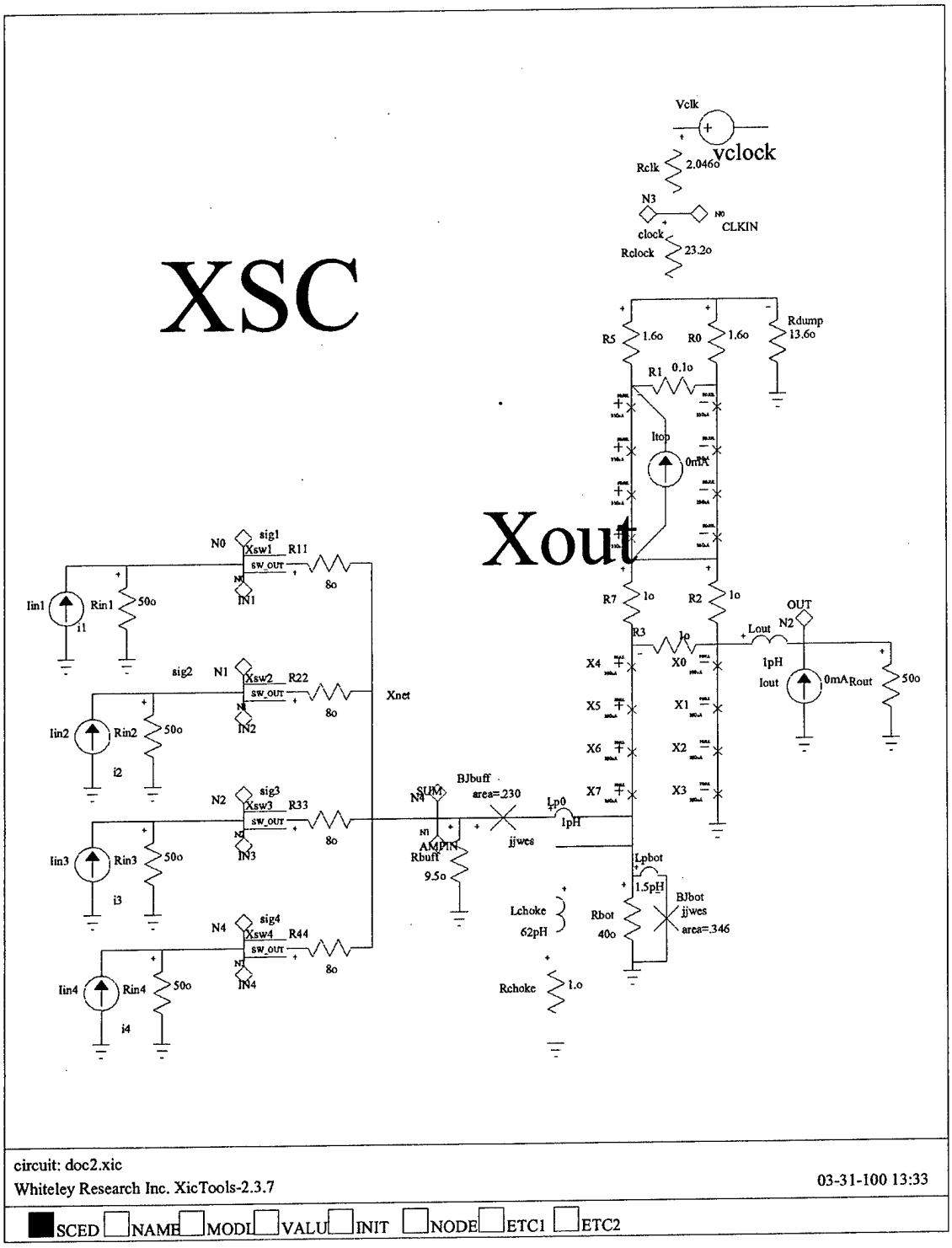


Figure III.1. Circuit schematic for the Glue Chip. The output amplifier used a race between 4-high junction stacks to get 2.5 GHz speed from 1 kA/cm^2 junctions. Junction BJbuff resolves contention by blocking more than one input signal. Junction BJbot latches to trigger the output stack, then resets after the choke current rises; this prevents punchthrough.

The Glue chip design resolves contention with a latching buffer junction. The chip can receive inputs from any one of 4 Switch chips. It should produce an output signal if there is one input of 150 μA. No output should be produced for 2, 3, or 4 inputs. As shown in Figure III.1, the combined inputs from the 4 Switch chips were passed through a 230-μA buffer junction. To produce an output signal, the junction at the bottom of the output junction stacks, BJbot, must be latched when the clock current rises. For a single input, the 150-μA current provides a trigger. For multiple inputs, the buffer junction, Bjbuff latches and diverts the input current through the resistor Rbuff, which blocks any triggering of an output.

The output stage used a choked damping resistor to aid reset of the trigger junction, Bjbot. This helped prevent punchthrough. During turn on Lchoke blocks this current path to provide strong triggering of output junctions X0-X3. After they have turned on, current rises, with a 62-psec time constant, through the choke resistor, Rchoke. Diverting the current away from Bjbot allows it to reset, even while the output stack continues to provide an output signal.

We used PSCAN to optimize the circuit design of the glue chip. PSCAN had produced the design for the Gold Code generator, a 650-chip SFQ circuit that worked on the first try. Unfortunately, PSCAN does not work well with latching circuits, like the glue chip. Ultimately, manual optimization worked better.

Much of the success of Rapid Single Flux Quantum (RSFQ) circuits is due to their highly developed optimization software. The Gold Code generator shown in Figure III.2 was optimized with PSCAN. The first chip tested worked as designed. Unfortunately, this optimization software did not work well with the latching circuits of the Glue chip. The software specifies the condition of the circuit through the junction phases. Correct operation is determined from phase changes of 2*pi during a specified time window. Attempts to adapt this to latching circuits were not successful. Ultimately, the Glue chip schematic was optimized manually.

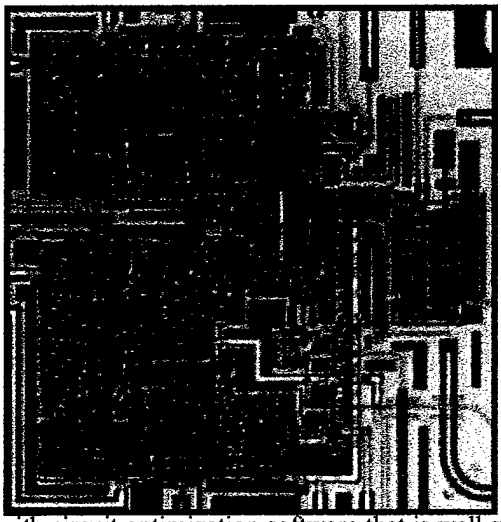


Figure III.2. PSCAN works with circuit optimization software that is well suited to RSFQ circuits like this 650-junction Gold Code generator chip. Junction phase, not voltage, is the key variable. Consequently, PSCAN optimization is not well-suited to latching logic.

The output voltage specification for the glue chip was modified to permit higher output signal levels. The previous specification was 5 to 6 mV. The new specification permits 5 to 10 mV. This allowed us to change the ratio of shunt resistor to bias resistor so that a larger fraction of the bias voltage was applied to the output. This gave good margins.

The original specification for the output voltage was based upon two stacked junctions. Since 2*Vg = 5.4 mV, the specified output voltage was 5 – 6 mV. This works well for high Jc junctions switched to the gap. Low J_c junctions will punch through at 2.5 GHz, unless they are damped to a lower voltage. More than 2-high junction stack would be needed for the output stage.

Simulations showed that there is a resistive divider effect when the output stack switches to the voltage state. The clock voltage, vclock in Figure III.1, divides across the dump resistor, Rdump, and the clock resistor, Rclock. To maximize the operating margins against variations in the clock voltage, it is necessary to drive more current to the load, Rout. A specification of 5 to 6 mV out only allows +/-10% variation from 5.5 mV. (This does not apply to voltage regulated circuits, but it is unavoidable for voltage divider circuits.) While the HBT decision circuit, which is the load, may require a minimum of 100 μA, there was no reason that it could not make a proper decision with an input of 200 μA. So the output specification was changed to permit output voltages from 5 to 10 mV, which corresponds to currents of 100 to 200 μA. This allows +/-33% variations about the mean of 7.5 mV.

The design for the glue chip is complete. A partial mask layout was started. The funds for this effort have been expended. No fabrication is planned. The Crossbar switch program has determined that the MVTL design is good enough.

In summary,

Low Jc circuits should use race gates to get high speed and avoid punchthrough.

QFPs are redundant with the new interface specifications, due to gain saturation.

Race gates work at higher output voltage, since the HBT interface circuit will accept larger signals.

IV. Digital Correlator and Synchronizer

At the outset of the current contract in April 1999, the spread spectrum modem development was directed toward the use of a digital correlator, instead of the previous analog correlator. Northrop Grumman was given the task of developing a digital correlator and the Lincoln Lab effort to develop an analog correlator ended.

In August 1999, Northrop Grumman moved its Science & Technology Center from Pittsburgh, PA to Baltimore, MD. Only two researchers stayed with the program and made the move to Baltimore, Drs. Don Miller and John Przybysz. Four people left the program to pursue other career opportunities.

Concurrently, the customer support for the SCE spread spectrum modem was rapidly diminishing, and there was little prospect of sustaining the effort in the long term. Rather than hire new designers, who could not be supported in the long term, the design of the Digital Correlator was subcontracted to Stony Brook University. The chips were fabricated at Hypres, Inc, because Stony Brook had a library of cells for the Hypres process. A second phase of the subcontract tasked Stony Brook University to design a Synchronizer chip, which was also fabricated at Hypres.

Stony Brook University performed low speed tests (up to 10 kHz) using their chip holders and test equipment. Northrop Grumman performed high speed tests (up to 3 GHz) using separate chips, which were designed to fit the high speed chip holders. The Digital Correlator performed all functions at low speed. The Digital Correlator demonstrated most functions at speeds up to 3 GHz. The Synchronizer performed most of its functions at low speed. The program was not able to complete the high speed tests of the Synchronizer on the available funds.

Here we give an overview of the Digital Correlator. The details are given in the Stony Brook University report, which follows.

The Digital Correlator compares a digital representation of the received spread spectrum signal with a locally generated code (Figure IV.1). The demodulated receive signal should rise and fall in a manner that is correlated with the local code (DATA ZERO) or anti-correlated (DATA ONE).

The Digital Correlator chip received digital data from the external test equipment, performed a digital mix, and accumulated the correlation sum (Figure IV.2). The 6-bit accumulator (Figure IV.3) could process up to 32 words of 2-bit input data mixed with 1-bit code. The 2-bit data from the receiver's analog to digital converter (ADC) represents the four possible states of the received signal – very low, low, high, and very high (Figure IV.4).

The Correlator mixed 1-bit Code with 2-bit Data (Figure IV.5). Since most semiconductor test equipment uses non-return to zero (NRZ) signal format, special circuits were used to convert these signals to RSFQ data (Figure IV.6).

It is very important to control the timing of signals as they propagate through the GHz logic gates. The accumulator used many D-cells (Set/Reset logic gates) to control timing (Figure IV.7).

The low speed Digital Correlator chip successfully performed all of its functions, though the bias margins were as low as 6% (Figure IV.8).

The high speed Digital Correlator accumulated single inputs up to 3 GHz. When only one input was HIGH, the accumulator would increment by 1, 2, or 3 counts, depending on the input (Figure IV.9). At the highest speed the margin on Bias1 was only 1.6%. The correlation output correctly indicated the number of clock cycles where the single input was HIGH. For example, Figure IV.10 shows a correlation total of 1, when the least significant bit (LSB) was HIGH for only 1 cycle.

In the tests at 320 MHz, there is noticeable amplifier droop in the outputs of the six accumulator bits (Figure IV.11). The test gear used high speed GaAs amplifiers at room temperature, between the dewar and the scope. These GaAs amplifiers had a low frequency cutoff at 500 MHz. When accumulating for 32 clock cycles at 320 MHz, the read out rate was only 10 MHz (Figure IV.12).

The Digital Correlator performance was rated satisfactory overall (Figure IV.13). It performed all low speed tests correctly. It properly mixed Code with Data and accumulated the correlation sum at 320 MHz. It accumulated single inputs at speeds up to 3 GHz.

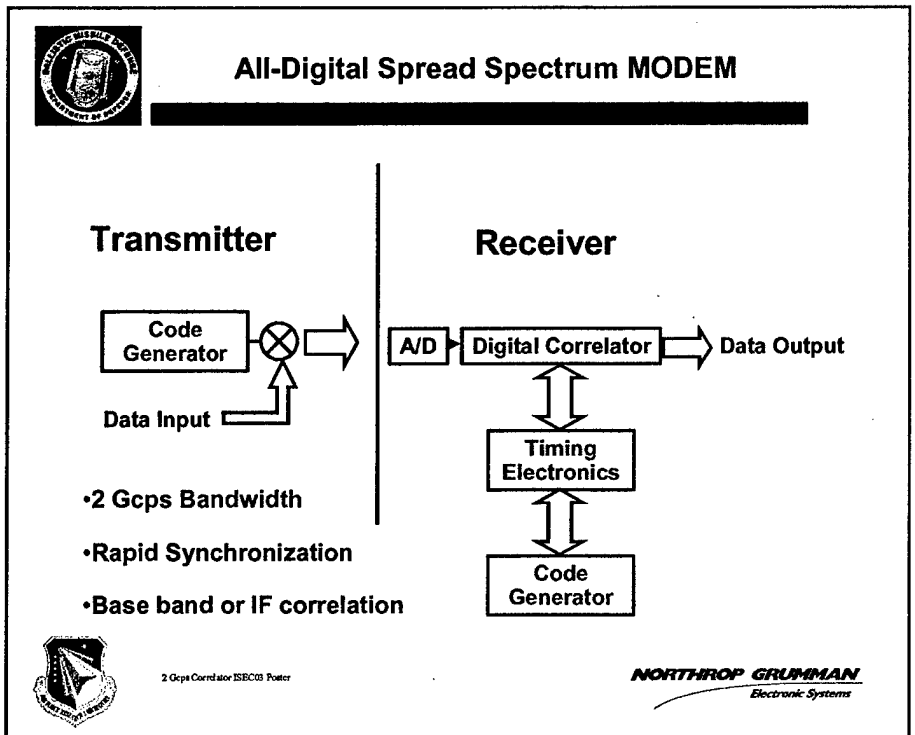


Figure IV.1. The Digital Correlator compares the output of the receiver's analog to digital converter to the local Code Generator and accumulates the correlation.

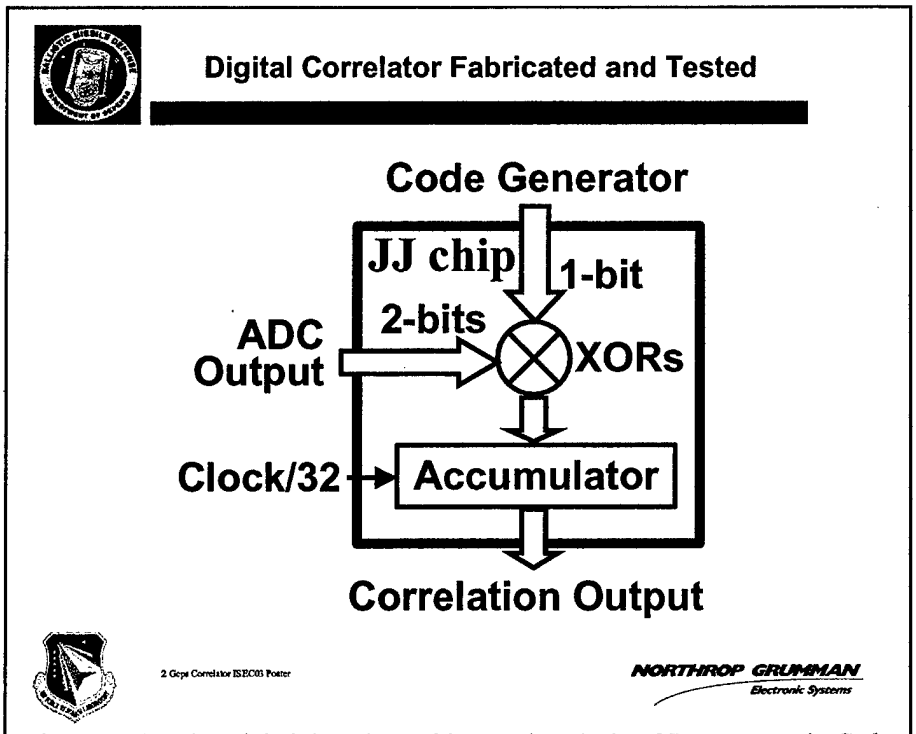


Figure IV.2. The Digital Correlator chips used exclusive OR gates to mix Code with the ADC output.

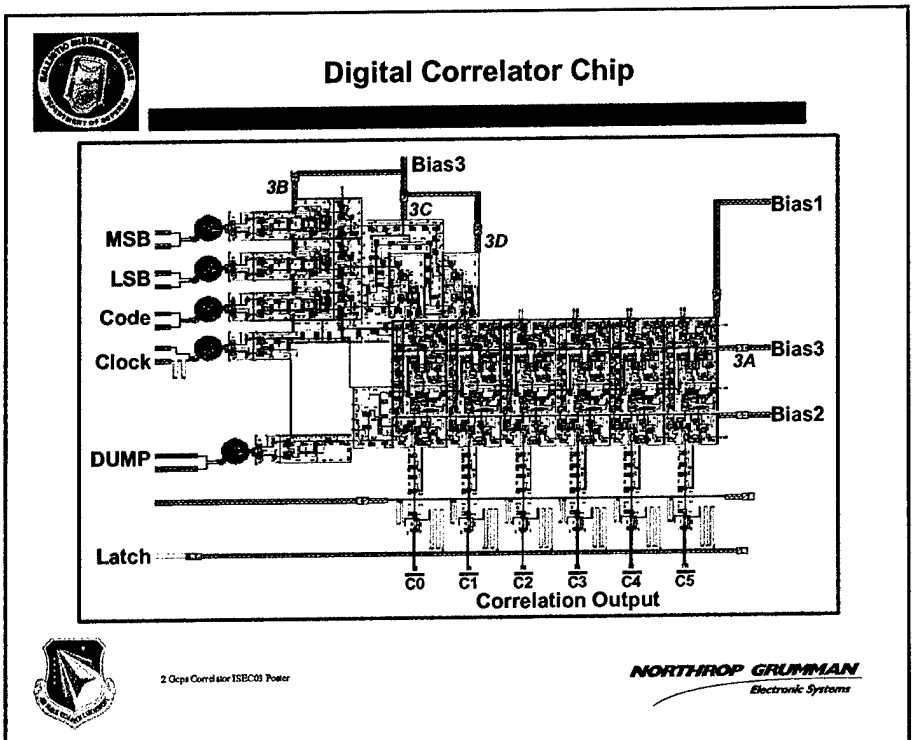


Figure IV.3. Mask drawing of the Digital Correlator. The low speed chip had more independent bias points (3A, 3B, 3C, and 3D), which were serviced by a single bias (Bias 3) in the high speed chip.

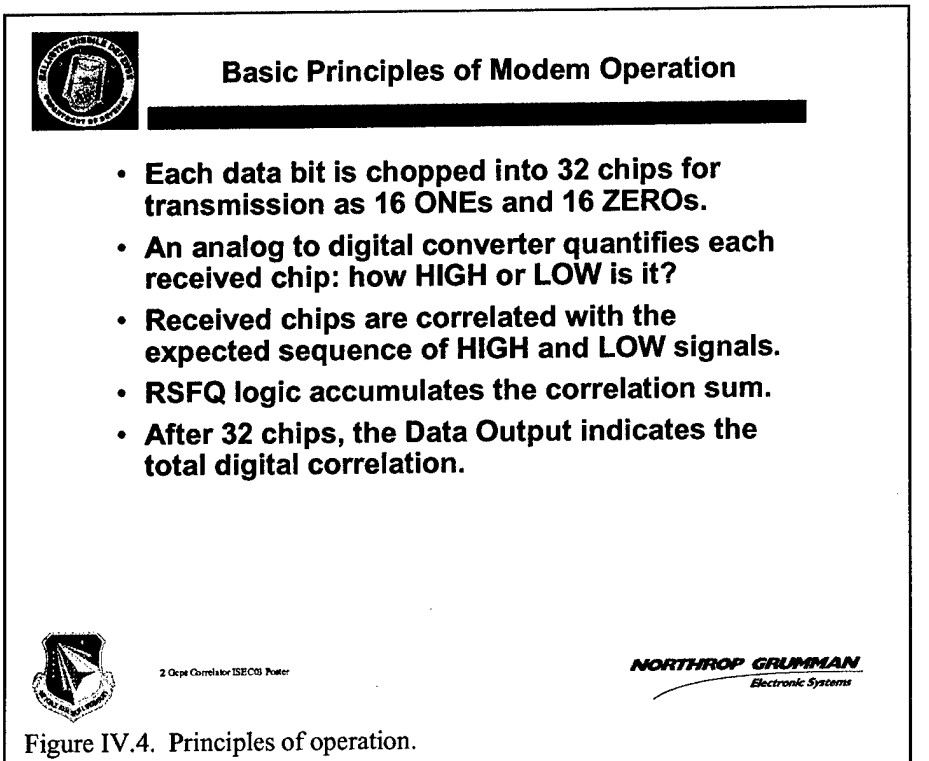
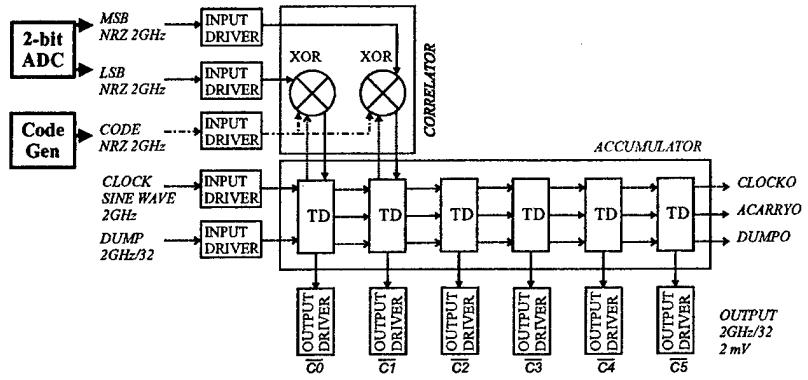


Figure IV.4. Principles of operation.

Correlator Mixed 1-bit CODE with 2-bit DATA



- **Accumulate for 32 cycles, then DUMP correlation sum.**

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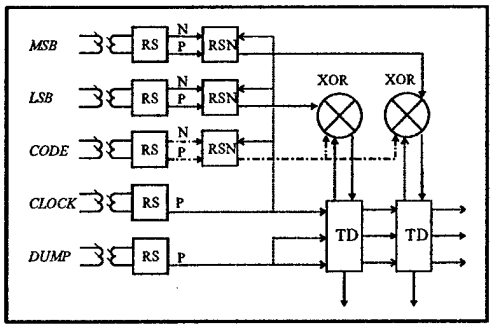
Figure IV.5. The 6-bit accumulator correlated 32 samples of 2-bit data with 1-bit code.

High-Speed Inputs Worked with Non-Return-to-Zero Data

- **RS emitted single pulse when input swung HIGH or LOW.**
- **Clock read HIGH or LOW state of RSN cell.**
  - **non-destructive read**
- **XOR gates mixed CODE and DATA.**



Flux-coupled I/O for GHz signals

NORTHROP GRUMMAN Electronic Systems

Figure IV.6. Special gates converted non-Return to Zero data inputs from semiconductor test equipment into RSFQ data.

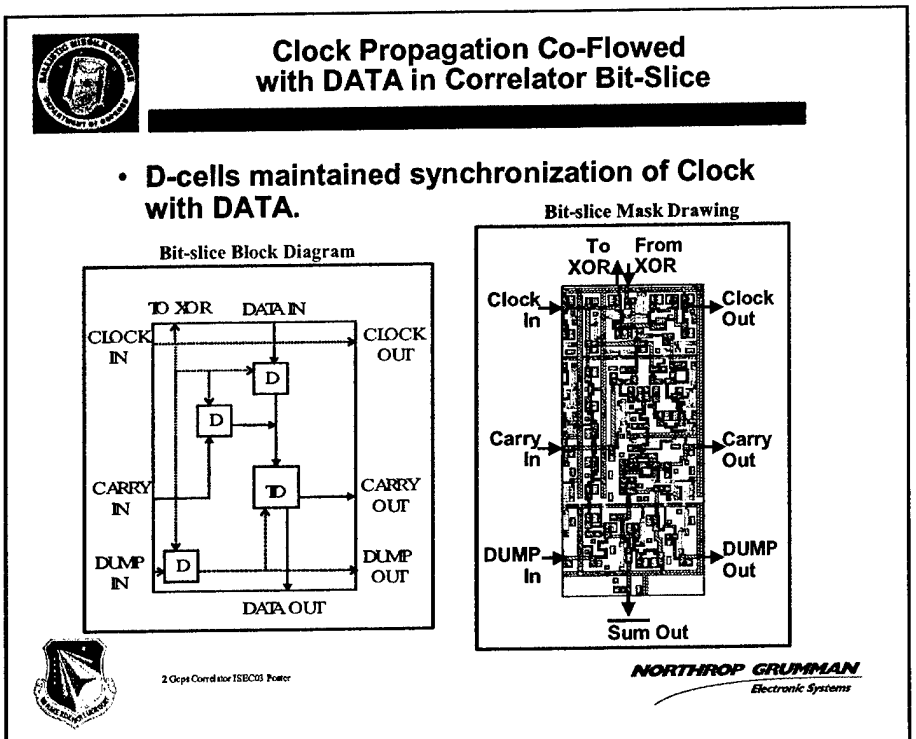


Figure IV.7. Comparison of block diagram to mask drawing for one bit slice of the accumulator.

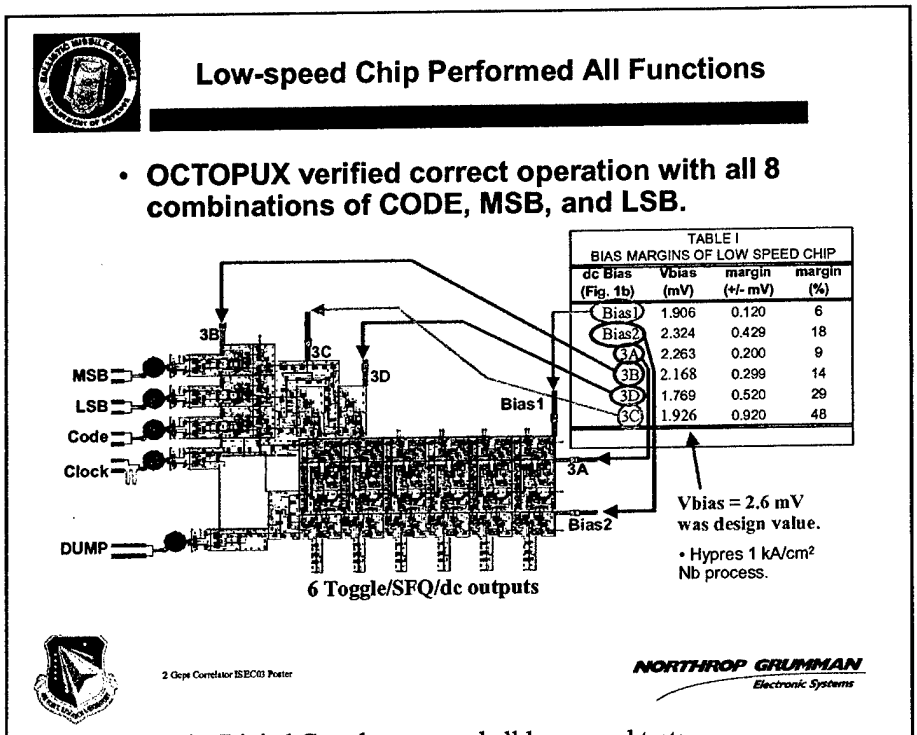


Figure IV.8. The Digital Correlator passed all low speed tests.

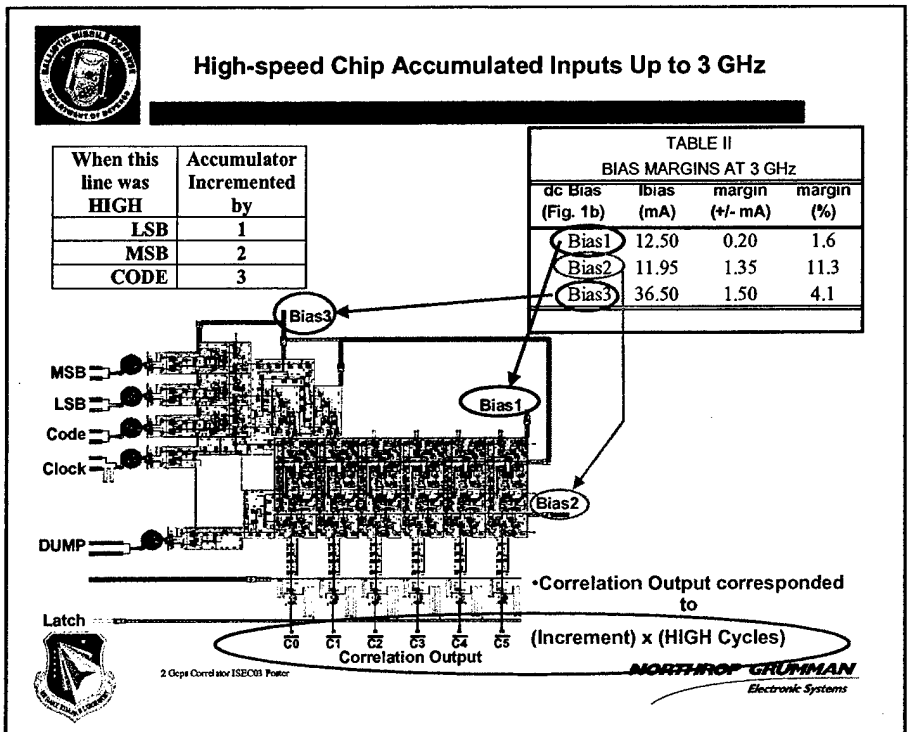


Figure IV.9. The Digital Correlator operated properly with any single Code or Data input, accumulating the number of cycles of HIGH inputs.

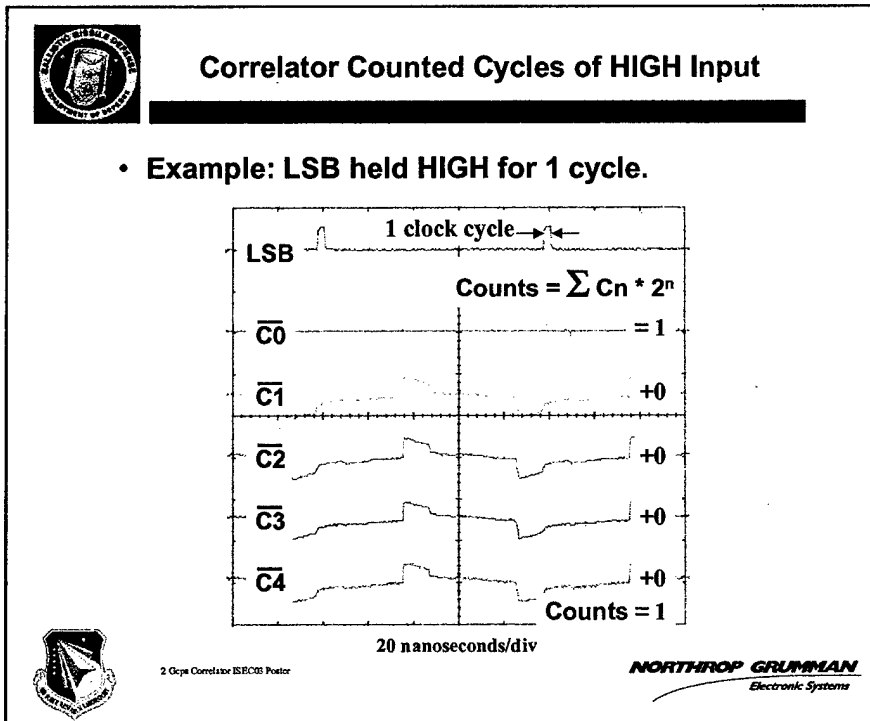


Figure IV.10. In this test the Correlator counted one cycle of HIGH signal on the least significant bit.

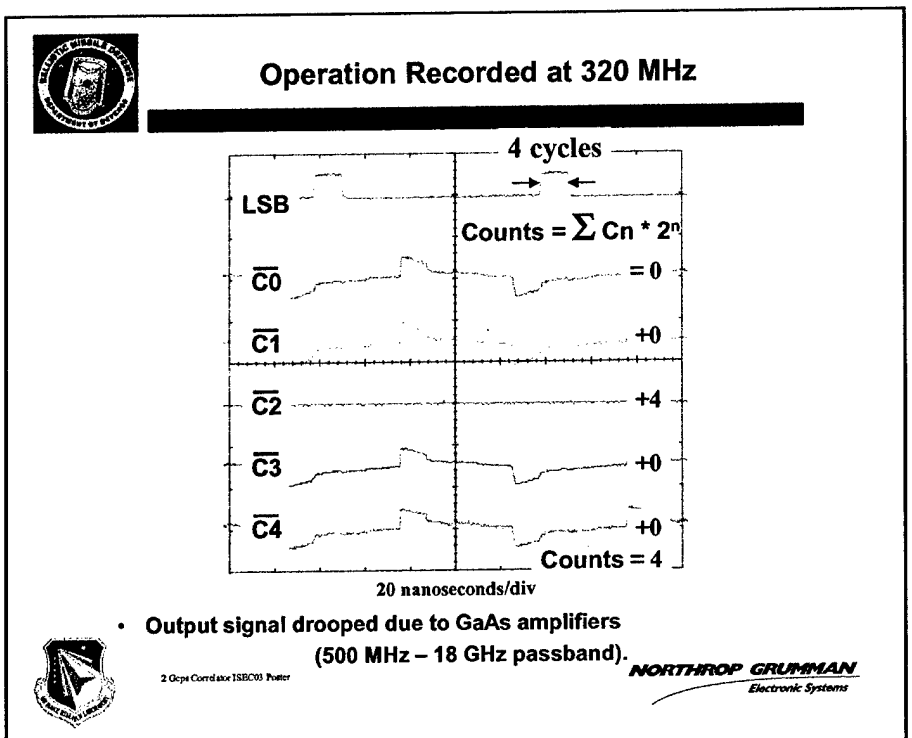


Figure IV.11. In this test the LSB was held HIGH for four cycles, which were correctly counted by the accumulator.

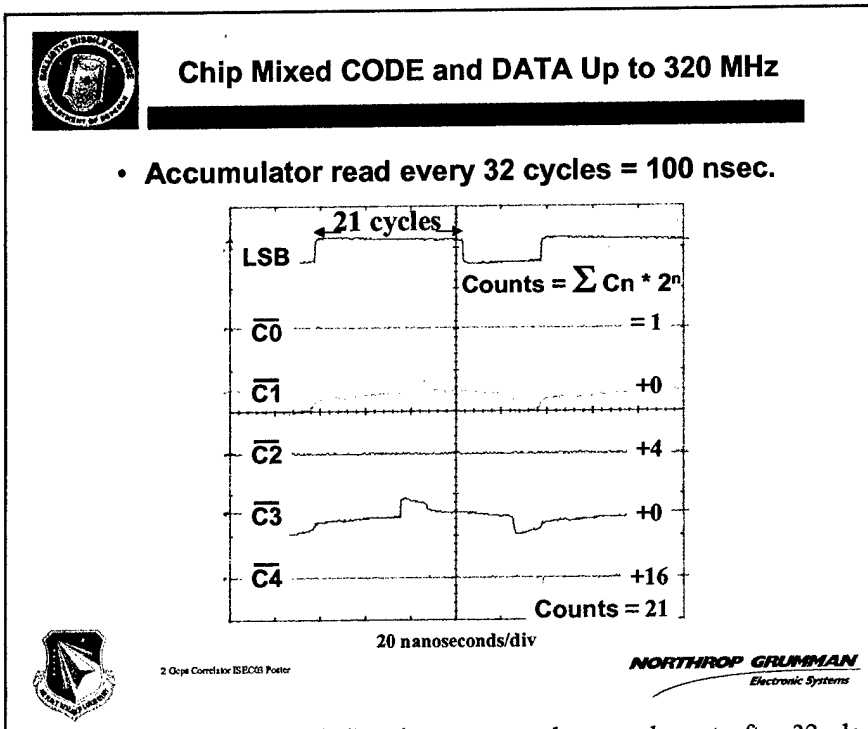


Figure IV.12. The Digital Correlator was read out and reset after 32 clock cycles. Here it counted 21 cycles of LSB HIGH.

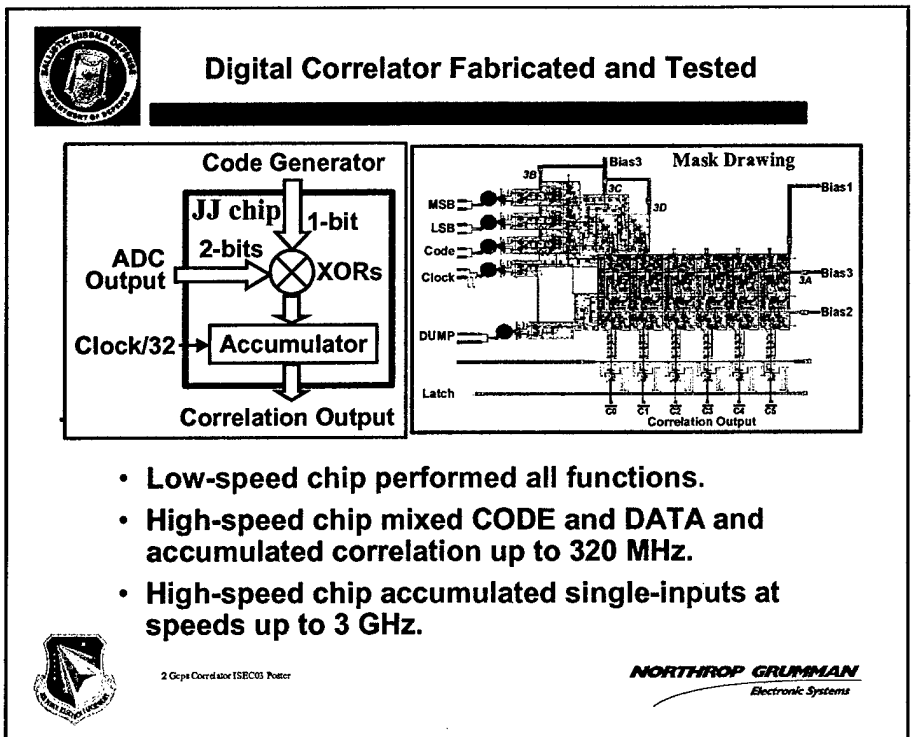


Figure IV.13. The Digital Correlator performed all functions at low speed, mixed code and data at 320 MHz, and accumulated single inputs at 3 GHz.

Scientific Paper, "Digital Correlator for a Spread Spectrum Modem Operating at 2 Gigachips per Second"

The test results of the Digital Correlator were reported in a scientific paper at the 9th International Superconductive Electronics Conference in Sidney, Australia, July 2003.

John X. Przybysz, Christopher Lavoie, Donald L. Miller, Aaron A. Pesetski, Timur V. Filippov, and Vasili K. Semenov, "Digital correlator for a spread spectrum modem operating at 2 gigachips per second," Extended Abstracts of 9th International Superconductive Electronics Conference, paper PMo16, Sydney, July 7-11, 2003.

Digital Correlator for a Spread Spectrum Modem Operating at 2 Gigachips per Second

John X. Przybysz, Christopher Lavoie, Donald L. Miller, Aaron A. Pesetski, Timur V. Filippov, Sergey V. Pflyuk, and Vasili K. Semenov

Abstract— **A digital correlator was designed in RSFQ logic, fabricated, and operated at clock speeds up to 3 GHz. One-bit CODE was mixed with 2-bit DATA in a pair of XOR gates. These correlation samples were summed in a 6-bit accumulator for 32 clock cycles. A DUMP command sent the accumulated correlation to 6 SFQ/Latch output interfaces and reset the accumulator. All functions were performed properly, while dissipating only 150 μW. The critical bias margin at 3 GHz was 1.6%.**

I. Introduction

A digital correlator can be used in the receiver of a spread spectrum communications link, such as Code Division Multiple Access (CDMA), to enable frequency reuse through digital techniques. The speed of Josephson digital circuits could enable chip rates up to 20 GHz [1], but the limited bandwidth of analog components such as amplifiers and antennas made it more attractive for this work to focus on a lower chip rate. Such a correlator could be used with 2-GHz code generators and data modulators already developed [2] – [4].

A digital correlator was designed, fabricated, and operated at speeds up to 3 GHz. It mixed pseudorandom code with a 2-bit digital representation of the received signal (2-bit ADC output). These samples were accumulated for 32 clock cycles in a 6-bit accumulator. A DUMP command read out the correlation sum and reset the accumulator for the next correlation interval.

Two versions of the correlator were tested, low speed and high speed. The low speed chip used Toggle/dc cells for diagnostic and output interfaces and had 6 independent dc bias lines. It operated correctly under all test conditions. The high-speed version used SFQ/Latch outputs, had no other diagnostics outputs, and was limited to 3 independent dc bias lines. It operated correctly up to 3 GHz, with reduced bias margins.

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This work was supported by contract F19628-99-C-0025, funded by MDA and technically managed by Air Force Research Lab, Hanscom.

II. Circuit Design

The digital correlator uses XOR gates to mix the spreading CODE with a 2-bit representation of the received signal, as shown in Fig. 1. The Least Significant Bit (LSB) of the received signal is mixed with CODE and added to the LSB of the accumulator. The MSB is mixed with CODE and added to the second accumulator bit. After 32 cycles, the DUMP command reads and resets the accumulator. The accumulator was constructed from toggle flip-flops with destructive readout; see Fig. 2.

The high-speed inputs to the chip were inductively coupled to minimize sensitivity to chip ground ripple, as shown in Fig. 3. Inductively coupled read outs were used in the RSN gates to sample the high or low state of the DATA and the CODE.

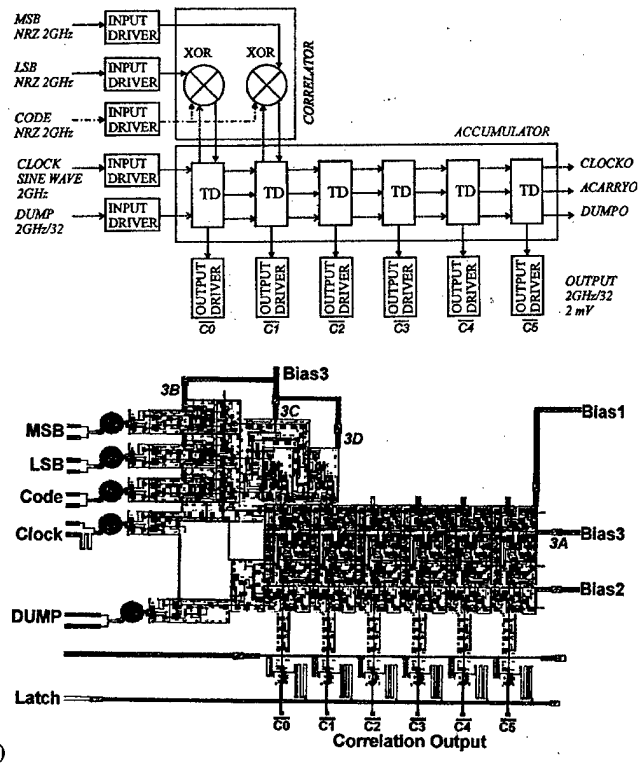

Fig. 1. The digital correlator was designed to mix the output DATA from a 2-bit ADC with the locally generated CODE and accumulate the correlation sum in a 6-bit accumulator. a) Block diagram. b) Mask drawing shows 6 SFQ/Latch converter outputs and 3 independent dc Bias lines. In the low speed chip, Bias3 was supplied by 4 independent lines at nodes 3A, 3B, 3C, and 3D.

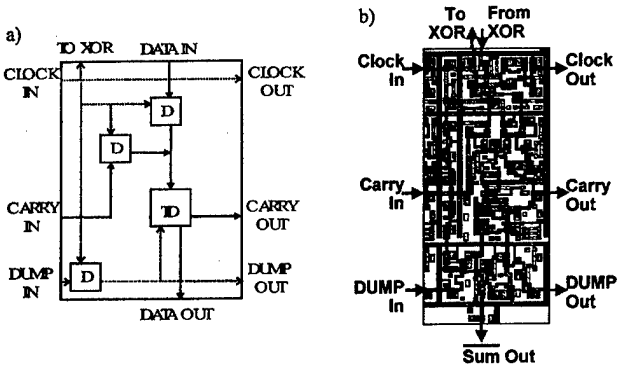

Fig. 2. The accumulator bit slice used clocked, 1-bit storage, D cells to synchronize data flow with logic gates in this forward propagating design. a) Block diagram. b) Mask drawing.

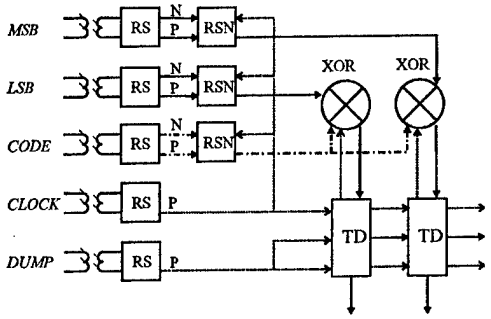

Fig. 3. The high-speed inputs were designed to accept non-return-to-zero data with a wide tolerance for peak-to-peak amplitude. The RESET/SET (RS) block emits a single SFQ pulse when the input swings High (P) or Low (N). The clock signal determines the state of the input by sampling a RS Non-destructive read (RSN) gate. Received signal is mixed with local CODE in a pair of XOR gates.

III. Test Results

Low speed tests were performed at Stony Brook University using OCTOPUX to verify correct operation with all 8 possible combinations of LSB, MSB, and CODE. The chip was designed to operate at 2.6-mV bias, but fabrication problems caused this and all chips tested from that run to be far from nominal, see Table I. Nonetheless, the chip performed all functions correctly in low speed tests.

For the high-speed tests, the accumulator was able to correctly count the number of clock cycles for which the input was high, as shown in Fig. 4. For single inputs, the accumulator would increment by 1 for LSB high, increment by 2 for MSB high, or increment by 3 for CODE high. Proper counting, mixing of CODE with DATA, and accumulation of correlation sums were observed up to 320 MHz. For single inputs, proper accumulation was observed up to 3 GHz. Bias margins at 3 GHz are shown in Table II.

TABLE I
BIAS MARGINS OF LOW SPEED CHIP

dc Bias (Fig. 1b)	Vbias (mV)	margin (+/- mV)	margin (%)
Bias1	1.906	0.120	6
Bias2	2.324	0.429	18
3A	2.263	0.200	9
3B	2.168	0.299	14
3D	1.769	0.520	29
3C	1.926	0.920	48

TABLE II
BIAS MARGINS AT 3 GHz

dc Bias (Fig. 1b)	Ibias (mA)	margin (+/- mA)	margin (%)
Bias1	12.50	0.20	1.6
Bias2	11.95	1.35	11.3
Bias3	36.50	1.50	4.1

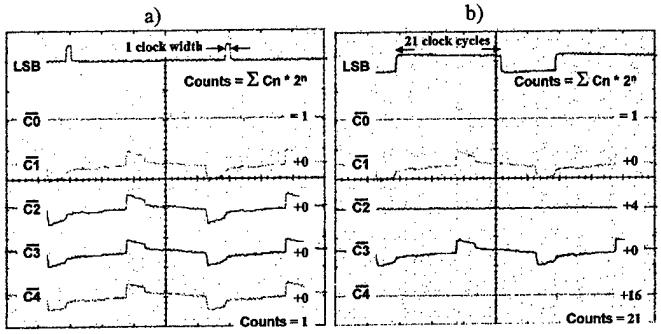

Fig. 4. The accumulator counted correctly the number of 320-MHz clock cycles for which the input was high. The DUMP signal read out the complement of the accumulator. The SFQ/Latch output signals drooped because the passband of the GaAs amplifiers was 0.5–18 GHz. a) single pulse. b) 21 counts. Time base was 20 nanoseconds/div.

IV. Discussion

The digital correlator performed the essential functions of mixing CODE with DATA and accumulating the correlation sum at clock speeds up to 3 GHz. The high-speed chip had low margins because so many bias lines were merged into a single line feeding 36 mA. Since the operating biases of the low speed chip were about 20 % below the design values, it was sufficient that the high-speed chip worked. Recent improvements at Hypres should provide better process control.

The tests presented here accumulated correlations for 32 clock cycles, but other correlation periods may be appropriate for different operating conditions. Certain combinations of CODE and DATA add 3 counts to the accumulated correlation, so a 6-bit accumulator could roll over during 32 cycles.

This correlator demonstrated the unmatched capability of Josephson electronics to perform significant digital functions at multi-GHz clock rates, while dissipating only 150 μW of power. Even accounting for cryocooler efficiency, superconductive electronics is at least an order of magnitude lower in power than semiconductors.

Acknowledgment

The authors would like to thank Mr. John Turtle of the Air Force Research Laboratory for program guidance.

References

[1] Oleg A. Mukhanov, Vasily K. Semenov, Wenquan Li, Timur Filippov, Deepnarayan Gupta, Alan M. Kadin, Darren K. Brock, Alex F. Kirichenko, Yury A. Polyakov, and Igor V. Vernik, "A superconductor high-resolution ADC," IEEE Transactions on Applied Superconductivity, vol. 11, no. 1, pp. 601-606, March, 2001.

[2] P.D. Dresselhaus, E.J. Dean, J.X. Przybysz, and S.V. Polonsky, "Modulation and Demodulation of 2 GHz Pseudo Random Binary Sequence Using SFQ Digital Circuits," IEEE Trans. on Applied Superconductivity 9(2), (1999).

[3] E. J. Dean, P. D. Dresselhaus, J. X. Przybysz, A. H. Miklich, A. H. Worsham, and S. V. Polonsky, "Bit Error Rate Measurements for GHz Code Generator Circuits," IEEE Trans. on Applied Superconductivity 9(2), (1999).

[4] J. X. Przybysz, J. D. McCambridge, and P. D. Dresselhaus, "Dewar-to-Dewar Data Transfer at 2 Gigabits per Second," IEEE Trans. on Applied Superconductivity 9(2), (1999).

Correlation is the critical function in a spread spectrum receiver, but a practical receiver must be able to synchronize with the incoming signal in a reasonable time. GPS receivers can take 30 seconds to acquire the spread spectrum signal from the GPS navigation satellites. Theatre missile defense needs rapid synchronization in its communications links. Only superconductive electronics can provide GHz logic at low power for rapid synchronization of GHz bandwidth spreading codes. The final phase of this contract designed and demonstrated Synchronizer chips for rapid synchronization of spread spectrum communication links.

The Synchronizer chip used the Digital Correlator at its heart and added additional functional blocks to accomplish synchronization (Figure IV.14). The concept of operation is that an idle receiver will begin a search for incoming packets by initializing the synchronizer chip with a SYNCHRONIZE command. The receiver Code Generator is mixed with the received signal (Coded Data In), and the correlation of these signals is accumulated for 63 clock cycles, and then dumped to the Test circuit. A signaling protocol is assumed whereby the Transmitter begins each data packet with at least 63 complete cycles of CODE_BAR, to provide adequate opportunity for the Receiver to find synchronization. This header represents an overhead of 3% on a standard JTIDS packet of 2 kilobits, which is well within the 5-10% overhead goal.

The synchronization chip finds the timing of the local code generator by searching all 63 possible timings of the 63-chip code. While the Receiver code generator is out of synch with the incoming packet header, the correlation sum will accumulate to 31 or 32. The Receiver code generator will skip one clock cycle, then try the next timing relative to the incoming signal. When the Receiver finds the right timing, the correlator can accumulate 63 outputs from the XOR gate. This indicates synchronization.

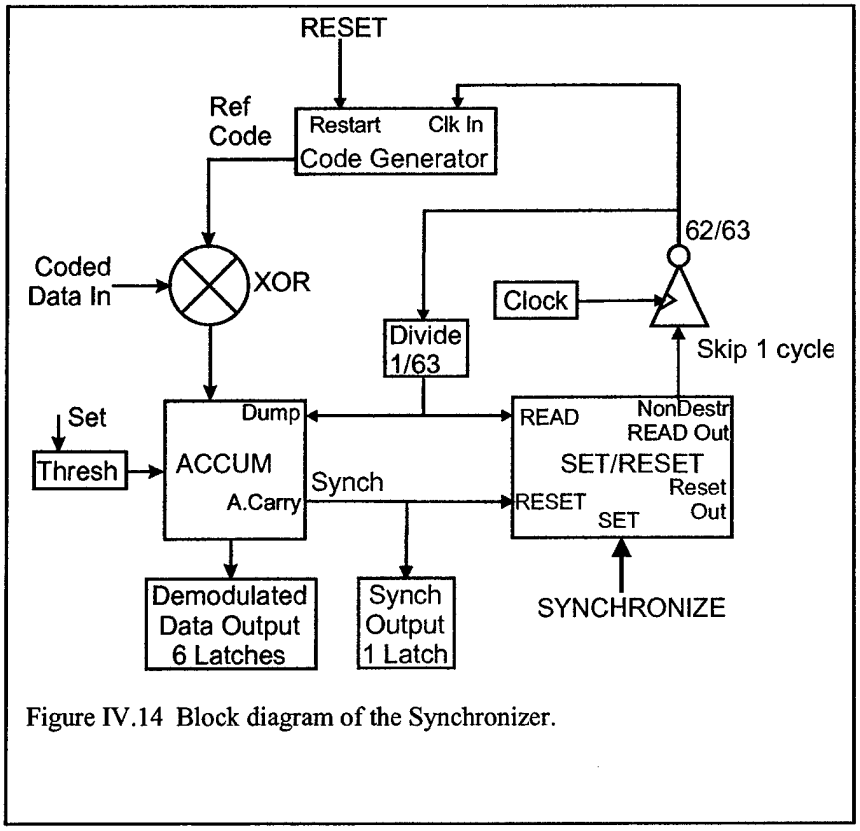

Figure IV.14 Block diagram of the Synchronizer.

To provide the largest noise margin, the Threshold circuit is set to 47, midway between no synch at 31, and complete correlation at 63. In practice, this is accomplished by preloading a count of 17 into the accumulator. Then the 47th correlation count causes the 6-bit accumulator to roll over (17 + 47 = 64), which generates an asynchronous carry pulse to signify that the timing of the local code generator is synchronized with the incoming signal. This resets the SET/RESET block, locks the timing of the local code generator, and stops the preloading of the threshold count. Subsequently, the correlator will accumulate 63 counts for Data_ONE and 0 counts for Data_ZERO, in the absence of noise. Noise and jamming will cause less perfect correlation, but the threshold of 32 counts can still be used to distinguish ONEs from ZEROs.

Synchronizer chips were designed, fabricated, and tested. The original designs had a mask-drawing flaw, which was corrected. The final fabrication run produced working chips. The low speed chips successfully performed most of the functions individually. The low speed Synchronizer:

loaded the Threshold quantity into the Accumulator,

the Accumulator counted correctly,

the code generator produced the proper code,

the clock was divided by 63,

and the code generator skipped one clock cycle after 63 cycles while SYNCHRONIZE was SET at HIGH.

The high speed tests were not completed. The high speed chip holder has fewer I/O leads. Most of them were used for biases and signal Input/Output. There were no diagnostic leads to aid in finding proper bias conditions, so testing progressed slowly. The funding ran out before high speed operation could be verified. It is estimated that another $50,000 would be needed to complete the high speed tests.

A detailed description of the Synchronizer chip and low speed tests is given in the following report from Stony Brook University.

DEVELOPMENT OF RSFQ COMPONENTS FOR SPREAD SPECTRUM RECEIVER

Report to the

Northrop Grumman

Electronics Sensors and Systems Sector

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I. Introduction

A major part of a spread spectrum modulator/demodulator (MODEM) consists of the baseband construction that includes taking a data pattern, modulating it with predetermined code and transmitting the modulated (encoded) data to the outside world. This encoded data is received at a separate location and the modulation is removed, thus recovering the original data pattern.

This approach is used widely in semiconductor electronics to provide reliable and secure communications links (see, e.g., [1]). However, we believe that the unique properties of superconductor SFQ technology [2], such as low-power consumption and high multi-GHz speed (recently superconductor ADC operating at 19.6 GHz has been reported in [3]), will permit to improve MODEM's characteristics and even win the competition with silicon technologies.

The whole Transmitter/Receiver system can be and should be divided into several subsystems to be analyzed and designed using SFQ technology. Some of them have been tested recently. They include RSFQ circuits to modulate, transmit, and demodulate encoded data without their accumulation [4-6]. All experimental data have been obtained at 2 Gigachips per second rate. The data were modulated by bit patterns produced by a pseudo random binary sequence (PRBS) generator [7]. Each bit of data is encoded with a sequence of code chips through an exclusive OR (XOR) operation. These encoded data are then transmitted to a receiver (dewar-to-dewar transmission). The spread spectrum receiver contains its own identical PRBS generator; a correlator to decode incoming data using code produced on-chip through a XOR operation.

There are also several subsystems to be designed and tested as separate parts. The first one is an accumulator of decoded data; the second is a multi-bit correlator. The last function to be checked is a self-synchronization of PRBSs located on Transmitter and Receiver chips.

II. Structure of a correlator and an accumulator

The block diagram of a 2-input correlator and an accumulator is shown in Fig.1. Two XOR gates form the correlator. An accumulator consists of 6 TD modules based on T flip-flop with destructive read out (the block diagram of a TD module and its layout are shown in Fig.2).

The correlation is stored during 63 clock periods. Then the DUMP pulse reads out the content of the accumulator, sends it to output drivers and resets the array of TD cells into the initial state. In the ideal case the number 63 stored in the accumulator corresponds to single "one" coded by a transmitter and encoded by a receiver. The zero output of an accumulator corresponds to a single "zero" sent by transmitter in form of 63 coded pulses.

The design has 5 input channels: the CLOCK and DUMP channels, 2 data channels (DAT1 and DAT2) and the CODE channel. CLOCK pulse processes any combination of incoming DAT1, DAT2 and CODE pulses. Note that for purposes of this

demo experiment, the SFQ code generator and the 2-bit ADC are simulated using a external pulse pattern generator.

The 1st XOR feeds the 1st slice of the accumulator. The output of the 2nd XOR is connected to the 2nd slice of the accumulator. As a result left alone DAT1 pulse adds "1" to the number stored in the accumulator and DAT2 pulse adds "2", while CODE pulse alone is added to both 1st and 2nd slices (effective added value of 3). When those pulses do come together the result of a XOR function between data and CODE channels is sent to appropriate slice.

All possible resulting output of the correlator during one clock period can be described as SUM = XOR (DAT1, CODE) + 2 * XOR (DAT2, CODE).

If all six TD cells forming the accumulator are in the state "1" (equivalent to the stored number 2^6 -1=63) and a new data pulse arrives from the correlator and there is no DUMP pulse, one can expect a pulse at ACARRYO output (see Fig.1) and the states of all TD cells become "0".

The details of front-end interface are shown in Fig.3 (only two slices of an accumulator are shown). Sine waves or NRZ signals from external pattern generators are applied to imitate CLOCK, DUMP or CODE, DATA1, DATA2 signals respectively. All of them are magnetically coupled to RS cells. As a result rising and falling edges of the applied external signals produce patterns of SFQ pulses labeled P and N in Fig.3. The P pulses corresponding to CODE and DATA1, DATA2 set states of RSN cells (RS flip-flop with non-destructive read out; based on TN cell described in [8]) so that CLOCK pulses read out 1's and forward them to XOR gates to be processed.

The pulse sent through DUMP channel splits into two. The first one reads out states of all TD cells and serves as a true DUMP pulse. The second delayed pulse is auxiliary. Because of particular design of TD cell its state after DUMP pulse is "1" in contrast to required "0". So the second delayed pulse feeds CARRY IN input (Fig.2) of the 1st slice. Provided that there are no incoming data during the next clock period, delayed pulse will create a CARRY OUT pulse in all 6 slices and as a result sets all TD cells in "0" states. Note that one can observe just described CARRY OUT pulse on the output via the ACARRYO terminal shown in Fig.1 and use it to monitor the proper operation of the circuit.

The circuit is biased by 6 independent dc voltage sources. BTR line feeds the front-end interface; BXOR line supplies two XOR gates; BCL1 and BCL2 biases affect the propagation of CLOCK and DUMP pulses respectively; BK bias affects the operation of TD cells; BFR line controls all output monitors. The CLOCK, DUMP, DAT1, DAT2 and CODE input drivers (see Fig.2) are fed by alternate currents. They can be characterized by two threshold levels I_{high} and I_{low}.

III. Testing

Two slightly different chips were designed for low- and high-frequency testing and both of them were fabricated by Hypres, Inc using the standard 1kA/cm^2 niobium process [9]. The chip for LF testing includes additional standard SFQ/dc converters [2] to monitor CLOCKO, ACARRYO and DUMPO outputs (Fog.1). The high-voltage output drivers/latches [10] were also replaced by standard SFQ/dc converters for the sake of simplicity. For LF measurements we used OCTOPUX experimental setup [11] that does

not require high-voltage signals. The layouts of the chips CORR04/CORR05 for HF/LF testing are shown in Fig. 4.

A. Low-frequency

During the first phase of chip testing the preliminary working point of bias voltages was found. In order to do it some test pulses were sent and all available output monitors were observed.

Let us describe, for example, the simplest experiment with ACARRYO monitor. As it was discussed above, by sending pulses through DAT1, DAT2 and CODE channels we effectively add 0, 1, 2 or 3 to TD cells of the accumulator. After sending 64 pulses through DAT1 channel (1 per each clock period) one can expect to see exactly 1 output through ACARRYO channel. So it permits to adjust BK bias for correct logic operation of TD cells. This preliminary testing gave also the values of threshold levels of the alternate current to feed input drivers: $I_{high} = 0.3$ mA and $I_{low} = -0.25$mA.

During the second phase we performed more complicated testes. Our testing procedure was based on continual comparison of experimental data with the predictions of a computer simulator developed specially for our testing purposes. This simulator includes mathematical description of all cells and their responses on data and clock pulses. So we were able to compare any measured response at output terminals with simulator prediction at the end of each clock period.

Any measurement included the setting of the correlator and accumulator in the predetermined initial state. The simplest way to set TD array in predetermined state is to send DUMP pulse. It sets all TD cells in the state of "0" (as it was described above) and allows us to initialize the simulator. However the TD array can be set also in any specific state by sending, for example, DAT1 and CLOCK pulses and by monitoring ACARRYO terminal.

The ultimate test pattern was about 500 clock periods long and involved all eight possible combinations of incoming data and CODE pulses. At the end of this pattern the DUMP pulse was used to read the states of the TD cells to the six output channels and those values were in turn compared to the ones calculated by the simulator.

The experimental results are presented in Table I.

Table I.
Experimental testing: chip CORR05 @ kl442a

Bias name	Working point, mV	Margins, mV
BTR	2.168	+/- 0.299
BXOR	1.769	+/- 0.520
BCL1	1.906	+/- 0.120
BK	2.263	+/- 0.200
BCL2	2.324	+/- 0.429
BFR	2.000	+/- 0.425

B. High-frequency

Fig. 5 shows the experimental setup for HF testing. HF testing is in progress.

IV. Synchronization demo experiment

As it was mentioned above the PRBS generators located on Transmitter and Receiver chips should be properly synchronized in order to provide a correct operation of whole MODEM system. Such self-synchronization can be easily reached by the sending of 63 1's encoded by Transmitter.

Figure 6 shows the block diagram of the proposed synchronization experiment. The Code Generator is a 6-bit PRBS generator described in [7]. The other parts of this diagram are discussed above. So let us concentrate on the feedback loop that includes SET/RESET block and NOT gate. This loop permits finding appropriate chip timing.

The SET/RESET block is mainly a RSN cell (Set/Reset Non-destructive read). The SYNCHRONIZE signal sets its state to 0. As a result the READ pulse will write 1 into NOT gate keeping the state of RSN cell unchanged. The new state of NOT gate causes the skipping of one clock pulse and changes correspondingly the phase of the code sequence produced by PRBS generator relative to the incoming synchronizing sequence. If the content of the accumulator does not exceed the threshold value after 63 clock pulses, another clock pulse will be skipped during the next cycle of 63-clock pulses.

If the threshold value is reached, the asynchronous carry pulse CARRY OUT generated by MSB TD cell will switch the state of SET/RESET block to the 1 state. It means that the synchronization has been reached and the feedback loop does not affect anymore the propagation of clock pulses.

It is important to note that the frequency divider should be attached after NOT gate. In this case the DUMP pulse is generated in time, taking into account the skipped clock pulse.

The THRESH block is used to set the threshold value of an accumulator. It consists of array of TN cells and their contents can be written easily using SET input just before the experiment. Because of inevitable errors of data transmission and some errors during the digital data processing exact numbers 0 and 63 are not reachable. So some threshold values should be established. Usually the threshold for single "one" is set to be 48 (75% of 63). So the content of THRESH block should be 16.

V. Design of PRBS generator

The block-diagram of a 6-bit PRBS generator [7] is shown in Fig. 7. It consists of 5 shift registers, a NOT gate as a first stage of the shift register chain and XOR gate. It also includes the RESET switch attached after the NOT gate in the chain. It is used to set the generator to the well-defined initial state. When the switch is "off", zeroes will be clocked into the shift registers. Once the switch is turned on, the feedback will send the specified code through the shift registers.

Fig.8 shows the possible implementation of PRBS generator. The upper row of D cells is used to store the generated code, clock pulses control the passage of the code through the upper row (from left to right). The lower row of D cells is implemented to avoid a long asynchronous propagation of a content of the rightmost D cell in the upper row to NOT cell (from right to left). Simulations show that this circuit could operate only up to 6 GHz because the combination of XOR and NOT cells requires a lot of time to

process data. However the maximum operating frequency and margins could be increased by implementation of circuit shown in Fig. 9.

It is easy to prove that 63-bit codes are equivalent for both PRBS generators. Let us summarize in Table II all possible states of XOR and NOT cells, where A is XOR input from rightmost D cell; B is a state of the NOT cell; C is output of the NOT cell. One can see that TN and NOT cells as shown in Fig.9 could replace the combination of XOR and NOT cells.

Table II.

A	1	1	0	0
B	0	1	0	1
C	1	0	1	0
Next B	0	1	1	0

Fig.10 shows the implementation of the digital RESET switch. The output of TN cell is connected to the upper row formed by D cells through RSN cell. The state of RSN cell is controlled by applying NRZ signal through input driver (described above). The CARRY output of TN cell clocks the D cell where the P pulse is stored. It permits to synchronize the applied NRZ signal with particular state of TN cell.

Two chips were designed to test the operation of PRBS generator at low (Fig.11) and high (Fig.12) frequencies. Testing is in progress.

VI. Auxiliary circuitry

A. The THRESH block and its interface to accumulator

The THRESH block consists of 4 TN cells connected in series (Fig.13). The required contents can be written in by using SET input through input driver. The THRESH value is read out by DUMP pulse generated by a frequency divider. Clock pulses from the accumulator control the propagation of DUMP pulse from left to right through D cells. As a result the readout of THRESH value is synchronized to clock pulses in the accumulator.

B. The frequency divider

The frequency divider (FD) described in [12] was used to design the full-size synchronization demo experiment. Note that the period of DUMP pulses should be 63 to match the length of an accumulator. Because the period of described FD is 64 we connected its output and input terminals to reduce the period by one clock period. However, the first DUMP pulse requires 64 clock pulses.

C. An extra RSN cell to cancel propagation of DUMP pulses after synchronization

There is an extra RSN cell (located just below SET/RESET block) to avoid the propagation of DUMP pulse along the THRESH block after synchronization. The SYNCHRONIZE signal sets its state to 0. As a result the DUMP pulse passes the RSN

cell to read out the contents of the THRESH block. If the threshold value is reached, the asynchronous carry pulse CARRY OUT generated by MSB TD cell will switch the state of the extra RSN cell to the 1 state. It means that the synchronization has been reached and DUMP pulses do not pass the RSN cell to read out the THRESH value.

D. An extra NOT cell to eliminate an auxiliary CARRY OUT pulse

Because of particular design of TD cell, its state after DUMP pulse is "1" in contrast to required "0". So we used the second delayed DUMP pulse to set TD array of the accumulator into "0" state (see Chapter II for details). However in this case we need to eliminate the auxiliary CARRY OUT pulse. To do that we put an extra NOT cell located just behind the rightmost TD cell. The NOT cell is feed by DUMP pulse and clocked by CARRY OUT pulse. In this case the true CARRY OUT pulse without DUMP pulse propagates through feedback loop to switch the state of SET/RESET block to 1 state. However an auxiliary CARRY OUT pulses are wiped out by DUMP pulses.

VII. Testing of chips CORR12/CORR13

Designs of chips CORR10, CORR11, CORR12, CORR13 are similar to CORR08, CORR09, CORR07, CORR06 correspondingly except minor corrections of their layouts.

A. Chip CORR12

Our testing procedure was based on continual comparison of experimental data with the predictions of a computer simulator that includes mathematical description of all cells and their responses on data and clock pulses. So we were able to compare any measured response at output terminals with simulator prediction at the end of each clock period.

The chip was tested according to the procedure described in Appendix A.

We proved the operability of the following parts:

THRESH block by means of CARRY OUT pulse from MSB TD;

PRG by means of PRG monitor and counting pulses from PRG in an accumulator (data pulses are off);

SET/RESET block and clock skip regime;

Accumulator and frequency divider by counting of pure input data (PRG is off).

However the design failed to demonstrate the operation of the whole system. We believe the reason is that the bias current distribution along the chip affected the operability of its parts because all measured chips were extremely sensitive to flux trapping - chips needed to be "defluxed" tens times to get any reasonable response.

Four copies of chip CORR12 were tested. Two of them did not work at all. Two were partly operable. The testing results for the best one are summarized in Table III.

Table III.

Experimental testing: chip CORR12 @ kl578

Bias name	Working point, mV
BPRG	2.5

BCL1	2.1
BCL2	2.1
BK	1.9
BIN1	1.9
BIN2	2.3

B. Chip CORR13

The chip CORR13 includes two PRGs (upper and lower designs) that differ only in biasing schemes. The upper PRG has two bias lines: one is for PRG itself (BPRG) and another one is for dc/SFQ and SFQ/dc converters (BFR). The design of he lower PRG allows one to bias parts of PRG separately (BPRG1-BPRG4). The bias voltages are summarized in Table IV.

The both PRGs were successfully tested at low frequency. The experimental data coincided with the predictions of a computer simulator. Fig.17 is to confirm the correct operation of the PRG.

Table IV shows that the PRGs located on the same chip required different biasing. For example, the bias BFR to feed dc/SFQ and SFQ/dc converters are quite different in case of upper and lower designs. It could be explain only by variation of circuit parameters due to fabrication because the upper and lower biased parts are identical.

One can see also that all BPRG bias voltages for lower design is similar to BPRG for upper design except BPRG3 that is responsible for propagation of clock pulses inside the generator. This variation of bias voltage could be explained either by some fabrication defect or by non-ideal timing of the circuitry. In the second case it means that PRG requires "slower" propagation of clock pulses.

Table IV.

Experimental testing: chip CORR13 @ kl578

Bias name	Working point, mV	Margins, mV
Upper design		
BPRG	2.399	+/- 0.300
BFR	1.974	+/- 0.201
Lower design		
BPRG1	2.375	+/- 0.188
BPRG2	2.312	+/- 0.352
BPRG3	1.898	+/- 0.538
BPRG4	2.325	+/- 0.225
BFR	2.389	+/- 0.475

VIII. Conclusion

We have designed and experimentally tested 2-bit correlator and 6-bit accumulator for spread spectrum MODEM based on SFQ technology. The module style of the accumulator permits an easy increase of its length.

We have also designed a SFQ digital circuit to synchronize the local receiver's code generator with incoming synchronization sequence. This makes a receiver ready to demodulate outside coded stream of data.

Thirteen different chips were designed and submitted for fabrication, including the designs of full-size synchronization experiment for low (Fig. 14) and high (Fig.15) frequency testing. All designs were optimized to operate at frequencies up to 10 GHz.

Appendix A.

Testing procedure for design CORR08

1. All inputs channels CLOCK, DATA, THRESH_SET, SET/RESET_SET, PRG_SET, READOUT are shown in Fig. 16.
   Bias power lines BIN, BCL1, BCL2, BK, BPRG. The nominal voltage is 2.6 mV.

2. Apply CLOCK and READOUT pulses.
   All output drivers give 1s. OK. Each TD cells after DUMP pulse (generated internally) is in 0 state, which sets all output drivers into 1 state because the read out of TD cells is inverted.

   Not all output drivers give 1s.
   a) Probably, PRG is on. To turn PRG off, apply a single strobe to PRG_SET. The duration of the strobe should be long enough, say 10-15 clock periods.
   b) Probably, SET/RESET block is turned on and some number is written in THRESH block. To turn SET/RESET block off, apply several DATA (1s) pulses to get CARRY OUT pulse from MSB TD cell. Turn DATA pulses off.

3. Keep CLOCK and READOUT on.
   Turn SET/RESET block on, by applying a single strobe to SET/RESET_SET. The outputs provide an information about a number written in THRESH block.

   One can apply multiple strobes to THRESH_SET to modify a number written in the THRESH block. Be aware that you modify a number written in the THRESH block from right to left (see Fig. 13), from TN cell located over the 6^{th} slice of accumulator to TN cell over the 3^{rd} slice. For example, a single strobe modifies the state of 6^{th} TN cell and maybe 5^{th} TN cell if there is a carry pulse from 6^{th} cell to 5^{th} one.

   Note that a number written in the THRESH block affects the accumulator starting the 3^{rd} slice. So the possible ripple of the 1^{st} and 2^{nd} outputs can not be explained by a number written in the THRESH block.

   Be aware also that the first CARRY OUT pulse from MSB TD cell turns SET/RESET block off. So some additional strobes to set SET/RESET block should be applied if it is necessary.

Set the required threshold value.

Do not forget to apply some DATA (1s) pulses to turn SET/RESET block off, if you do not plane using of the THRESH block.

4. Keep CLOCK and READOUT on.
   Add DATA (1s) pulses.
   All outputs give 0s. OK. It means that 63 data pulses were counted correctly, the state of the accumulator is 63 and the corresponding inverted output is "all 0s"

5. Keep CLOCK and READOUT on.
   Turn DATA off and wait until all outputs give 1s.
   Turn PRG on by applying a single strobe to PRG_SET.
   One can expect to see a stable output. The accumulator just counts a number of 1s in PRG sequence.

6. Keep CLOCK, READOUT and PRG on.
   Turn DATA (1s) on.
   The accumulator counts a number of 0s in PRG sequence. One can expect to see a stable output.

7. Keep CLOCK, READOUT, PRG and DATA (1s) on.
   Apply a single strobe to SET/RESET_SET to turn SET/RESET block on. The accumulator gives a sum of number of 0s in PRG sequence and the threshold value.

8. Keep CLOCK, READOUT, PRG and DATA on.
   Turn DATA off.
   Apply a single strobe to SET/RESET_SET. The accumulator gives a sum of a number of 1s in PRG sequence and the threshold value.

9. Keep CLOCK, READOUT and PRG on.
   Turn SET/RESET block on by applying a single strobe to SET/RESET_SET.
   Apply coded DATA to run the synchronization demo experiment.

10. Auxiliary experiments.
    One can
    a) count coded DATA without PRG to check that DATA are coded correctly;
    b) check that turning of SET/RESET block on does not affect counting of plain PRG sequence and plain DATA (1s).

References

[1] Robert C.Dixon, *Spread Spectrum Systems with Commercial Applications*, 3rd edition, Wiley, 1994.

[2] K. Likharev and V. Semenov, "RSFQ logic/memory family", *IEEE Trans. Appl. Supercond.*, vol.1, p. 3, March 1991.
[3] O. A. Mukhanov, V.K.Semenov, I.V. Vernik, A.M. Kadin, T.V. Filippov, D. Gupta, D.K. Brock, I. Rochwarger, Yu.A. Polyakov, ", "High-resolution ADC operation up to 19.6 GHz clock frequency", *Supercond. Sci. Technol.*, vol. 14, p. 1065, 2001.
[4] P.D. Dresselhaus, E.J. Dean, A.H. Worsham, J.X. Przybysz, S.V. Polonsky, "Modulation and demodulation of 2 GHz pseudo random binary sequence using SFQ digital circuits", *IEEE Trans. Appl. Supercond.*, vol. 9, p. 3585, June 1999.
[5] J. X. Przybysz, J.D. McCambridge, P.D. Dresselhaus, A.H. Worsham, E.J. Dean, J.P.Sage, T.J. Weir, "Dewar-to-dewar data transfer at GHz rates", *IEEE Trans. Appl. Supercond.*, vol. 9, p. 2981, June 1999.
[6] J.X. Przybysz, E.J.Dean, P.D. Dresselhaus, D.L. Miller, A.H. Worsham, S.V. Polonsky, "Spread spectrum data transfer from dewar to dewar at 2 Gigachips per second", *IEEE Trans. Appl. Supercond.*, vol. 11, p. 982, March 2001.
[7] E.J. Dean, P.D. Dresselhaus, J.X. Przybysz, A.H. Miklich, A.H. Worsham, S.V. Polonsky, "Bit Error Rate Measurements for GHz Code Generator Circuits", *IEEE Trans. Appl. Supercond.*, vol. 9, p. 3598, June 1999.
[8] T.V. Filippov, S.V. Pflyuk, V.K. Semenov, E.B. Wikborg, "Encoders and decimation filters for superconductor oversampling ADCs", *IEEE Trans. Appl. Supercond.*, vol. 11, p. 545, March 2001.
[9] HYPRES, Inc., 175 Clearbrook Rd., Elmsford, NY 10523, phone 914-592-1190.
[10] J. X. Przybysz, D.L. Miller, S.S. Martinet, J. Kang, A.H. Worsham, M.L. Farich, "Interface circuits for chip-to-chip data transfer at GHz rates", *IEEE Trans. Appl. Supercond.*, vol. 7, p. 2657, June 1997.
[11] D.Y. Zinoviev, Y.A. Polyakov, "Octopux: an advanced automated setup for testing superconductor circuits", *IEEE Trans. Appl. Supercond.*, vol. 7, p. 3240, June 1997.
[12] J.C.Lin, V.K.Semenov, K.K.Likharev, "Design of SFQ-Counting Analog-to-Digital Converter", *IEEE Trans. Appl. Supercond.*, vol.5, p.2252, June 1995.

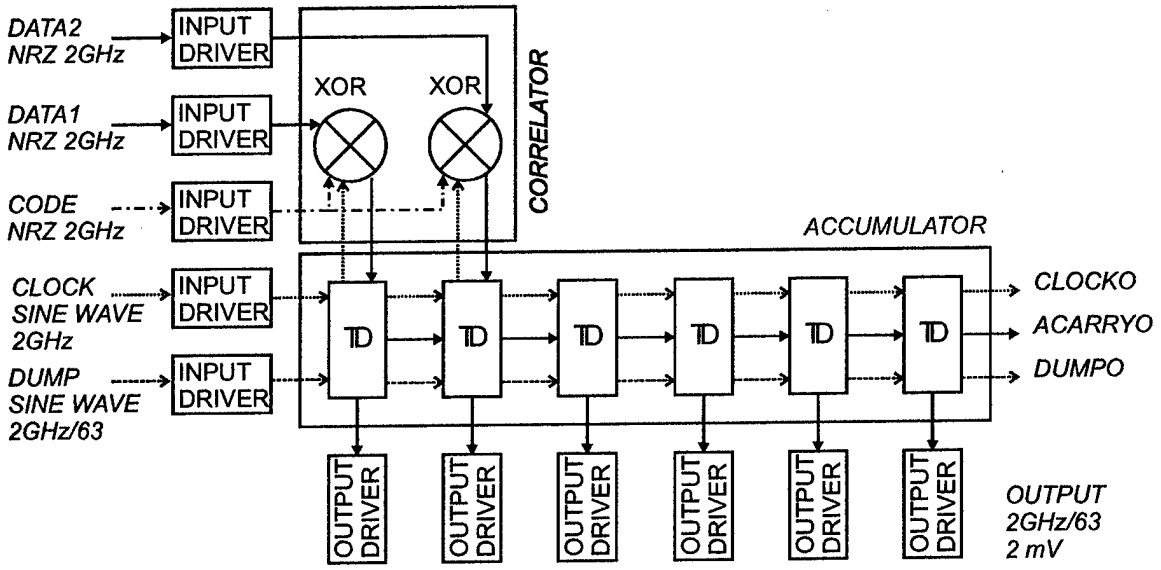


Fig.1. Block diagram of a 2-input correlator and an accumulator.

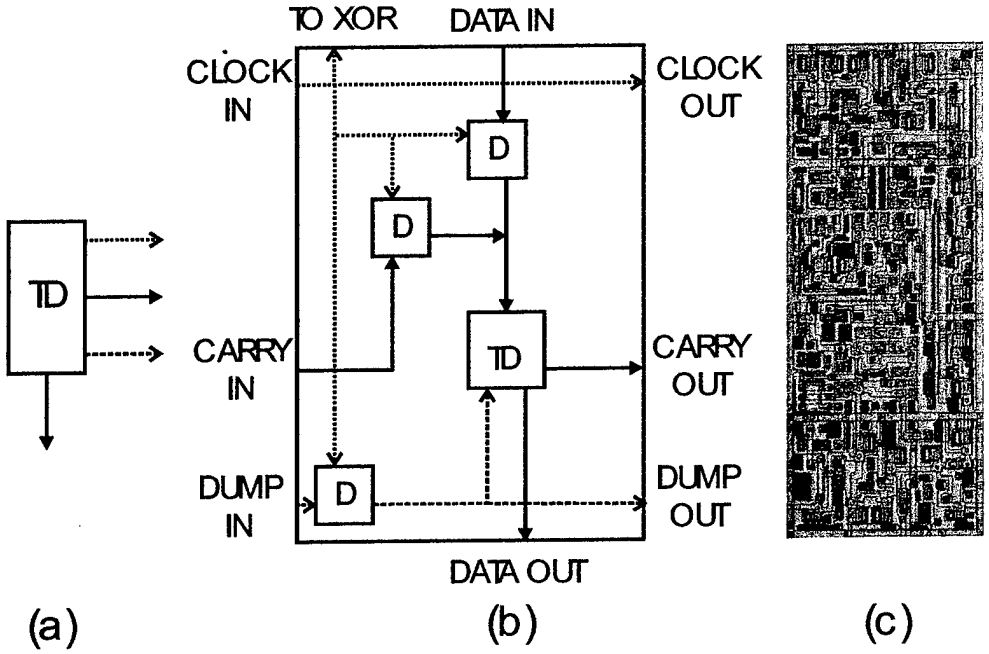


Fig.2. Notation (a), block diagram (b) and microphotograph (c) of one slice of an accumulator. The size of TD module is 200um x 523um, it consists of 58 Josephson junctions and the effective size per junction is about 42um x 42um.

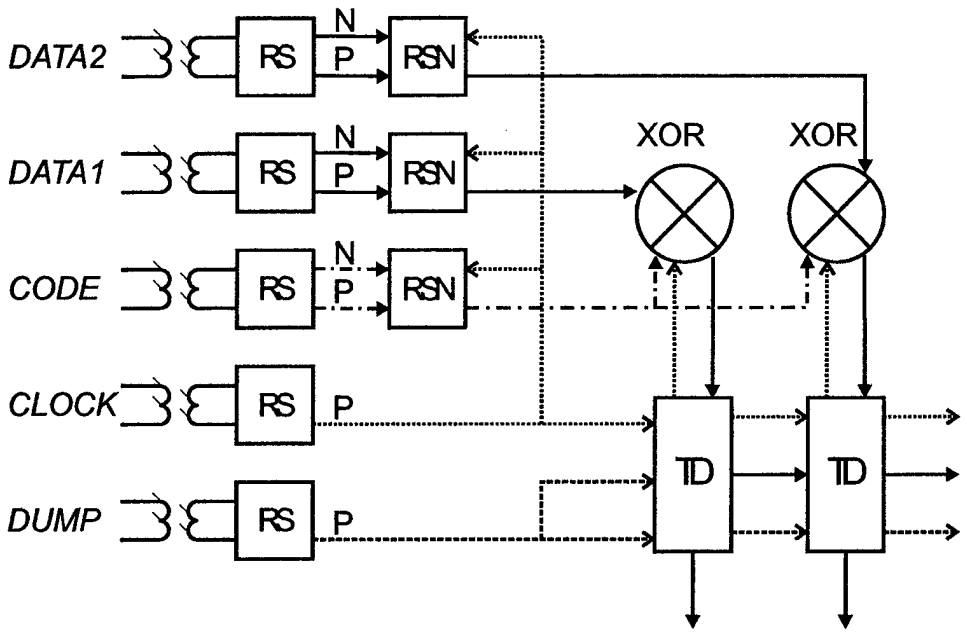
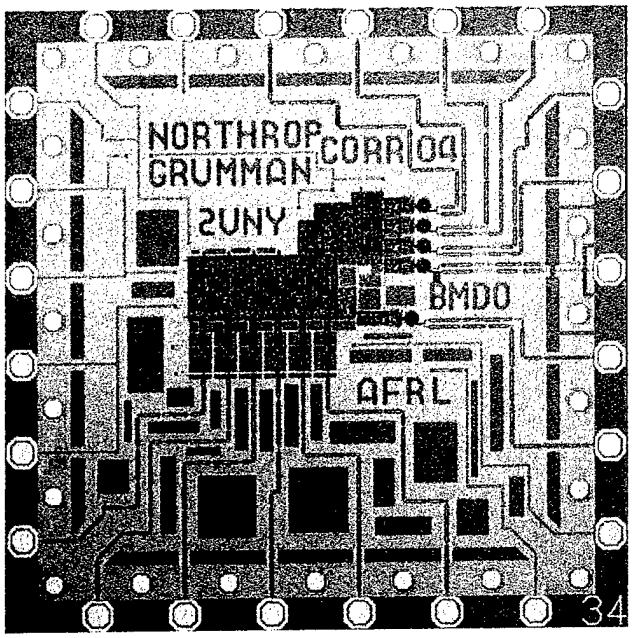
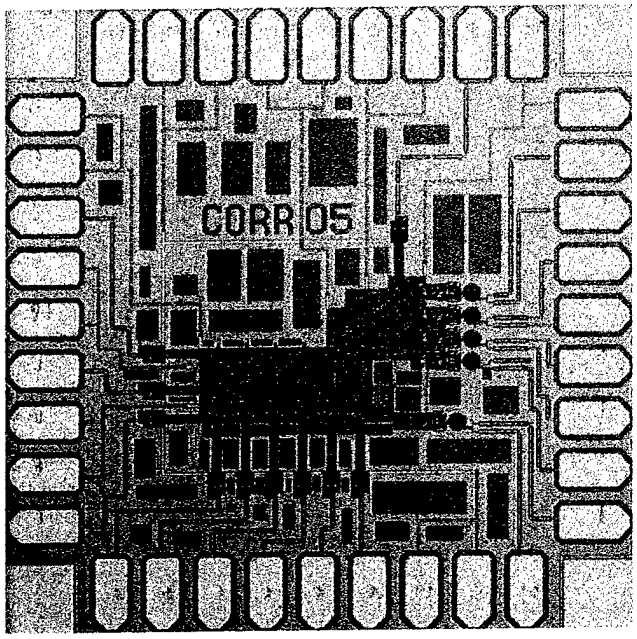


Fig.3. Block diagram of a front-end interface (see text for details).



(a)



(b)

Fig.4 Layouts of chips CORR04 (a) and CORR05 (b) for high- and low-frequency testing.

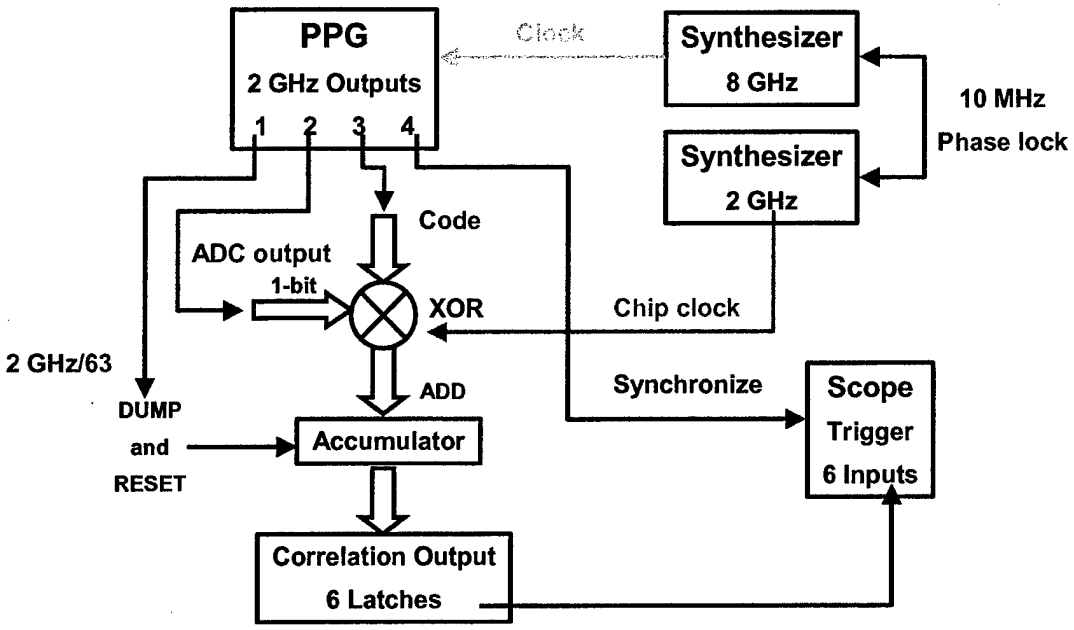


Figure 5. Operation of the digital correlator at 2 GHz was verified using a high-speed pattern generator to simulate inputs from a code generator and an analog to digital converter. For strong signals, the correlator outputs should be 31 or 32 before synchronization. After synch, the correlator should output 63 for Data_1 and 0 for Data_0.

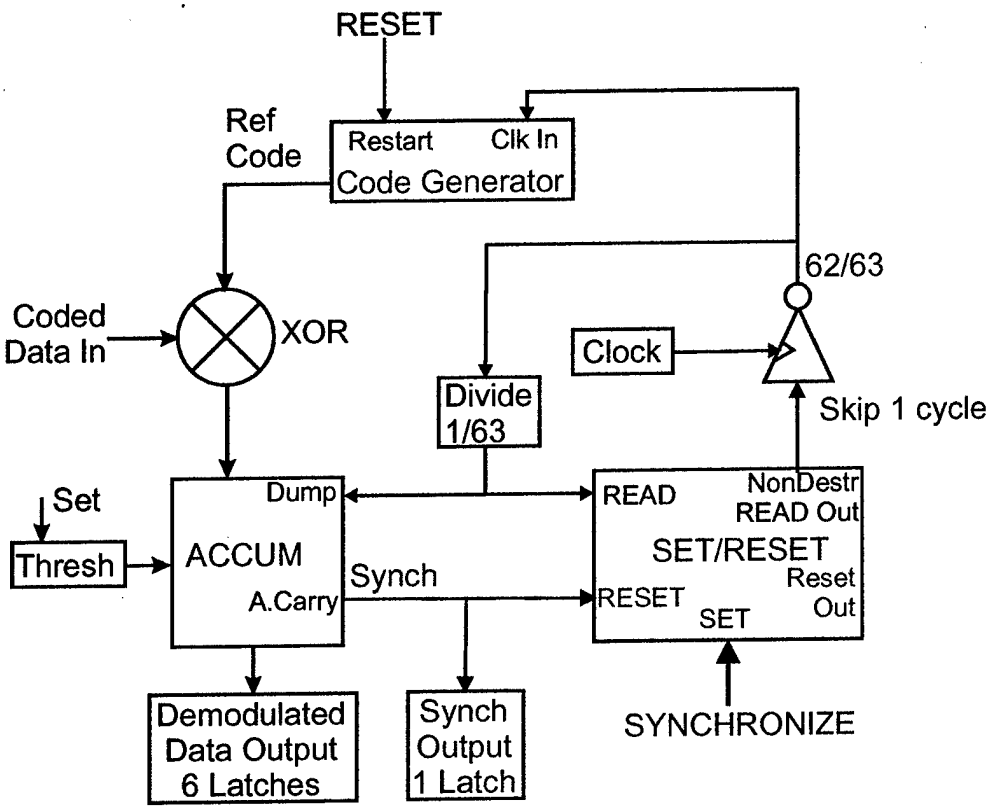


Fig.6. Block diagram of synchronization experiment (see text for details).

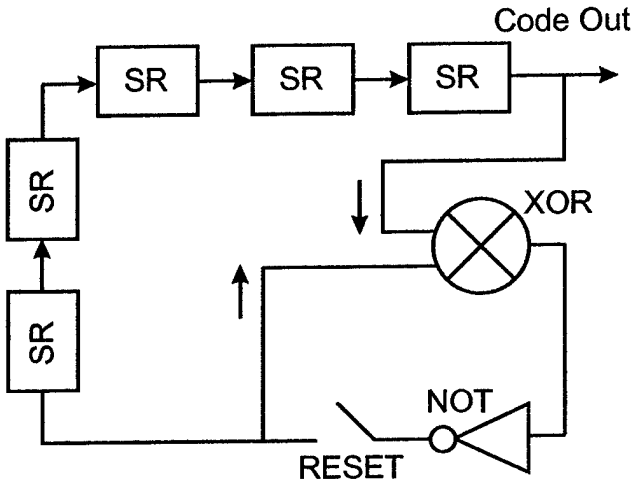


Fig.7 The six-bit code generator diagram (SR = shift register) [7].

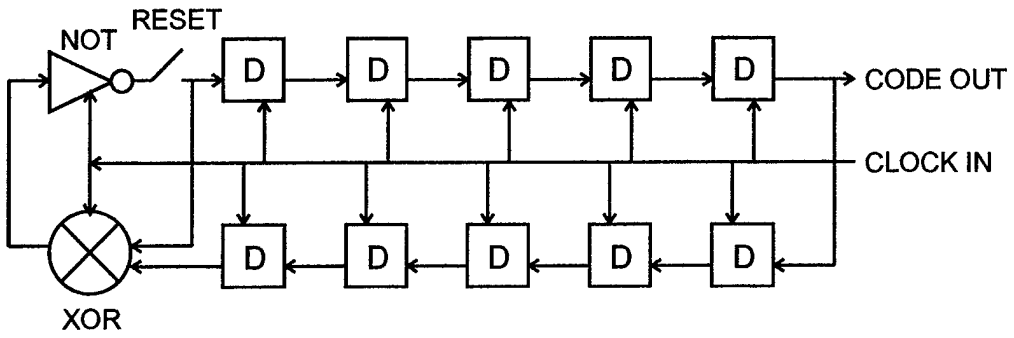


Fig. 8. Block diagram of PRBS generator based on XOR and NOT cells.

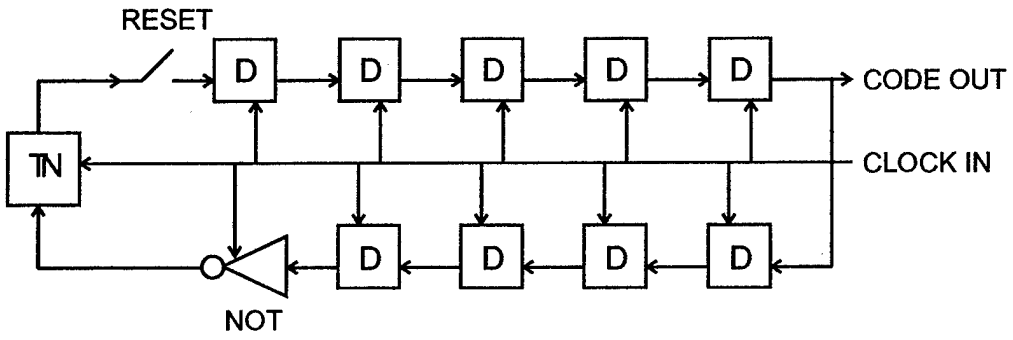


Fig. 9. Block diagram of PRBS generator based on TN and NOT cells.

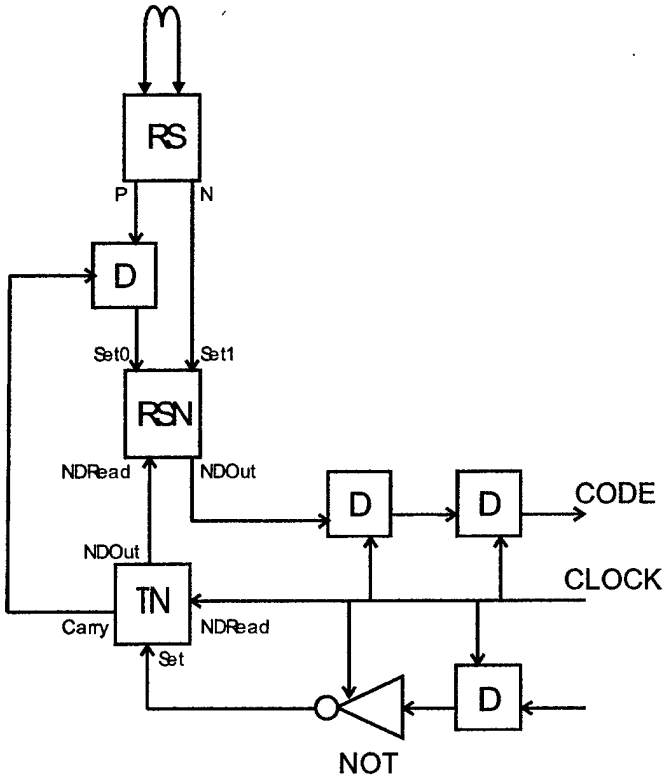


Fig. 10. Block diagram of digital switch RESET (see text for details).

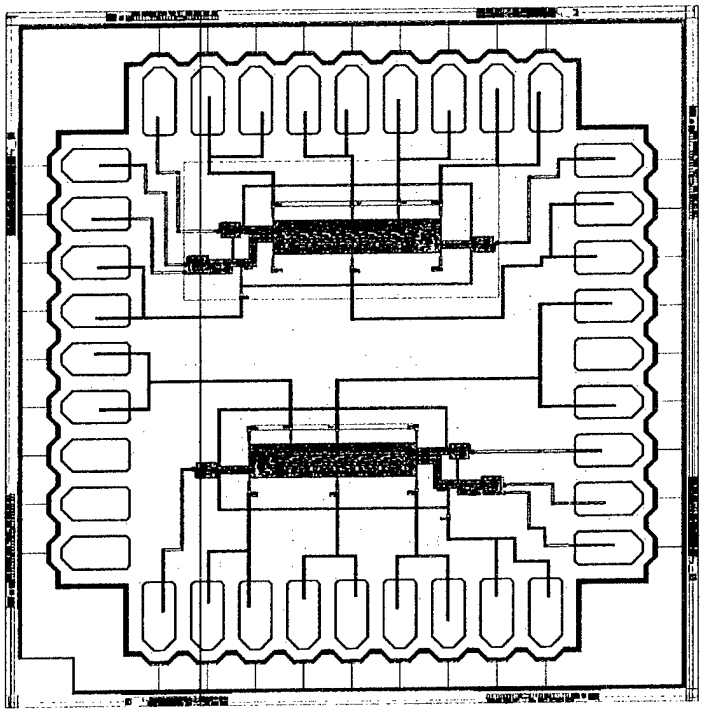


Fig. 11 Layout of PRBS generator (chip corr06 for low frequency testing).

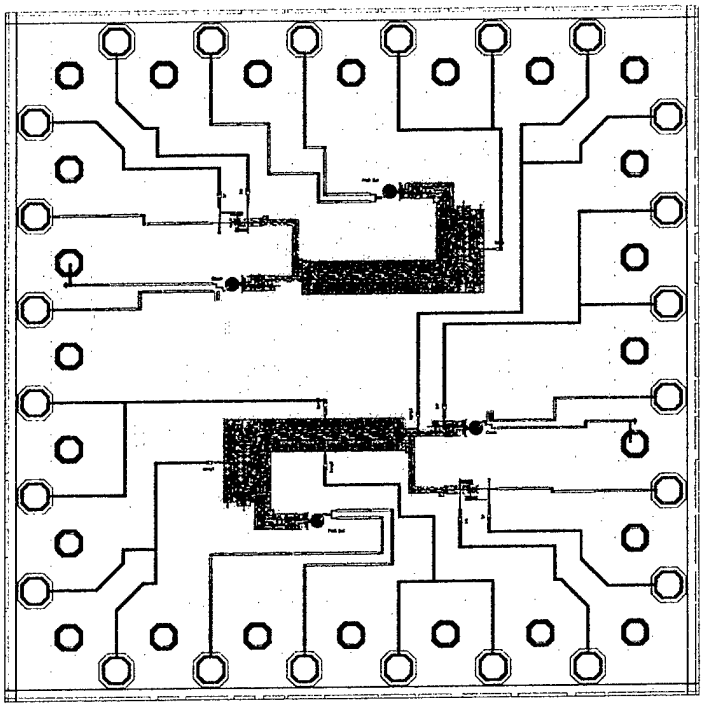


Fig. 12 Layout of PRBS generator (chip corr09 for high frequency testing).

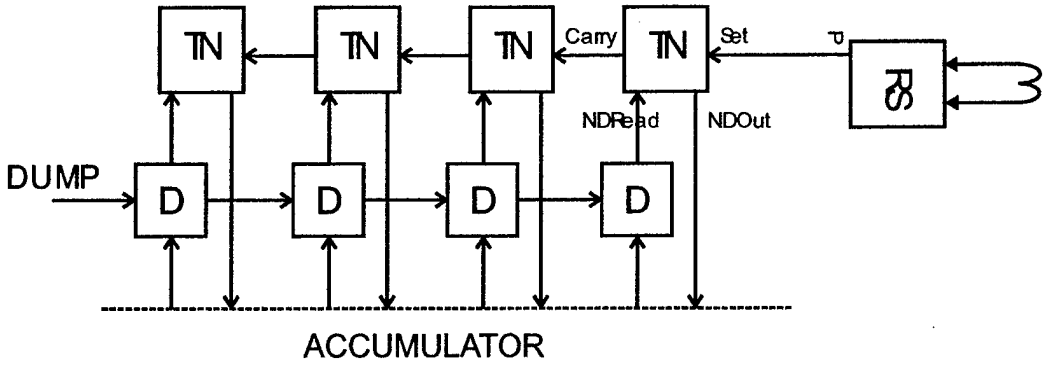


Fig. 13 Block diagram of THRESH block and its interface to an accumulator.

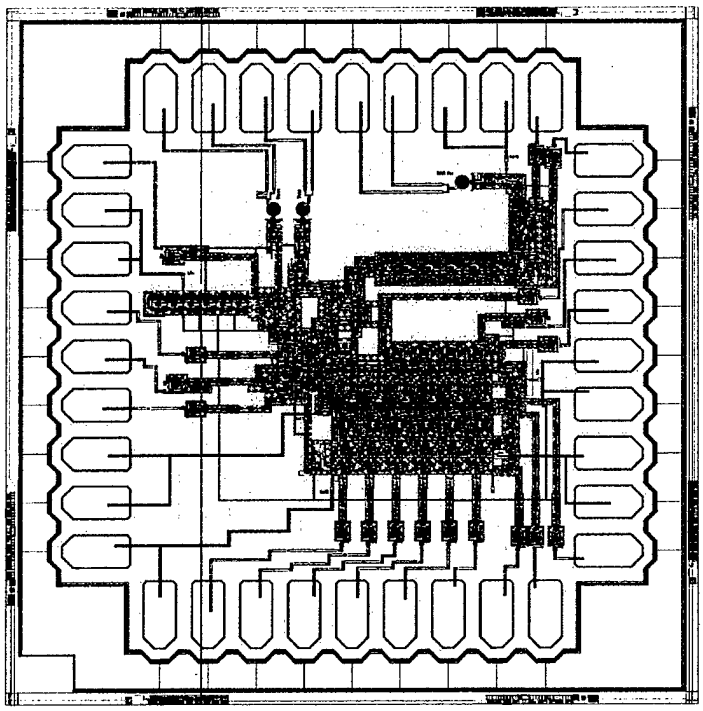


Fig.14. Layout of full-size synchronization demo experiment (chip corr07 for low frequency testing).

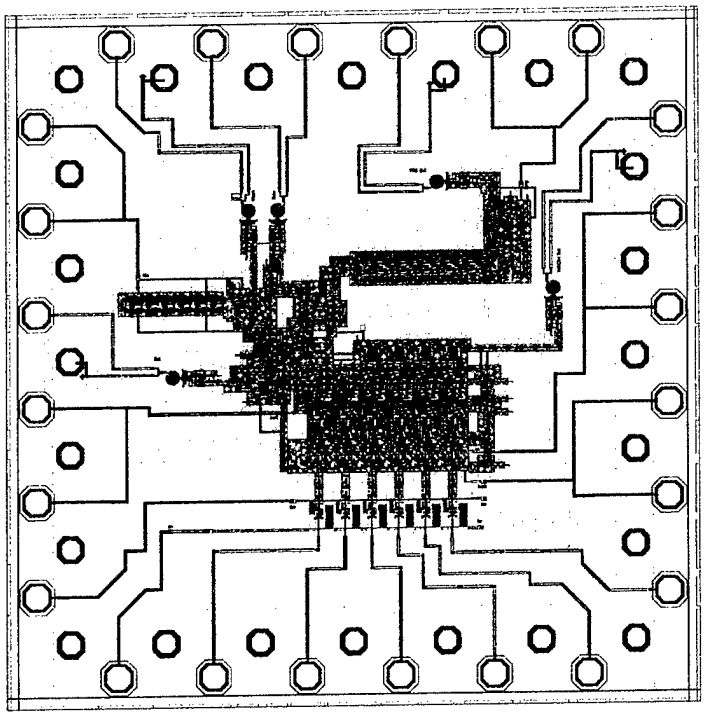


Fig. 15. Layout of full-size synchronization demo experiment (chip corr08 for high frequency testing).

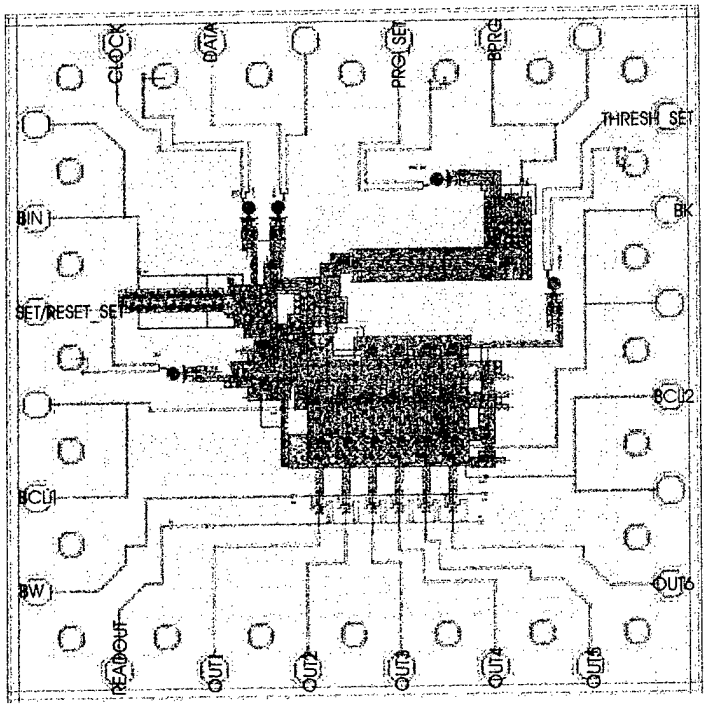


Fig. 16. Layout of chip corr08: all contact pads are labeled as in Appendix A.

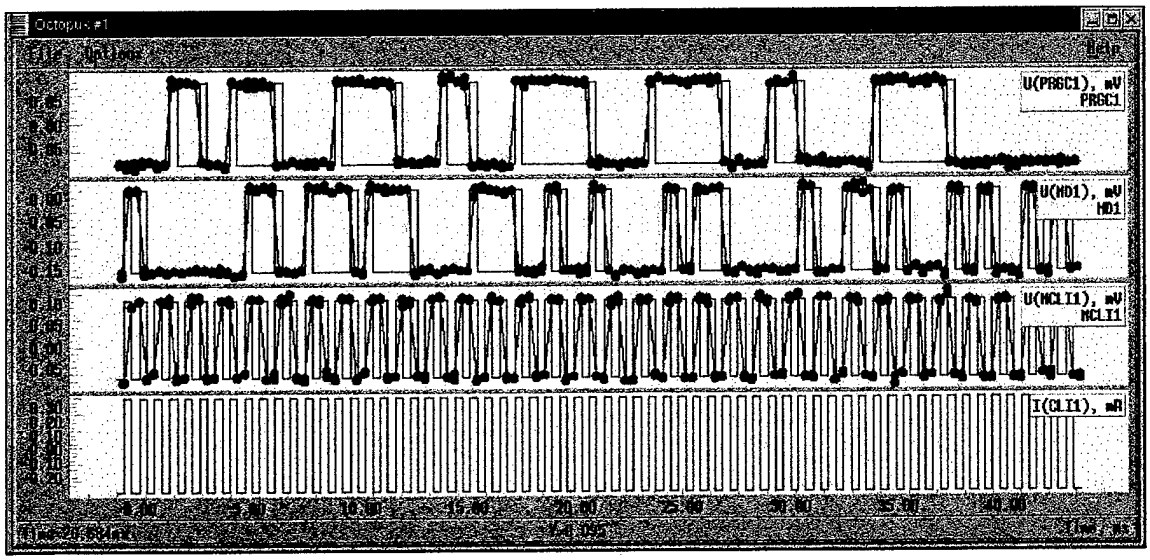


Fig. 17. Experimental testing of chip CORR13. MD1 is output monitor of PRG, PRGC1 is a monitor of carry pulses from digital switch RESET (see Fig.10 for details)

V. Discussion

This contract built upon the success of previous AFRL contracts to develop digital correlators and rapid synchronizers for spread spectrum modems based on superconductive electronics. The prior work had demonstrated low power chips that operated at 2 GHz (Figure V.1) and performed all important spread spectrum functions (Figure V.2). This final contract demonstrated that the correlation and rapid synchronization could also be performed with superconductive digital electronics.

This series of programs was marvelously successful from a scientific point of view, advancing the knowledge and art of high speed digital electronics. Josephson shift registers worked at 3.2 GHz in 1989, solving problems that were yet undreamed of by CMOS designers. This was 200 times faster than the 16-MHz CPUs used in personal computers at that time.

AFRL began a series of contracts in superconductive electronics with the Terahertz Technology program in 1986. Radar, communications, and other sensors were included in that program. By 1991, the AFRL programs were focused on spread spectrum communications. Both analog and digital circuits were included. In the end, digital circuits based on Rapid Single Flux Quantum logic made the most advanced demonstrations of spread spectrum communications.

The most rapid advances in SCE design and demonstration came during the period of the University Research Initiative in Low Temperature Superconductor Digital Electronics, 1991- 1997. That research focused on niobium based superconductors operating at 4.2 Kelvin. There was a hope that High Temperature Superconductors (HTS) would make rapid progress, so that the results could be transitioned to HTS for easier cooling. But HTS materials were too complex; the highest levels of integration never exceeded 50 junctions.

Cryocoolers for 4.2-Kelvin operation are expensive. Small coolers (~200 mW lift) cost $16,000, while larger coolers (~3 W lift) cost $35,000. These are small additional costs, compared to the $300,000,000 that it costs to launch a satellite. But coolers set a lower bound on the set of applications where SCE can compete. The vast majority of electronics applications cost less than $16,000. SCE does not sell to those markets, which are a huge economic engine driving the advance of semiconductor chips.

Support for superconductive electronics has slowed in recent years as the momentum of commercial electronics provided ever greater tool sets to CMOS manufacturing. The IBM CMOS foundry that opened in 2002 cost $2.5B. That 90-nm facility is now turning out G5 PowerPC chips, while Josephson foundries still use 1,250-nm lithography. CMOS makes up for a lack of speed by employing more transistors in the same chip area.

Superconductive digital still wins battles for pure speed. The highest speed semiconductor circuits are InP HBT asynchronous dividers, operating at 150 GHz. SCE dividers operate at 780 GHz. For applications that depend on speed, SCE can provide more performance than semiconductors.

There are applications where pure speed makes the difference. Transformational communications is today's high speed king. Free-space lasers can move hundreds of gigabits per second between satellites, but a cloudy day prevents laser data from reaching ground forces. RF links, based on Josephson digital circuits, operating at 40 GHz clock speeds is the next frontier for SCE communications (Figure V.3).

The accomplishments of the AFRL programs to develop SCE for spread spectrum communications provide an excellent basis for the future development of Gigabit modems for transformational communications.

Low Power Chips Operated at 2 GHz

- **Designed, Fabricated and Tested Spread Spectrum Code Generator and Modulator at 2 GHz**
  - **High Speed data I/O**
  - **Data Modulation**
  - **Data Demodulation**
  - **Time Forward and Reverse Codes**
  - **Gold Codes**
  - **Base Band Demonstration of Spread Spectrum Communications**

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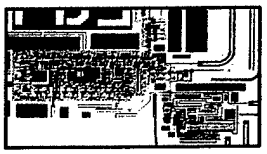
Figure V.1. Josephson digital circuits operated at 2 GHz while dissipating microwatts. No other technology can provide these features simultaneously.

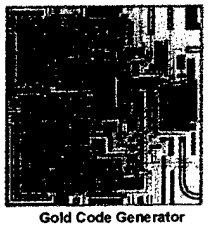
JJ Chips Demonstrated Spread Spectrum Modem Functions

Code Generator



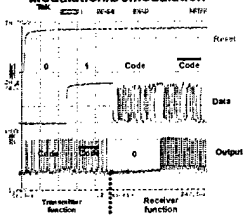
Spread Spectrum Modulators and Demodulators at 2GHz

Bit Error Rates < 10^{-12}



Gold Code Generator

Modulation/Demodulation



Gold Code Data at 2 GHz

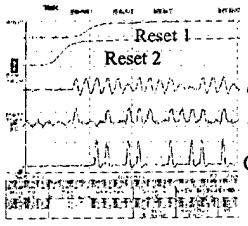


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Figure V.2. Superconductive electronics demonstrated all these spread spectrum functions at GHz speed.

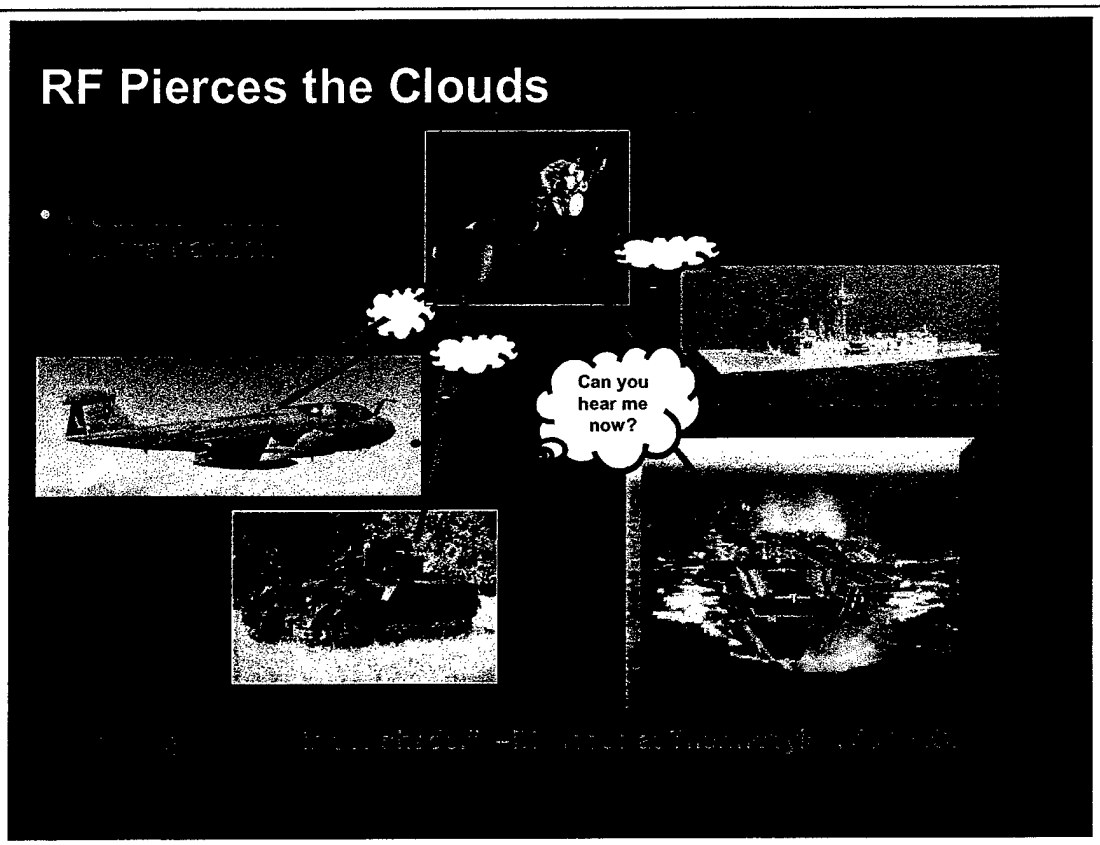

Figure V.3. Transformational communication systems need RF links to communicate through the clouds to surface forces. Lasers can transport 40 Gbps between satellites. Superconductive digital circuits can modulate and demodulate 4 Gbps data as QPSK signals onto a Ka-band carrier.