A PC-BASED TIME INTERVAL COUNTER WITH 200 PS RESOLUTION

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Abstract

This paper describes the design and technical features of the precise time-interval counters realized as PC computer boards with ISA, PCI, and PXI interfaces. Thanks to the use of a specialized, interpolating counter chip fabricated in CMOS FPGA technology, the 200 ps resolution (1 LSB - Least Significant Bit) was achieved in single-shot measurements of time intervals within the range from 0 to 43 s. The standard measurement uncertainty is below 1 LSB as a result of automatic correction of nonlinearity of two interpolators contained in the FPGA counter chip. The counter board can also be used for frequency measurement up to 1.1 GHz. The dedicated software operating in a Windows environment provides comprehensive control, diagnostics, and statistical processing of the measured data.

INTRODUCTION

Precise time and time interval measurements are crucial in many areas of research and industry. In timekeeping systems, navigation systems, and laser rangefinders, the time counters are usually controlled by a computer or microcontroller. When we designed and tested a precise and economical interpolation time counter with 200 ps resolution in a single CMOS FPGA (Complementary-Metal-Oxide-Semiconductor Field-Programmable-Gate-Array) device **[1,2]**, as a next step we considered its possible applications and designed three models of precise time counters in the form of PC boards. They differ mainly by the used computer bus interface. The first design, T-2000, was based on the classic ISA interface, and then we designed the counter with the PCI (T-2200) and PXI (T-2200PXI) interface. The latter one can be used in the PXI mainframes (*National Instruments*) for professional applications in research and industry. One model of the PCI counter board (T-2200R) can be driven by an external 10 MHz reference clock (for example, an atomic clock) to achieve high accuracy and long-term stability. The all boards are controlled by a user-friendly software working in the Windows environment and creating a virtual front-panel of the counter on the monitor screen.

In this paper, we describe the electronic design of these counter boards and the respective technical details. We also present the results of tests performed.

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DESIGN

Figure 1 shows the block diagram of the counter board T-2200. The inputs A and B are used for time interval measurements, and their impedance can be selected as 50 Ω or 1 MΩ. The fast comparators (FC) allow one to select the required sensitivity and polarity of the input pulses. The corresponding input threshold levels ranging from -5 V to +5 V can be adjusted manually or automatically by the control software.

The standardized TTL pulses from the comparator outputs are fed to the inputs of the FPGA counter **[2]**. The chip can be used to measure the time intervals with 200 ps resolution within the range from 0 to 43 s, or to measure the frequency of the input pulses up to 150 MHz. An additional fast frequency divider has been used to allow the maximum frequency (at the F input) of 1.1 GHz.

The built-in calibration generator can be used to perform a calibration routine needed for compensation of the input time offset and for identification of two nonlinearity correction vectors related to the precise, tapped delay lines in the FPGA counter **[1, 2, 5]**. The calibration pulses are simultaneously applied to the inputs A and B through the respective relays. The correction vectors are saved in the EEPROM (Electrically Erasable and Programmable Read-Only Memory) device.

The additional inputs EN and SPEN can be used to enable or disable the inputs A and B, respectively. The STOP ENABLE (SPEN) pulse disables the B input by the time equal to its width, after the START input pulse has been accepted. Alternatively, instead of the external SPEN pulse, an internal programmable counter can be utilized to set the required disable time over a range of 20 ns to 167 ms with a step of 20 ns. The polarities of the input pulses and the corresponding threshold levels can be selected by software. To set the threshold voltages at the comparators related to the inputs (A, B, EN, and SPEN), four Digital-to-Analog Converters (DAC) with internal data registers have been utilized.

To stabilize the counter performance over the allowed ambient temperature range, a DLL (Delay-Locked Loop) circuit has been incorporated, which controls the supply voltage of the FPGA device **[6]**. The related digital delay line and the phase detector are contained within the FPGA device, while the loop filter and the supply buffer are located externally on the board.

The counter board has its own quartz reference generator producing fast TTL pulses of a 100 MHz frequency and stability of 5 ppm. In the T-2200R board, this generator has been replaced by a synthesizer chip, which can be driven by the 10 MHz reference oscillator (1 ppm), located on the board, or by a 10 MHz external reference. In the latter case, an atomic clock can be used to greatly improve the long-term stability and accuracy of the counter.

The control of the board is accomplished by a dedicated CPLD (Complex Programmable Logic Device) controller. The standard chip PLX9052 realizes the interface with the computer PCI bus.

Figure 2 shows the external view of the board T-2200. The FPGA counter is located in the center and below is the PCI interface chip. A screen snapshot shown in Figure 3 presents an example of the virtual front panel of the counter.

OPERATION MODES

The counter boards can operate in one of three modes: time interval measurement, frequency measurement, and calibration. In the first mode the time interval can be measured either between two pulses START and STOP applied to the inputs (A and B) or between such pulses appearing consecutively at a single common input (A or B). In the first case, the minimum measured time interval is zero, while in the second case, it is about 7 ns. The latter configuration is also used for measurement of a signal period. By suitable setting of thresholds of the fast comparators, the rise or fall time of the input pulse can also be measured. The measuring range is then limited by the minimal slew rate of the input pulses, which is allowed by the comparators, and is about 500 ns.

For measurements of time intervals, the dual interpolation method is used. The method combines the long range of a simple counting method and high accuracy of the direct time-to-digital conversion. In the FPGA chip, a 32-bit real-time counter driven by a 100 MHz clock has been used to obtain long measurement range (43 s), while two differential digital delay lines allow one to interpolate within one clock period to provide a high single-shot resolution (200 ps). The resolution can still be improved (up to 1 ps) by averaging. The control software allows one to set the sample size and a number of repeated measurements of that sample.

For frequency measurements, two methods are employed. When the frequency exceeds 100 kHz, the basic counting method is used. For this purpose, the timebase counter, implemented in the FPGA device, generates four gates (10.5 ms, 168 ms, 1.3 s, 5.4 s), selectable with the aid of virtual control panel. To improve the measurement accuracy when the frequency is below 100 kHz, the respective period is measured using the dual interpolation method. There are three inputs on the counter board that can be used for frequency measurements. Two of them (A and B) are intended for signals with frequency below 150 MHz, which can be measured directly by the FPGA chip. The sensitivity at each input is then 250 mV (rms). When the frequency exceeds 150 MHz, the measurements are carried out with the aid of a frequency divider chip, which is connected to the F input. This extends the range of measured frequency up to 1.1 GHz and improves the input sensitivity to 22.5 mV (rms).

Two calibration procedures are provided. In the first one, a large preset number (e.g. 100000) of random time intervals (having a uniform probability distribution within the clock period) is generated to identify the integral nonlinearity of both interpolators integrated in the FPGA device. It allows one to calculate two correction vectors, which are stored in the EEPROM memory chip (as a "look-up table") and used for compensation of the linearity error during "normal" measurements. The built-in calibration generator operates asynchronously with regard to the clock and allows one to complete that calibration in about 100 s. The identified characteristics of the interpolators are relatively stable at the typical ambient temperature changes (+20 ± 5 centigrade) and, thus, the calibration routine should be performed only when a greater ambient temperature change has occurred, or may be performed once before the measurement session. When the temperature inside a typical PC case increases after cold start, the used DLL circuit stabilizes the performance of the FPGA device.

The second calibration procedure is much shorter and lasts only about 3 seconds. It allows one to identify the time offset between the inputs A and B, and is carried out at each virtual "turning on" the counter. Both calibrations can be initiated in any time manually or automatically, according to user needs.

EXPERIMENTAL RESULTS

The main timing parameters, such as resolution, measurements range, and accuracy, are determined by the used FPGA time counter **[2,3]**. The standard uncertainty (random error) of the measurement depends mainly on the quantization step or resolution (*LSB*), and the integral nonlinearity of two time-coding differential delay lines contained in the FPGA chip.

The quantization error can be represented by the binomial probability distribution, like in the simple time counters. The error has a zero mean value, but its standard deviation depends on the quantization step (*LSB*). In a simplified model of the interpolating counter, the *maximum* value of the standard deviation can be as high as σ = 0.5 *LSB* = 100 ps. The *average standard deviation* can be calculated as **[8]**

$$\sigma_{av} = \frac{\pi LSB}{8} \cong 0.39 LSB = \text{ 78 ps.}$$

The nonlinearity of the delay lines is compensated with the use of the correction vectors identified during calibration. Figure 4 shows an example of the integral linearity plot for a single delay line, measured with the aid of the diagnostic software (supplied with the counter board). The plot shown in Figure 4a illustrates a "rough" (not corrected) characteristic, while Figure 4b shows the same characteristic after correction. The result is a dramatic lowering of the error due to nonlinearity. The maximum nonlinearity of about 2.6 LSB has been lowered to about 0.13 LSB or 20 times.

The compensation of nonlinearity in both delay lines results in much lower standard uncertainty of the counter board (Figure 5). The maximum value of standard deviation equal to 350 ps before correction has been reduced to about 140 ps (0.7 LSB) after correction. Because the standard uncertainty due to nonlinearity is repetitive within each fraction **Frc** (time interval / clock period) **[7]**, the tests were performed for time intervals within a single clock period. The delays differing by 1 ns were generated with the use of a set of precisely cut coaxial cables.

When the measured time intervals are longer than about 10 ms, the standard uncertainty of the counter becomes more influenced by the short-term error of the reference clock. To determine the standard uncertainty of the two counter boards: T-2200 (with an internal 100 MHz quartz generator) and T-2200R (with an internal 10 MHz quartz generator and a 100 MHz digital synthesizer) within a long measurement range, we measured time intervals generated by the commercial delay generator DG535 (*Stanford Research Systems*). We also measured the test time intervals using two desktop counters: HP53132A (*Hewlett-Packard*) and SR620 (*Stanford Research Systems*). The results are presented in Figure 6.

CONCLUSIONS

The described time counter boards allow precise measurements of long time intervals with picosecond accuracy at a lower price than stand-alone counters of comparable parameters. The natural applications of the counters are advanced systems for time keeping, laser ranging, and navigation. They can also be used in industrial and research laboratories, and in ATE systems. Thanks to the use of programmable devices (FPGA and CPLD), the counter boards can be customized to match user applications.

Summary of Technical Specifications

Time Interval	
Range	0 – 43 s (inputs A and B)
***Resolution - Least Significant Bit* (LSB)**	200 ps for a single measurement 1 ps in averaging mode
Standard uncertainty	< 200 ps without averaging < 200/√(sample_size) ps with averaging
Frequency	
Range	Inputs A and B: from 0.1 Hz to 150 MHz Sensitivity:< 250 mV RMS typ. (0.01 to 100 MHz) Input F: from 100 MHz to 1.1 GHz Sensitivity < -20 dBm (< 22.5 mV RMS)
Inputs A and B	
Impedance	1 MΩ or 50 Ω, software selectable
Input voltage	< ± 5 V
Threshold level	preset by software within the range of -5 V to +5 V with 40 mV resolution or automatic preset
Input F	
Impedance	50 Ω
Internal Timebase	
T-2200	max. ± 5 ppm at + 25 C, ± 25 ppm (0 do + 70 °C);
T-2200R	max. ± 1 ppm at + 25 C

More detailed technical specifications are available at the Web site *www.vigo.com.pl.*

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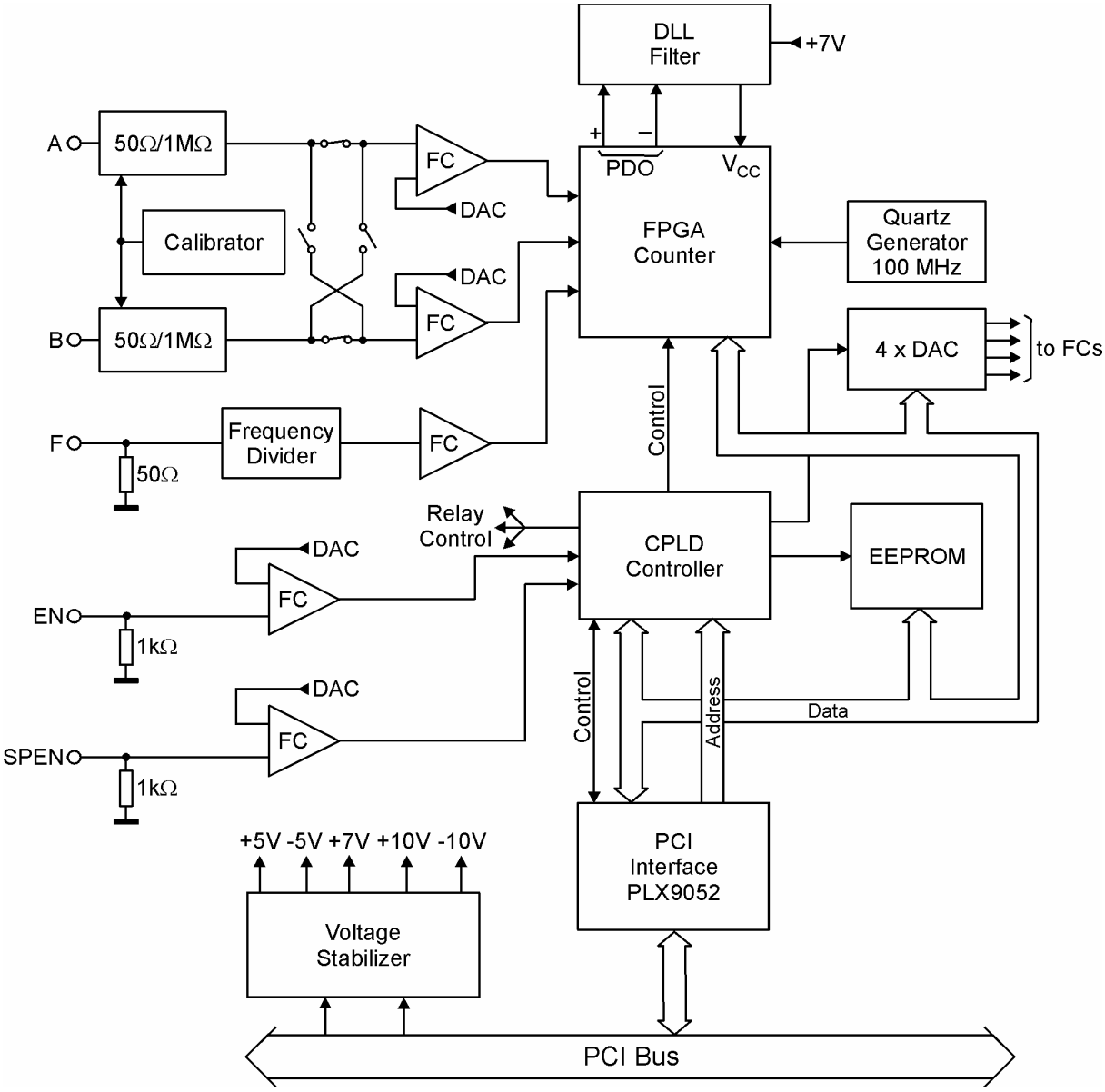


Figure 1. Simplified block diagram of the counter boards T-2200 and T-2200PXI. In the T-2200R board, the internal 100 MHz quartz generator is replaced by a 100 MHz synthesizer chip fed by an internal or external 10 MHz reference clock.

Figure 2. External view of the counter board T-2200.

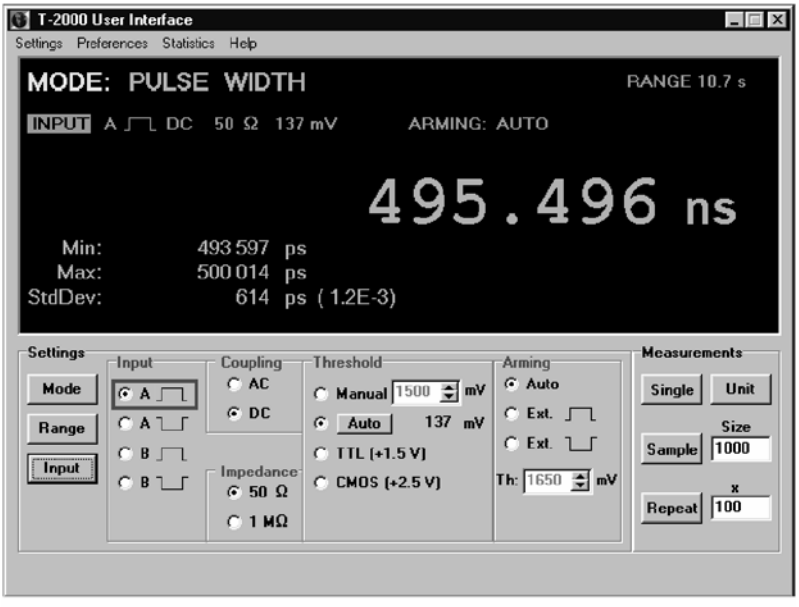
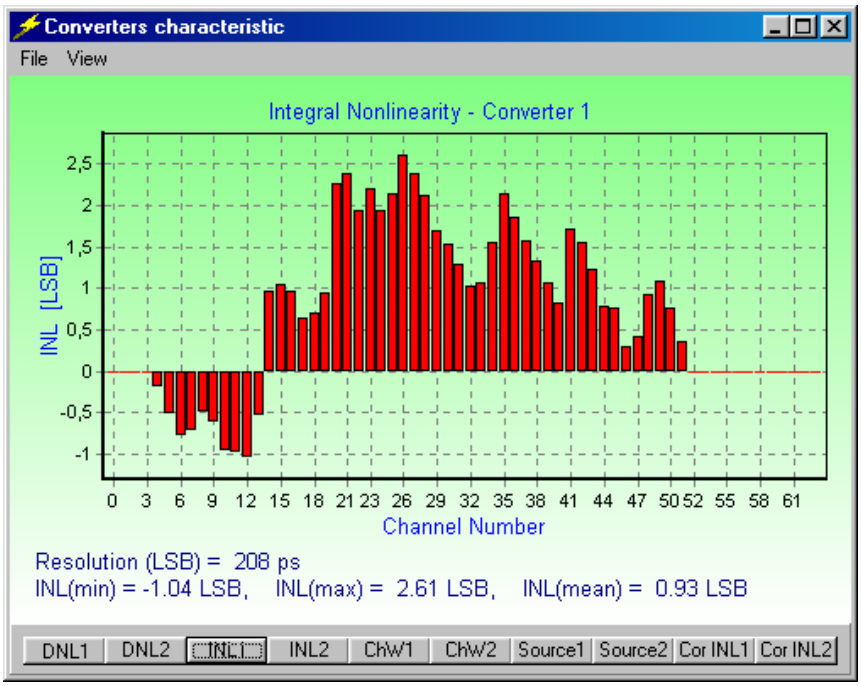


Figure 3. An example of the virtual front panel of the counter T-2200.

a)



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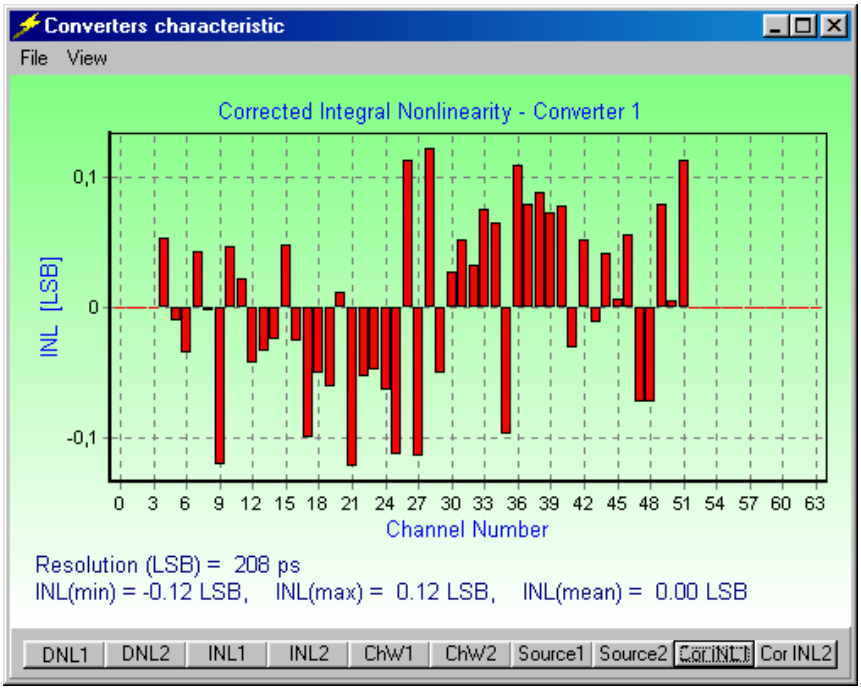

Figure 4. Integral nonlinearity of a single interpolator before (a) and after correction (b).

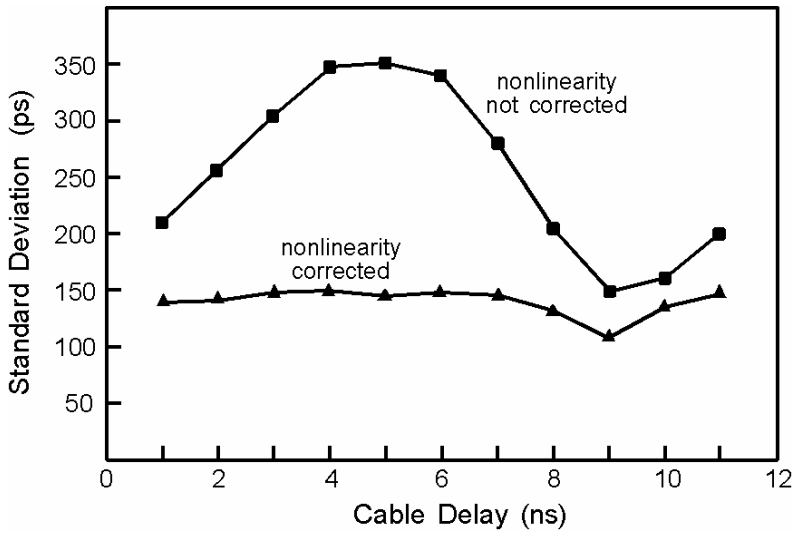

Figure 5. Standard uncertainty of the time counter obtained without and with nonlinearity correction of the differential delay lines.

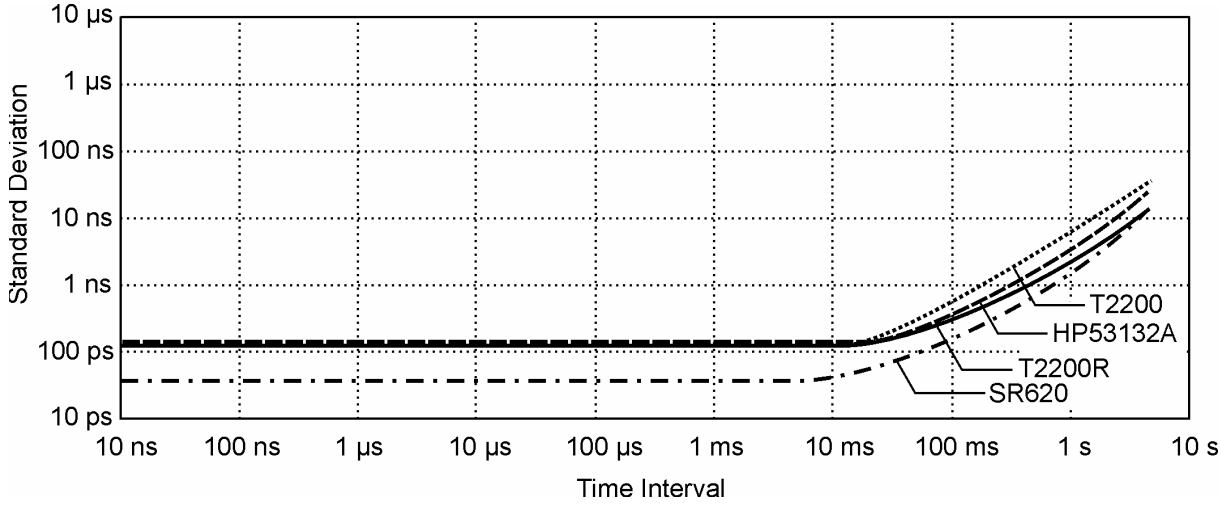

Figure 6. Comparison of standard deviations of the time intervals measured by two counter boards and two desktop commercial counters.

QUESTIONS AND ANSWERS

DAVE HOWE (National Institute of Standards and Technology): I was wondering if any of the possibilities for high-resolution counters you might have thought of involved any analog interpolators. Years ago, HP made what they called a "computing counter" that had an analog interpolator. There were a number of other companies that made those, too. I have not seen that implemented in any of the recent designs. But it would be fairly straightforward, I think, to add it to your digital interpolator. Have you thought about doing that to increase the resolution maybe another factor of ten?

RYSZARD SZPLET: Technology now allows one to design time-to-digital converters as straight-to-digital circuits. We can use the time of the digital lines with a very small delay, as small as 30 picoseconds. It is the smallest quantization step that we can reach in async circuits. Some laboratories, for example in Finland, which are related to Nokia, develop such time-to-digital converters. But async technology is a little bit more expensive than FPGA.

In FPGA, we have another time-to-digital converter with resolution two times better than presented here. It means that we obtained 100-picosecond resolution and the accuracy is even better, about 80 picoseconds. I do not know more about such resolutions.