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Quarterly Technical Report

Solid State Research

2004:2

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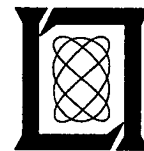

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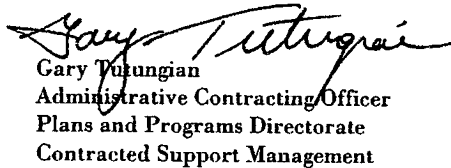

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Solid State Research

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1 February – 30 April 2004

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ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 February through 30 April 2004. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, DARPA, MDA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

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INTRODUCTION

1. QUANTUM ELECTRONICS

A first $AgGaSe_2$ wafer bonding experiment has demonstrated considerable promise for nonlinear optics applications. The bonded wafer pair was repolished on both front and back faces and showed a uniform optical transmission.

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

A self-organized natural superlattice (NSL), which is tilted with respect to (001) terraces of vicinal GaSb, is observed in GaInAsSb epilayers grown by organometallic vapor-phase epitaxy. The NSL period is geometrically correlated with the periodicity of surface undulations.

3. SUBMICROMETER TECHNOLOGY

A new technique for the study of liquid-solid interfaces, rapid cryofixation/freeze-fracture, allows high-resolution imaging of the interfaces between water and substrates with varying degrees of hydrophobicity. By using this technique, we have confirmed the spontaneous formation of nanobubbles at the interface of a gas-saturated fluid and a hydrophobic surface.

Silicon micromachining techniques have been used to fabricate nanoscale probes for testing molecular electronic devices. Self-assembled monolayers of thiols and biphenyl-dithiols have been characterized using this apparatus.

4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

A version of the sample-preparation cartridge LiNK (Lincoln Nucleic acid Kit) has been designed to address multiple requirements. It collects and purifies environmental samples in the field, yielding DNA-containing eluate that is compatible with the RAZOR instrument (Idaho Technology) for polymerase chain reaction analysis.

5. ADVANCED IMAGING TECHNOLOGY

A large-area, high-frame-rate charge-coupled device, incorporating back-side illumination, has been developed for scientific and military use. It comprises eight million pixels in 20 cm^2 of area, with two-stage amplification of the outputs and blooming control to avoid spreading of the charge packet beyond the pixel in which the photoelectron was captured.

6. ANALOG DEVICE TECHNOLOGY

An assessment has been made to determine the potential for decreasing energy per bit requirements to close a link from a ground sensor to an unmanned aerial vehicle. It was determined that such requirements can be decreased by applying advanced technology to the modulator/carrier generation and the output stage amplifier.

7. ADVANCED SILICON TECHNOLOGY

Simplified MOSFET-like devices have been fabricated to characterize the effect of gate resistance on device performance at high frequencies. A guideline is presented for modeling gate resistance.

REPORTS ON SOLID STATE RESEARCH
1 FEBRUARY THROUGH 30 APRIL 2004

PUBLICATIONS

Title	Authors	Reference
Coherent Beam Combining and Phase Noise Measurements of Ytterbium Fiber Amplifiers	S. J. Augst T. Y. Fan A. Sanchez	*Opt. Lett.* **29**, 474 (2004)
Stereolithographic Patterning of Diazonaphthoquinone/Novolac Photoresist	T. M. Bloomstein S. T. Palmacci R. R. Kunz M. Rothschild	*J. Microlithogr. Microfab. Microsyst.* **3**, 339 (2004)
DC Measurements of Macroscopic Quantum Levels in a Superconducting Qubit Structure with a Time-Ordered Meter	D. S. Crankshaw* K. Segall* D. Nakada T. P. Orlando* L. S. Levitov* S. Lloyd* S. O. Valenzuela* N. Markovic* M. Tinkham* K. K. Berggren	*Phys. Rev. B* **69**, 144518-1 (2004)
Air-Bridged Lateral Growth of Crack-Free, Al(0.24)Ga(0.76)N on Highly Relaxed Porous GaN	R. S. Q. Farheed* V. Adivarahan* C. Q. Chen* S. Rai* E. Kuokstis* J. W. Yang* M. A. Khan* J. M. Caissie R. J. Molnar	*Appl. Phys. Lett.* **84**, 696 (2004)

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Recombination Parameters for Antimonide-Based Semiconductors Using the Radio Frequency Photoreflectance Technique	R. J. Kumar* R. J. Gutmann* J. M. Borrego* P. S. Dutta* C. A. Wang R. U. Martinelli* G. Nichols*	*J. Electron. Mater.* **33**, 94 (2004)
Electron Scattering in AlGaN/GaN Structures	S. Syed* M. J. Manfra Y. J. Wang* R. J. Molnar H. L. Stormer*	*Appl. Phys. Lett.* **84**, 1507 (2004)
Research on Macro- and Microsegregation in Semiconductor Crystals Grown from the Melt under the Direction of August F. Witt at the Massachusetts Institute of Technology	C. A. Wang D. Carlson* S. Motakef* M. E. K. Wiegel M. J. Wargo*	*J. Cryst. Growth* **264**, 566 (2004)
Wafer Bonding and Epitaxial Transfer of GaSb-Based Epitaxy to GaAs for Monolothic Interconnection of Thermophotovoltaic Devices	C. A. Wang D. A. Shiau* P. G. Murphy P. W. O'Brien R. K. Huang M. K. Connors A. C. Anderson D. Donetsky* S. Anikeev* G. Belenky* D. M. Depoy*	*J. Electron. Mater.* **33**, 213 (2004)

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Energy Relaxation Time Between Macroscopic Quantum Levels in a Superconducting Persistent-Current Qubit	Y. Yu* D. Nakada J. L. Lee* B. Singh* D. S. Crankshaw* T. P. Orlando* K. K. Berggren W. D. Oliver	*Phys. Rev. Lett.* **92**, 117904-1 (2004)

PRESENTATIONS†

150-W Cryogenically Cooled Yb:YAG Laser	D. J. Ripin J. R. Ochoa R. L. Aggarwal T. Y. Fan	OSA Topical Meeting on Advanced Solid-State Photonics, Santa Fe, New Mexico, 1–4 February 2004
Energy-Scavenging Amplifiers for Miniature Solid-State Lasers	J. J. Zayhowski A. L. Wilson, Jr.	OSA Topical Meeting on Advanced Solid-State Photonics, Santa Fe, New Mexico, 1–4 February 2004
Resist Materials for Advanced Lithography	T. H. Fedynyshyn	DARPA Program Review, Las Vegas, Nevada, 2–5 February 2004
The Development of Immersion Lithography	M. Switkes M. Rothschild	DARPA Program Review, Las Vegas, Nevada, 2–5 February 2004

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† Titles of presentations are listed for information only. No copies are available for distribution.

CCD Technology for LSST	B. E. Burke	Large-Aperture Synoptic Survey Telescope (LSST) Workshop, Brookhaven National Laboratory, Upton, New York, 4 February 2004
GaInAsSb/AlGaAsSb/GaSb Thermophotovoltaic Devices	C. A. Wang	Technical Seminar, Massachusetts Institute of Technology, Cambridge, Massachusetts, 4 February 2004
Is Increasing Mask Complexity Inevitable for Advanced Optical Lithography?	M. Fritze B. Tyrrell	Microlithography 2004, Santa Clara, California, 22–27 February 2004
193 nm Lithography: Fundamentals and Issues	R. R. Kunz	Microlithography 2004, Santa Clara, California, 22–27 February 2004
Photoresist Outgassing: A Potential Achilles Heel for Short-Wavelength Optical Lithography?	R. R. Kunz	Microlithography 2004, Santa Clara, California, 22–27 February 2004
Time Resolved Photoresist Outgassing	R. R. Kunz D. K. Downs	Microlithography 2004, Santa Clara, California, 22–27 February 2004
Photo-induced Changes in 157-nm Optical Coating	V. Liberman T. M. Bloomstein M. Rothschild S. T. Palmacci J. H. C. Sedlacek	Microlithography 2004, Santa Clara, California, 22–27 February 2004

Scattering in Liquid Immersion Lithography	M. Switkes T. M. Bloomstein M. Rothschild M. Yeung*	Microlithography 2004, Santa Clara, California, 22–27 February 2004
Automated CANARY Testbed for Fast Bioaerosol Identification	J. D. Harper	2nd Joint Conference on Point Detection for Chemical and Biological Defense, Williamsburg, Virginia, 1–5 March 2004
Laser-Induced Breakdown Spectroscopy (LIBS) of Airborne Bioaerosol Particles	J. D. Hybl	2nd Joint Conference on Point Detection for Chemical and Biological Defense, Williamsburg, Virginia, 1–5 March 2004
Development of a UV LED Based Biosensor	T. H. Jeys L. Desmarais J. G. Ingwersen X. T. Le P. L. Ward V. Daneu	2nd Joint Conference on Point Detection for Chemical and Biological Defense, Williamsburg, Virginia, 1–5 March 2004
Luminescence Spectroscopy of Biological Simulants and Interferents	D. J. Ripin J. D. Hybl W. D. Herzog T. H. Jeys P. J. Foti A. Sanchez	2nd Joint Conference on Point Detection for Chemical and Biological Defense, Williamsburg, Virginia, 1–5 March 2004

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All Digital Geiger-Mode Avalanche Photodiode Intensity Camera Using Solid-State Photon-Counting Focal Plane	A. G. Stern B. F. Aull B. B. Kosicki R. R. Reich B. J. Felton A. H. Loomis D. J. Young R. Slattery K. Percival R. B. Halloway C. D. Jones	Meeting of the Military Sensing Symposia Specialty Group on Passive Sensors, Tucson, Arizona, 1–5 March 2004
Sub-volt V_{π} InGaAsP Electro-refractive Modulators Using Symmetric, Uncoupled Quantum Wells	P. W. Juodawlkis F. J. O'Donnell R. J. Bailey J. J. Plant K. G. Ray D. C. Oakley A. Napoleone G. E. Betts*	29th Annual Government Microcircuit Applications and Critical Technology (GOMAC) Conference, Monterey, California, 15–18 March 2004
Enhancing Silicon MOSFETs for High Performance Mixed-Signal Applications	C. Keast M. Fritze C-L. Chen P. Wyatt J. Knecht	29th Annual Government Microcircuit Applications and Critical Technology (GOMAC) Conference, Monterey, California, 15–18 March 2004
Nanostructured Direct Energy Conversion Materials and Devices	T. C. Harman	National Nanotechnology Initiative Grand Challenge Workshop: Nanoscience Research for Energy Needs, Crystal City, Virginia, 16–18 March 2004

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Detecting Low Vapor Pressure Chemicals	R. R. Kunz M. W. Geis T. M. Lyszczarz	Homeland Security Advanced Research Projects Agency (HSARPA) Workshop, Arlington, Virginia, 6–7 April 2004
High-Speed Solid-State Imager Technology	R. Reich D. Rathman D. O'Mara D. Young A. Loomis E. Kohler R. Osgood R. A. Murphy M. Rose R. Berger B. Kosicki S. Watson* M. Ulibarri* T. Perry*	Lincoln Laboratory Technical Seminar Series, University of Florida, Gainesville, Florida, 8 April 2004
Development of a UV LED Based Biosensor	T. H. Jeys L. Desmarais J. G. Ingwersen X. T. Le V. Daneu	SPIE International Symposium on Defense and Security, Orlando, Florida, 12–16 April 2004
InGaAsP/InP Quantum-Well Electrorefractive Modulators Having Sub-volt V_π	P. W. Juodawlkis F. J. O'Donnell R. J. Bailey J. J. Plant K. G. Ray D. C. Oakley A. Napoleone M. R. Watts* G. E. Betts*	SPIE International Symposium on Defense and Security, Orlando, Florida, 12–16 April 2004

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165-W Cryogenically Cooled Yb:YAG Laser	D. J. Ripin J. R. Ochoa R. L. Aggarwal T. Y. Fan	SPIE International Symposium on Defense and Security, Orlando, Florida, 12–16 April 2004
MIT Lincoln Laboratory's 3D Circuit Integration Technology	C. L. Keast J. A. Burns C. K. Chen J. M. Knecht K. Warner	SEMATECH 3D Technology, Modeling and Process Symposium, San Francisco, California, 13 April 2004

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1. QUANTUM ELECTRONICS

1.1 $AgGaSe_2$ WAFER BONDING

$AgGaSe_2$ is an interesting nonlinear optical material, and considerable progress has been made in growing high-quality bulk crystals [1],[2]. Bonding (or fusion) of GaAs wafer stacks has previously been demonstrated for quasi phase-matching [3]. Here, we report a first $AgGaSe_2$ wafer bonding, which is promising for walk-off compensation for efficient nonlinear frequency conversion.

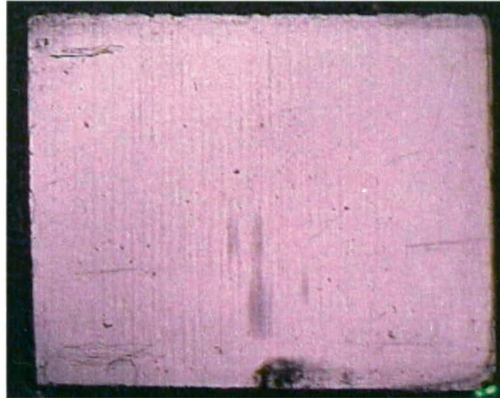
Double-side polished wafers of 7.5-mm length, 6.0-mm width, and 0.5-mm thickness were purchased from Cleveland Crystals, Inc., Highland Heights, Ohio. Designed for a second-harmonic-generation experiment, the wafer surface was oriented at a 49° angle with respect to the crystal's c-axis. The polished wafers generally showed good flatness and smoothness. The surface had some mild microscopic waviness, however, which appeared as a uniform coverage of parallel striations arranged in a ~1-μm pitch (in a quasi periodic manner) when examined under an optical microscope with interference contrast. In a given wafer, the striations were predominantly parallel to the 7.5-mm side on one face and to the 6.0-mm side on the opposite face. A wafer corner was lightly scribed for identification, so that faces of the same striation direction would be used for bonding. The scribed marks can be seen in the micrographs of Figure 1-1.

Two wafers were first briefly rinsed in isopropanol with gentle agitation. Afterwards, they were removed (wet) from the isopropanol bath and dropped on a small quartz pedestal one after the other. The wafers became stacked and self-aligned because of surface tension. The bulk of the isopropanol on the surface evaporated in ~1 h, but a remaining thin film took several more hours to evaporate. This unusually slow evaporation indicates a strong adhesive force to the surface. The wafer pair became bonded, apparently by van der Waals force [4], and did not separate under gentle handling.

In order to heat treat the bonded wafer pair without any pressure, it was placed in a graphite container in a plugged quartz tube and then loaded into a furnace tube. The furnace system was purged with Ar flow. The temperature was slowly raised to 400°C, kept there for 8 h, and then slowly lowered back down. The wafers, however, easily separated after this heat treatment.

The wafers were immediately reloaded back into the graphite container, this time shimmed to raise the graphite plug to a tight fit inside a thick-wall quartz cylinder. This would lead to a high uniaxial pressure in heat treatment, due to the differential thermal expansion between graphite and quartz [5]. The furnace temperature was ramped to 550°C at rates generally less than 2°C/min. The 550°C treatment lasted 15 h, and the system was then cooled slowly back down to room temperature.

The wafer pair became quite strongly bonded and possibly fused, i.e., covalent bonds formed. The outer faces, however, were marred by contacting graphite in the process, as is evident in Figure 1-1(a). Surface smoothness was then restored after a light polish, as shown in Figure 1-1(b). Note that this


(a)

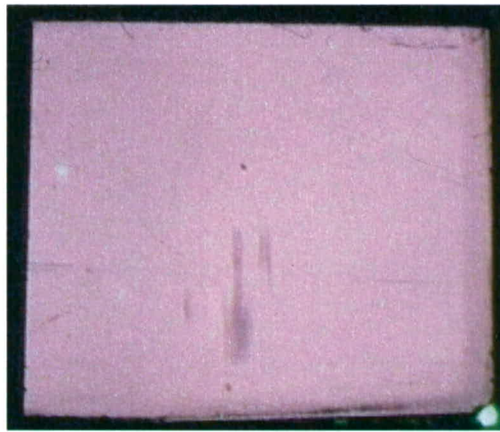

(b)

Figure 1-1. Infrared (790-nm wavelength) transmission optical micrographs of (a) an as bonded pair of 7.5 × 6.0-mm $AgGaSe_2$ wafers, and (b) the same wafer pair (but opposite face) after a light surface polish.

micrograph shows a uniform transmission across the bonded wafer pair, except for few small spots near the middle. The lower transmission of the spots indicates unbonded gaps approaching one quarter of 790 nm, the wavelength of light used here. These wafer bonding results show considerable promise for nonlinear optics applications.

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2. ELECTRO-OPTICAL MATERIALS AND DEVICES

2.1 SELF-ORGANIZED VERTICAL SUPERLATTICES IN EPITAXIAL GaInAsSb

Phase separation in multicomponent compound semiconductors has been widely reported [1]. Of particular interest are materials systems that spontaneously self-organize with a significant degree of regularity, since this periodicity can impact the electronic band structure and thus the materials properties and device performance. The length scale of these ordered phases ranges from the atomic scale, as reported for CuPt ordering in GaInP [2], to microscopic dimensions on the order of ~50 nm, which is known as composition modulation [3]–[7]. Lateral composition modulation (LCM) persists parallel (lateral) to the growth direction, while vertical composition modulation (VCM) is perpendicular to the growth direction. LCM has been reported in strained alloy systems such as bulk AlInAs and GaInP epilayers [3]–[5], as well as in short-period superlattices such as GaP/InP, AlAs/InAs, GaAs/InAs, and InAs/GaSb [6]–[7].

VCM and self-organized natural superlattices (NSLs) in alloy layers that are homogenously grown have also been observed, but these studies are less frequently reported and the mechanism for the self-organization is less understood. NSLs have been reported in ZnSeTe grown on vicinal GaAs substrates [8] and SiGe grown on (001) Si [9]. The NSL period was 2–3 nm for both of these materials systems, and a model based on step-flow growth and local strain fields that are modulated during growth were developed to explain the phenomena [9]. In addition, InAsSb and GaAsSb [10] were reported to spontaneously form a periodic structure that consisted of platelets of alternating composition and periodicity on the order of 20–50 nm. Both InAsSb and GaAsSb exhibit miscibility gaps [11], and this larger-scale modulation was attributed to the tendency for these alloys to phase separate. More recently, spontaneous superlattice formation was observed for GaInAsSb [12], AlGaInN [13], and AlGaInAsSb [14]. These NSLs have a modulation period ranging from 10 to 30 nm.

This work reports spontaneous formation of self-organized NSLs in GaInAsSb alloys grown nominally lattice matched to vicinal GaSb substrates. The NSL is inclined 4° with respect to the (001) terrace of the vicinal substrate. Furthermore, the NSL period is correlated with the periodicity of undulations on the epilayer surface, which clearly demonstrates the intimate coupling between composition modulation and morphological perturbations [15],[16]. It is further shown that surface undulations can intentionally induce the NSL.

GaInAsSb epitaxial layers were grown nominally lattice matched to (001) GaSb substrates with miscut angles of 2° or 6° toward (1-11)B or (101) by organometallic vapor-phase epitaxy (OMVPE), as previously described [17],[18]. The growth temperature was either 525°C or 575°C. Trimethylindium, triethylgallium, tertiarybutylarsine, and trimethylantimony were used as organometallic precursors. Growth was initiated by simultaneously flowing the four precursors into the OMVPE reactor. The growth rate was ~5 μm/h, and the layers were 1–4 μm in thickness. Two different alloy compositions were grown: $Ga_{0.89}In_{0.11}As_{0.09}Sb_{0.91}$ and $Ga_{0.8}In_{0.2}As_{0.17}Sb_{0.83}$, which have 300-K photoluminescence (PL) peak

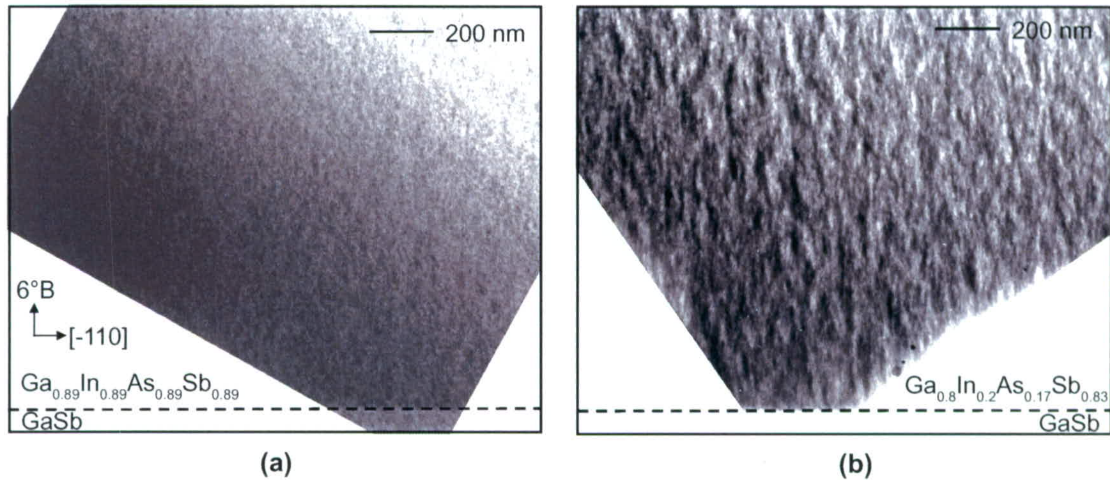


Figure 2-1. Bright-field <110> cross-sectional transmission electron microscopy (TEM) images using g = <220> two-beam diffraction of GaInAsSb grown at 525°C on substrates oriented (001) 6° toward (1-11)B: (a) 0.6-eV $Ga_{0.89}In_{0.11}As_{0.09}Sb_{0.91}$ and (b) 0.5-eV $Ga_{0.8}In_{0.2}As_{0.17}Sb_{0.83}$. The images are oriented so that the growth direction is straight up.

energy at 0.6 and 0.5 eV, respectively. The microstructure of GaInAsSb was studied by examining <110> cross sections in a transmission electron microscope (TEM) operated at 200 kV. The NSL was imaged using *g* = <222> or <111> two-beam conditions, in either bright- or dark-field conditions. The layers were also characterized by PL at 300 and 4 K and atomic force microscopy (AFM) operating in tapping mode.

Figures 2-1(a) and 2-1(b) show bright-field <110> cross-sectional TEM images of 0.6-eV GaInAsSb and 0.5-eV GaInAsSb, respectively. The layers were grown at 525°C on (001) GaSb substrates miscut 6° toward (1-11)B. Minimal TEM diffraction contrast is observed for 0.6-eV GaInAsSb, while significant spinodal-like contrast [1] is observed for 0.5-eV GaInAsSb. This contrast results from strain that is associated with phase separation into GaAs- and InSb-rich regions [17],[18] and is consistent with the 0.5-eV GaInAsSb alloy being further in the miscibility gap [11]. Excellent optical properties were observed with 4-K PL full width at half-maximum (FWHM) of 4.3 and 9.5 meV, for Figures 2-1(a) and 2-1(b), respectively.

In addition to the spinodal-like contrast observed in Figure 2-1(b) for 0.5-eV GaInAsSb, Figure 2-1 shows the presence of a self-organized NSL in dark-field <110> TEM cross sections. On the other hand, no NSL was detected in 0.6-eV GaInAsSb. The image shown in Figure 2-2(a) is a [110] cross section; the step-flow direction is [1-10] [18]. The NSL has a 10° tilt with respect to the surface normal, which is an additional 4° compared to the 6° miscut angle, i.e., it is tilted 4° from the (001) terrace. The NSL is observed at the onset of growth, is laterally continuous throughout the epilayer, and has a periodicity of

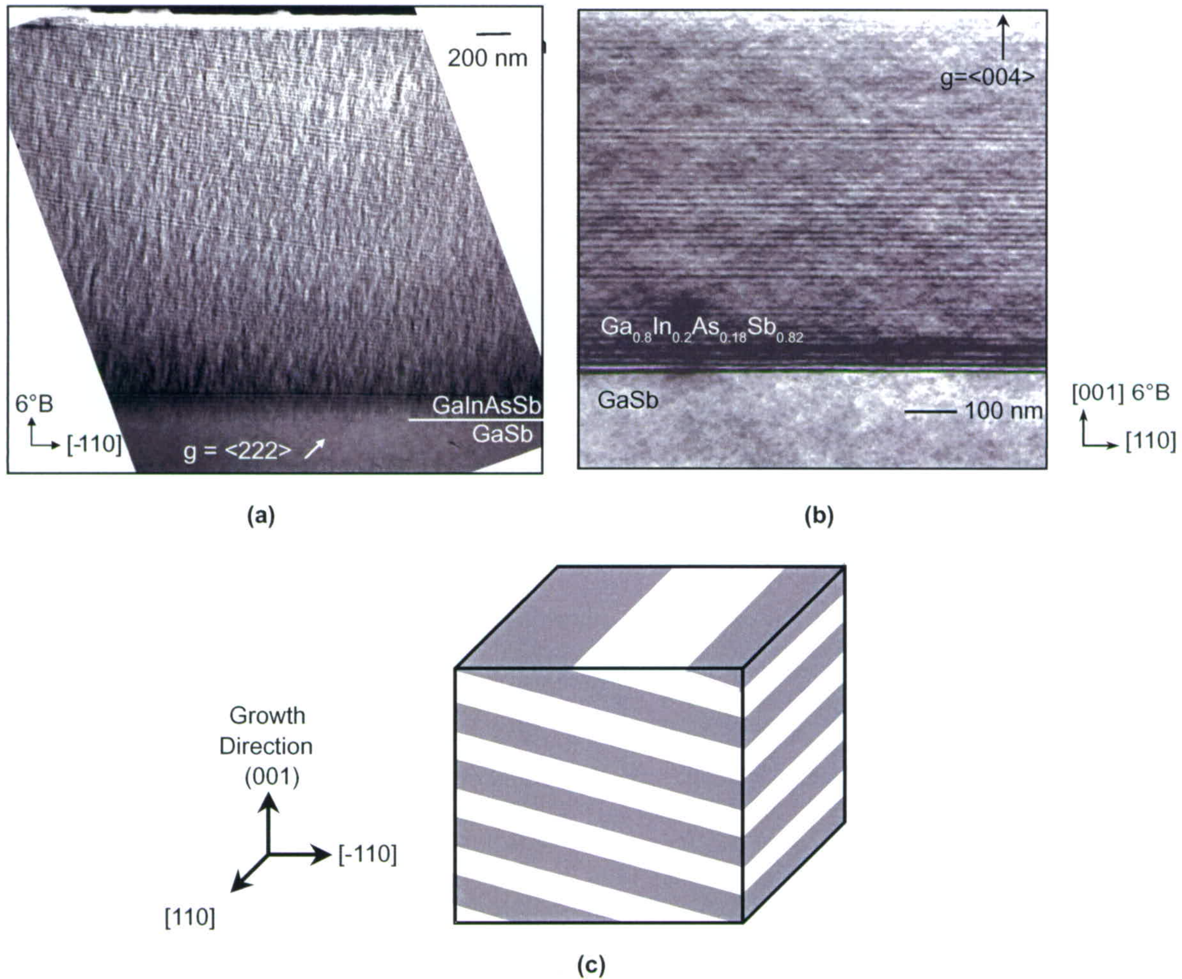


Figure 2-2. TEM images and schematic microstructure of 0.5-eV GaInAsSb: (a) [110] cross section using dark-field g = <222> two-beam conditions, (b) [-110] cross section using g = <004> two-beam conditions, and (c) three-dimensional schematic of tilted natural superlattice (NSL) microstructure.

20 nm throughout the 2-μm-thick epilayer. Figure 2-2(b) is the orthogonal [-110] cross section and shows that the NSL is parallel to the growth surface. Figure 2-2(c) schematically shows the geometry of the microstructure.

Figures 2-3(a) and 2-3(b) show atomic force microscopy (AFM) images of 0.6-eV GaInAsSb and 0.5-eV GaInAsSb, respectively. The surface of 0.6-eV GaInAsSb is relatively smooth and flat. Conversely, 0.5-eV GaInAsSb exhibits a periodic surface undulation that is aligned along the step edges of the vicinal

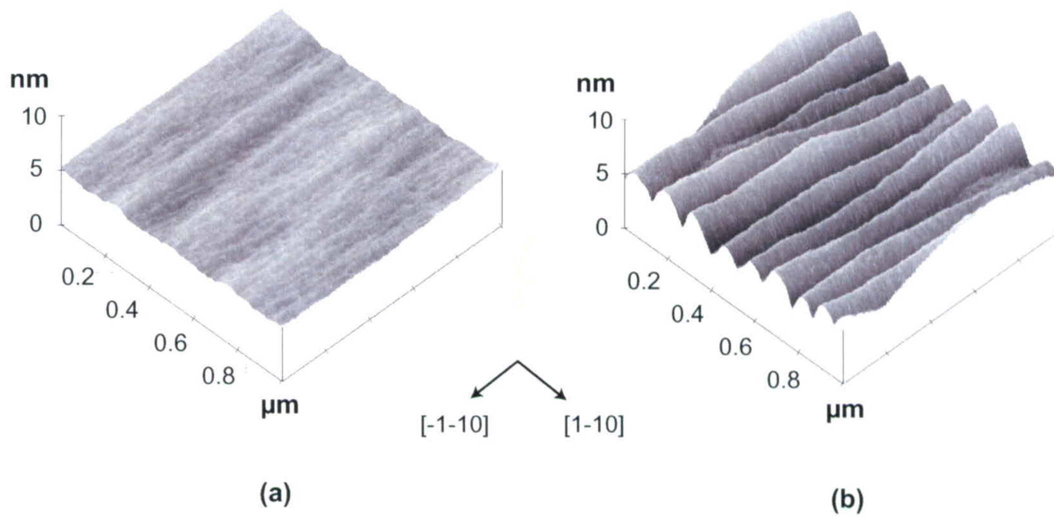


Figure 2-3. Atomic force microscopy (AFM) images of the surface undulations of GaInAsSb samples grown on (001) 6° toward [1-11]B GaSb substrates: (a) 0.6-eV GaInAsSb with no tilted NSL and (b) 0.5-eV GaInAsSb with a tilted NSL.

substrate, i.e., along [110]. Since the tilted NSL intersects the surface of the epilayer, it was of interest to compare the period of the tilted NSL with the periodicity of these surface undulations. The 20-nm period with a 10° tilt corresponds to a surface period of 115 nm. The surface undulation of the AFM image shown in Figure 2-3(b) has a lateral period of about 111 nm. Thus, the tilted NSL and the period of the surface undulations are correlated. Table 2-1 lists additional samples with various miscut angles and directions with similar correlation. The additional tilt angle with respect to the vicinal substrate is about 4° in each case.

These results suggest that the tilted NSL and surface undulations are coupled and furthermore depend on the thermodynamic driving force for phase separation. To study this hypothesis a test structure, shown in Figure 2-4(a), was specially grown. It consists of two different alloy compositions of GaInAsSb, shown as layers 1, 3, and 5, separated by 2-nm GaSb, shown as layers 2 and 4. Layers 1 and 5 are 0.6-eV GaInAsSb, while layer 3 is 0.5-eV GaInAsSb. Based on the results shown in Figures 2-1 and 2-2, spinodal-like contrast and a tilted NSL are expected in layer 3 but not in layers 1 and 5. Examination of TEM cross sections showed no tilted NSL in layer 1 and a tilted NSL in layer 3, as expected. On the other hand, the TEM cross section shown in Figure 2-4(b) reveals a tilted NSL not only in layer 3 but also in layer 5. The contrast modulation associated with the NSL in layer 5 is weaker, but the periodicity (17.2 nm) of the NSL in layers 3 and 5 is the same. Although the composition associated with layer 5 does not

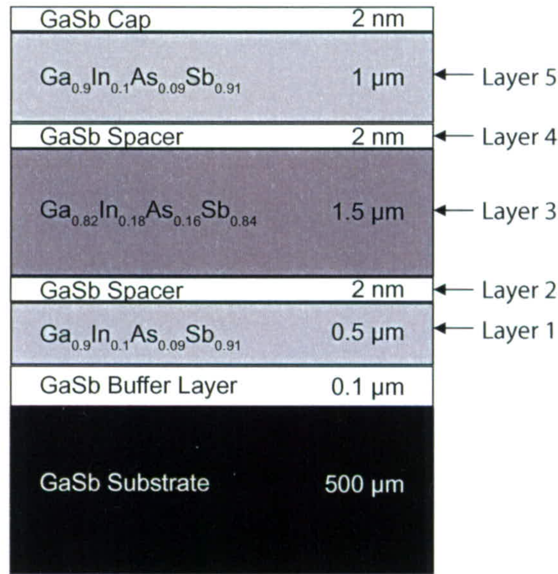
TABLE 2-1
Correlation of Tilted Natural Superlattice and Surface Undulations

Miscut Angle and Direction	NSL Period (nm)	NSL Tilt Angle (°)	NSL Lateral Period (nm)	AFM Period (nm)
6° [1-11]B	20	10	115	111
2° [1-11]B	14.6	5.8	144	143
2° [101]	13.8	6.0	132	160

inherently phase separate to form a tilted NSL, it did so in this case because surface undulations present on layer 3 created a lateral surface segregation, which then induced the NSL. These results clearly illustrate the coupling of compositional and morphological perturbations [15],[16].

A qualitative model for the initial formation of the tilted NSL and its propagation throughout the epilayers is proposed. The thermodynamic driving force of the miscibility gap causes adatoms to segregate, which forms a LCM, with one phase slightly enriched in InSb and the other slightly enriched in GaAs. Once such LCM forms, the surface is strained because of the lattice mismatch between the two GaInAsSb phases enriched in GaAs and InSb. As has recently been shown theoretically by Glas [16], a surface with such LCM can effectively relieve its strain if the larger lattice constant phase (InSb-rich phase) forms peaks, while the smaller lattice constant phase (GaAs-rich phase) forms valleys. Therefore, the surface forms a series of peaks and valleys, creating surface undulations, as are observed in the AFM image in Figure 2-3(b). Once such undulations form, all subsequent epitaxial deposition is biased to minimize surface stresses so that surface peaks preferentially incorporate InSb-enriched GaInAsSb, while the surface valleys preferentially incorporate GaAs-enriched GaInAsSb. This strain locking causes the NSL to continually propagate throughout epilayer growth. Therefore, the composition modulation associated with the tilted NSL is directly coupled to the surface undulations, and shows that surface strain or roughness can promote phase separation. Such strain-locking mechanisms due to surface stress are also known to play important roles in other epitaxial phenomena such as the vertical registry of multiple layers of quantum dots.

The mechanism for the additional tilt of the NSL with respect to surface steps can be explained in part by the mechanism suggested by Venezuela et al. [9]. The model is based on alloy decomposition at step bunches, which are compressively and tensilely strained at the base and top of the bunch, respectively. NSL formation with a period on the order of the step-bunch height of a few nanometers and with an additional tilt angle with respect to the substrate miscut angle was predicted for alloys grown on surfaces with modulated strain fields. However, since the NSL periods observed in this study are on the order of



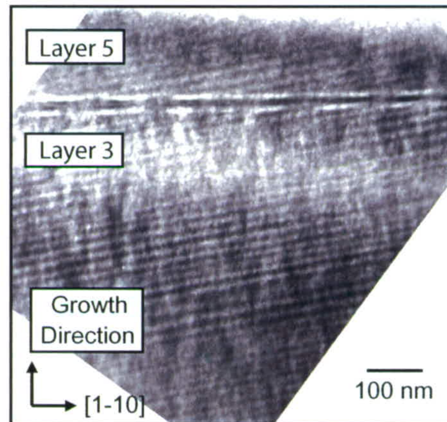


Figure 2- 4. (a) Schematic test structure and (b) <222> two-beam diffraction of layers 3–5.

20 nm, that model cannot fully explain the larger NSL periods observed here. Therefore, it is proposed that surface undulations play a similar role to step bunches in the Venezuela model. Rather than ejection and capture of single steps from step bunches, in this case the additional tilt is caused by ejection and capture of single steps from surface peak or valley regions. The lateral period of the undulations range from 100 to 200 nm. Each peak or valley is therefore spaced 50–100 nm, and thus comprises on average 17–34

individual steps (for a 6° miscut) or 6–11 steps (for a 2° miscut). As epitaxial growth proceeds, if an individual step is ejected by a valley and captured by an adjacent peak, that step would switch its incorporation preference from GaAs enrichment to InSb enrichment. Similarly, that step would eventually be ejected from the peak and captured by the adjacent valley, switching its preference back to GaAs enrichment. The magnitude of the additional tilt with respect to the substrate miscut angle is dependent on the relative lateral velocities of the surface undulations and the individual steps comprising those undulations.

In summary, self-organized NSLs are observed in GaInAsSb epilayers. The NSL exhibits a 4° tilt with respect to the miscut angle of the GaSb substrate, and the NSL period is directly correlated with periodic undulations on the epilayer surface. While the underlying driving force for this phase separation arises from solution thermodynamics, the mechanism for the self-organized microstructure is related to local strains associated with surface undulations. The undulations form to relieve the local strain associated with composition modulation of the tilted NSL and demonstrate the coupling between composition modulation and morphological perturbations. A qualitative model for the propagation and robustness of the tilted NSL is discussed.

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3. SUBMICROMETER TECHNOLOGY

3.1 RAPID CRYOFIXATION/FREEZE-FRACTURE FOR THE STUDY OF NANOBUBBLES AT SOLID-LIQUID INTERFACES

Liquid immersion [1] is a leading resolution enhancement candidate for extending optical lithography to the 70-nm regime and beyond. At the 193-nm exposure wavelength, deionized water is a suitable fluid for filling the space between the final lens element and the wafer, but there are concerns over the formation of bubbles [2] at the water-resist interface that will affect the quality of the patterning. Several recent tapping-mode atomic force microscopy (AFM) studies of immersed hydrophobic surfaces [3]–[6] have shown the presence of soft domains on the 100-nm scale, dubbed nanobubbles. Using a new technique for the study of these interfaces, rapid cryofixation/freeze-fracture (RCF), we confirm the presence of these domains and show that they arise spontaneously from dissolved gas in the water on time scales <1 min.

RCF for the study of liquid-surface interfaces evolved from biological sample preparation techniques, freeze fracture and quick-freeze deep etch [7], which are used to capture high-resolution images of both static structures and dynamic biological processes [8]. Normal freezing leads to the rearrangement of water molecules into crystalline ice and thus the distortion of the original structures [9]. However, freezing at a rate of about 20,000 K/s or greater [10] leads to the formation of amorphous ice and to the preservation of the original structures. Once the sample is well preserved, an area of interest can be exposed by cleaving the sample with a knife (freeze fracture). For embedded structure imaging, cleaving may be followed by sublimation of water from the fractured surface (quick-freeze deep etch). The exposed surface can then be imaged directly, for example with cryogenic AFM [11], or more commonly through a replica formed by depositing metal on the surface. In this investigation a combination of rapid freezing and freeze fracture were used to preserve, expose, and replicate the interface between water and various substrates.

To study solid-liquid interfaces with RCF, the freezing must proceed through the solid substrate, which must therefore be thermally conductive. A schematic diagram of the procedure is shown in Figure 3-1. The substrate presenting the surface of interest is suspended above a support stage, and the water is introduced between the two. This sandwich is then brought into contact with a cooled copper mirror, resulting in rapid flow of heat through the conductive substrate and the formation of a layer of amorphous ice at the water-substrate interface. The frozen sandwich is maintained at low temperature and placed under high vacuum where the substrate is fractured off of the amorphous ice interface, exposing the frozen water surface for direct imaging or the formation of a replica.

RCF was used to study the interface between deionized water and a Si substrate. Hydrophilic and hydrophobic surface treatments were tested with both gas-saturated and degassed water. The Si substrate material was first prepared by patterning and thinning. A 12-μm periodic grating was etched 100 nm into

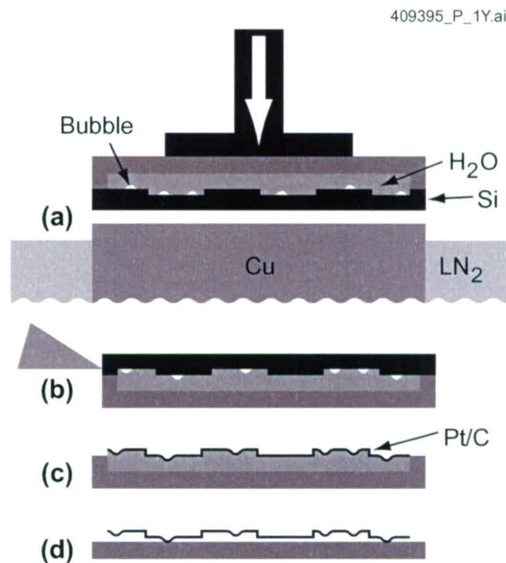

Figure 3-1.Schematic diagram of rapid cryofixation/freeze-fracture procedure: (a) Sample is frozen by rapid contact with a polished Cu block immersed in liquid N_2, (b) top Si layer is removed under high vacuum, (c) thin layers of Pt and C are evaporated to form a replica of the frozen water surface, and (d) sample is warmed and dehydrated leaving the replica for microscopic examination.

the surface of a Si wafer using standard photolithographic techniques. The presence of this pattern, visible immediately in a low-powered optical microscope, assured that the final replica indeed represented the interfacial region. The Si substrates also had to be thinned since the effective thermal conductance of the standard 0.4-mm-thick wafers was too low. Attempts to freeze through substrates at this thickness led to the formation of large ice crystals, distorting the interface. To improve conductivity, the backs of the substrates were polished yielding a total thickness of ~70 μm, which was sufficient both for ease of handling and for high-quality cryofixation of the underlying water layer.

Various surface treatments were used to produce hydrophilic and hydrophobic surface terminations on the Si substrates. For hydrophilic surfaces the Si was cleaned and then exposed to an oxygen plasma for 5 min, leading to the formation of a SiO_2 surface layer. The static contact angles of water and decalin on these surfaces were 29 and 20°, respectively, yielding polar and dispersive surface energies of 3.6×10^{-2} and 2.8×10^{-2} Nm^{-1}, respectively [12]. The preparation of hydrophobic surfaces began in the same manner. After the oxygen plasma, the samples were exposed to hexamethyldisilazane (HMDS) vapor for 30 min or more. These samples were then stored in hexane until ready for use. Water and decalin had static contact angles of 92 and 35°, respectively, on these surfaces, yielding polar and dispersive surface energies of 2.8×10^{-3} and 2.5×10^{-2} Nm^{-1}.

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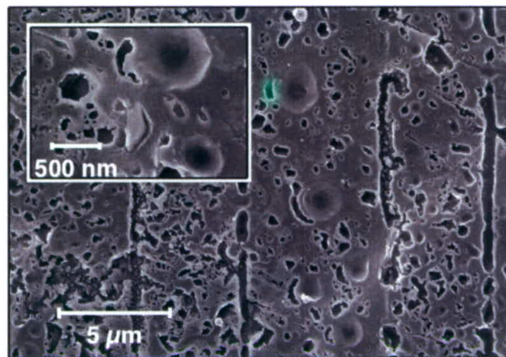

Figure 3-2. Combination of gas-saturated water and hydrophobic surface producing a replica filled with voids due to nanobubble formation at the interface. The vertical lines seen at the right result from a grating etched into the Si substrate, ensuring that the correct interface was replicated.

Degassed water was prepared by multiple cycles of freezing and thawing under vacuum until no further evolution of bubbles was observed on thawing. The degassed water was then sealed under high vacuum and opened less than 1 min prior to use. Either this water or standard gas-saturated deionized water was injected to fill the 2-mm space between the patterned Si substrates and a smooth support stage. Within 1 min of this filling, the samples were placed on a commercial impact freezer (Leica EM CPC MM80, Glatbrugg, Switzerland) and frozen by contact with a polished Cu block immersed in liquid N_2. Numerical simulations predict freezing rates >40,000 K/s for the water within 20 μm of the Si surface and thus the formation of an amorphous ice layer at least this thick.

The frozen samples were placed on a stage held at ~80 K in a high-vacuum freeze-fracture device (Cressington CFE60, Watford, UK, pressure $<10^{-5}$ Torr), and a cooled manipulator was used to remove the patterned Si substrate. At this point the exposed surface reflected the morphology of the water-surface interface, frozen in amorphous ice. This surface was preserved by quickly evaporating ~1-nm Pt and ~10-nm C at low angle (20°) to form a replica. After removal from the high vacuum, the sample was allowed to warm and dehydrate at room temperature. As the water evaporated, the replica settled on the support stage and was ready for examination by electron microscopy.

Scanning electron micrographs of replicas are shown in Figures 3-2 through 3-4. In each figure, the pattern that was etched into the Si substrate is clearly visible, ensuring that the replica is of the liquid-surface interface and not, for example, of some deeper fracture plane within the ice. The combination of gas-saturated water with a hydrophobic substrate, shown in Figure 3-2, leads to a dense, interconnected network of voids in the replica with the lateral extent of a single "cell" from 50 to 500 nm. Because of the low angle of evaporation, the 11-nm-thick replica does not capture the height of the surface features. Any depression with a diameter height ratio less than 5.5 would be expected to leave such a void.

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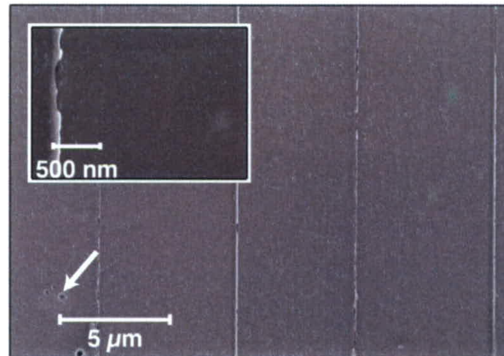

Figure 3-3. Combination of hydrophobic surface with degassed water producing a smooth surface interrupted only by the grating lines etched into the Si substrate. The arrow indicates a small interruption in the smooth surface, perhaps due to air entrained as the sample was filled.

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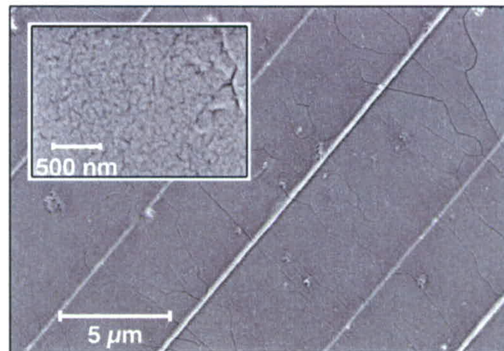

Figure 3-4. Combination of gas-saturated water and hydrophilic surface producing an interface that is smooth but not as smooth as in the case of degassed water. The origin of the cracks running from lower right to upper left is still unknown.

Without dissolved gas, this network of voids is absent. The replica in Figure 3-3, formed from degassed water on a hydrophobic surface, is smooth with no trace of the voids seen in the gas-saturated case. There are several depressions in the replica clustered in the lower left-hand side of the image (indicated by an arrow). We speculate that these are due to air entrained at the surface during the injection of the water into the sample sandwich. Finally, Figure 3-4 shows the replica formed when gas-saturated water interacts with a hydrophilic surface. The network of voids seen at the hydrophobic surface is absent, but long cracks run through the replica essentially perpendicular to the grating. In addition, as the inset shows, the surface of this replica appears much rougher than that produced by degassed water.

Using rapid cryofixation, we have for the first time been able to explore the influence of dissolved gas on the interface between water and surfaces of varying hydrophobicity. Dissolved gas has a profound impact on the morphology of the interface at hydrophobic surfaces. Degassed water produces smooth interfaces that conform to the underlying substrate, while gas-saturated water produces an intricate network of features at the 100 nm scale. These features have a spatial and size distribution similar to those seen in AFM imaging [6], confirming the status of the latter as nanobubbles that form spontaneously from the dissolved gas in the water.

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3.2 TESTING NANOSCALE METAL-SAM-METAL JUNCTIONS

In recent years, interest in the field of molecular electronics has been growing [13]. Much of the excitement has been driven by results obtained in clever transport measurements of small numbers of molecules, such as the pioneering work measuring self-assembled monolayers (SAMs) using a mechanical break junction [14]. However, a need remains for a technique capable of obtaining rapid, reproducible transport data of metal-SAM-metal junctions with nanoscale contact areas. We have developed an adjustable-electrode technique [15] capable of achieving aggressive contact areas, which differs from present-day techniques in that it relies primarily on the micromachining processes of the semiconductor industry and offers the potential for scalability.

The primary component of the technique is the silicon knife-edge structure shown in Figure 3-5. It is fabricated from a wafer of crystalline silicon and includes four electrically isolating standoffs. Measurements are performed using a two-chip set. The top chip is rotated perpendicular to the bottom chip in such a way that all four standoffs are aligned and the top chip rests face down on the bottom chip with the two gold-coated knife-edge probes facing one another. The standoffs are patterned ~100 nm higher than the knife edges, thus creating a ~200-nm gap between the crossed edges. Pressure is applied to the top chip, and this bends the silicon substrate thereby closing the gap between the probes. Prior to assembling the two chips, one or both knife edges are coated with the SAM materials to be tested. Conductivity measurements are taken as pressure is applied to the top chip, and the formation of a metal-SAM-metal junction is marked by an increase in the conductance across the gap. The process is repeated by translating one chip with respect to the other such that a new junction is formed between the probes. In this way multiple measurements can be performed with the same SAM layer and a given chip set.

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*Author not at Lincoln Laboratory.

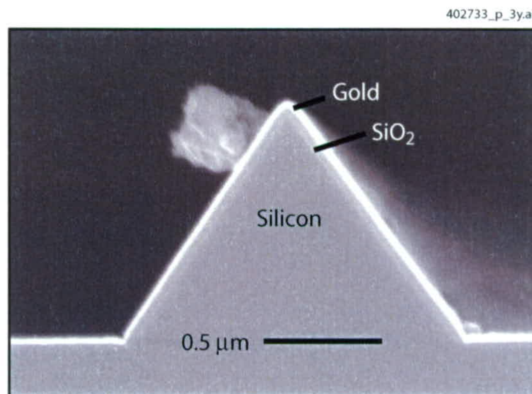

Figure 3-5. Cross-sectional scanning electron micrograph of a completed knife edge. (Some debris from the cleave is visible.)

Initial conductivity data for alkanethiol monolayers of different lengths are displayed in Figure 3-6(a). These data were recorded using a force on SAM, F_{SAM}, estimated [15] to be the minimum achievable with this technique (~20 nN). The initial resistance, derived from the linear part of the current-voltage (I-V) curves (below ~500 mV), varies by 3 orders of magnitude as the chain length is increased from C8-thiol (1.4 nm, 21 MΩ) to C14-thiol (2.2 nm, 15 GΩ). The C8-thiol measurements were repeated ten times on the same electrode set, and a histogram of the initial resistances is included in the inset of Figure 3-6. The resistance is tightly clustered about 20 MΩ (±2 MΩ) with one outlier at 5 MΩ. Data for the biphenyl dithiol (BPDT) monolayer (0.4 MΩ) are shown in Figure 3-6(b). No hysteresis was observed for any of the SAMs measured.

The effects of an increased F_{SAM} were investigated using $[CH_3(CH_2)_{10}SH]$ (C11-thiol) monolayers. After initial contact, I-V behavior was monitored while the force on the SAM was increased incrementally until SAM breakdown, as shown in Figure 3-7. Upon initial contact, I-V curves generally equilibrate over ~1 min to a less conductive state, as seen in the inset of Figure 3-7(a). Subsequent addition of incremental pressure requires only ~10-s equilibration. However, this time will increase if the pressure increment is increased. By using an incremental increase in pressure and allowing the system to fully equilibrate upon each pressure change, it was found that the initial resistance of the C11-thiol decreased exponentially with applied force [Figure 3-7(a)], as has been observed previously in alkanethiols [16]. As the two electrodes were brought into closer contact [Figure 3-7(a)], the resistance decreased by approximately a factor of 6. Using our measured [15] value of the substrate spring constant, k_{chip}, and approximating the SAM response as linear until breakdown, we estimate the vertical deflection in Figure 3-7(b), which at breakdown is 1 nm. By comparison, the monolayer thickness of C11-thiol (30° tilt) is 1.6 nm.

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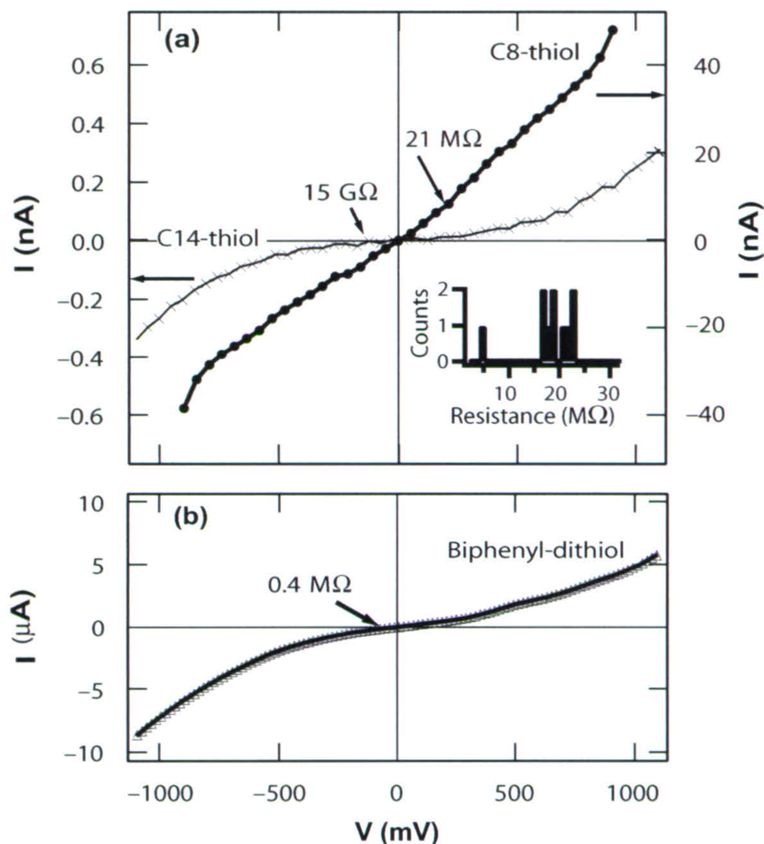

Figure 3-6. Current-voltage (I-V) characteristics for metal-SAM-metal junctions of different thicknesses: (a) C8-thiol SAM and C14-thiol SAM and (b) biphenyl dithiol SAM. The inset in (a) shows the distribution of initial resistance for ten separate C8-thiol junctions.

The electrically induced breakdown voltages (BDVs) of the insulating alkanethiols under equilibrium conditions and using a minimum F_{SAM} are shown in Figure 3-8. The BDV increases with increasing chain length, from 2.1 V for the C8-thiol to 2.9 V for the C14-thiol. In addition to these monolayer measurements, we demonstrate the amenability of the technique to bilayer junctions by coating both the top and bottom electrodes with C8-thiol. The 4-V BDV of these bilayers is roughly double that of the C8-thiol monolayer. The BDVs could be reduced from the values obtained at minimum F_{SAM} either by increasing F_{SAM} or by collecting data immediately after initial contact, thus not allowing the SAM to fully equilibrate (adiabatic data). Surprisingly, these effects were comparable in magnitude, decreasing the BDV

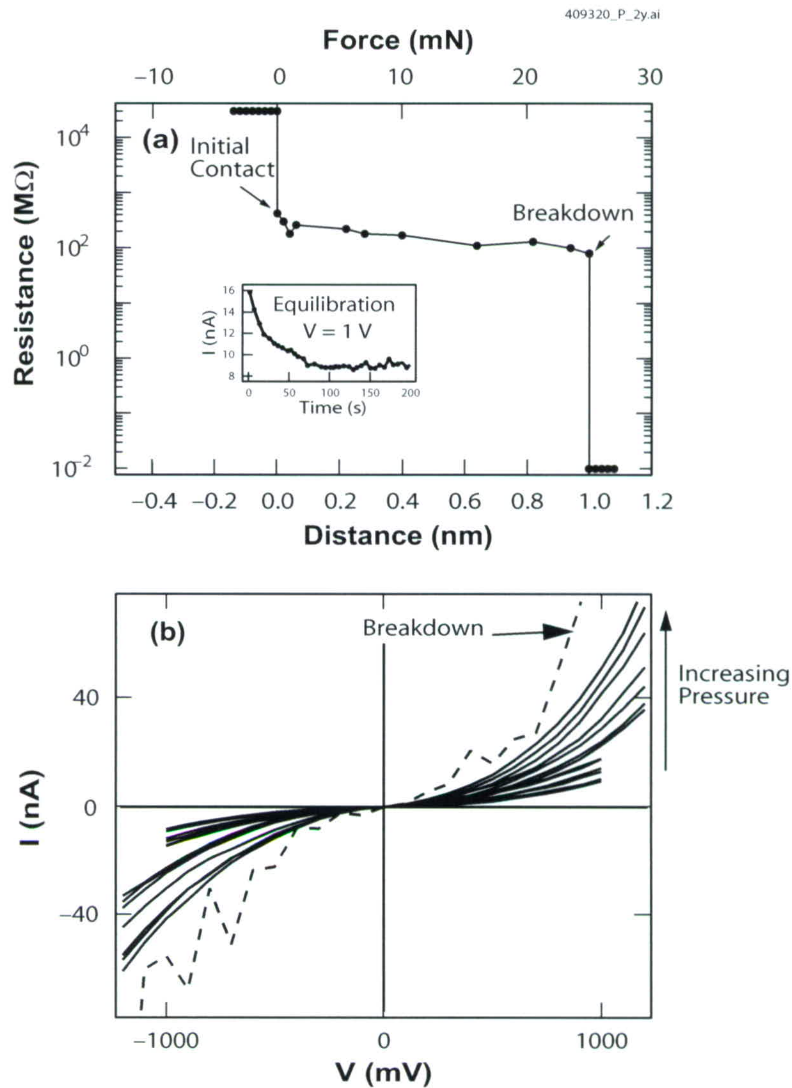

Figure 3-7. (a) Resistance of C11-thiol SAM as a function of vertical displacement of the top contact, estimated using $k_{chip} = 2.5 \times 10^7$ *N/m, and (b) I-V curves from which the resistances were derived. In (a), zero displacement represents the point at which the top chip initially contacts the SAM, the top axis is the force applied to the top chip after contact, and the inset shows the equilibration of the current under an applied voltage of 1 V after initial contact. Note that the system was allowed to equilibrate before each of the I-V curves in (b) was measured.*

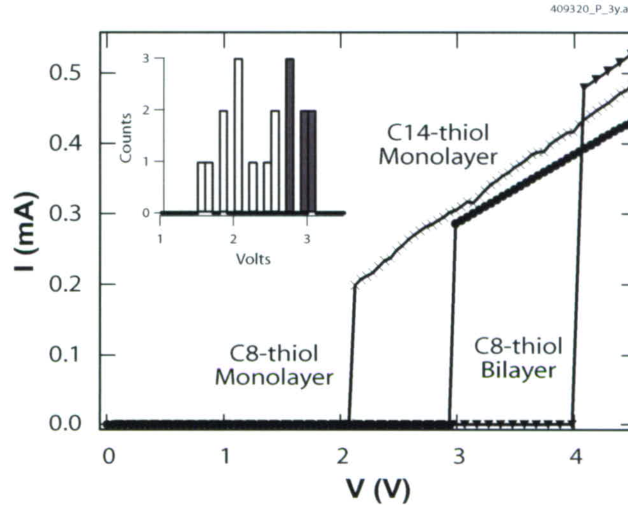

Figure 3-8. Breakdown I-V curves for monolayer and bilayer SAM junctions. For the bilayer measurements SAM was grown on both chips. The inset is a histogram of C14-thiol breakdown voltages, solid bars correspond to equilibrium data obtained using the minimum F_{SAM}, and open bars were obtained under additional pressure as described in the text.

by ~33%, to 1.4 V for C8-thiol and to 2 V for C14-thiol. The inset to Figure 3-8 displays a histogram of C14-thiol BDVs, with the equilibrium data (filled symbols) clustered about 3 V, and the adiabatic or increased F_{SAM} data (open symbols) spread more widely about 2 V.

Electronic transport in aliphatic alkanethiols is dominated by coherent tunneling along the molecular backbone with a negligible contribution due to interchain hopping. As a result the I-V curves are sigmoidal in shape and lack hysteresis. The initial linear regime of the I-V curves, from which resistance is derived, has been measured via other techniques to span a few hundred millivolts. Since tunneling along the backbone is the dominant transport mechanism, the initial resistance R increases exponentially with chain length as

$$R = R_0 \exp(\beta s) \tag{3.1}$$

where R_0 is the contact resistance, β is the exponential decay constant, and s is the SAM length. Experimentally determined values of β cluster near $1/CH_2$, with conductive probe atomic force microscopy (CPAFM) studies [17] yielding a value of $\beta = 1.19/CH_2$, where CH_2 refers to the length of a methyl group. Our data, shown in Figure 3-6, display not only the expected sigmoidal shape and lack of hysteresis, but also a linear region spanning the expected voltage range. Additionally, the changes in our measured resistances as a function of alkanethiol chain length (15 GΩ for C14-thiol as compared to 21 MΩ for C8-thiol) are consistent with an exponentially increasing resistance with $\beta = 1.1/CH_2$.

Our measurements of the aromatic dithiolated BPDT are perhaps best compared to the break junction measurements of Reed et al. [14] on the related 1,4-dithiol benzene in which, similar to our measurements, contact was made between an Au lead and the exposed thiol of a SAM adsorbed to a second Au lead. Reed et al. observed a slightly asymmetrical and sigmoidal I-V curve. Our measurements of BPDT reveal a sigmoidal curve and a similarly slight asymmetry. The small asymmetry in the I-V curves for the symmetric BPDT molecule may be the result of an asymmetry in the two contacts as has been speculated [18] in the break junction measurements of 1,4 dithiol benzene. Thus, the consistency of our transport data with previous measurements of similar SAMs clearly demonstrates that dry contacts can be achieved with the top electrode for both the monothiol SAMs (physical contact between top electrode and the inert methyl tail) and dithiol SAMs (chemisorption to both electrodes).

Given the negligible interchain hopping among alkanethiols, we assume the junction resistance scales inversely with contact area. We thus estimate our electrical contact area by comparing our measured resistances to similar alkanethiol measurements, using CPAFM [19], from which a resistance per area can be derived for a given alkanethiol. In order to make an appropriate comparison we use data in which the applied forces are comparable to our estimated F_{SAM} of 20 nN. Based on these comparisons, we estimate contact areas of $(23 \pm 1\ \text{nm})^2$ for the C8-thiol data with an outlier at $(47\ \text{nm})^2$. The C11-thiol data (400 MΩ at the minimum F_{SAM}) and the C14-thiol data yield $(9\ \text{nm})^2$ and $(35\ \text{nm})^2$, respectively. These data are consistent with our expectations based on microscopy of the electrodes [20].

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4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

4.1 DESIGN OF A FIELD-DEPLOYABLE SAMPLE-PREPARATION CARTRIDGE FOR USE IN PCR ANALYSIS

A version of the sample-preparation cartridge LiNK (Lincoln Nucleic acid Kit) has been developed customized for use in rapid, polymerase chain reaction (PCR) analysis of DNA. While sensitive and accurate detection of biological agents, excluding toxins, is currently done by PCR analysis, many PCR analysis instruments are too slow, bulky, and complicated for use in the field. Moreover, field samples can contain PCR inhibitors and be difficult to transport. The RAZOR instrument (Idaho Technology) for PCR analysis addresses the first set of concerns, and our customized cartridge (LiNK 2.0) addresses the second set. In combination, the RAZOR and LiNK 2.0 offer the capability to collect, purify, and analyze samples in the field, with a total processing time <40 min.

A benchtop protocol, called SNAP (Simple Nucleic Acid Prep), was developed previously at Lincoln Laboratory for purification of DNA from environmental samples, and aspects of the SNAP protocol were then packaged into an easy-to-use sample-preparation cartridge, LiNK 1.0 [1]. The LiNK 1.0 enables sample collection followed by either immediate extraction of benchtop PCR-compatible DNA or long-term DNA stabilization. The LiNK 1.0 consists of modified COTS components, shown in Figure 4-1, and incorporates a chemically treated paper that stabilizes DNA while killing vegetative bacteria and viruses. The cartridge has been tested successfully with a wide variety of samples, including environmental, medical, and food samples. The basic operational characteristics of the LiNK 1.0 are shown in Figure 4-2.

The LiNK 2.0 was developed to be compatible with the field-deployable RAZOR real-time PCR instrument. A key feature of the RAZOR is its quick processing time. Since the RAZOR processes samples in 30 min or less, the LiNK 2.0 processing time had to be significantly shorter than that to maintain the advantage of rapid analysis. Another characteristic of the RAZOR is its vacuum-sealed pouch, shown in Figure 4-3. The pouch contains four loading ports, each of which is designed to draw in ~0.4 mL of fluid. Since the sample loading is driven by the vacuum in the pouch, the vessel that is used to transfer sample into the pouch must accommodate the loss of sample volume either by reducing its internal volume or by venting to atmosphere. To minimize risks of contamination of either the sample or the user, the option of venting to atmosphere was eliminated, leaving internal volume adjustment as the requirement. If such adjustment does not occur, the internal pressure of the pouch and transfer vessel will begin to equilibrate, with the net result that not enough fluid will leave the transfer vessel and enter the pouch. A syringe provided the simplest solution to this design requirement, as the plunger could simply be moved down to reduce the internal volume. Other approaches, such as flexible walls or accordion-style transfer vessels, were considered but judged to be needlessly complicated and to have an unacceptably high risk of failure.

Figure 4-1. LiNK 1.0 components.

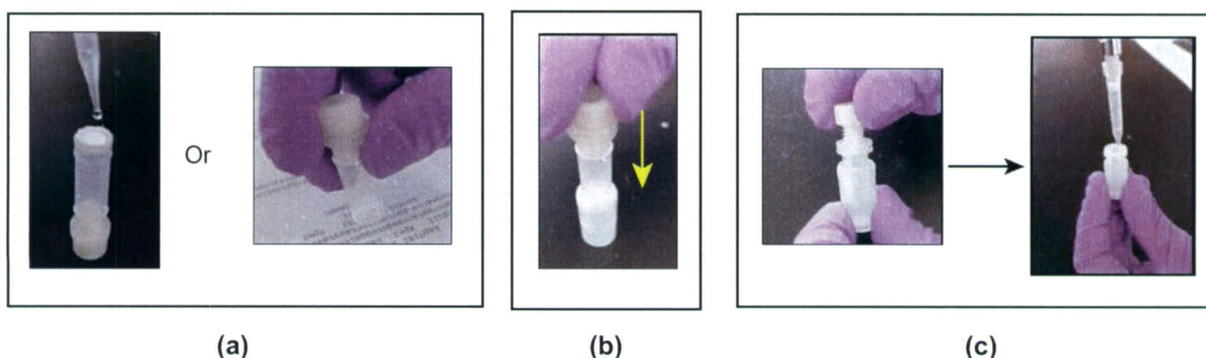

Figure 4-2. Operation of LiNK 1.0: (a) Sample is applied to the chemically treated paper on the end of the LiNK inner plunger/body and allowed to sit for 5 min while chemicals act on the sample, (b) inner plunger is inserted into the outer cylinder loaded with 0.175 mL of elution fluid, and (c) the lid of the LiNK 1.0 is removed and the eluate extracted. The total process time is 6 min.

For optimal field deployment, reagents are lyophilized inside the RAZOR pouch, as shown in Figure 4-3, so we needed to keep salt concentration in LiNK 2.0 sample eluate below inhibitory levels. Earlier work with ABI TaqMan reagents used in a benchtop real-time PCR instrument (ABI 7700) showed that PCR results were inhibited at chaotropic salt concentrations higher than 20–30 mM, as seen in Figure 4-4; a similar experiment was performed with the RAZOR vacuum pouches. To generate sufficient LiNK eluate for these experiments, LiNK 1.0 cartridges were processed using nuclease-free water as both sample and elution fluid. After processing, the eluates were combined into a single tube and the chaotropic salt concentration measured using a conductivity meter. To prepare samples, a 1:10 dilution of *Bacillus thuringiensis kurstaki* (Btk) culture was made into deionized water. This solution was used to make a $1:10^5$

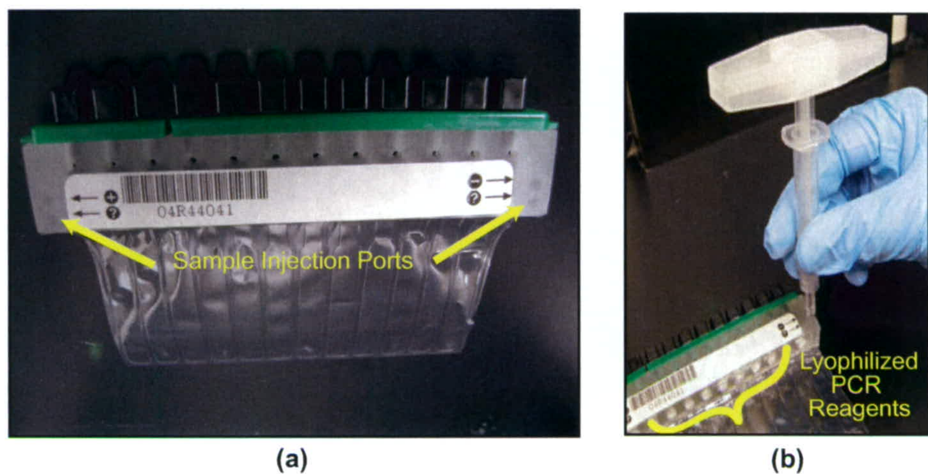

Figure 4-3. (a) Vacuum-sealed pouch with thin flexible lower section for insertion into the RAZOR, and (b) loading of sample into a RAZOR pouch using a controlled-aspiration syringe with blunt cannula tip and customized handle.

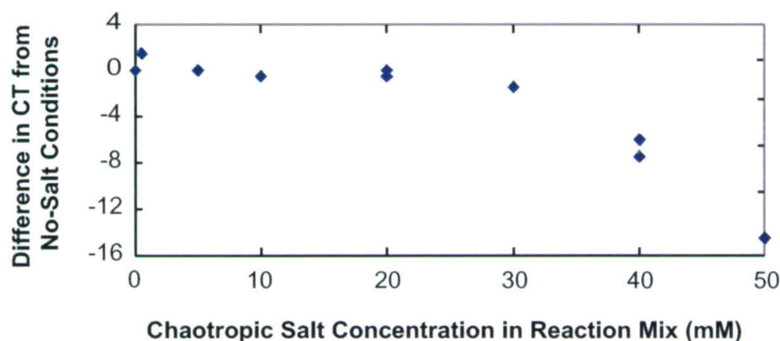

Figure 4-4. Effect of chaotropic salt on polymerase chain reaction (PCR) analysis. Samples were prepared by diluting vegetative Ba culture 1:100 in water containing a range of chaotropic salt concentrations and run on a benchtop PCR instrument. The cycle threshold (CT) was measured at a normalized fluorescence level of 0.1.

dilution into both water and LiNK eluates. An inhibitory effect was seen at a salt concentration of 55 mM, as shown in Figure 4-5(a). At 22 mM, the cycle threshold (CT) actually dropped slightly relative to the lower-salt samples, indicating earlier detection. A later experiment clarified these results and found that at a salt concentration of 40 mM no PCR inhibition was observed for the RAZOR, as shown in Figure 4-5(b). Based on these results, the salt concentration in the LiNK 2.0 eluate had to be kept at or below 40 mM.

Another requirement of LiNK 2.0 was that it eliminate or at least minimize bubbles in sample eluate. Like the vast majority of real-time PCR instruments, the RAZOR tracks the degree of target amplification

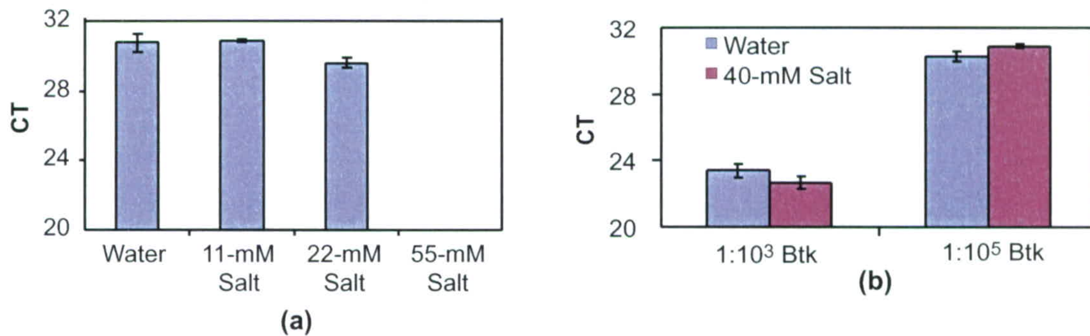

Figure 4-5. (a) Effect of chaotropic salt concentration generated by LiNK 1.0 on RAZOR analysis of vegetative Bacillus thuringiensis kurstaki (Btk) and (b) effect of chaotropic salt and target concentration on RAZOR detection of vegetative Btk. Note that the difference between water and 40-mM salt in (b) is not significant for either concentration. CT values are taken from RAZOR.

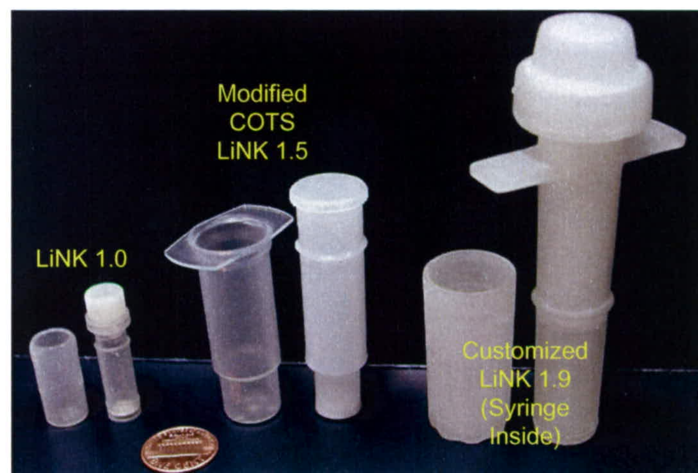

Figure 4-6. Evolution of LiNK cartridge.

by monitoring the sample chamber optically and measuring the amount of fluorescence generated during each PCR cycle. Therefore, anything in the sample chamber that interferes with this optical interrogation could affect the signal. Experimental evidence confirms that the presence of bubbles in a RAZOR pouch sample chamber can lead to erroneous false positives and false negatives.

Several different designs were proposed before agreement was reached on the basic features of LiNK 2.0. Initially an intermediary device was suggested, composed primarily of commercial off-the-shelf (COTS) components, to provide an immediate, if nonideal, solution to the need for RAZOR-compatible

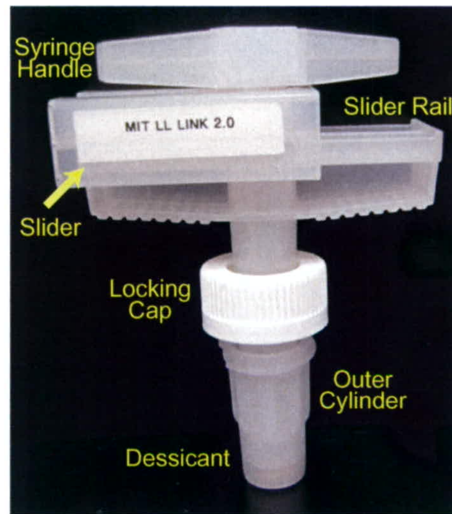

Figure 4-7. LiNK 2.0 prototype.

(a)

(b)

Figure 4-8. (a) LiNK 2.0 kit components including (left) a dropper bottle containing PCR-grade water and (right) the outer cylinder filled with elution buffer, and (b) LiNK 2.0 transport pouch with labels on either side providing instructions for use and space to record tracking information.

sample preparation devices. This device, the COTS LiNK 1.5, which is shown in Figure 4-6, was larger and easier to handle than the LiNK 1.0 and could provide a sufficient volume of RAZOR-compatible eluate, but was far from ideal in terms of operability and did not include a sample-transfer device to load liquid into the RAZOR pouch.

The final LiNK 2.0 design could not be prototyped from COTS or hand-machined components. It included some COTS components, such as the 0.5-mL aspiration syringe and accompanying blunt cannula tip, but consisted primarily of custom-designed components injection molded from medical-grade polypropylene. The key features of LiNK 2.0 are labeled in Figure 4-7. The kit for field use is shown in Figure 4-8(a), and the pouch for transport before and after LiNK 2.0 processing is shown in Figure 4-8(b).

Laboratory tests of LiNK 2.0 prototypes have demonstrated its compatibility with RAZOR.

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5. ADVANCED IMAGING TECHNOLOGY

5.1 DEVELOPMENT OF A LARGE-AREA, HIGH-FRAME-RATE CHARGE-COUPLED DEVICE WITH BLOOMING CONTROL

Technical demands for improved performance of electronic imagers have prompted the development of a large-area, high-frame-rate charge-coupled device (CCD), incorporating back-side illumination and blooming control. A diagram of the imager is shown in Figure 5-1. Similar to the imager developed for the University of Hawaii consortium [1], it comprises an array of 2048 × 4100 pixels, each 15-μm square, and can be subjected to back-side illumination [2]. It also incorporates blooming control [3], so that a large-intensity signal is prevented from spilling (blooming) down the column of the CCD. To increase the frame rate of the device, four two-stage output ports are incorporated along the serial register at the bottom of the device; this allows the eight million pixels in the imaging array to be read out several times a second, while preserving low-readout-noise characteristics [4]. The device may also be read out from only two ports as the serial register allows for bidirectional clocking. The layout of an individual output is shown in Figure 5-2, where the first- and second-stage output field-effect transistors (FETs) are arranged in a source follower configuration, with the constant-current-source FET acting as the load of the source follower. The source of the second-stage FET is connected to the gate of an off-chip junction field-effect transistor (JFET), in a second source follower arrangement.

Operation of the CCD has indicated a read noise of 11 e^- at 1-MHz clock rate of the serial register and 13 e^- at 4 MHz. The quality of the images obtained is excellent, as shown in Figure 5-3; the images were captured while integrating the CCD in the dark at a temperature of –60°C for ~100 s. The bright streaks and pixels are due to cosmic rays passing through the device during this integration period. The bright glow near the serial register is due to power dissipation in the output transistors and may be minimized by decreasing the drain voltage of those transistors or only operating them while clocking out the serial register. The absence of other defects attests to the quality of the device.

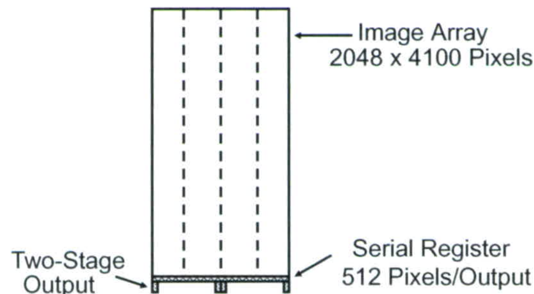

Figure 5-1. Diagram of large-area, high-frame-rate charge-coupled device (CCD) with back-side illumination and blooming control.

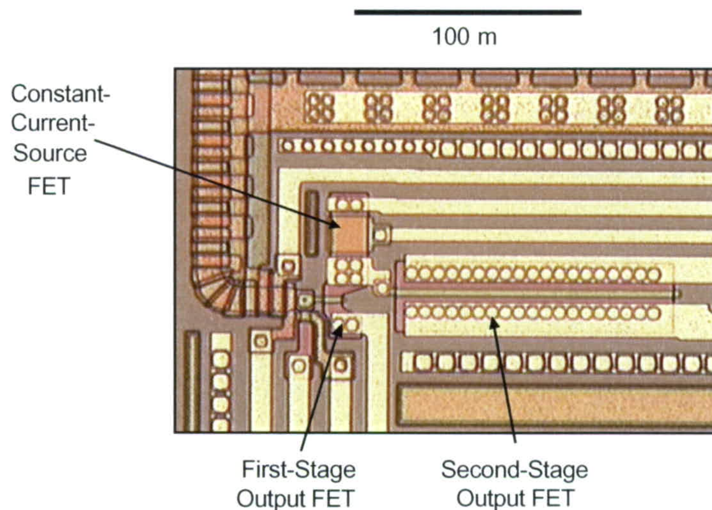

Figure 5-2. Layout of an individual two-stage output.

Figure 5-3. Dark-current image of large-area CCD.

In the first wafer lot of these devices, the charge-transfer efficiency (CTE) of the devices was found to depend markedly on the transfer time of the rows. Transfers at times <24 μs would cause an abrupt fall in CTE beyond certain rows (typically 1500–3500 rows away from the serial register) of the device. The problem did not appear in the serial register CTE, even for transfer times of 250 ns. Probing the voltage drop along the buslines driving the rows suggested a resistance-capacitance (RC) time constant effect, which limited the response speed of the rows to their driving clocks. Modeling of the capacitance and resistance of the rows, both in SPICE and analytically, and their buslines confirmed this hypothesis. As a consequence of these measurements and models, the second lot of devices had additional metal lines directed from the clock to the top row of the CCD, creating a current path parallel to the buslines. This

(a)

(b)

Figure 5-4. Improvement in charge-transfer efficiency shown by comparison of Fe^{55}-induced charge packets in (a) CCD from 47lot1 and (b) CCD from 47lot 2.

design modification decreased the effective resistance of the clocklines and the associated RC time constant, allowing the voltage potential in the CCD array to respond to the driving clocks. Some improvement could be made by increasing the clock swings for the individual phases, but this limited the flexibility of the drive electronics, a problem not encountered when additional metal is added to the buslines.

One of the techniques used to measure CTE is to expose the device to a radioactive Fe^{55} source. The x-rays emitted by this source create a charge packet containing 1620 e^-, when absorbed in a pixel; counting the number of electrons when that pixel is read out allows the calculation of CTE since the position of the pixel is known. A map of these Fe^{55} x-ray hits in a 47lot1 device is shown in Figure 5-4(a), where the row transfer time was 12 μs. The serial register is to the left of this sector (512 columns × 4100 rows), and it is apparent that the images of the charge packets fade into the background about two-thirds of the way from the left to the right, or at about row 3500. Close examination of this image indicates the charge packets become elongated, because of the poor CTE, at high row numbers.

Figure 5-4(b), on the other hand, displays an image from a chip produced in 47lot2, with the extra metal paralleling the buslines. Here the Fe^{55} charge packets remain distinct and above background from the serial register to the far right of the image, corresponding to row 4100, indicating excellent CTE across the entire image. Similar results were found in 47lot2 devices using row transfer times <10 μs.

In summary, a new large-area CCD imager has been fabricated and has demonstrated excellent performance. Further tests are under way to determine its performance in the thinned, back-side-illuminated configuration and its ability to suppress blooming of large charge packets.

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6. ANALOG DEVICE TECHNOLOGY

6.1 GROUND-TO-UAV ULTRA-LOW-POWER COMMUNICATIONS LINK

A study has been completed of an ultra-low-power communications link between the ground and an unmanned aerial vehicle (UAV). The prime figure of merit in the study is the energy required to successfully transmit a data bit to the UAV. The various contributions to the energy per bit were tracked in the calculation. The energy contributors consisted of packetization and forward error correction coding, modulation, and amplification. The goal of the study was to understand the impact on the energy per bit from the various implementation options, such as carrier frequency, modulation option, and choice of coding. We also assessed the potential benefits of extending the design techniques emerging for the commercial low-power wireless field for the ground-to-UAV link.

A first-pass system design was developed in the study to more accurately assess the energy contributors and the implementation options. A high-level data link control (HDLC)-like layer was selected for its simplicity and low overhead. Turbo coding is the logical choice for the forward error correction coding. M-ary frequency shift keyed (FSK) modulation was selected for its power-efficient implementation and reduced transmit signal level requirements for demodulation, i.e., the energy per bit to noise power ratio, E_b/N_0. The channel burst rate is variable over the range from 100 kbps to 10 Mbps. It was observed that the link should have the ability to adapt the modulation order, burst rate, and perhaps forward error correction (FEC) code rate to adjust the link parameters for maximum data throughput, thereby minimizing wasted energy in excess link margin.

The first-pass system design was also used to assess the potential for power reduction using advanced technology. Estimates for the energy contribution for the various functions were made for three different technology levels. The estimate for the first level, designated commercial off the shelf (COTS), was made using existing component specifications, such as power consumption, clock rate, and gain, obtained in catalogs or through measurement. The estimate for the second level, designated application-specific integrated circuit (ASIC), was made using performance calculations for ASICs based on a standard cell design for the digital aspects of the system and a low-risk approach (baseband modulation upconverted to RF with a mixer) for the analog aspects. The estimate for the third level, designated ultra-low power (ULP), was made using performance calculations for ASICs with advanced design techniques. This entails subthreshold designs for the digital portions of the system and low-power wireless approaches for the analog portions. The results of the study show that the opportunity for power savings is significantly greater with the ULP approach than with techniques currently employed by the DoD.

To facilitate bursty communications, it is common practice to encapsulate the data stream in packets. The primary function of the packet is to signal the beginning and end of data. Other functions often included in the link layer packet are addressing or using identifiers for the intended recipient, error detection via a cyclic redundancy check (CRC), and link management. The envisioned link layer is a

simplified version of the HDLC protocol. The energy per bit calculation assumed the HDLC protocol added a 15% overhead to the number of information bits. Note that the HDLC beginning and end of data flags are different from the preamble that is sent to establish the link at the physical layer and that typically more than one HDLC packet would be sent during a given connection.

FEC coding is used to increase the probability that the packet will be correctly received at the far end of the link. There are many types of FEC coding, but they share the property that they reduce the overall energy spent to transmit the information despite the fact that more bits (information + parity) are sent. This happens because the FEC reduces the E_b/N_0 needed at the far end of the link to still correctly receive the data. This reduction is often referred to as coding gain. In the past 10 years, a family of codes, called turbo codes, have been developed that greatly improves the performance of communications links. The use of these codes is incorporated into the first-pass system design. The energy per bit cost to implement the code is modest and the coding gain for M-ary FSK is 4 dB or more, depending on modulation order and channel conditions, for rate ½ codes [1].

The estimates of the energy per bit to implement the HDLC packetization and turbo coding are given in Table 6-1 for the three technology levels. For this estimate a field-programmable gate array (FPGA) based solution was assumed for COTS, a standard-cell ASIC design was assumed for ASIC, and a subthreshold ASIC design was assumed for ULP. Note that the volume of data (channel bits) is increased by a factor of 2.3—15% overhead for the packetization plus 2 times for the coding—over the original data (information bits).

TABLE 6-1
Energy per Bit Estimates for Packetization and Coding

Technology	COTS	ASIC	ULP
Energy per Information Bit	47 nJ/bit	500 pJ/bit	30 pJ/bit

The digital data must be modulated onto an RF carrier for transmission from the ground to the UAV. The most common modulation approach, referred to as band-pass modulation, results in RF signals with relatively small fractional bandwidths. A newly emerging technique, referred to as ultra-wideband modulation, does offer the promise of low-power consumption. To date, however, this modulation technique has only shown utility for short-range communication and radar (10's of meters). Further, the goal of this study is to lead to a low-power link compatible with existing RF allocations, and better with existing fielded radios. Thus, the combination of the two issues of fractional bandwidth larger than existing military ground-to-air RF allocations and the experimental aspect of the long-haul links led us not to consider ultra-wideband modulation at this time.

Instead, we focus on the more conventional modulation techniques of FSK, phase shift keying (PSK), and quantized amplitude modulation (QAM). Standard communication systems textbooks, such as Sklar [2], show that the FSK and other orthogonal modulation techniques, such as pulse position modulation (PPM), offer the possibility of smaller transmitter powers than PSK or QAM, but at the cost of

requiring larger bandwidths. Further, the power required to modulate the signal can be much smaller for FSK than for the other techniques. Thus, we have selected FSK modulation for the baseline system design.

We have estimated the E_b to generate the modulated signal at the desired carrier frequency. As discussed below, we are considering operation at three representative frequencies: 100 MHz, 1 GHz, and 15 GHz. The values for E_b used in the study are given in Table 6-2. These values are the estimates to produce the modulated carrier frequency as a function of channel burst rate (maximum modulation rate), carrier frequency, and technology option. We have only explored solutions that result in small fractional bandwidths; thus, we do not estimate the modulation energy for 1- and 10-Mbps burst rates for the 1-MHz carrier nor the 10-Mbps burst rate for the 1-GHz carrier. The COTS solution is based on available components or extrapolated from available components with similar specifications. The ASIC solution assumes a baseband modulator (<100 MHz) upconverted to the carrier frequency. This is the conventional approach but suffers from the inefficiencies of the mixing (upconversion) process. The values are based on extrapolations from commercially available parts and results reported in the literature. The ULP solution

TABLE 6-2
Energy per Bit Estimates for the Modulated Carrier Generation

	100 MHz	1 GHz	15 GHz
COTS Technology Solution			
100 kbps	200 nJ/bit	400 nJ/bit	22 μJ/bit
1 Mbps	-	60 nJ/bit	2.4 μJ/bit
10 Mbps	-	-	500 nJ/bit
ASIC Technology Solution			
100 kbps	50 nJ/bit	180 nJ/bit	300 nJ/bit
1 Mbps	-	25 nJ/bit	50 nJ/bit
10 Mbps	-	-	15 nJ/bit
ULP Technology Solution			
100 kbps	20 nJ/bit	40 nJ/bit	165 nJ/bit
1 Mbps	-	5 nJ/bit	40 nJ/bit
10 Mbps	-	-	5 nJ/bit

assumes indirect modulation of a voltage-controlled oscillator operating at the carrier frequency [3]. In this approach the carrier frequency is tied to a crystal oscillator reference to provide frequency stability;

however, the divide-by-n circuit in the phase-locked loop is designed to provide flexibility in several respects. First, the value of n is constantly varied using a so-called sigma-delta technique that results in fine control over the transmitted frequency. Second, the values used in the sigma-delta modulation can be adapted to overcome the distortion introduced in the phase lock loop filter, allowing for frequency excursions beyond the range typically realized for a given loop bandwidth. Third, this technique readily provides the means to adapt the modulation order and the burst rate, permitting adaptation in the channel for changing link conditions and operational scenarios.

Three representative frequencies of operation were considered. The first frequency, 100 MHz, was chosen for the foliage and building penetration properties at VHF. However, there are at least two difficulties at VHF. The first is the inefficiency of using an electrically small antenna in order to maintain reasonable proportion with both the ground sensor and the airborne platform. The second is the rather noisy ambient signal environment requiring increased transmitted signal levels to provide sufficient signal-to-noise levels in the receiver. In this work, we assumed the ambient noise level to be 15 dB greater than the thermal noise. The second frequency, 1 GHz, was chosen as the lowest frequency where the antenna and noise issues are reasonable. At 1 GHz it is possible to form a resonant antenna on the ground sensor and a moderately directive antenna, and there are portions of the spectrum where one can reasonably assume the signal environment is thermal noise limited. The third frequency, 15 GHz, was chosen because it offers the possibility of using moderately directive antennas on both the ground sensor and the platform. As will be shown below, the increased directivity of the antennas more than overcomes the inefficiencies in the modulator and power amplifiers operating at the higher frequency.

The output stage amplifier is a major source of energy consumption and, therefore, should be given careful consideration. The power efficiencies of switch-mode amplifiers, classes E, F, and others, should be used to the maximum extent possible. The power-added efficiencies (PAEs) used in the calculation are given in Table 6-3. At 100 MHz, switch-mode amplifiers are commercially available. The modest increase in efficiency with the ASIC and ULP designs is due to optimizing the design for the operating bandwidth and other parameters. At 1 GHz, switch-mode amplifiers are not yet available as COTS, and the 35% PAE

TABLE 6-3
Power-Added Efficiencies for the Output Stage Amplifier

	100 MHz	1 GHz	15 GHz
COTS	70%	35%	10%
ASIC	75%	60%	35%
ULP	80%	70%	48%

is for amplifier operation in class A-B. However, the techniques for switch-mode performance are understood and can be implemented at 1 GHz without too much difficulty, thus resulting in the relatively

high PAEs used in the ASIC and ULP technologies. The available COTS components for amplifiers at 15 GHz are rather poor, but not uncommon. There are COTS amplifiers with greater PAEs (20–30%) in a few bands at frequencies under 50 GHz with moderate market potential. Extending the switch-mode amplifier techniques to 15 GHz, however, is not straightforward. The imprecision in the transistor models and the losses in the transmission elements and in the transistors themselves make achieving PAEs greater than 50% a research endeavor. It should be possible to approach PAEs of 50% using some of the ideas from switch-mode operation, namely harmonic tuning, and given the advanced state of transistor models and computer-aided design tools.

The last aspect of the RF link considered in this study is the antenna. The carrier frequency makes a significant difference in the type of antenna that is appropriate for the ground sensor and the platform as well as the gain, as shown in the values in Table 6-4.

TABLE 6-4
Type of Antenna and Assumed Gain as a Function of Carrier Frequency

	100 MHz		1 GHz		15 GHz	
	Transmit	**Receive**	**Transmit**	**Receive**	**Transmit**	**Receive**
Size	Small Dipole	Blade	Monopole	0.22 m^2 (21-in. diam)	0.006 m^2 (3.5-in. diam)	0.07 m^2 (12-in. diam)
Gain (dB)	–3	0	3	12	15	30

The model prediction for the E_b as a function of propagation distance is shown in Figure 6-1. The calculation begins by using the standard link equation to determine the transmitter power required at the three carrier frequencies, using the antenna gains in Table 6-4, E_b/N_o required of 7 dB (8 FSK with turbo coding in a Rician, Kr = –10 dB, channel [4], and 3 dB of link margin). The transmit power is divided by the amplifier PAE and multiplied by the bit period to determine the amplifier contribution to E_b. Next, the contributions to E_b for the packetization and coding and the modulation are taken from appropriate entries in Tables 6-1 and 6-2. For clarity, Figure 6-1 shows only the results for the COTS and the ULP cases. Further, the values in the curves are for channel bits, that is, for the bit actually transmitted, which could be an information, packetization overhead, or parity bit. This is done for easier comparison to COTS wireless systems that quote energy per bit in this manner. Table 6-5, however, shows the tabulation of the E_b components for all three technology realizations for the slant range of 100 km. It also shows the energy per bit for the source (information) bits. Each source bit translates into 2.3 channel bits.

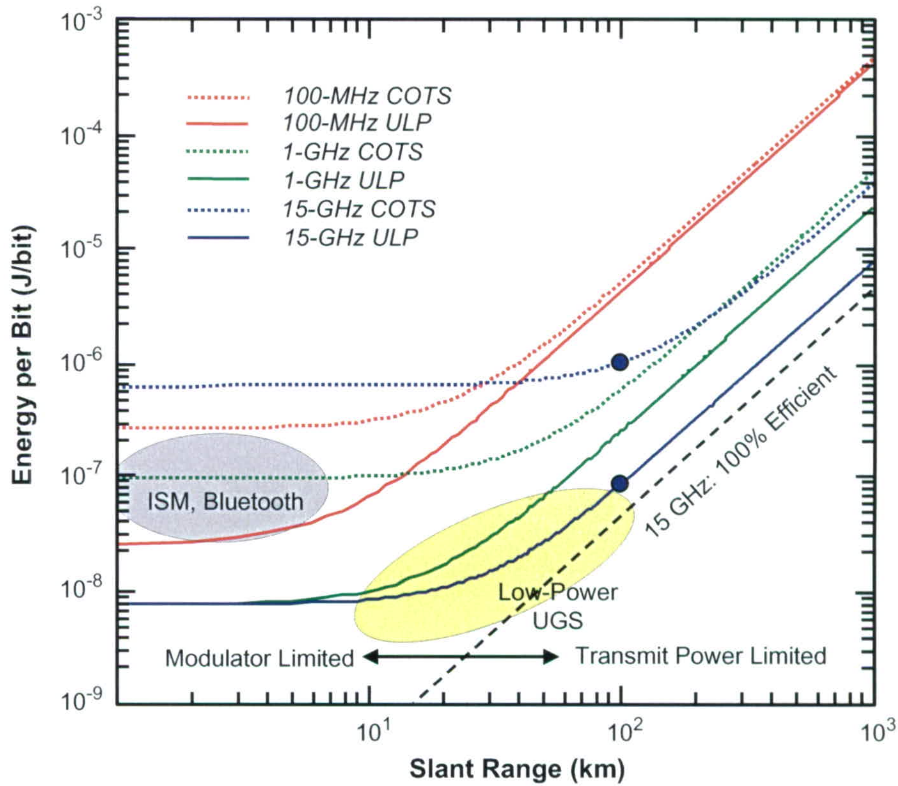

Figure 6-1. Energy per bit as a function of slant range for three carrier frequencies and two technology realizations. The values shown by the curves are the energy per bit for the channel bits.

TABLE 6-5
Summary of Energy per Bit Components for a Slant Range of 100 km at 15 GHz*

	COTS (nJ/bit)	ASIC (nJ/bit)	ULP (nJ/bit)
Packetization and Coding	47	0.5	0.03
Modulation	1150	35	12
Amplification	690	230	144
Total	1887	265	156

*The values shown are the energy per bit for the source bits.

Several observations need to be made about Figure 6-1. The E_b values for short slant ranges (left) are primarily composed of modulator energy, whereas the E_b values for long slant ranges (right) are primarily composed of transmitter energy. The potential for significant energy savings with the ULP technology realization is clearly seen (solid lines). Finally, the larger antenna gain at 15 GHz more than compensates for the reduced efficiencies of the electronic components, making it an attractive solution.

In summary, we have completed a system-level study to assess the relative energy contributions of the packetization and coding, modulation and carrier generation, and output stage amplification to the total E_b required to close a link from a ground sensor to an overhead UAV. We have also assessed the potential for decreasing E_b using advanced technology. It was determined that significant opportunities exist to lower E_b if advanced technology is applied to the modulator/carrier generation and the output stage amplifier. We will be pursuing these opportunities in newly started programs.

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7. ADVANCED SILICON TECHNOLOGY

7.1 HIGH-FREQUENCY CHARACTERIZATION OF Si-MOSFET GATE RESISTANCE

With aggressive gate scaling, silicon metal-oxide semiconductor field-effect transistors (MOSFETs), have pushed the cutoff frequency f_T to the 200-GHz range and are becoming more widely used in high-speed analog and RF circuits. Traditionally used for digital circuits where the effect of gate resistance is small, current Si MOSFET models do not have an adequate gate-resistance component that can accurately represent the device characteristics at high frequencies. As a result, either the gate finger width is based on empirical data or the narrowest possible gate is simply used to minimize the gate resistance effect [1].

The purpose of this work is to better understand how the gate resistance affects device performance at high frequencies and to provide a guideline on modeling the gate resistance. Our approach is to fabricate simplified MOSFET-like test devices to characterize the effect of gate resistance and to compare these with MOSFETs. The behavior of the gate structure is explained with proposed equivalent circuits that can best match the measured results.

MOSFETs and gate test structures were fabricated on silicon-on-insulator (SOI) substrates. As shown in Figure 7-1, the gate test structure is basically a single-gate *n*-MOSFET with source and drain connected together to ground, and it operates as an MOS capacitor. The capacitor has either a metal T-gate or a conventional silicided poly-Si gate, where there is no metal overlay. The poly-Si gate length is 0.18 μm and the T-gate length is 0.3 μm. The cross section of the T-gate is also shown in Figure 7-1, and details of T-gate fabrication have been previously reported [2].

The scattering (S) parameters were measured using a network analyzer from 2 to 40 GHz with on-wafer RF probes. The gate is biased at 1 V so that there is an inverted electron layer under the gate oxide. From measured DC and S parameters of the two-port gate line, the estimated sheet resistances are 29 and 0.33 Ω/sq for the silicided poly-Si gate and the metal T-gate, respectively. The resistance of a single contact from metal-1 to the silicided gate is ~10 Ω. The total contact resistance between the metal T-gate and the poly-Si is negligibly small because a continuous contact is made along the entire gate.

Figure 7-2(a) shows plots of measured S parameters of a 20-μm-wide one-port capacitor on a Smith chart. The measured data of the T-gate capacitor follows a constant-resistance circle over the frequency range, indicating the capacitor can be represented by a simple series resistance-capacitance (RC) circuit, shown in Figure 7-2(b). The R_g is the gate resistance and R_s is the source resistance of the MOS capacitor. A good match between the measured and calculated data is obtained. The gate capacitance of 37 fF in the equivalent circuits is slightly higher than the 32 fF calculated based on the 4-nm gate oxide and 0.18-μm gate length as a simple parallel-plate capacitor. The higher capacitance could be caused partially by the parasitics of the overhung metal T-gate. Since for a one-port capacitor, R_g and R_s are in series, the simulated results are affected by the sum of the two. In our simulation, the R_g is estimated based on the

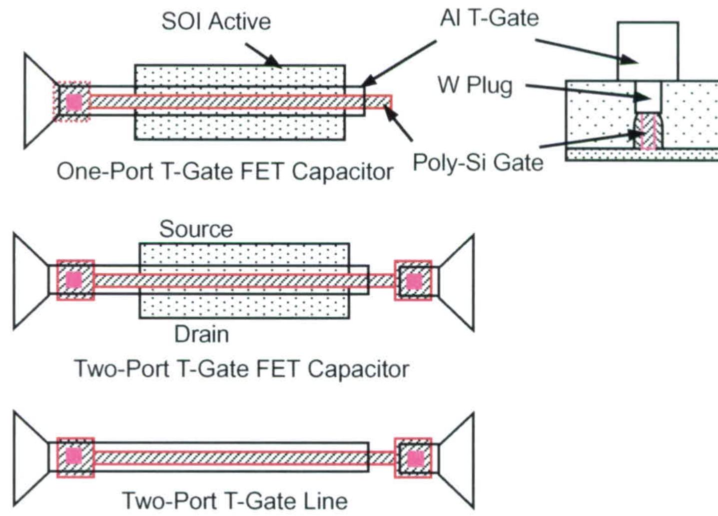

Figure 7-1. Gate test structures used for RF characterization. The metal T-gate contacts through a metal-filled slot on top of the silicided poly-Si gate. The source and drain are connected to the ground during the measurement.

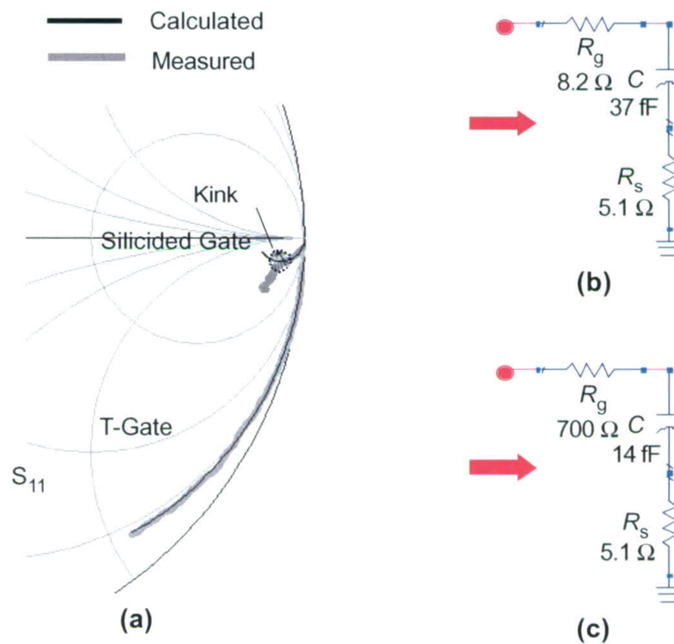

Figure 7-2. Measured results of 20-μm-wide MOS capacitor: (a) input S parameters, (b) series RC equivalent circuit of the T-gate capacitor, and (c) series RC equivalent circuit of the silicided-gate capacitor. In (a), the wide curves are measured results and the narrow curves simulated results using the equivalent circuits shown.

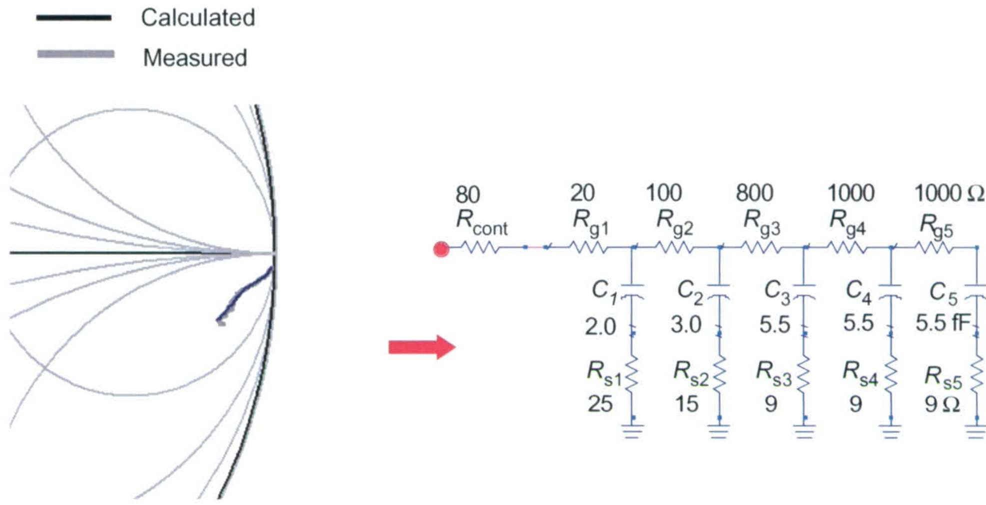

Figure 7-3. S-parameter plots and RC network equivalent circuit for 20-μm-wide MOS capacitor with silicided gate shown in Figure 7-2(c). R_{cont} is the contact resistance, including the gate resistance between the contact and the gate region on top of the SOI.

sheet resistance data and the physical dimensions. The R_s is then varied to optimize the data fit. Not shown here, good data fit was also obtained for capacitors with gate widths of 10 and 50 μm, and the values of components in the equivalent circuit scale with the gate width W as $R_g \propto W$ and $R_s \propto 1/W$.

As shown in the Smith chart of Figure 7-2(a), characteristics of the capacitor with silicided gate are very different. At low frequencies, it generally falls on a constant resistance circle, characteristic of a series RC circuit. At approximately 12 GHz, the curvature of the S_{11} plot changes, and it follows more closely a constant admittance circle at higher frequencies. Similar behavior has been observed on real transistors, and the breaking point of the curvature is referred to as the kink [3],[4].

A simple series RC circuit, shown in Figure 7-2(c), cannot produce the kink, and a good match can be achieved only up to ~12 GHz before the occurrence of the kink. The capacitance in the equivalent circuit is 14 fF, which is less than half of the 32 fF calculated. The equivalent gate resistance of 700 Ω is also smaller than the 3200 Ω estimated from the DC sheet resistance value. Smaller than expected resistance and capacitance suggest that we did not measure the entire gate capacitor at high frequencies.

It is easy to understand that with a high gate resistance the signal applied to the capacitor attenuates along the gate and the capacitance at the two ends makes different contributions to the measured S parameter. If the applied signal is reduced to zero by the resistive loss before reaching the end of the gate, part of the gate capacitance is never measured. Therefore, instead of a simple RC in series, the capacitor with high gate resistance should be treated as a distributed circuit, which can be represented by an RC network, as shown in Figure 7-3. When the frequency is low enough that the impedance of the capacitance,

$X_c = 1/\omega C$, is much higher than the gate resistance R_g, the RC network can be reduced to a simple RC in series. With increasing frequencies, X_c becomes comparable to R_g, and the network resembles more of a parallel RC in nature. The transition from series to parallel RC coincides with the kink observed in measured S parameters.

The distributed gate capacitor can be more accurately represented with an increasing number of sections in the RC network. In Figure 7-3, only five RC sections are used to represent the same 20-μm-wide silicide gate shown in Figure 7-2, and a good match is achieved. The important result is that a multiple-section RC network can produce the behavior of matching measured S parameters with kink, which cannot be achieved with a simple series RC circuit. The kink observed for transistors has been attributed to the interaction of zeros and poles of a complex equivalent circuit [3]. It is shown here that the kink also appears in a simpler device of a MOS capacitor, and it can be simply attributed to the high gate resistance.

To understand if the observations on MOS capacitors are applicable to the transistors, *n*-MOSFETs with two gate fingers fabricated on the same wafer were characterized. The gate length is 0.18 μm, and the widths of the gate finger are 10 or 20 μm. As shown in Figure 7-4, kinks are observed in both S_{11} and S_{22} plots for FETs with the silicided gate but not for FETs with the T-gate. For the 2 × 20-μm-wide FET, estimated kink frequency is 11 GHz for both S_{11} and S_{22}. Higher kink frequencies of 30 and 25 GHz for S_{11} and S_{22}, respectively, are measured for the 2 × 10-μm-wide FET. The large resistance of the silicided gate significantly increases both the loss and delay. For instance, if the phase difference is to be kept below 1/16 of a wavelength throughout the gate, the highest operating frequency is limited to 15 GHz for the 10-μm gate and to 5 GHz for the 20-μm gate. Note that although paralleling multiple gate fingers can lower the apparent overall gate resistance, the phase constraint imposed on each gate finger remains the same.

We assumed that the input of an FET is simply R and C in series, a reasonable approximation below the kink frequency, and the RC values can be obtained from the real and imaginary part of Z_{11}, which is converted from measured S parameters. The resulting R and C values as a function of frequency for various FETs are plotted in Figure 7-5. The resistance of T-gate FETs is approximately 10 Ω and increases slightly with the frequency. As shown in Figure 7-5(b), the capacitance of T-gate FETs scales with the gate area and also increases slowly with frequency.

Although a much higher resistance for silicided-gate FETs is expected, a rapid decrease in values with frequency is distinctively different. The capacitance of these FETs has frequency dependence similar to the resistance. Note that, at low frequencies, both R and C of silicided-gate MOSFETs scale with the gate area. However, above certain frequencies, R and C converge to the same values regardless of the gate width.

In Figure 7-5(c), the impedance of input capacitance, $X_c = 1/\omega C$, is plotted along with the input resistance R. It appears that when the X_c becomes comparable to the resistance, to within approximately 100 Ω in both FETs, the kink occurs. It is not clear if the kink at the output is induced also by the high gate resistance, but the similar kink frequencies suggest that they probably are related.

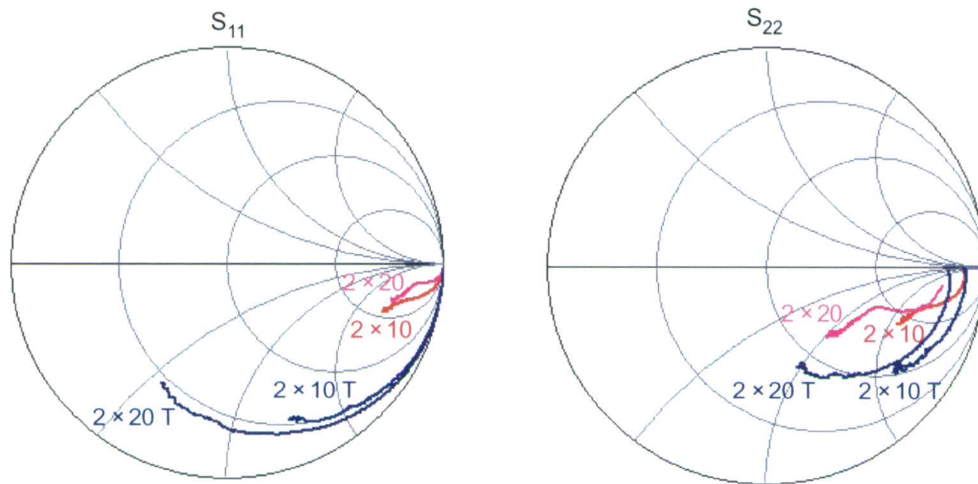

Figure 7-4. Measured S parameters of n-MOSFETs from 2 to 50 GHz. The labels 2 × 10 or 2 × 20 indicate, respectively, two 10- or 20-µm-wide gate fingers, and T indicates a metal T gate. The drain and gate biases are 1.5 and 0.8 V, respectively.

Thus, the behavior of the input resistance and capacitance of silicided-gate MOSFETs can be explained by the distributed gate-resistance model proposed for the MOS capacitors. Because of the high gate resistance, the proportion of the MOSFET that can respond to the signal decreases with increasing frequency. As a result of the apparent narrowing gate, both R and C values decrease.

The gate resistance of a MOSFET is usually represented by a resistor in either a small-signal equivalent circuit or as an added external component in the BSIM model. Our results show that as long as the reactance of the gate capacitance X_c is moderately higher than the ohmic resistance of the gate at all frequencies of interest, this model is accurate. It implies that the maximum allowable operating frequency decreases as the square of the gate width. Above this frequency, an RC network representation is needed to represent the distributed nature of the gate. The accuracy of the model improves with increasing number of RC sections, but this will increase the simulation time and may become prohibitive for a large-scale circuit. Our study suggests that to accurately model the input of a wide-gate FET with high gate resistance, the FET can be broken up into several narrower parallel FETs with each unit satisfying the distributed-gate rule and being represented by a lumped gate resistance.

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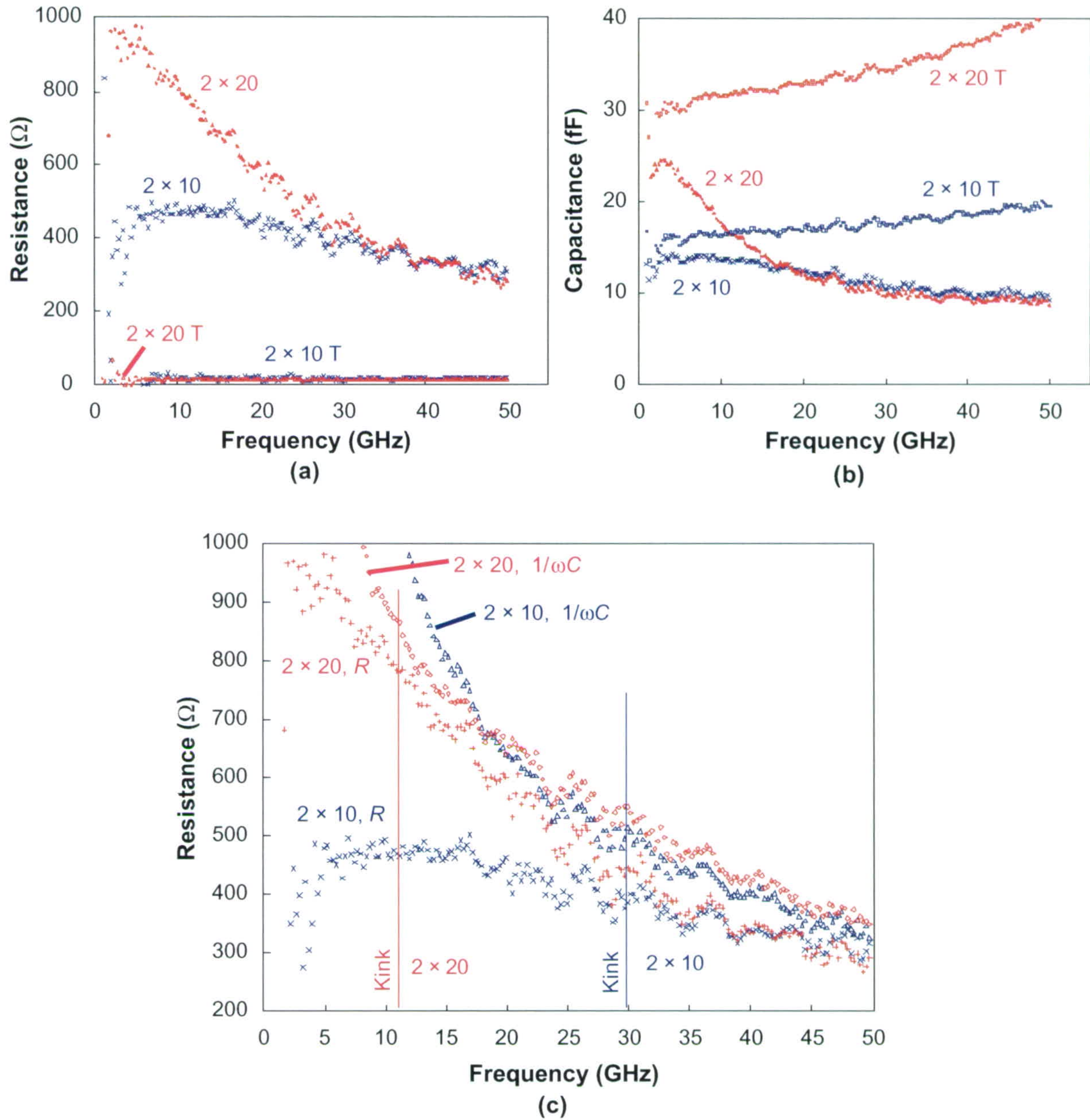

Figure 7-5. Input series resistance and capacitance values of n-MOSFET derived from measured S parameters: (a) resistance, (b) capacitance, and (c) reactance of input capacitance superimposed on input resistance. The vertical lines indicate the frequency of kinks in Figure 7-4.

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14. ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 February through 30 May 2004. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, DARPA, MDA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

15. SUBJECT TERMS

quantum electronics	biosensor technology	$AgGaSe_2$ wafer bonding	polymerase chain reaction
electro-optical devices	molecular technology	natural superlattices	charge-coupled devices
materials research	advanced imaging technology	optical lithography	communications technology
submicrometer technology	analog device technology	self-assembled monolayers	gate resistance characterization

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